

Schematics

DG645 Schematic Diagram List

Sheet	Description	Document
1	Motherboard Block Diagram and IO	DG_MB_BLOCK
2	Microcontroller	DG_MB_CPU
3	FPGA	DG_MB_FPGA
4	100 MHz Timebase	DG_MB_TIMEBASE
5	DDS and Trigger Selection	DG_MB_TRIG
6	Time to Amplitude Converter	DG_MB_TAC
7	T0-T1 Vernier Ramps	DG_MB_VERNIER_T01
8	AB Vernier Ramps	DG_MB_VERNIER_AB
9	CD Vernier Ramps	DG_MB_VERNIER_CD
10	EF Vernier Ramps	DG_MB_VERNIER_EF
11	GH Vernier Ramps	DG_MB_VERNIER_GH
12	Channel Logic for T0-T1 and End of Delay	DG_MB_CHANNEL_LOGIC_T01
13	Channel Logic for AB, CD	DG_MB_CHANNEL_LOGIC_ABCD
14	Channel Logic for EF, GH	DG_MB_CHANNEL_LOGIC_EFGH
15	GPIO	DG_MB_GPIO
16	Power Supply and IO	DG_MB_PSIO
17	Front Panel Keyboard & Displays	DG_FP1C
18	Power Supply	DG_PS1B
19	Output Driver Control	DG_DR1C
20	T0 Output Driver	DG_DR2C
21	AB Output Driver	DG_DR3C
22	CD Output Driver	DG_DR4C
23	EF Output Driver	DG_DR5C
24	GH Output Driver	DG_DR6C
25	Rear Panel 8-Channel Distribution	DG_RP1C
26	Rear Panel 8-Channel Outputs	DG_RP2C
27	HV Rear Panel Distribution	DG_HV1B
28	HV Rear Panel Outputs	DG_HV2B
29	Combo Rear Panel Distribution	DG_CB1B
30	Combo Rear Panel Outputs	DG_CB2B