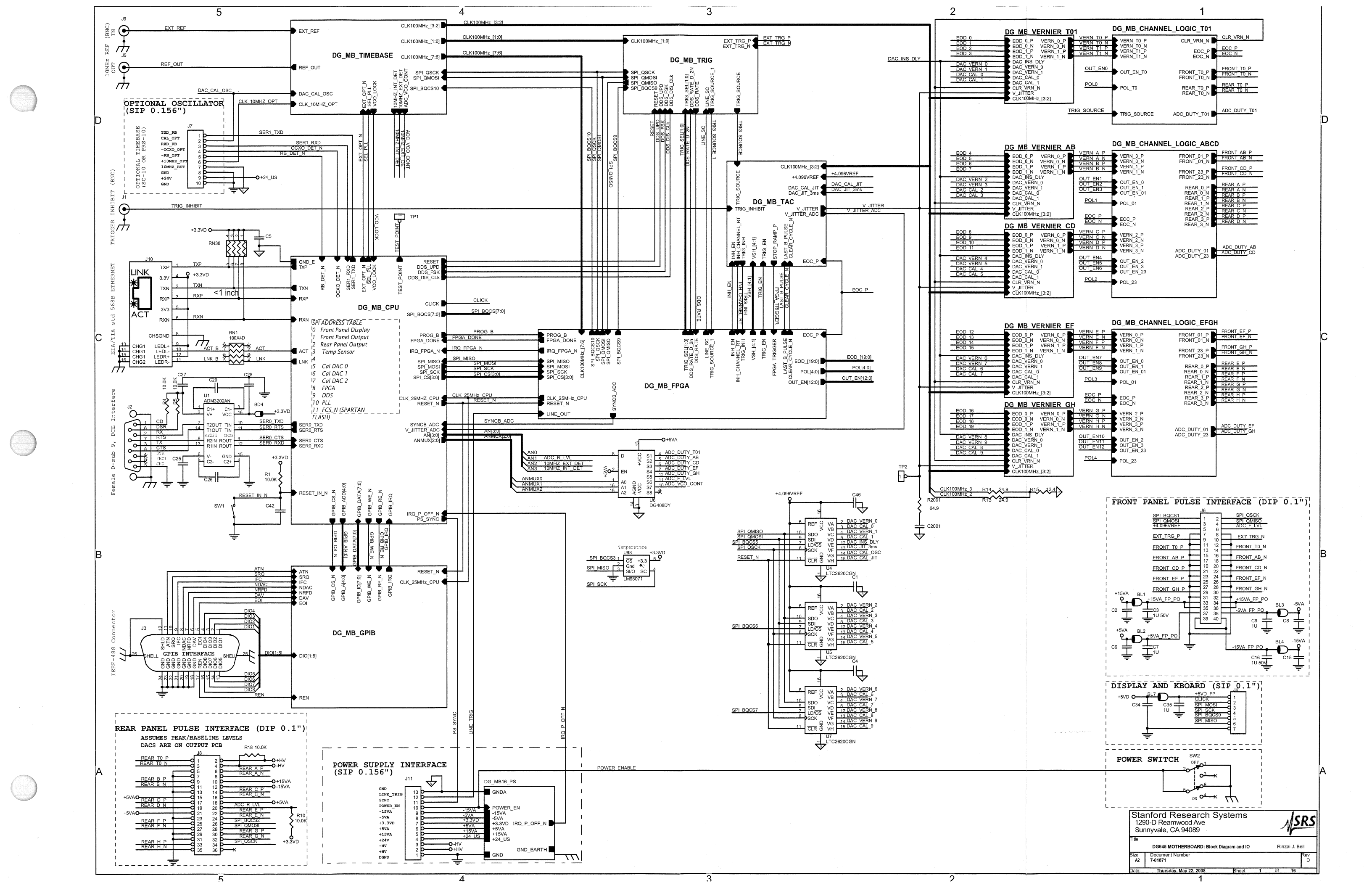
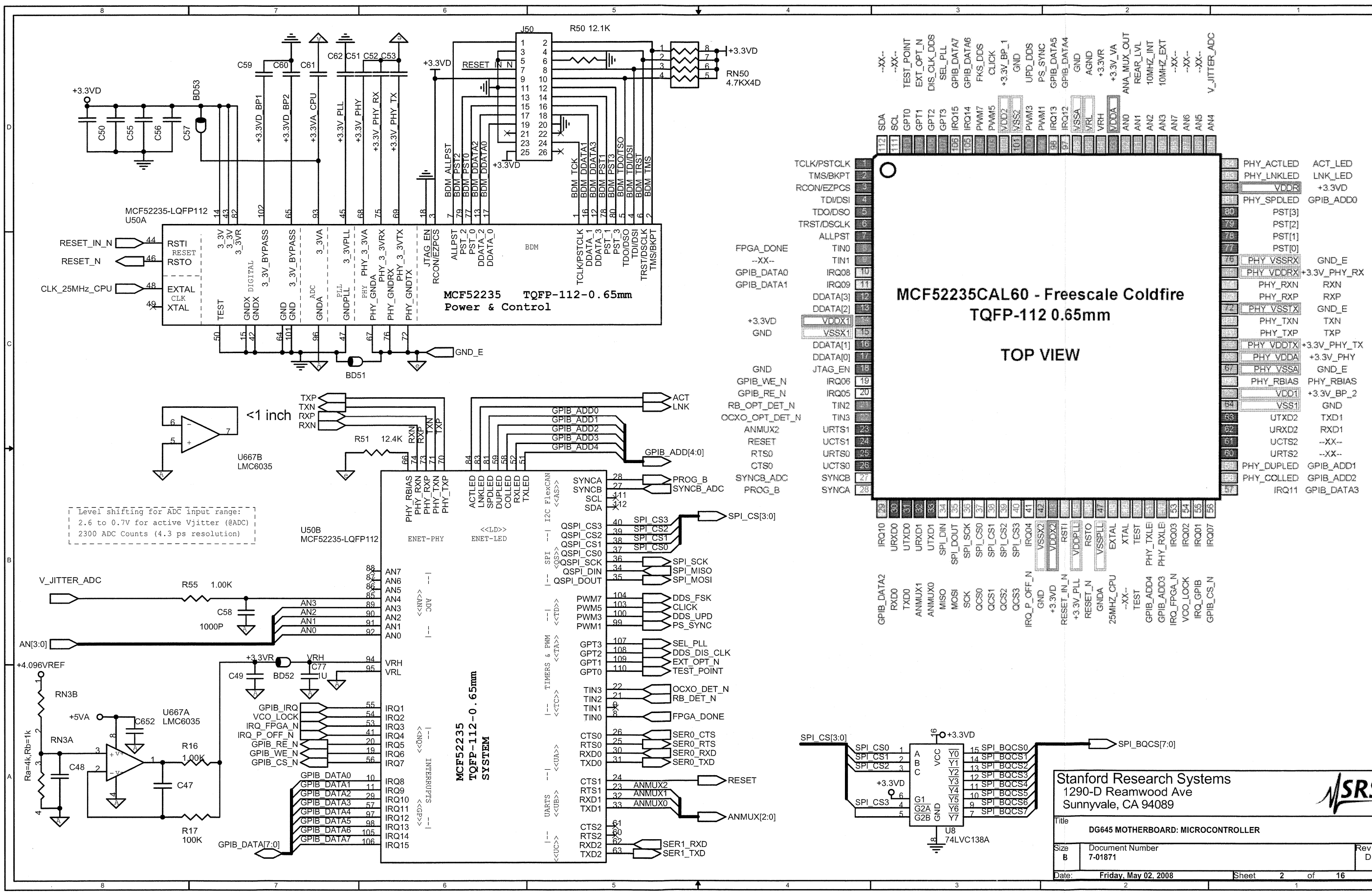

DG_MB_TIMEBASE
DG_MB_TRIG
DG_MB_TAC
DG_MB_CPU
DG_MB_FPGA
DG_MB_GPIB
DG_MB_VERNIER_T01
DG_MB_CHANNEL_LOGIC_T01
DG_MB_VERNIER_AB
DG_MB_CHANNEL_LOGIC_ABCD
DG_MB_VERNIER_CD
DG_MB_VERNIER_EF
DG_MB_CHANNEL_LOGIC_EFGH
DG_MB_VERNIER_GH
OPTIONAL OSCILLATOR (SIP 0.156")
REAR PANEL PULSE INTERFACE (DIP 0.1")
ASSUMES PEAK/BASELINE LEVELS
DACS ARE ON OUTPUT PCB
POWER SUPPLY INTERFACE (SIP 0.156")
FRONT PANEL PULSE INTERFACE (DIP 0.1")
DISPLAY AND KBOARD (SIP 0.1")
POWER SWITCH
SPI ADDRESS TABLE
0 Front Panel Display
1 Front Panel Output
2 Rear Panel Output
3 Temp Sensor
4
5 Cal DAC 0
6 Cal DAC 1
7 Cal DAC 2
8 FPGA
9 DDS
10 PLL
11 FCS_N (SPARTAN FLASH)
TRIGGER INHIBIT (BNC)
10MHz REF (BNC) IN OUT
EIA/TIA std 568B ETHERNET
Female D-sub 9, DCE Interface
IEEE-488 Connector
Stanford Research Systems
1290-D Reamwood Ave
Sunnyvale, CA 94089
DG645 MOTHERBOARD: Block Diagram and IO
Rinzal J. Bell
Document Number 7-01871
Rev D
Thursday, May 22, 2008
Sheet 1 of 16


MCF52235-LQFP112
U50A
MCF52235 TQFP-112-0.65mm
Power & Control
BDM
RESET_IN_N
RESET_N
CLK_25MHz_CPU
+3.3VD
BD53
BD51
GND_E
J50
R50 12.1K
RN50
4.7KX4D
MCF52235CAL60 - Freescale Coldfire
TQFP-112 0.65mm
TOP VIEW
<1 inch
U667B
LMC6035
R51 12.4K
U50B
MCF52235-LQFP112
ENET-PHY
ENET-LED
MCF52235
TQFP-112-0.65mm
SYSTEM
ACT
LNK
GPIB_ADD[4:0]
PROG_B
SYNCB_ADC
SPI_CS[3:0]
SPI_SCK
SPI_MISO
SPI_MOSI
DDS_FSK
CLICK
DDS_UPD
PS_SYNC
SEL_PLL
DDS_DIS_CLK
EXT_OPT_N
TEST_POINT
OCXO_DET_N
RB_DET_N
FPGA_DONE
SER0_CTS
SER0_RTS
SER0_RXD
SER0_TXD
RESET
ANMUX[2:0]
SER1_RXD
SER1_TXD
V_JITTER_ADC
R55 1.00K
C58
1000P
AN[3:0]
+4.096VREF
RN3B
RN3A
Ra=4k,Rb=1k
U667A
LMC6035
C652
C48
R16
1.00K
C47
R17
100K
GPIB_DATA[7:0]
+3.3VR
C49
BD52
C77
VRH
VRL
GPIB_IRQ
VCO_LOCK
IRQ_FPGA_N
IRQ_P_OFF_N
GPIB_RE_N
GPIB_WE_N
GPIB_CS_N
Level shifting for ADC input range:
2.6 to 0.7V for active Vjitter (@ADC)
2300 ADC Counts (4.3 ps resolution)
SPI_CS[3:0]
SPI_BQCS[7:0]
U8
74LVC138A
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DG645 MOTHERBOARD: MICROCONTROLLER
Size B
Document Number 7-01871
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U80B
SPARTAN 3E TQ144
SPARTAN 3E POWER
1.2/2.5/3.3V
2.5V
1.2V
VCCO_0
VCCO_1
VCCO_2
VCCO_3
VCCAUX
VCCINT
GND
XC3S250-4TQ144CS1
+2.5VD
+3.3VD
+1.2VD
C80 C94
22U 10V
U70 LP3878-ADJ
Vin
OFF
GND
Vout
ADJ
ByPs
R70 4.99K
C76
R71 3.32K
C17
C95 C96 C97 C98 C99
C81
U78 LP3879-1.2
Vout
SNS
C82 C83 C84 C85 C86
+1.2VD
C87
RN88
TRIG_SEL0
TRIG_SEL1
DDS_RATE_D_2n
VS2 = 1
VS1 = 1
VS0 = 1
R1000 4.22K
U72
M25PE20
SPROM_CLK
SPROM_MISO
SPROM_MOSI
SPROM_CS_N
C91
To U80.65
JTAG FPGA Programming
U80A
SPARTAN 3E TQ144
CCLK(O)
DIN_MISO(I)
MOSI (O)
CSO_B(O)
TCK
TDO
TDI
TMS
DONE
MODE
BUSY
M0 1
M1 0
M2 JTAG/SPI
INIT_B
PROG_B
HSWAP
J70
J1002
M2 4.99K
R75
R76 4.99K
R77 4.99K
FPGA_DONE
INIT_B
PROG_B
U80C
SPARTAN 3E TQ144
BANK 0
IO
IOD_P
IOD_N
OUT_EN12
OUT_EN11
OUT_EN10
OUT_EN9
OUT_EN8
OUT_EN7
OUT_EN6
OUT_EN5
OUT_EN4
OUT_EN3
OUT_EN2
OUT_EN1
OUT_EN0
SYNCB_ADC
GCLK9
GCLK8
RN84
RN85
RN86
4.7KX4D
R73 4.99K
R72 4.99K
CLR_EOD
BD72
U42B
U42A
SN74LVC74APW
C54
CLK100MHz_B1
CLK_25MHz_CPU
XC3S100E TQ144 / XC3S250E TQ144
Spartan 3E
XILINX
Bank 0
Bank 1
Bank 2
Bank 3
U80D
SPARTAN 3E TQ144
BANK 1
POL0
POL1
POL2
POL3
POL4
POL[4:0]
FEOD_0
FEOD_1
FEOD_2
FEOD_3
FEOD_4
FEOD_5
FEOD_6
FEOD_7
FEOD_8
FEOD_9
EOC_P
CLR_EOD
RN76 47X4D
U82
MAX9113-SOT
C79
CLK100MHz_[7:6]
CLK100MHz_7
CLK100MHz_6
CLK100MHz_B0
CLK100MHz_B1
U80E
SPARTAN 3E TQ144
BANK 2
LINE_SC
SPI_BQCS9
SPI_QSCK
TRIG_SEL[1:0]
DDS_RATE_D_2n
SPI_QMOSI
FPGA_TRIGGER
TRIG_INH
SPI_QMISO
TRIG_SOURCE_1
INH_CHANNEL_RT
DDS_RATE
U80F
SPARTAN 3E QF144
BANK 3
IRQ_FPGA_N
SPI_MISO
VSH_1
VSH_2
VSH_3
VSH_4
VSH_[4:1]
INH_EN
LAST_B_PULSE
CLEAR_CYCLE_N
TRIG_EN
SPI_BQCS10
SPI_MOSI
SPI_SCK
RESET_N
LINE_OUT
SPI_CS3
SPI_CS2
SPI_CS1
SPI_CS0
SPI_CS[3:0]
BD71
+2.5VD_EOD
FEOD_0
FEOD_1
FEOD_2
FEOD_3
FEOD_4
FEOD_5
FEOD_6
FEOD_7
FEOD_8
FEOD_9
U77
U81
U83
U84
U85
U71
U73
U74
U75
U76
SN74AUC1G74
PR
D
CK
CL
VCC
Q
GND
QE0D_0
QE0D_1
QE0D_2
QE0D_3
QE0D_4
QE0D_5
QE0D_6
QE0D_7
QE0D_8
QE0D_9
QE0D_10
QE0D_11
QE0D_12
QE0D_13
QE0D_14
QE0D_15
QE0D_16
QE0D_17
QE0D_18
QE0D_19
C78
C88
C89
C92
C93
RN70 150X4D
RN77 150X4D
RN78 150X4D
RN79 150X4D
RN80 150X4D
RN81 150X4D
RN83 150X4D
RN72 150X4D
RN74 150X4D
RN75 150X4D
EOD_0
EOD_1
EOD_2
EOD_3
EOD_4
EOD_5
EOD_6
EOD_7
EOD_8
EOD_9
EOD_10
EOD_11
EOD_12
EOD_13
EOD_14
EOD_15
EOD_16
EOD_17
EOD_18
EOD_19
EOD_[19:0]
+T0-+T1-+A-+B-+C-+D-+E-+F-+G-+H-
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Sunnyvale, CA 94089
SRS
Title
DG645 MOTHERBOARD: FPGA
Size
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Document Number
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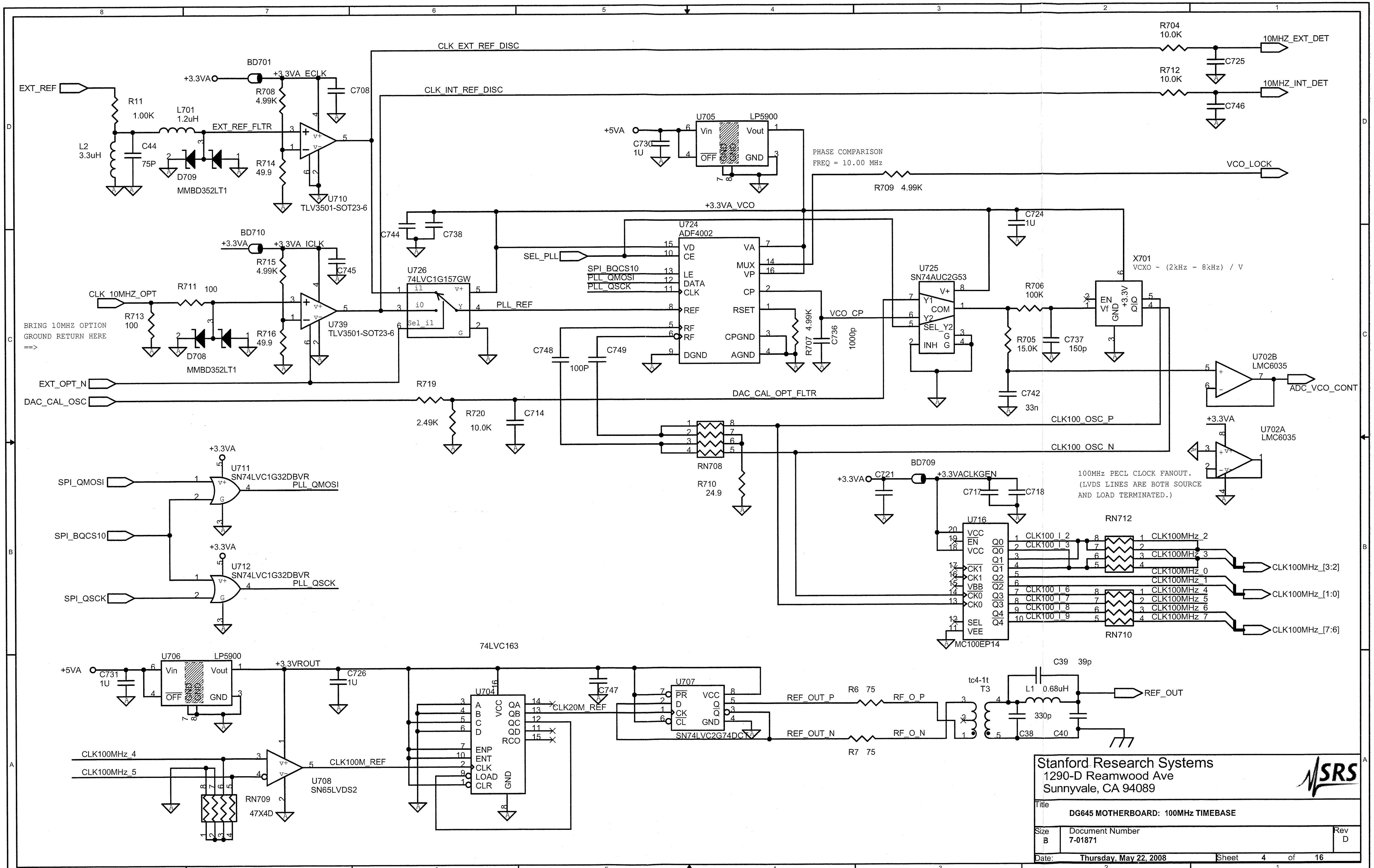
EXT_REF
CLK_10MHZ_OPT
BRING 10MHZ OPTION GROUND RETURN HERE ==>
EXT_OPT_N
DAC_CAL_OSC
CLK_EXT_REF_DISC
CLK_INT_REF_DISC
EXT_REF_FLTR
BD701
BD710
U710 TLV3501-SOT23-6
U739 TLV3501-SOT23-6
D709 MMBD352LT1
D708 MMBD352LT1
U726 74LVC1G157GW
PLL_REF
SEL_PLL
SPI_BQCS10
PLL_QMOSI
PLL_QSCK
U724 ADF4002
+3.3VA_VCO
U705 LP5900
PHASE COMPARISON
FREQ = 10.00 MHz
VCO_LOCK
VCO_CP
DAC_CAL_OPT_FLTR
U725 SN74AUC2G53
X701
VCXO ~ (2kHz - 8kHz) / V
U702B LMC6035
ADC_VCO_CONT
U702A LMC6035
10MHZ_EXT_DET
10MHZ_INT_DET
CLK100_OSC_P
CLK100_OSC_N
RN708
100MHz PECL CLOCK FANOUT.
(LVDS LINES ARE BOTH SOURCE AND LOAD TERMINATED.)
BD709
+3.3VACLKGEN
U716 MC100EP14
RN712
RN710
CLK100MHz_[3:2]
CLK100MHz_[1:0]
CLK100MHz_[7:6]
SPI_QMOSI
SPI_BQCS10
SPI_QSCK
U711 SN74LVC1G32DBVR
U712 SN74LVC1G32DBVR
U706 LP5900
+3.3VROUT
74LVC163
U704
CLK20M_REF
U707 SN74LVC2G74DCT
REF_OUT_P
REF_OUT_N
RF_O_P
RF_O_N
tc4-1t T3
REF_OUT
CLK100MHz_4
CLK100MHz_5
U708 SN65LVDS2
CLK100M_REF
RN709 47X4D

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Title	DG645 MOTHERBOARD: 100MHz TIMEBASE	
Size B	Document Number 7-01871	Rev D
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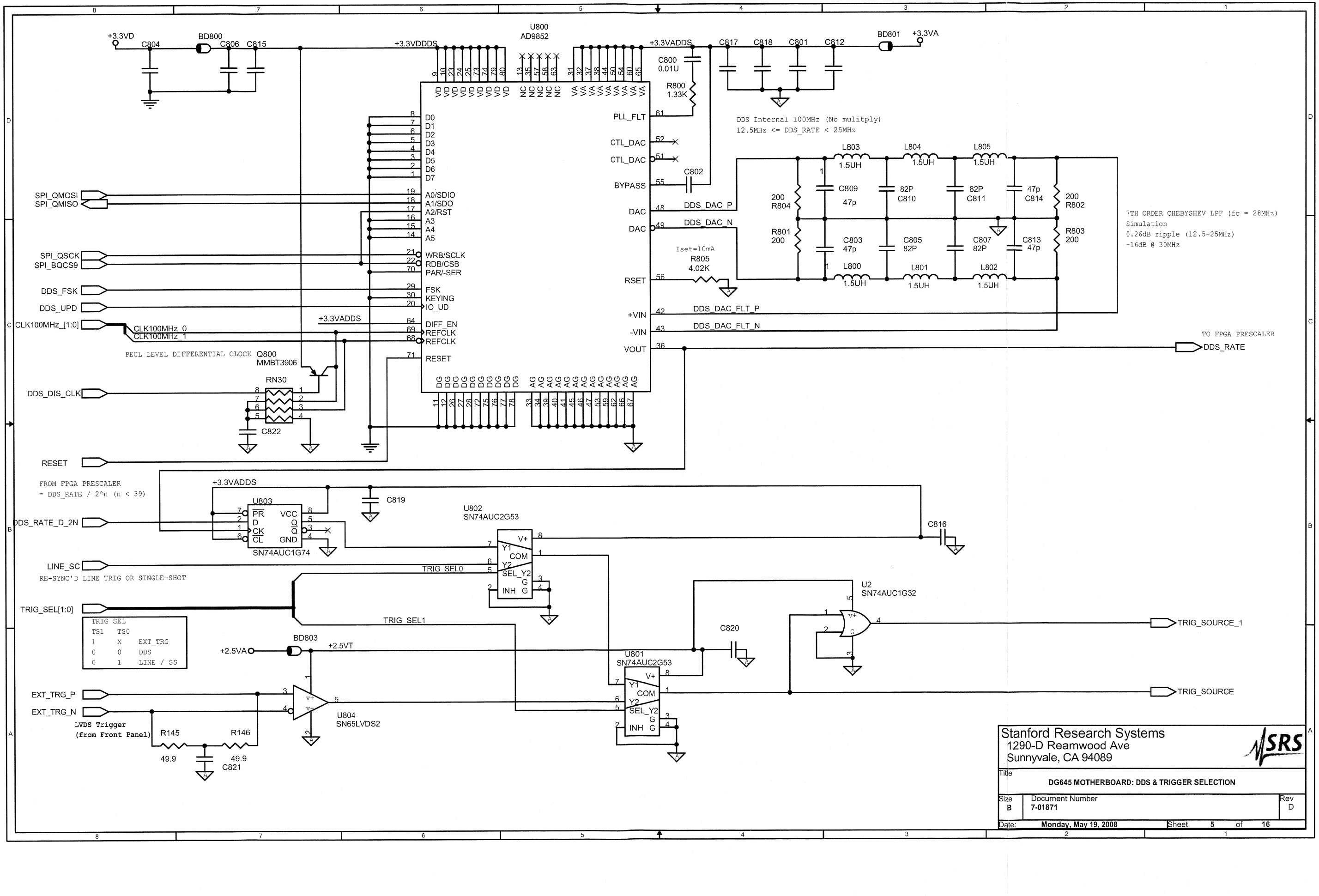
+3.3VD
C804
BD800
C806
C815
+3.3VDDS
U800
AD9852
+3.3VADDS
C817
C818
C801
C812
BD801
+3.3VA
C800
0.01U
R800
1.33K
PLL_FLT
CTL_DAC
CTL_DAC
BYPASS
DAC
DAC
RSET
+VIN
-VIN
VOUT
C802
DDS_DAC_P
DDS_DAC_N
R805
4.02K
Iset=10mA
DDS Internal 100MHz (No mulitply)
12.5MHz <= DDS_RATE < 25MHz
L803
L804
L805
1.5UH
200
R804
C809
47p
82P
C810
82P
C811
47p
C814
200
R802
R801
200
C803
47p
C805
82P
C807
82P
C813
47p
R803
200
L800
L801
L802
1.5UH
7TH ORDER CHEBYSHEV LPF (fc = 28MHz)
Simulation
0.26dB ripple (12.5-25MHz)
-16dB @ 30MHz
TO FPGA PRESCALER
DDS_RATE
DDS_DAC_FLT_P
DDS_DAC_FLT_N
D0
D1
D2
D3
D4
D5
D6
D7
A0/SDIO
A1/SDO
A2/RST
A3
A4
A5
WRB/SCLK
RDB/CSB
PAR/-SER
FSK
KEYING
IO_UD
DIFF_EN
REFCLK
REFCLK
RESET
SPI_QMOSI
SPI_QMISO
SPI_QSCK
SPI_BQCS9
DDS_FSK
DDS_UPD
CLK100MHz_[1:0]
CLK100MHz_0
CLK100MHz_1
PECL LEVEL DIFFERENTIAL CLOCK
Q800
MMBT3906
+3.3VADDS
RN30
DDS_DIS_CLK
C822
RESET
FROM FPGA PRESCALER
= DDS_RATE / 2^n (n < 39)
+3.3VADDS
U803
SN74AUC1G74
PR
D
CK
CL
VCC
Q
Q
GND
C819
DDS_RATE_D_2N
U802
SN74AUC2G53
V+
Y1
COM
Y2
SEL_Y2
G
INH
G
C816
LINE_SC
RE-SYNC'D LINE TRIG OR SINGLE-SHOT
TRIG_SEL0
TRIG_SEL[1:0]
TRIG SEL
TS1 TS0
1 X EXT_TRG
0 0 DDS
0 1 LINE / SS
TRIG_SEL1
U2
SN74AUC1G32
TRIG_SOURCE_1
BD803
+2.5VA
+2.5VT
C820
U801
SN74AUC2G53
TRIG_SOURCE
EXT_TRG_P
EXT_TRG_N
LVDS Trigger
(from Front Panel)
R145
R146
49.9
49.9
C821
U804
SN65LVDS2
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Sunnyvale, CA 94089
SRS
Title
DG645 MOTHERBOARD: DDS & TRIGGER SELECTION
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"START" MUST BE RE-SYNC'D TO AVOID METASTABILITY WRT THE REMOVAL OF THE CLR INPUT.

4ns DELAY

START JITTER RAMP SYCHRONOUSLY W/TRIG

PIPELINE DELAY & AVOID METASTABLE

STOP JITTER RAMP ON THE SECOND CLOCK AFTER TRIG.

BD602 BD606 +2.5VAJ +2.5VAJQ +2.5VA C616 C629 R610 4.99K

TRIG_EN INH_EN TRIG_INHIBIT RN605 1KX4D U615 TLV3501-SOT23-6

U627 SN74AUC1G08 U623 SN74AUC1G00 ARM U628 SN74AUC1G32

U644 SN74AUC1G74 C644 U643 SN65LVDS1 U642 SN65LVDS2 R662 100

C657 U641 SN74AUC1G74 START_RAMP

U665 SN74AUC1G74 U663 SN74AUC1G74 C607 STOP_RAMP_P STOP_RAMP_N

Synchronous Trigger Jitter : Ext Trig to Given Signal 8.x ps

PRE_START C605

TRIG_SOURCE CLK100MHz_[3:2] CLK100MHz_2 CLK100MHz_3 U664 SN65LVDS2 CLK100M

+2.5VA U630 SN74AUC1G08 CLEAR_CYCLE_N EOC_P LAST_B_PULSE U629 SN74AUC1G00

RESET AFTER LAST PULSE IN BURST.

B_CLEAR_CYCLE_N U645 SN74AUC1G74 INH_CHANNEL_RT

TRIG_INH TRIG_INH

BD621 +12VA +12VA_TTA C607 CLEAN +12VDC

C692 C690 1000P R682 147 C686 R668 249 C672 C671 R676 49.9K

RN622 4.7KX4D U602A LMC6035 DAC_CAL_JIT LMC6035 U602B R682 2.49K R678 49.9 Q619 MMBT3906

10mA Nominal

R665 75 R669 10 9.3V R667 10 75 R664 Pulse 9.30V 8.50V

+3.3VA C673 R671 24.9 Q614 R666 24.9 Q612B Q612A Q611 R673 24.9 +3.3VA STOP_RAMP_P

+3.3VA STOP_RAMP_N R672 200 C663 1000P R639 24.9 R677 422 R674 200

C650 R633 205K C641

Synchronous Trigger Jitter : Ext Trig to Given Signal 8.x ps

START_RAMP R661 499 U622 LM7171 D605 MMBD1701A R638 49.9 Vint U626 THS4631

100MHz Sensitive R645 1.00K C656 2.2P C651 100P V_guard GUARD RING

TP600 R670 V_JITTER_R R635 1.2 L600 470n

R652 1.00K C662 1.0P

+12VA_TTA U638 LM7171 D607 D606 MMBD1701A MMBD1701A

TEMP COMP FOR PRECHARGE DIODES IN V_JITTER & RAMP.

-15VA R603 49.9 -15VA_TTA C604

+4.096VREF R680 10.0K R675 11.3K

200 6.8 5.8 4.5 -3 ns 10 ns 20 ns

SAMPLE AND HOLD TIMING: ASSERT (ACTIVE LOW) AS SHOWN HERE:

VSH_[4:1] VSH_1 (PRETRIG TO 50us) VSH_2 (50us TO END_OF_CYCLE) VSH_3 (3ms TO END_OF_CYCLE) VSH_4

+4.096VREF DAC_JIT_3ms R687 2.26K U610B TLC072 VSH_4 VSH_3 U601C ADG1211

7.2V(0V DAC) to 5.4V (4.095V DAC)

R686 3.32K R685 1.00K

TWO-STAGE, LOW-DROOP SAMPLE & HOLD TO MAINTAIN V_JITTER FOR 2000S.

VSH_2 U601D ADG1211 U609B TLC072 VSH_1

VSJH R634 1.00K

U601E ADG1211

+12VA_TTA U610A TLC072 VSH_GUARD R679 200 VSJH_0 U601B ADG1211 VSH_1 VSH_4 U601A ADG1211 C628 3.3N

+4.096VREF R690 10.0K U609A TLC072 R693 2.15K V_JITTER_ADC R602 4.02K R691 1.00K R640 2.15K C691 220P

Level shifting for ADC input range:
0.7V to 5V
2.6 to 0.7V for active Vjitter (@ADC)
2300 ADC Counts (4.3 ps resolution)

V_JITTER STARTS AT ABOUT +4.5V AND RAMPS UP TO BETWEEN 5.5 & 6.5V.

V_JITTER

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Title: DG645 MOTHERBOARD: TIME TO AMPLITUDE CONVERTER

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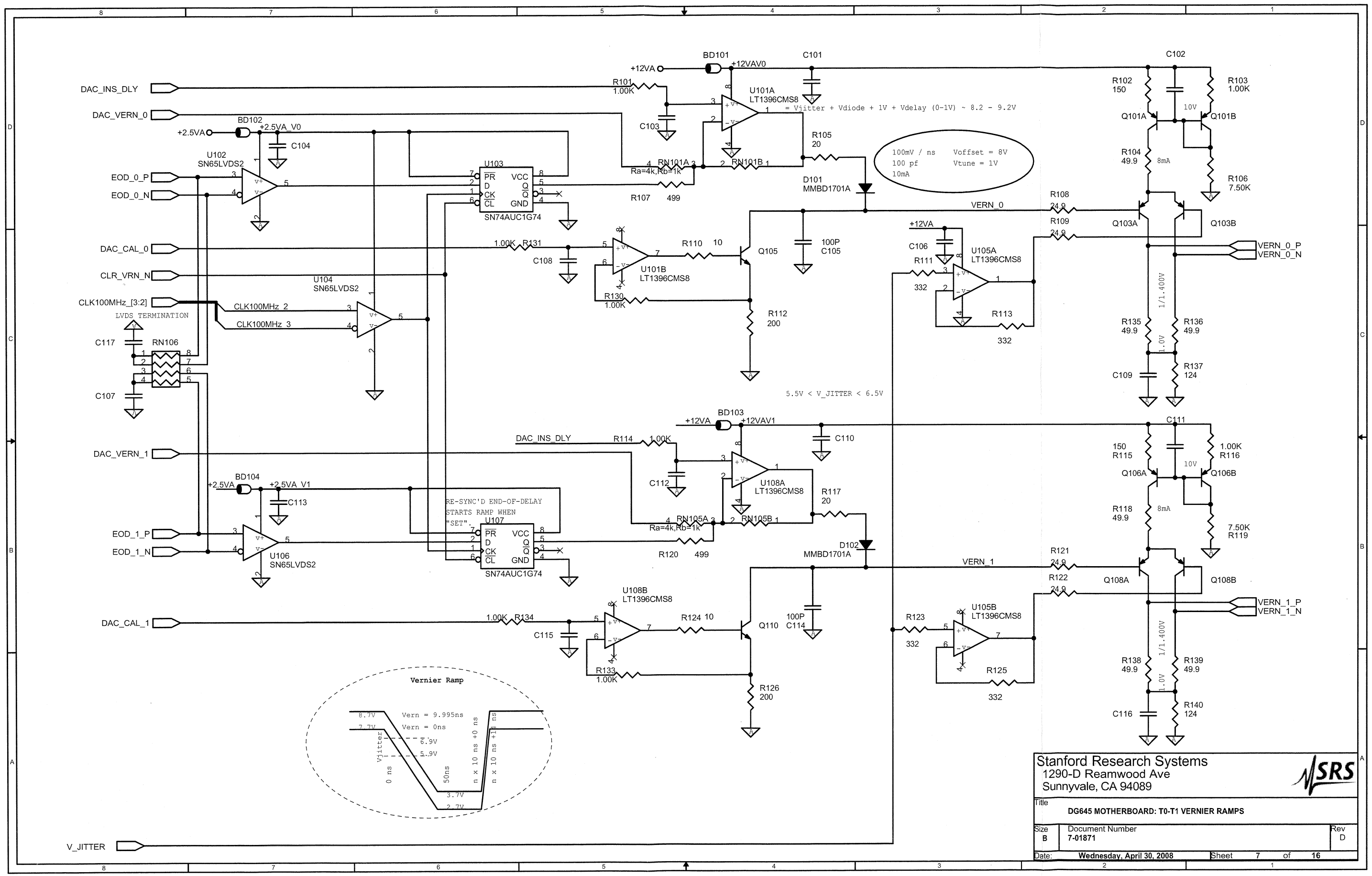

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Sunnyvale, CA 94089

Title: DG645 MOTHERBOARD: T0-T1 VERNIER RAMPS

Size	Document Number	Rev
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100mV / ns Voffset = 8V
100 pf Vtune = 1V
10mA

= Vjitter + Vdiode + 1V + Vdelay (0-1V) ~ 8.2 - 9.2V

Synchronous Trigger
Jitter : Ext Trig to Given Signal
8.x ps

Synchronous Trigger
Jitter : Ext Trig to Given Signal
12 ps

5.5V < V_JITTER < 6.5V

DAC_INS_DLY
DAC_VERN_0
DAC_CAL_0
CLR_VRN_N
CLK100MHz_[3:2]
EOD_0_P
EOD_0_N
DAC_INS_DLY
DAC_VERN_1
DAC_CAL_1
EOD_1_P
EOD_1_N
V_JITTER

+12VA
+2.5VA
BD201
BD202
BD203
BD204
+12VAV0
+12VAV1
+2.5VA_V0
+2.5VA_V1

R201 1.00K
C201
C202
C203
C204
C205
C206
C207
C208
C209
C210
C211
C212
C213
C215
C216
C217

U201A LT1396CMS8
U201B LT1396CMS8
U202 SN65LVDS2
U203 SN74AUC1G74
U204 SN65LVDS2
U205A LT1396CMS8
U205B LT1396CMS8
U206 SN65LVDS2
U207 SN74AUC1G74
U208A LT1396CMS8
U208B LT1396CMS8

RN201A
RN201B
Ra=4k,Rb=1k
R205 20
R207 499
D201 MMBD1701A
R210 10
Q205
R212 200
R230 1.00K
R231 1.00K

RN206
LVDS TERMINATION
CLK100MHz_2
CLK100MHz_3

RN205A
RN205B
Ra=4k,Rb=1k
R217 20
R220 499
D202 MMBD1701A
R224 10
Q210
R226 200
R233 1.00K
R234 1.00K

R202 150
R203 1.00K
R204 49.9
R206 7.50K
Q201A
Q201B
R208 24.9
R209 24.9
Q203A
Q203B
R211 332
R213 332
R235 49.9
R236 49.9
R237 124

R215 150
R216 1.00K
R218 49.9
R219 7.50K
Q206A
Q206B
R221 24.9
R222 24.9
Q208A
Q208B
R223 332
R225 332
R238 49.9
R239 49.9
R240 124

VERN_0
VERN_1
VERN_0_P
VERN_0_N
VERN_1_P
VERN_1_N

Vernier Ramp
8.7V
7.7V
Vern = 9.995ns
Vern = 0ns
Vjitter
6.9V
5.9V
0 ns
50ns
n x 10 ns +0 ns
n x 10 ns +1 ns
3.7V
2.7V

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Title: DG645 MOTHERBOARD: AB VERNIER RAMPS
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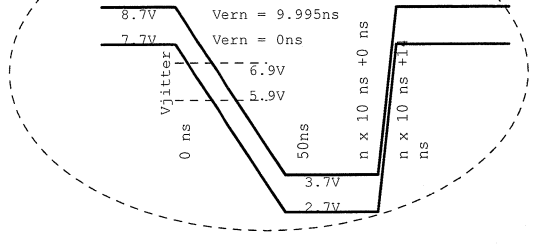
DAC_INS_DLY
DAC_VERN_0
EOD_0_P
EOD_0_N
DAC_CAL_0
CLR_VRN_N
CLK100MHz_[3:2]
LVDS_TERMINATION
C317
RN306
C307
BD302
+2.5VA
+2.5VA_V0
C304
U302
SN65LVDS2
U303
PR
D
CK
CL
VCC
Q
Q
GND
SN74AUC1G74
U304
SN65LVDS2
CLK100MHz_2
CLK100MHz_3
1.00K R331
C308
BD301
+12VA
+12VAV0
C301
R301
1.00K
C303
U301A
LT1396CMS8
= Vjitter + Vdiode + 1V + Vdelay (0-1V) ~ 8.2 - 9.2V
R305
20
RN301A
RN301B
Ra=4k,Rb=1k
R307 499
D301
MMBD1701A
100mV / ns Voffset = 8V
100 pf Vtune = 1V
10mA
U301B
LT1396CMS8
R310 10
Q305
100P
C305
R330
1.00K
200
R312
5.5V < V_JITTER < 6.5V
VERN_0
C302
R302
150
R303
1.00K
Q301A
Q301B
R304
49.9
R306
7.50K
R308
24.9
R309
24.9
Q303A
Q303B
VERN_0_P
VERN_0_N
R335
49.9
R336
49.9
C309
R337
124
+12VA
C306
R311
332
U305A
LT1396CMS8
R313
332
BD303
+12VA
+12VAV1
C310
R314 1.00K
C312
U308A
LT1396CMS8
R317
20
RN305A
RN305B
Ra=4k,Rb=1k
R320 499
D302
MMBD1701A
VERN_1
C311
R315
150
R316
1.00K
Q306A
Q306B
R318
49.9
R319
7.50K
R321
24.9
R322
24.9
Q308A
Q308B
VERN_1_P
VERN_1_N
R338
49.9
R339
49.9
C316
R340
124
U308B
LT1396CMS8
1.00K R334
C315
R324 10
Q310
100P
C314
R333
1.00K
R326
200
R323
332
U305B
LT1396CMS8
R325
332
DAC_INS_DLY
DAC_VERN_1
BD304
+2.5VA
+2.5VA_V1
C313
U306
SN65LVDS2
U307
PR
D
CK
CL
VCC
Q
Q
GND
SN74AUC1G74
DAC_CAL_1
V_JITTER

Vernier Ramp



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1290-D Reamwood Ave
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Title: DG645 MOTHERBOARD: CD VERNIER RAMPS

Size	Document Number	Rev
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Date: Wednesday, April 30, 2008 Sheet 9 of 16

DAC_INS_DLY
DAC_VERN_0
BD402
+2.5VA
+2.5VA_V0
C404
U402
SN65LVDS2
EOD_0_P
EOD_0_N
U403
PR
D
CK
CL
VCC
Q
Q
GND
SN74AUC1G74
DAC_CAL_0
CLR_VRN_N
CLK100MHz_[3:2]
LVDS TERMINATION
C417
RN406
C407
U404
SN65LVDS2
CLK100MHz_2
CLK100MHz_3
BD401
+12VA
+12VAV0
C401
R401
1.00K
C403
U401A
LT1396CMS8
= Vjitter + Vdiode + 1V + Vdelay (0-1V) ~ 8.2 - 9.2V
R405
20
RN401A
RN401B
Ra=4k,Rb=1k
R407
499
D401
MMBD1701A
100mV / ns
100 pf
10mA
Voffset = 8V
Vtune = 1V
VERN_0
1.00K R431
C408
R410
10
Q405
100P
C405
U401B
LT1396CMS8
R430
1.00K
R412
200
5.5V < V_JITTER < 6.5V
C402
R402
150
R403
1.00K
Q401A
Q401B
R404
49.9
R406
7.50K
R408
24.9
R409
24.9
Q403A
Q403B
+12VA
C406
R411
332
U405A
LT1396CMS8
R413
332
VERN_0_P
VERN_0_N
R435
49.9
R436
49.9
R437
124
C409
BD103
+12VA
+12VAV1
C410
R414
1.00K
C412
U408A
LT1396CMS8
R417
20
RN405A
RN405B
Ra=4k,Rb=1k
R420
499
D402
MMBD1701A
C411
R415
150
R416
1.00K
Q406A
Q406B
R418
49.9
7.50K
R419
VERN_1
R421
24.9
R422
24.9
Q408A
Q408B
VERN_1_P
VERN_1_N
BD404
+2.5VA
+2.5VA_V1
C413
U406
SN65LVDS2
EOD_1_P
EOD_1_N
U407
SN74AUC1G74
DAC_CAL_1
1.00K R434
C415
U408B
LT1396CMS8
R424
10
Q410
100P
C414
R433
1.00K
R426
200
R423
332
U405B
LT1396CMS8
R425
332
R438
49.9
R439
49.9
R440
124
C416
Vernier Ramp
8.7V
7.7V
6.9V
5.9V
3.7V
2.7V
Vjitter
0 ns
50ns
n x 10 ns +0 ns
n x 10 ns +1 ns
Vern = 9.995ns
Vern = 0ns
V_JITTER

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Title: DG645 MOTHERBOARD: EF VERNIER RAMPS

Size: B | Document Number: 7-01871 | Rev: D

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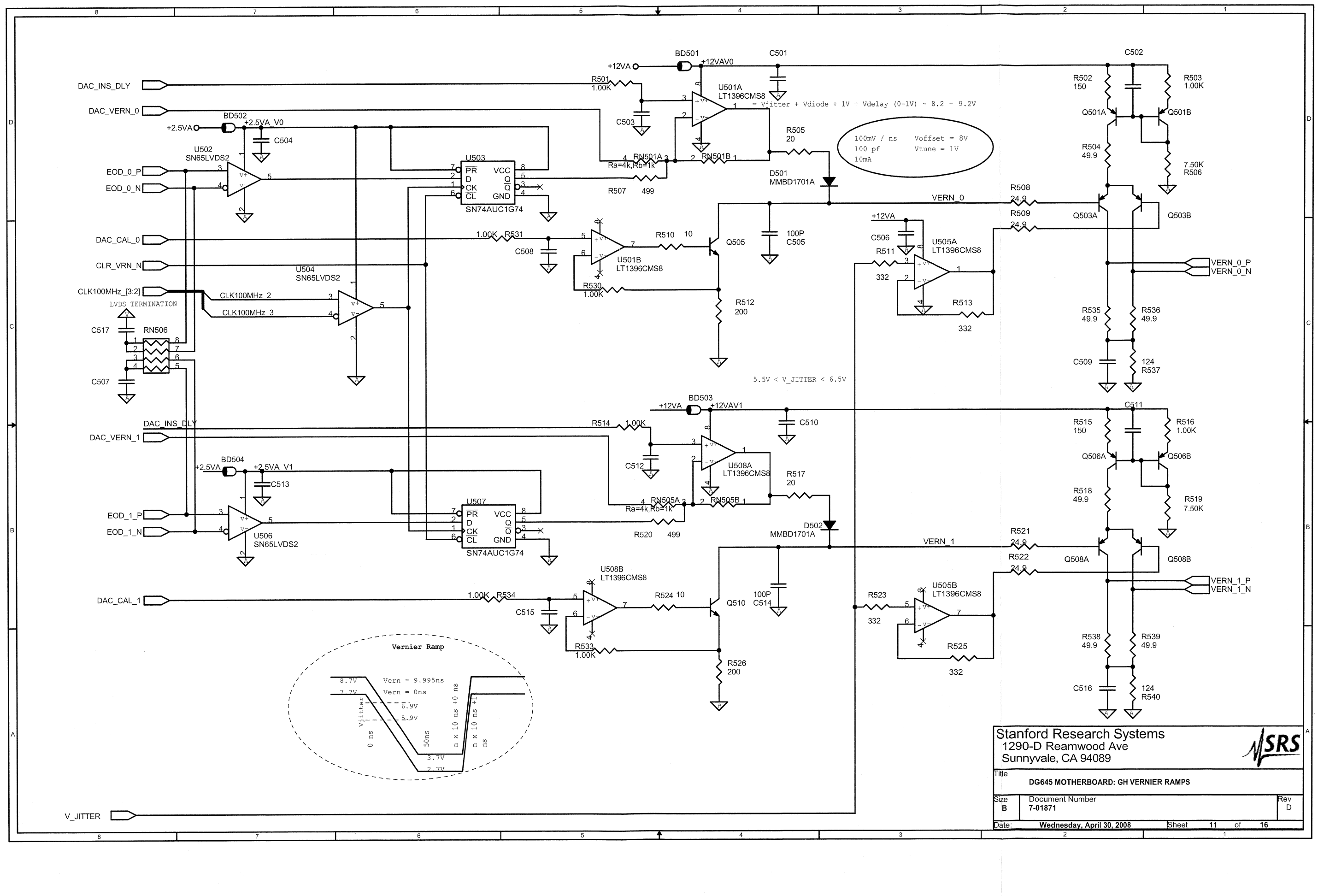
DAC_INS_DLY
DAC_VERN_0
EOD_0_P
EOD_0_N
DAC_CAL_0
CLR_VRN_N
CLK100MHz_[3:2]
LVDS TERMINATION
DAC_INS_DLY
DAC_VERN_1
EOD_1_P
EOD_1_N
DAC_CAL_1
V_JITTER
BD501
+12VA
+12VAV0
BD502
+2.5VA
+2.5VA_V0
BD503
+12VAV1
BD504
+2.5VA
+2.5VA_V1
U501A
LT1396CMS8
U501B
LT1396CMS8
U502
SN65LVDS2
U503
SN74AUC1G74
U504
SN65LVDS2
U505A
LT1396CMS8
U505B
LT1396CMS8
U506
SN65LVDS2
U507
SN74AUC1G74
U508A
LT1396CMS8
U508B
LT1396CMS8
= Vjitter + Vdiode + 1V + Vdelay (0-1V) ~ 8.2 - 9.2V
100mV / ns
100 pf
10mA
Voffset = 8V
Vtune = 1V
5.5V < V_JITTER < 6.5V
Ra=4k,Rb=1k
Ra=4k,Rb=1k
VERN_0
VERN_1
VERN_0_P
VERN_0_N
VERN_1_P
VERN_1_N
CLK100MHz_2
CLK100MHz_3
Vernier Ramp
8.7V
7.7V
Vern = 9.995ns
Vern = 0ns
Vjitter
6.9V
5.9V
0 ns
50ns
n x 10 ns +0 ns
n x 10 ns +1
ns
3.7V
2.7V
Stanford Research Systems
1290-D Reamwood Ave
Sunnyvale, CA 94089
Title
DG645 MOTHERBOARD: GH VERNIER RAMPS
Size
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Wednesday, April 30, 2008
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16

Note:
Calibration for TAC:
Set DDS to 1.000MHz (Sync trigger)
Set T1 to 1.5us
Set T0 to 1us - Tins - 10ns (produces 10ns pulse at U165.Q)
Adjust phase register in DDS to cross over phase (monitor Vjitter ADC)
Adjust Vjitter Cal for minimum deviation in T01_DUTY

For T0T1 cal use 1us/1.01us
Scan across 10ns boundary
Set CAL DAC to minimize deviation in T01_DUTY

+2.5VA
BD151
+2.5VAT0
C151
U151
SN65LVDS2
VERN_T0_P
VERN_T0_N
T0
U152
SN74AUC1G32
C152
U153
SN74AUC1G08
C153
U154
SN65LVDS1
REAR_T0_P
REAR_T0_N
OUT_EN_T0
POL_T0
U155
SN74AUC1G86
U156
SN65LVDS1
FRONT_T0_P
FRONT_T0_N
+2.5VA
TRIG_SOURCE
U12
SN74AUC1G02
U165
SN74AUC1G74
PR VCC
D Q
CK Q
CL GND
+3.3VA
R151
1.00K
C156
U159A
LMC6035
C166
1000P
ADC_DUTY_T01
U159B
LMC6035
R152
100K
R153
499
Duty Factor for Calibration:
Vout ~ 2.5V/ %

HIGH-SPEED, LOW-JITTER, 30NS ONE-SHOT TO GENERATE "END-OF-CYCLE"

+2.5VA
BD152
+2.5VAT1
C157
U163
SN65LVDS2
VERN_T1_P
VERN_T1_N
T1
U162
SN74AUC1G74
R155
249
U160
SN74AUC2G53
Y1
COM
Y2
SEL_Y2
INH G
82P
C159
R154
1.00K
C158
R156
1.00K
R157
4.99K
U161
SN65LVDS2
EOC_P
EOC_N
U166
SN74AUC1G32
CLR_VRN_N

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Title
DG645 MOTHERBOARD: END OF DELAY AND WAVEFORM CONDITIONING - T01

Size	Document Number	Rev
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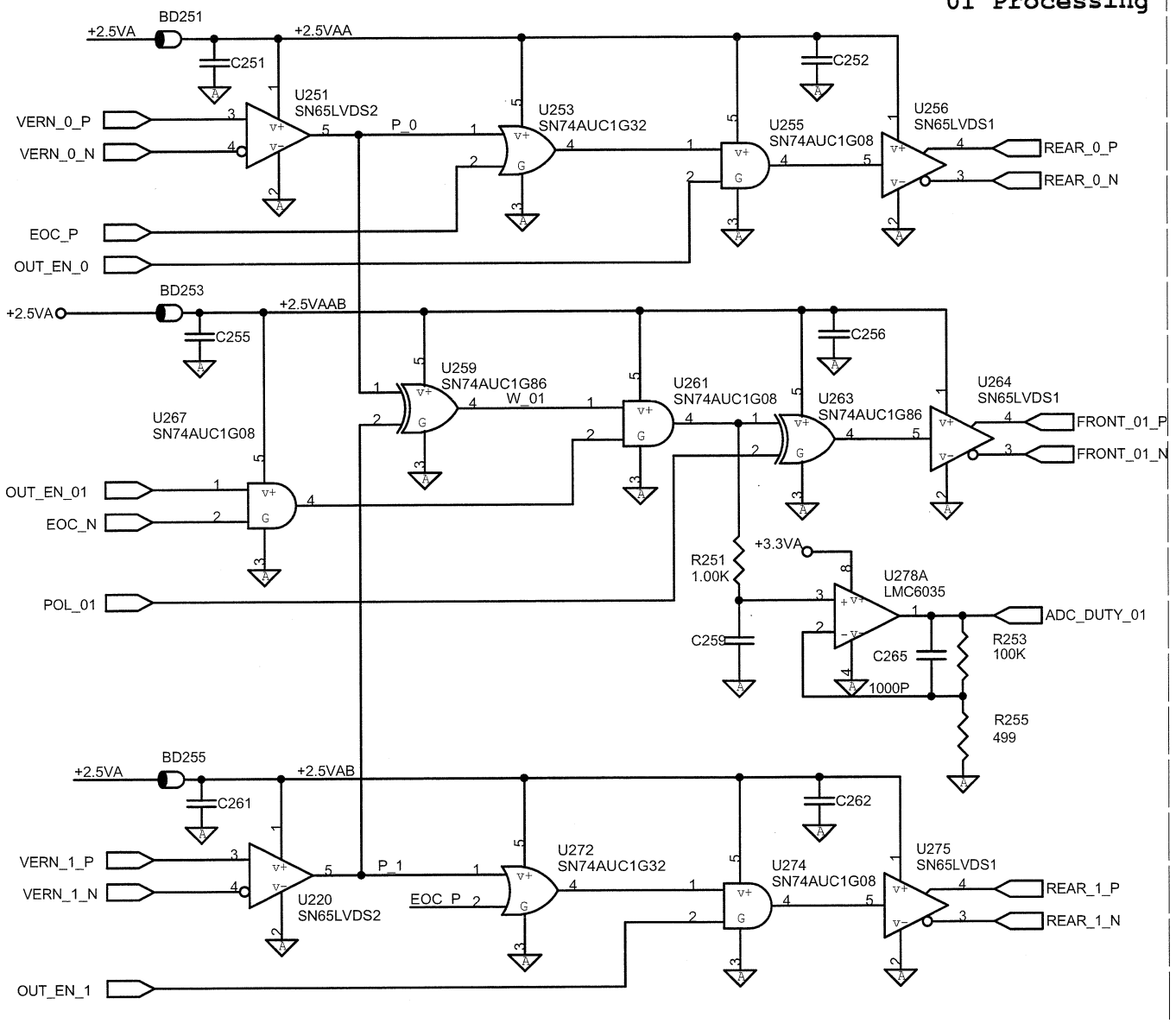
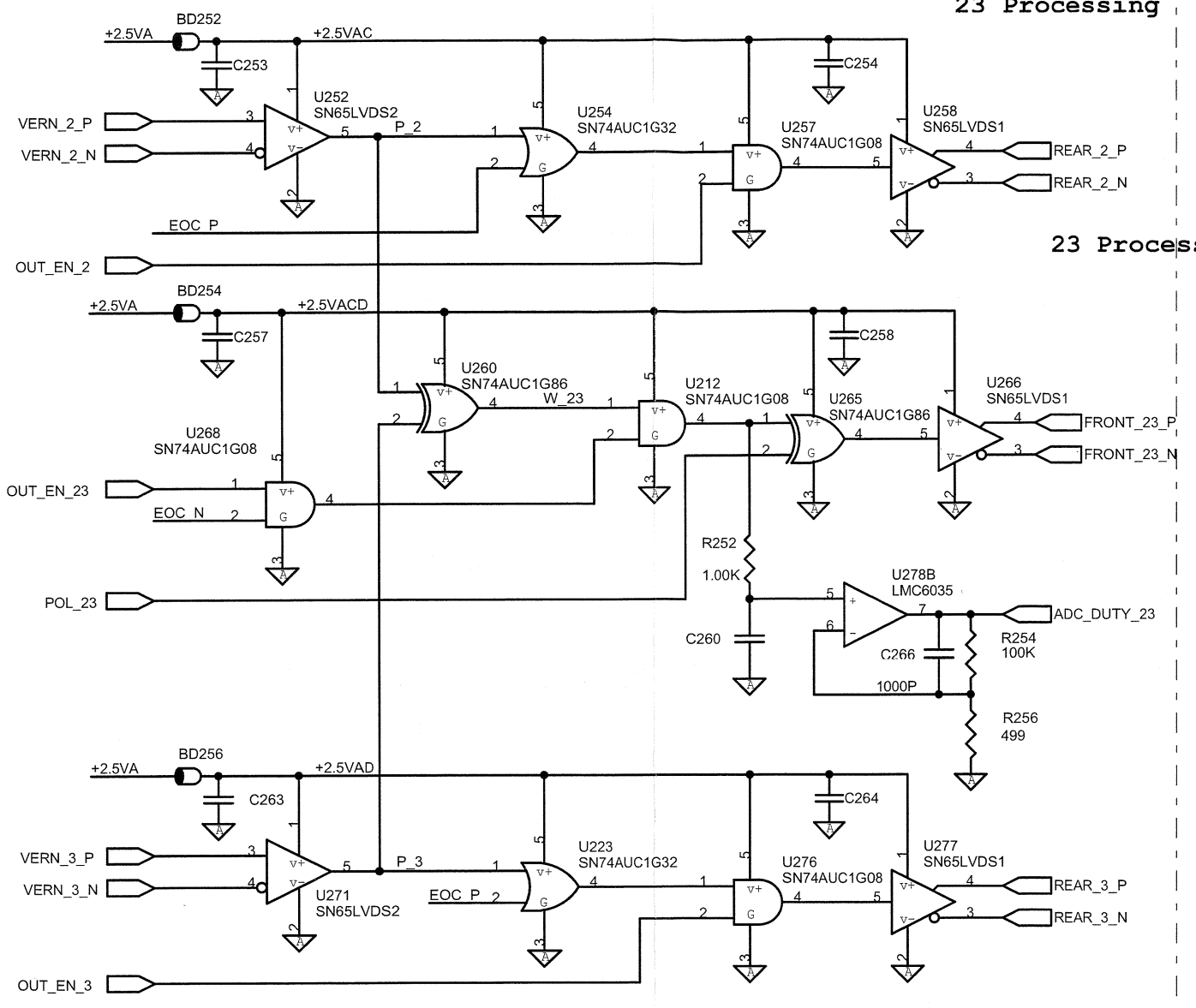
Date: Thursday, May 22, 2008 Sheet 12 of 16

01 Processing



23 Processing

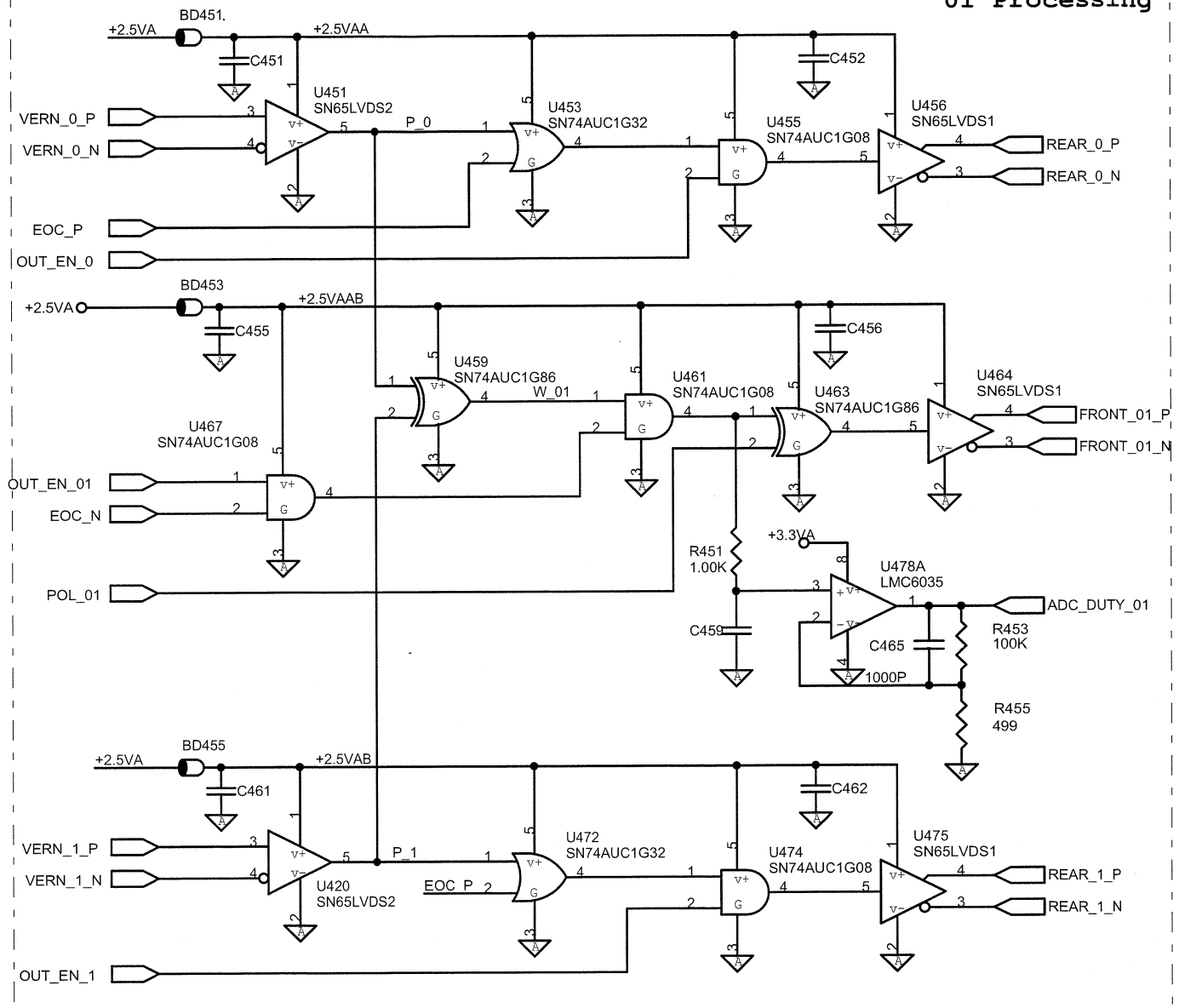


23 Processing

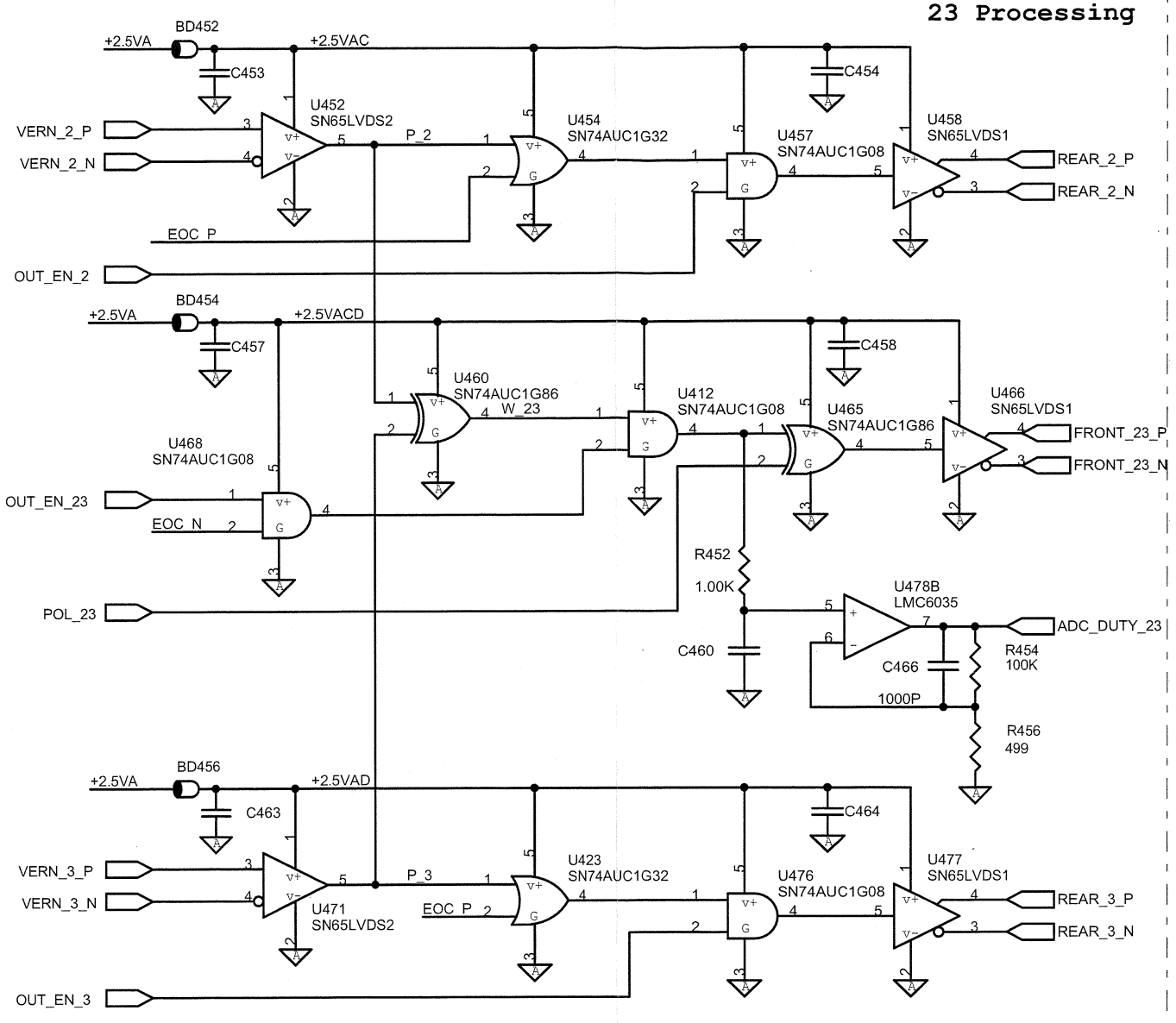
23 Processing

Stanford Research Systems 1290-D Reamwood Ave Sunnyvale, CA 94089		SRS
Title: DG645 MOTHERBOARD: WAVEFORM CONDITIONING - AB & CD		
Size: B	Document Number: 7-01871	Rev: D
Date: Wednesday, April 30, 2008	Sheet 13 of 16	

01 Processing



23 Processing



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Sunnyvale, CA 94089

Title: **DG645 MOTHERBOARD: WAVEFORM CONDITIONING - EF & GH**

Size	Document Number	Rev
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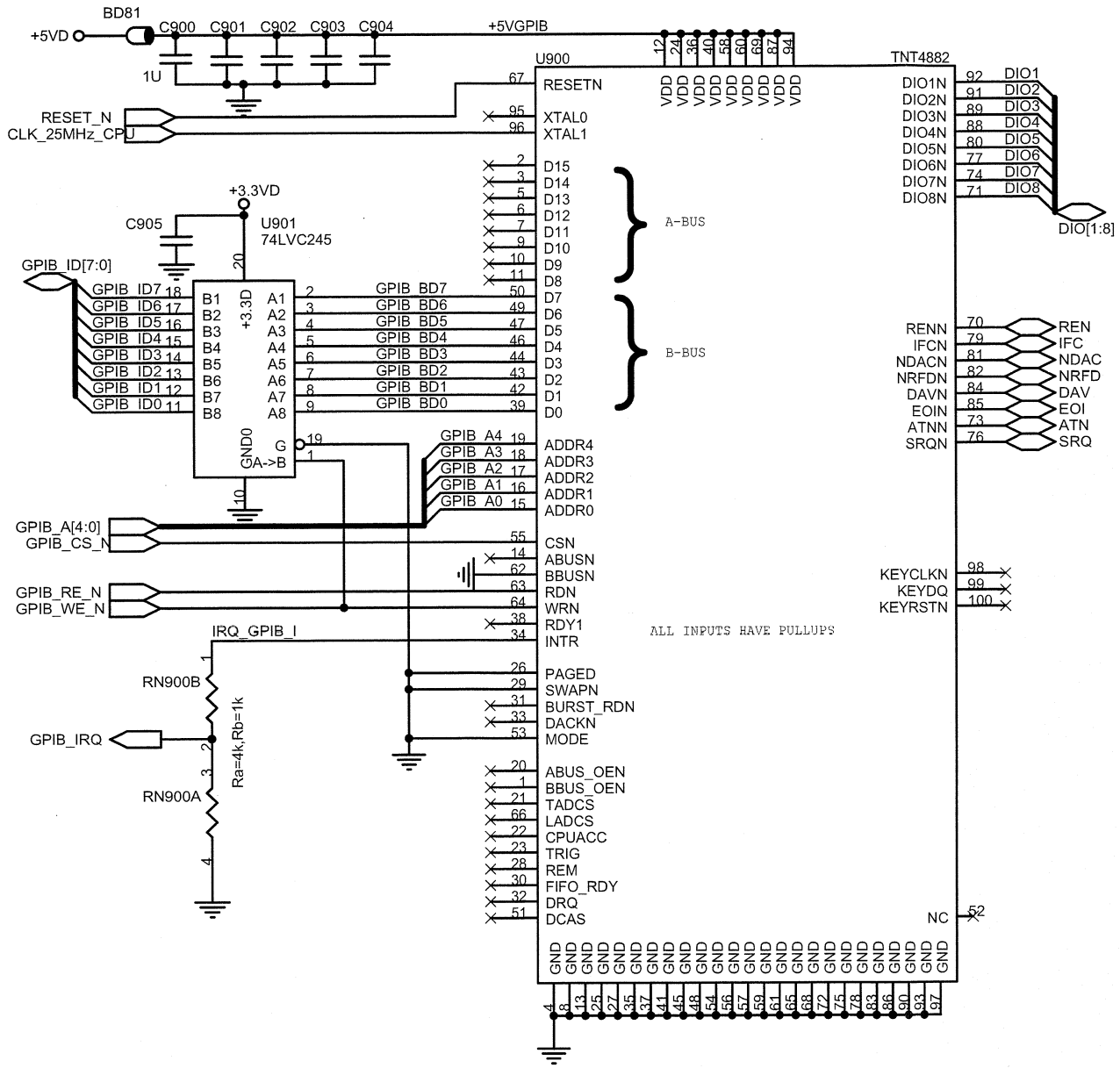
Date: **Wednesday, April 30, 2008** Sheet **14** of **16**



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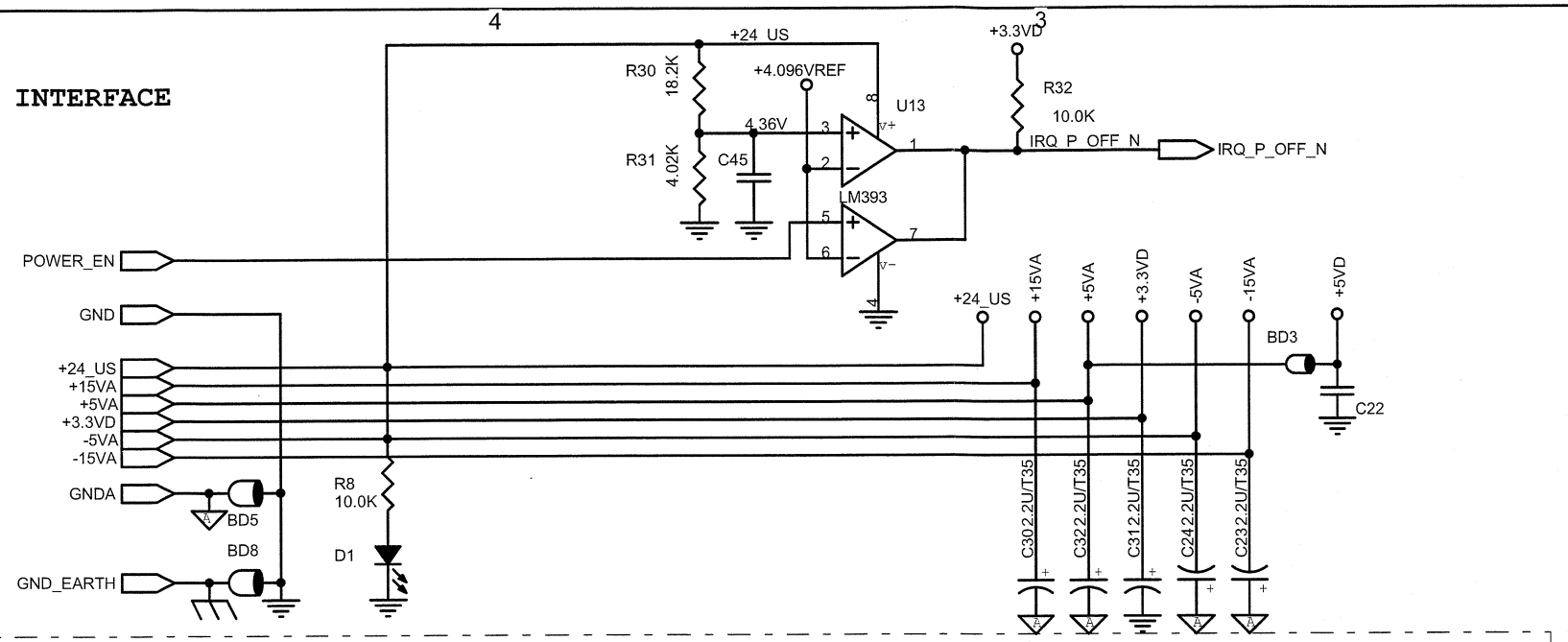
Title	DG645 DELAY GENERATOR: GPIB	
Size B	Document Number 7-01871	Rev D
Date: Thursday, June 05, 2008	Sheet 15 of 16	

POWER SUPPLY INTERFACE



REV B Changes

1: Net "2.5VA" @ BD803 => "+2.5VA"
2: FOOTPRINT FOR TLV3501 U615
3: PINOUT FOR MAX9913-SOT
4: SPI FLASH IO FOR FPGA
5: R668 changed to 249
6: TERMINATE VJITTER (64R AC)
7: Add Interrrupt on Power Enable
8: Add clear on all EOD ff (from T0/1)
9: Add Temp monitor
10: Modify Vjitter ADC Monitor and assign DAC channel for Digital Control
11: "SyncB" between FPGA & uP (ADC Trigger)
12: Added PowerDown Detection
13: Added RAW Trigger_Inhibit to FPGA
14: Removed 20MHz Osc - Added 3.3V 10MHz detectors

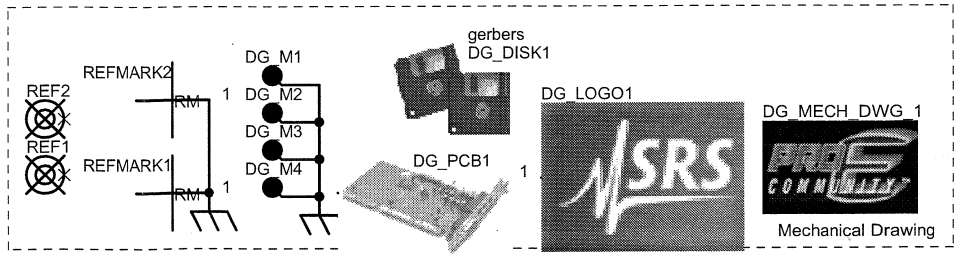
REV C Changes

1: Added 10K @ ADC_R_LVL to detect "no board"

REV D Changes

1: Changed all 1u 1206 C (V < 5V) to 0603/16V
2: Corrected RS232 & Oscillator part Numbers
3: Corrected DDS Filter layout
4: Moved BDM and JTAG connectors
5: Changed C628 to 3.3n PP
6: Changed c691 to 220p
7: Changed R638 to 49.9 & R675 to 11.3k
8: Changed (non)paired MMBT3640 to (M)MBT3906
9: Change C651 to 100pf NPO
10: Added L/R to comp Vjitter
11: Improved Shielding on C651 to reduce FR4 issues
12: Added 49.9k R for possible Vjitter Comp
13: Added series Rs between U626 and Guard ring
14: Rotated JTAG to reduce ambiguities with Display
15: Corrected RS232 xcvr footprint
16: Increased pads for CSP packages
17: Changed End of delay timing to 25 ns (C159 = 82 p)
18: Balance Heat disip in dif pair Q612
19: Added buffers for AD4002 SPI lines

NOTES:
1) All unmarked non-polarized caps are 0.1uF X7R 0603
2) All unmarked polarized caps are 2.2uF/tant/16V
3) All unmarked PNPs are dual MBT3906
4) All unmarked NPNs are MMBR5179
5) All unmarked RNs are 47x4D



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Title: **DG645 MOTHERBOARD: POWER SUPPLY IO**

Size	Document Number	Rev
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Date: Thursday, May 22, 2008 Sheet 16 of 16

3.3V TO 5.0V LEVEL TRANSLATION

SET STROBE BIT HIGH TO ENABLE 4 DIGITS, 8 LAMPS AND 6 KEYS.

EDGE | = | LINK | +/-1ks | SECONDS | MILLISECONDS | MICROSECONDS | NANOSECONDS | PICOSECONDS

FOR LOOP-BACK TEST

DISABLE LEDS IF -CS STOPS

STB4 DSPL PRMT

D1	RATE	-LAMP0
D2	THRES	-LAMP1
D3	B_DELAY	-LAMP2
D4	B_CNT	-LAMP3
D5	B_PER	-LAMP4
D6	DELAY	-LAMP5
D7	LEVEL	-LAMP6
D8	STATUS	-LAMP7

D41 BAL99LT1

SW1	TRIG_UP	KEY0
SW2	TRIG	KEY1
SW3	BURST	KEY2
SW4	DELAY	KEY3
SW5	LEVEL	KEY4
SW6	SHIFT	KEY5

STB3 TRIGGER

D9	TRIG'D	-LAMP0
D10	BURST	-LAMP1
D11	INT	-LAMP2
D12	+EXT	-LAMP3
D13	-EXT	-LAMP4
D14	SNGL	-LAMP5
D15	LINE	-LAMP6
D16	TRIG_ERR	-LAMP7

D42 BAL99LT1

SW7	TRIG_DN	KEY0
SW8	<EDGE	KEY1
SW9	EDGE>	KEY2
SW10	<LINK	KEY3
SW11	LINK>	KEY4
SW12	STORE	KEY5

STB2 STATUS

D17	TRIG_INH	-LAMP0
D18	T0	-LAMP1
D19	T1	-LAMP2
D20	A	-LAMP3
D21	B	-LAMP4
D22	C	-LAMP5
D23	D	-LAMP6
D24	SHIFT	-LAMP7

D43 BAL99LT1

SW13	BKSP	KEY0
SW14	RECALL	KEY1
SW15	7	KEY2
SW16	8	KEY3
SW17	9	KEY4
SW18	MOD_UP	KEY5

STB1

D25	E	-LAMP0
D26	F	-LAMP1
D27	G	-LAMP2
D28	H	-LAMP3
D29	Hz	-LAMP4
D30	SEC	-LAMP5
D31	V	-LAMP6
D32	STEP	-LAMP7

D44 BAL99LT1

SW19	0	KEY0
SW20	(.)	KEY1
SW21	+/-	KEY2
SW22	ENTER	KEY3
SW23	1	KEY4
SW24	2	KEY5

STB0

D33	EXT	-LAMP0
D34	ERR	-LAMP1
D35	REM	-LAMP2
D36	ACT	-LAMP3
D37	ERR	-LAMP4
D38	(RESERVED)	
D39	(RESERVED)	
D40	(RESERVED)	

D45 BAL99LT1

SW25	3	KEY0
SW26	4	KEY1
SW27	5	KEY2
SW28	6	KEY3
SW29	MOD_DN	KEY4
SW30	STEP	KEY5

STANFORD RESEARCH SYSTEMS

Title: DG645: FRONT PANEL KEYBOARD & DISPLAYS

Size: C | Document Number: DG_FP1C | REV: C

Date: April 30, 2008 | Sheet 1 of 1

LETHAL VOLTAGES ARE PRESENT WHENEVER INSTRUMENT IS CONNECTED TO AC LINE VOLTAGE!!!

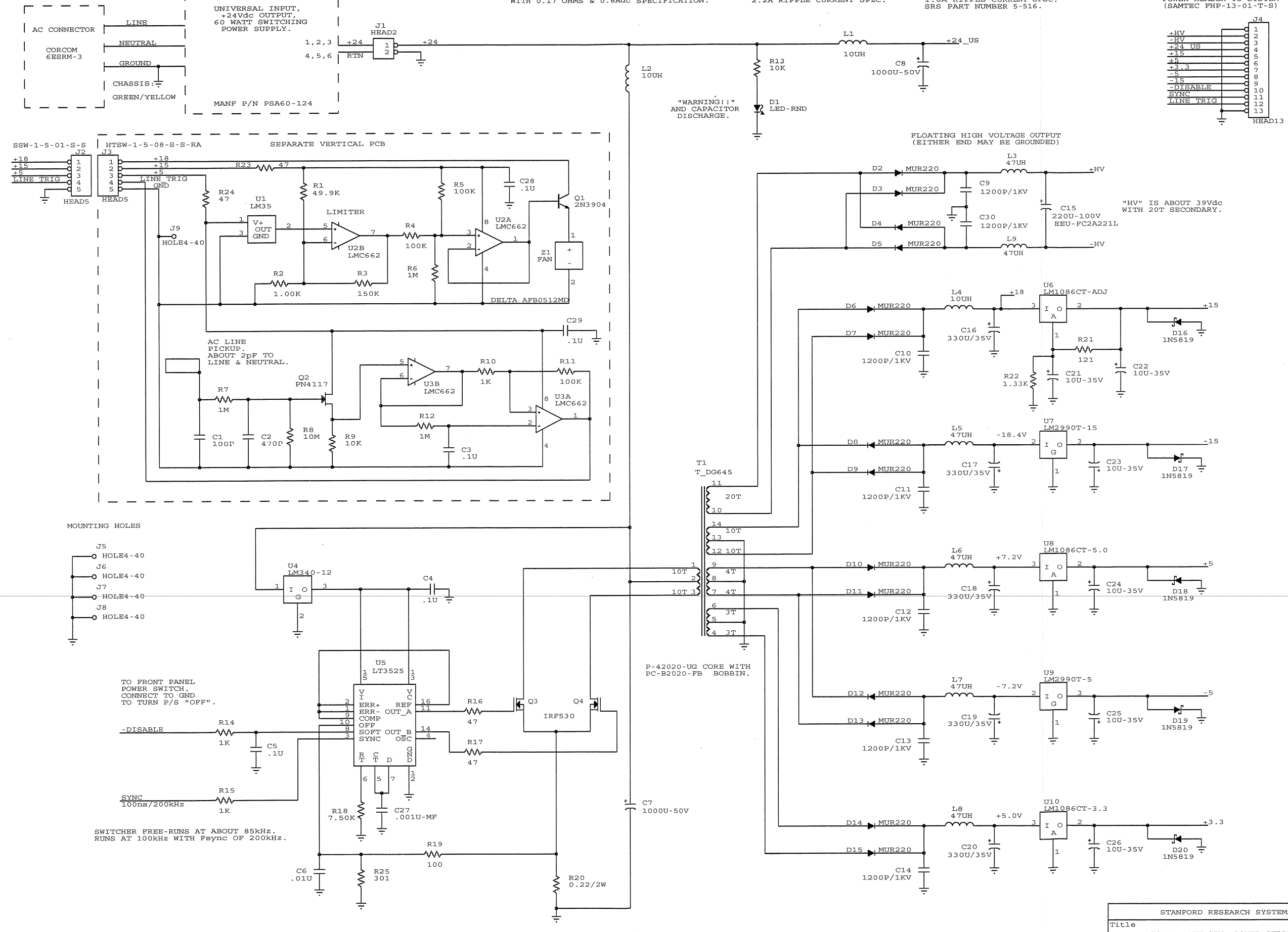
UNIVERSAL INPUT, +24Vdc OUTPUT POWER SUPPLY IS ALWAYS "ON".

10UH INDUCTORS ARE TOKO R622LY-100K WITH 0.045 OHMS & 2Adc SPECIFICATION.
47UH INDUCTORS ARE TOKO R622LY-470K WITH 0.17 OHMS & 0.8Adc SPECIFICATION.

1000UF-50V CAPACITORS ARE PANASONIC EEUPC1H102 WITH ESR=0.034 OHM AND 2.2A RIPPLE CURRENT SPEC.

330UF-35V CAPACITORS ARE PANASONIC EEUPC1V331 WITH ESR=0.068 OHM AND 1.0A RIPPLE CURRENT SPEC. SRS PART NUMBER 5-516.

POWER HEADER TO SYSTEM (SAMTEC FHP-13-01-T-S)



ALL OF THESE CIRCUITS ARE ENCLOSED IN A SEPARATE METAL ENCLOSURE INSIDE THE INSTRUMENT CHASSIS.

STANFORD RESEARCH SYSTEMS		
Title: DG645 DELAY GEN: POWER SUPPLIES		
Size: C	Document Number: DG_PS1B	REV: B
Date: July 12, 2007	Sheet 1 of 1	

EXT TRIG INPUT
Zin = 1M+22pF

J100
BNC

+4.096V
-4.096V
N100
4X1.0M
C100
33P
C101
27P

0-4.096V
R100
249
R101
10.0K
+5
L100
BEAD
C103
.1U
U100
TLV3501
U111
74LVC1G86
+3.3
C104
.1U
U101
SN65LVDS1

INTERFACE TO MOTHER-BOARD.
PIN #1 IS ON THE LEFT SIDE
(FACING FROM THE FRONT)
AND IS CLOSEST TO THE FRONT.

J101
HEAD40

-CS/LD
SPI CLK
SPI DI
SPI DO
VREF
OUT MON
+TRIG
-TRIG
+T0
-T0
+AB
-AB
+CD
-CD
+EF
-EF
+GH
-GH
+5
-5
+15
-15

L101
BEAD
C105
.1U
C106
4.7U/25V
C107
.1U
C108
.1U
C109
.1U
L102
BEAD
C110
4.7U/25V

U102
74HCT595A
VCC SI CLK CLR RCK OE GND
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 SO

MULTIPLEXER TO MONITOR OUTPUT LEVELS.

U103
74HC4051
TO MON
AB MON
CD MON
EF MON
GH MON
X0 X1 X2 X3 X4 X5 X6 X7
VCC
A B C
INH
GND
VEE
C116
.1U
C117
.1U
U104A
LMC6492
R102
200
R103
806
SCALE 4.096 TO 3.3V

L103
BEAD
U108
LM317
I O A
C111
4.7U/25V
R107
124
C119
4.7U/35V
R109
200
C120
4.7U/35V
+10.0V
C112
4.7U/25V
R108
866
R110
124
IAO
+6.7V
U109
LM337
NEGATIVE REGULATOR:
CURRENT SINK AT 6.7V
REFERENCED TO +10.0V.

U110
LP2985AIM5-3.3
VIN OUT EN C GND
C121
4.7U/25V
C122
.1U
C123
4.7U/25V
+3.3

C114
.1U
OCTAL 12-BIT DAC FOR
OUTPUT AMPLITUDES.
U106
LTC2620
VCC REF CLR CS SCK SDI GND
VA VB VC VD VE VF VG VH SDO
+4.096V
T0 AMPL
AB AMPL
CD AMPL
EF AMPL
GH AMPL
TRIG LVL
DAC1 TST
OFFS_REF

OCTAL 12-BIT DAC FOR
OUTPUT OFFSET CONTROL.

REFERENCE FOR OFFSET DAC
IS SET TO 4.095V AFTER
ALL THE OFFSET DACs ARE SET.

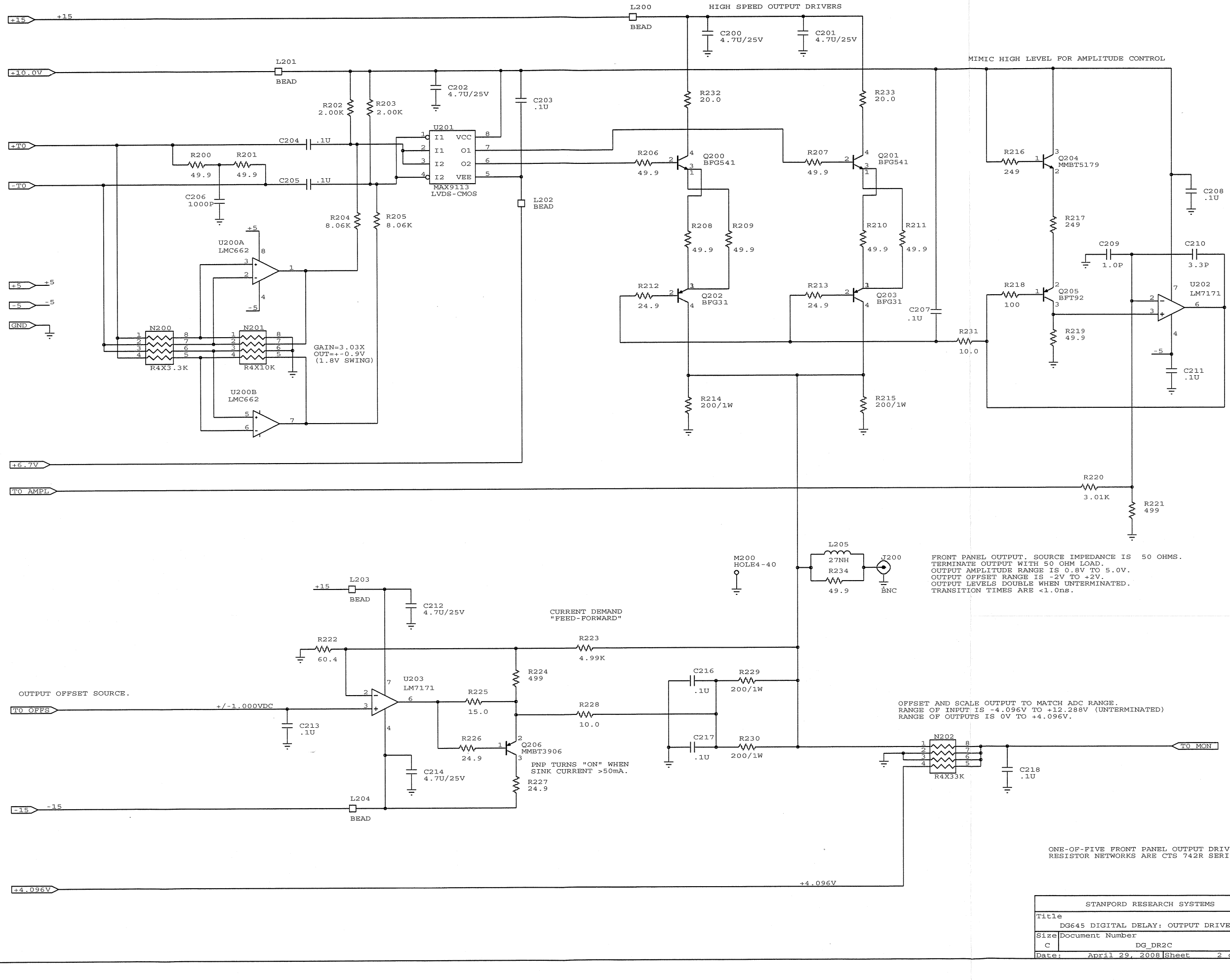
C115
.1U
U107
LTC2620
DAC2 TST
SPARE_DAC

U112
74LVC1G125
IVO
EG
TRISTATE AND CONVERT TO 3.3V

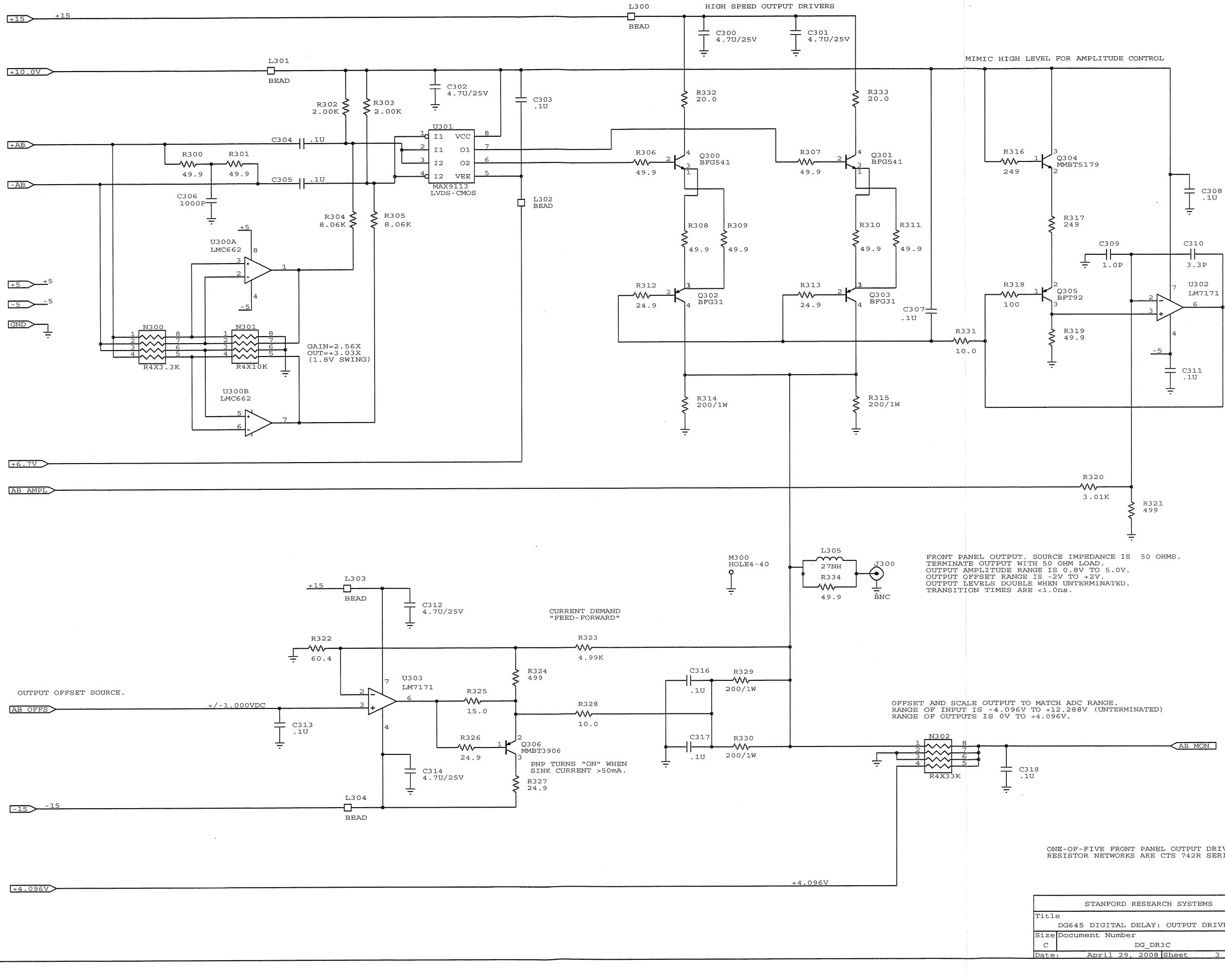
R104
100K
C118
.1U
U105A
LMC6492
+4.096V
R105
10.0K
R106
10.0K
U105B
LMC6492
-4.096V

N101
N102
N103
4X10K
T0 OFFS
AB OFFS
CD OFFS
EF OFFS
GH OFFS
COMMON OUTPUT OFFSET.
(SET TO -2.000VDC)
U104B
LMC6492

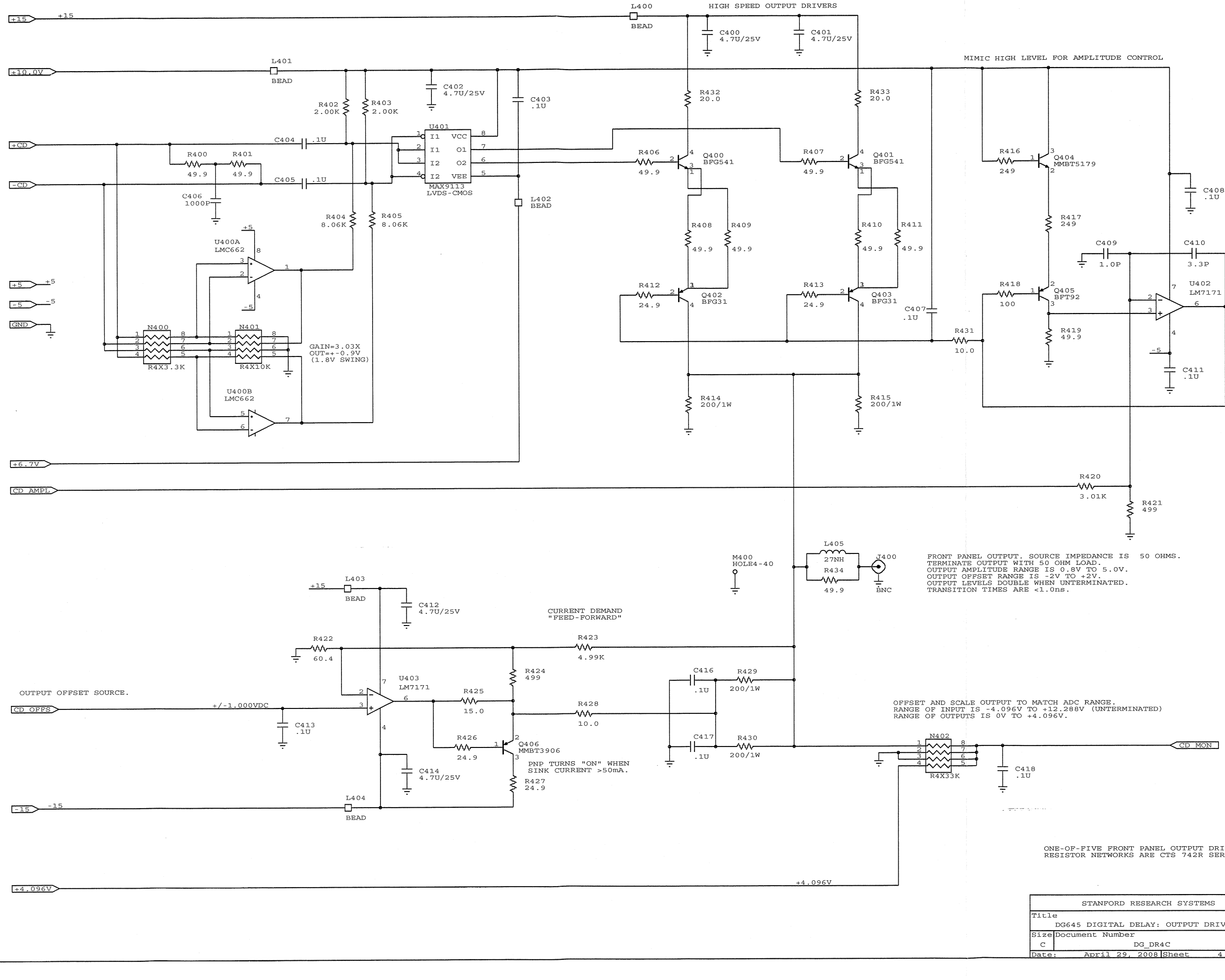
STANFORD RESEARCH SYSTEMS		
Title: DG645 DIGITAL DELAY: OUTPUT DRIVER CONTROL		
Size: C	Document Number: DG_DR1C	REV: C
Date: April 29, 2008	Sheet 1 of 6	



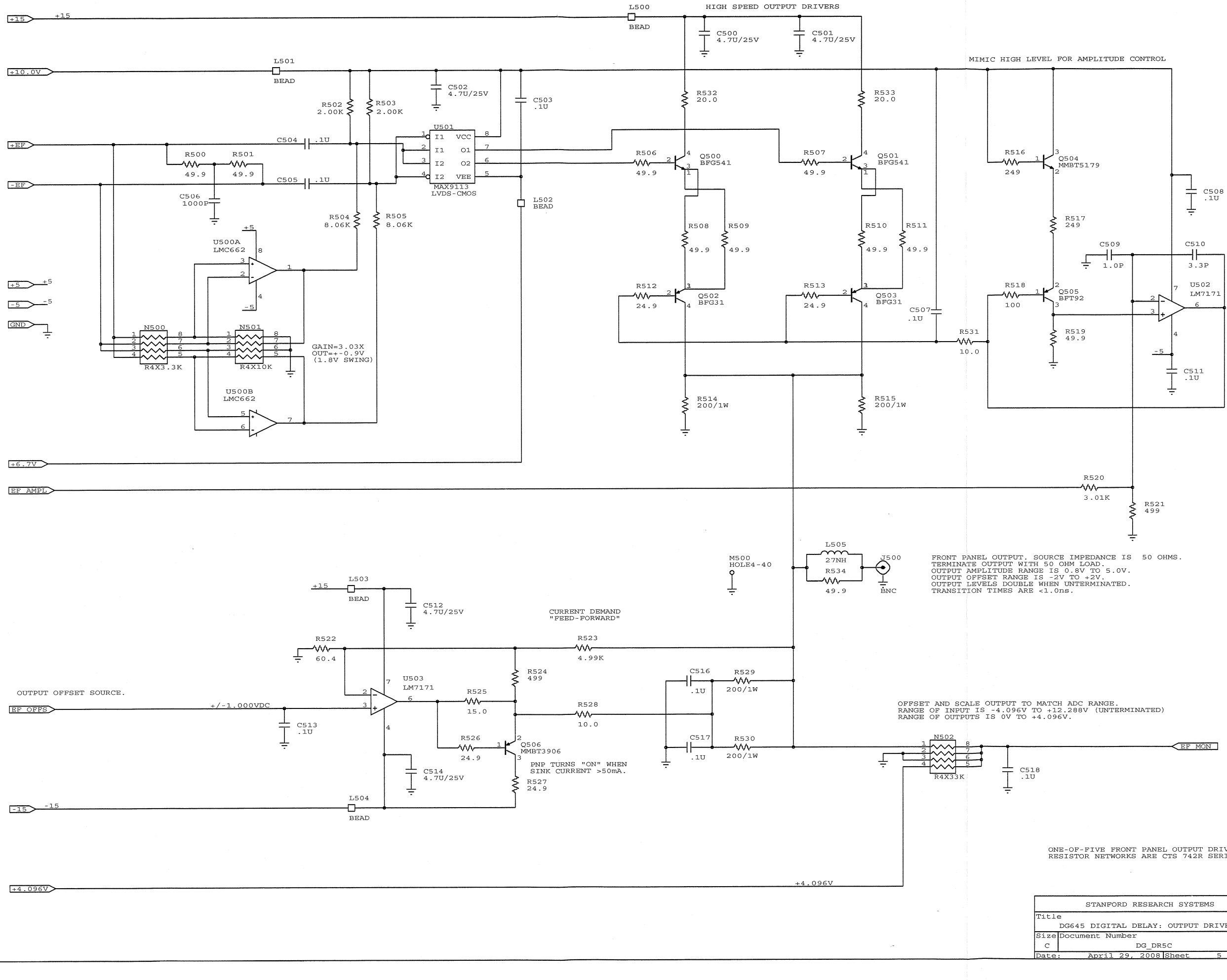
STANFORD RESEARCH SYSTEMS		
Title: DG645 DIGITAL DELAY: OUTPUT DRIVERS		
Size: C	Document Number: DG_DR2C	REV: C
Date: April 29, 2008	Sheet 2 of 6	



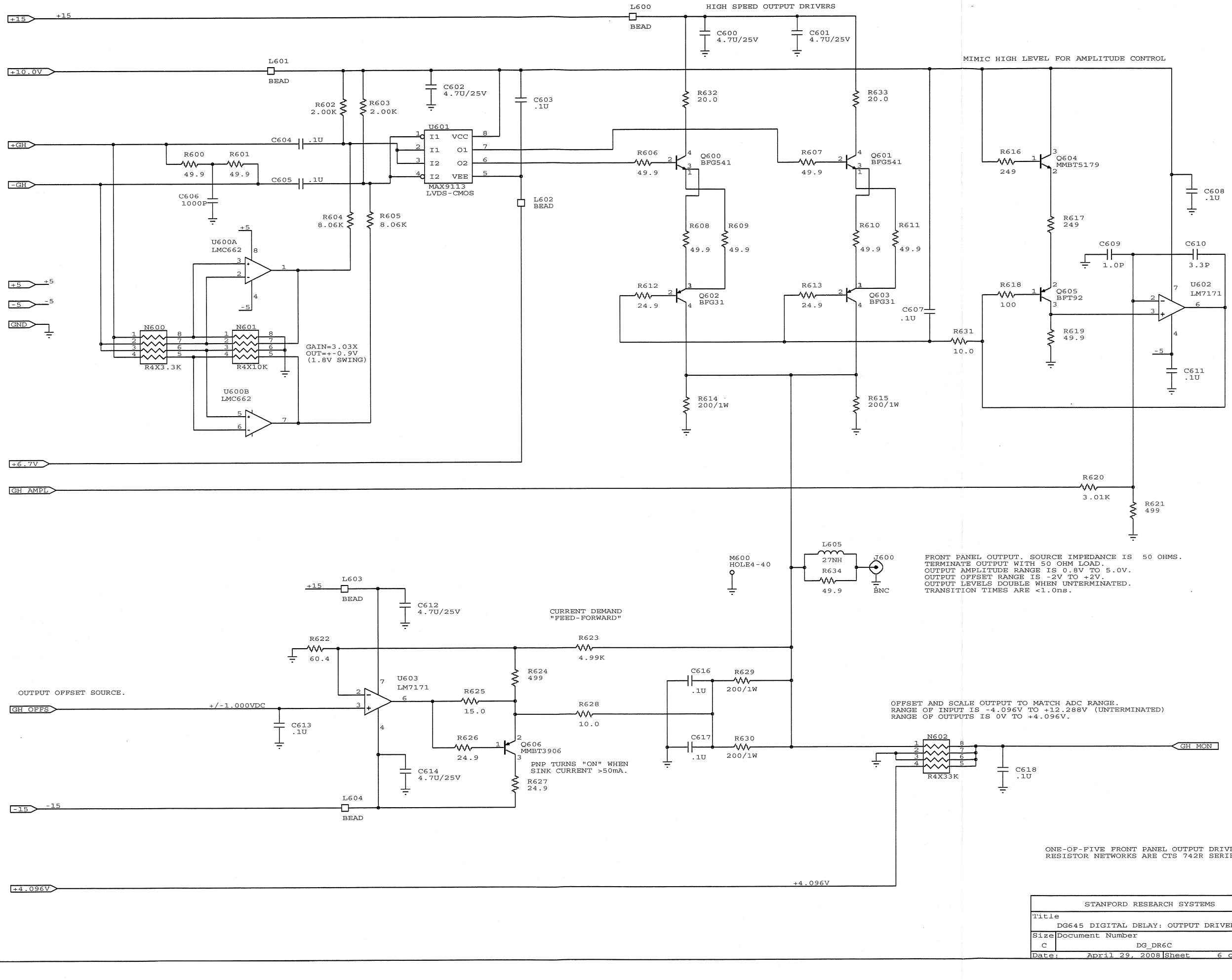
STANFORD RESEARCH SYSTEMS		
Title: DG645 DIGITAL DELAY: OUTPUT DRIVERS		
Size: C	Document Number: DG_DR3C	REV: C
Date: April 29, 2008	Sheet 3 of 6	



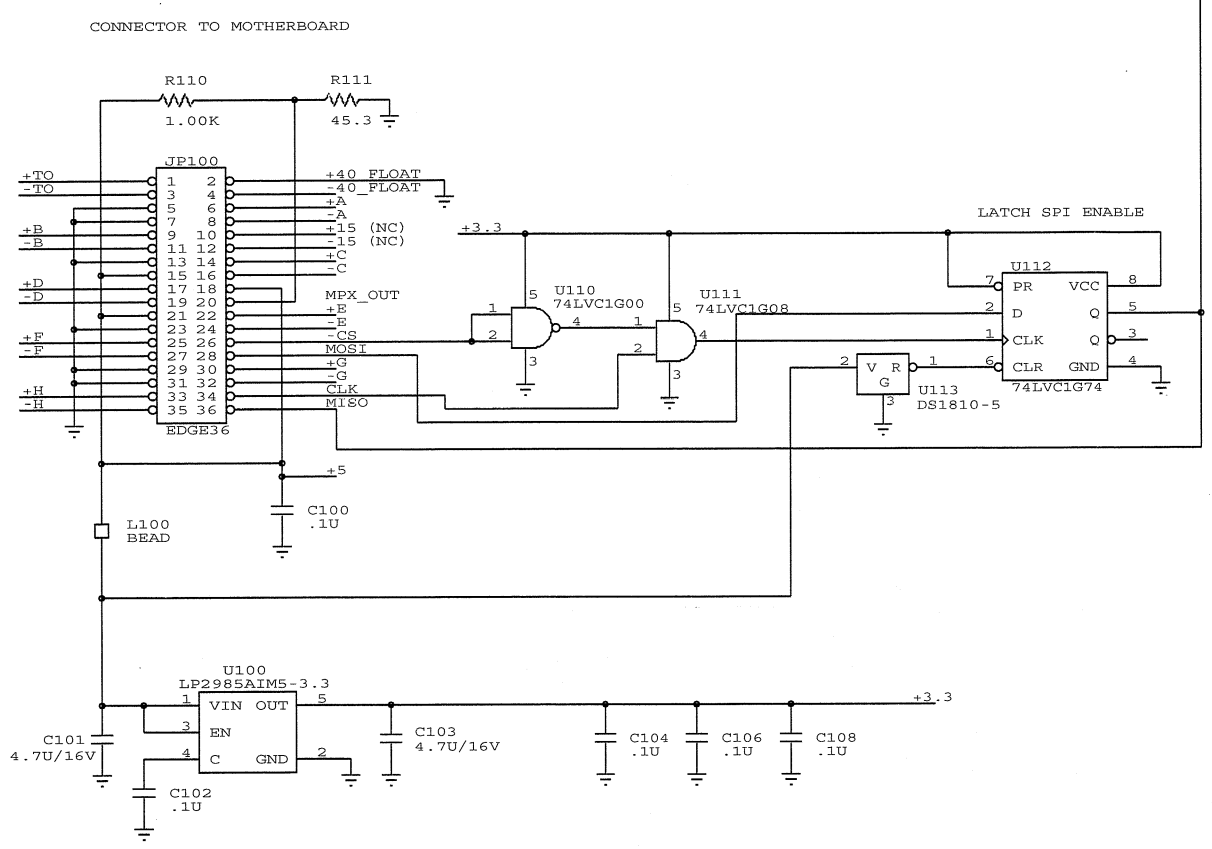
STANFORD RESEARCH SYSTEMS		
Title: DG645 DIGITAL DELAY: OUTPUT DRIVERS		
Size: C	Document Number: DG_DR4C	REV: C
Date: April 29, 2008	Sheet 4 of 6	

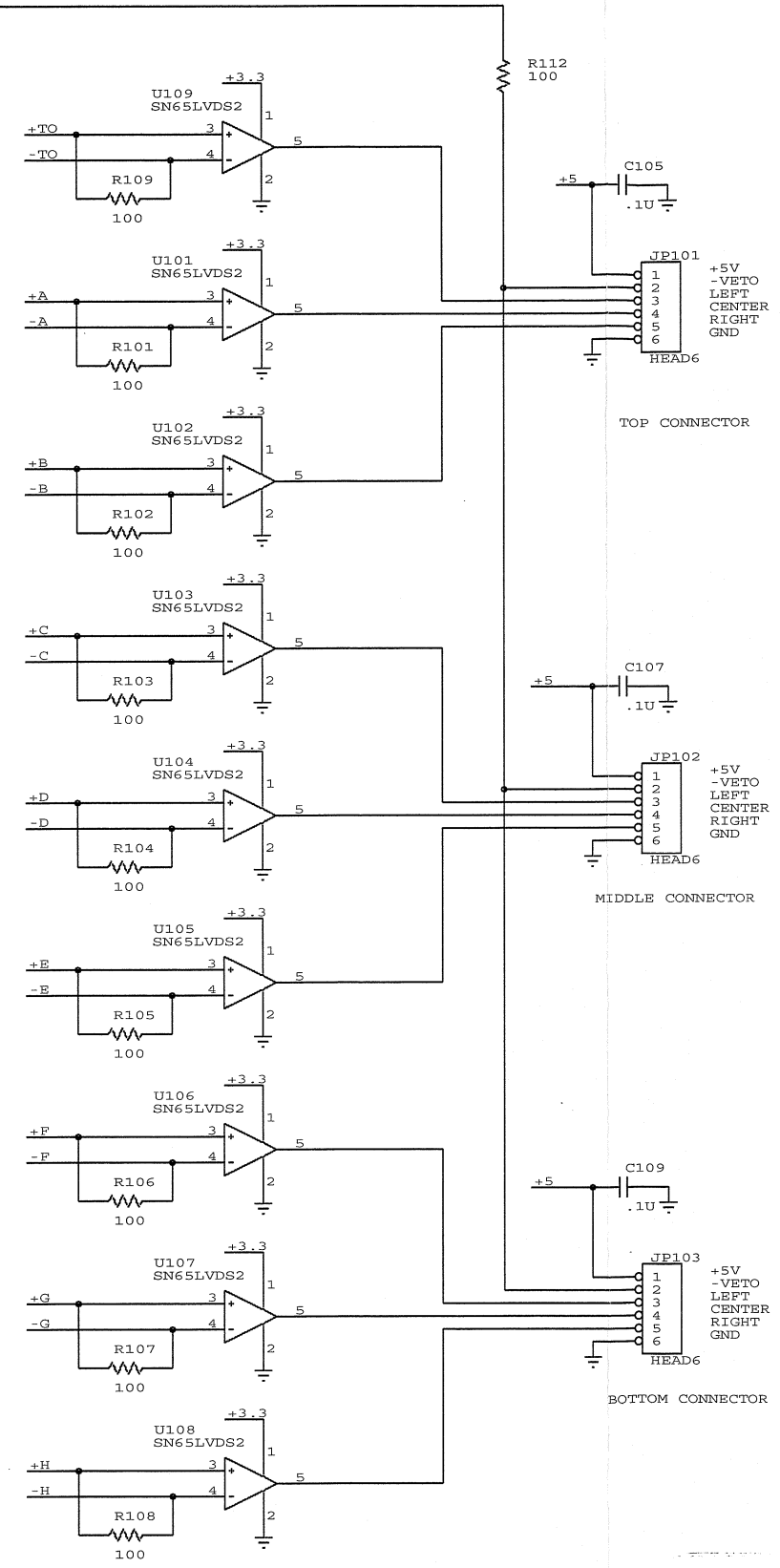


STANFORD RESEARCH SYSTEMS		
Title: DG645 DIGITAL DELAY: OUTPUT DRIVERS		
Size: C	Document Number: DG_DR5C	REV: C
Date: April 29, 2008	Sheet 5 of 6	



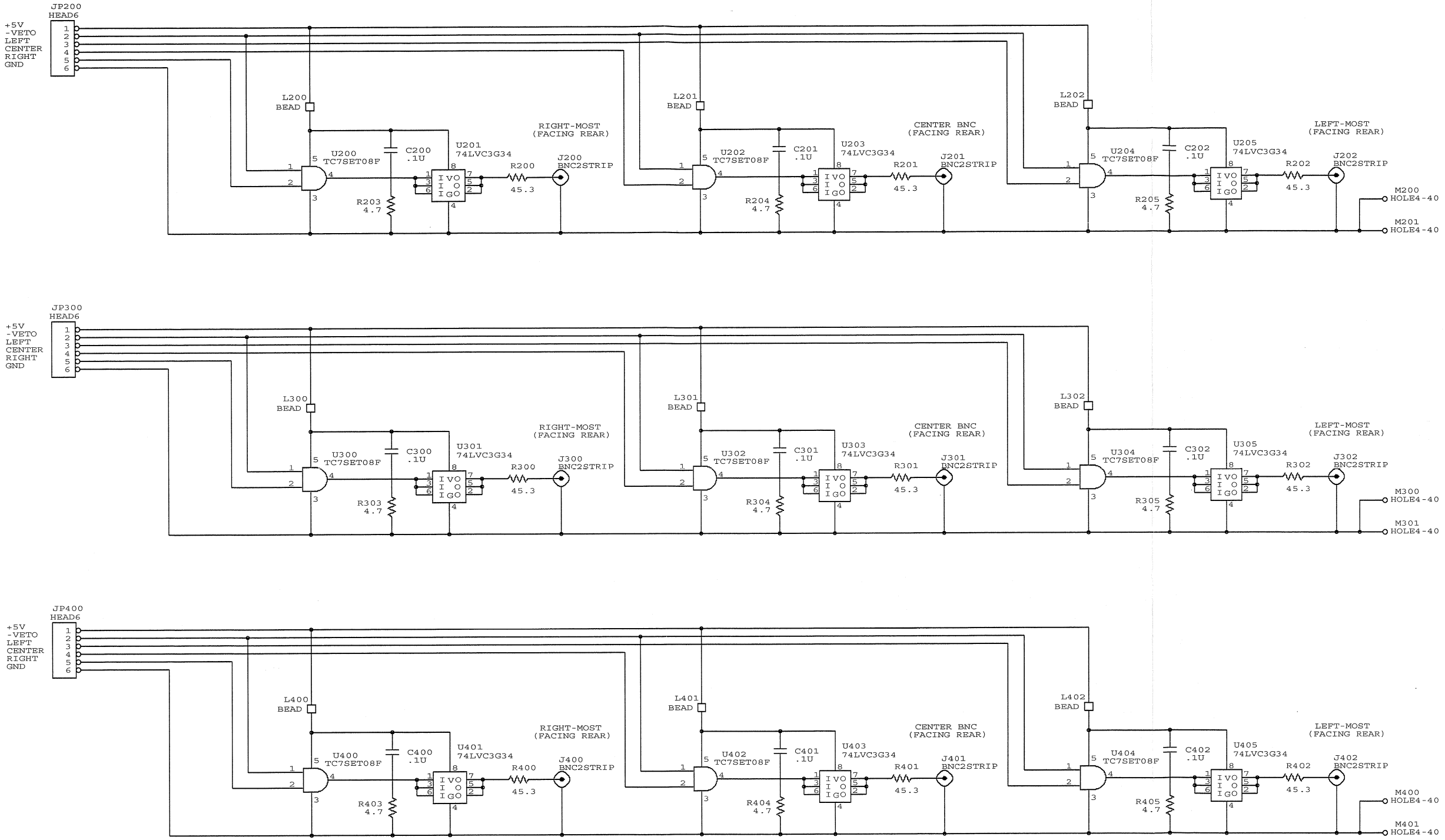
STANFORD RESEARCH SYSTEMS		
Title: DG645 DIGITAL DELAY: OUTPUT DRIVERS		
Size: C	Document Number: DG_DR6C	REV: C
Date: April 29, 2008	Sheet 6 of 6	





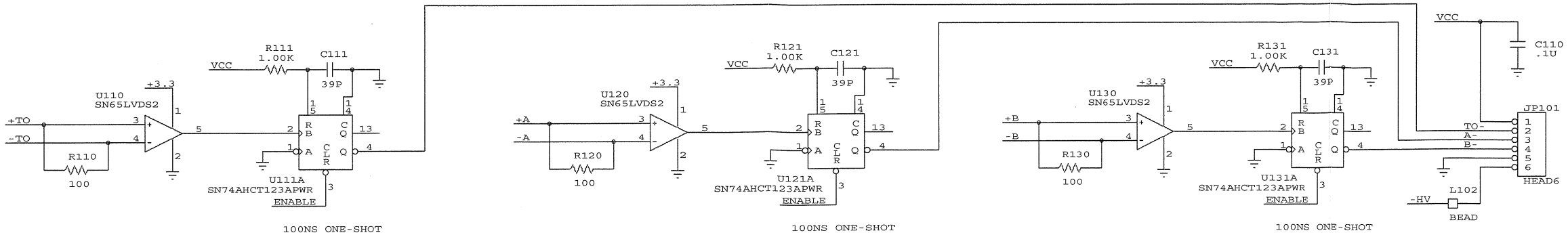
COMPONENTS SHOWN ON THIS SCHEMATIC ARE LOCATED ON THE VERTICAL PCB OF THE 8-CHANNEL OUTPUT (OPT 1).

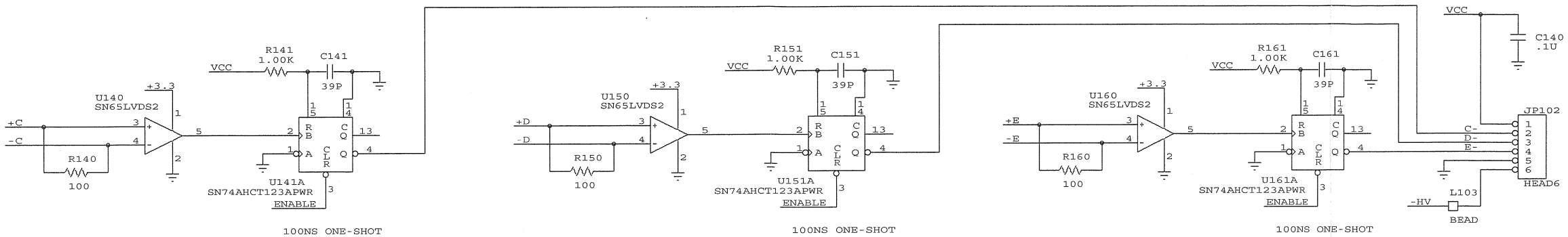
STANFORD RESEARCH SYSTEMS		
Title: DG645 DELAY GENERATOR: REAR PANEL 8 CHANNEL		
Size: C	Document Number: DG_RP1C	REV: C
Date: March 24, 2008	Sheet 1 of 2	

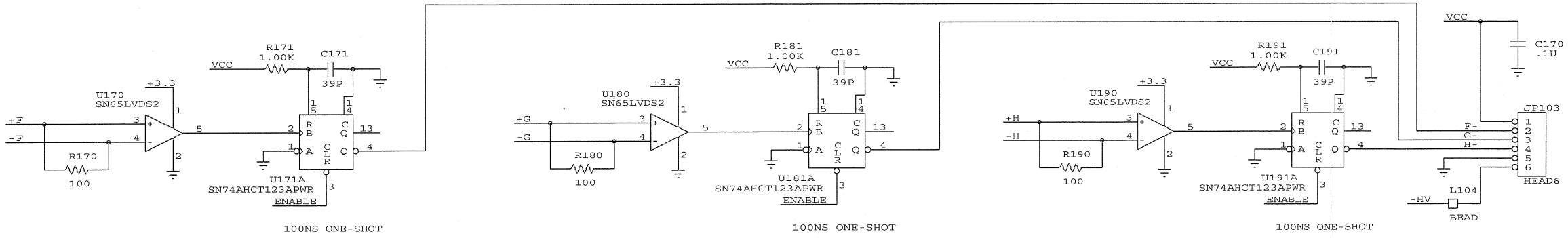


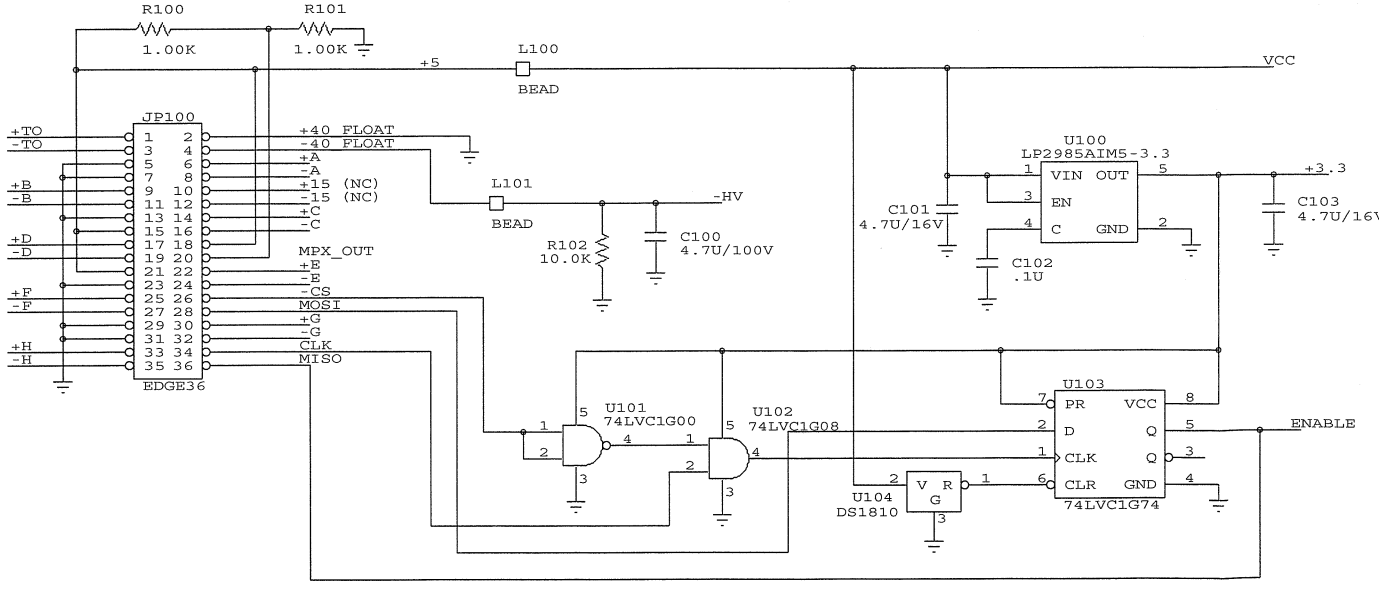
COMPONENTS SHOWN IN THIS SCHEMATIC ARE LOCATED ON THE THREE HORZONTAL PCBs ATTACHED TO THE REAR PANEL.

STANFORD RESEARCH SYSTEMS		
Title: DG645 DELAY GENERATOR: 8-CHANNEL REAR PANEL		
Size: C	Document Number: DG_RP2C	REV: C
Date: March 21, 2008	Sheet 2 of 2	

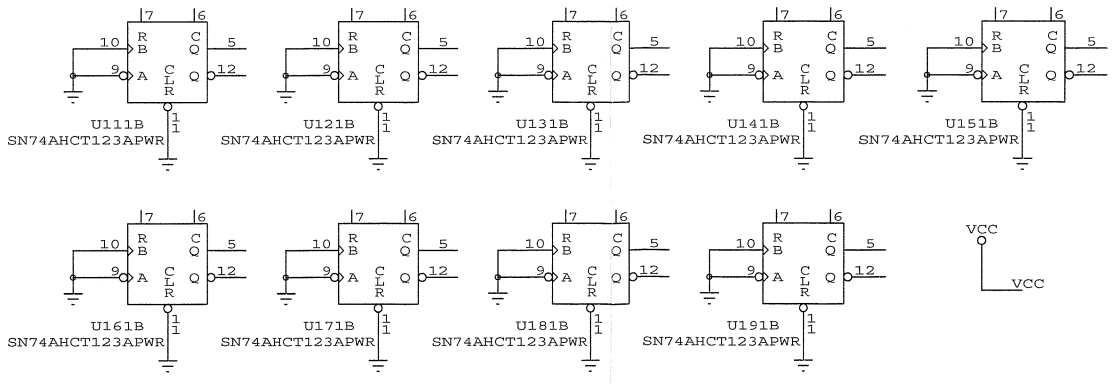




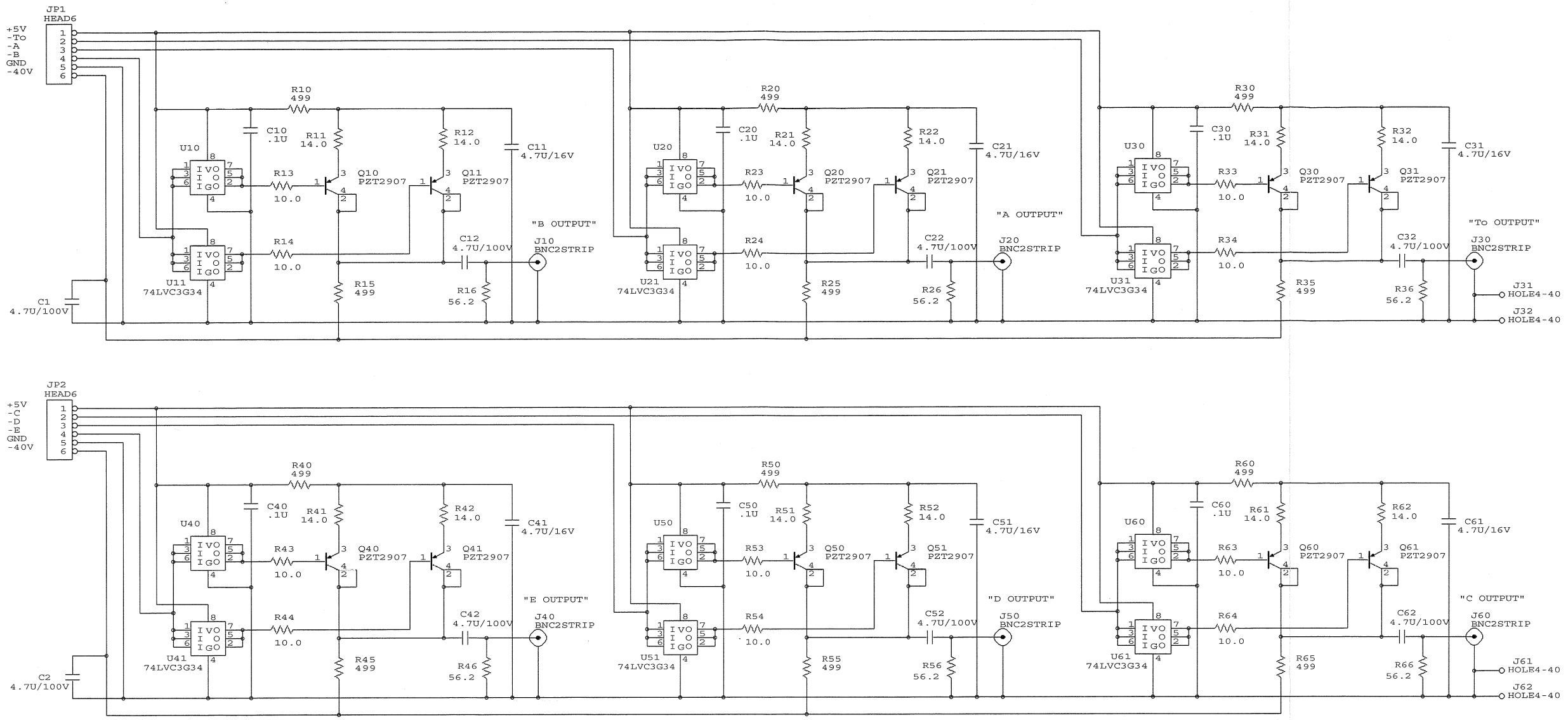




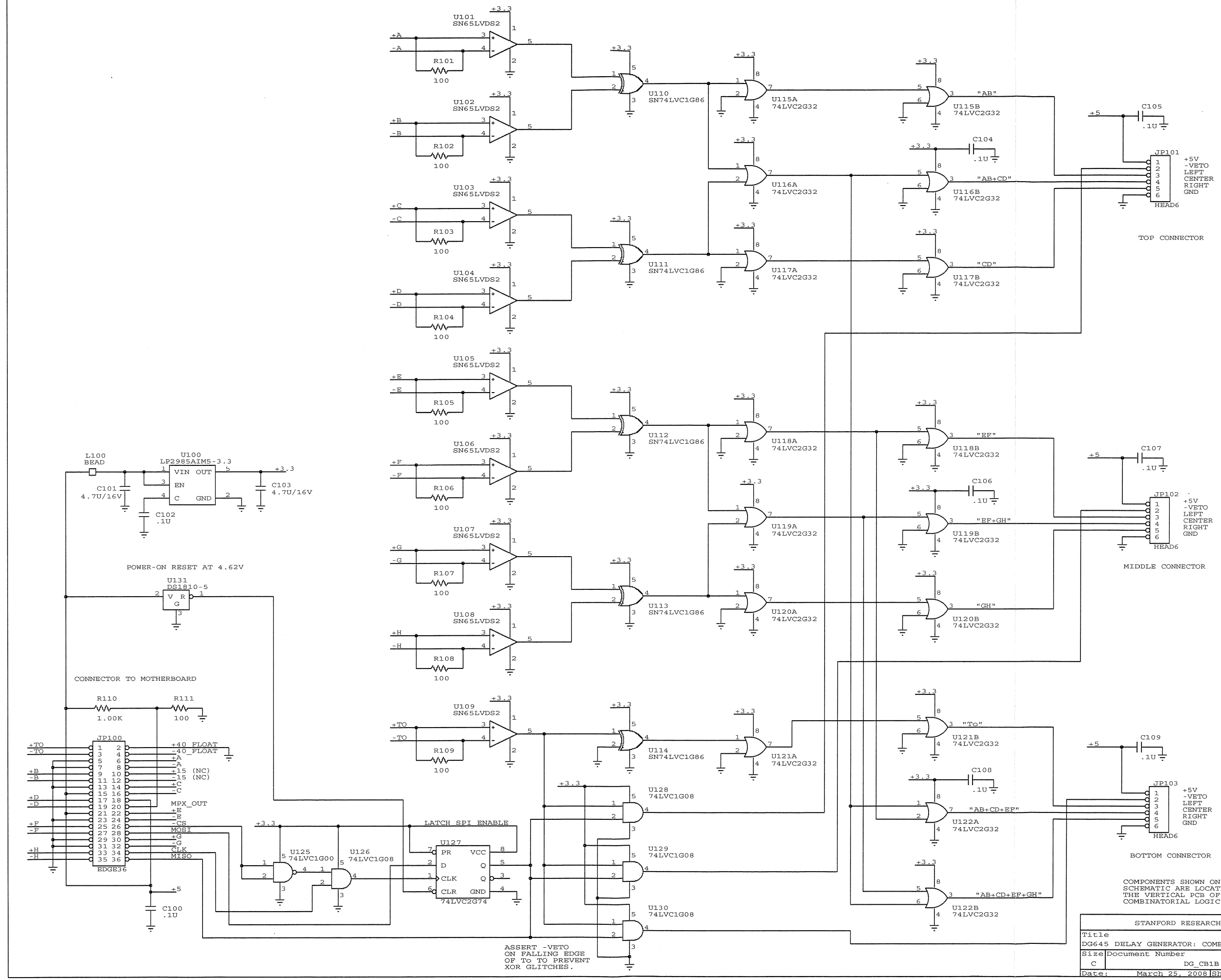
THE SECOND-HALF OF THE DUAL ONE-SHOTS ARE NOT USED TO AVOID PULSE-PULLING.

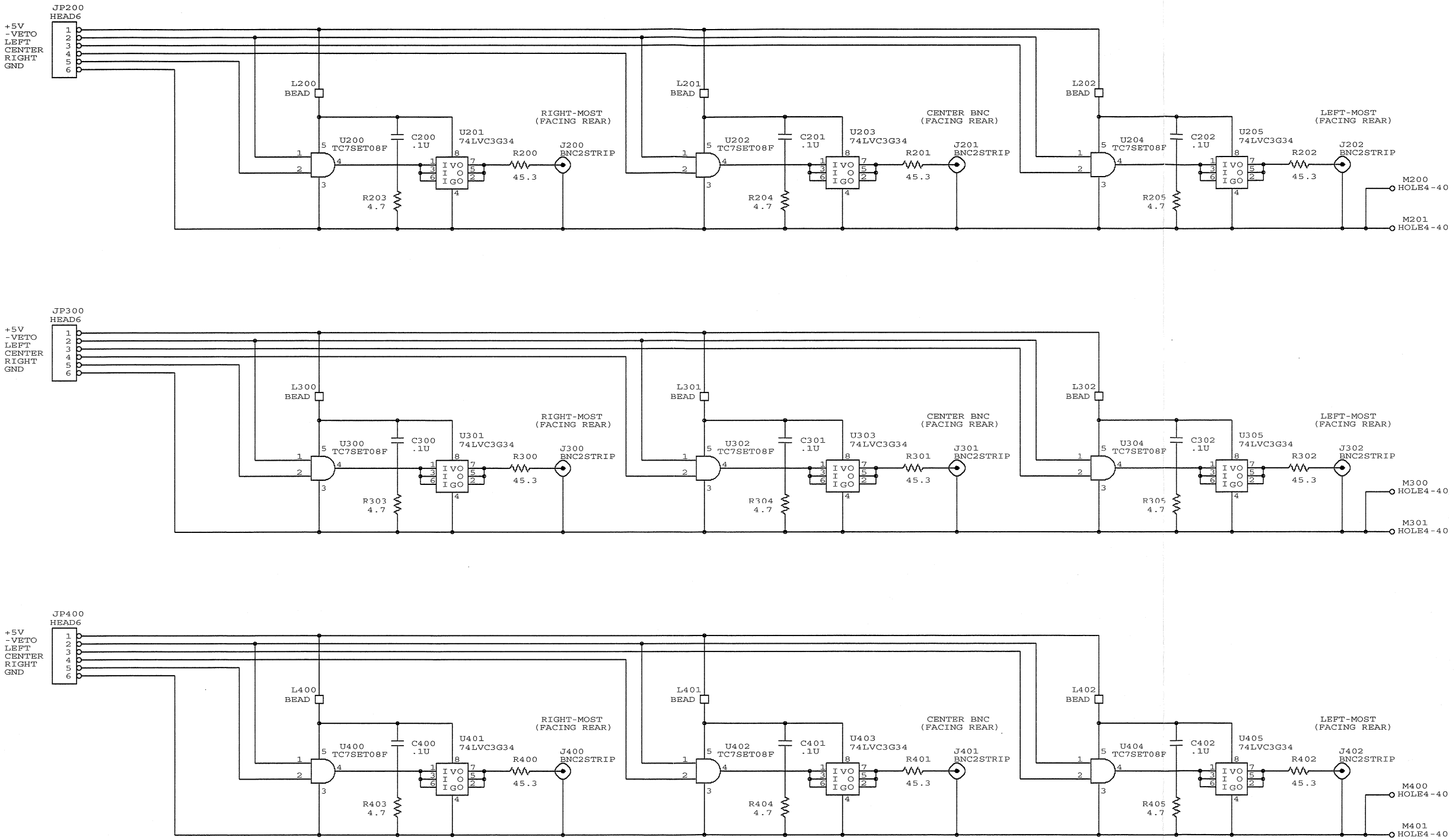


STANFORD RESEARCH SYSTEMS		
Title: DG645 DELAY GENERATOR: HV REAR PANEL OUTPUTS		
Size: C	Document Number: DG_HV1B	REV: B
Date: March 25, 2008	Sheet 1 of 2	



STANFORD RESEARCH SYSTEMS		
Title: DG645 DELAY GENERATOR: HV REAR PANEL OUTPUTS		
Size: C	Document Number: DG_HV2B	REV: B
Date: March 5, 2008	Sheet 2 of 2	


U101 SN65LVDS2
U102 SN65LVDS2
U103 SN65LVDS2
U104 SN65LVDS2
U105 SN65LVDS2
U106 SN65LVDS2
U107 SN65LVDS2
U108 SN65LVDS2
U109 SN65LVDS2
+A
-A
+B
-B
+C
-C
+D
-D
+E
-E
+F
-F
+G
-G
+H
-H
+TO
-TO
R101 100
R102 100
R103 100
R104 100
R105 100
R106 100
R107 100
R108 100
R109 100
U110 SN74LVC1G86
U111 SN74LVC1G86
U112 SN74LVC1G86
U113 SN74LVC1G86
U114 SN74LVC1G86
U115A 74LVC2G32
U115B 74LVC2G32
U116A 74LVC2G32
U116B 74LVC2G32
U117A 74LVC2G32
U117B 74LVC2G32
U118A 74LVC2G32
U118B 74LVC2G32
U119A 74LVC2G32
U119B 74LVC2G32
U120A 74LVC2G32
U120B 74LVC2G32
U121A 74LVC2G32
U121B 74LVC2G32
U122A 74LVC2G32
U122B 74LVC2G32
"AB"
"AB+CD"
"CD"
"EF"
"EF+GH"
"GH"
"To"
"AB+CD+EF"
"AB+CD+EF+GH"
+3.3
+5
C104 .1U
C105 .1U
C106 .1U
C107 .1U
C108 .1U
C109 .1U
JP101
JP102
JP103
+5V
-VETO
LEFT
CENTER
RIGHT
GND
HEAD6
TOP CONNECTOR
MIDDLE CONNECTOR
BOTTOM CONNECTOR
L100 BEAD
U100 LP2985AIM5-3.3
VIN OUT
EN
C GND
C101 4.7U/16V
C102 .1U
C103 4.7U/16V
POWER-ON RESET AT 4.62V
U131 DS1810-5
V R G
CONNECTOR TO MOTHERBOARD
R110 1.00K
R111 100
JP100
EDGE36
+40_FLOAT
-40_FLOAT
+15 (NC)
-15 (NC)
MPX_OUT
-CS
MOSI
-G
CLK
MISO
C100 .1U
U125 74LVC1G00
U126 74LVC1G08
LATCH SPI ENABLE
U127 74LVC2G74
PR VCC
D Q
CLK Q
CLR GND
U128 74LVC1G08
U129 74LVC1G08
U130 74LVC1G08
ASSERT -VETO ON FALLING EDGE OF To TO PREVENT XOR GLITCHES.
COMPONENTS SHOWN ON THIS SCHEMATIC ARE LOCATED ON THE VERTICAL PCB OF THE COMBINATORIAL LOGIC OPTION.
STANFORD RESEARCH SYSTEMS
Title
DG645 DELAY GENERATOR: COMBINATORIAL OUTPUTS
Size C
Document Number DG_CB1B
REV B
Date: March 25, 2008
Sheet 1 of 2



COMPONENTS SHOWN IN THIS SCHEMATIC
ARE LOCATED ON THE THREE HORZONTAL
PCBs OF THE COMBINATORIAL LOGIC OPTION.

STANFORD RESEARCH SYSTEMS		
Title: DG645 DELAY GENERATOR: COMBINATORIAL OUTPUTS		
Size: C	Document Number: DG_CB2B	REV: B
Date: March 25, 2008	Sheet 2 of 2	