Error Detection Using CRC in Altera FPGA Devices

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Introduction

In critical applications, it is important to be able to confirm that the configuration data in an FPGA device is correct and be able to trigger a re-configuration if data corruption occurs due to a single event upset (SEU). The error detection CRC feature in the Stratix and Cyclone series is recommended in high reliablity environments like avionics applications.

While soft errors are uncommon in Altera FPGAs, certain high reliability applications may require a design to account for these effects. This application note describes how to activate and utilize the optional error detection feature in user mode.

The error detection cyclic redundancy check (CRC) feature uses a 32-bit CRC circuit to ensure data reliability and trigger a re-configuration when affected by SEU. The error detection feature using CRC is supported for Stratix® II, Stratix, Stratix GX, Cyclone™ II and Cyclone devices. The Stratix HardCopy devices do not have any configuration cicuitry and therefore do not support CRC. Device performance is not affected when the error detection feature is used.

Error Detection Fundamentals

Error detection determines if the data received through a medium is corrupted during transmission. To accomplish this, the transmitter uses a function to calculate a checksum value for the data and appends it to the original data frame. The receiver uses the same calculation methodology, generates a checksum for the received data frame, and compares it against the transmitted checksum. If the two values are the same, the received data frame is correct and no corruption has occurred during transmission or storage. The same concept has been adopted in the user mode error detection feature in the Stratix and Cyclone series and can ensure the integrity of the configuration data.

A future version of this document will contain more information about Stratix II and Cyclone II devices.

Configuration Error Detection

CRC-based error checking in user mode is an additional feature for the Stratix and Cyclone series above and beyond the frame-based CRC that is used to check the integrity of the data during the configuration of the device. In configuration mode, a frame CRC is stored within the configuration data that contains the CRC value for each data frame.

During configuration, the FPGA calculates the CRC value based on the frame of data that is received and compares it against the frame CRC value in the data stream. Configuration continues until either the device detects an error or configuration is complete.

Stratix II and Cyclone II devices calculate the CRC value during configuration mode. At the end of configuration mode, these devices load the CRC value into the 32-bit storage register.

For Stratix, Stratix GX, and Cyclone devices, the CRC is computed by the Quartus® II software and downloaded into the device as a part of the configuration bit stream. These devices store the CRC in the 32-bit storage register at end of configuration mode.

When the error detection feature using CRC is enabled in user mode these devices re-calculate the CRC based on the contents of the device and compare it against the 32-bit storage register.

User Mode Error Detection

Stratix and Cyclone series have built-in error detection circuitry to detect data corruption by soft errors. Soft errors are the changes in the state of a configuration SRAM bit due to colliding alpha or neutron particle. When the data bit is re-written with the correct value by reconfiguring the device, the device functions correctly. This error detection capability continuously computes the CRC of the configured SRAM bits and compares it with the pre-calculated CRC. If the CRCs match, there is no error in the current configuration SRAM bits. The process of error detection continues until the device is reset (by pulling `nCONFIG` low).

The Stratix and Cyclone series error detection feature does not check memory blocks and I/O buffers. These device memory blocks support parity bits that can be used to check the contents of memory blocks for any error. The I/O buffers are not verified during error detection since these bits use flip-flops as storage elements, which are more resistant to soft errors. Similar flip-flops are used to store the pre-calculated CRC and other error detection circuitry option bits.

The error detection circuitry in the Stratix and Cyclone series uses a CRC-32 IEEE 802 standard, 32-bit polynomial as the CRC generator. Therefore, a single 32-bit CRC calculation is done by the device. If a soft error does not occur, the resulting 32-bit signature value will be `0x00000000`, which results in a `0` on the output signal `CRC_ERROR`. If a soft error occurs within the device, the resulting signature value will be non-zero and the `CRC_ERROR` output will be `1`.

CRC_ERROR Pin-Outs

Table 1 describes the CRC_ERROR pin. Tables 2 through 4 show the CRC_ERROR pin locations for the Stratix, Stratix GX, and Cyclone families. In the future, all pin locations for CRC_ERROR pins will be located in the device pin-outs on the web **www.altera.com**.

Table 1. CRC_ERROR Pin Description

Pin Name	Pin Type	Description
CRC_ERROR	I/O, output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. Otherwise, it is a user I/O pin.

Table 2. CRC_ERROR Pin Table for Stratix Devices

Device	Device Package						
	484-Pin FineLine BGA	672-Pin BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	956-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP1S10 *(1)*	N14	W10	W10	AA20	-	-	-
EP1S20	N14	W10	W10	AA20	-	-	-
EP1S25	-	W10	W10	AA20	-	AF20	-
EP1S30	-	-	-	AA20	AE21	AF20	-
EP1S40	-	-	-	AA20	AE21	AF20	AN25
EP1S60	-	-	-	-	AE21	AF20	AN25
EP1S80	-	-	-	-	AE21	AF20	AN25

Note to Table 2:
(1) EP1S10 engineering sample (ES) devices do not support the error detection feature.

Table 3. CRC_ERROR Pin Table for Stratix GX Devices

Device	Device Package	
	672-pin FineLine BGA	1,020-pin FineLine BGA
EP1SGX10C	U15	
EP1SGX10D	U15	
EP1SGX25C	U15	
EP1SGX25D	U15	AE21
EP1SGX25F		AE21
EP1SGX40D		AE21
EP1SGX40G		AE21

Table 4. CRC_ERROR Pin Table for Cyclone Devices

Device	Device Package					
	100-Pin TQFP	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
EP1C3	2	2	-	-	-	-
EP1C4	-	-	-	-	C2	C2
EP1C6	-	2	2	C3	-	-
EP1C12	-	-	2	C3	C2	-
EP1C20	-	-	-	-	C2	C2

Error Detection Block

You can enable the Stratix or Cyclone series error detection block in the Quartus II software (see "Software Support" on page 7). This block contains the logic necessary to calculate the 32-bit CRC signature for the configuration SRAM bits in the device.

The CRC circuit continues running even if an error occurs. When a soft error occurs, the device sets the CRC_ERROR pin high.

Error Detection Registers

There are two sets of 32-bit registers in the error detection circuitry that store the computed CRC signature and precalculated CRC value. A nonzero value on the signature register will cause the CRC_ERROR pin to drive high. Figure 1 shows the block diagram of the error detection block and the two related 32-bit registers: signature register, storage register.

Figure 1. Error Detection Block Diagram

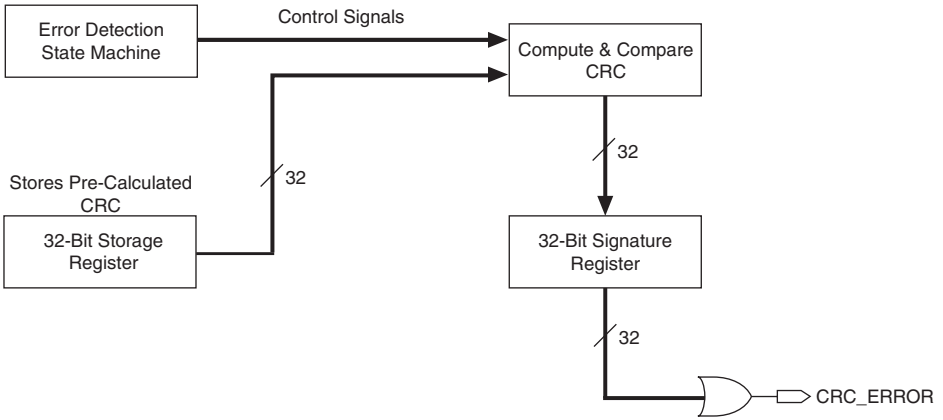


Table 5 defines the registers shown in Figure 1.

Table 5. Error Detection Registers

Register	Function
32-bit signature register	This register contains the CRC signature. The signature register contains the resultant of the user mode calculated CRC value compared against the pre-calculated CRC value. The signature register will be all-zeros if no errors are detected. A non-zero signature register indicates an error in configuration SRAM contents. The CRC_ERROR signal is derived from the contents of this register.
32-bit storage register	This register is loaded with the 32-bit precomputed CRC signature at the end of configuration stage. The signature is then loaded into the 32-bit CRC circuit (called "Compute & Compare CRC" in Figure 1) during user mode to calculate CRC error.

Error Detection Timing

When the CRC error detection feature is enabled through the Quartus II software, the device automatically activates the CRC process upon entering user mode after configuration and initialization is complete. The CRC_ERROR pin will be driven low until an error occurs. The CRC_ERROR pin will be driven high when the error detection circuitry has detected corrupted bit(s) in the previous CRC calculation. Once the CRC_ERROR pin goes high, it remains high even during the next CRC calculation. This pin does not keep a record of the previous CRC calculation. If the new CRC calculation does not contain any corrupted bits, the CRC_ERROR pin will toggle low. The error detection runs until the device is reset.

As soon as the device enters user mode, the error detection feature process is enabled. The error detection circuitry runs off the configuration oscillator (a 100-MHz clock in the Stratix series and a 80-MHz clock in Cyclone series). You can divide down this clock frequency by specifying the division in Quartus II software (see "Software Support" on page 7). The divider is a power of two (2^n), where n is between 0 and 8. The divider ranges from 1 to 256. For example, in Stratix series the maximum error detection frequency is 100 MHz, and the minimum error detection frequency is 390 kHz. See the following equation:

$$\text{Error detection frequency} = \frac{100\ \text{MHz}}{2^n}$$

The time it takes for each CRC calculation depends on the device and the error detection clock frequency. Table 6 shows the estimated time for each CRC calculation with minimum and maximum clock frequencies in Stratix and Cyclone series.

Table 6. CRC Calculation Time (Part 1 of 2)

Device	Minimum Time (ms) *(1)*	Maximum Time (s) *(2)*
EP1S10	4.3	1.1
EP1S20	7.2	1.9
EP1S25	9.8	2.5
EP1S30	12.8	3.3
EP1S40	15.3	3.9
EP1S60	21.7	5.6
EP1S80	29.6	7.6
EP1C3	0.92	0.24
EP1C4	1.3	0.32
EP1C6	1.8	0.45
EP1C12	3.5	0.90
EP1C20	5.4	1.4

Table 6. CRC Calculation Time (Part 2 of 2)

Device	Minimum Time (ms) *(1)*	Maximum Time (s) *(2)*
EP1SGX10C	4.3	1.1
EP1SGX10D	4.3	1.1
EP1SGX25C	9.8	2.5
EP1SGX25D	9.8	2.5
EP1SGX25F	9.8	2.5
EP1SGX40D	15.3	3.9
EP1SGX40G	15.3	3.9

Notes to Table 6:

(1) Minimum time corresponds to the maximum error detection clock frequency (100 MHz for Stratix series, 80 MHz for Cyclone series) and may vary with different processes, voltages, and temperatures.

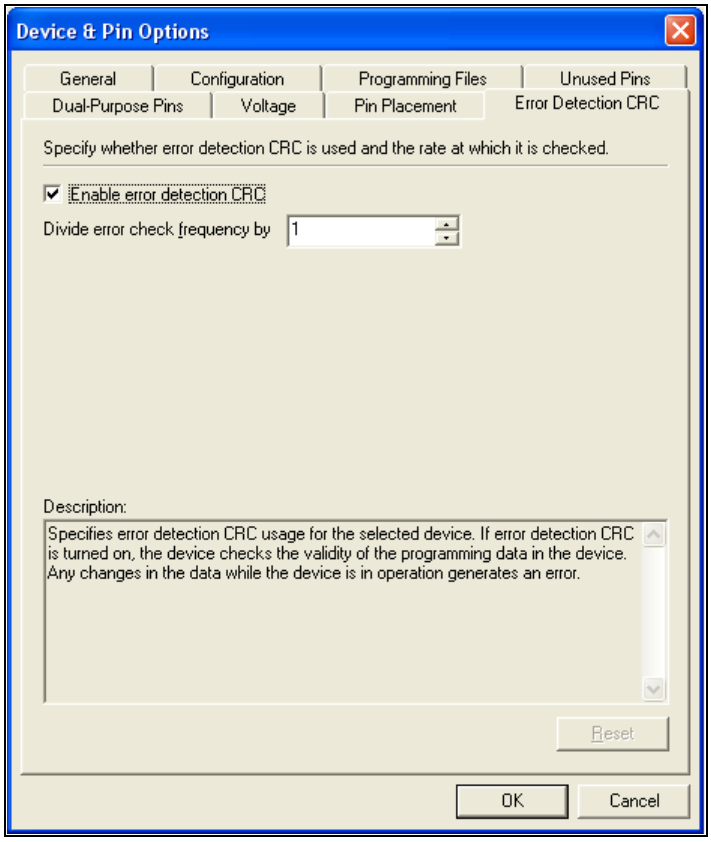
(2) Maximum time corresponds to the minimum error detection clock frequency (390 kHz for Stratix series, 312.5 kHz for Cyclone series) and may vary with different processes, voltages, and temperatures.

Software Support

The Quartus II software, version 4.1 and higher, supports the CRC error detection feature. Enabling this feature generates the `CRC_ERROR` output to the optional dual purpose `CRC_ERROR` pin.

The error detection CRC feature is controlled by the **Device & Pin Options** dialog box in the Quartus II software and uses a 32-bit CRC circuit to ensure data reliability. Figure 2 shows the **Device and Pin Options** dialog box. The error detection feature using CRC can be enable by checking the **Enable error detection CRC** and by setting the divider to a legal value 1, 2, 4, 8, 16, 32, 64, 128, or 256. The divide value divides down the frequency of the configuration oscillator output clock that clocks the CRC circuitry.

Figure 2. Enabling the Error Detection CRC in Quartus II



To open this dialog box perform the following steps.

1. Open the Quartus II software and load a project using the Stratix or Cyclone series.
2. Choose **Settings** (Assignments menu).
3. In the **Category** list, select **Device**.
4. Click **Device & Pin Options**.
5. In the **Device & Pin Options** dialog box, click the **Error Detection CRC** tab.
6. Click in the check box to **Enable error detection CRC**.

7. Type a value in the **Divide error check frequency by list**.

8. Click **OK**.

Conclusion

The purpose of CRC error detection is to detect if any configuration SRAM bits in the Stratix and Cyclone series have been flipped due to a soft error. Soft errors rarely occur, and this is only a concern in high-reliability applications. For this subset of environments, the error detection circuitry enables you to continuously verify the reliability of the configuration SRAM bits.

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