Stratix II High-Speed Development Board

September 2004, ver.1.0 Data Sheet

Introduction

The Stratix® II high-speed development board provides a hardware platform for developing and prototyping high-speed, source-synchronous and double data rate (DDR) memory interfaces based on Stratix II FPGAs using Altera® MegaCore® functions. The board supports the following high-speed protocols:

- SERDES framer interface level 4, phase 1 (SFI-4.1)
- 10-Gigabit Ethernet (XSBI)
- System packet interface level 4-phase 2 (SPI-4.2)
- 8-bit RapidIO™
- HyperTransport™
- 64-bit PCI and PCI-X over PCI mezzanine card (PMC)
- DDR2 dual in-line memory module (DIMM)

Featuring a Stratix II EP2S60F1020-C3 device (migratable to the largest member of the Stratix II device family), a MAX® EPM7256AETC144 device, a DDR2 SDRAM DIMM, a Flash, and two SRAM memory devices, the Stratix II high-speed development board's power supply is designed to allow maximum user-flexibility.

The Stratix II high-speed development board is also a platform to tour Stratix II device features, and is distributed as part of the *High-Speed Development Kit, Stratix II Edition*.

For more information on the *High-Speed Development Kit, Stratix II Edition*, go to **www.altera.com**.

Feature Summary

This section lists the interfaces, devices, memory, clocking, power, configuration, user I/O, monitor and control elements supported on the board.

Interfaces

In source-synchronous designs, bus throughput is critical to the overall system performance. Thus, the availability of high-speed, high-bandwidth board interfaces is an important factor. The Stratix II high-speed development board provides:

- SFI-4.1/XSBI at 622/644 Megabits per second (Mbps)
- SPI-4.2 at 1.0 Gbps
- RapidIO at 1.0 Gigabit per second (Gbps)

- HyperTransport at 1.0 Gbps
- 64-bit PMC at 66 MHz and PCI-X (over PMC) at 133 MHz
- DDR2 SDRAM DIMM memory at 267 MHz (533 Mbps)
- Subminiature type A (SMA) connector loopback at 1.0 Gbps
- Select configurations of PTMC
- 10/100 Ethernet interface

Devices

To stay within the permitted skew of high-speed interfaces with source-synchronous clocking schemes, Stratix II devices provide dynamic phase alignment (DPA) circuitry, which eliminates clock-to-channel skew. Additionally, the MAX or MAX II device performs as a configuration system controller when using the fast passive parallel (FPP) configuration scheme. Refer to "JTAG Expansion" on page 12.

The following Altera devices are available on the board:

- One Stratix II device (EP2S60F1020-C3), migratable to the largest member of the family (EP2S180)
- Either one MAX II device (EPM1270F256C3), or one MAX device (EPM7256AETC144)
- EPCS device

The board can be stuffed with either a MAX or MAX II device.

Memory

Memory bandwidth is a critical element of high-speed, source synchronous interfaces. Thus, the Stratix II high-speed development board includes:

- One DDR2 SDRAM DIMM connector, 72 bits
- One Flash 128 Mb memory device (AM29LV128MH113REI)
- Two SRAM 256 K x 16 memory devices (IDT71V416510PH)

Clocking

The Stratix II high-speed development board's clocking is generated using:

- External clock inputs/outputs via SMA connectors
- On-board oscillators (155.52/161 MHz, 100 MHz, 33.3 MHz, and 25 MHz) and clock drivers
- Oscillator sockets (155.52/161 MHz and 100 MHz)

The 155.52-MHz crystal oscillator comes standard with the development board. However, designers may use other frequency crystal oscillators in the socket.

Power

The Stratix II high-speed development board's power supply is designed to allow maximum user-flexibility, and provides:

- Power input through 16-V universal AC adapter or banana jacks
- Socketed fuses to isolate planes so that banana jacks can bring power to the board without conflicting with the AC adapter power
- On-board linear and switching regulators

Configuration

Board configuration modes include:

- FPP configuration using the MAX/MAX II device and on-board Flash memory
- JTAG stand-alone configuration using either the Altera USB-Blaster™ or ByteBlaster™ (or ByteBlaster II) download cable and the JTAG header
- Active serial (AS) configuration using the serial peripheral interface (SPI) with EPCS devices
- JTAG chain configuration between different boards using the JTAG master/slave headers

User I/O

Stratix II devices support the requirements of high-speed I/O protocols and offer up to 152 receiver and 156 transmitter channels that support source-synchronous signaling for data transfer rates up to 1 Gbps. The following user I/O elements are included on the board:

- Eight user LEDs, four power monitor LEDs, one power supply LED, and six status LEDs.
- Two seven-segment displays.
- Three octal DIP switches. One for user logic functions, one for configuration setting, and one for power enable.
- Seven push buttons for user logic functions; four general purpose, one system reset, one device clear, and one safe mode configuration push button.

Performance Monitoring & Control

Board performance monitoring and control is performed using:

- RS-232 interface for debugging and register access
- Tektronix and Agilent logic analyzer connectors
- 100-mil test headers

Power Input Sources, On-Board Regulators & Power Planes

The Stratix II development board's power supply is designed to allow maximum user flexibility. This section describes the power input sources, on-board regulators, and power planes. Additionally, the power generation and distribution scheme are explained.

Power Input Sources

The board can be powered in two ways:

- 16-V universal AC/DC power jack (header J9)
- Bench power supplies, i.e., various banana jacks

16-V Universal AC/DC Power Jack

A 16-V AC/DC power input is provided by a right-angle 2.5 mm power jack with a 5.5 mm barrel. The incoming DC voltage is regulated down to 1.2 V, 1.8 V, and 3.3 V by three switching power supplies. From these voltages all other on-board voltages are generated.

Bench Power Supplies

To allow bench power supplies to power input sections using banana jacks, the voltage planes are isolated from the regulators and socketed fuses are provided to bypass the 16-V universal power supply. To allow current draw measurements, the bench supply inputs are placed after the other board power supplies (whether linear or switching).

On-Board Regulators

The board has three linear and four switching regulators designed to provide power to all board interfaces. Table 1 lists the on-board regulators.

Table 1. On-Board Regulators (Part 1 of 2)

Reference Designator	Type	Voltage Output (V)	Destination	Manufacturer	Part Number
U27	Dual Switching regulator	3.3 V,1.8 V	3.3V - Stratix II, General Purpose, PMC 1.8V - Stratix II Banks 3 and 4, DDR2 SDRAM DIMM	Linear Technology	LTC3728EG
U28	Switching regulator	1.2 V	1.2V_INT plane Stratix II (Stratix II core supply)	Linear Technology	LTC1778EGN
U12	Switching regulator	-5.2 V	MSA300 connector (SFI-4.1/XSBI interface)	Linear Technology	LTC3704EMS

Table 1. On-Board Regulators (Part 2 of 2)

Reference Designator	Type	Voltage Output (V)	Destination	Manufacturer	Part Number
U9	Switching regulator	5.0 V	PMC	National Semiconductor	LM2678S-5.0
U11	Linear regulator	2.5 V	HyperTransport, RapidIO, SFI-4.1/XSBI, SPI-4.2, SS SMA	Micrel	MIC29502BU
U10	Linear regulator	1.2 V_LIN	Stratix II PLL analog supply	National Semiconductor	LP3883ES-1.2
U4	Linear regulator	0.9 V	DDR2 SDRAM DIMM Vref and VTT	National Semiconductor	LP2996M
U37	DC/DC controller	+12 V	Fan supply	Linear Technology	LTC1872B

Power Planes

Bench power supplies provide an easy way to measure the current draw on each power plane. When one plane is being powered by the bench power supply, all other planes still draw current from the AC adapter power supply.

Table 2 lists procedures for powering individual planes through bench power supplies. In the Table 2 instructions, remove only the fuses listed in the *Instructions* column. Leave the other fuses on the board.

Table 2. Procedures for Powering Individual Power Planes Through Bench Power Supplies (Part 1 of 2)

Power Plane	Instructions
1.2 V_LIN	Remove fuse F5. Apply (+1.2 V, GND) to (J6, J5) from bench power supply.
3.3 V	Remove fuse F6. Apply (+3.3 V, GND) to (J7, J5) from bench power supply.
1.8 V and 1.8 V_DDRII (common)	Remove fuse F8. Apply (+1.8 V, GND) to (J3, J5) from bench power supply.
1.8 V and 1.8 V_DDRII (separate)	Remove fuse F3 and F8. Apply (+1.8 V, GND) to (J3, J5) from bench power supply. Apply (+1.8 V, GND) to (J10, J5) from a separate bench power supply.
1.2 V_INT	Remove fuse F1. Apply (+1.2 V, GND) to (J1, J5) from bench power supply.
VTT_DDRII	Remove fuse F7. Apply (+0.9 V, GND) to (J12, J5) from bench power supply.
2.5 V	Remove fuse F4. Apply (+2.5V, GND) to (J4, J5) from bench power supply.

Table 2. Procedures for Powering Individual Power Planes Through Bench Power Supplies (Part 2 of 2)	
Power Plane	**Instructions**
5 V	Remove fuse F2. Apply (+5V, GND) to (J2, J5) from bench power supply.
GND JACKS	J5, J8
GND_PLL JACK	J11

Configuration

The on-board Stratix II device can be configured in one of four ways. This section describes the device-configuration schemes: JTAG stand-alone, AS, FPP, and JTAG expansion.

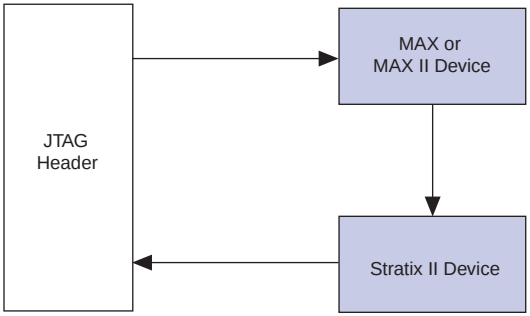
JTAG Stand-Alone Configuration Scheme

The JTAG header—a 10-pin key, right-angle, shrouded header (J55)—is provided for configuring the MAX or MAX II device and Stratix II FPGA in a single JTAG chain using the ByteBlaster II, or USB-Blaster and compatible JTAG programming adapters. The JTAG header is the Molex 39-26-7108. A double-pole, double-throw switch (SW3) is used to select which device is attached to the JTAG chain. The SW3 switch allows either a Stratix II and Stratix II device configuration, or a MAX and MAX II device configuration. Table 3 lists the JTAG bypass settings.

Table 3. Switch Settings for JTAG Stand-Alone Configuration Scheme		
Device in Chain	**Switch SW3 Position**	**Switch SW2 Position**
Stratix II device	STX2	Stand alone
Stratix II device and MAX or MAX II device	MAX_STX2	Stand alone

Figure 1 shows the board's JTAG chain configuration sequence. However, the MAX/MAX II device can be bypassed.

Figure 1. Board JTAG Chain



AS Configuration Scheme

The AS scheme uses the board's EPCS serial configuration device to program the Stratix II device. The configuration data is programmed into the EPCS device (U15) either remotely or through the JTAG connector. Table 4 lists the dipswitch (S2) configuration requirements.

Table 4. MSEL Settings for AS Configuration Scheme

Mode	MSEL3	MSEL2	MSEL1	MSEL0
20 MHz AS	1	1	0	1
40 MHz AS	1	0	0	0
20 MHz AS (Remote)	1	1	1	0
40 MHz AS (Remote)	1	0	0	1

When the dipswitches are configured in the desired mode, the board's power can be cycled. Upon power-up, the EPCS device configures the Stratix II device.

For remote configuration using AS mode, the initial design located at the EPCS device's offset `0` will select the configuration page to be loaded. The design will select the offset in the EPCS device where the next configuration file is located.

FPP Configuration Scheme

The FPP configuration scheme uses either the Altera MAX or MAX II device in conjunction with the on-board Flash memory. First, the configuration data is programmed in the non-volatile board Flash memory. Next, the MAX or MAX II device—functioning as the configuration system controller—pulls the data out of the Flash memory and sends it to the Stratix II device for configuration.

Table 5 lists the FPP interface signals, and includes both system control and configuration signals as well as dedicated function pins for configuration.

Table 5. Signals Used in FPP Configuration Scheme *Note (1)* *(Part 1 of 2)*

Signal Name	Description	Type *Note (2)*
FSE_A(26..0)	Shared bus address (Flash)	LVTTL output (27 bits)
FSE_D(15,7..0)	Shared bus data (Flash)	LVTTL input (9 bits)
CONFIG_D(7..0)	Config data	LVTTL output (8 bits)
FLASH_CEn	Flash chip enable	LVTTL output
FLASH_WEn	Flash write enable	LVTTL output
FLASH_OEn	Flash output enable	LVTTL output
FLASH_RY_BYn	Flash ready / not busy	Open drain input
FLASH_RESETn	Flash reset output	LVTTL output
FLASH_BYTEn	Flash byte-mode / word-mode select	LVTTL output
MPGM(2..0)	DIP switch configuration file select	LVTTL input (3 bits)
PGM(2..0)	Stratix II device configuration file select	LVTTL input (3 bits)
SYS_RESETn	System reset	LVTTL input
SAFEn	Safe-mode reset	LVTTI input
ENET_RESET	Ethernet reset	LVTTL output
INT_DEBUG	CPLD debug signal	LVTTL output
RU_N_LU	Remote/local mode select	LVTTL input
MSEL(3..0)	Remote/local mode select	LVTTL input (4 bits)
MAX_EN	MAX device config enable	LVTTL input
CLKA_CPLD	Input clock	LVTTL input (GCLK1)
CONFIG_DCLK	Config clk	–
USER_LED(7..0)	LED buffer input	LVTTL input (8 bits)
FLASH_CE_LEDn	LED buffer output	LVTTL output
USER_CPLD_LEDn	LED buffer output	LVTTL output

Table 5. Signals Used in FPP Configuration Scheme Note (1) (Part 2 of 2)		
Signal Name	**Description**	**Type** *Note (2)*
LOADING_LEDn	LED buffer output	LVTTL output
SAFE_LEDn	LED buffer output	LVTTL output
ERROR_LEDn	LED buffer output	LVTTL output
USER_LED_DRV(7..0)	LED buffer output	LVTTL output (8 bits)
CONFIG_DONE_LEDn	LED buffer output	LVTTL output
EP2S_INIT_DONE	Configuration init done	–
EP2S_CONF_DONE	Stratix II device config done	Open drain input
EP2S_CONFIGn	Stratix II device nCONFIG	Open drain bidir
EP2S_STATUSn	Stratix II device nSTATUS	Open drain input
CPLD_USER(3..0)	CPLD user pins	–
JTAG_TCK	JTAG clock	n/a
JTAG_TMS	JTAG mode select	n/a
JTAG_MAX_TDI	JTAG data in	n/a
JTAG_MAX_TDO	JTAG data out	n/a
3.3V	Internal power, 3.3 V	Power
-5V2_SD_MAX	-5.2 V shutdown	LVTTL output
GND	Ground	Ground

Notes to Table 5:
(1) MAX device I/O totals are 122 pins.
(2) The signal *Type* is relative to the MAX or MAX II device insofar as the I/O setting and direction.

Table 6 shows the switch settings for FPP configuration scheme.

Table 6. Switch Settings for FPP Configuration Scheme		
Devices in Chain	**Switch SW3 Position**	**Switch SW2 Position**
Stratix II device	STX2	Stand alone
Stratix II device, MAX or MAX II device	MAX_STX2	Stand alone

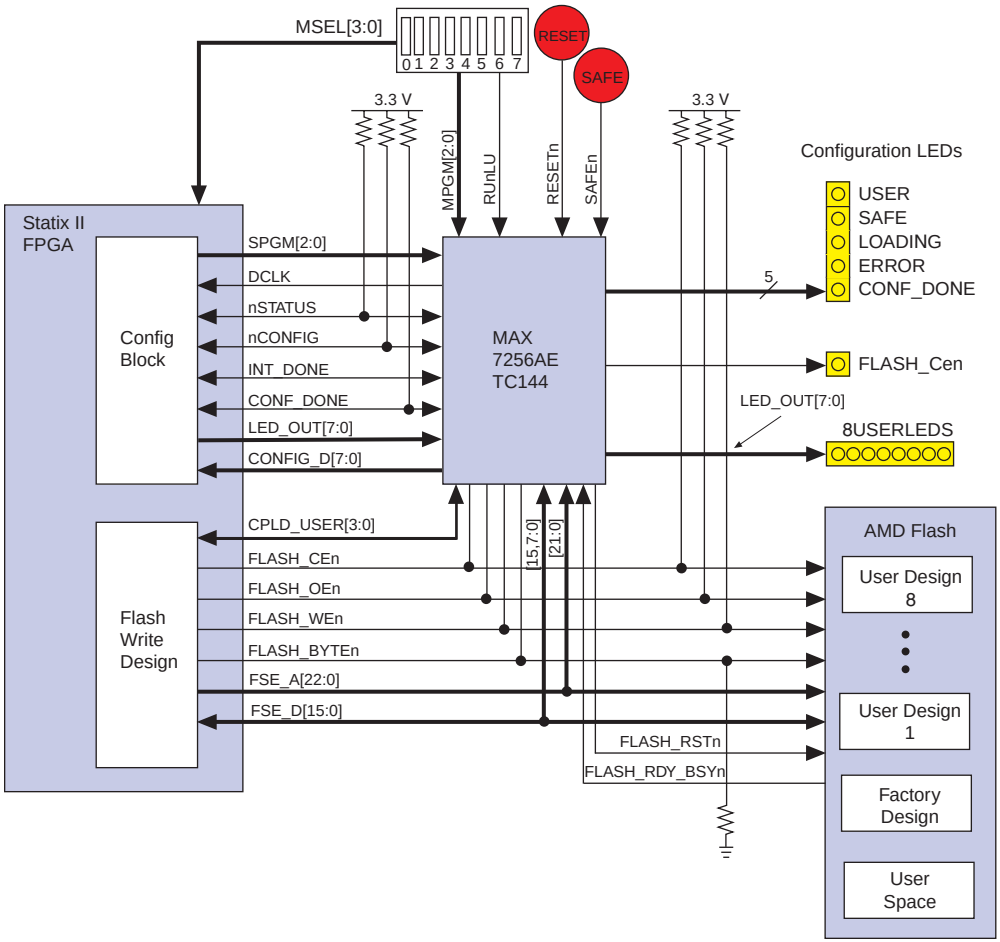
When in the FPP remote update mode, the MAX or MAX II device ignores the MPGM[2..0] bus inputs and instead looks at PGM[2..0] bus inputs transmitting from the Stratix II device (see Table 10 on page 14). The MPGM[2..0] inputs indicate which page that the MAX device should load from the Flash memory. Table 7 shows the MSEL[3..0] signal settings for the FPP configuration scheme.

Table 7. MSEL Settings for FPP

Mode	MSEL3	MSEL2	MSEL1	MSEL0
FPP (remote)	0	1	0	0
FPP with decompression and security enabled	1	0	1	1
FPP with decompression and security enabled (remote)	1	1	0	0

Figure 2 shows a general block diagram of the Stratix II high-speed development board using the FPP configuration scheme.

Figure 2. Block Diagram Using FPP Configuration Scheme



Notes to Figure 2:

(1) The `CONFIG_D[7..0]` bus from the MAX device to the Stratix II device is only required if banks 3 and 4 require low-voltage V_{CCIO} and Flash cannot meet V_{IN}.

(2) The `FSE_D[7..0]` bus link to MAX 7256 is only required if *Note (1)* applies. The only exception is that the `FSE_D[15..0]` bus is always required for byte-addressing.

(3) The `FSE_D[15..8]` bus is not required if a 16-bit Flash interface is not desired.

(4) Supports up to eight user-design files plus the factory default design.

(5) The `RUnLU` and `MSEL2` signals only require a dipswitch if remote configuration modes are to be supported (remote or local).

(6) The Flash address bus may vary based on Flash device size.

(7) Adding `CPLD_USER[3..0]` signals with pull-ups is highly recommended, and can be as little as two signals. The signals are used for control to/from MAX and Stratix II devices as needed for applications not discussed in this data sheet.

(8) The `FLASH_CEn` LED is an optional but recommended signal.

(9) The MAX 3000 device can be used for a MAX 7000 device where applicable.

(10) Remote system configuration requires SRAM, which Figure 2 does not show.

JTAG Expansion

The JTAG chain can expand to multiple Stratix II high-speed boards (or other boards) through the JTAG connectors J16 and J17. However, switch SW2 needs to be set to the *In Chain* mode. The board that is on the end of the chain (i.e., furthest from the board that has the ByteBlaster download cable plugged into it) loops the signals back through the return path by setting the SW2 position. The header/receptacle pair connects GND but not power and uses only a 2x4 array. The pinout connects the master's `TDO` pin to the slave's `TDI` pin and connects `TCK` and `TMS` directly through.

When chaining multiple boards, it is important to remember that all of the boards in the chain—except the last one—need to be set to *In Chain* mode. The last board needs to be set to *Stand Alone* mode.

Connectors, Switches & Jumpers Settings & Functions

This section summarizes the connectors, switches, and jumper settings required to achieve the desired board functionality.

Connector Settings

Table 8 lists the board's connectors and reference designators.

Table 8. Stratix II High-Speed Development Board Connectors

Connector	Reference Designator
HM-Zd connector (SPI-4.2 interface)	J37
Agilent logic analyzer connectors (for HM-Zd)	J33, J34
RapidIO mezzanine card (RMC)	J57
Tektronix logic analyzer connectors	J46, J47
HyperTransport connector	J56
MSA-300 connector (SFI-4.1/XSBI interfaces)	J28
PMC	PMCJN1, PMCJN2, PMCJN3
10/100 Ethernet	J13
RS-232	J54

Jumper & Switch I/O Functions

Table 9 lists the board's jumper and switch I/O functions.

Table 9. Stratix II High-Speed Development Board Jumper & Switch Functions

I/O Function	Stratix II Device	Not Device Specific	Jumper Connections
Power switch	–	SW1	–
JTAG chaining	–	SW2	–
JTAG device select	–	SW3	Position 1 is Stratix II device and MAX device in chain; position 2 is Stratix II device only
100 MHz OSC/SMA select	–	SW4	Connect pins 1 and 2 for `osc clk`; connect pin 2 and 3 for SMA `clk`.
DIP switch for selecting options (refer to "Board DIP Switch Settings" on page 13).	–	S1, S2, S10	Refer to "Board DIP Switch Settings" on page 13.
VCC select	U14.AC23	J40	Connect pin 1 and 2 for low-voltage VCC; connect pin 2 and 3 for high-voltage VCC.
SFI/XSBI clock select	–	J51	Connect J51 pins 1 and 2 for 155.52 MHz `clk`; connect pin 2 and 3 for socket `clk` (J45).
100 MHz VCO select	–	J53	Connect J53 pins 1 and 2 for SMT `clk`; connect pin 2 and 3 for socket `clk` (J52).

User I/O Standards

This section summarizes board user I/O functionality and settings, including DIP switches, push buttons, LEDs, and seven-segment displays.

Board DIP Switch Settings

An 8-position DIP switch allows the user to configure board-specific options. Because the board-specific options affect hard-wired device function pins, they are not available for general programming use. The `RU_N_LU` and `MSEL` switches are only needed when the user wants to use the remote/local update block in Stratix II devices to initiate reconfiguration, and if so, to indicate the configuration mode.

Upon power-up or system reset, the `MPGM[2..0]` pins select one of eight possible PLD configuration file images in Flash. The Stratix II device can also point to the configuration file using its `PGM[2..0]` pins (using

ALT_REMOTE IP block in Stratix II devices) that drive the board's SPGM[2..0] nets. Table 10 lists Stratix II device board DIP switch pinouts:

- When the switch is in the ON position a *0* is selected.
- When the switch is in the OFF position, a *1* is selected.

Table 10. Stratix II DIP Switch (S2) Pinouts

Signal Name	DIP Switch (S2) Pin	Max (U1), Stratix II Device (U14) Pin	DIP Position *ON*	DIP Position *OFF*
MPGM0	16	U1.101	0 for PGM0	1 for PGM0
MPGM1	15	U1.102	0 for PGM1	1 for PGM1
MPGM2	14	U1.103	0 for PGM2	1 for PGM2
RU_N_LU	13	U1.22, U14.AG17	Stratix II device local mode	Stratix II device remote mode
MSEL0	12	U1.92, U14.B2	*Note (1)*	*Note (1)*
MSEL1	11	U1.93, U14.F6	*Note (1)*	*Note (1)*
MSEL2	10	U1.94, U14.J10	*Note (1)*	*Note (1)*
MSEL3	9	U1.96, U14.H10	*Note (1)*	*Note (1)*
GND	1	NA	–	–
GND	2	NA	–	–
GND	3	NA	–	–
GND	4	NA	–	–
GND	5	NA	–	–
GND	6	NA	–	–
GND	7	NA	–	–
GND	8	NA	–	–

Note to Table 10:

(1) For more information, refer to *Chapter 3 Configuration & Testing*, of the *Stratix II Device Family Data Sheet*, within the *Stratix II Device Handbook*.

Table 11 lists the Stratix II device board enable DIP switch (S10) pinouts.

Table 11. Stratix II Device Board Enable DIP Switch (S10) Pinouts

Signal Name	DIP Switch (S10) Pin	DIP Position *ON*	DIP Position *OFF*
VINT_PWR_EN	1	VINT_PWR disabled	VINT_PWR enabled
3.3V_EN	2	3.3 V disabled	3.3 V enabled
1.8V_EN	3	1.8 V disabled	1.8 V enabled
-5V2_EN	4	-5.2 V disabled	5.2 V enabled
5V_EN	5	5 V disabled	5 V enabled
2.5V_EN	6	2.5 V disabled	2.5 V enabled
VCCPLL_ENABLE	7	PLL 1.2 V disabled	PLL 1.2 V enabled
VTT_SDn	8	VTT_DDRII disabled	VTT_DDRII enabled
GND	9-16	–	–

User DIP Switch Settings

There is one user DIP switch, and it is reserved for reference design functions and general purpose use. Table 12 lists pin assignments for the user DIP switch:

- When a switch is in the ON position a *0* is selected.
- When the switch is in the OFF position, a *1* is selected.

Table 12. Stratix II User DIP Switch Pinouts (Part 1 of 2)

Signal Name	Dip Switch (S1) Pin	Stratix II (U14) Pin
DIP0	16	K16
DIP1	15	K17
DIP2	14	L17
DIP3	13	H20
DIP4	12	L16
DIP5	11	K15
DIP6	10	J15
DIP7	9	H21
GND	1	NA
GND	2	NA

Table 12. Stratix II User DIP Switch Pinouts (Part 2 of 2)		
Signal Name	**Dip Switch (S1) Pin**	**Stratix II (U14) Pin**
GND	3	NA
GND	4	NA
GND	5	NA
GND	6	NA
GND	7	NA
GND	8	NA

Push Buttons

Push buttons are provided for board-level reset, device-wide reset, and for user-defined functions. Table 13 lists the push-button and LED pinouts.

Table 13. Push Button & LED Pinouts			
Signal Name	**Function**	**Push Button Number**	**Stratix II Device (U14), or MAX (U1) Device**
PB0_IN	Stratix II device, user defined	S3	U14.H11
PB1_IN	Stratix II device, user defined	S4	U14.J11
PB2_IN	Stratix II device, user defined	S5	U14.K11
PB3_IN	Stratix II device, user defined	S6	U14.H12
PB_DEV_CLR_INn	Stratix II device clear	S7	U14.AG19
SYS_RESETn	Initiates a reconfiguration of the FPGA from the selected page	S8	U1.127
SAFE_INn	Resets board, loads FPGA with factory default configuration data	S9	U1.117

General Purpose LEDs

Yellow, surface mount LEDs (SM1206) are provided for general purpose use. The MAX 7256AE device operates as a buffer between the Stratix II device and diodes, as the diodes have a forward voltage (V_{FD}) of 2.1 V and require a 20-mA current to output light at the recommended levels. Table 14 lists the user LED pinouts:

- A logic 0 is driven on the I/O port to turn the LED *ON*.
- A logic 1 is driven on the I/O port to turn the LED *OFF*.

Table 14. User LED Pinout

Signal Name	Reference Designator	MAX Device Connection
USER_LED_DRV0	D13	MAX: U10.106 (input), U1.55 (output)
USER_LED_DRV1	D14	MAX: U10.107 (input), U1.56 (output)
USER_LED_DRV2	D15	MAX: U10.108 (input), U1.60 (output)
USER_LED_DRV3	D16	MAX: U10.109 (input), U1.61 (output)
USER_LED_DRV4	D17	MAX: U10.110 (input), U1.62 (output)
USER_LED_DRV5	D18	MAX: U10.111 (input), U1.63 (output)
USER_LED_DRV6	D19	MAX: U1.65 (input), U1.112 (output)
USER_LED_DRV7	D20	MAX: U1.113 (input), U1.82 (output)

Status LEDs

Surface-mount LED's (SM1206) indicate board status. Table 15 lists the surface-mount LED description, reference designator, and color.

Table 15. Status LEDs (Part 1 of 2)

Signal Name	Description	Ref. Des.	LED Color
DC_INPUT_OK	Indicates input power supply is on.	D1	Blue
FLASH_CE_LEDn	Indicates flash is enabled.	D22	Yellow
USER_CPLD_LEDn	User status LEDs.	D21	Green
LOADING_LEDn	Indicates the Stratix II device configuration is loading.	D12	Green
SAFE_LEDn	Indicates that the default configuration is loaded.	D11	Yellow
ERROR_LEDn	Indicates a system error has occurred.	D10	Red
CONFIG_DONE_LEDn	Indicates Stratix II device configuration is finished.	D9	Green
3.3V_MON	Indicates 3.3 V power is available on the board.	D6	Green
2.5V_MON	Indicates 2.5 V power is available on the board.	D4	Green

Table 15. Status LEDs (Part 2 of 2)

Signal Name	Description	Ref. Des.	LED Color
1.8V_MON	Indicates 1.8 V power is available on the board.	D3	Green
1.2V_MON	Indicates 1.2 V power is available on the board.	D5	Green
RS232 Port A TX	Indicates RS232 Port A is transmitting.	D26	Yellow
RS232 Port A RX	Indicates RS232 Port A is receiving.	D25	Yellow
RS232 Port B TX	Indicates RS232 Port B is transmitting.	D24	Yellow
RS232 Port B RX	Indicates RS232 Port B is receiving.	D23	Yellow
Ethernet Link	Indicates that the Ethernet link is established.	J13	Green
Ethernet Active	Indicates that data transfer is in progress.	J13	Yellow

Seven-Segment LED Displays

Two single-digit, seven-segment LED displays are provided, and each display is controlled by the Stratix II device. Each segment of the display can be illuminated by driving the connected device's I/O pin with a logic 0. Table 16 shows Stratix II device seven-segment LED pinouts through a buffer/driver.

Table 16. Stratix II Device Seven-Segment Display Pinouts

Display Segment	Display Connection	Signal Name	FPGA Connection
A_SEGA	U17.10	DIG_1_A	U14.AK15
B_SEGA	U17.9	DIG_1_B	U14.AE21
C_SEGA	U17.8	DIG_1_C	U14.AE20
D_SEGA	U17.5	DIG_1_D	U14.AK18
E_SEGA	U17.4	DIG_1_E	U14.T11
F_SEGA	U17.2	DIG_1_F	U14.T6
G_SEGA	U17.3	DIG_1_G	U14.AH18
DP_SEGA	U17.7	DIG_1_DP	U14.AL19
A_SEGB	U18.10	DIG_2_A	U14.AH13
B_SEGB	U18.9	DIG_2_B	U14.AG13
C_SEGB	U18.8	DIG_2_C	U14.AJ12
D_SEGB	U18.5	DIG_2_D	U14.AG15
E_SEGB	U18.4	DIG_2_E	U14.AG14
F_SEGB	U18.2	DIG_2_F	U14.AH14
G_SEGB	U18.3	DIG_2_G	U14.AD8
DP_SEGB	U18.7	DIG_2_DP	U14.AC6

Clocking

This section describes the following board clocking generation techniques:

- Oscillators and differential SMA inputs
- HSB clock nets

Oscillators & Differential SMA Inputs

The board has four crystal oscillators. The oscillators are all powered by a 3.3-V power supply and have supply filters to isolate noise from system power planes. This section describes the four oscillators, the differential SMA inputs, and illustrates the board's clocking circuitry.

- A SMT 3.3 V, 33.333 MHz oscillator (Y2) is dedicated to configuration circuitry and is driven also to the Stratix II device and MAX/ MAX II device for general purpose use. There is a simple, low-cost clock buffer to provide a lower-jitter clock to more sources for greater flexibility. The entire 33.333-MHz clock system is low voltage transistor-transistor logic (LVTTL).

- A SMT 3.3 V, 100.000 MHz oscillator (Y3) is used for lower-jitter, high-speed Stratix II device applications. The oscillator is meant as the primary clock source for most FPGA designs. The oscillator has a dual-footprint that allows users to add in their own crystal by disabling the on-board device through a jumper, which increases reliability and allows the use of higher-quality, readily-available SMT crystals. It can be easily replaced with custom frequency oscillators from many different vendors. The clock system is buffered using a 1.8-V high-speed transceiver logic (HSTL) clock buffer before connecting to the Stratix II device.

  The SMA input (J41) allows both the 100 MHz oscillator to be bypassed and the single-ended clock to be brought directly from an external clock source. This clock also goes through the same HSTL buffer as the 100 MHz oscillator. This input is very useful for sweeping frequencies to verify $\mathbf{f_{MAX}}$ performance of designs.

- The 25.000 MHz oscillator is required for the Standard Microsystems 91c111 Ethernet chip as a dedicated reference clock.

- The 155.52 MHz/161 MHz oscillator (dual footprint) is used for providing a clock reference to the SFI/XSBI interface. The board has the 155.52 MHz oscillator soldered down, but the dual footprint allows users to plug in a different frequency oscillator.

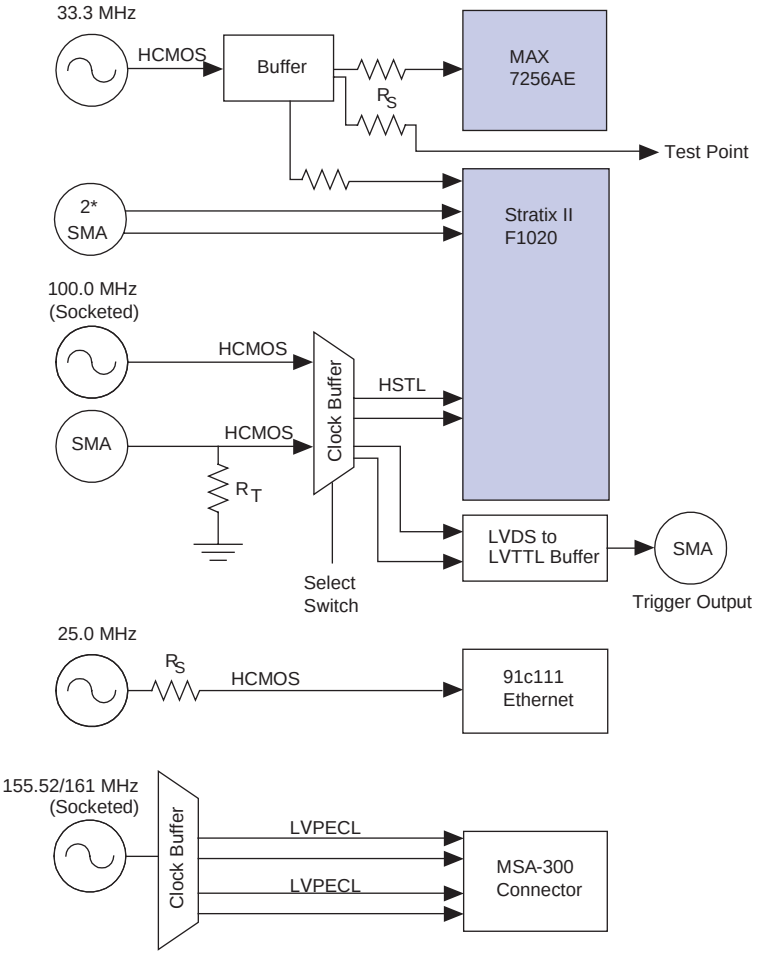
Altera provides a 155.52-MHz standard crystal oscillator with the board. However, designers may use their own 161-MHz, or other frequency, crystal oscillator in the socket.

To use the 161-MHz oscillator, (1) place the oscillator in the socket, (2) remove the shunt between pins 1 and 2 of J51, and (3) place the shunt between pins 2 and 3. To revert back to using the 155.52-MHz oscillator, put the shunt back in its original position (i.e., pins 1 and 2 of J51).

The differential SMA inputs (J26 and J27) allow differential clocks to be brought from external equipment directly to the Stratix II device.

Figure 3 shows a diagram of the board's four oscillators and clocking circuitry.

Figure 3. Stratix II High-Speed Development Board's Clocking Circuitry



Note:

(1) Figure 3 shows only the important blocks of the clocking network. For more information, refer to the board schematics.

HSB Clock Nets

Table 17 lists and describes the Stratix II high-speed development board's critical clock nets.

Table 17. Stratix II High-Speed Development Board's Critical Clock Nets (Part 1 of 2)

Clock Name	Origin	Destination	Description
CLKA_OSC	Oscillator (Y2)	Clock buffer (U20)	33.33 MHz system/configuration input clock for the Stratix II device.
CLKB_OSC	Oscillator (Y3) or (J52)	Clock buffer (U22)	100.00 MHz high speed clock for the Stratix II device.
CLKB_SMA	SMA (J41)	Clock buffer (U22)	High speed clock input for the Stratix II device. This clock may be used instead of the on-board oscillator.
CLK_25MHZ	Crystal osc (Y4)	Ethernet (U30)	25.00 MHz input clock to the LAN91C111 device, XTAL1, pin 127.
CLKB_PLL5_P CLKB_PLL5_N	U22	Stratix II device (U14)	Differential clock input to the Stratix II device.
PLL11_OUT1_P PLL11_OUT1_N	Stratix II device (U14)	SMA (J25) SMA (J29)	Differential SSTL-1.8 clock output from the Stratix II device.
DDRII_REF_CLK_SMA	Stratix II device (U14)	SMA (J32)	DDR2 reference clock input to the Stratix II device.
DDRII_CLKFB_P DDRII_CLKFB_N	Stratix II device (U14)	50 Ω term to VTT_DDRII	DDR2 clock feedback test signal
CLKA_TP_OUT	Clock buffer (U20)	Test point (TP34)	33.33 MHz system/configuration output clock from clock buffer (U20). Can be used for monitoring/debugging.
CLKA_CPLD	Clock buffer (U20)	MAX device (U1) MAX II device (U2)	33.33 MHz system/configuration output clock for MAX/MAX II device.
CLKA_FPGA	Clock buffer (U20)	Stratix II device (U14)	33.33 MHz system/configuration output clock for Stratix II device.
CLKB_TRIG_OUT	Diff clock buffer (U25)	SMA (J48)	CLKB output from the selected input (U22). Useful for triggering during eye diagram measurements.
CLKB_TP_OUT	Diff clock buffer (U25)	Test point (TP46)	CLKB output from the selected input (U22). Can be used for monitoring/debugging.

Table 17. Stratix II High-Speed Development Board's Critical Clock Nets (Part 2 of 2)

Clock Name	Origin	Destination	Description
DPA_SMA_RXCLK_P DPA_SMA_RXCLK_N	SMA (J26) SMA (J27)	Stratix II device (U14)	Differential clock input for source-synchronous (SS) testing.
DPA_SMA_TXCLK_P DPA_SMA_TXCLK_N	Stratix II device (U14)	SMA (J30) SMA (J31)	Differential clock output for SS testing.

High-Speed Interfaces

This section describes the following high-speed interfaces supported by the board:

- SPI-4.2
- HyperTransport
- RapidIO mezzanine card (RMC)
- PMC
- SFI-4.1/XSBI
- Source-synchronous SMAs

SPI-4.2 Interface

Using low voltage differential (LVDS) signaling, the SPI-4.2 interface supports 16 data channels, one DDR clock and one control signal in each direction. Additionally, low voltage transistor-transistor logic (LVTTL) signaling is used for FIFO status, with two status channels and a clock in each direction operating at one quarter of the data rate.

Because the Stratix II device maximum I/O speed is targeted to be 1000 Mbps, Altera supports a clock rate of up to 500 MHz on the SPI-4.2 interface, which results in full-duplex data throughput of up to 16 Gbps.

The signals listed in Table 18 are relative to the Stratix II device as far as the direction of data flow is concerned.

The SPI-4.2 interface uses an HM-Zd interconnect (receptacle) identical to the one used on the Stratix GX development board. The interconnect part number is 1469001-1 from Tyco Electronics. The HM-Zd receptacle will plug into the HM-Zd interconnect (header) 1469002-1 also from Tyco Electronics.

The board reference designator for the HM-Zd interconnect is J37. Table 18 lists the SPI-4.2 interface pinout.

Table 18. SPI-4.2 Interface Pinout (Part 1 of 3)

Signal Name	Stratix II Device (U14) Pin	Hm-Zd Interconnect (J37) Pin
spi_rctl_n	N30	6F
spi_rctl_p	N31	6E
spi_rdat_n0	D31	10D
spi_rdat_n1	E29	9H
spi_rdat_n10	K29	7B
spi_rdat_n11	K31	7H
spi_rdat_n12	L29	6B
spi_rdat_n13	L31	6D
spi_rdat_n14	M29	7D
spi_rdat_n15	N28	6H
spi_rdat_n2	E31	9D
spi_rdat_n3	F29	10F
spi_rdat_n4	F31	10B
spi_rdat_n5	G29	9F
spi_rdat_n6	G31	8F
spi_rdat_n7	H29	8D
spi_rdat_n8	H31	7F
spi_rdat_n9	J31	8B
spi_rdat_p0	D32	10C
spi_rdat_p1	E30	9G
spi_rdat_p10	K30	7A
spi_rdat_p11	K32	7G
spi_rdat_p12	L30	6A
spi_rdat_p13	L32	6C
spi_rdat_p14	M30	7C
spi_rdat_p15	N29	6G
spi_rdat_p2	E32	9C
spi_rdat_p3	F30	10E
spi_rdat_p4	F32	10A
spi_rdat_p5	G30	9E
spi_rdat_p6	G32	8E

Table 18. SPI-4.2 Interface Pinout (Part 2 of 3)

Signal Name	Stratix II Device (U14) Pin	Hm-Zd Interconnect (J37) Pin
spi_rdat_p7	H30	8C
spi_rdat_p8	H32	7E
spi_rdat_p9	J32	8A
spi_rdclk_n	T29	9B
spi_rdclk_p	T30	9A
spi_rsclk	AH19	8G
spi_rstat0	AL26	10H
spi_rstat1	AL8	10G
spi_tctl_n	R24	5D
spi_tctl_p	R25	5C
spi_tdat_n0	H27	2H
spi_tdat_n1	J26	1D
spi_tdat_n10	P26	4B
spi_tdat_n11	P28	4D
spi_tdat_n12	R26	4F
spi_tdat_n13	P24	5F
spi_tdat_n14	T22	3D
spi_tdat_n15	R22	5H
spi_tdat_n2	L23	1B
spi_tdat_n3	K26	1F
spi_tdat_n4	M22	3F
spi_tdat_n5	L25	1H
spi_tdat_n6	M24	3B
spi_tdat_n7	N22	2B
spi_tdat_n8	N26	4H
spi_tdat_n9	N24	2F
spi_tdat_p0	H28	2G
spi_tdat_p1	J27	1C
spi_tdat_p10	P27	4A
spi_tdat_p11	P29	4C
spi_tdat_p12	R27	4E
spi_tdat_p13	P25	5E
spi_tdat_p14	T23	3C
spi_tdat_p15	R23	5G
spi_tdat_p2	L24	1A

Table 18. SPI-4.2 Interface Pinout (Part 3 of 3)

Signal Name	Stratix II Device (U14) Pin	Hm-Zd Interconnect (J37) Pin
spi_tdat_p3	K27	1E
spi_tdat_p4	M23	3E
spi_tdat_p5	L26	1G
spi_tdat_p6	M25	3A
spi_tdat_p7	N23	2A
spi_tdat_p8	N27	4G
spi_tdat_p9	N25	2E
spi_tdclk_n	M26	3H
spi_tdclk_p	M27	3G
spi_tsclk	AJ7	5A
spi_tstat0	AE13	2D
spi_tstat1	AE12	2C

RMC Interface

The 8-bit RapidIO interface has nine TX channels, nine RX channels, one input clock, one output clock, and five control signals. All of the signals, except the control signals, use the 2.5-V LVDS I/O standard. RapidIO is a DDR interface and the target support speed is 500 Mbps to 1000 Mbps per channel (clock speed of 250 MHz to 500 MHz). The control signals use the LVTTL standard.

The RapidIO interface uses an RMC interconnect and can interface to industry standard RMC boards. The interconnect used on the Stratix II high-speed development board is the Samtec receptacle ASP-103612-01. Table 19 shows the RMC interface pinout.

Table 19. RMC Interface Pinout (Part 1 of 3)

Signal Name	Stratix II (U14) Pin	RMC (J57) Pin
rio_cpu_rstn	AM7	F4
rio_i2c_scl	AM8	F16
rio_i2c_sda	AG22	F14
rio_irq_outn	AL23	F8
rio_rclk_n	U31	B5
rio_rclk_p	U32	A5
rio_rd_n0	V30	B1

Table 19. RMC Interface Pinout (Part 2 of 3)

Signal Name	Stratix II (U14) Pin	RMC (J57) Pin
rio_rd_n1	W31	E1
rio_rd_n2	AA31	B3
rio_rd_n3	Y30	E3
rio_rd_n4	AB31	E5
rio_rd_n5	AA29	B7
rio_rd_n6	Y28	E7
rio_rd_n7	AB29	B9
rio_rd_p0	V31	A1
rio_rd_p1	W32	D1
rio_rd_p2	AA32	A3
rio_rd_p3	Y31	D3
rio_rd_p4	AB32	D5
rio_rd_p5	AA30	A7
rio_rd_p6	Y29	D7
rio_rd_p7	AB30	A9
rio_rframe_n	AJ31	E9
rio_rframe_p	AJ32	D9
rio_rmcrdy	AL24	F12
rio_rstn	AM24	F2
rio_tclk_n	W26	B15
rio_tclk_p	W27	A15
rio_td_n0	U22	B19
rio_td_n1	V23	E19
rio_td_n2	W24	B17
rio_td_n3	Y24	E17
rio_td_n4	Y26	E15
rio_td_n5	U27	B13
rio_td_n6	W28	E13
rio_td_n7	V28	B11
rio_td_p0	U23	A19
rio_td_p1	V24	D19
rio_td_p2	W25	A17
rio_td_p3	Y25	D17
rio_td_p4	Y27	D15

Table 19. RMC Interface Pinout (Part 3 of 3)

Signal Name	Stratix II (U14) Pin	RMC (J57) Pin
rio_td_p5	U28	A13
rio_td_p6	W29	D13
rio_td_p7	V29	A11
rio_tframe_n	AA26	E11
rio_tframe_p	AA27	D11
rio_trstn	AK7	C2

PCI Mezzanine Card (PMC) Interface

The board features a 64-bit PCI interface running at 33/66 MHz. The interface is used to facilitate PCI transactions over a PMC interface. The board's PMC interface also supports the PCI-X bus protocol, which offers a 64-bit bus running at 133 MHz.

To support telecom and telephony functionality, the board also supports the PCI telecom mezzanine card (PTMC) specification, including configurations one (UTOPIA II 8-bit data path) and two (TDM, RMII). If the mating card uses only three connectors, other PTMC configurations will be supported. The PTMC is an extension to the PMC specification and is defined in PICMG 2.15 and its update (ECN 1.0). The user-defined signals of the fourth connector are not used on this board.

Another PMC interface supported is the processor PMC (PrPMC), which is particularly well-suited for third-generation (3G) wireless networks and merged router/firewall device applications. Some sample PrPMC cards and their associated processors are PrPMC600 and PrPMC610. Table 20 shows the PMC interface pinout.

Table 20. PMC Interface Pinout (Part 1 of 4)

Signal Name	Stratix II (U14) Pin	PMC (JN1/JN2/JN3) Pin
pmc_ack64n	AJ5	PMCJN2.61
pmc_ad0	AH6	PMCJN3.61
pmc_ad1	AK5	PMCJN3.60
pmc_ad10	AM5	PMCJN2.48
pmc_ad11	AH9	PMCJN3.48
pmc_ad12	AL11	PMCJN3.47
pmc_ad13	AC13	PMCJN2.46
pmc_ad14	AK6	PMCJN2.45

Table 20. PMC Interface Pinout (Part 2 of 4)

Signal Name	Stratix II (U14) Pin	PMC (JN1/JN2/JN3) Pin
pmc_ad15	AM11	PMCJN3.46
pmc_ad16	AB21	PMCJN2.25 / PMCJN2.31
pmc_ad17	AE10	PMCJN3.32
pmc_ad18	AD22	PMCJN2.29
pmc_ad19	AL16	PMCJN3.29
pmc_ad2	AH7	PMCJN3.59
pmc_ad20	AC11	PMCJN2.28
pmc_ad21	AE11	PMCJN3.28
pmc_ad22	AK13	PMCJN3.27
pmc_ad23	AE22	PMCJN2.26
pmc_ad24	AC19	PMCJN2.23
pmc_ad25	AD10	PMCJN3.23
pmc_ad26	AK20	PMCJN2.22
pmc_ad27	AD11	PMCJN3.22
pmc_ad28	AJ17	PMCJN3.21
pmc_ad29	AJ22	PMCJN2.20
pmc_ad3	AG8	PMCJN3.58
pmc_ad30	AL20	PMCJN2.19
pmc_ad31	AG16	PMCJN3.20
pmc_ad32	AB12	PMCJN1.58
pmc_ad33	AC12	PMCJN1.55
pmc_ad34	AG12	PMCJN1.54
pmc_ad35	AJ10	PMCJN1.53
pmc_ad36	AC16	PMCJN1.52
pmc_ad37	AC17	PMCJN1.49
pmc_ad38	AB20	PMCJN1.48
pmc_ad39	AC21	PMCJN1.47
pmc_ad4	AM6	PMCJN3.55
pmc_ad40	AD18	PMCJN1.46
pmc_ad41	AL13	PMCJN1.43
pmc_ad42	AM14	PMCJN1.42
pmc_ad43	AM23	PMCJN1.41
pmc_ad44	AE19	PMCJN1.40
pmc_ad45	AD21	PMCJN1.37

Table 20. PMC Interface Pinout (Part 3 of 4)

Signal Name	Stratix II (U14) Pin	PMC (JN1/JN2/JN3) Pin
pmc_ad46	AF22	PMCJN1.36
pmc_ad47	AG20	PMCJN1.35
pmc_ad48	AH26	PMCJN1.34
pmc_ad49	AG24	PMCJN1.31
pmc_ad5	AG9	PMCJN3.54
pmc_ad50	AM21	PMCJN1.30
pmc_ad51	AH22	PMCJN1.29
pmc_ad52	AH24	PMCJN1.28
pmc_ad53	AJ23	PMCJN1.25
pmc_ad54	AH25	PMCJN1.24
pmc_ad55	AJ25	PMCJN1.23
pmc_ad56	AK25	PMCJN1.22
pmc_ad57	AM26	PMCJN1.19
pmc_ad58	AM27	PMCJN1.18
pmc_ad59	AH28	PMCJN1.17
pmc_ad6	AH8	PMCJN3.53
pmc_ad60	AL27	PMCJN1.16
pmc_ad61	AM28	PMCJN1.13
pmc_ad62	AJ27	PMCJN1.12
pmc_ad63	AM29	PMCJN1.11
pmc_ad7	AK4	PMCJN2.51
pmc_ad8	AL4	PMCJN2.49
pmc_ad9	AM9	PMCJN3.49
pmc_busmoden1	AB11	PMCJN3.7
pmc_busmoden2	AK24	PMCJN2.11
pmc_busmoden3	AK23	PMCJN2.14
pmc_busmoden4	AK22	PMCJN2.16
pmc_c_ben0	AK8	PMCJN3.52
pmc_c_ben1	AK10	PMCJN2.43
pmc_c_ben2	AC20	PMCJN2.32
pmc_c_ben3	AL17	PMCJN3.26
pmc_c_ben4	AL29	PMCJN1.7
pmc_c_ben5	AK28	PMCJN1.6
pmc_c_ben6	AK27	PMCJN1.5

Table 20. PMC Interface Pinout (Part 4 of 4)

Signal Name	Stratix II (U14) Pin	PMC (JN1/JN2/JN3) Pin
pmc_c_ben7	AJ28	PMCJN1.4
pmc_clk_loop_in	AM19	–
pmc_clk_loop_out	AJ18	–
pmc_clk0	AL18	PMCJN3.13
pmc_devseln	AL12	PMCJN3.37
pmc_framen	AJ13	PMCJN3.33
pmc_gntn	AD14	PMCJN3.16
pmc_intan	AG23	PMCJN3.4
pmc_intbn	AB18	PMCJN3.5
pmc_intcn	AB15	PMCJN3.6
pmc_intdn	AC15	PMCJN3.9
pmc_irdyn	AK17	PMCJN3.36
pmc_lockn	AM12	PMCJN3.40
pmc_m66en	AM4	PMCJN2.47
pmc_monarchn	AC14	PMCJN2.64
pmc_par	AK11	PMCJN3.43
pmc_par64	AL28	PMCJN1.10
pmc_perrn	AB17	PMCJN2.39
pmc_req64n	AH5	PMCJN3.64
pmc_reqn	AL22	PMCJN3.17
pmc_resetn	AM17	PMCJN2.13
pmc_serrn	AK12	PMCJN2.42
pmc_stopn	AC18	PMCJN2.38
pmc_trdyn	AH16	PMCJN2.35
pcixcap	AH16	PMCJN3.39

Three connectors—PMCJN1, PMCJN2, PMCJN3—are used to support the 64-bit interface, and their part number is 71439-0164 from Molex.

HyperTransport Interface

The HyperTransport interface has nine TX channels, nine RX channels, two clock signals, and two control signals. All the signals use the HyperTransport I/O standard, which is a differential I/O standard using

a 2.5-V supply. HyperTransport is a DDR interface and the target support speed is 800 Mbps to 1000 Mbps per channel (clock speed of 400 MHz to 500 MHz). Table 21 shows the HyperTransport interface pinout.

The connector used for the HyperTransport interface is the Samtec QTE-060-01-FD-EM3-GP, which is an edge-mount connector.

Table 21. HyperTransport Interface Pinout (Part 1 of 2)

Signal Name	Stratix II (U14) Pin	HyperTransport (J56) Pin
ht_pwrok	AE27	25
ht_resetn	AE28	23
ht_rx_cad_n0	AH31	89
ht_rx_cad_n1	AG29	83
ht_rx_cad_n2	AG31	75
ht_rx_cad_n3	AF29	69
ht_rx_cad_n4	AF31	55
ht_rx_cad_n5	AE29	49
ht_rx_cad_n6	AE31	43
ht_rx_cad_n7	AD31	35
ht_rx_cad_p0	AH32	91
ht_rx_cad_p1	AG30	85
ht_rx_cad_p2	AG32	77
ht_rx_cad_p3	AF30	71
ht_rx_cad_p4	AF32	57
ht_rx_cad_p5	AE30	51
ht_rx_cad_p6	AE32	45
ht_rx_cad_p7	AD32	37
ht_rx_clk_n	AJ29	63
ht_rx_clk_p	AJ30	65
ht_rx_ctl_n	AC31	92
ht_rx_ctl_p	AC32	90
ht_tx_cad_n0	AA24	32
ht_tx_cad_n1	AC26	38
ht_tx_cad_n2	AE25	46
ht_tx_cad_n3	AD26	52
ht_tx_cad_n4	AD24	66
ht_tx_cad_n5	AC24	72

Table 21. HyperTransport Interface Pinout (Part 2 of 2)

Signal Name	Stratix II (U14) Pin	HyperTransport (J56) Pin
ht_tx_cad_n6	AB23	78
ht_tx_cad_n7	AA22	86
ht_tx_cad_p0	AA25	30
ht_tx_cad_p1	AC27	36
ht_tx_cad_p2	AE26	44
ht_tx_cad_p3	AD27	50
ht_tx_cad_p4	AD25	64
ht_tx_cad_p5	AC25	70
ht_tx_cad_p6	AB24	76
ht_tx_cad_p7	AA23	84
ht_tx_clk_n	AB25	58
ht_tx_clk_p	AB26	56
ht_tx_ctl_n	Y22	92
ht_tx_ctl_p	Y23	90

SFI-4.1 & XSBI Interfaces

The board supports OC-192/STM-64 SONET/SDH and 10-Gigabit Ethernet (wide area network, physical layer [WAN-PHY] and local area network, physical layer [LAN-PHY]) optical transponders compatible with the MSA300 over SFI-4.1 and XSBI interfaces. All of the signals use the LVDS standard. The SFI-4.1 and XSBI interfaces use single-edge clocking. The SFI-4.1 operates at 622.08 MHz per bit for total throughput of 9,953.28 Mbps, and XSBI operates at 644.53125 MHz for total throughput of 1,0312.5 Mbps—required to carry the 10 Gbps of 64b/66b encoded data.

The signal connections for the XSBI and SFI-4 interfaces are identical; however, the data rate is slightly different.

Table 22 shows the SFI-4.1 and XSBI interface MSA-300 connector pinout.

Table 22. SFI-4.1 & XSBI Interface MSA-300 Connector Pinout (Part 1 of 3)

Signal Name	Stratix II (U14) Pin	MSA-300 (J28) Pin
sfi_ffu_rx_n1	Y3	G14
sfi_ffu_rx_n2	AA2	J8
sfi_ffu_rx_p1	Y2	G13
sfi_ffu_rx_p2	AA1	J7
sfi_ffu_tx_n1	V5	J24
sfi_ffu_tx_p1	V4	J23
sfi_i2c_clk	AK21	K15
sfi_i2c_data	AJ21	K18
sfi_rx_clk_n	U4	E14
sfi_rx_clk_p	U3	E13
sfi_rx_n0	AJ2	A2
sfi_rx_n1	AG4	A5
sfi_rx_n2	AE4	A8
sfi_rx_n3	AB2	A11
sfi_rx_n4	AH2	C2
sfi_rx_n5	AF2	C5
sfi_rx_n6	AD2	C8
sfi_rx_n7	AB4	C11
sfi_rx_n8	AH4	E2
sfi_rx_n9	AF4	E5
sfi_rx_n10	AC2	E8
sfi_rx_n11	AA4	E11
sfi_rx_n12	AG2	G2
sfi_rx_n13	AE2	G5
sfi_rx_n14	AC4	G8
sfi_rx_n15	Y5	G11
sfi_rx_p0	AJ1	A1
sfi_rx_p1	AG3	A4
sfi_rx_p2	AE3	A7
sfi_rx_p3	AB1	A10
sfi_rx_p4	AH1	C1
sfi_rx_p5	AF1	C4

Table 22. SFI-4.1 & XSBI Interface MSA-300 Connector Pinout (Part 2 of 3)

Signal Name	Stratix II (U14) Pin	MSA-300 (J28) Pin
sfi_rx_p6	AD1	C7
sfi_rx_p7	AB3	C10
sfi_rx_p8	AH3	E1
sfi_rx_p9	AF3	E4
sfi_rx_p10	AC1	E7
sfi_rx_p11	AA3	E10
sfi_rx_p12	AG1	G1
sfi_rx_p13	AE1	G4
sfi_rx_p14	AC3	G7
sfi_rx_p15	Y4	G10
sfi_tx_clk_n	AA9	G29
sfi_tx_clk_p	AA8	G28
sfi_tx_n0	AD7	A17
sfi_tx_n1	AD9	A20
sfi_tx_n2	AB10	A23
sfi_tx_n3	Y7	A26
sfi_tx_n4	AC7	C17
sfi_tx_n5	AC9	C20
sfi_tx_n6	AA11	C23
sfi_tx_n7	W5	C26
sfi_tx_n8	AB6	E17
sfi_tx_n9	AB8	E20
sfi_tx_n10	Y11	E23
sfi_tx_n11	W7	E26
sfi_tx_n12	AA7	G17
sfi_tx_n13	Y9	G20
sfi_tx_n14	W9	G23
sfi_tx_n15	V7	G26
sfi_tx_p0	AD6	A16
sfi_tx_p1	AD8	A19
sfi_tx_p2	AB9	A22
sfi_tx_p3	Y6	A25
sfi_tx_p4	AC6	C16
sfi_tx_p5	AC8	C19

Table 22. SFI-4.1 & XSBI Interface MSA-300 Connector Pinout (Part 3 of 3)

Signal Name	Stratix II (U14) Pin	MSA-300 (J28) Pin
sfi_tx_p6	AA10	C22
sfi_tx_p7	W4	C25
sfi_tx_p8	AB5	E16
sfi_tx_p9	AB7	E19
sfi_tx_p10	Y10	E22
sfi_tx_p11	W6	E25
sfi_tx_p12	AA6	G16
sfi_tx_p13	Y8	G19
sfi_tx_p14	W8	G22
sfi_tx_p15	V6	G25
sfi_txp_clk_n	AJ4	E29
sfi_txp_clk_p	AJ3	E28

Source-Synchronous SMA Interface

The source-synchronous SMA interface has two TX channels, two RX channels, one TX clock, and one RX clock. The connectors are designed to perform eye-diagram or loopback testing using coaxial cables. The maximum intended speed is 1.0 Gbps. Table 23 shows the source-synchronous SMA connector pinout.

Table 23. Source-Synchronous SMA Connector Pinout

Net Name	Reference Designator	Stratix II Pin Connection
DPA_SMA_TX_P0 DPA_SMA_TX_N0	J42 J43	U5 U6
DPA_SMA_TX_P1 DPA_SMA_TX_N1	J49 J50	U10 U11
DPA_SMA_TXCLK_P DPA_SMA_TXCLK_N	J30 J31	V9 V10
DPA_SMA_RX_P0 DPA_SMA_RX_N0	J42 J43	V2 V3
DPA_SMA_RX_P1 DPA_SMA_RX_N1	J38 J39	W1 W2
DPA_SMA_RXCLK_P DPA_SMA_RXCLK_N	J26 J27	U1 U2

10/100 Ethernet Interface

The board provides a 10/100 Ethernet interface for Ethernet connections up to 100 Mbps. The reference designator for the 10/100 Ethernet interface is J13. Table 24 shows the 10/100 Ethernet interface pinout.

Memory Interfaces

This section describes the shared bus, Flash, SRAM, and DDR2 DIMM memory interfaces.

Shared Bus Interface

The board employs the same shared-bus architecture as the Altera Nios® development boards designed for Stratix II and Cyclone™ devices. The shared-bus architecture allows for a 3X reduction in pins for asynchronous peripherals and memory devices. The bus shares address and data for the following components:

- Flash
- SRAM
- LAN91C111 Ethernet MAC/PHY

Table 24 shows the Flash, SRAM, Ethernet shared-bus pinout.

Table 24. Flash, SRAM, & Ethernet Shared-Bus Pinout (Part 1 of 3)

Signal Name	Stratix II Pin Number (U14)	Flash Pin Number (U32)	SRAM Pin Number (U31,U29)	Ethernet Pin Number (U30)
FSE_A0	J6	51	–	–
FSE_A1	J7	31	–	78
FSE_A2	J8	26	1	79
FSE_A3	J9	25	2	80
FSE_A4	K8	24	3	81
FSE_A5	K9	23	4	82
FSE_A6	L9	22	5	83
FSE_A7	L10	21	18	84
FSE_A8	L7	20	19	85
FSE_A9	L8	10	20	86
FSE_A10	K6	9	21	87
FSE_A11	K7	8	22	88
FSE_A12	L5	7	23	89
FSE_A13	L6	6	24	90
FSE_A14	M10	5	25	91
FSE_A15	M11	4	26	92

Table 24. Flash, SRAM, & Ethernet Shared-Bus Pinout (Part 2 of 3)

Signal Name	Stratix II Pin Number (U14)	Flash Pin Number (U32)	SRAM Pin Number (U31,U29)	Ethernet Pin Number (U30)
FSE_A16	M8	3	27	–
FSE_A17	M9	54	42	–
FSE_A18	M6	19	43	–
FSE_A19	M7	18	44	–
FSE_A20	N6	11	–	–
FSE_A21	N7	12	–	–
FSE_A22	N8	15	–	–
FSE_A23	N9	2	–	–
FSE_A24	P8	1	–	–
FSE_A25	P9	56	–	–
FSE_A26	T5	55	–	–
FSE_D0	D1	35	U31.7	107
FSE_D1	D2	37	U31.8	106
FSE_D2	E3	39	U31.9	105
FSE_D3	E4	41	U31.10	104
FSE_D4	E1	44	U31.13	102
FSE_D5	E2	46	U31.14	101
FSE_D6	F3	48	U31.15	100
FSE_D7	F4	50	U31.16	99
FSE_D8	F1	–	U31.29	76
FSE_D9	F2	–	U31.30	75
FSE_D10	G3	–	U31.31	74
FSE_D11	G4	–	U31.32	73
FSE_D12	G1	–	U31.35	71
FSE_D13	G2	–	U31.36	70
FSE_D14	J3	–	U31.37	69
FSE_D15	J4	–	U31.38	68
FSE_D16	H1	–	U29.7	66
FSE_D17	H2	–	U29.8	65
FSE_D18	J1	–	U29.9	64
FSE_D19	J2	–	U29.10	63
FSE_D20	K3	–	U29.13	61
FSE_D21	K4	–	U29.14	60

Table 24. Flash, SRAM, & Ethernet Shared-Bus Pinout (Part 3 of 3)

Signal Name	Stratix II Pin Number (U14)	Flash Pin Number (U32)	SRAM Pin Number (U31,U29)	Ethernet Pin Number (U30)
FSE_D22	K1	–	U29.15	59
FSE_D23	K2	–	U29.16	58
FSE_D24	L3	–	U29.29	56
FSE_D25	L4	–	U29.30	55
FSE_D26	N4	–	U29.31	54
FSE_D27	N5	–	U29.32	53
FSE_D28	M3	–	U29.35	51
FSE_D29	M4	–	U29.36	50
FSE_D30	L1	–	U29.37	49
FSE_D31	L2	–	U29.38	48

Flash Interface

The 128 MB AMD uniform sector Flash memory device (AM29LV128MH113REI) is the board's non-volatile memory. Additionally, the board has:

- A footprint for an AMD Flash device that supports common flash interface (CFI) programming algorithms.
- A common TSOP-56 pinout that is expandable from 8 MB to 128 MB in a single package.

The Flash device qualifies as part of the shared bus circuitry. The signals for the shared bus are listed in Table 24.

Table 25 on page 40 shows an example Stratix II device 16 MB Flash memory map. The memory map is a generic starting point and **NOT** necessarily a definitive map.

User Code Space and areas marked *Other* are reserved for Nios embedded processor software images and other binary files for use in demos, etc.

Configuration files can be placed closer than Table 25 shows, and is accomplished by increasing the complexity of the configuration state machine to start counting on non-power-of-two address offsets. For example, a file of just over 2 MB needs 4 MB to be placed in a power-of-

two offset base address. This assures the smallest possible address counter. Alternatively, start the counter at 3 MB with a slightly larger counter, or even at 2.5 MB with yet a larger counter.

Table 25. Stratix II Device 16 MB Flash Memory Map

Block Name	Address
PLD Design 5 / Other	0x0FFF.FFFF 0x0E00.0000
PLD Design 4 / Other	0x0DFF.FFFF 0x0C00.0000
PLD Design 3 / Other	0x0BFF.FFFF 0x0A00.0000
PLD Design 2 / Other	0x09FF.FFFF 0x0800.0000
PLD Design 1	0x07FF.FFFF 0x0600.0000
PLD Design 0	0x05FF.FFFF 0x0400.0000
Safe Design	0x03FF.FFFF 0x0200.0000
User Code Space	0x01FF.FFFF 0x0000.0000

SRAM Interface

The Stratix II high-speed development board has two 256K x 16 SRAM devices as part of the shared bus. The devices are wired in parallel to provide a 256K x 32 interface to the Stratix II device (i.e., 1 MB of contiguous space). The signals for the shared bus are listed in Table 24 on page 37.

DDR2 SDRAM DIMM Interface

The board supports a DDR2 SDRAM DIMM memory interface at 267 MHz (533 Mbps). The intended target is a Micron DIMM MT9HTF3272A-53E. DIMMs from other vendors are used as they become available. The intended target Micron DIMM is a 32 x 72 (256 MB) module. The interface is connected to banks three and four of the Stratix II device and uses 1.8-V power supply and 0.9-V for VTT and Vref.

Table 26 shows the DDR2 SDRAM DIMM connector pinouts and the connection to the Stratix II device.

Table 26. DDR2 SDRAM DIMM Pinout (Part 1 of 8)

Signal Name	Pin Number	Stratix II Pin Number (U14)
1.8V_DDRII	51	N/A
1.8V_DDRII	53	N/A
1.8V_DDRII	56	N/A
1.8V_DDRII	59	N/A
1.8V_DDRII	62	N/A
1.8V_DDRII	64	N/A
1.8V_DDRII	67	N/A
1.8V_DDRII	69	N/A
1.8V_DDRII	72	N/A
1.8V_DDRII	75	N/A
1.8V_DDRII	78	N/A
1.8V_DDRII	170	N/A
1.8V_DDRII	172	N/A
1.8V_DDRII	175	N/A
1.8V_DDRII	178	N/A
1.8V_DDRII	181	N/A
1.8V_DDRII	184	N/A
1.8V_DDRII	187	N/A
1.8V_DDRII	189	N/A
1.8V_DDRII	191	N/A
1.8V_DDRII	194	N/A
1.8V_DDRII	197	N/A
1.8V_DDRII	238	N/A
DDRII_CB0	42	E13
DDRII_CB1	43	D13
DDRII_CB2	48	D14
DDRII_CB3	49	F15
DDRII_CB4	161	G13
DDRII_CB5	162	F13
DDRII_CB6	167	A14
DDRII_CB7	168	B14

Table 26. DDR2 SDRAM DIMM Pinout (Part 2 of 8)

Signal Name	Pin Number	Stratix II Pin Number (U14)
DDRII_CLK_N0	186	C15
DDRII_CLK_N1	138	D16
DDRII_CLK_N2	221	E15
DDRII_CLK_P0	185	B15
DDRII_CLK_P1	137	C16
DDRII_CLK_P2	220	D15
DDRII_DIMM_A0	188	K20
DDRII_DIMM_A1	183	L19
DDRII_DIMM_A10	70	K21
DDRII_DIMM_A11	57	H14
DDRII_DIMM_A12	176	J13
DDRII_DIMM_A13	196	L20
DDRII_DIMM_A14	174	J12
DDRII_DIMM_A15	173	L13
DDRII_DIMM_A2	63	K19
DDRII_DIMM_A3	182	J19
DDRII_DIMM_A4	61	L18
DDRII_DIMM_A5	60	K18
DDRII_DIMM_A6	180	L15
DDRII_DIMM_A7	58	J14
DDRII_DIMM_A8	179	K14
DDRII_DIMM_A9	177	L14
DDRII_DIMM_BA0	71	G20
DDRII_DIMM_BA1	190	J20
DDRII_DIMM_BA2	54	K13
DDRII_DIMM_CASN	74	H22
DDRII_DIMM_CLKE0	52	K12
DDRII_DIMM_CLKE1	171	L12
DDRII_DIMM_CSN0	193	J21
DDRII_DIMM_CSN1	76	K22
DDRII_DIMM_ODT0	195	F25
DDRII_DIMM_ODT1	77	L21
DDRII_DIMM_RASN	192	G21

Table 26. DDR2 SDRAM DIMM Pinout (Part 3 of 8)		
Signal Name	**Pin Number**	**Stratix II Pin Number (U14)**
DDRII_DIMM_WEN	73	G22
DDRII_DM0	125	B5
DDRII_DM1	134	B8
DDRII_DM2	146	C10
DDRII_DM3	155	C12
DDRII_DM4	202	B21
DDRII_DM5	211	B23
DDRII_DM6	223	D25
DDRII_DM7	232	C28
DDRII_DM8	164	C13
DDRII_DQ0	3	D6
DDRII_DQ1	4	D5
DDRII_DQ10	21	A8
DDRII_DQ11	22	C9
DDRII_DQ12	131	E7
DDRII_DQ13	132	B7
DDRII_DQ14	140	C8
DDRII_DQ15	141	A9
DDRII_DQ16	24	F8
DDRII_DQ17	25	F10
DDRII_DQ18	30	B10
DDRII_DQ19	31	D10
DDRII_DQ2	9	A4
DDRII_DQ20	143	E8
DDRII_DQ21	144	D8
DDRII_DQ22	149	D11
DDRII_DQ23	150	A10
DDRII_DQ24	33	G11
DDRII_DQ25	34	A11
DDRII_DQ26	39	E11
DDRII_DQ27	40	D12
DDRII_DQ28	152	G10
DDRII_DQ29	153	B11

Table 26. DDR2 SDRAM DIMM Pinout (Part 4 of 8)

Signal Name	Pin Number	Stratix II Pin Number (U14)
DDRII_DQ3	10	A5
DDRII_DQ30	158	A12
DDRII_DQ31	159	G12
DDRII_DQ32	80	C20
DDRII_DQ33	81	B20
DDRII_DQ34	86	A22
DDRII_DQ35	87	C22
DDRII_DQ36	199	E19
DDRII_DQ37	200	E20
DDRII_DQ38	205	C21
DDRII_DQ39	206	A21
DDRII_DQ4	122	E5
DDRII_DQ40	89	A23
DDRII_DQ41	90	C23
DDRII_DQ42	95	D23
DDRII_DQ43	96	F23
DDRII_DQ44	208	F22
DDRII_DQ45	209	D21
DDRII_DQ46	214	C24
DDRII_DQ47	215	A24
DDRII_DQ48	98	A26
DDRII_DQ49	99	C25
DDRII_DQ5	123	C6
DDRII_DQ50	107	E26
DDRII_DQ51	108	E27
DDRII_DQ52	217	E24
DDRII_DQ53	218	A25
DDRII_DQ54	226	D26
DDRII_DQ55	227	C26
DDRII_DQ56	110	A29
DDRII_DQ57	111	C27
DDRII_DQ58	116	D28
DDRII_DQ59	117	E28

Table 26. DDR2 SDRAM DIMM Pinout (Part 5 of 8)		
Signal Name	**Pin Number**	**Stratix II Pin Number (U14)**
DDRII_DQ6	128	B4
DDRII_DQ60	229	A27
DDRII_DQ61	230	A28
DDRII_DQ62	235	B29
DDRII_DQ63	236	D27
DDRII_DQ7	129	A6
DDRII_DQ8	12	E6
DDRII_DQ9	13	A7
DDRII_DQS_P0	7	C4
DDRII_DQS_P1	16	D7
DDRII_DQS_P2	28	F9
DDRII_DQS_P3	37	F11
DDRII_DQS_P4	84	D19
DDRII_DQS_P5	93	D22
DDRII_DQS_P6	105	B25
DDRII_DQS_P7	114	B27
DDRII_DQS_P8	46	F14
DDRII_RESETN	18	E22
DDRII_SCL	120	B28
DDRII_SDA	119	J22
GND	2	N/A
GND	5	N/A
GND	8	N/A
GND	11	N/A
GND	14	N/A
GND	17	N/A
GND	20	N/A
GND	23	N/A
GND	26	N/A
GND	29	N/A
GND	32	N/A
GND	35	N/A
GND	38	N/A

Table 26. DDR2 SDRAM DIMM Pinout (Part 6 of 8)

Signal Name	Pin Number	Stratix II Pin Number (U14)
GND	41	N/A
GND	44	N/A
GND	47	N/A
GND	50	N/A
GND	65	N/A
GND	66	N/A
GND	79	N/A
GND	82	N/A
GND	85	N/A
GND	88	N/A
GND	91	N/A
GND	94	N/A
GND	97	N/A
GND	100	N/A
GND	101	N/A
GND	103	N/A
GND	106	N/A
GND	109	N/A
GND	112	N/A
GND	115	N/A
GND	118	N/A
GND	121	N/A
GND	124	N/A
GND	127	N/A
GND	130	N/A
GND	133	N/A
GND	136	N/A
GND	139	N/A
GND	142	N/A
GND	145	N/A
GND	148	N/A
GND	151	N/A
GND	154	N/A

Table 26. DDR2 SDRAM DIMM Pinout (Part 7 of 8)		
Signal Name	**Pin Number**	**Stratix II Pin Number (U14)**
GND	157	N/A
GND	160	N/A
GND	163	N/A
GND	166	N/A
GND	169	N/A
GND	198	N/A
GND	201	N/A
GND	204	N/A
GND	207	N/A
GND	210	N/A
GND	213	N/A
GND	216	N/A
GND	219	N/A
GND	222	N/A
GND	225	N/A
GND	228	N/A
GND	231	N/A
GND	234	N/A
GND	237	N/A
GND	239	N/A
GND	240	N/A
NC	6	N/A
NC	15	N/A
NC	19	N/A
NC	27	N/A
NC	36	N/A
NC	45	N/A
NC	55	N/A
NC	68	N/A
NC	83	N/A
NC	92	N/A
NC	102	N/A
NC	104	N/A

Table 26. DDR2 SDRAM DIMM Pinout (Part 8 of 8)

Signal Name	Pin Number	Stratix II Pin Number (U14)
NC	113	N/A
NC	126	N/A
NC	135	N/A
NC	147	N/A
NC	156	N/A
NC	165	N/A
NC	203	N/A
NC	212	N/A
NC	224	N/A
NC	233	N/A
VREF_DDRII	1	N/A

System Monitoring Interfaces

To increase the ability to provide more information about a design—or potential demo—without requiring a great deal of equipment, the Stratix II development board includes several devices designed for real-time, board monitoring. This includes the Stratix II FPGA temperature, various system voltages, and overall system power consumption. This section provides details about the application specific standard products (ASSPs) used to add this functionality.

Temperature Sense

The Maxim 1619 temperature sense chip can read subtle changes in voltage-drop across the Stratix II temperature sense diode circuit. This is useful in doing on-the-fly temperature reading by chip designs versus manual measurements. The MAX1619 comes in a QSOP-16 package and provides the following features:

- Two measurement channels
  - Local (MAX1619)
  - Remote (Stratix II device)
- +/- 2°C accuracy
- Programmable over/under temperature outputs
- SMBus interface for real-time readings

Power Sense

A Linear Technology (LTC2901), quad-voltage-watchdog device monitors board voltages. The 3.3-V, 2.5-V, 1.8-V, and 1.2-V monitoring signals are connected to green LEDs to provide immediate visual voltage status. This device is used in mode 11 and only allows monitoring of the following voltages:

- 3.3 V (derived from 3.3 V)
- 2.5 V (derived from 3.3 V)
- 1.8 V (from switching supply)
- 1.2 V (from switching supply)

Board Stack-Up

The board is manufactured using standard FR4 dielectric and through hole vias. The nominal impedance is 50 Ω for single-ended traces and 100 Ω for differential traces. The impedance tolerance is ±10%. The board thickness is 90.20±7 mils. Table 27 shows the Stratix II development board's layer stack-up.

Table 27. Stratix II Development Board's Layer Stack-Up (Part 1 of 2)
Notes (1), (2)

Layer Number	Layer Type	Description	Thickness & Tolerances	
			Copper Thickness (Mils)	Laminate (Mils)
1	Top	Foil	0.6	
		Pre-preg		3
2	GND plane		1.2	
		Core		4
3	Signal		0.6	
		Pre-preg		8
4	Signal		0.6	
		Core		4
5	GND plane		1.2	
		Pre-preg		4
6	Signal		0.6	
		Core		12
7	GND plane		1.2	
		Pre-preg		4
8	GND plane		1.2	

Table 27. Stratix II Development Board's Layer Stack-Up (Part 2 of 2)
Notes (1), (2)

Layer Number	Layer Type	Description	Thickness & Tolerances	
			Copper Thickness (Mils)	Laminate (Mils)
		Core		12
9	Signal		0.6	
		Pre-preg		4
10	GND		1.2	
		Core		4
11	Signal		0.6	
		Pre-preg		8
12	Signal		0.6	
		Core		
13	GND plane		1.2	
		Pre-preg		3
14	Bottom		0.6	

Notes to Table 27:
(1) 0.5 ounces of copper is equivalent to a 0.6 mils trace width.
(2) Total board height is 90.20±7 mils

Termination Schemes

This section outlines the following three termination schemes used for the board's high speed and memory interfaces:

- DDR2 SDRAM DIMM termination scheme
- SFI-4.1/XSBI termination scheme
- High speed interfaces (except SFI-4.1/XSBI) termination scheme

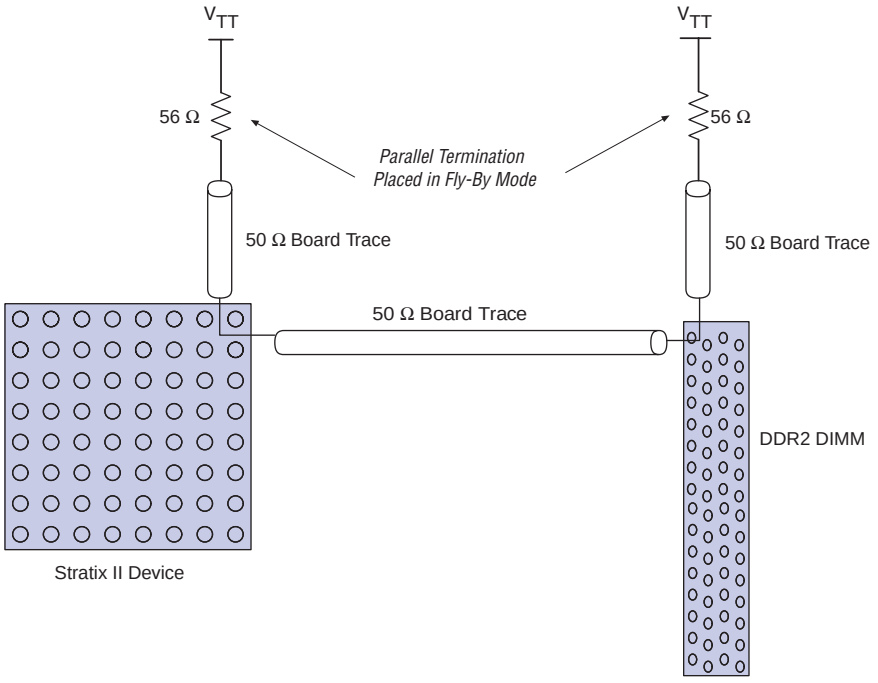
DDR2 SDRAM DIMM Termination Scheme

The DDR2 SDRAM DIMM interface has bi-directional and uni-directional signals, and the termination scheme is different for both types of signals.

Bi-Directional Signals

For bi-directional signals (i.e., DQ, DQS, DM, and parity bit signals), the board uses a dual-parallel termination scheme with 56 Ω resistors, see Figure 4. The resistors are placed in fly-by mode.

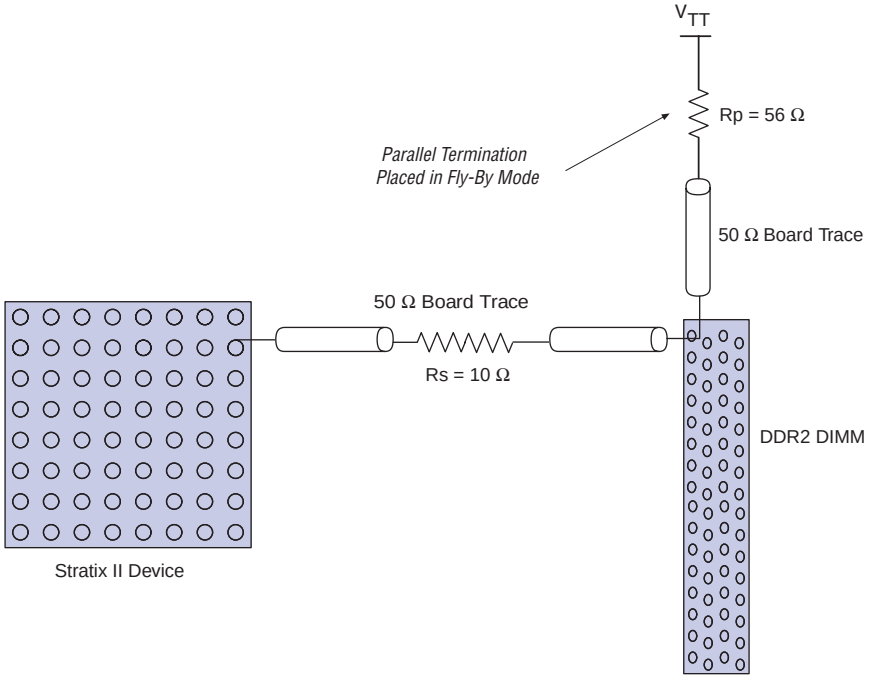
Figure 4. DDR2 DIMM Bi-Directional Signal (DQ, DQS, DM, & Parity Bits) Termination Scheme



Uni-Directional Signals

For uni-directional signals (i.e., address and control signals)—transmitting from the Stratix II device to the DIMM—the board uses a 10 Ω resistor-in-series in conjunction with a 56 Ω pull-up. See Figure 5.

Figure 5. DDR2 DIMM Uni-Directional Signal (Address & Control) Termination Scheme



The clocks of the DIMM interfaces are terminated on the DIMM itself, so no termination is required on the board.

SFI-4.1/XSBI Termination Scheme

The on-chip termination (OCT) feature of the Stratix II device is used to terminate the signals on the SFI-4.1/XSBI interface. Thus, no termination resistors are present on the SFI-4.1/XSBI interface. The differential clocks transmitting to the Stratix II PLL inputs are terminated with a 100-Ω resistor.

High-Speed Interfaces (Except SFI-4.1/XSBI) Termination Scheme

All of the board's high-speed interfaces (SPI-4.2, RapidIO, HyperTransport, SS SMA)—except SFI-4.1/XSBI—are terminated with a 100-Ω resistor close to the Stratix II device's receiver pins.

Stratix II Device Pinout

Table 28 shows the Stratix II device pinout, both alphabetical by signal name and alphabetical by pin number.

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 1 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
1.2v_int	AA12	A10	ddrii_dq23
1.2v_int	AC10	A11	ddrii_dq25
1.2v_int	AD15	A12	ddrii_dq30
1.2v_int	AE18	A13	gnd
1.2v_int	AE8	A14	ddrii_cb6
1.2v_int	AF25	A15	1.8v
1.2v_int	H15	A16	ddrii_clkfb_p
1.2v_int	H25	A17	clkb_pll5_p
1.2v_int	H7	A18	1.8v
1.2v_int	J18	A19	nc
1.2v_int	K10	A2	gnd
1.2v_int	K23	A20	gnd
1.2v_int	M21	A21	ddrii_dq39
1.2v_int	N13	A22	ddrii_dq34
1.2v_int	N15	A23	ddrii_dq40
1.2v_int	N17	A24	ddrii_dq47
1.2v_int	N19	A25	ddrii_dq53
1.2v_int	P14	A26	ddrii_dq48
1.2v_int	P16	A27	ddrii_dq60
1.2v_int	P18	A28	ddrii_dq61
1.2v_int	P20	A29	ddrii_dq56
1.2v_int	R13	A3	1.8v
1.2v_int	R15	A30	1.8v
1.2v_int	R17	A31	gnd

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 2 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
1.2v_int	R19	A4	ddrii_dq2
1.2v_int	T14	A5	ddrii_dq3
1.2v_int	T16	A6	ddrii_dq7
1.2v_int	T18	A7	ddrii_dq9
1.2v_int	T20	A8	ddrii_dq10
1.2v_int	T9	A9	ddrii_dq15
1.2v_int	U13	AA1	sfi_ffu_rx_p2
1.2v_int	U15	AA10	sfi_tx_p6
1.2v_int	U17	AA11	sfi_tx_n6
1.2v_int	U19	AA12	1.2v_int
1.2v_int	U24	AA13	3.3v
1.2v_int	U7	AA14	gnd
1.2v_int	V14	AA15	3.3v
1.2v_int	V16	AA16	3.3v
1.2v_int	V18	AA17	3.3v
1.2v_int	V20	AA18	3.3v
1.2v_int	V25	AA19	gnd
1.2v_int	W13	AA2	sfi_ffu_rx_n2
1.2v_int	W15	AA20	3.3v
1.2v_int	W17	AA21	gnd
1.2v_int	W19	AA22	ht_tx_cad_n7
1.2v_int	W21	AA23	ht_tx_cad_p7
1.2v_int	Y14	AA24	ht_tx_cad_n0
1.2v_int	Y16	AA25	ht_tx_cad_p0
1.2v_int	Y18	AA26	rio_tframe_n
1.2v_int	Y20	AA27	rio_tframe_p
1.2v_lin	AE15	AA28	2.5v
1.2v_lin	AE7	AA29	rio_rd_n5
1.2v_lin	AF18	AA3	sfi_rx_p11
1.2v_lin	AF26	AA30	rio_rd_p5
1.2v_lin	G15	AA31	rio_rd_n2
1.2v_lin	H17	AA32	rio_rd_p2

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 3 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
1.2v_lin	H26	AA4	sfi_rx_n11
1.2v_lin	H8	AA5	2.5v
1.2v_lin	R9	AA6	sfi_tx_p12
1.2v_lin	T24	AA7	sfi_tx_n12
1.2v_lin	U9	AA8	sfi_tx_clk_p
1.2v_lin	V26	AA9	sfi_tx_clk_n
1.8v	A15	AB1	sfi_rx_p3
1.8v	A18	AB10	sfi_tx_n2
1.8v	A3	AB11	pmc_busmoden1
1.8v	A30	AB12	pmc_ad32
1.8v	E12	AB13	rs232a_txd
1.8v	E21	AB14	rs232a_cts
1.8v	J16	AB15	pmc_intcn
1.8v	J17	AB16	gnd
1.8v	M16	AB17	pmc_perrn
1.8v	M17	AB18	pmc_intbn
133mhzn	AM22	AB19	rs232a_rxd
2.5v	AA28	AB2	sfi_rx_n3
2.5v	AA5	AB20	pmc_ad38
2.5v	AK1	AB21	pmc_ad16
2.5v	AK32	AB22	gnd
2.5v	C32	AB23	ht_tx_cad_n6
2.5v	M28	AB24	ht_tx_cad_p6
2.5v	R32	AB25	ht_tx_clk_n
2.5v	T21	AB26	ht_tx_clk_p
2.5v	U12	AB27	nc
2.5v	U21	AB28	nc
2.5v	V1	AB29	rio_rd_n7
2.5v	V32	AB3	sfi_rx_p7
3.3v	AA13	AB30	rio_rd_p7
3.3v	AA15	AB31	rio_rd_n4
3.3v	AA16	AB32	rio_rd_p4

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 4 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
3.3v	AA17	AB4	sfi_rx_n7
3.3v	AA18	AB5	sfi_tx_p8
3.3v	AA20	AB6	sfi_tx_n8
3.3v	AF15	AB7	sfi_tx_p9
3.3v	AF16	AB8	sfi_tx_n9
3.3v	AH12	AB9	sfi_tx_p2
3.3v	AH21	AC1	sfi_rx_p10
3.3v	AM15	AC10	1.2v_int
3.3v	AM18	AC11	pmc_ad20
3.3v	AM3	AC12	pmc_ad33
3.3v	AM30	AC13	pmc_ad13
3.3v	C1	AC14	pmc_monarchn
3.3v	M13	AC15	pmc_intdn
3.3v	M15	AC16	pmc_ad36
3.3v	M18	AC17	pmc_ad37
3.3v	M20	AC18	pmc_stopn
3.3v	M5	AC19	pmc_ad24
3.3v	N12	AC2	sfi_rx_n10
3.3v	N21	AC20	pmc_c_ben2
3.3v	R1	AC21	pmc_ad39
3.3v	R12	AC22	config_cs
3.3v	R21	AC23	vccsel
3.3v	T12	AC24	ht_tx_cad_n5
3.3v	V12	AC25	ht_tx_cad_p5
3.3v	V21	AC26	ht_tx_cad_n1
3.3v	Y12	AC27	ht_tx_cad_p1
3.3v	Y21	AC28	gnd
alertn	T31	AC29	nc
asdi	F17	AC3	sfi_rx_p14
clka_fpga	AM16	AC30	nc
clkb_pll5_n	B17	AC31	ht_rx_ctl_n
clkb_pll5_p	A17	AC32	ht_rx_ctl_p
config_cen	C30	AC4	sfi_rx_n14

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 5 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
config_cs	AC22	AC5	gnd
config_csn	AG18	AC6	sfi_tx_p4
config_cson	G19	AC7	sfi_tx_n4
config_d0	H19	AC8	sfi_tx_p5
config_d1	F20	AC9	sfi_tx_n5
config_d2	G23	AD1	sfi_rx_p6
config_d3	H23	AD10	pmc_ad25
config_d4	J23	AD11	pmc_ad27
config_d5	L22	AD12	gnd
config_d6	F24	AD13	rs232b_txd
config_d7	G24	AD14	pmc_gntn
config_dclk	B31	AD15	1.2v_int
config_rsn	AF23	AD16	gnd_pll
config_ry_byn	H24	AD17	gnd_pll
config_wsn	AE23	AD18	pmc_ad40
cpld_user0	R11	AD19	gnd
cpld_user1	AJ15	AD2	sfi_rx_n6
cpld_user2	AH15	AD20	gnd
cpld_user3	AL15	AD21	pmc_ad45
ddrii_a0	K20	AD22	pmc_ad18
ddrii_a1	L19	AD23	nc
ddrii_a2	K19	AD24	ht_tx_cad_n4
ddrii_a3	J19	AD25	ht_tx_cad_p4
ddrii_a4	L18	AD26	ht_tx_cad_n3
ddrii_a5	K18	AD27	ht_tx_cad_p3
ddrii_a6	L15	AD28	gnd
ddrii_a7	J14	AD29	nc
ddrii_a8	K14	AD3	nc
ddrii_a9	L14	AD30	nc
ddrii_a10	K21	AD31	ht_rx_cad_n7
ddrii_a11	H14	AD32	ht_rx_cad_p7
ddrii_a12	J13	AD4	nc

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 6 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
ddrii_a13	L20	AD5	gnd
ddrii_a14	J12	AD6	sfi_tx_p0
ddrii_a15	L13	AD7	sfi_tx_n0
ddrii_ba0	G20	AD8	sfi_tx_p1
ddrii_ba1	J20	AD9	sfi_tx_n1
ddrii_ba2	K13	AE1	sfi_rx_p13
ddrii_casn	H22	AE10	pmc_ad17
ddrii_cb0	E13	AE11	pmc_ad21
ddrii_cb1	D13	AE12	spi_tstat1
ddrii_cb2	D14	AE13	spi_tstat0
ddrii_cb3	F15	AE14	rs232b_cts
ddrii_cb4	G13	AE15	1.2v_lin
ddrii_cb5	F13	AE16	gnd_pll
ddrii_cb6	A14	AE17	gnd_pll
ddrii_cb7	B14	AE18	1.2v_int
ddrii_clk_n0	C15	AE19	pmc_ad44
ddrii_clk_n1	D16	AE2	sfi_rx_n13
ddrii_clk_n2	E15	AE20	dig_1_c
ddrii_clk_p0	B15	AE21	dig_1_b
ddrii_clk_p1	C16	AE22	pmc_ad23
ddrii_clk_p2	D15	AE23	config_wsn
ddrii_clke0	K12	AE24	jtag_tms
ddrii_clke1	L12	AE25	ht_tx_cad_n2
ddrii_clkfb_n	B16	AE26	ht_tx_cad_p2
ddrii_clkfb_n	C18	AE27	ht_pwrok
ddrii_clkfb_p	A16	AE28	ht_resetn
ddrii_clkfb_p	B18	AE29	ht_rx_cad_n5
ddrii_csn0	J21	AE3	sfi_rx_p2
ddrii_csn1	K22	AE30	ht_rx_cad_p5
ddrii_dm0	B5	AE31	ht_rx_cad_n6
ddrii_dm1	B8	AE32	ht_rx_cad_p6
ddrii_dm2	C10	AE4	sfi_rx_n2

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 7 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
ddrii_dm3	C12	AE5	nc
ddrii_dm4	B21	AE6	nc
ddrii_dm5	B23	AE7	1.2v_lin
ddrii_dm6	D25	AE8	1.2v_int
ddrii_dm7	C28	AE9	nc
ddrii_dm8	C13	AF1	sfi_rx_p5
ddrii_dq0	D6	AF10	enet_cyclen
ddrii_dq1	D5	AF11	enet_w_rn
ddrii_dq2	A4	AF12	gnd
ddrii_dq3	A5	AF13	gnd
ddrii_dq4	E5	AF14	nc
ddrii_dq5	C6	AF15	3.3v
ddrii_dq6	B4	AF16	3.3v
ddrii_dq7	A6	AF17	gnd
ddrii_dq8	E6	AF18	1.2v_lin
ddrii_dq9	A7	AF19	rs232b_rxd
ddrii_dq10	A8	AF2	sfi_rx_n5
ddrii_dq11	C9	AF20	gnd
ddrii_dq12	E7	AF21	gnd
ddrii_dq13	B7	AF22	pmc_ad46
ddrii_dq14	C8	AF23	config_rsn
ddrii_dq15	A9	AF24	jtag_tck
ddrii_dq16	F8	AF25	1.2v_int
ddrii_dq17	F10	AF26	1.2v_lin
ddrii_dq18	B10	AF27	nc
ddrii_dq19	D10	AF28	nc
ddrii_dq20	E8	AF29	ht_rx_cad_n3
ddrii_dq21	D8	AF3	sfi_rx_p9
ddrii_dq22	D11	AF30	ht_rx_cad_p3
ddrii_dq23	A10	AF31	ht_rx_cad_n4
ddrii_dq24	G11	AF32	ht_rx_cad_p4
ddrii_dq25	A11	AF4	sfi_rx_n9

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 8 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
ddrii_dq26	E11	AF5	nc
ddrii_dq27	D12	AF6	nc
ddrii_dq28	G10	AF7	gnd_pll
ddrii_dq29	B11	AF8	pll_en
ddrii_dq30	A12	AF9	gnd
ddrii_dq31	G12	AG1	sfi_rx_p12
ddrii_dq32	C20	AG10	enet_rdyrtnn
ddrii_dq33	B20	AG11	enet_aen
ddrii_dq34	A22	AG12	pmc_ad34
ddrii_dq35	C22	AG13	dig_2_b
ddrii_dq36	E19	AG14	dig_2_e
ddrii_dq37	E20	AG15	dig_2_d
ddrii_dq38	C21	AG16	pmc_ad31
ddrii_dq39	A21	AG17	runlu
ddrii_dq40	A23	AG18	config_csn
ddrii_dq41	C23	AG19	pb_dev_clrn
ddrii_dq42	D23	AG2	sfi_rx_n12
ddrii_dq43	F23	AG20	pmc_ad47
ddrii_dq44	F22	AG21	nc
ddrii_dq45	D21	AG22	rio_i2c_sda
ddrii_dq46	C24	AG23	pmc_intan
ddrii_dq47	A24	AG24	pmc_ad49
ddrii_dq48	A26	AG25	nc
ddrii_dq49	C25	AG26	gnd_pll
ddrii_dq50	E26	AG27	gnd_pll
ddrii_dq51	E27	AG28	gnd
ddrii_dq52	E24	AG29	ht_rx_cad_n1
ddrii_dq53	A25	AG3	sfi_rx_p1
ddrii_dq54	D26	AG30	ht_rx_cad_p1
ddrii_dq55	C26	AG31	ht_rx_cad_n2
ddrii_dq56	A29	AG32	ht_rx_cad_p2
ddrii_dq57	C27	AG4	sfi_rx_n1

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 9 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
ddrii_dq58	D28	AG5	gnd
ddrii_dq59	E28	AG6	gnd
ddrii_dq60	A27	AG7	gnd_pll
ddrii_dq61	A28	AG8	pmc_ad3
ddrii_dq62	B29	AG9	pmc_ad5
ddrii_dq63	D27	AH1	sfi_rx_p4
ddrii_dqs_p0	C4	AH10	gnd
ddrii_dqs_p1	D7	AH11	enet_iown
ddrii_dqs_p2	F9	AH12	3.3v
ddrii_dqs_p3	F11	AH13	dig_2_a
ddrii_dqs_p4	D19	AH14	dig_2_f
ddrii_dqs_p5	D22	AH15	cpld_user2
ddrii_dqs_p6	B25	AH16	pmc_trdyn
ddrii_dqs_p7	B27	AH17	nc
ddrii_dqs_p8	F14	AH18	dig_1_g
ddrii_odt0	E25	AH19	spi_rsclk
ddrii_odt1	L21	AH2	sfi_rx_n4
ddrii_rasn	G21	AH20	gnd
ddrii_ref_clk_sma	E16	AH21	3.3v
ddrii_resetn	E22	AH22	pmc_ad51
ddrii_scl	B28	AH23	gnd
ddrii_sda	J22	AH24	pmc_ad52
ddrii_sync_clk	B13	AH25	pmc_ad54
ddrii_sync_clk	C17	AH26	pmc_ad48
ddrii_wen	G22	AH27	gnd
dig_1_a	AK15	AH28	pmc_ad59
dig_1_b	AE21	AH29	nc
dig_1_c	AE20	AH3	sfi_rx_p8
dig_1_d	AK18	AH30	nc
dig_1_dp	AL19	AH31	ht_rx_cad_n0
dig_1_e	T11	AH32	ht_rx_cad_p0
dig_1_f	T6	AH4	sfi_rx_n8

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 10 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
dig_1_g	AH18	AH5	pmc_req64n
dig_2_a	AH13	AH6	pmc_ad0
dig_2_b	AG13	AH7	pmc_ad2
dig_2_c	AJ12	AH8	pmc_ad6
dig_2_d	AG15	AH9	pmc_ad11
dig_2_dp	AJ14	AJ1	sfi_rx_p0
dig_2_e	AG14	AJ10	pmc_ad35
dig_2_f	AH14	AJ11	enet_iorn
dig_2_g	AL14	AJ12	dig_2_c
dip0	K16	AJ13	pmc_framen
dip1	K17	AJ14	dig_2_dp
dip2	L17	AJ15	cpld_user1
dip3	H20	AJ16	temp_sense_clk
dip4	L16	AJ17	pmc_ad28
dip5	K15	AJ18	pmc_clk_loop_out
dip6	J15	AJ19	gnd
dip7	H21	AJ2	sfi_rx_n0
dpa_sma_rx_n0	V3	AJ20	gnd
dpa_sma_rx_n1	W2	AJ21	sfi_i2c_data
dpa_sma_rx_p0	V2	AJ22	pmc_ad29
dpa_sma_rx_p1	W1	AJ23	pmc_ad53
dpa_sma_rxclk_n	U2	AJ24	gnd
dpa_sma_rxclk_p	U1	AJ25	pmc_ad55
dpa_sma_tx_n0	U6	AJ26	rs232a_rts
dpa_sma_tx_n1	U11	AJ27	pmc_ad62
dpa_sma_tx_p0	U5	AJ28	pmc_c_ben7
dpa_sma_tx_p1	U10	AJ29	ht_rx_clk_n
dpa_sma_txclk_n	V10	AJ3	sfi_txp_clk_p
dpa_sma_txclk_p	V9	AJ30	ht_rx_clk_p
enet_adsn	AK9	AJ31	rio_rframe_n
enet_aen	AG11	AJ32	rio_rframe_p
enet_ben0	AL5	AJ4	sfi_txp_clk_n

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 11 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
enet_ben1	AL6	AJ5	pmc_ack64n
enet_cyclen	AF10	AJ6	gnd
enet_intrq0	AJ8	AJ7	spi_tsclk
enet_iochrdy	AL10	AJ8	enet_intrq0
enet_iorn	AJ11	AJ9	gnd
enet_iown	AH11	AK1	2.5v
enet_lclk	AL9	AK10	pmc_c_ben1
enet_ldevn	AM10	AK11	pmc_par
enet_rdyrtnn	AG10	AK12	pmc_serrn
enet_w_rn	AF11	AK13	pmc_ad22
ep2s_config_done	J25	AK14	gnd
ep2s_confign	AL30	AK15	dig_1_a
ep2s_init_done	G25	AK16	temp_sense_data
ep2s_statusn	B30	AK17	pmc_irdyn
flash_cen	T1	AK18	dig_1_d
flash_oen	T2	AK19	gnd
flash_ry_byn	F16	AK2	gnd
flash_wen	D17	AK20	pmc_ad26
fse_a0	J6	AK21	sfi_i2c_clk
fse_a1	J7	AK22	pmc_busmoden4
fse_a2	J8	AK23	pmc_busmoden3
fse_a3	J9	AK24	pmc_busmoden2
fse_a4	K8	AK25	pmc_ad56
fse_a5	K9	AK26	gnd
fse_a6	L9	AK27	pmc_c_ben6
fse_a7	L10	AK28	pmc_c_ben5
fse_a8	L7	AK29	gnd
fse_a9	L8	AK3	nio_pullup
fse_a10	K6	AK30	jtag_trstn
fse_a11	K7	AK31	gnd
fse_a12	L5	AK32	2.5v
fse_a13	L6	AK4	pmc_ad7

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 12 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
fse_a14	M10	AK5	pmc_ad1
fse_a15	M11	AK6	pmc_ad14
fse_a16	M8	AK7	rio_trstn
fse_a17	M9	AK8	pmc_c_ben0
fse_a18	M6	AK9	enet_adsn
fse_a19	M7	AL1	gnd
fse_a20	N6	AL10	enet_iochrdy
fse_a21	N7	AL11	pmc_ad12
fse_a22	N8	AL12	pmc_devseln
fse_a23	N9	AL13	pmc_ad41
fse_a24	P8	AL14	dig_2_g
fse_a25	P9	AL15	cpld_user3
fse_a26	T5	AL16	pmc_ad19
fse_d0	D1	AL17	pmc_c_ben3
fse_d1	D2	AL18	pmc_clk0
fse_d2	E3	AL19	dig_1_dp
fse_d3	E4	AL2	porsel
fse_d4	E1	AL20	pmc_ad30
fse_d5	E2	AL21	pcixn
fse_d6	F3	AL22	pmc_reqn
fse_d7	F4	AL23	rio_irq_outn
fse_d8	F1	AL24	rio_rmcrdy
fse_d9	F2	AL25	rs232b_rts
fse_d10	G3	AL26	spi_rstat0
fse_d11	G4	AL27	pmc_ad60
fse_d12	G1	AL28	pmc_par64
fse_d13	G2	AL29	pmc_c_ben4
fse_d14	J3	AL3	nc
fse_d15	J4	AL30	ep2s_configN
fse_d16	H1	AL31	jtag_stratix_tdi
fse_d17	H2	AL32	gnd
fse_d18	J1	AL4	pmc_ad8

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 13 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
fse_d19	J2	AL5	enet_ben0
fse_d20	K3	AL6	enet_ben1
fse_d21	K4	AL7	gnd
fse_d22	K1	AL8	spi_rstat1
fse_d23	K2	AL9	enet_lclk
fse_d24	L3	AM10	enet_ldevn
fse_d25	L4	AM11	pmc_ad15
fse_d26	N4	AM12	pmc_lockn
fse_d27	N5	AM13	gnd
fse_d28	M3	AM14	pmc_ad42
fse_d29	M4	AM15	3.3v
fse_d30	L1	AM16	clka_fpga
fse_d31	L2	AM17	pmc_resetn
gnd	A13	AM18	3.3v
gnd	A2	AM19	pmc_clk_loop_in
gnd	A20	AM2	gnd
gnd	A31	AM20	gnd
gnd	AA14	AM21	pmc_ad50
gnd	AA19	AM22	133mhzn
gnd	AA21	AM23	pmc_ad43
gnd	AB16	AM24	rio_rstn
gnd	AB22	AM25	gnd
gnd	AC28	AM26	pmc_ad57
gnd	AC5	AM27	pmc_ad58
gnd	AD12	AM28	pmc_ad61
gnd	AD19	AM29	pmc_ad63
gnd	AD20	AM3	3.3v
gnd	AD28	AM30	3.3v
gnd	AD5	AM31	gnd
gnd	AF12	AM4	pmc_m66en
gnd	AF13	AM5	pmc_ad10
gnd	AF17	AM6	pmc_ad4

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 14 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
gnd	AF20	AM7	rio_cpu_rstn
gnd	AF21	AM8	rio_i2c_scl
gnd	AF9	AM9	pmc_ad9
gnd	AG28	B1	gnd
gnd	AG5	B10	ddrii_dq18
gnd	AG6	B11	ddrii_dq29
gnd	AH10	B12	gnd
gnd	AH20	B13	ddrii_sync_clk
gnd	AH23	B14	ddrii_cb7
gnd	AH27	B15	ddrii_clk_p0
gnd	AJ19	B16	ddrii_clkfb_n
gnd	AJ20	B17	clkb_pll5_n
gnd	AJ24	B18	ddrii_clkfb_p
gnd	AJ6	B19	nc
gnd	AJ9	B2	msel0
gnd	AK14	B20	ddrii_dq33
gnd	AK19	B21	ddrii_dm4
gnd	AK2	B22	gnd
gnd	AK26	B23	ddrii_dm5
gnd	AK29	B24	gnd
gnd	AK31	B25	ddrii_dqs_p6
gnd	AL1	B26	gnd
gnd	AL32	B27	ddrii_dqs_p7
gnd	AL7	B28	ddrii_scl
gnd	AM13	B29	ddrii_dq62
gnd	AM2	B3	tempdiode_n
gnd	AM20	B30	ep2s_statusn
gnd	AM25	B31	config_dclk
gnd	AM31	B32	gnd
gnd	B1	B4	ddrii_dq6
gnd	B12	B5	ddrii_dm0
gnd	B22	B6	gnd

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 15 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
gnd	B24	B7	ddrii_dq13
gnd	B26	B8	ddrii_dm1
gnd	B32	B9	gnd
gnd	B6	C1	3.3v
gnd	B9	C10	ddrii_dm2
gnd	C11	C11	gnd
gnd	C29	C12	ddrii_dm3
gnd	C5	C13	ddrii_dm8
gnd	C7	C14	vref_ddrii
gnd	D20	C15	ddrii_clk_n0
gnd	D29	C16	ddrii_clk_p1
gnd	D3	C17	ddrii_sync_clk
gnd	D30	C18	ddrii_clkfb_n
gnd	D4	C19	vref_ddrii
gnd	E10	C2	vref_ddrii
gnd	E14	C20	ddrii_dq32
gnd	E23	C21	ddrii_dq38
gnd	E9	C22	ddrii_dq35
gnd	F12	C23	ddrii_dq41
gnd	F27	C24	ddrii_dq46
gnd	F28	C25	ddrii_dq49
gnd	F5	C26	ddrii_dq55
gnd	F7	C27	ddrii_dq57
gnd	G17	C28	ddrii_dm7
gnd	H13	C29	gnd
gnd	J24	C3	jtag_conn_tdi0_a
gnd	J28	C30	config_cen
gnd	J5	C31	vref_ddrii
gnd	K28	C32	2.5v
gnd	K5	C4	ddrii_dqs_p0
gnd	L11	C5	gnd
gnd	M12	C6	ddrii_dq5

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 16 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
gnd	M14	C7	gnd
gnd	M19	C8	ddrii_dq14
gnd	N1	C9	ddrii_dq11
gnd	N14	D1	fse_d0
gnd	N16	D10	ddrii_dq19
gnd	N18	D11	ddrii_dq22
gnd	N20	D12	ddrii_dq27
gnd	N32	D13	ddrii_cb1
gnd	P12	D14	ddrii_cb2
gnd	P13	D15	ddrii_clk_p2
gnd	P15	D16	ddrii_clk_n1
gnd	P17	D17	flash_wen
gnd	P19	D18	pll11_out1_p
gnd	P21	D19	ddrii_dqs_p4
gnd	P3	D2	fse_d1
gnd	P30	D20	gnd
gnd	R14	D21	ddrii_dq45
gnd	R16	D22	ddrii_dqs_p5
gnd	R18	D23	ddrii_dq42
gnd	R20	D24	vref_ddrii
gnd	T13	D25	ddrii_dm6
gnd	T15	D26	ddrii_dq54
gnd	T17	D27	ddrii_dq63
gnd	T19	D28	ddrii_dq58
gnd	T3	D29	gnd
gnd	T4	D3	gnd
gnd	T7	D30	gnd
gnd	U14	D31	spi_rdat_n0
gnd	U16	D32	spi_rdat_p0
gnd	U18	D4	gnd
gnd	U20	D5	ddrii_dq1
gnd	U29	D6	ddrii_dq0

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 17 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
gnd	U30	D7	ddrii_dqs_p1
gnd	V11	D8	ddrii_dq21
gnd	V13	D9	vref_ddrii
gnd	V15	E1	fse_d4
gnd	V17	E10	gnd
gnd	V19	E11	ddrii_dq26
gnd	V22	E12	1.8v
gnd	V27	E13	ddrii_cb0
gnd	W12	E14	gnd
gnd	W14	E15	ddrii_clk_n2
gnd	W16	E16	ddrii_ref_clk_sma
gnd	W18	E17	spgm2
gnd	W20	E18	pll11_out1_n
gnd	W3	E19	ddrii_dq36
gnd	W30	E2	fse_d5
gnd	Y1	E20	ddrii_dq37
gnd	Y13	E21	1.8v
gnd	Y15	E22	ddrii_resetn
gnd	Y17	E23	gnd
gnd	Y19	E24	ddrii_dq52
gnd	Y32	E25	ddrii_odt0
gnd_pll	AD16	E26	ddrii_dq50
gnd_pll	AD17	E27	ddrii_dq51
gnd_pll	AE16	E28	ddrii_dq59
gnd_pll	AE17	E29	spi_rdat_n1
gnd_pll	AF7	E3	fse_d2
gnd_pll	AG26	E30	spi_rdat_p1
gnd_pll	AG27	E31	spi_rdat_n2
gnd_pll	AG7	E32	spi_rdat_p2
gnd_pll	F26	E4	fse_d3
gnd_pll	G16	E5	ddrii_dq4
gnd_pll	G18	E6	ddrii_dq8

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 18 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
gnd_pll	G26	E7	ddrii_dq12
gnd_pll	G7	E8	ddrii_dq20
gnd_pll	G8	E9	gnd
gnd_pll	H16	F1	fse_d8
gnd_pll	H18	F10	ddrii_dq17
gnd_pll	R8	F11	ddrii_dqs_p3
gnd_pll	T25	F12	gnd
gnd_pll	T26	F13	ddrii_cb5
gnd_pll	T8	F14	ddrii_dqs_p8
gnd_pll	U25	F15	ddrii_cb3
gnd_pll	U26	F16	flash_ry_byn
gnd_pll	U8	F17	asdi
gnd_pll	V8	F18	spgm0
ht_pwrok	AE27	F19	spgm1
ht_resetn	AE28	F2	fse_d9
ht_rx_cad_n0	AH31	F20	config_d1
ht_rx_cad_n1	AG29	F21	nc
ht_rx_cad_n2	AG31	F22	ddrii_dq44
ht_rx_cad_n3	AF29	F23	ddrii_dq43
ht_rx_cad_n4	AF31	F24	config_d6
ht_rx_cad_n5	AE29	F25	nc
ht_rx_cad_n6	AE31	F26	gnd_pll
ht_rx_cad_n7	AD31	F27	gnd
ht_rx_cad_p0	AH32	F28	gnd
ht_rx_cad_p1	AG30	F29	spi_rdat_n3
ht_rx_cad_p2	AG32	F3	fse_d6
ht_rx_cad_p3	AF30	F30	spi_rdat_p3
ht_rx_cad_p4	AF32	F31	spi_rdat_n4
ht_rx_cad_p5	AE30	F32	spi_rdat_p4
ht_rx_cad_p6	AE32	F4	fse_d7
ht_rx_cad_p7	AD32	F5	gnd
ht_rx_clk_n	AJ29	F6	msel1

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 19 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
ht_rx_clk_p	AJ30	F7	gnd
ht_rx_ctl_n	AC31	F8	ddrii_dq16
ht_rx_ctl_p	AC32	F9	ddrii_dqs_p2
ht_tx_cad_n0	AA24	G1	fse_d12
ht_tx_cad_n1	AC26	G10	ddrii_dq28
ht_tx_cad_n2	AE25	G11	ddrii_dq24
ht_tx_cad_n3	AD26	G12	ddrii_dq31
ht_tx_cad_n4	AD24	G13	ddrii_cb4
ht_tx_cad_n5	AC24	G14	nc
ht_tx_cad_n6	AB23	G15	1.2v_lin
ht_tx_cad_n7	AA22	G16	gnd_pll
ht_tx_cad_p0	AA25	G17	gnd
ht_tx_cad_p1	AC27	G18	gnd_pll
ht_tx_cad_p2	AE26	G19	config_cson
ht_tx_cad_p3	AD27	G2	fse_d13
ht_tx_cad_p4	AD25	G20	ddrii_ba0
ht_tx_cad_p5	AC25	G21	ddrii_rasn
ht_tx_cad_p6	AB24	G22	ddrii_wen
ht_tx_cad_p7	AA23	G23	config_d2
ht_tx_clk_n	AB25	G24	config_d7
ht_tx_clk_p	AB26	G25	ep2s_init_done
ht_tx_ctl_n	Y22	G26	gnd_pll
ht_tx_ctl_p	Y23	G27	nc
jtag_conn_tdi0_a	C3	G28	nc
jtag_stratix_tdi	AL31	G29	spi_rdat_n5
jtag_tck	AF24	G3	fse_d10
jtag_tms	AE24	G30	spi_rdat_p5
jtag_trstn	AK30	G31	spi_rdat_n6
msel0	B2	G32	spi_rdat_p6
msel1	F6	G4	fse_d11
msel2	J10	G5	nc
msel3	H10	G6	nc

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 20 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
nc	A19	G7	gnd_pll
nc	AB27	G8	gnd_pll
nc	AB28	G9	tempdiode_p
nc	AC29	H1	fse_d16
nc	AC30	H10	msel3
nc	AD23	H11	pb0
nc	AD29	H12	pb3
nc	AD3	H13	gnd
nc	AD30	H14	ddrii_a11
nc	AD4	H15	1.2v_int
nc	AE5	H16	gnd_pll
nc	AE6	H17	1.2v_lin
nc	AE9	H18	gnd_pll
nc	AF14	H19	config_d0
nc	AF27	H2	fse_d17
nc	AF28	H20	dip3
nc	AF5	H21	dip7
nc	AF6	H22	ddrii_casn
nc	AG21	H23	config_d3
nc	AG25	H24	config_ry_byn
nc	AH17	H25	1.2v_int
nc	AH29	H26	1.2v_lin
nc	AH30	H27	spi_tdat_n0
nc	AL3	H28	spi_tdat_p0
nc	B19	H29	spi_rdat_n7
nc	F21	H3	nc
nc	F25	H30	spi_rdat_p7
nc	G14	H31	spi_rdat_n8
nc	G27	H32	spi_rdat_p8
nc	G28	H4	nc
nc	G5	H5	nc
nc	G6	H6	nc

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 21 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
nc	H3	H7	1.2v_int
nc	H4	H8	1.2v_lin
nc	H5	H9	nc
nc	H6	J1	fse_d18
nc	H9	J10	msel2
nc	J29	J11	pb1
nc	J30	J12	ddrii_a14
nc	K24	J13	ddrii_a12
nc	K25	J14	ddrii_a7
nc	L27	J15	dip6
nc	L28	J16	1.8v
nc	M31	J17	1.8v
nc	M32	J18	1.2v_int
nc	N10	J19	ddrii_a3
nc	N11	J2	fse_d19
nc	P22	J20	ddrii_ba1
nc	P23	J21	ddrii_csn0
nc	P31	J22	ddrii_sda
nc	P32	J23	config_d4
nc	R28	J24	gnd
nc	R29	J25	ep2s_config_done
nc	R30	J26	spi_tdat_n1
nc	R31	J27	spi_tdat_p1
nc	T27	J28	gnd
nc	T28	J29	nc
nc	W10	J3	fse_d14
nc	W11	J30	nc
nc	W22	J31	spi_rdat_n9
nc	W23	J32	spi_rdat_p9
nio_pullup	AK3	J4	fse_d15
overtempn	T32	J5	gnd
pb0	H11	J6	fse_a0

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 22 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
pb1	J11	J7	fse_a1
pb2	K11	J8	fse_a2
pb3	H12	J9	fse_a3
pb_dev_clrn	AG19	K1	fse_d22
pcixn	AL21	K10	1.2v_int
pll11_out1_n	E18	K11	pb2
pll11_out1_p	D18	K12	ddrii_clke0
pll_en	AF8	K13	ddrii_ba2
pmc_ack64n	AJ5	K14	ddrii_a8
pmc_ad0	AH6	K15	dip5
pmc_ad1	AK5	K16	dip0
pmc_ad2	AH7	K17	dip1
pmc_ad3	AG8	K18	ddrii_a5
pmc_ad4	AM6	K19	ddrii_a2
pmc_ad5	AG9	K2	fse_d23
pmc_ad6	AH8	K20	ddrii_a0
pmc_ad7	AK4	K21	ddrii_a10
pmc_ad8	AL4	K22	ddrii_csn1
pmc_ad9	AM9	K23	1.2v_int
pmc_ad10	AM5	K24	nc
pmc_ad11	AH9	K25	nc
pmc_ad12	AL11	K26	spi_tdat_n3
pmc_ad13	AC13	K27	spi_tdat_p3
pmc_ad14	AK6	K28	gnd
pmc_ad15	AM11	K29	spi_rdat_n10
pmc_ad16	AB21	K3	fse_d20
pmc_ad17	AE10	K30	spi_rdat_p10
pmc_ad18	AD22	K31	spi_rdat_n11
pmc_ad19	AL16	K32	spi_rdat_p11
pmc_ad20	AC11	K4	fse_d21
pmc_ad21	AE11	K5	gnd
pmc_ad22	AK13	K6	fse_a10

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 23 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
pmc_ad23	AE22	K7	fse_a11
pmc_ad24	AC19	K8	fse_a4
pmc_ad25	AD10	K9	fse_a5
pmc_ad26	AK20	L1	fse_d30
pmc_ad27	AD11	L10	fse_a7
pmc_ad28	AJ17	L11	gnd
pmc_ad29	AJ22	L12	ddrii_clke1
pmc_ad30	AL20	L13	ddrii_a15
pmc_ad31	AG16	L14	ddrii_a9
pmc_ad32	AB12	L15	ddrii_a6
pmc_ad33	AC12	L16	dip4
pmc_ad34	AG12	L17	dip2
pmc_ad35	AJ10	L18	ddrii_a4
pmc_ad36	AC16	L19	ddrii_a1
pmc_ad37	AC17	L2	fse_d31
pmc_ad38	AB20	L20	ddrii_a13
pmc_ad39	AC21	L21	ddrii_odt1
pmc_ad40	AD18	L22	config_d5
pmc_ad41	AL13	L23	spi_tdat_n2
pmc_ad42	AM14	L24	spi_tdat_p2
pmc_ad43	AM23	L25	spi_tdat_n5
pmc_ad44	AE19	L26	spi_tdat_p5
pmc_ad45	AD21	L27	nc
pmc_ad46	AF22	L28	nc
pmc_ad47	AG20	L29	spi_rdat_n12
pmc_ad48	AH26	L3	fse_d24
pmc_ad49	AG24	L30	spi_rdat_p12
pmc_ad50	AM21	L31	spi_rdat_n13
pmc_ad51	AH22	L32	spi_rdat_p13
pmc_ad52	AH24	L4	fse_d25
pmc_ad53	AJ23	L5	fse_a12
pmc_ad54	AH25	L6	fse_a13

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 24 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
pmc_ad55	AJ25	L7	fse_a8
pmc_ad56	AK25	L8	fse_a9
pmc_ad57	AM26	L9	fse_a6
pmc_ad58	AM27	M1	sram_ben2
pmc_ad59	AH28	M10	fse_a14
pmc_ad60	AL27	M11	fse_a15
pmc_ad61	AM28	M12	gnd
pmc_ad62	AJ27	M13	3.3v
pmc_ad63	AM29	M14	gnd
pmc_busmoden1	AB11	M15	3.3v
pmc_busmoden2	AK24	M16	1.8v
pmc_busmoden3	AK23	M17	1.8v
pmc_busmoden4	AK22	M18	3.3v
pmc_c_ben0	AK8	M19	gnd
pmc_c_ben1	AK10	M2	sram_ben3
pmc_c_ben2	AC20	M20	3.3v
pmc_c_ben3	AL17	M21	1.2v_int
pmc_c_ben4	AL29	M22	spi_tdat_n4
pmc_c_ben5	AK28	M23	spi_tdat_p4
pmc_c_ben6	AK27	M24	spi_tdat_n6
pmc_c_ben7	AJ28	M25	spi_tdat_p6
pmc_clk0	AL18	M26	spi_tdclk_n
pmc_clk_loop_in	AM19	M27	spi_tdclk_p
pmc_clk_loop_out	AJ18	M28	2.5v
pmc_devseln	AL12	M29	spi_rdat_n14
pmc_framen	AJ13	M3	fse_d28
pmc_gntn	AD14	M30	spi_rdat_p14
pmc_intan	AG23	M31	nc
pmc_intbn	AB18	M32	nc
pmc_intcn	AB15	M4	fse_d29
pmc_intdn	AC15	M5	3.3v
pmc_irdyn	AK17	M6	fse_a18

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 25 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
pmc_lockn	AM12	M7	fse_a19
pmc_m66en	AM4	M8	fse_a16
pmc_monarchn	AC14	M9	fse_a17
pmc_par	AK11	N1	gnd
pmc_par64	AL28	N10	nc
pmc_perrn	AB17	N11	nc
pmc_req64n	AH5	N12	3.3v
pmc_reqn	AL22	N13	1.2v_int
pmc_resetn	AM17	N14	gnd
pmc_serrn	AK12	N15	1.2v_int
pmc_stopn	AC18	N16	gnd
pmc_trdyn	AH16	N17	1.2v_int
porsel	AL2	N18	gnd
rio_cpu_rstn	AM7	N19	1.2v_int
rio_i2c_scl	AM8	N2	sram_ben0
rio_i2c_sda	AG22	N20	gnd
rio_irq_outn	AL23	N21	3.3v
rio_rclk_n	U31	N22	spi_tdat_n7
rio_rclk_p	U32	N23	spi_tdat_p7
rio_rd_n0	V30	N24	spi_tdat_n9
rio_rd_n1	W31	N25	spi_tdat_p9
rio_rd_n2	AA31	N26	spi_tdat_n8
rio_rd_n3	Y30	N27	spi_tdat_p8
rio_rd_n4	AB31	N28	spi_rdat_n15
rio_rd_n5	AA29	N29	spi_rdat_p15
rio_rd_n6	Y28	N3	sram_ben1
rio_rd_n7	AB29	N30	spi_rctl_n
rio_rd_p0	V31	N31	spi_rctl_p
rio_rd_p1	W32	N32	gnd
rio_rd_p2	AA32	N4	fse_d26
rio_rd_p3	Y31	N5	fse_d27
rio_rd_p4	AB32	N6	fse_a20

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 26 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
rio_rd_p5	AA30	N7	fse_a21
rio_rd_p6	Y29	N8	fse_a22
rio_rd_p7	AB30	N9	fse_a23
rio_rframe_n	AJ31	P1	test4
rio_rframe_p	AJ32	P10	user_led4
rio_rmcrdy	AL24	P11	user_led5
rio_rstn	AM24	P12	gnd
rio_tclk_n	W26	P13	gnd
rio_tclk_p	W27	P14	1.2v_int
rio_td_n0	U22	P15	gnd
rio_td_n1	V23	P16	1.2v_int
rio_td_n2	W24	P17	gnd
rio_td_n3	Y24	P18	1.2v_int
rio_td_n4	Y26	P19	gnd
rio_td_n5	U27	P2	test5
rio_td_n6	W28	P20	1.2v_int
rio_td_n7	V28	P21	gnd
rio_td_p0	U23	P22	nc
rio_td_p1	V24	P23	nc
rio_td_p2	W25	P24	spi_tdat_n13
rio_td_p3	Y25	P25	spi_tdat_p13
rio_td_p4	Y27	P26	spi_tdat_n10
rio_td_p5	U28	P27	spi_tdat_p10
rio_td_p6	W29	P28	spi_tdat_n11
rio_td_p7	V29	P29	spi_tdat_p11
rio_tframe_n	AA26	P3	gnd
rio_tframe_p	AA27	P30	gnd
rio_trstn	AK7	P31	nc
rs232a_cts	AB14	P32	nc
rs232a_rts	AJ26	P4	user_led2
rs232a_rxd	AB19	P5	user_led3
rs232a_txd	AB13	P6	user_led0

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 27 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
rs232b_cts	AE14	P7	user_led1
rs232b_rts	AL25	P8	fse_a24
rs232b_rxd	AF19	P9	fse_a25
rs232b_txd	AD13	R1	3.3v
runlu	AG17	R10	sram_csn
sfi_ffu_rx_n1	Y3	R11	cpld_user0
sfi_ffu_rx_n2	AA2	R12	3.3v
sfi_ffu_rx_p1	Y2	R13	1.2v_int
sfi_ffu_rx_p2	AA1	R14	gnd
sfi_ffu_tx_n1	V5	R15	1.2v_int
sfi_ffu_tx_p1	V4	R16	gnd
sfi_i2c_clk	AK21	R17	1.2v_int
sfi_i2c_data	AJ21	R18	gnd
sfi_rx_clk_n	U4	R19	1.2v_int
sfi_rx_clk_p	U3	R2	test3
sfi_rx_n0	AJ2	R20	gnd
sfi_rx_n1	AG4	R21	3.3v
sfi_rx_n2	AE4	R22	spi_tdat_n15
sfi_rx_n3	AB2	R23	spi_tdat_p15
sfi_rx_n4	AH2	R24	spi_tctl_n
sfi_rx_n5	AF2	R25	spi_tctl_p
sfi_rx_n6	AD2	R26	spi_tdat_n12
sfi_rx_n7	AB4	R27	spi_tdat_p12
sfi_rx_n8	AH4	R28	nc
sfi_rx_n9	AF4	R29	nc
sfi_rx_n10	AC2	R3	test2
sfi_rx_n11	AA4	R30	nc
sfi_rx_n12	AG2	R31	nc
sfi_rx_n13	AE2	R32	2.5v
sfi_rx_n14	AC4	R4	sram_wen
sfi_rx_n15	Y5	R5	sram_oen
sfi_rx_p0	AJ1	R6	user_led6

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 28 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
sfi_rx_p1	AG3	R7	user_led7
sfi_rx_p2	AE3	R8	gnd_pll
sfi_rx_p3	AB1	R9	1.2v_lin
sfi_rx_p4	AH1	T1	flash_cen
sfi_rx_p5	AF1	T10	test1
sfi_rx_p6	AD1	T11	dig_1_e
sfi_rx_p7	AB3	T12	3.3v
sfi_rx_p8	AH3	T13	gnd
sfi_rx_p9	AF3	T14	1.2v_int
sfi_rx_p10	AC1	T15	gnd
sfi_rx_p11	AA3	T16	1.2v_int
sfi_rx_p12	AG1	T17	gnd
sfi_rx_p13	AE1	T18	1.2v_int
sfi_rx_p14	AC3	T19	gnd
sfi_rx_p15	Y4	T2	flash_oen
sfi_tx_clk_n	AA9	T20	1.2v_int
sfi_tx_clk_p	AA8	T21	2.5v
sfi_tx_n0	AD7	T22	spi_tdat_n14
sfi_tx_n1	AD9	T23	spi_tdat_p14
sfi_tx_n2	AB10	T24	1.2v_lin
sfi_tx_n3	Y7	T25	gnd_pll
sfi_tx_n4	AC7	T26	gnd_pll
sfi_tx_n5	AC9	T27	nc
sfi_tx_n6	AA11	T28	nc
sfi_tx_n7	W5	T29	spi_rdclk_n
sfi_tx_n8	AB6	T3	gnd
sfi_tx_n9	AB8	T30	spi_rdclk_p
sfi_tx_n10	Y11	T31	alertn
sfi_tx_n11	W7	T32	overtempn
sfi_tx_n12	AA7	T4	gnd
sfi_tx_n13	Y9	T5	fse_a26
sfi_tx_n14	W9	T6	dig_1_f

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 29 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
sfi_tx_n15	V7	T7	gnd
sfi_tx_p0	AD6	T8	gnd_pll
sfi_tx_p1	AD8	T9	1.2v_int
sfi_tx_p2	AB9	U1	dpa_sma_rxclk_p
sfi_tx_p3	Y6	U10	dpa_sma_tx_p1
sfi_tx_p4	AC6	U11	dpa_sma_tx_n1
sfi_tx_p5	AC8	U12	2.5v
sfi_tx_p6	AA10	U13	1.2v_int
sfi_tx_p7	W4	U14	gnd
sfi_tx_p8	AB5	U15	1.2v_int
sfi_tx_p9	AB7	U16	gnd
sfi_tx_p10	Y10	U17	1.2v_int
sfi_tx_p11	W6	U18	gnd
sfi_tx_p12	AA6	U19	1.2v_int
sfi_tx_p13	Y8	U2	dpa_sma_rxclk_n
sfi_tx_p14	W8	U20	gnd
sfi_tx_p15	V6	U21	2.5v
sfi_txp_clk_n	AJ4	U22	rio_td_n0
sfi_txp_clk_p	AJ3	U23	rio_td_p0
spgm0	F18	U24	1.2v_int
spgm1	F19	U25	gnd_pll
spgm2	E17	U26	gnd_pll
spi_rctl_n	N30	U27	rio_td_n5
spi_rctl_p	N31	U28	rio_td_p5
spi_rdat_n0	D31	U29	gnd
spi_rdat_n1	E29	U3	sfi_rx_clk_p
spi_rdat_n2	E31	U30	gnd
spi_rdat_n3	F29	U31	rio_rclk_n
spi_rdat_n4	F31	U32	rio_rclk_p
spi_rdat_n5	G29	U4	sfi_rx_clk_n
spi_rdat_n6	G31	U5	dpa_sma_tx_p0
spi_rdat_n7	H29	U6	dpa_sma_tx_n0

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 30 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
spi_rdat_n8	H31	U7	1.2v_int
spi_rdat_n9	J31	U8	gnd_pll
spi_rdat_n10	K29	U9	1.2v_lin
spi_rdat_n11	K31	V1	2.5v
spi_rdat_n12	L29	V10	dpa_sma_txclk_n
spi_rdat_n13	L31	V11	gnd
spi_rdat_n14	M29	V12	3.3v
spi_rdat_n15	N28	V13	gnd
spi_rdat_p0	D32	V14	1.2v_int
spi_rdat_p1	E30	V15	gnd
spi_rdat_p2	E32	V16	1.2v_int
spi_rdat_p3	F30	V17	gnd
spi_rdat_p4	F32	V18	1.2v_int
spi_rdat_p5	G30	V19	gnd
spi_rdat_p6	G32	V2	dpa_sma_rx_p0
spi_rdat_p7	H30	V20	1.2v_int
spi_rdat_p8	H32	V21	3.3v
spi_rdat_p9	J32	V22	gnd
spi_rdat_p10	K30	V23	rio_td_n1
spi_rdat_p11	K32	V24	rio_td_p1
spi_rdat_p12	L30	V25	1.2v_int
spi_rdat_p13	L32	V26	1.2v_lin
spi_rdat_p14	M30	V27	gnd
spi_rdat_p15	N29	V28	rio_td_n7
spi_rdclk_n	T29	V29	rio_td_p7
spi_rdclk_p	T30	V3	dpa_sma_rx_n0
spi_rsclk	AH19	V30	rio_rd_n0
spi_rstat0	AL26	V31	rio_rd_p0
spi_rstat1	AL8	V32	2.5v
spi_tctl_n	R24	V4	sfi_ffu_tx_p1
spi_tctl_p	R25	V5	sfi_ffu_tx_n1
spi_tdat_n0	H27	V6	sfi_tx_p15

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 31 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
spi_tdat_n1	J26	V7	sfi_tx_n15
spi_tdat_n2	L23	V8	gnd_pll
spi_tdat_n3	K26	V9	dpa_sma_txclk_p
spi_tdat_n4	M22	W1	dpa_sma_rx_p1
spi_tdat_n5	L25	W10	nc
spi_tdat_n6	M24	W11	nc
spi_tdat_n7	N22	W12	gnd
spi_tdat_n8	N26	W13	1.2v_int
spi_tdat_n9	N24	W14	gnd
spi_tdat_n10	P26	W15	1.2v_int
spi_tdat_n11	P28	W16	gnd
spi_tdat_n12	R26	W17	1.2v_int
spi_tdat_n13	P24	W18	gnd
spi_tdat_n14	T22	W19	1.2v_int
spi_tdat_n15	R22	W2	dpa_sma_rx_n1
spi_tdat_p0	H28	W20	gnd
spi_tdat_p1	J27	W21	1.2v_int
spi_tdat_p2	L24	W22	nc
spi_tdat_p3	K27	W23	nc
spi_tdat_p4	M23	W24	rio_td_n2
spi_tdat_p5	L26	W25	rio_td_p2
spi_tdat_p6	M25	W26	rio_tclk_n
spi_tdat_p7	N23	W27	rio_tclk_p
spi_tdat_p8	N27	W28	rio_td_n6
spi_tdat_p9	N25	W29	rio_td_p6
spi_tdat_p10	P27	W3	gnd
spi_tdat_p11	P29	W30	gnd
spi_tdat_p12	R27	W31	rio_rd_n1
spi_tdat_p13	P25	W32	rio_rd_p1
spi_tdat_p14	T23	W4	sfi_tx_p7
spi_tdat_p15	R23	W5	sfi_tx_n7
spi_tdclk_n	M26	W6	sfi_tx_p11

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 32 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	**Pin Number**	**Pin Number**	**Signal Name**
spi_tdclk_p	M27	W7	sfi_tx_n11
spi_tsclk	AJ7	W8	sfi_tx_p14
spi_tstat0	AE13	W9	sfi_tx_n14
spi_tstat1	AE12	Y1	gnd
sram_ben0	N2	Y10	sfi_tx_p10
sram_ben1	N3	Y11	sfi_tx_n10
sram_ben2	M1	Y12	3.3v
sram_ben3	M2	Y13	gnd
sram_csn	R10	Y14	1.2v_int
sram_oen	R5	Y15	gnd
sram_wen	R4	Y16	1.2v_int
temp_sense_clk	AJ16	Y17	gnd
temp_sense_data	AK16	Y18	1.2v_int
tempdiode_n	B3	Y19	gnd
tempdiode_p	G9	Y2	sfi_ffu_rx_p1
test1	T10	Y20	1.2v_int
test2	R3	Y21	3.3v
test3	R2	Y22	ht_tx_ctl_n
test4	P1	Y23	ht_tx_ctl_p
test5	P2	Y24	rio_td_n3
user_led0	P6	Y25	rio_td_p3
user_led1	P7	Y26	rio_td_n4
user_led2	P4	Y27	rio_td_p4
user_led3	P5	Y28	rio_rd_n6
user_led4	P10	Y29	rio_rd_p6
user_led5	P11	Y3	sfi_ffu_rx_n1
user_led6	R6	Y30	rio_rd_n3
user_led7	R7	Y31	rio_rd_p3
vccsel	AC23	Y32	gnd
vref_ddrii	C14	Y4	sfi_rx_p15
vref_ddrii	C19	Y5	sfi_rx_n15
vref_ddrii	C2	Y6	sfi_tx_p3

Table 28. Stratix II High-Speed Development Board's Stratix II Device Pinout (Part 33 of 33)

Alphabetical by Signal Name		Alphabetical by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
vref_ddrii	C31	Y7	sfi_tx_n3
vref_ddrii	D24	Y8	sfi_tx_p13
vref_ddrii	D9	Y9	sfi_tx_n13

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