8-Channel, 12-Bit, Configurable ADC/DAC with On-Chip Reference, I²C Interface

Data Sheet

AD5593R

FEATURES

- 8-channel, configurable ADC/DAC/GPIO
  - Configurable as any combination of
    - 8 12-bit DAC channels
    - 8 12-bit ADC channels
    - 8 general-purpose I/O pins
- Integrated temperature sensor
- 16-lead TSSOP and LFCSP and 16-ball WLCSP packages
- I²C interface

APPLICATIONS

- Control and monitoring
- General-purpose analog and digital I/O

GENERAL DESCRIPTION

The AD5593R has eight input/output (I/O) pins, which can be independently configured as digital-to-analog converter (DAC) outputs, analog-to-digital converter (ADC) inputs, digital outputs, or digital inputs. When an I/O pin is configured as an analog output, it is driven by a 12-bit DAC. The output range of the DAC is 0 V to V_{REF} or 0 V to 2 × V_{REF}. When an I/O pin is configured as an analog input, it is connected to a 12-bit ADC via an analog multiplexer. The input range of the ADC is 0 V to V_{REF} or 0 V to 2 × V_{REF}. The I/O pins can also be configured to be general-purpose, digital input or output (GPIO) pins. The state of the GPIO pins can be set or read back by accessing the GPIO write data register and GPIO read configuration registers, respectively, via an I²C write or read operation.

The AD5593R has an integrated 2.5 V, 20 ppm/°C reference that is turned off by default and an integrated temperature indicator that gives an indication of the die temperature. The temperature value is read back as part of an ADC read sequence.

The AD5593R is available in 16-lead TSSOP and LFCSP, as well as a 16-ball WLCSP, and operates over a temperature range of −40°C to +105°C.

Table 1. Related Products

Product	Description
AD5592R	AD5593R equivalent with SPI interface
AD5592R-1	AD5593R equivalent with SPI interface and V_{LOGIC} pin

FUNCTIONAL BLOCK DIAGRAM

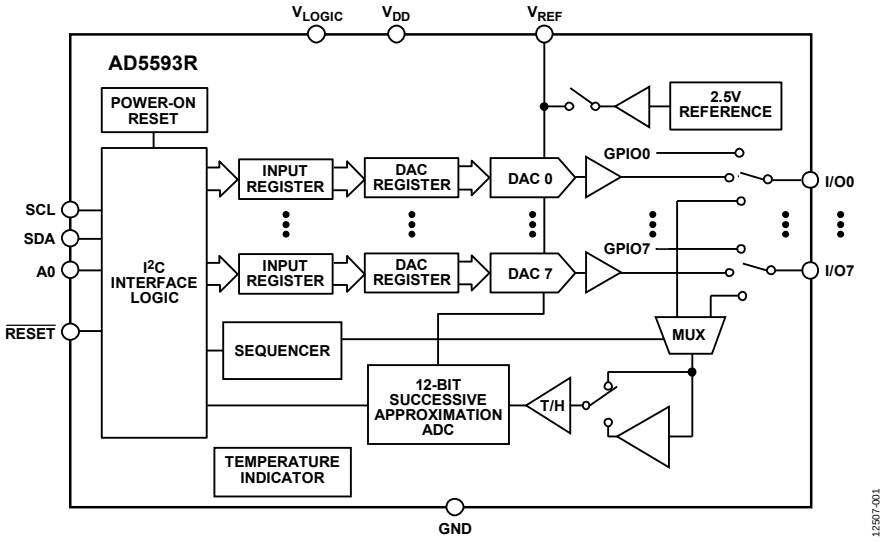

Figure 1.

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- AD5593R Evaluation Board

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Data Sheet

- AD5593R: 8-Channel, 12-Bit, Configurable ADC/DAC with On-Chip Reference, I2C Interface Data Sheet

User Guides

- UG-756: Evaluating the AD5593R: 8-Channel, 12-Bit, Configurable ADC/DAC with On-Chip Reference

Tools and Simulations

- AD5593R IBIS Model

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- CN0229

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SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V (internal), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC PERFORMANCE					f_{IN} = 10 kHz sine wave
Resolution		12		Bits	
Input Range[1]	0		V_{REF}	V	ADC range select bit = 0
	0		2 × V_{REF}	V	ADC range select bit = 1
Integral Nonlinearity (INL)	−2		+2	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	
Offset Error			±5	mV	
Gain Error			0.3	% FSR	
Track Time (t_{TRACK})[2]	500			ns	
Conversion Time (t_{CONV})[2]			2	µs	
Signal to Noise Ratio (SNR)[3]		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 5.5 V, input range = 0 V to V_{REF}
		61		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Signal-to-Noise + Distortion (SINAD) Ratio		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		60		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Total Harmonic Distortion (THD)		−91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		−89		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		−72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Spurious Free Dynamic Range (SFDR)		91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		91		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Aperture Delay[2]		15		ns	V_{DD} = 3 V
		12		ns	V_{DD} = 5 V
Aperture Jitter[2]		50		ps	
Channel-to-Channel Isolation		−95		dB	f_{IN} = 5 kHz
Full Power Bandwidth		8.2		MHz	At 3 dB
		1.6		MHz	At 0.1 dB
DAC PERFORMANCE[4]					
Resolution		12		Bits	
Output Range	0		V_{REF}	V	DAC range select bit = 0
	0		2 × V_{REF}	V	DAC range select bit = 1
INL	−1		+1	LSB	
DNL	−1		+1	LSB	
Offset Error	−3		+3	mV	
Offset Error Drift[2]		8		µV/°C	
Gain Error			±0.2	% FSR	Output range = 0 V to V_{REF}
			±0.1	% FSR	Output range = 0 V to 2 × V_{REF}
Zero Code Error		0.65	2	mV	
Total Unadjusted Error (TUE)		±0.03	±0.25	% FSR	Output range = 0 V to V_{REF}
		±0.015	±0.1	% FSR	Output range = 0 V to 2 × V_{REF}
Capacitive Load Stability			2	nF	R_{LOAD} = ∞
			10	nF	R_{LOAD} = 1 kΩ
Resistive Load	1			kΩ	
Short-Circuit Current		25		mA	
DC Crosstalk[2]	−4		+4	µV	Single channel, full-scale output change
DC Output Impedance		0.2		Ω	
DC Power Supply Rejection Ratio (PSRR)[2]		0.15		mV/V	DAC code = midscale, V_{DD} = 3 V ± 10% or 5 V ± 10%
Load Impedance at Rails[5]		25		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Load Regulation		200		µV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
		200		µV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
Power-Up Time		7		µs	Exiting power-down mode, V_{DD} = 5 V
AC SPECIFICATIONS					
Slew Rate		1.25		V/µs	
Settling Time		6		µs	
DAC Glitch Impulse		2		nV-sec	
DAC to DAC Crosstalk		1		nV-sec	
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		1		nV-sec	
Digital Feedthrough		0.1		nV-sec	
Multiplying Bandwidth		240		kHz	DAC code = full scale, output range = 0 V to 2 × V_{REF}
Output Voltage Noise Spectral Density		200		nV/√Hz	DAC code = midscale, output range = 0 V to 2 × V_{REF}, measured at 10 kHz
SNR		81		dB	
SFDR		77		dB	
SINAD		74		dB	
Total Harmonic Distortion		−76		dB	
REFERENCE INPUT					
V_{REF} Input Voltage	1		V_{DD}	V	
DC Leakage Current	−1		+1	µA	No I/Ox pins configured as DACs
V_{REF} Input Impedance		12		kΩ	DAC output range = 0 V to 2 × V_{REF}
		24		kΩ	DAC output range = 0 V to V_{REF}
REFERENCE OUTPUT					
V_{REF} Output Voltage	2.495	2.5	2.505	V	
V_{REF} Temperature Coefficient		20		ppm/°C	
Capacitive Load Stability		5		µF	R_{LOAD} = 2 kΩ
Output Impedance		0.15		Ω	V_{DD} = 2.7 V
		0.7		Ω	V_{DD} = 5 V
Output Voltage Noise		10		µV p-p	0.1 Hz to 10 Hz
Density		240		nV/√Hz	At ambient, f = 1 kHz, C_L = 10 nF
Line Regulation		20		µV/V	At ambient, sweeping V_{DD} from 2.7 V to 5.5 V
		10		µV/V	At ambient, sweeping V_{DD} from 2.7 V to 3.3 V
Load Regulation					
Sourcing		210		µV/mA	At ambient, −5 mA ≤ load current ≤ +5 mA
Sinking		120		µV/mA	At ambient, −5 mA ≤ load current ≤ +5 mA
Output Current Load Capability		±5		mA	V_{DD} ≥ 3 V
GPIO OUTPUT					
I_{SOURCE} and I_{SINK}		1.6		mA	
Output Voltage					
High, V_{OH}	V_{DD} − 0.2			V	I_{SOURCE} = 1 mA
Low, V_{OL}			0.4	V	I_{SOURCE} = 1 mA
GPIO INPUT					
Input Voltage					
High, V_{IH}	V_{DD} × 0.7			V	
Low, V_{IL}			V_{DD} × 0.3	V	
Input Capacitance		20		pF	
Hysteresis		0.2		V	
Input Current		±1		µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input Voltage					
High, V_{INH}	$0.7 \times V_{LOGIC}$			V	
Low, V_{INL}			$0.3 \times V_{LOGIC}$	V	
Input Current, I_{IN}	−1	+0.01	+1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUT (SDA)					
Output High Voltage, V_{OH}	$V_{LOGIC} - 0.2$			V	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.5 V
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Floating-State Output Capacitance		10		pF	
TEMPERATURE SENSOR[2]					
Resolution		12		Bits	
Operating Range	−40		+105	°C	
Accuracy		±3		°C	
Track Time			5	µs	ADC buffer enabled
			20	µs	ADC buffer disabled
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD}			2.7		Digital inputs = 0 V or V_{DD}
Power-Down Mode			3.5	µA	
Normal Mode					
V_{DD} = 5 V		1.6		mA	I/O0 to I/O7 are DACs, internal reference, gain = 2
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 2
		2.4		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 2
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 2
		1		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 2
		0.75		mA	I/O0 to I/O7 are ADCs, external reference, gain = 2
		0.5		mA	I/O0 to I/O7 are general-purpose outputs
		0.5		mA	I/O0 to I/O7 are general-purpose inputs
V_{DD} = 3 V		1.1		mA	I/O0 to I/O7 are DACs, internal reference, gain = 1
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 1
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 1
		0.78		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 1
		0.75		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 1
		0.5		mA	I/O0 to I/O7 are ADCs, external reference, gain = 1
		0.45		mA	I/O0 to I/O7 are general-purpose outputs
		0.45		mA	I/O0 to I/O7 are general-purpose inputs
V_{LOGIC}	1.8		V_{DD}	V	
I_{LOGIC}			3.5	µA	

[1] When using the internal ADC buffer, there is a dead band of 0 V to 5 mV.
[2] Guaranteed by design and characterization; not production tested.
[3] All specifications expressed in decibels are referred to full-scale input, FSR, and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[4] DC specifications tested with the outputs unloaded, unless otherwise noted. Linearity calculated using a reduced code range of 8 to 4085. An upper dead band of 10 mV exists when $V_{REF} = V_{DD}$.
[5] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 26 and Figure 27).

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; V_{DD} = 2.7 V to 5.5 V, 1.8 V ≤ V_{LOGIC} ≤ V_{DD}; 2.5 V ≤ V_{REF} ≤ V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
t_1	2.5			µs	SCL cycle time
t_2	0.6			µs	t_{HIGH}, SCL high time
t_3	1.3			µs	t_{LOW}, SCL low time
t_4	0.6			µs	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100			ns	$t_{SU,DAT}$, data setup time
t_6[2]			0.9	µs	$t_{HD,DAT}$, data hold time
t_7	0.6			µs	$t_{SU,STA}$, setup time for repeated start
t_8	0.6			µs	$t_{SU,STO}$, stop condition setup time
t_9	1.3			µs	t_{BUF}, bus free time between a stop and a start condition
t_{10}			300	ns	t_R, rise time of SCL and SDA when receiving
	0			ns	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}			250	ns	t_F, fall time of SDA when transmitting
	0			ns	t_F, fall time of SDA when receiving (CMOS compatible)
			300	ns	t_F, fall time of SCL and SDA when receiving
	20 + 0.1C_B[3]			ns	t_F, fall time of SCL and SDA when transmitting
C_B[3]			400	pF	Capacitive load for each bus line

[1] Guaranteed by design and characterization; not production tested.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[3] C_B is the total capacitance of one bus line in pF. t_R and t_F are measured between 0.3 V_{DD} and 0.7 V_{DD}.

Timing Diagram

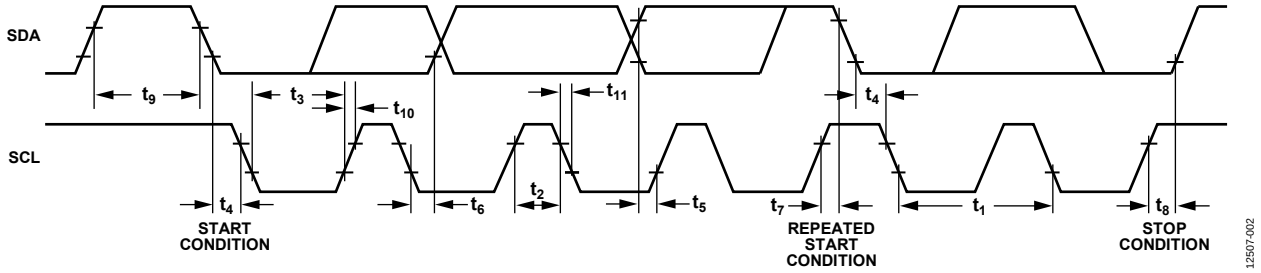

Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{LOGIC} +0.3 V
V_{REF} to GND	−0.3 V to V_{DD} +0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	+150°C
Lead Temperature	JEDEC industry-standard
Soldering	J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead TSSOP	112	°C/W
16-Lead LFCSP	137	°C/W
16-ball WLCSP	60	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

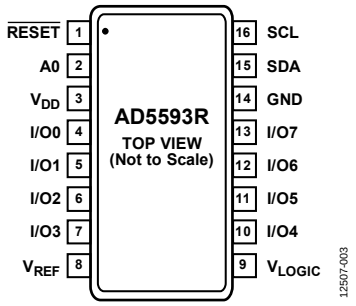

Figure 3. 16-Lead TSSOP Pin Configuration

Table 6. 16-Lead TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5593R is reset to its default configuration.
2	A0	Address Input. Sets the LSB of the 7-bit slave address.
3	V_{DD}	Power Supply Input. The AD5593R can operate from 2.7 V to 5.5 V. Decouple the supply with a 0.1 µF capacitor to GND.
4 to 7, 10 to 13	I/O0 to I/O7	Input/Output 0 Through Input/Output 7. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the appropriate bits in the configuration registers.
8	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on the V_{REF} pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5593R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
9	V_{LOGIC}	Interface Power Supply. The voltage on this pin ranges from 1.8 V to 5.5 V.
14	GND	Ground Reference Point for All Circuitry.
15	SDA	Serial Data Input. This pin is used in conjunction with the SCL line to clock data in to or out of the input shift register. SDA is a bidirectional, open-drain line that must be pulled to the V_{LOGIC} supply with an external pull-up resistor.
16	SCL	Serial Clock Line. This pin is used in conjunction with the SDA line to clock data in to or out of the 16-bit input register.

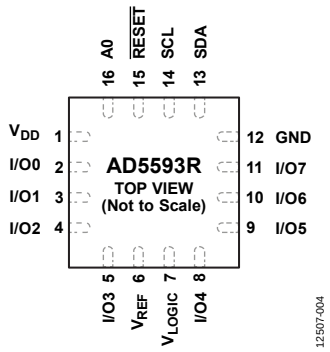

Figure 4. 16-Lead LFCSP Pin Configuration

Table 7. 16-Ball LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The AD5593R operates from 2.7 V to 5.5 V. Decouple the supply with a 0.1 µF capacitor to GND.
2 to 5, 8 to 11	I/O0 to I/O7	Input/Output 0 through Input/Output 7. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the appropriate bits in the configuration registers.
6	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on the pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5593R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
7	V_{LOGIC}	Interface Power Supply. The voltage ranges from 1.8 V to 5.5 V.
12	GND	Ground Reference Point for All Circuitry.
13	SDA	Serial Data Input. This pin is used in conjunction with the SCL line to clock data into or out of the input shift register. SDA is a bidirectional, open-drain line that must be pulled to the V_{LOGIC} supply with an external pull-up resistor.
14	SCL	Serial Clock Line. This is pin used in conjunction with the SDA line to clock data into or out of the 16-bit input register.
15	$\overline{\text{RESET}}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5593R is reset to its default configuration.
16	A0	Address Input. This pin sets the LSB of the 7-bit slave address.

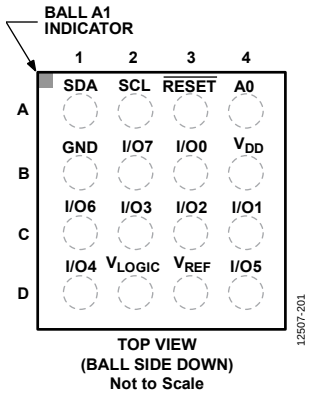

Figure 5. 16-Ball WLCSP Pin Configuration

Table 8. 16-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
A3	$\overline{\text{RESET}}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5593R is reset to its default configuration.
A4	A0	Address Input. Sets the LSB of the 7-bit slave address.
B4	V_{DD}	Power Supply Input. The AD5593R can operate from 2.7 V to 5.5 V. Decouple the supply with a 0.1 µF capacitor to GND.
B3, C4, C3, C2, D1, D4, C1, B2	I/O0 to I/O7	Input/Output 0 through Input/Output 7. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the appropriate bits in the configuration registers.
D3	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on the pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5593R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
D2	V_{LOGIC}	Interface Power Supply. The voltage ranges from 1.8 V to 5.5 V.
B1	GND	Ground Reference Point for All Circuitry.
A1	SDA	Serial Data Input. This pin is used in conjunction with the SCL line to clock data into or out of the input shift register. SDA is a bidirectional, open-drain line that must be pulled to the V_{LOGIC} supply with an external pull-up resistor.
A2	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input register.

TYPICAL PERFORMANCE CHARACTERISTICS

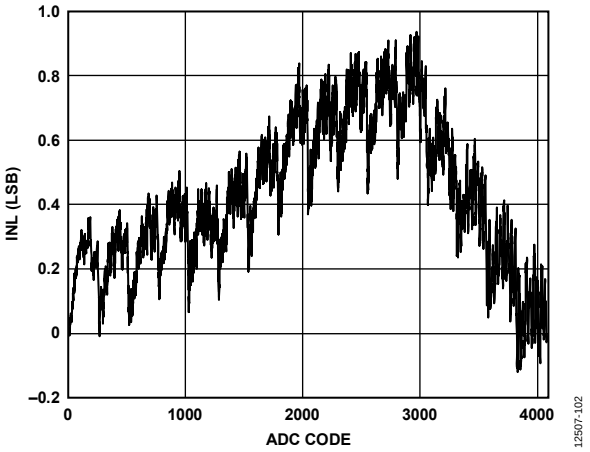

Figure 6. ADC INL; V_{DD} = 5.5 V

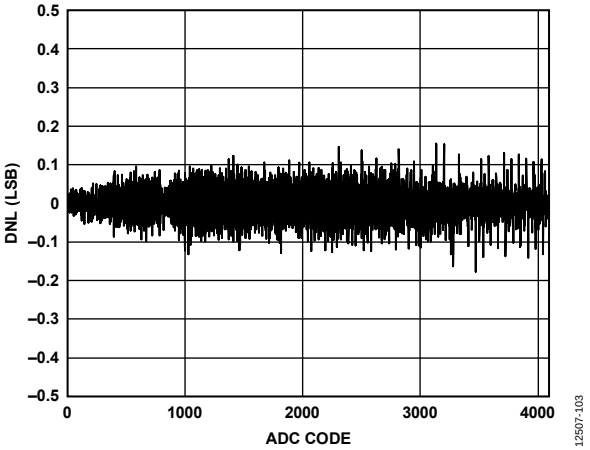

Figure 7. ADC DNL; V_{DD} = 5.5 V

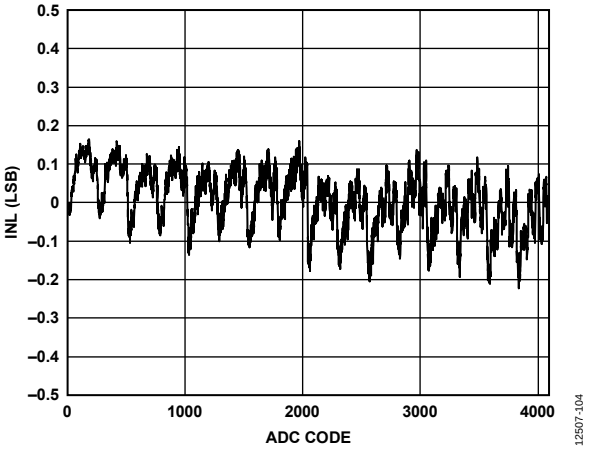

Figure 8. ADC INL; V_{DD} = 2.7 V

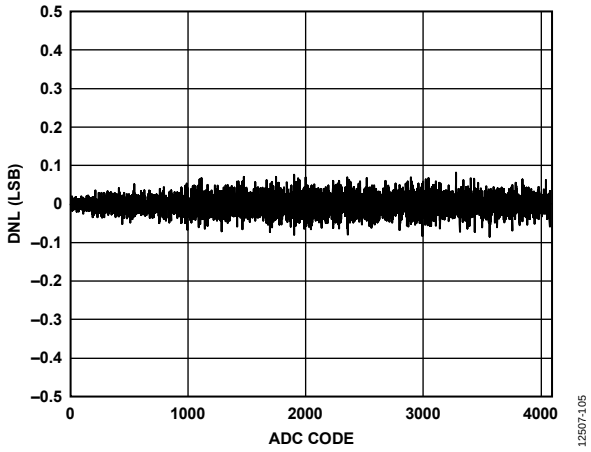

Figure 9. ADC DNL; V_{DD} = 2.7 V

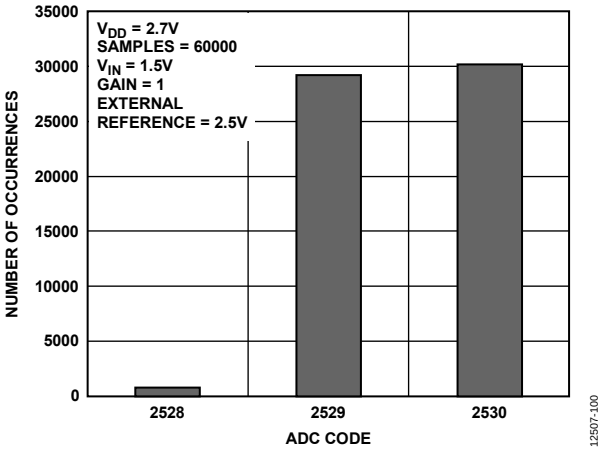

Figure 10. Histogram of ADC Codes; V_{DD} = 2.7 V

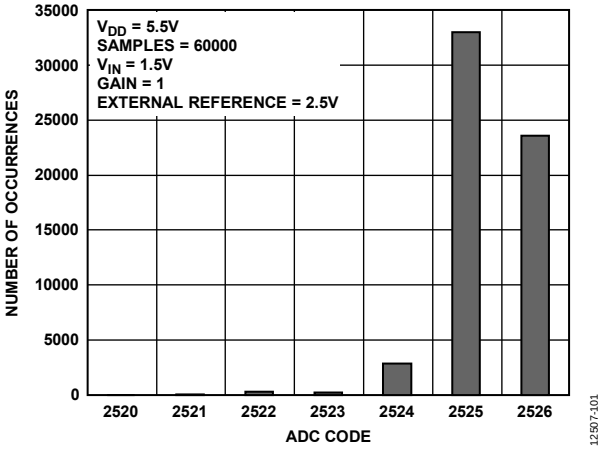

Figure 11. Histogram of Codes; V_{DD} = 5.5 V

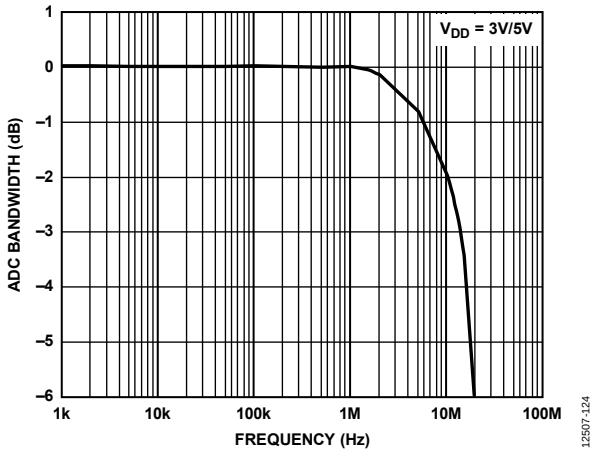

Figure 12. ADC Bandwidth

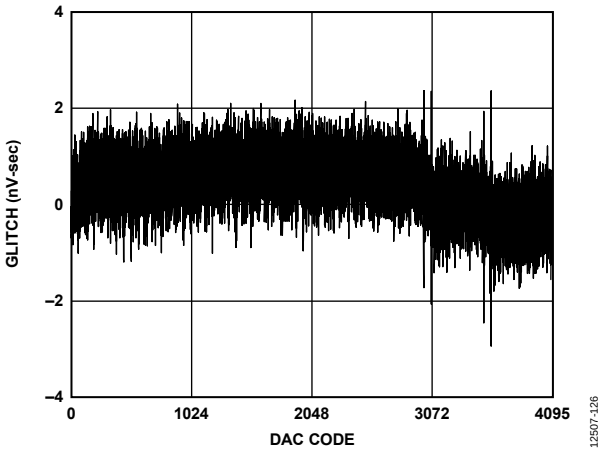

Figure 15. DAC Adjacent Code Glitch

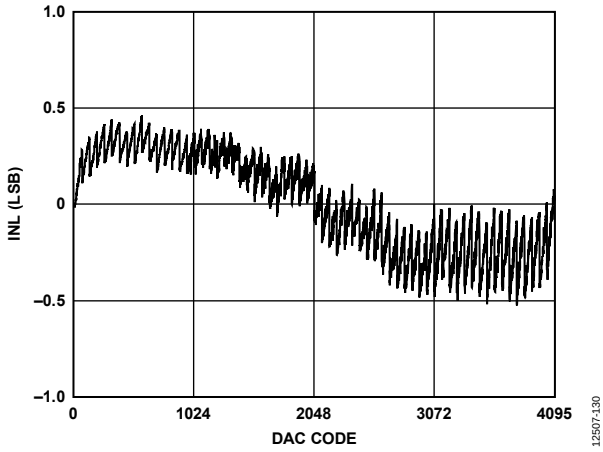

Figure 13. DAC INL

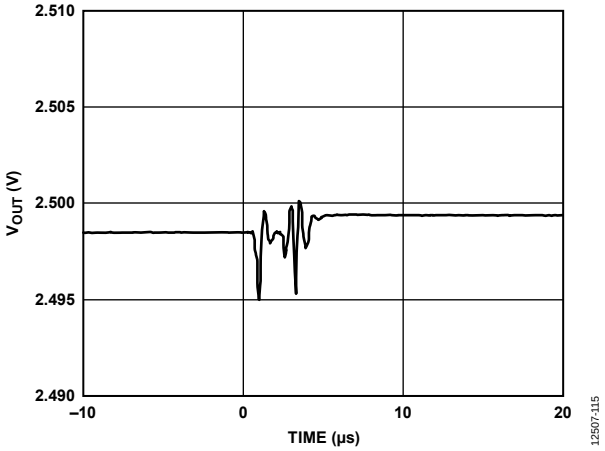

Figure 16. DAC Digital to Analog Glitch (Rising)

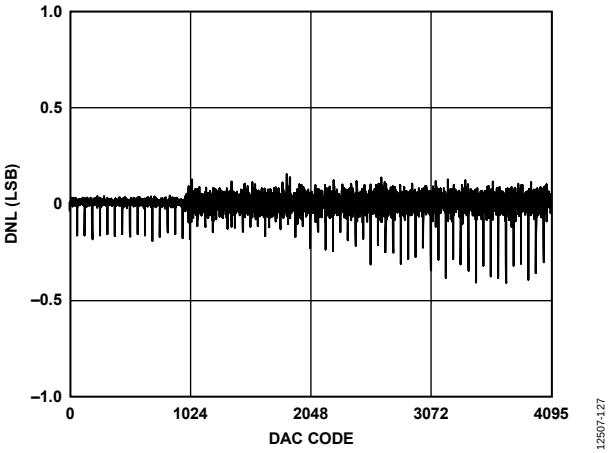

Figure 14. DAC DNL

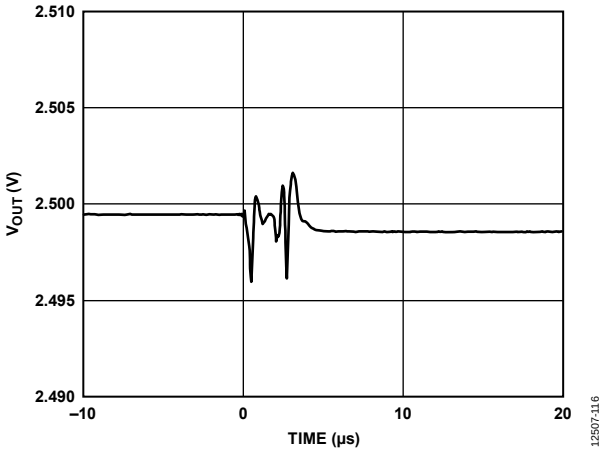

Figure 17. DAC Digital to Analog Glitch (Falling)

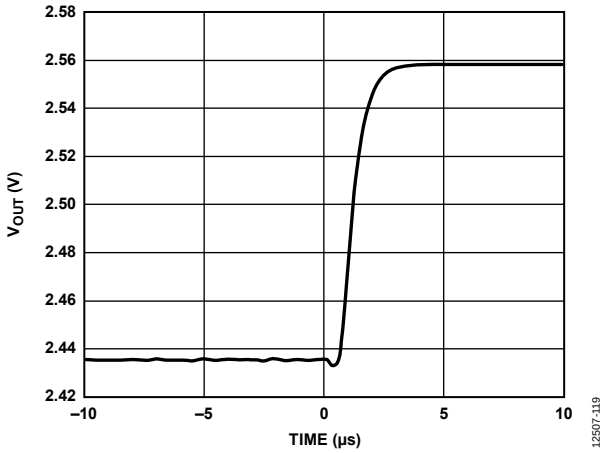

Figure 18. DAC Settling Time (100 Code Change, Rising Edge)

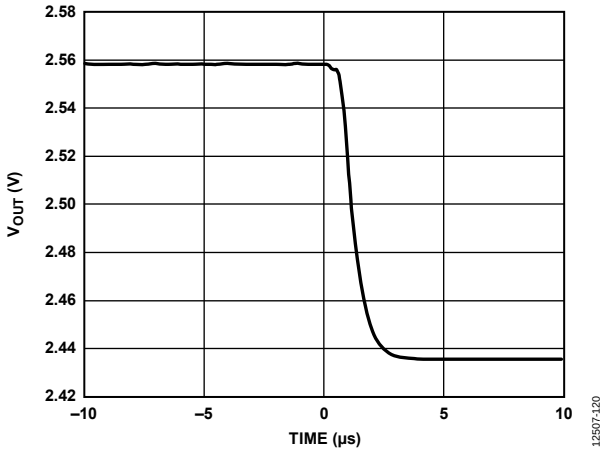

Figure 19. DAC Settling Time (100 Code Change, Falling Edge)

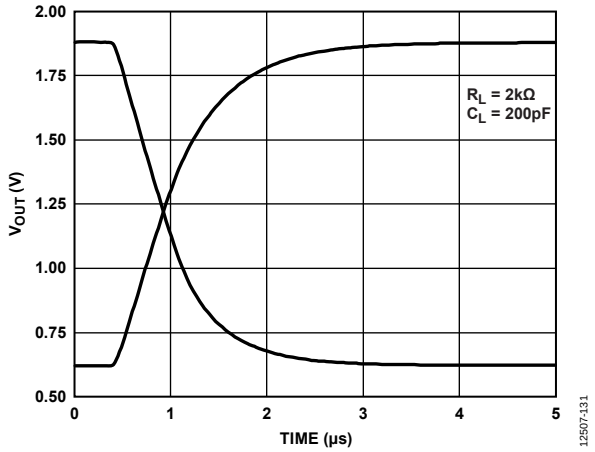

Figure 20. DAC Settling Time, Output Range = 0 V to V_{REF}

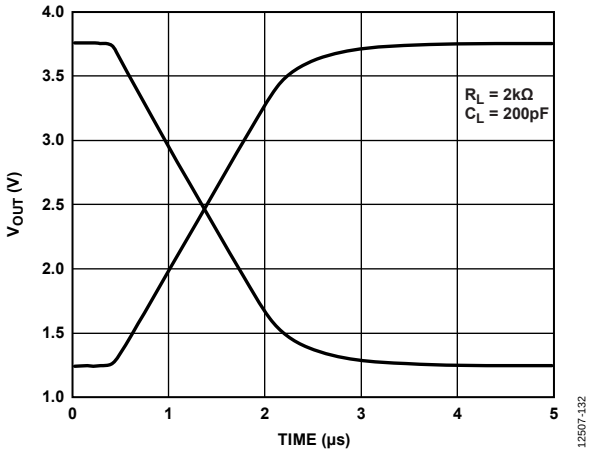

Figure 21. DAC Settling Time, Output Range = 0 V to 2 × V_{REF}

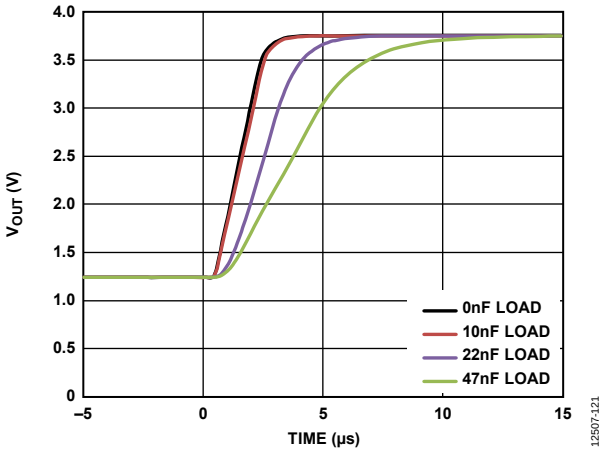

Figure 22. DAC Settling Time vs. Capacitive Load

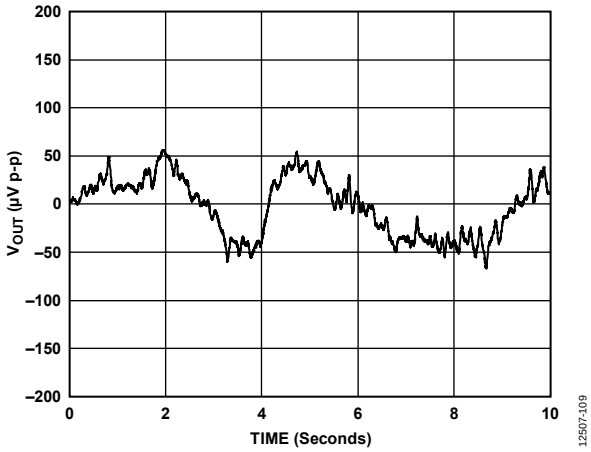

Figure 23. DAC 1/f Noise with External Reference

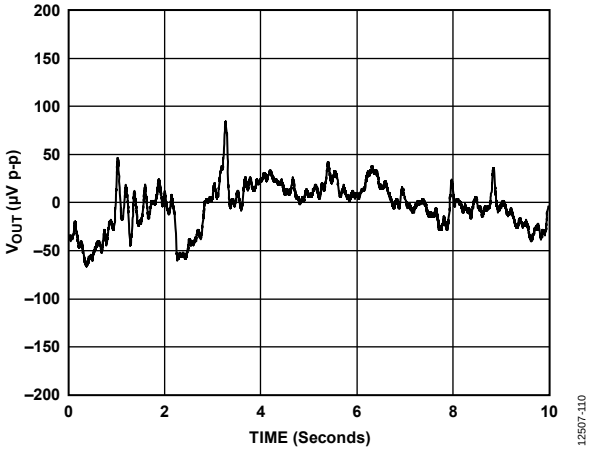

Figure 24. DAC 1/f Noise with Internal Reference

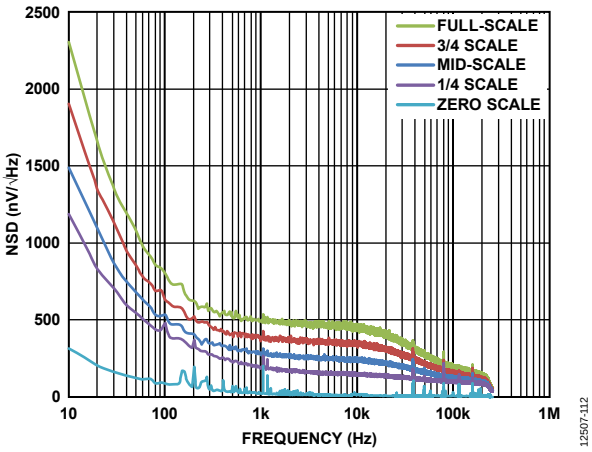

Figure 25. DAC Output Noise Spectral Density

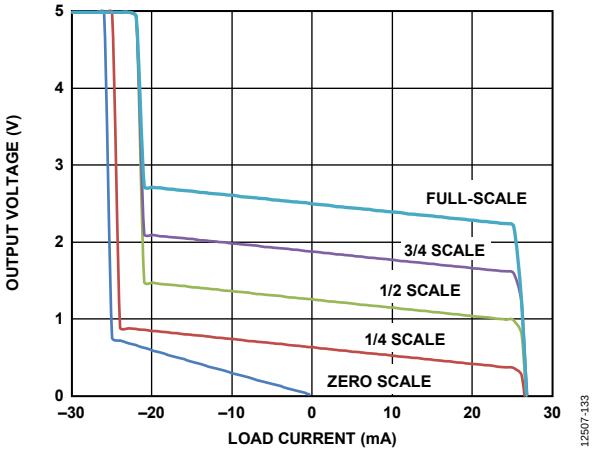

Figure 26. DAC Output Sink and Source Capability, Output Range = 0 V to V_{REF}

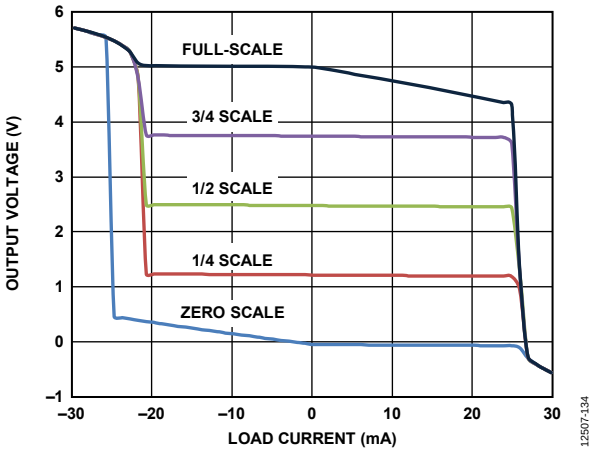

Figure 27. DAC Output Sink and Source Capability, Output Range = 0 V to 2 × V_{REF}

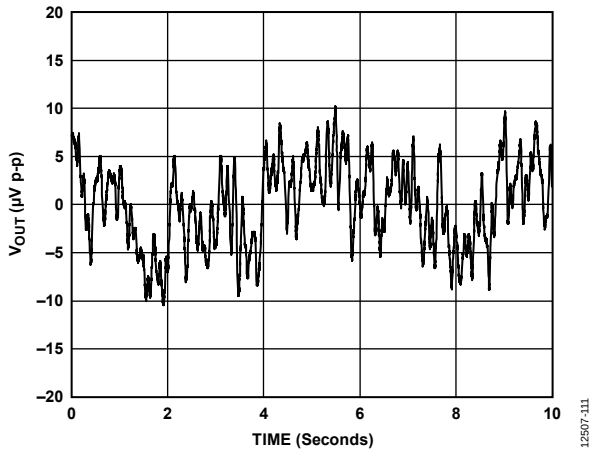

Figure 28. Internal Reference 1/f Noise

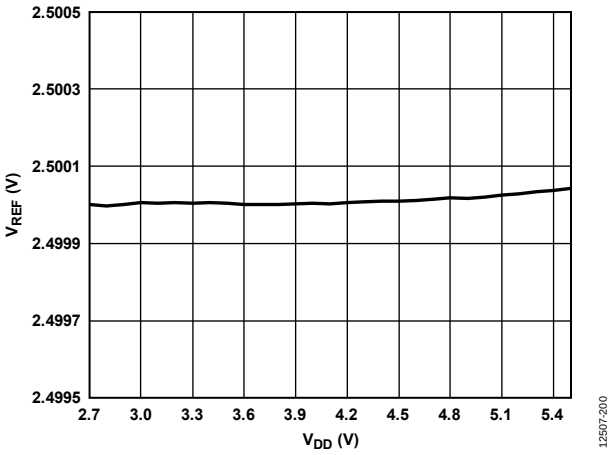

Figure 30. Reference Line Regulation

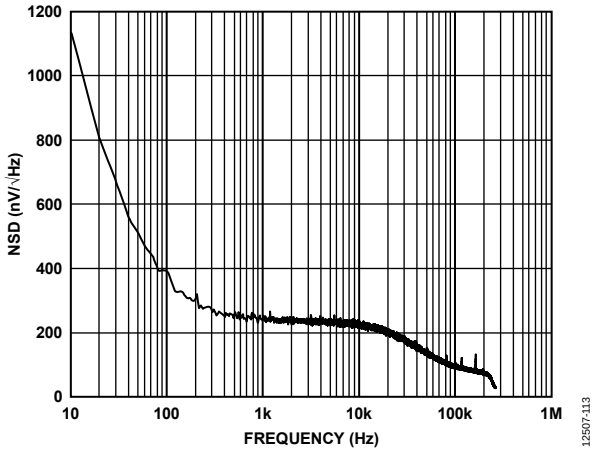

Figure 29. Reference Noise Spectral Density

TERMINOLOGY

ADC Integral Nonlinearity (INL)
For the ADC, INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The end points of the transfer function are zero scale, a point that is 1 LSB below the first code transition, and full scale, a point that is 1 LSB above the last code transition.

ADC Differential Nonlinearity (DNL)
For the ADC, DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
Offset error is the deviation of the first code transition (00 … 000) to (00 … 001) from the ideal, that is, AGND + 1 LSB.

Gain Error
Gain error is the deviation of the last code transition (111 … 110) to (111 … 111) from the ideal (that is, V_{REF} − 1 LSB) after the offset error has been adjusted out.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 5 kHz sine wave signal to all nonselected ADC input channels and determining how much that signal is attenuated in the selected channel. This specification is the worst case across all ADC channels for the AD5593R.

ADC Power Supply Rejection Ratio (PSRR)
For the ADC, variations in power supply affect the full-scale transition, but not the converter linearity. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Track-and-Hold Acquisition Time
The track-and-hold amplifier goes into track mode when the ADC sequence register has been written to. The track and hold amplifier goes into hold mode when the conversion starts (see Figure 37). Track-and-hold acquisition time is the minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within ±1 LSB of the applied input signal, given a step change to the input signal.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the measured ratio of signal to (noise + distortion) at the output of the analog-to-digital converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD for an ideal N-bit converter with a sine wave input is given by

Signal-to-(Noise + Distortion) (dB) = 6.02*N* + 1.76

Thus, for a 12-bit converter, this is 74 dB.

ADC Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD5593R, it is defined as

$$THD\,(\mathrm{dB}) = 20 \times \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

DAC Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 13.

DAC Differential Nonlinearity (DNL)
For the DAC, differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 14.

Zero Code Error
Zero code error is a measurement of the output error when zero code (0x000) is loaded to the DAC register. Ideally, the output is 0 V. The zero code error is always positive in the AD5593R because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error can be negative or positive.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

DAC DC Power Supply Rejection Ratio (PSRR)
For the DAC, PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of SDA that generates the stop condition.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FF to 0x800) (see Figure 16 and Figure 17).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Noise Spectral Density (NSD)
NSD is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. A plot of noise spectral density is shown in Figure 25.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is first measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then it is measured by executing a software LDAC and monitoring the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this finite bandwidth. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

DAC Total Harmonic Distortion (THD)
For the DAC, THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Voltage Reference Temperature Coefficient (TC)
Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The voltage reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(NOM)} \times Temp\ Range} \right] \times 10^6$$

where:
$V_{REF(MAX)}$ is the maximum reference output measured over the total temperature range.
$V_{REF(MIN)}$ is the minimum reference output measured over the total temperature range.
$V_{REF(NOM)}$ is the nominal reference output voltage, 2.5 V.
Temp Range is the specified temperature range of −40°C to +105°C.

THEORY OF OPERATION

The AD5593R is an 8-channel, configurable analog and digital I/O port. The AD5593R has eight pins that can be independently configured as a 12-bit DAC output channel, a 12-bit ADC input channel, a digital input pin, or a digital output pin.

The function of each pin is determined by programming the ADC, DAC, or GPIO configuration registers as appropriate.

DAC SECTION

The AD5593R contains eight 12-bit DACs. Each DAC consists of a string of resistors followed by an output buffer amplifier. Figure 31 shows a block diagram of the DAC architecture.

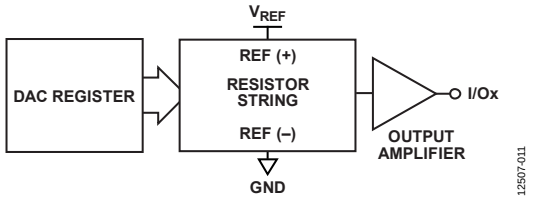

Figure 31. DAC Channel Architecture Block Diagram

The DAC channels share a single DAC range bit (see Bit D4 in Table 13) that sets the output range to 0 V to V_{REF} or 0 V to 2 × V_{REF}. Because the range bit is shared by all channels, it is not possible to set different output ranges on a per channel basis. The input coding to the DAC is straight binary. Therefore, the ideal output voltage is given by

$$V_{OUT} = G \times V_{REF} \times \left(\frac{D}{2^N} \right)$$

where:
G = 1 for an output range of 0 V to V_{REF} or G = 2 for an output range of 0 V to 2 × V_{REF}.
V_{REF} is the voltage on the V_{REF} pin.
D is the decimal equivalent of the binary code (0 to 4095) that is loaded to the DAC register.
N = 12.

Resistor String

The simplified segmented resistor string DAC structure is shown in Figure 32. The code loaded to the DAC register determines the switch on the string that is connected to the output buffer.

Because each resistance in the string has the same value, R, the string DAC is guaranteed monotonic.

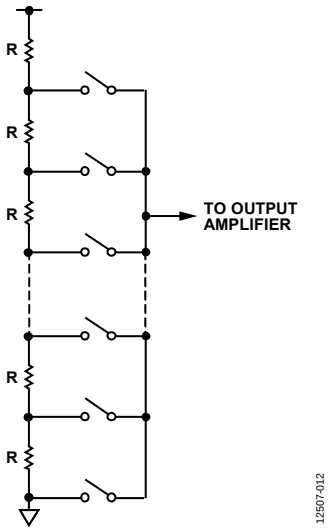

Figure 32. Resistor String

DAC Output Buffer

The output buffer is designed as an input/output rail-to-rail buffer. The output buffer can drive 2 nF capacitance with a 1 kΩ resistor in parallel. The slew rate is 1.25 V/µs with a ¼ to ¾ scale settling time of 6 µs. By default, the DAC outputs update directly after data has been written to the input register. The LDAC register delays the updates until additional channels have been written to if required. See the LDAC Mode Operation section for more information.

ADC SECTION

The ADC section is a fast, 12-bit, single-supply ADC with a conversion time of 2 µs. The ADC is preceded by a multiplexer that switches selected I/O pins to the ADC. A sequencer is included to switch the multiplexer to the next selected channel automatically. Channels are selected for conversion by writing to the ADC sequence register. When the write to the ADC sequence register has completed, the first channel in the conversion sequence is put into track mode. Each channel can track the input signal for a minimum of 500 ns. The conversion is initiated on the rising edge of the clock for the acknowledge (ACK) that occurs after the slave address (see Figure 37).

Each conversion takes 2 µs. The ADC has a range bit (ADC range select in the general-purpose control register, see Bit D5 in Table 13) that sets the input range as 0 V to V_{REF} or 0 V to 2 × V_{REF}. All input channels share the same range. The output coding of the ADC is straight binary. It is possible to set each I/Ox pin as both a DAC and an ADC. In this case, the primary function is that of the DAC. If the pin is selected for inclusion in an ADC conversion sequence, the voltage on the pin is converted and made available via the serial interface. This allows the DAC voltage to be monitored.

Calculating ADC Input Current

The current flowing into the I/Ox pins configured as ADC inputs varies with sampling rate (f_S), the voltage difference between successive channels (V_{DIFF}), and whether buffered or unbuffered mode is used. Figure 33 shows a simplified version of the ADC input structure. When a new channel is selected for conversion, 5.8 pF must be charged to or discharged from the voltage that on the previously selected channel. The time required for the charge or discharge depends on the voltage difference between the two channels. This dependence affects the input impedance of the multiplexer and, therefore, the input current flowing into the I/Ox pins.

In buffered mode, Switch S1 is open and Switch S2 is closed. In buffered mode, the U1 buffer directly drives the 23.1 pF capacitor and the charging time of the capacitors is negligible. In unbuffered mode, Switch S1 is closed and Switch S2 is closed. In unbuffered mode, the 23.1 pF capacitor must be charged from the I/Ox pins; this charging contributes to the input current. For applications where the ADC input current is too high, an external input buffer may be required. The choice of buffer is a function of the particular application.

Calculate the input current for buffered mode as follows:

$$f_S \times C \times V_{DIFF} + 1 \text{ nA}$$

where:
f_S is the ADC sample rate in Hz.
C is the sampling capacitance in farads.
V_{DIFF} is the voltage change between successive channels.

Calculate the input current for buffered mode as follows:

$$f_S \times C \times V_{DIFF}$$

where 1 nA is the dc leakage current associated with unbuffered mode.

The input current for the ADC in buffered mode, where I/O0 = 0.5 V, I/O1 = 2 V, and f_S = 10 kHz, is as follows:

$$(10{,}000 \times 5.8 \times 10^{-12} \times 1.5) + 1 \text{ nA} = 88 \text{ nA}$$

Under the same conditions, the ADC input current in unbuffered mode is as follows:

$$(10{,}000 \times 28.9 \times 10^{-12} \times 1.5) = 433.5 \text{ nA}$$

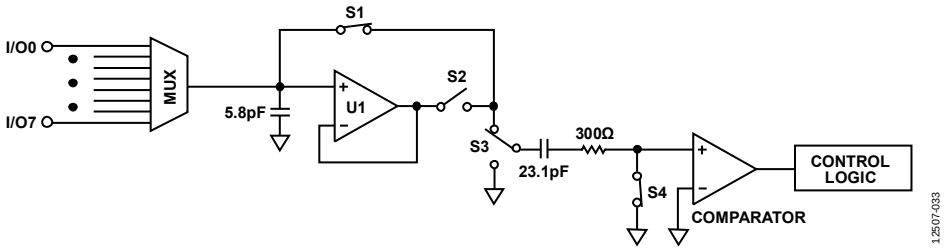

Figure 33. ADC Input Structure

GPIO SECTION

Each of the eight I/Ox pins can be configured as a general-purpose digital input or output pin by programming the GPIO control register. When an I/Ox pin is configured as an output, the pin can be set high or low by programming the GPIO write data register. Logic levels for general-purpose outputs are relative to V_{DD} and GND. When an I/Ox pin is configured as an input, its status can be determined by reading the GPIO read configuration register. When an I/Ox pin is set as an output, it is possible to read its status by also setting it as an input pin. When reading the status of the I/Ox pins set as inputs the status of an I/Ox pin set as both and input and output pin is also returned.

INTERNAL REFERENCE

The AD5593R contains an on-chip 2.5 V reference. The reference is powered down by default and is enabled by setting Bit D9 in the power-down/reference control register to 1. When the on-chip reference is powered up, the reference voltage appears on the V_{REF} pin and may be used as a reference source for other components. When the internal reference is used, it is recommended to decouple V_{REF} to GND using a 100 nF capacitor. It is recommended that the internal reference be buffered before using it elsewhere in the system. When the reference is powered down, an external reference must be connected to V_{REF}. Suitable external reference sources for the AD5593R include the AD780, AD1582, ADR431, REF193, and ADR391.

RESET FUNCTION

The AD5593R has an asynchronous $\overline{\text{RESET}}$ pin. For normal operation, $\overline{\text{RESET}}$ is tied high. A falling edge on $\overline{\text{RESET}}$ resets all registers to their default values and reconfigures the I/O pins to their default values (85 kΩ pull-down resistor to GND). The reset function takes 250 µs maximum; do not write new data to the AD5593R during this time. The AD5593R has a software reset that performs the same function as the $\overline{\text{RESET}}$ pin. The reset function is activated by writing 0x0F to the pointer byte and 0x0D and 0xAC to the most significant and least significant bytes, respectively.

TEMPERATURE INDICATOR

The AD5593R contains an integrated temperature indicator that can be read to provide an estimation of the die temperature. This can be used in fault detection where a sudden rise in die temperature may indicate a fault condition, such as a shorted output. Temperature readback is enabled by setting Bit D8 in the ADC sequence register. The temperature result is then added to the ADC sequence. The temperature result has an address of 0b1000 and care must be taken that this result is not confused with the readback from DAC0. The temperature conversion takes 5 µs with the ADC buffer enabled and 20 µs when the buffer is disabled. Calculate the temperature using the following formulae:

For ADC gain = 1,

$$Temperature\ (°C) = 25 + \frac{ADC\ Code - 820}{2.654}$$

For ADC gain = 2,

$$Temperature\ (°C) = 25 + \frac{ADC\ Code - 410}{2.654}$$

The range of codes returned by the ADC when reading from the temperature indicator is approximately 645 to 1035, corresponding to a temperature between −40°C to +105°C. The accuracy of the temperature indicator is typically 3°C when averaged over five samples.

SERIAL INTERFACE

The AD5593R has a 2-wire, I²C-compatible serial interface (refer to *The I²C -Bus Specification*, Version 2.1, January 2000). The AD5593R is connected to an I²C bus as a slave device under the control of a master device. See Figure 2 for a timing diagram of a typical write sequence. The AD5593R supports standard mode (100 kHz) and fast mode (400 kHz). Support is not provided for 10-bit addressing and general call addressing. The AD5593R has a 7-bit slave address; its six MSBs are set to 001000. The LSB is set by the state of the A0 address pin, which determines the state of the A0 bit. The facility to change the logic level of the A0 pin before a read or write operation allows the user to incorporate multiple AD5593R devices on one bus.

The 2-wire serial bus protocol operates as follows: the master initiates data transfer by establishing a start condition when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.

Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL. When all data bits have been read or written, a stop condition is established.

In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master brings the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a stop condition.

WRITE OPERATION

When writing to the AD5593R, the user must begin with a start command followed by an address byte R/$\overline{W}$ = 0), after which the AD5593R acknowledges that it is prepared to receive data by pulling SDA low. The AD5593R requires three bytes of data. The first byte is the pointer byte. This byte contains information defining the type of operation that is required of the AD5593R, such as configuring the I/O pins and writing to a DAC. The pointer byte is followed by the most significant byte and the least significant byte, as shown in Figure 34. After these data bytes are acknowledged by the AD5593R, a stop condition follows.

READ OPERATION

When reading data back from the AD5593R, the user begins with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to transmit data by pulling SDA low. The pointer byte is then written to select what is to be read back. A repeat start or a new I²C transmission can then follow to read two bytes of data from the AD5593R. Both bytes are acknowledged by the master, as shown in Figure 35.

It is also possible to perform consecutive readbacks without having to provide interim start and stop conditions or slave addresses. This method can be used to read blocks of conversions from the ADC, as shown in Figure 37.

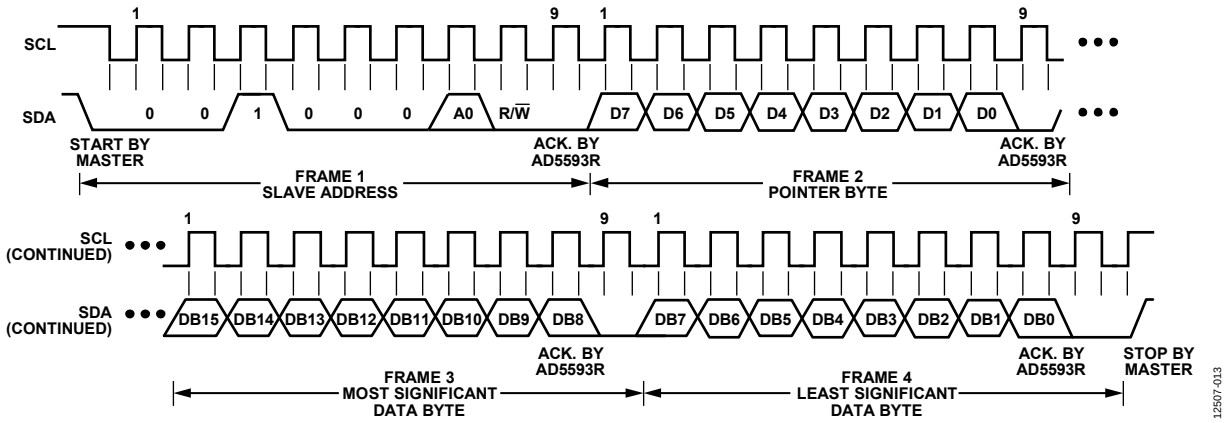

Figure 34. 4-Byte I²C Write

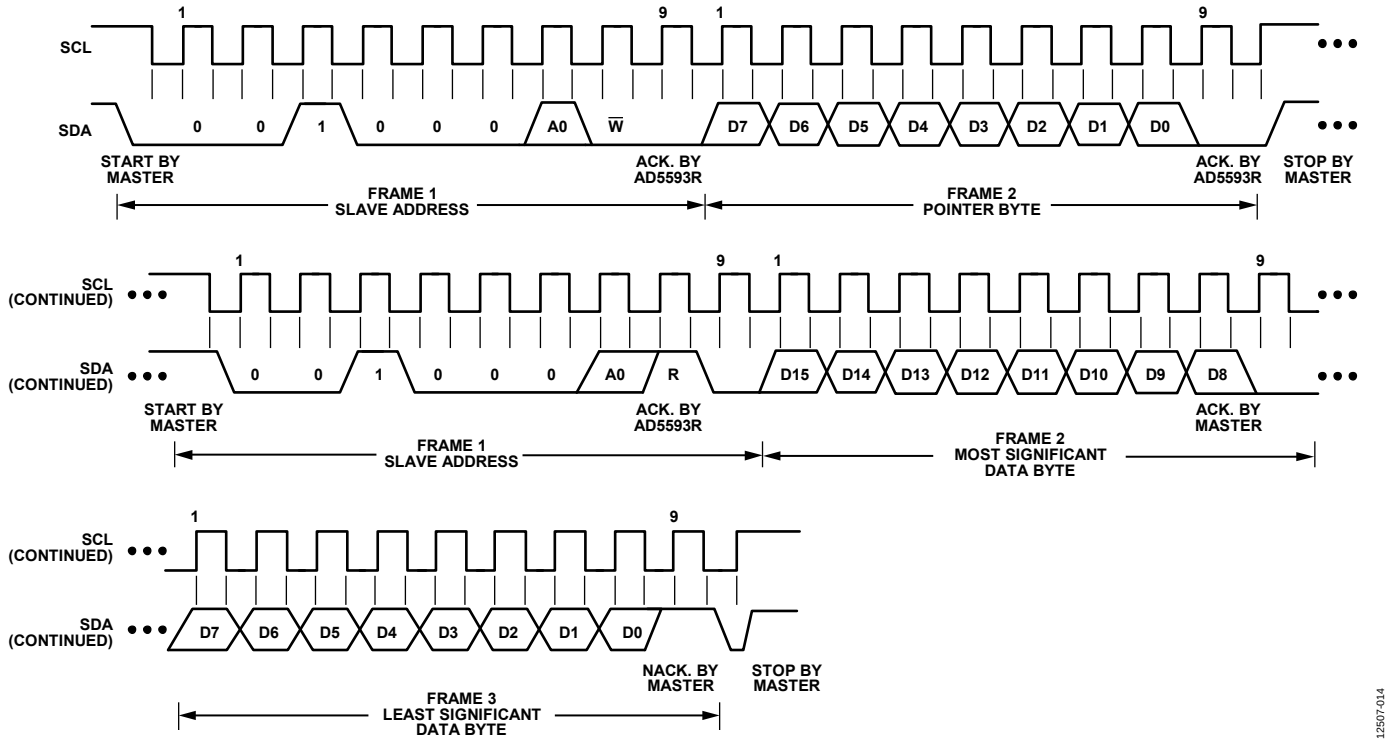

Figure 35. Read One 16-Bit Word

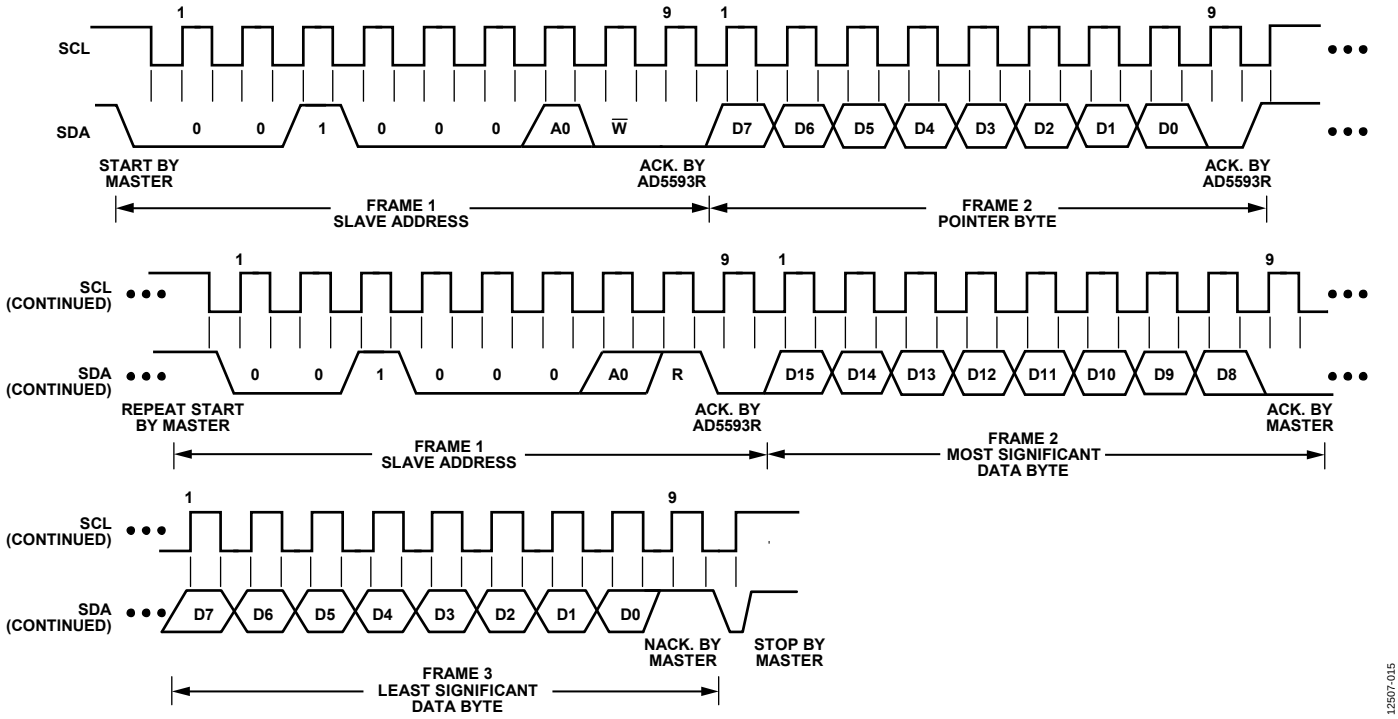

Figure 36. Read One 16-Bit Word, Maintain Control of the Bus

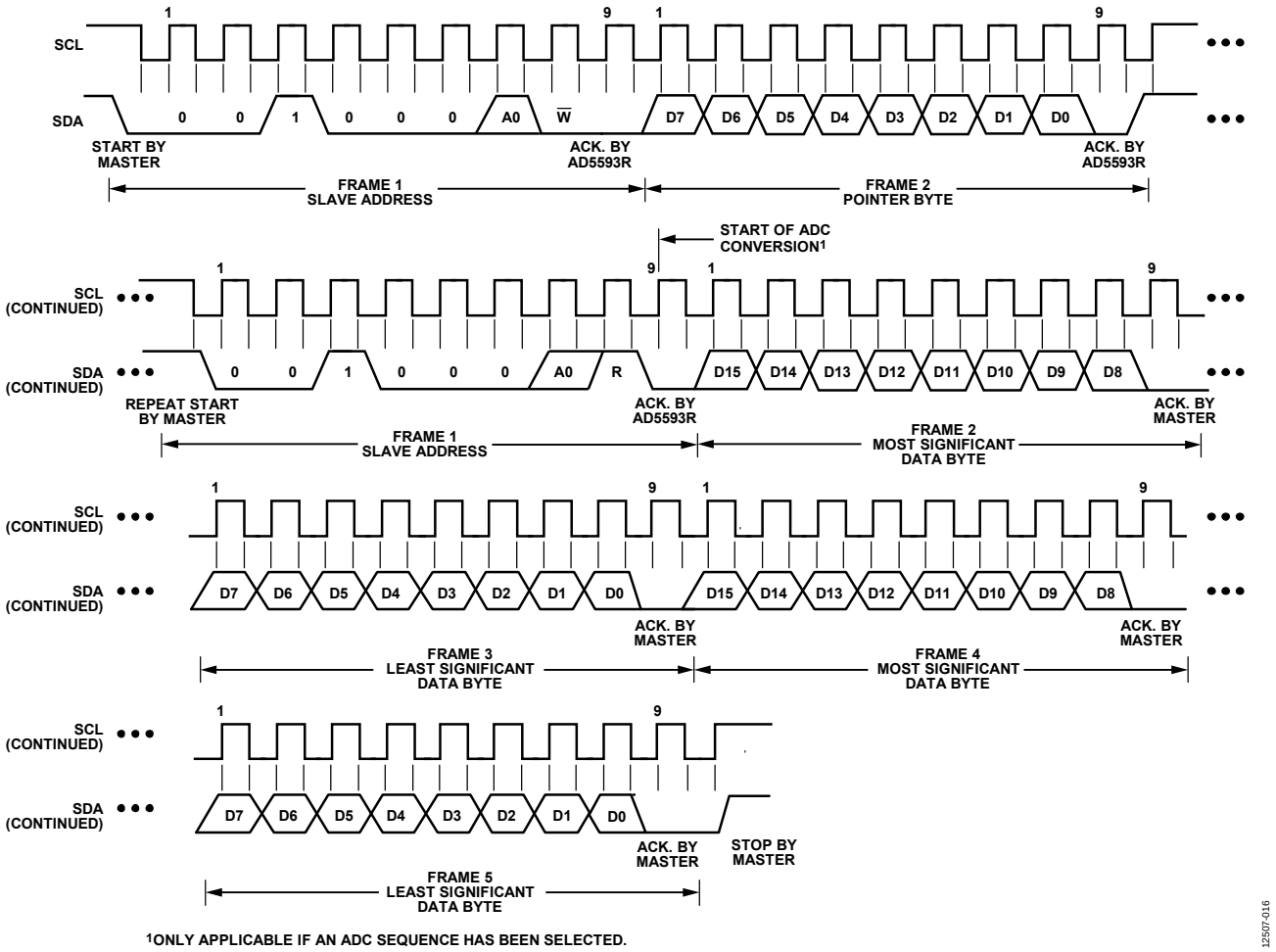

Figure 37. I²C Block Read

POINTER BYTE

The pointer byte contains eight bits. Bits[D7:D4] are mode bits that select the operation to be executed. The data contained in Bits[D3:D0] depend on the operation required. Table 9 shows the configuration of the pointer byte. When Bits[D7:D4] are 0b0000, the mode dependent bits (Bits[D3:D0]) select a control register to write data to. The data written to a control register is contained in the MSB and LSB as shown in Figure 34. The mode dependent data bits also select which DAC is updated during a DAC write operation and which register is selected for readback.

Table 9. Pointer Byte Configuration

D7	D6	D5	D4	D3	D2	D1	D0
Mode bits				Mode dependent data bits			

Table 10. Mode Bits

D7	D6	D5	D4	Description
0	0	0	0	Configuration mode
0	0	0	1	DAC write
0	1	0	0	ADC readback
0	1	0	1	DAC readback
0	1	1	0	GPIO readback
0	1	1	1	Register readback

CONTROL REGISTERS

Table 11 shows the control register map for the AD5593R. The control registers configure the I/O pins and set various operating parameters in the AD5593R, such as enabling the reference, selecting the LDAC mode function, or selecting power-down modes. The control registers are written to using the 4-byte I²C write sequence shown in Figure 34. To write to a control register, the mode bits (Bits[D7:D4]) of the pointer byte are zeros. The mode dependent data bits (Bits[D3:D0]) of the pointer byte select which control register is to be accessed. The data to be written to the control register is contained in the most significant and least significant data bytes. These contain a total of 16 bits and are shown as D15 to D0 in Table 12 and Table 13. The contents of the control registers can be read back using the read sequence shown in Figure 35 or Figure 36.

GENERAL-PURPOSE CONTROL REGISTER

The general-purpose control register enables or disables certain functions associated with the DAC, ADC, and I/O pin configuration (see Table 13). The register sets the output range of the DAC and input range of the ADC, which sets their transfer functions, enables/disables the ADC buffer, and enables the precharge function (see the ADC Section for more details). The register is also used to lock the I/O pin configuration to prevent accidental change. When Bit D7 is set to 1, writes to the configuration registers are ignored.

Table 11. Control Registers

Pointer Byte [D7:D0]	Register Name	Description	Default Value
00000000	NOP	No operation	0x0000
00000010	ADC sequence register	Selects ADCs for conversion	0x0000
00000011	General-purpose control register	DAC and ADC control register	0x0000
00000100	ADC pin configuration	Selects which pins are ADC inputs	0x0000
00000101	DAC pin configuration	Selects which pins are DAC outputs	0x0000
00000110	Pull-down configuration	Selects which pins have an 85 kΩ pull-down resistor to GND	0x00FF
00000111	LDAC mode	Selects the operation of the load DAC	0x0000
00001000	GPIO write configuration	Selects which pins are general-purpose outputs	0x0000
00001001	GPIO write data	Writes data to general-purpose outputs	0x0000
00001010	GPIO read configuration	Selects which pins are general-purpose inputs	0x0000
00001011	Power-down/reference control	Powers down the DACs and enables/disables the reference	0x0000
00001100	Open-drain configuration	Selects open-drain or push-pull for general-purpose outputs	0x0000
00001101	Three-state pins	Selects which pins are three-stated	0x0000
00001110	Reserved		
00001111	Software reset	Resets the AD5593R	0x0000

Table 12. General-Purpose Control Register

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved						ADC buffer precharge	ADC buffer enable	Lock configuration	Write all DACs	ADC range select	DAC range select	Reserved			

Table 13. General-Purpose Control Register Descriptions

Bits	Description
D15 to D10	Reserved. Set these bits to 0.
D9	ADC buffer precharge. 0: the ADC buffer is not used to precharge the ADC. If the ADC buffer is enabled, it is always powered up (default). 1: the ADC buffer is used to precharge the ADC. If the ADC buffer is enabled, it is powered up while the conversion takes place and then powered down until the next conversion takes place.
D8	ADC buffer enable. 0: the ADC buffer is disabled (default). 1: the ADC buffer is enabled.
D7	Lock configuration. 0: the contents of the I/O pin configuration registers can be changed (default). 1: the contents of the I/O pin configuration registers cannot be changed.
D6	Write all DACs. 0: for future DAC writes, the DAC address bits determine which DAC is written to (default). 1: for future DAC writes, the DAC address bits are ignored and all channels configured as DACs are updated with the same data.
D5	ADC range select. 0: the ADC range is 0 to V_{REF} (default). 1: the ADC range is 0 to $2 \times V_{REF}$.
D4	DAC range select. 0: the DAC range is 0 to V_{REF} (default). 1: the DAC range is 0 to $2 \times V_{REF}$.
D3 to D0	Reserved; set these bits to 0.

CONFIGURING THE AD5593R

The AD5593R I/O pins are configured by writing to a series of pin configuration registers. The control registers are accessed when Bits[D7:D4] are 0b0000. Bits[D3:D0] determine which register is accessed as shown in Table 11.

On power-up, the I/O pins are configured as 85 kΩ resistors connected to GND. The I/O channels of the AD5593R can be configured to operate as DAC outputs, ADC inputs, digital outputs, digital inputs, three-state, or connected to GND with 85 kΩ pull-down resistors. When configured as digital outputs, the pins have the additional option of being configured as push/pull or open-drain.

The I/O channels are configured by writing to the appropriate configuration registers, as shown in Table 11. To assign a particular function for an I/O channel, write to the appropriate register and set the corresponding bit to 1. For example, setting Bit D0 in the DAC configuration register configures I/O0 as a DAC. In the event that the bit for an I/O channel is set in multiple configuration registers, the I/O channel adopts the function dictated by the last write operation.

The exceptions to this rule are that an I/Ox pin can be set as both a DAC and ADC or as a digital input and output. When an I/Ox pin is configured as a DAC and ADC, the primary function is as a DAC and the ADC can be used to measure the voltage being provided by the DAC. This feature can be used to monitor the output voltage to detect short circuits or overload conditions. Figure 38 shows an example of how to configure I/O1 and I/O7 as DACs. When a pin is configured as both a general-purpose input and output, the primary function is as an output pin. This configuration allows the status of the output pin to be determined by reading the GPIO read configuration register.

The general-purpose control register contains a lock configuration bit. When the lock configuration bit is set to 1, any writes to the pin configuration registers are ignored, thus preventing the function of the I/O pins from being changed.

The I/O pins can be reconfigured any time when the AD5593R is in an idle state, that is, no ADC conversions are taking place and no registers are being read back. The lock configuration bit must also be set to 0.

Table 14. I/O Pin Configuration Registers[1]

D7	D6	D5	D4	D3	D2	D1	D0
I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0

[1] Setting an I/O pin configuration bit to 1 after writing to a control register enables that function on the selected I/O pin.

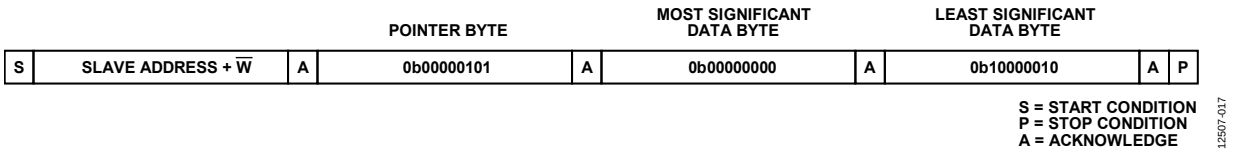

Figure 38. Configuring I/O1 and I/O7 as DACs

DAC WRITE OPERATION

Data is written to a DAC when the mode bits (Bits[D7:D4]) of the pointer byte are 0b0001 (see Table 10). Bits[D2:D0] determine which DAC is addressed. Data to be written to the DAC is contained in the MSB and LSB, as shown in Table 17. Data is written to the selected DAC input register. Data written to the input register can be automatically copied to the DAC register, if required. Data is transferred to the DAC register based on the setting of the LDAC mode register (see Table 15).

LDAC Mode Operation

The transfer of data from an input register to a DAC register is controlled by Bit D1 and Bit D0 of the readback and LDAC mode register (pointer byte = 0b00000111). When the LDAC mode bits (Bit D1 and Bit D0) are set to 00, new data is automatically transferred from the input register to the DAC register and the analog output updates. When the LDAC mode bits are set to 01, data remains in the input register. This allows writes to input registers without affecting the analog outputs. After loading the input registers with the desired values and setting the LDAC mode bits to 10, the values in the input registers transfer to the DAC registers and the analog outputs update simultaneously. The LDAC mode bits then revert to 01.

Table 15. LDAC Mode Register

D1	D0	LDAC Mode
0	0	Data written to an input register is immediately copied to a DAC register and the DAC output updates (default).
0	1	Data written to an input register is not copied to a DAC register. The DAC output is not updated.
1	0	Data in the input registers is copied to the corresponding DAC registers. When the data has been transferred, the DAC outputs are updated simultaneously.
1	1	Reserved.

DAC READBACK

The input register of each DAC can be read back via the I²C interface. This can be useful to confirm that the data was received correctly before writing to the LDAC register or simply checking what value was last loaded to a DAC. Data can be read back from a DAC only when no ADC conversion sequence is taking place. A DAC input register can be read back using the sequence shown in Figure 35 or Figure 36. The mode bits, Bits[D3:D0], of the pointer register, 0b0101, select which DAC input register is to be read back. When the DAC register is read back, the MSB of the most significant data byte is a 1 to indicate that the result is a DAC register. The next three bits (Bits[D14:D12]) contain the DAC register address (see Table 17) and Bits[D11:D0] contain the DAC register value. Figure 39 shows an example of reading the input register of DAC2.

Table 16. DAC Pointer Byte Address

DAC Address	D7	D6	D5	D4	D3	D2	D1	D0
DAC0	0	0	0	1	0	0	0	0
DAC1	0	0	0	1	0	0	0	1
DAC2	0	0	0	1	0	0	1	0
DAC3	0	0	0	1	0	0	1	1
DAC4	0	0	0	1	0	1	0	0
DAC5	0	0	0	1	0	1	0	1
DAC6	0	0	0	1	0	1	1	0
DAC7	0	0	0	1	0	1	1	1

Table 17. DAC Data Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	DAC address			12-bit DAC data											

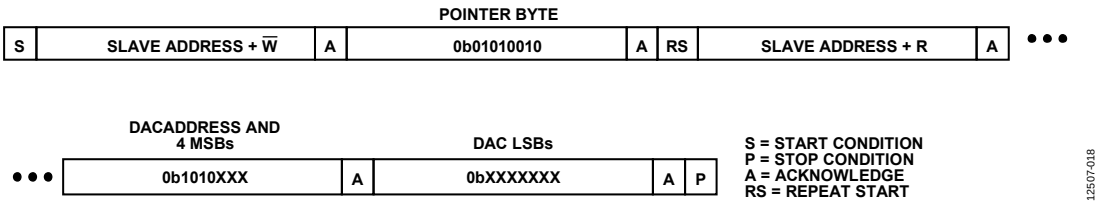

Figure 39. DAC Input Register Readback

ADC OPERATION

The ADC channels of the AD5593R operate as a traditional multichannel ADC, where each serial transfer selects the next channel for conversion. The user must write to the ADC sequence register (see Table 19) to select the input channels to be included in the conversion sequence before initiating any conversions. This is done using the I²C write sequence shown in Figure 34. When writing to the ADC sequence register, select which channels are to be converted in sequence. The user can also set the REP bit to have the ADC repeat conversions in the sequence.

When the sequence register has been written to, the ADC begins to track the first channel in the sequence. ADC data can be read from the AD5593R using any of the three read operations shown in Figure 35, Figure 36, and Figure 37, with the I²C block read (Figure 37) being the most efficient.

If more than one channel is selected in the ADC sequence register, the ADC converts all selected channels sequentially in ascending order. Conversion is started by the rising edge of SCL at the acknowledge (ACK) preceding the MSB (see Figure 37).

If the REP bit is set after all of the selected channels in the sequence register have been converted, the ADC repeats the sequence. If the REP bit is clear, the ADC clocks out the last result on subsequent I²C reads. When ADC data is clocked out by the serial interface, D15 = 0 to indicate that the result is ADC data. D14 to D12 contain a 3-bit address to indicate which ADC the data is coming from, and D11 to D0 contain the 12-bit ADC result (see Table 20).

Figure 40 shows how to configure the AD5593R to perform ADC conversions. In Step 1, I/O7 and I/O0 are configured as ADCs. Step 2 writes to the ADC configuration register, sets the REP bit, and selects ADC7 and ADC0 for inclusion in the conversion sequence. Step 3 selects the ADCs for reading and Step 4 begins reading the ADC results. The conversions are repeated until a stop condition is given by the controller.

The ADC sequence can be changed by writing the new sequence to the ADC sequence register when conversions are not taking place. When a new sequence is written, any channels remaining to be converted from the earlier sequence are ignored and the ADC starts converting the first channel of the new sequence.

To stop the ADC conversion sequence, clear the REP, TEMP, and ADC7 to ADC0 bits in the ADC sequence register to 0.

Table 18. ADC Sequence Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Reserved						REP	TEMP	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

Table 19. ADC Sequence Register Descriptions

Bits	Description
D15 to D10	Reserved; set this bit to 0
D9	REP: ADC sequence repeat 0 = sequence repetition disabled (default) 1 = sequence repetition enabled
D8	TEMP: include temperature indicator in ADC sequence 0 = disable temperature indicator readback (default) 1 = enable temperature indicator readback
D7 to D0	Setting these bits to 1 includes the appropriate ADC in the conversion sequence; by default no channels are included

Table 20. ADC Data Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	ADC address			12-bit ADC data											

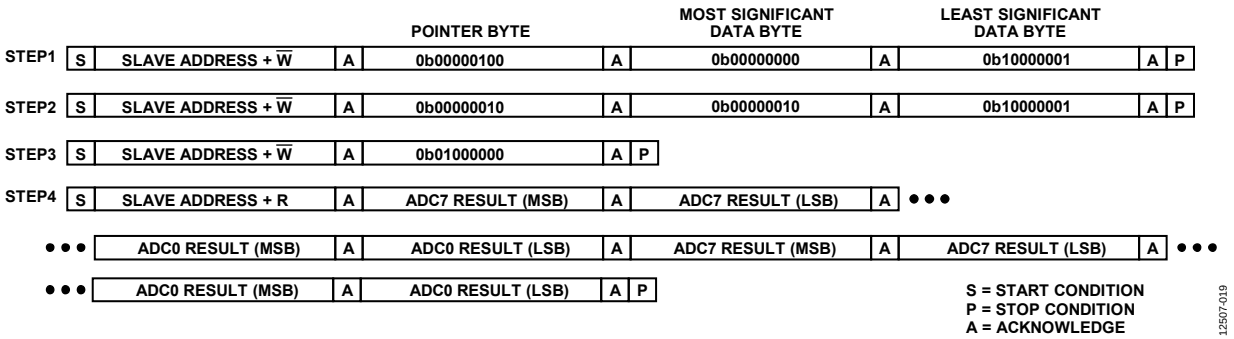

Figure 40. Configuring the ADC for Conversion

GPIO OPERATION

Each of the I/Ox pins of the AD5593R can be configured to operate as a general-purpose, digital input or output pin. The function of the pins is determined by writing to the appropriate bit in the GPIO read configuration and GPIO write configuration registers using the 4-byte I^2C write shown in Figure 34.

Setting Pins as Outputs

To set a pin as a general-purpose output, set the appropriate bit in the GPIO write configuration register to 1. For example, setting Bit D0 to 1 enables I/O0 as a general-purpose output.

The outputs can be independently configured as push/pull or open-drain outputs. When in push/pull configuration, the output is driven to V_{DD} or GND as determined by the data in the GPIO write data register. When in open-drain configuration, the output is driven to GND when a data bit in the GPIO write data register sets the pin low. When the pin is set high, the output is not driven and must be pulled high by an external resistor. This allows multiple output pins to be tied together. If all the pins are normally high, it allows one pin to pull down the others. This is commonly used where multiple pins are used to trigger an alarm or interrupt pin. The state of the output pin is controlled by setting or clearing the bits in the GPIO write data register (pointer byte = 0b00001001). A data bit is ignored if it is written to a location that is not configured as an output.

Table 21. GPIO Write Configuration Register Descriptions

Bits	Description
D15 to D8	Reserved; set these bits to 0
D7 to D0	Select pins as GPIO outputs
	D[7:0] = 1: I/O[7:0] is a general-purpose output pin
	D[7:0] = 0: I/O[7:0] function is determined by the pin configuration registers (default)

Table 22. GPIO Open-Drain Control Register Descriptions

Bits	Description
D15 to D8	Reserved; set these bits to 0
D7 to D0	Sets output pins as open-drain
	D[7:0] = 1: I/O[7:0] is an open-drain output pin
	D[7:0] = 0: I/O[7:0] is a push/pull output pin (default)

Table 23. GPIO Write Data Register Descriptions

Bits	Description
D15 to D8	Reserved; set these bits to 0
D7 to D0	Sets the state of a GPIO output
	D[7:0] = 1: I/O[7:0] is a Logic 1
	D[7:0] = 0: I/O[7:0] is a Logic 0 (default)

Setting Pins as Inputs

To set an I/Ox pin as a general-purpose input, set the appropriate bit in the GPIO read configuration register to 1. For example, setting Bit D0 to 1 enables I/O0 as a general-purpose input. To read the state of general-purpose inputs, set the pointer byte to 0b01100000 (see Table 10) using any of the read operations shown in Figure 35, Figure 36, and Figure 37. The status of any I/O pin set as a general-purpose input appears in the appropriate bit location in the least significant data byte.

Three-State Pins

The I/Ox pins can be set to three-state by writing to the three-state configuration register (pointer byte = 0b00001101) as shown in Table 24.

Table 24. Three-State Configuration Register Descriptions

Bits	Description
D15 to D8	Reserved; set these bits to 0
D7 to D0	Set pins as three-state outputs
	D[7:0] = 1: I/O[7:0] is a three-state output pin
	D[7:0] = 0: I/O[7:0] function is determined by the pin configuration registers (default)

85 kΩ Pull-Down Pins

The I/Ox pins can be connected to GND via a pull-down resistor (85 kΩ) by setting the appropriate bits in the pull-down configuration register (pointer byte = 00000110) as shown in Table 25.

Table 25. Pull-Down Configuration Register Descriptions

Bits	Description
D15 to D8	Reserved; set these bits to 0
D7 to D0	Set pins as weak pull-down outputs
	D[7:0] = 1: I/O[7:0 is connected to GND via an 85 kΩ pull-down resistor
	D[7:0] = 0: I/O[7:0] function is determined by the pin configuration registers (default)

POWER-DOWN/REFERENCE CONTROL

The AD5593R has a power-down/reference control register (pointer byte = 0b00001011) that reduces the power consumption when certain functions are not needed. The power-down register allows any channels set as DACs to be placed in a power-down state individually. When in power-down, the DAC outputs are three-stated. When a DAC channel is returned into normal mode, the DAC output returns to its previous value. The internal reference and its buffer are powered down by default and are enabled by setting the EN_REF bit in the power-down register. The internal reference voltage then appears at the V_{REF} pin.

There is no dedicated power-down function for the ADC, but the ADC is automatically powered down if none of the I/Ox pins are selected as ADCs. The ADC powers up if a read of the temperature indicator is initiated. The PD_ALL bit powers down all the DACs, the reference, its buffer, and the ADC. The PD_ALL bit also overrides the settings of Bit D9 to Bit D0. Table 26 shows the power-down register.

RESET FUNCTION

The AD5593R can be reset to its default conditions by writing 0x0DAC to the reset register (pointer byte = 0b00001111). This resets all registers to their default values and reconfigures the I/Ox pins to their default values (85 kΩ pull-down to GND). The reset function is triggered on the SCL falling edge of the eighth bit of the least significant byte (DB0 of Frame 4 in Figure 34), and the AD5593R does not generate an ACK signal for this byte of data. The reset function takes 100 µs maximum and new data must not be written to the AD5593R during this time. The AD5593R has a $\overline{\text{RESET}}$ pin that performs the same function. For normal operation, $\overline{\text{RESET}}$ is tied high. A falling edge on $\overline{\text{RESET}}$ triggers the reset function.

Table 26. Power-Down Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	PD_ALL	EN_REF	0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Table 27. LDAC Mode Register Descriptions

Bits	Bit Name	Description
D15 to D11	Reserved	Reserved; set these bits to 0
D10	PD_ALL	0 = the power-down states of the reference and DACs are determined by D9 and D7 to D0 (default). 1 = the reference, the DACs, and the ADC are powered down.
D9	EN_REF	0 = the reference and its buffer are powered down (default). Set this bit if an external reference is used. 1 = the reference and its buffer are powered up. The reference is available on the V_{REF} pin.
D7 to D0	PD7 to PD0	0 = the channel is in normal operating mode (default). 1 = the channel is powered down if it is configured as a DAC.

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5593R is via a serial bus using a standard I²C protocol. The communications channel requires a 2-wire interface consisting of a clock signal and a data signal.

AD5593R TO ADSP-BF537 INTERFACE

The I²C interface of the AD5593R is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 41 shows the AD5593R connected to the Analog Devices Blackfin® DSP. The Blackfin has an integrated I²C port that can be connected directly to the I²C pins of the AD5593R.

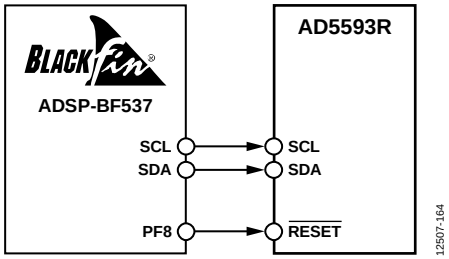

Figure 41. ADSP-BF537 Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board (PCB) on which the AD5593R is mounted must be designed so that the AD5593R lies on the analog plane.

The AD5593R must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

OUTLINE DIMENSIONS

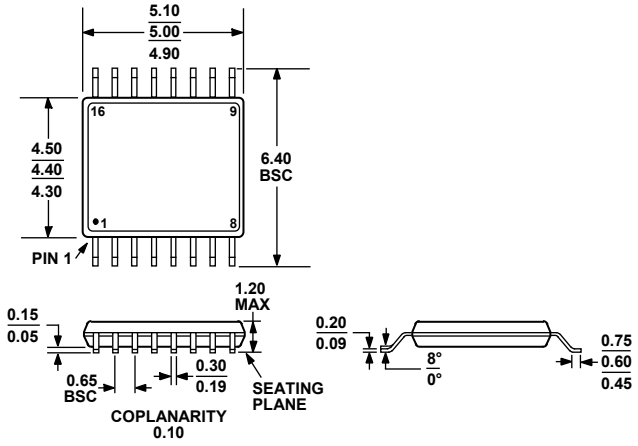

Figure 42. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

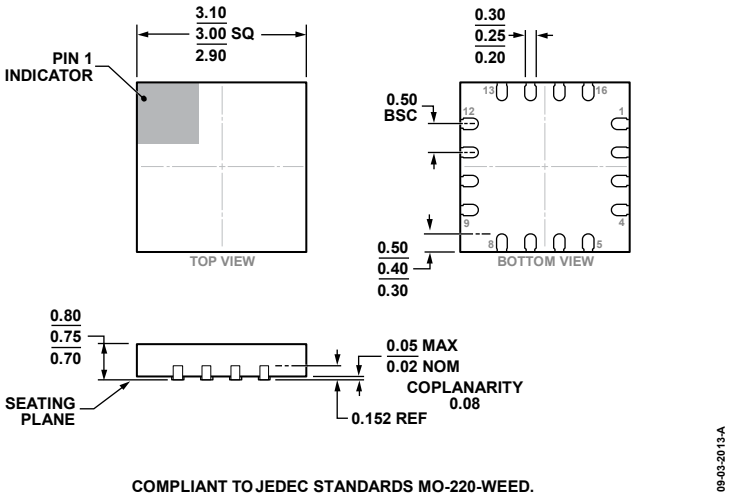

Figure 43. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-32)
Dimensions shown in millimeters

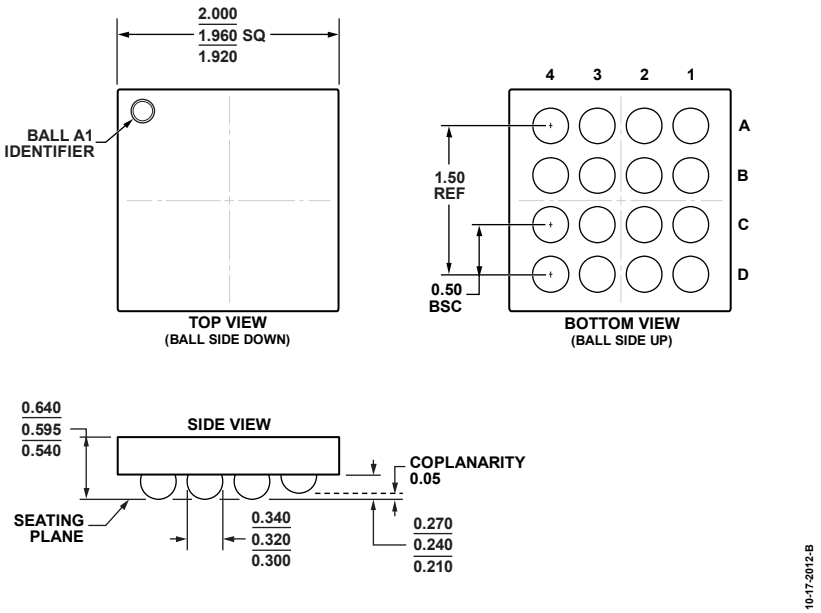

Figure 44. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD5593RBRUZ	−40°C to +105°C	16-Lead TSSOP	RU-16	
AD5593RBCPZ-RL7	−40°C to +105°C	16-Lead LFCSP	CP-16-32	DM6
AD5593RBCBZ-RL7	−40°C to +105°C	16-Ball WLCSP	CB-16-3	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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