



Ultra-Low Noise and Distortion, High Speed Op-Amp

Preliminary Technical Data

AD8099

FEATURES

Ultra-Low Noise

0.95nV/rt Hz

2.6pA/rt Hz

Ultra-Low Distortion

2nd Harmonic

-100dB @ 1MHz

-92dB @ 10MHz

3rd Harmonic

-100dB @ 1MHz

-92dB @ 10MHz

High Speed

500MHz, (G = +2)

500MHz (G=+10)

1600 V/s (G=+10)

External Compensation

Low Power 15mA I_s

Offset Voltage 1mV Max

Wide Supply Voltage Range

5V to 12V

APPLICATIONS

Pre-amp

Receiver

Instrumentation

IF and Baseband Amplifier

Filters

A-to-D Driver

DAC Buffer

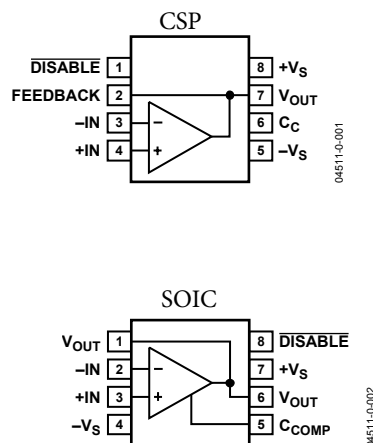
GENERAL DESCRIPTION

The AD8099 is a ultra low noise (0.95nV/vHz) and distortion (92dBc@10MHz) voltage feedback op-amp. Few op amps have noise or distortion as good as the AD8099, none have the combination making it ideal for 16 and 18 bit systems.

Incredibly, this highest performance high-speed op amp uses only 15mA of supply current and contains a disable pin that lowers the power and puts the amplifier output into high impedance. ADI's proprietary 2nd generation XFCB process enables such high performance amplifiers with relatively low power.

Featuring external compensation the AD8099 allows the user to chose the gain bandwidth product that best suites the application. The AD8099 is externally compensated enabling gains from +2 to +10 with minimal trade-off in bandwidth. The AD8099 also features extremely high slew rate of 1600V/us giving the designer the flexibility to use the entire dynamic range without trading off bandwidth and distortion. The AD8099 is a very well behaved amp that settles to 0.002% in

CONNECTION DIAGRAMS



35ns and has fast overload recovery of 50ns.

The AD8099 amplifier offers low power of 15 mA, and is capable of driving 100ohm loads at break through performance levels. With the wide supply voltage range (5V to 12V), low offset voltage (1mV max), wide bandwidth (500MHz for low gains) and a GBWP up to 3GHz; the AD8099 is designed to work in a wide variety of applications.

The AD8099 amplifier is available in tiny lead frame chip-scale packaging (LFCSP) with new standard pin out that is specifically optimized for high performance high-speed amplifiers. The new package and pin out enables the breakthrough performance that previously was not achievable with amplifiers.

The AD8099 is also offered in the industry standard package (8-lead SOIC) with the industry standard pin out. The AD8099 is rated to work over the extended industrial temperature range, -40C to +125C

Rev. A

9/25/03

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REVISION HISTORY

SPECIFICATIONS

SPECIFICATIONS WITH ± 5 V SUPPLYTable 1. $V_S = \pm 5$ V @ $T_A = 25^\circ\text{C}$, $G = +2$, $C_C = 6.8\text{pF}$, $C_L = 5\text{pF}$, $R_L = 100\Omega$ to ground, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$G = +2$, $V_o = 0.2\text{Vp-p}$		500		MHz
	$G = +2$, $V_o = 2\text{Vp-p}$		70		MHz
	$G = +10$, $V_o = 0.2\text{Vp-p}$		500		MHz
	$G = +10$, $V_o = 2\text{Vp-p}$		70		MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_o = 0.2$ V p-p		150		MHz
Slew Rate	$G = +2$, $V_o = 2$ V Step		500		V/ μs
Settling Time to 0.1%	$G = +2$, $V_o = 2$ V Step		12		ns
Overload recovery Input/Output			50/20		ns
NOISE/DISTORTION PERFORMANCE					
2 nd /3 rd harmonic)	$f_c = 1$ MHz, $V_o = 2$ V p-p		-100/100		dBc
2 nd /3 rd harmonic	$f_c = 10$ MHz, $V_o = 2$ V p-p		-85/87		dBc
2 nd /3 rd harmonic)	$f_c = 1$ MHz, $V_o = 2$ V p-p $R_L = 500\Omega$		-100/100		dBc
2 nd /3 rd harmonic	$f_c = 10$ MHz, $V_o = 2$ V p-p $R_L = 500\Omega$		-92/92		dBc
Input Voltage Noise	$f = 100$ kHz		1		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100$ kHz		2.6		pA/ $\sqrt{\text{Hz}}$
Differential Gain Error	NTSC, $G = +2$, $R_L = 150\Omega$		0.01		%
Differential Phase Error	NTSC, $G = +2$, $R_L = 150\Omega$		0.01		Degree
DC PERFORMANCE					
Input Offset Voltage			0.2	1	mV
	$T_{\min} - T_{\max}$			1.5	mV
Input Offset Voltage Drift	T_{\min} to T_{\max}		3		$\mu\text{V}/^\circ\text{C}$
Input Bias Current ¹			3		μA
	T_{\min} to T_{\max}		8		μA
Input Offset Current					μA
Open-Loop Gain	$V_o = \pm 2.5$		86		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1/1.8		M Ω /pF
Differential Input Impedance			4/2.0		M Ω /pF
Input Common-Mode Voltage Range			-3.6 to 3.6		V
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5$		90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	$R_L = 500\Omega$		-3.5 to 3.5		V
Short-Circuit Current	$V_o = \pm 3.0$ V		100		mA
Capacitive Load Drive	30% Overshoot		35		pF
POWER SUPPLY					
Operating Range		5		12	V
Quiescent Current/Amplifier		12	15	18	mA
Power Supply Rejection Ratio	$V_S \pm 1$ V		-80		dB

¹ Plus (or no sign) indicates current into pin; minus indicates current out of pin.

SPECIFICATIONS WITH +5 V SUPPLY

Table 2. $V_S = +5\text{ V}$ @ $T_A = 25^\circ\text{C}$, $G = +2$, $C_C = 6.8\text{pF}$, $C_L = 5\text{pF}$, $R_L = 100\Omega$ to ground, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$G = +2$, $V_o = 0.2\text{Vp-p}$		500		MHz
	$G = +2$, $V_o = 2\text{Vp-p}$		70		MHz
	$G = +10$, $V_o = 0.2\text{Vp-p}$		500		MHz
	$G = +10$, $V_o = 2\text{Vp-p}$		70		MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_o = 0.2\text{ V p-p}$		150		MHz
Slew Rate	$G = +2$, $V_o = 2\text{ V Step}$		500		V/ μs
Settling Time to 0.1%	$G = +2$, $V_o = 2\text{ V Step}$		12		ns
Overload recovery Input/Output			50/20		ns
NOISE/DISTORTION PERFORMANCE					
2 nd /3 rd harmonic)	$f_c = 1\text{ MHz}$, $V_o = 2\text{ V p-p}$		-100/100		dBc
2 nd /3 rd harmonic	$f_c = 10\text{ MHz}$, $V_o = 2\text{ V p-p}$		-85/87		dBc
2 nd /3 rd harmonic)	$f_c = 1\text{ MHz}$, $V_o = 2\text{ V p-p}$ $R_L = 500\Omega$		-100/100		dBc
2 nd /3 rd harmonic	$f_c = 10\text{ MHz}$, $V_o = 2\text{ V p-p}$ $R_L = 500\Omega$		-92/92		dBc
Input Voltage Noise	$f = 100\text{ kHz}$		1		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		2.6		pA/ $\sqrt{\text{Hz}}$
Differential Gain Error	NTSC, $G = +2$, $R_L = 150\Omega$		0.01		%
Differential Phase Error	NTSC, $G = +2$, $R_L = 150\Omega$		0.01		Degree
DC PERFORMANCE					
Input Offset Voltage			0.2	1	mV
Input Offset Voltage Drift	$T_{\min} - T_{\max}$			1.5	mV
	T_{\min} to T_{\max}		3		$\mu\text{V}/^\circ\text{C}$
Input Bias Current ¹			3		μA
	T_{\min} to T_{\max}		8		μA
Input Offset Current					μA
Open-Loop Gain	$V_o = \pm 2.5$		86		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1/1.8		M Ω /pF
Differential Input Impedance			4/2.0		M Ω /pF
Input Common-Mode Voltage Range			-3.6 to 3.6		V
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5$		90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	$R_L = 500\Omega$		-3.5 to 3.5		V
Short-Circuit Current	$V_o = \pm 3.0\text{ V}$		100		mA
Capacitive Load Drive	30% Overshoot		35		pF
POWER SUPPLY					
Operating Range		5		12	V
Quiescent Current/Amplifier		12	15	18	mA
Power Supply Rejection Ratio	$V_S \pm 1\text{ V}$		-80		dB

¹ Plus (or no sign) indicates current into pin; minus indicates current out of pin.

TYPICAL PERFORMANCE CHARACTERISTICS

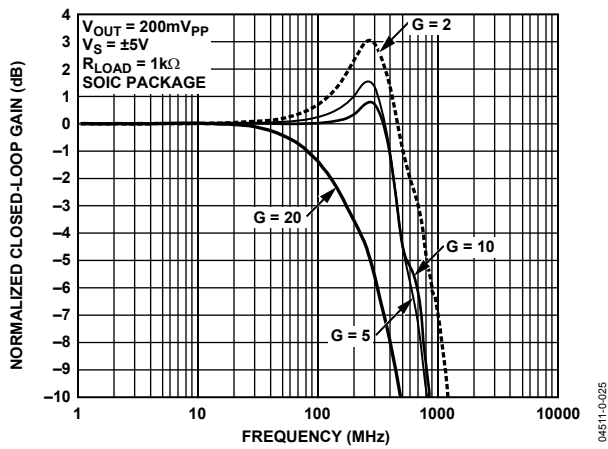


Figure 2. Small Signal Gains vs. Frequency (SOIC)

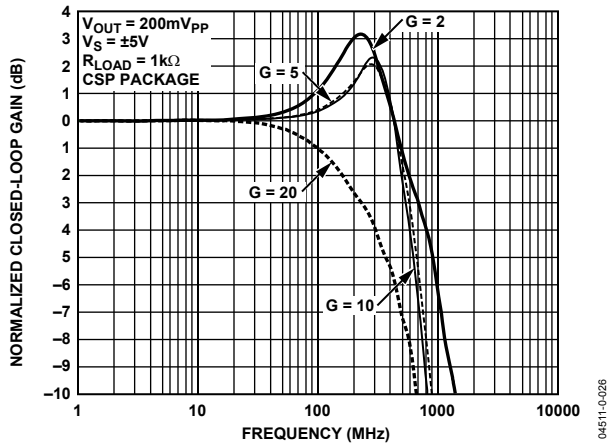


Figure 3. Small Signal Gains vs. Frequency (CSP)

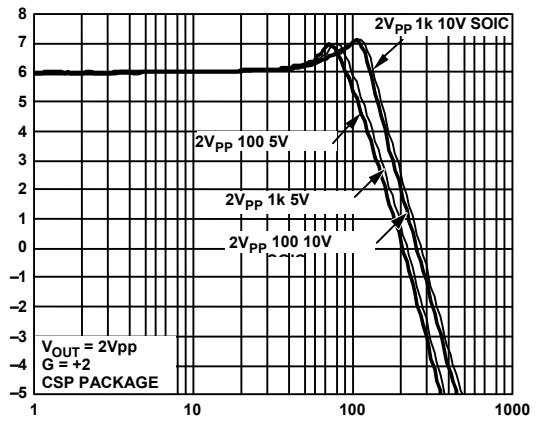


Figure 5. Large Signal Gain vs. Various Loads and Supplies CSP

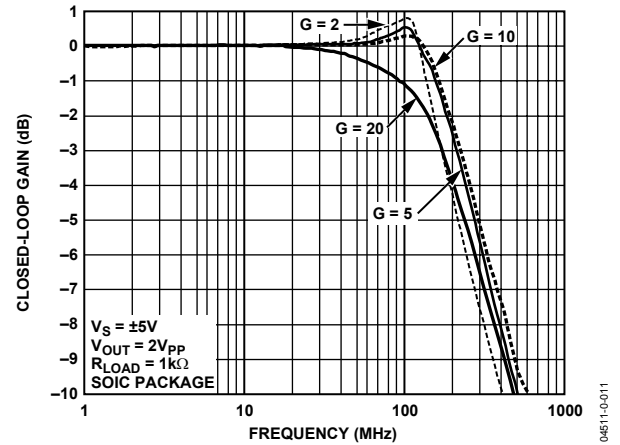


Figure 6. Various Large Signal Gains vs. Frequency SOIC

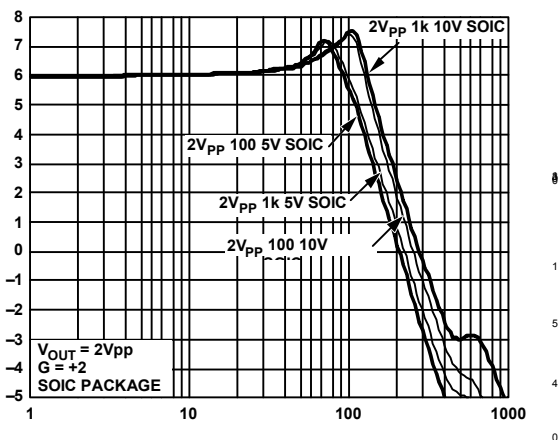


Figure 4. Large Signal Gain vs. Various Loads and Supplies SOIC

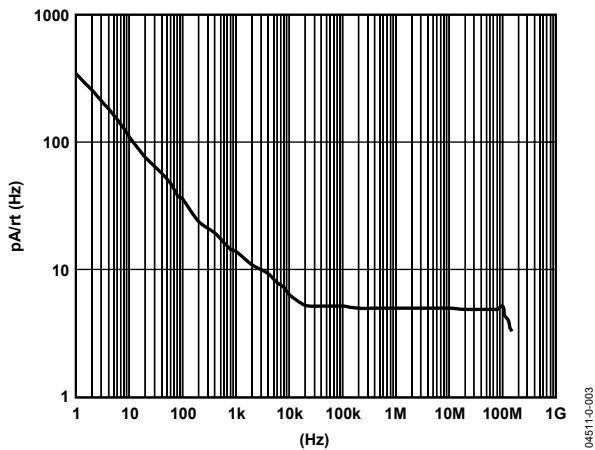


Figure 7. Input Current Noise vs. Frequency Disable Pin=+Vs

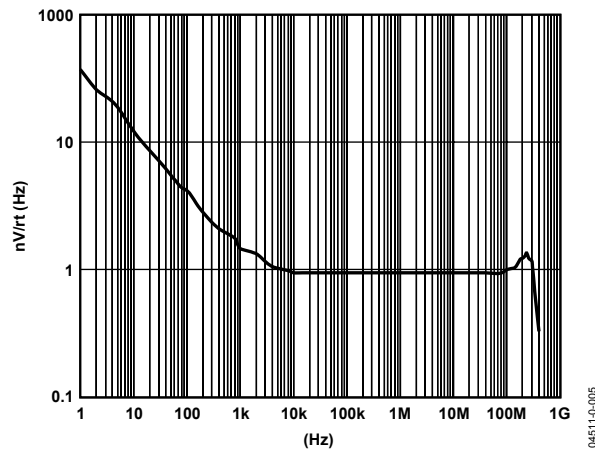


Figure 10. Voltage Noise vs. Frequency

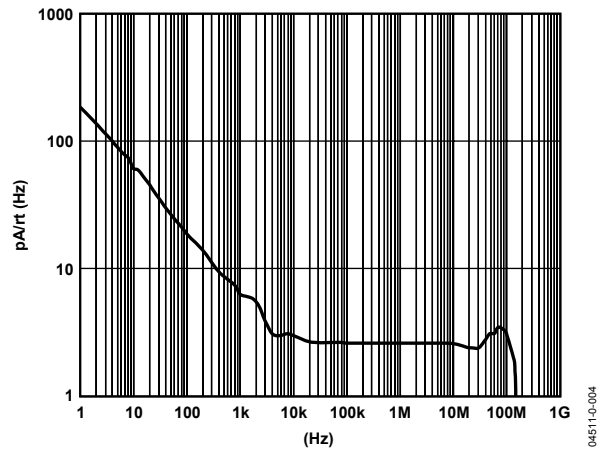


Figure 8. Input Current Noise vs. Frequency, Disable Pin = Open

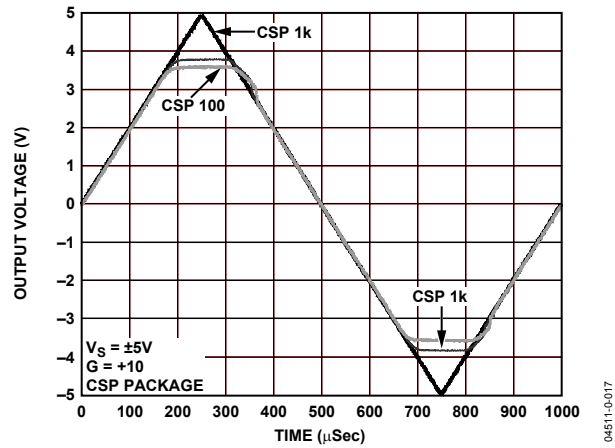


Figure 11. Output Overdrive (CSP)

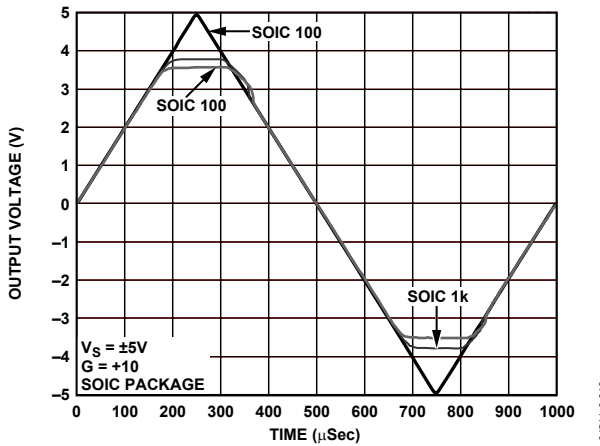


Figure 9. Output Overdrive (SOIC)

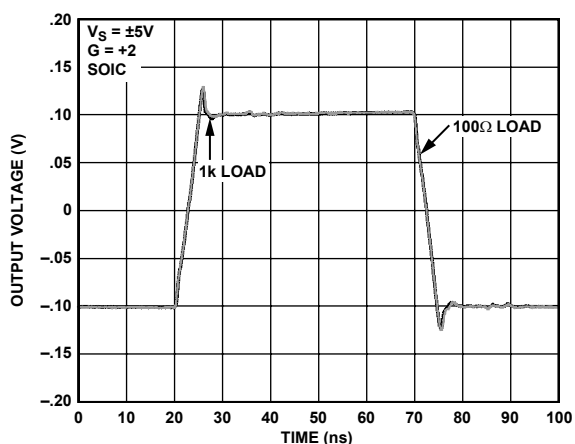


Figure 12 Small Signal Pulse Response vs. Rload

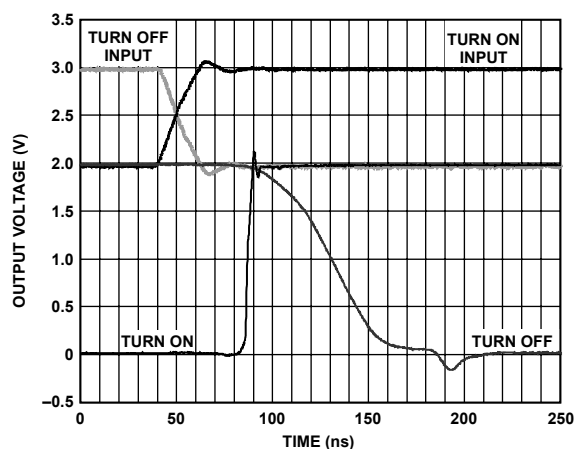


Figure 15. Switching Speed

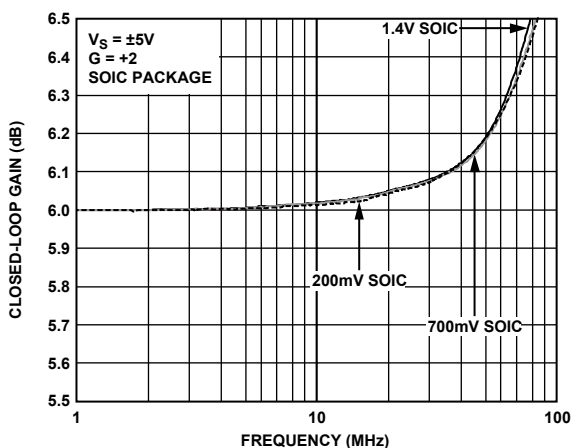


Figure 23. . 0.1dB Flatness (SOIC)

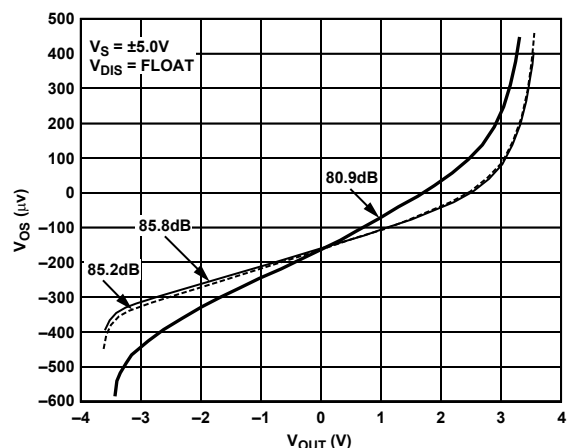


Figure 16. Input Offset Voltage vs. Output Voltage vs. Open Loop Gain

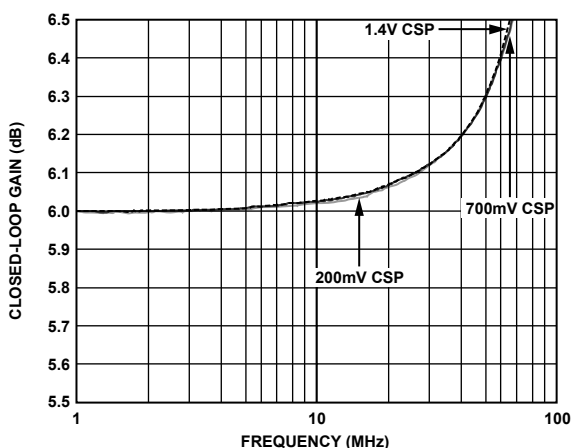


Figure 14. 0.1dB Flatness (CSP)

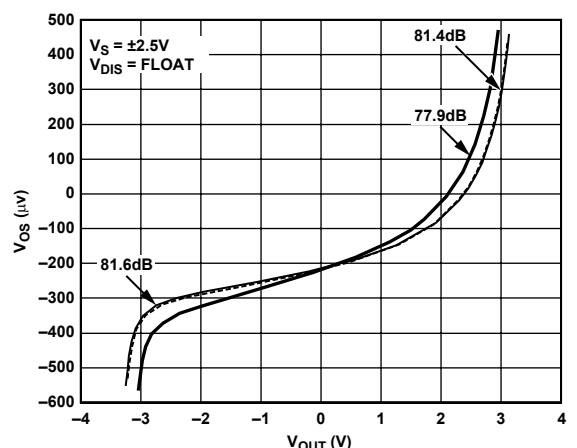


Figure 17 Input Offset Voltage vs. Output Voltage vs. Open Loop Gain

DESIGN TOOLS AND TECHNICAL SUPPORT

Analog Devices is committed to its customers by providing technical support and online design tools. ADI offers technical

support through free evaluation boards, sample ICs, spice models, interactive evaluation tools, application notes, and phone and email support—all available at www.analog.com

OUTLINE DIMENSIONS

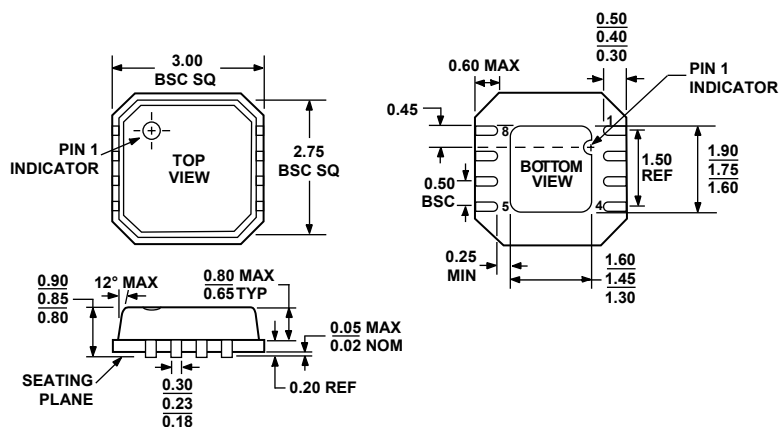
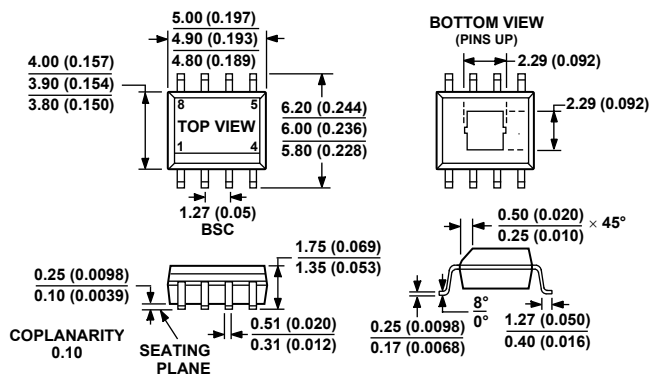


Figure 3.



COMPLIANT TO JEDEC STANDARDS MS-012

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 4.

ORDERING GUIDE

Model	Minimum Ordering Quantity	Temperature Range	Package Description	Package Option
AD8099AR*	1	–40°C to +125°C	8-Lead SOIC	R-8
AD8099AR-REEL*	2,500	–40°C to +125°C	8-Lead SOIC	R-8
AD8099AR-REEL7*	1,000	–40°C to +125°C	8-Lead SOIC	R-8
AD8099CP-R2	250	–40°C to +125°C	8-Lead CSP	CP-8
AD8099CP-REEL	5,000	–40°C to +125°C	8-Lead CSP	CP-8
AD8099CP-REEL7	1,500	–40°C to +125°C	8-Lead CSP	CP-8

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

