ANALOG DEVICES

AN-215A
APPLICATION NOTE

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Designer's Guide to Flash-ADC Testing

Part 1
Flash ADCs Provide the Basis for High Speed Conversion

by Walt Kester

Building high-performance circuits that take advantage of the high sampling rates of flash ADCs requires a knowledge of these converters' many intricacies. Part 1 of this 3-part series discusses the pitfalls of designing with flash ADCs, how to evaluate certain data-sheet specifications, and how to choose external components that complement your particular converter. Parts 2 and 3 will explore test and measurement methods that you can use to verify a converter's performance in your system.

To digitize analog signals whose bandwidths exceed 1 MHz, you'll probably need flash ADCs. Many flash converters with 4 to 10 bits of resolution are now available, thanks to recent advances in VLSI process technology and design techniques. However, to use these converters successfully at the high sampling rates that they provide, you must take into account and compensate for a variety of flash-converter characteristics.

The basic features of most flash converters are shown in Fig 1. A flash ADC simultaneously applies an analog-input signal to $2^N - 1$ latched comparators, where N is the number of the converter's output bits. A resistive voltage divider generates each comparator's reference voltage and sets each reference level 1 LSB higher than the level of the comparator immediately below it. Comparators that have a reference voltage below the input-signal level will assume a logic 1. The comparators with a reference voltage above the level of the input signal will produce a logic 0. A secondary logic stage decodes the thermometer code that results from the $2^N - 1$ comparisons. An optional output register latches the decoding stage's digital output for one clock cycle.

Timing is everything

One of the first difficulties you'll encounter when using flash converters is removing valid data from the converter. In practice, the comparator bank has two states controlled by a conversion-command signal. Various converters call this command the convert, the encode, or simply the clock command. When this signal is in its convert-command state, the comparators track the analog-input signal, and during this time the output data is invalid. When the command line changes state, it latches the comparator outputs. Valid output data is now available for transfer to an external register. You'll find most flash converters somewhat sensitive to the duty cycle and frequency of this command pulse. In other words, the performance of the converter, specifically its differential and integral nonlinearity performance, is related to the clock's duty cycle and frequency. Performance degradation is especially pronounced when you run the device at or near its maximum sampling rate.

Reprinted from EDN – January 4, 1990

Because of recent advances in VLSI processing and design techniques, many flash converters that have from 4 to 10 bits of resolution are available.

The way you handle the binary output depends on whether the converter has an internal output latch. Without a latch, the data will be invalid for a period equal to the sampling clock's pulse width. At high sample rates, the data-invalid time will impinge on the data-valid time, making it difficult for you to strobe the flash converter's output into an external register. For instance, if you operate a flash converter at 100M samples/sec with a 50%-duty-cycle sampling clock, the output data will be valid for only 5 nsec. When you consider the finite rise and fall time of the output binary bits, this short time doesn't leave you much leeway, even if you use the fastest external logic. In fact, you may ultimately lose data. The addition of an internal output latch simplifies clocking of the output data, because the output data is valid for approximately the entire clock cycle. In return for a longer data-valid time, you'll have to accept an inherent 1-cycle or more pipeline delay—an acceptable compromise in most systems applications.

Try to place an appropriate buffer register next to the flash converter. If you route the converter's digital output directly to a backplane data bus through a card-edge connector, signal coupling between the digital-output signals and analog input will degrade the S/N ratio and harmonic performance.

In many high-speed data-acquisition designs, you'll need a large and fast buffer memory to store the output data. A 500M-sample/sec converter can fill 1M byte of memory in 2 msec. To reduce the required speed—and thus the cost—of the memory, you can demultiplex the high-speed data stream (**Fig 2**), which slows it to frequencies compatible with cost-efficient CMOS RAMs. **Fig 2**'s circuit clocks the two output registers at half the sample rate, and it latches data in each register 180x out of phase from the other. Some flash converters that operate in excess of 200 MHz have onboard demultiplexing for added convenience.

All that sparkles isn't gold

So far, these timing difficulties refer to how you deal with the converter's output data. But flash converters can have internal problems as well. Low input frequencies can cause comparator metastability, and

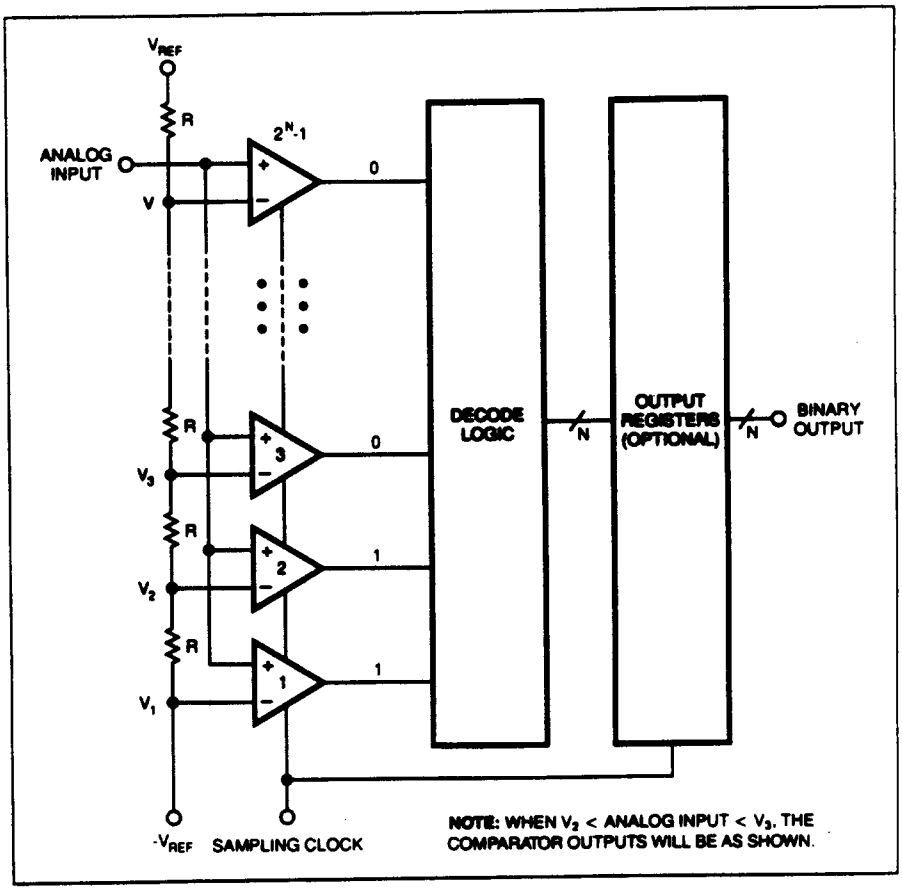


***Fig 1—Flash converters contain a bank** of 2^N-1 comparators, where N is the number of output bits. Decoding logic transforms the comparator outputs into the appropriate N-bit result. Timing and input characteristics of the converter, such as mismatched comparator delays, mismatched ladder resistors, and nonlinear input capacitances, are just a few sources of converter errors.*

high input frequencies can lead to errors caused by slew-rate and delay mismatches. All of these errors may manifest themselves as sparkle codes in a poorly designed flash converter.

Sparkle codes are random errors whose magnitude may approach the full-scale range of the converter. The term refers to the white dots or "sparkles" that appear against a gray background when the ADC output drives a video display. There are two sources of sparkle codes: comparator metastable states and thermometer-code bubbles.

A comparator metastable state occurs if the comparator output falls between the logic-0 and logic-1 threshold of the digital decoding logic. If the threshold uncertainty region has a width of ΔV_L and the comparator has a gain of A, then the error probability P_m is a uniformly distributed value that's equal to

$$P_m = \frac{\Delta V_L}{Aq},$$

where q is the weight of the LSB.

A latched comparator in a flash converter has a regenerative gain of

$$A = A_0 e^{t/\tau}$$

when t>0, and

$$A = A_0$$

when t≤0. τ equals the regeneration-time constant, and t is the time after the application of a latch command. The probability of a metastable state, P_m, for a regenerative comparator bank driving decoding logic is

$$P_m = \frac{\Delta V_L}{A_0 q} e^{-t/\tau}.$$

The magnitude of the sparkle code depends on the location of the metastable comparator in the comparator bank and on the logic-decoding scheme. For instance, the 128th comparator determines the MSB of an 8-bit flash converter with straight binary decoding logic. If this comparator's output is in a metastable state, the decoding logic may mistakenly convert the input voltage whose correct binary representation is 01111111 to 11111111, producing a full-scale error. If the comparator bank's thermometer-code output is first decoded into Gray code, latched, and then converted into binary code, the metastable error is reduced to 1 LSB, regardless of the comparator in error. Flash converters, however, rarely use this scheme because of the ripple-through time and the increased logic density of the Gray-to-binary circuitry. Instead, converter designers often use "pseudo-Gray" decoding techniques to eliminate the delay time associated with traditional Gray-to-binary circuits.

Note that the probability of a metastable-state error increases as the time-after-latch, t, decreases (assum-

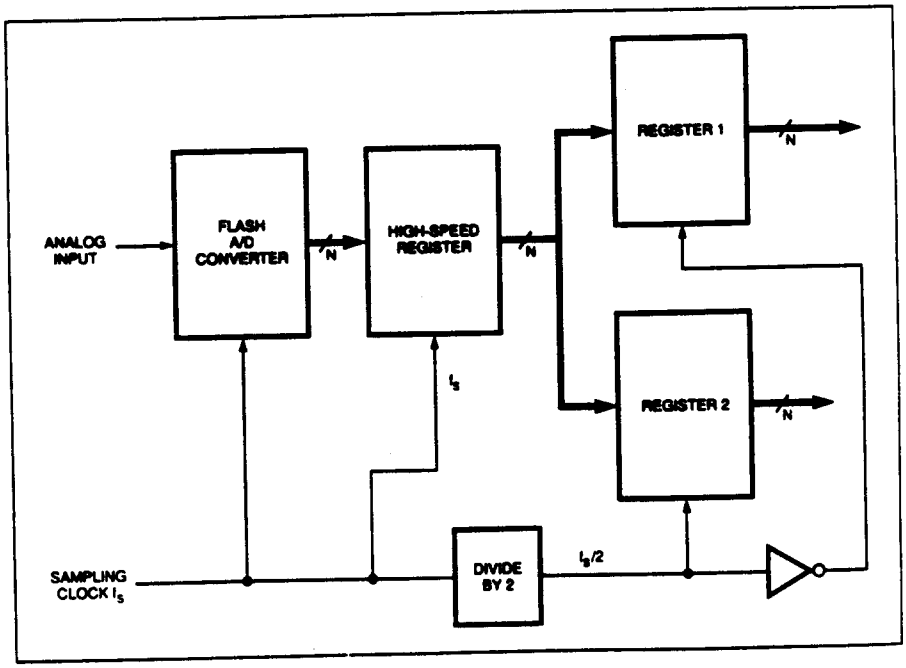
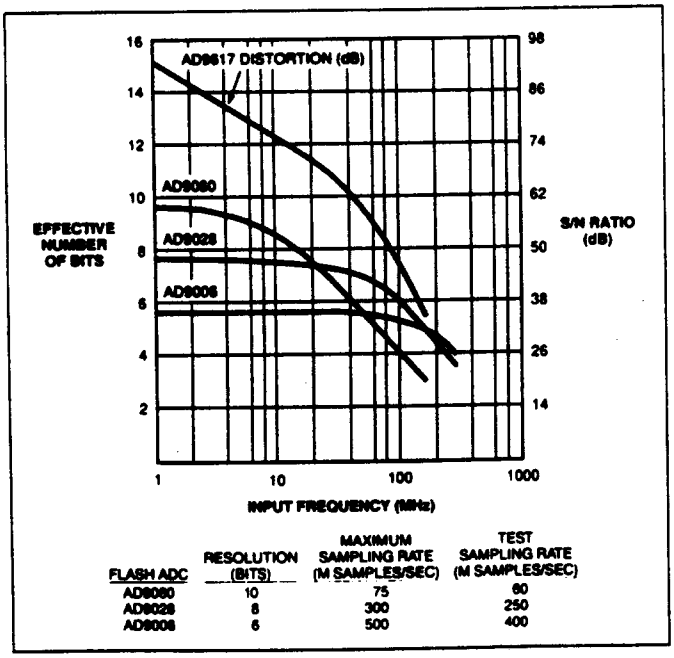


***Fig 2—Flash converters can operate** at extremely high sample rates. Thus, you must have an output register that can handle this fast data. By demultiplexing the converter's outputs, you can slow the data to a rate that's compatible with standard CMOS memory.*

One of the first difficulties you'll encounter when using flash converters is removing valid data from the converter.

ing a constant value of τ). This implies that the flash converter is more apt to produce metastable-state errors as you increase the sampling rate, because t must decrease correspondingly. Most manufacturers reduce metastable comparator states by minimizing the regeneration-time constant, τ. Lower regeneration-time constants result in higher power dissipation, which is one reason why many high-speed flash converters are power-hungry devices.

Thermometer-code bubbles are another potential source of sparkle codes. A well-behaved flash converter's comparator bank produces a specific sequence of ones up to a certain point in the input range of the converter, and it produces a sequence of zeros beyond that point. The decoding logic then assigns a binary number to the thermometer code. For low-frequency inputs, most flash converters' comparator banks are well behaved. At high speeds, however, delay mismatches among comparators may produce out-of-sequence ones and zeros in the thermometer code. The decoding logic then assigns an error binary code to these out-of-sequence points, or bubbles, which also result in sparkle codes. Again, proper comparator design and more sophisticated decoding-logic circuitry within the ADC itself can reduce these errors to acceptable levels.



FLASH ADC	RESOLUTION (BITS)	MAXIMUM SAMPLING RATE (M SAMPLES/SEC)	TEST SAMPLING RATE (M SAMPLES/SEC)
AD9060	10	75	60
AD9028	8	300	250
AD9006	6	500	400

Fig 3—Theoretically, a flash converter should maintain its performance across the full Nyquist bandwidth. But as the curves in this figure illustrate, the S/N ratio starts to degrade well below each device's maximum sampling rate. (Note that these curves are based on test sampling rates that are somewhat lower than each device's maximum possible rate.)

These comparator-timing errors degrade both the differential and integral linearity of a flash ADC as the input slew rate increases. In addition to static errors, such as missing codes and sparkle-code errors, slew-rate limitations manifest themselves as dynamic errors, such as increased harmonic distortion and degradation in the S/N ratio. Ideally, a flash converter should maintain its static performance specifications across the full Nyquist bandwidth, and certain applications demand full performance beyond the Nyquist bandwidth. The theoretical, rms S/N ratio for an N-bit ADC is given by the well-known equation

$$\text{S/N ratio} = 6.02N + 1.76 \text{ dB}.$$

However, as shown in a typical plot of S/N ratio versus input frequency for actual flash converters (**Fig 3**), the S/N ratio degrades as the input frequency increases. This degradation starts well below these converters' maximum sampling rates. The left vertical axis of **Fig 3** shows the S/N ratio in another term: effective number of bits. The effective number of bits is simply the value of N when you solve the above equation using a specific value for the S/N ratio. Aperture jitter (sample-to-sample variations in the effective-sampling instant) can also cause degradation in the overall S/N ratio for high-slew-rate inputs. Jitter can be internal or external to the converter. Part 3 of this series will cover this topic in more detail. To minimize externally produced jitter components, you should always practice proper grounding, power-supply-decoupling, and pc-board-layout techniques.

Watch for dangerous data-sheet territory

Most of the timing difficulties and error sources discussed so far are common to all flash converters. However, each converter features its own unique design and specifications; thus the data sheets require scrutiny. Don't be fooled into believing that sampling rate and input bandwidth are interchangeable; they're different specifications. It wasn't until recently that you'd even find input bandwidth specified for an ADC. Even now, no accepted industry-wide definition exists for a flash converter's full-power-bandwidth specification. Scrutinize the data sheet carefully and make sure you understand the manufacturer's definition and test method. The full-power bandwidth of a traditional op amp is the maximum frequency at which the amplifier

can produce the specified p-p output voltage at a specified level of distortion. Another commonly used definition calculates the full-power bandwidth by dividing the amplifier's slew rate by $2\pi V_O$, where the output-voltage range of the amplifier is $\pm V_O$.

When you apply traditional analog-bandwidth definitions to flash converters, the results can be misleading. The dynamic-error sources previously discussed may become predominant long before the comparator front end approaches its maximum bandwidth. If you use a common definition of full-power bandwidth as the frequency at which the p-p reconstructed-sine-wave output is reduced by 3 dB for a full-scale input, then the effective number of bits (S/N ratio) at this input frequency may render the flash converter useless in your system. Thus, to get a true idea of a converter's performance, you must consider both the full-power bandwidth and the effective number of bits (S/N ratio) at a specific sampling rate.

Another definition you'll encounter occasionally for full-power bandwidth is the maximum, full-scale input signal at a specified sampling rate that produces no missing codes. Using this definition always gives the most pessimistic number, so specifications based on this definition appear on only a few data sheets. The following is a recently proposed definition for full-power bandwidth (courtesy Chris Manglesdorf, a senior scientist at Analog Devices): the frequency at which the fundamental component of the reconstructed FFT output—excluding harmonics—is reduced by 3 dB from full scale.

Just when you think you've mastered the intricacies of flash ADCs, you'll realize that you have another component to worry about: the input buffer amplifier. Fortunately (or unfortunately depending upon your perspective), the flash converter—not the amplifier—usually limits the converter's dynamic performance. A flash converter typically digitizes a signal from a 50, 75, or 93Ω bipolar or unipolar source. If the input range of the flash converter is incompatible with the signal, then you'll clearly need a wideband op amp to generate the required gain and offset (**Fig 4**). In addition, the input capacitance of some flash converters may vary as a function of the analog input's signal amplitude. Therefore, so that the nonlinear capacitance doesn't produce undesirable harmonics in the digitized signal, you'll need to use a buffer amplifier for isolation. For certain flash converters, the input capacitance is so high that a buffer amplifier is needed just to preserve the signal bandwidth.

A good choice for the buffer is a high-speed transimpedance amplifier. These amplifiers have high bandwidths and flat frequency responses over a broad range of input frequencies. Also, many transimpedance amplifiers exhibit extremely low distortion. Pairing the right amplifier with your converter is important. For instance, **Fig 3** shows the S/N ratio of various converters plotted along with the harmonic distortion of the AD9617. Since the THD of the amplifier is better than the S/N ratio of the converters, the amplifier won't degrade the flash converters' performance over the major portion of their usable bandwidth.

Another factor to consider when driving the input of flash converters is the input-signal polarity. Positive input signals, which forward bias the substrate diode, can damage a converter that has a unipolar, negative input-voltage range. Installing an external Schottky diode provides effective protection.

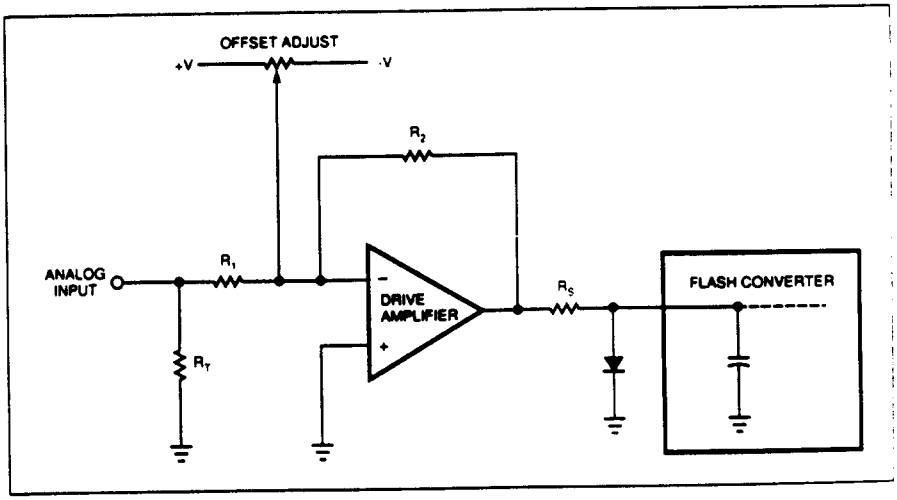


Fig 4—If the voltage range of the analog signal and the input range of the ADC aren't compatible, you'll have to adjust the gain using R_1 and R_2 and also adjust the input signal's offset. Because of the substantial value and the often nonlinear nature of a flash converter's input capacitance, you must choose an appropriate drive amplifier and value for R_S.

Ideally, a flash converter should maintain its static-performance specifications across the full Nyquist bandwidth, but in reality ADCs fall far short of this ideal.

The flash converter's input capacitance and the drive amplifier's isolation resistor, R_S, form a lowpass filter. Typical series-resistor and input-capacitance values of 10Ω and 20 pF create a single-pole lowpass filter that has a bandwidth of 800 MHz. However, if the input capacitance changes from 20 to 15 pF over the input range of the converter, then an attenuation error of 1.4% occurs for a 50-MHz input signal. This 1.4% nonlinearity will produce 37 dBc of harmonics. (The unit dBc refers to the number of dB between the signal you're measuring and the carrier frequency). If you minimize the value of R_S and still maintain op-amp stability, you can reduce the attenuation error caused by these lowpass filtering effects. The signal dependence of input capacitance is rarely specified, but as converters move toward higher bandwidths, you can expect to see this parameter on more data sheets.

Few, if any, flash converters contain an internal voltage reference, so in addition to an external drive amplifier, you must also design your own voltage-reference generator. **Fig 5** illustrates a typical −2V, unipolar reference-voltage circuit for a flash converter. A buffer transistor is necessary because the resistance of the converter's ladder string is usually fairly low. The total reference-ladder resistance of a flash converter depends heavily on the fabrication process and may vary considerably from device to device. Also, the ladder's resistance may exhibit a large temperature coefficient.

If the flash converter allows bipolar operation, then you'll have to generate two reference voltages. The circuit in **Fig 6** allows great flexibility in setting both the gain and the offset of a bipolar flash converter, and it operates on ±5V power supplies. A few flash converters provide a sense pin for the voltage reference. You can use this pin to compensate for the voltage drop caused by the package's pin and bond-wire resistances, as shown in the bipolar-reference circuit in **Fig 6**. In addition, some ADCs give you access to one or more taps along the internal, reference-ladder resistor string. To achieve better integral linearity, you can drive these taps from low-impedance sources.

Improve dynamics with T/H amplifiers

As previously discussed, the effective-sample time-delay variations among the latched comparators degrade the S/N ratio and the harmonic performance. You can visualize the individual comparators within an array as having variable delay lines in series with their latch-strobe inputs. To understand the effect of this delay on performance, consider an 8-bit, 100M-sample/sec flash converter that's digitizing a full-scale, 50-MHz sine-wave input. You can express the sine wave as

$$v(t)=V_p\sin 2\pi ft.$$

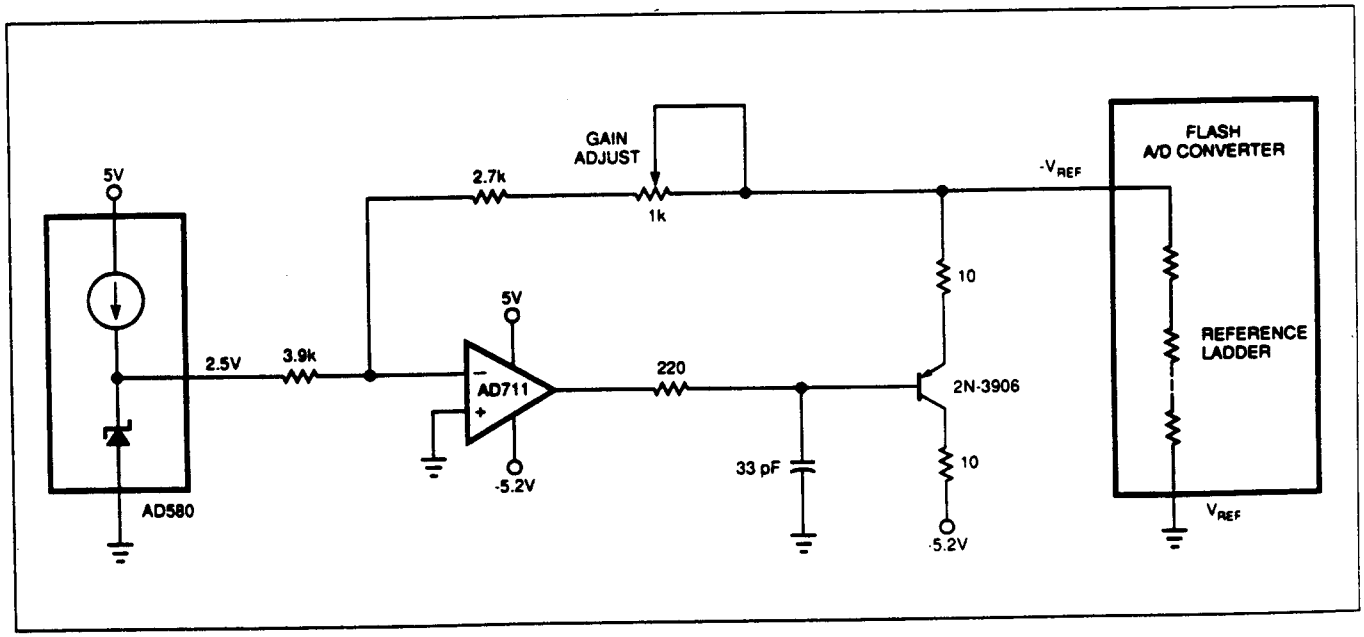


Fig 5—Flash converters don't have internal references, so you must design them externally. This particular circuit provides a stable −2V reference for a unipolar converter.

To improve flash-converter performance at sampling rates as high as 25 MHz, you can use front-end T/H amplifiers to implement a "track-and-slow-down" approach.

The maximum rate-of-change of this signal occurs at the zero-crossing point and is equal to

$$\left.\frac{dv}{dt}\right|_{max} = 2\pi f V_P = \left.\frac{\Delta v}{\Delta t}\right|_{max}.$$

By solving this equation for Δt_{max}, you obtain

$$\Delta t_{max} = \frac{\Delta V}{2\pi f V_P}.$$

If the input-voltage range of the flash converter is 2V, or $V_P = 1V$, then the LSB weight is 8 mV for an 8-bit ADC. For the flash converter's error to be less than 1 LSB, Δt_{max} must equal 25 psec. The effective-sample delay mismatch between comparators can't exceed this value. If the mismatch is greater, a 50-MHz, full-scale sine-wave input will produce missing codes in the converter's output.

Placing an ideal track-and-hold (T/H) amplifier ahead of the flash converter theoretically would eliminate this problem, because the flash converter basically would be digitizing a dc input. In actual practice, T/H amplifiers aren't ideal, especially at high speeds. The signal presented to the flash converter is still changing, although at a slower rate. Nevertheless, this "track-and-slow-down" approach can improve the flash-converter performance at sampling rates as high as approximately 25 MHz. At sampling rates above 25 MHz, the T/H circuit needs to be mounted on the same substrate as the flash converter in a suitable hybrid package. Monolithic T/H amplifiers in hybrid packages with 8-bit flash converters have successfully achieved 7 effective bits at Nyquist inputs and at sampling rates of 250 MHz. These hybrid packages exact a penalty of higher cost and power consumption, however.

You'll find it difficult to select an appropriate discrete T/H amplifier, because the interaction between the T/H amplifier and the flash ADC is hard to predict. You should evaluate key T/H amplifier specifications such as acquisition time, full-power bandwidth, slew rate, and harmonic distortion. Harmonic-distortion specifications typically are provided for the track mode. The T/H amplifier's performance may be considerably

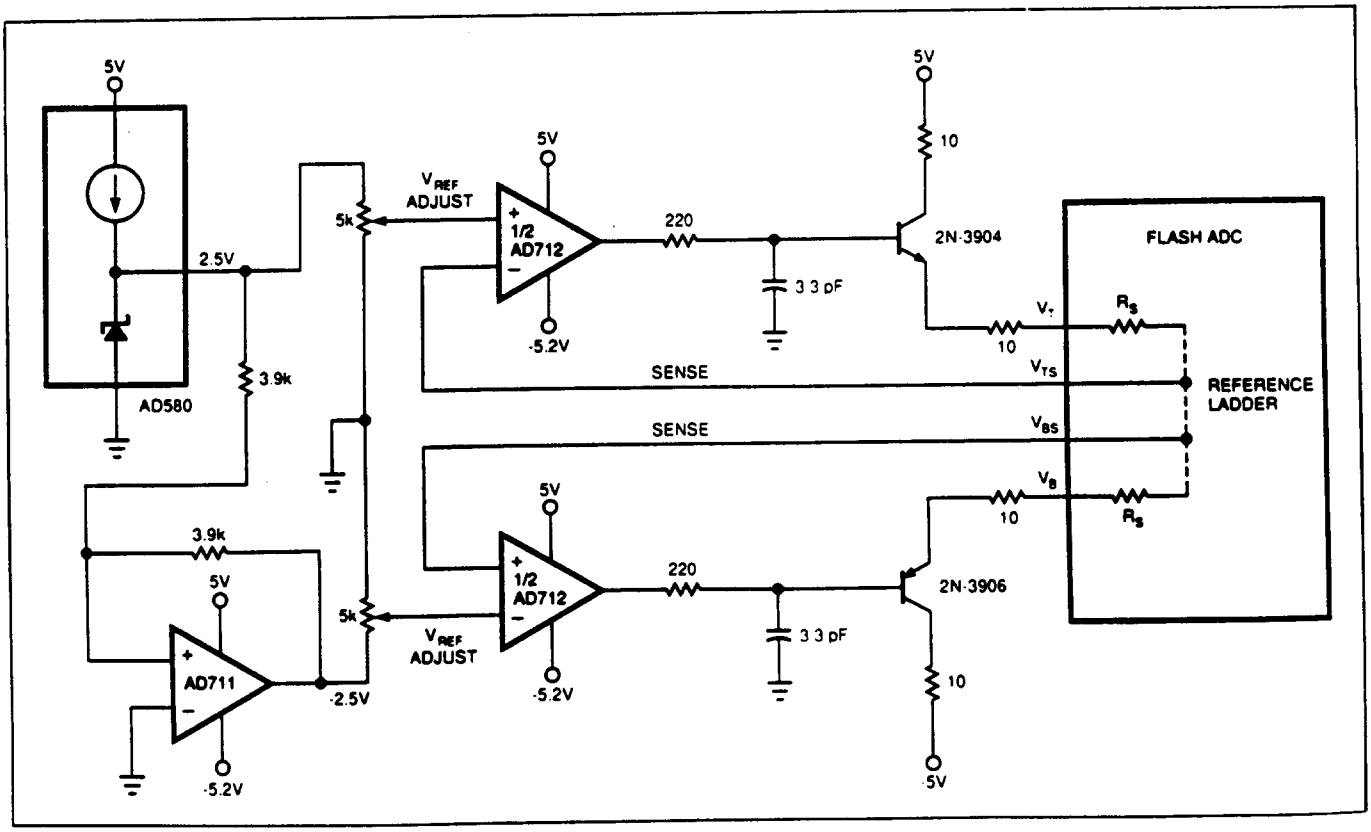


Fig 6—This reference generator for a bipolar flash converter uses the sense pins provided by the resistor ladder to compensate for the voltage drops in the package's pin and bond-wire resistances.

worse than the stated specifications when the amplifier is in the hold mode and actually driving a flash converter. Also, the loading effects of the converter may degrade the T/H amplifier's performance. In addition, obtaining the optimum relationship between the various timing pulses that drive the T/H amplifier and the flash converter may require considerable experimentation.

Because of these many difficulties, the current goal of many ADC manufacturers is either to provide flash converters whose dynamic performance is acceptable without a T/H function, or to integrate the T/H function and converter on the same chip. In either case, manufacturers can fully specify the ADC for dynamic performance and spare you the somewhat difficult design problems associated with interfacing the T/H amplifier to the converter.

The knowledge of internal ADC features and the requirements these ADCs place on external circuits should guide your initial design efforts. But once you finish the design and build your circuit, you'll want to ensure that the combined performance of your converter and its support circuits meets your requirements. Part 2 will discuss various DSP-based test methods that are particularly effective in flash-converter testing.

Reference

1. Sheingold, Dan, *Analog-Digital Conversion Handbook*, 3rd ed, Prentice-Hall, Englewood Cliffs, NJ, 1986.