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Build a Single-Shot Recorder to Catch Fast Transients

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Capturing fast transients places special requirements on filters, track/hold amplifiers, and A/D converters. By using an A/D converter with a high input bandwidth and oversampling at a 10:1 ratio, you can digitize and then analyze transients without using an expensive analog or digital storage scope.

Don't tie up expensive equipment trying to capture transients that occur infrequently. If you build a low-cost transient recorder or event sampler, you can dedicate it to capturing single-shot events. Typical applications for transient recorders include monitoring power-mains transients, evaluating power supplies, and capturing pressure and vacuum-line transients in medical equipment.

To build a transient recorder or burst-mode event sampler, you need a high-speed A/D converter, a wide-band track/hold amplifier, and an antialiasing filter. The A/D converter must have a sampling rate of at least twice the bandwidth to satisfy the Nyquist criterion. In practice, you should oversample the input signal. At 2× oversampling (a sampling frequency of twice the input bandwidth), you'll need to use a filter with an infinite roll-off rate to avoid aliasing effects. At 3× oversampling, the roll-off requirement drops to 50 dB/octave in an 8-bit system. With an oversampling ratio of 10:1, the filter roll-off need be only about 16 dB/octave. (See box, "Oversampling reduces antialiasing requirements.")

High-speed sampling A/D converter chips routinely include track/hold amplifiers on the same chip. The AD7821 is an example of this trend. It combines a 100-kHz track/hold amplifier with a 1M-sample/sec 8-bit A/D converter. Because the A/D conversion rate is 10 times the input bandwidth, you don't have to design a complex antialiasing filter. In fact, if the input signal exhibits only a low-power spectral content at and above 500 kHz, you can eliminate the filter altogether.

The AD7821 uses a half-flash conversion technique to perform an 8-bit conversion in 660 nsec. A requirement of a 350-nsec signal-acquisition period between conversions results in a maximum acquisition rate of 1M samples/sec. You can operate the A/D converter with a single or dual supply for either unipolar or bipolar inputs.

Capture single-shot waveforms

One of the difficulties in capturing single-shot events is the speed at which the transient recorder circuit responds once the input signal has crossed a predetermined trigger point. If the recorder circuit responds too slowly, it can miss fast transients altogether.

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To build a transient recorder or burst-mode event sampler you need a high-speed A/D converter, a wideband track/hold amplifier, 1 an antialiasing filter.

Therefore, to accurately capture fast events, you need a high-speed A/D converter and a wide-bandwidth track/hold amplifier. For example, an 8-bit A/D converter that has a 1-μsec conversion time can capture 1-μsec transients only if it's not preceded by a track/hold amplifier. If you match this A/D converter with a track/hold amplifier that has a 100-kHz bandwidth, the ADC can recover 6-μsec-wide 5V transients.

To simplify fault detection or take corrective measures, you need a transient recorder that can grab pretransient information. You can use this pretransient data to learn timing relationships between the transient and another waveform. Additionally, your recorder should be able to react to both positive and negative transients.

Another important criterion for transient recorders is cost. Although you could use a digital storage oscilloscope (DSO) to capture frequently occurring or very fast transients, dedicating a DSO to capturing random events would be an expensive proposition.

Transient recorder

A block diagram of a transient recorder (Fig 1) shows the minimum hardware you'll need to build a high-speed transient recorder with playback. For sim-

Oversampling reduces antialiasing requirements

In the spectrum of a periodically sampled waveform, the spectrum of the (unsampled) input-signal repeats around harmonics of the sampling frequency. Any frequency contained in the input signal is repeated above and below each harmonic of the sampling frequency. Therefore, in the spectrum of the sampled signal, the band between 0 and f_{IN} (the input spectrum), appears—among other places—between $f_S - f_{IN}$ and f_S, where f_S is the sampling frequency. Though you may be under the impression that the input-signal bandwidth is 100 kHz, if the sampling frequency is 1M sample/sec, a signal at 991 kHz in the input spectrum would appear as a 9-kHz "alias" component in the sampled signal's spectrum.

The purpose of an antialiasing filter is to remove or at least attenuate any noise or spurious signals that could be aliased back into the bandwidth of interest. **Fig A** shows the frequency response of an antialiasing filter for a generalized A/D converter. You determine the filter roll-off by drawing a straight line between the highest signal frequency of interest, f_{IN}, and the stopband attenuation frequency, $f_S - f_{IN}$. As the ratio of f_S to f_{IN} increases (that is, as the oversampling ratio increases) the slope of the line decreases.

In an 8-bit system, an ideal ADC's signal-to-noise ratio (S/N) is slightly greater than 256:1 or 48 dB. To avoid having noise limit the system performance, the ratio of the input signal to noise should exceed the approximately 48-dB limit imposed by the ADC. Here, the signal is the peak-to-peak value of the signal within

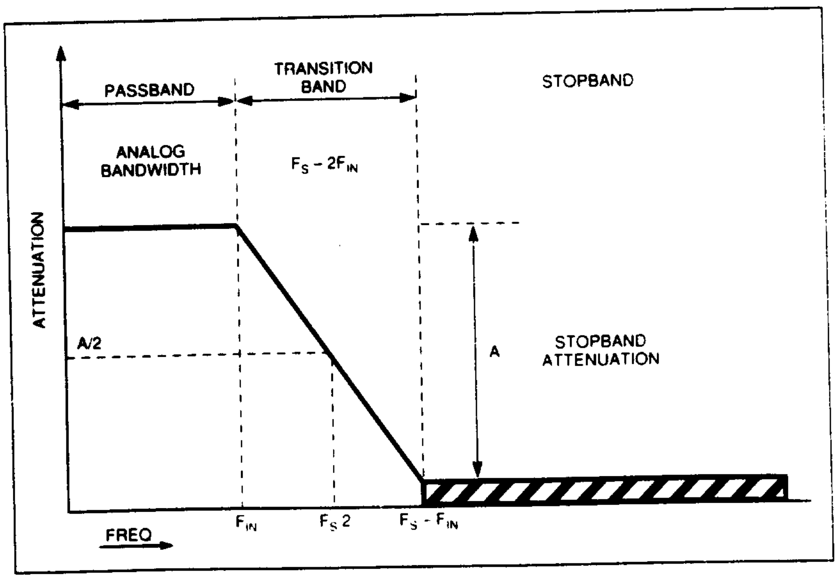


Fig A—The antialiasing filter *that precedes the transient recorder's ADC can be simple or complex depending on the degree of oversampling. When the sampling frequency is 10× the highest frequency of interest, the filter has 3 octaves to roll in its attenuation. A simple 3-pole filter has 18 dB/octave roll-off. An 8-bit ADC needs slightly more than 48 dB of attenuation. Hence, a 3-pole filter is usually sufficient for 8-bit resolution.*

plicity, the design uses a clock with an even mark/space ratio. The clock's 50% duty cycle limits the acquisition rate to 660k samples/sec rather than the A/D converter's 1-M sample/sec maximum rate. (This simplification reduces the oversampling ratio to 6.6:1.) A memory chip stores the digitized data for later playback on an X-Y plotter or oscilloscope via a dual 12-bit D/A converter and a quad op-amp. One half of the samples are pretransient information; the other half are transient data.

A more detailed schematic (**Fig 2**) shows that two counters, IC_1 and IC_2, control where the circuit stores pretransient and transient data. The counters also

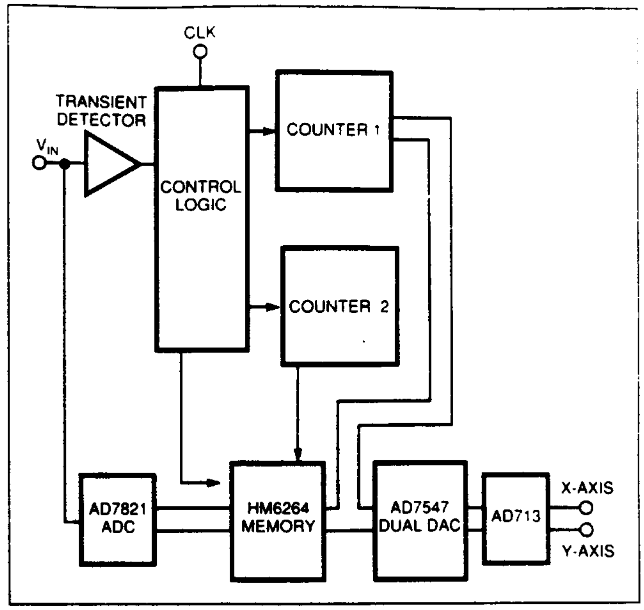


***Fig 1—If you think of a transient recorder** as merely an ADC, look again. This recorder contains several purely digital blocks as well as the DAC that drives the display.*

the band of interest, and the noise is the square root of the sum of the squares of the amplitudes of all of the frequency components outside that band. The attenuation required on signals outside the band of interest depends on the application and the expected magnitude of the out-of-band signals. In most cases, the magnitude of these signals is much lower than that of the desired signal.

Usually, 8-bit systems require 50 dB of attenuation for signals that can be aliased into the band of interest. Even if 50 dB is not the desired number, the following calculations show the kind of reduction in antialiasing filter requirements brought about by oversampling. With 2× oversampling, (that is with $f_S = 2 \cdot f_{IN}$), f_S and f_{IN} are at the same point and the filter has to have infinite roll-off to attenuate signals at $f_S - f_{IN}$. With $f_S = 3 \cdot f_{IN}$ (3× oversampling), the filter's attenuation must drop from 0 dB at f_{IN} to 50 dB at $2 \cdot f_{IN}$. In other words, the slope of the attenuation vs frequency curve must be 50 dB/octave; the filter (if it has a Butterworth characteristic) must have more than eight poles.

With 10× oversampling, there are three octaves for the attenuation to drop from 0 to 50 dB. The required slope is a little more than 16 dB/octave; a 3-pole Butterworth filter will do the job.

The above analysis of the antialiasing filter holds true regardless of the type of ADC that follows the filter. No matter what the conversion technique, oversampling reduces the antialiasing filter requirements. Oversampling also reduces the ADC noise within the signal bandwidth because it spreads the quantization noise over a wider bandwidth. Oversampling has recently gained considerable popularity in connection with sigma-delta ADCs. In the case of these converters, the advantages of oversampling are much greater than with successive-approximation or flash ADCs because noise shaping produces dramatic improvements in noise performance as the oversampling ratio increases.

The relationship between antialiasing-filter performance and oversampling is, however, exactly the same for an oversampled sigma-delta modulator as for a half-flash or a successive-approximation ADC. A sigma-delta ADC and a half-flash ADC with the same oversampling ratio place the same requirements on the antialiasing filter.

The disadvantage of the sigma-delta process for transient recording is the pipelining or averaging technique inherent in sigma-delta converters. Because of the pipelining, a step change requires a significant time (the settling time of the ADC's digital filter) to ripple through to the output. Therefore, there is a delay before a sigma-delta converter produces an output that represents an input change. Between the time the input changes and the sigma-delta converter's output reflects the change, the ADC's output does not accurately represent the converter's input. Such performance is not appropriate for transient recorders of the type discussed here.

To avoid aliasing effects, at 2× oversampling (a sampling frequency of twice the input bandwidth) you need a filter with infinite roll-off rate.

clock out data to either the oscilloscope or the X-Y plotter. You can use the fast clock input, CLK IN_1, for the clock source when you're using the circuit in the record mode or displaying stored data on an oscilloscope. The design also provides a slower clock input, CLK IN_2, to print data on an X-Y plotter.

The transient recorder operates in two basic modes: record and playback. You select the record mode by placing switch S_1 in the record position. (IC_{18A} and IC_{18B} provide debouncing for this switch.) Having the MODE output of IC_{13D} low makes one input of both IC_{15D} and IC_{14D} low. Hence the clock inputs of IC_{9A} and IC_{9B} (pins 10 and 2, respectively) are disabled, ensuring that the $1\overline{Q}$ and $2\overline{Q}$ outputs of IC_{9A} and IC_{9B} are high. Besides disabling the chip-select inputs of the D/A converter, $\overline{CSA}$ and $\overline{CSB}$, the circuit disables the output-

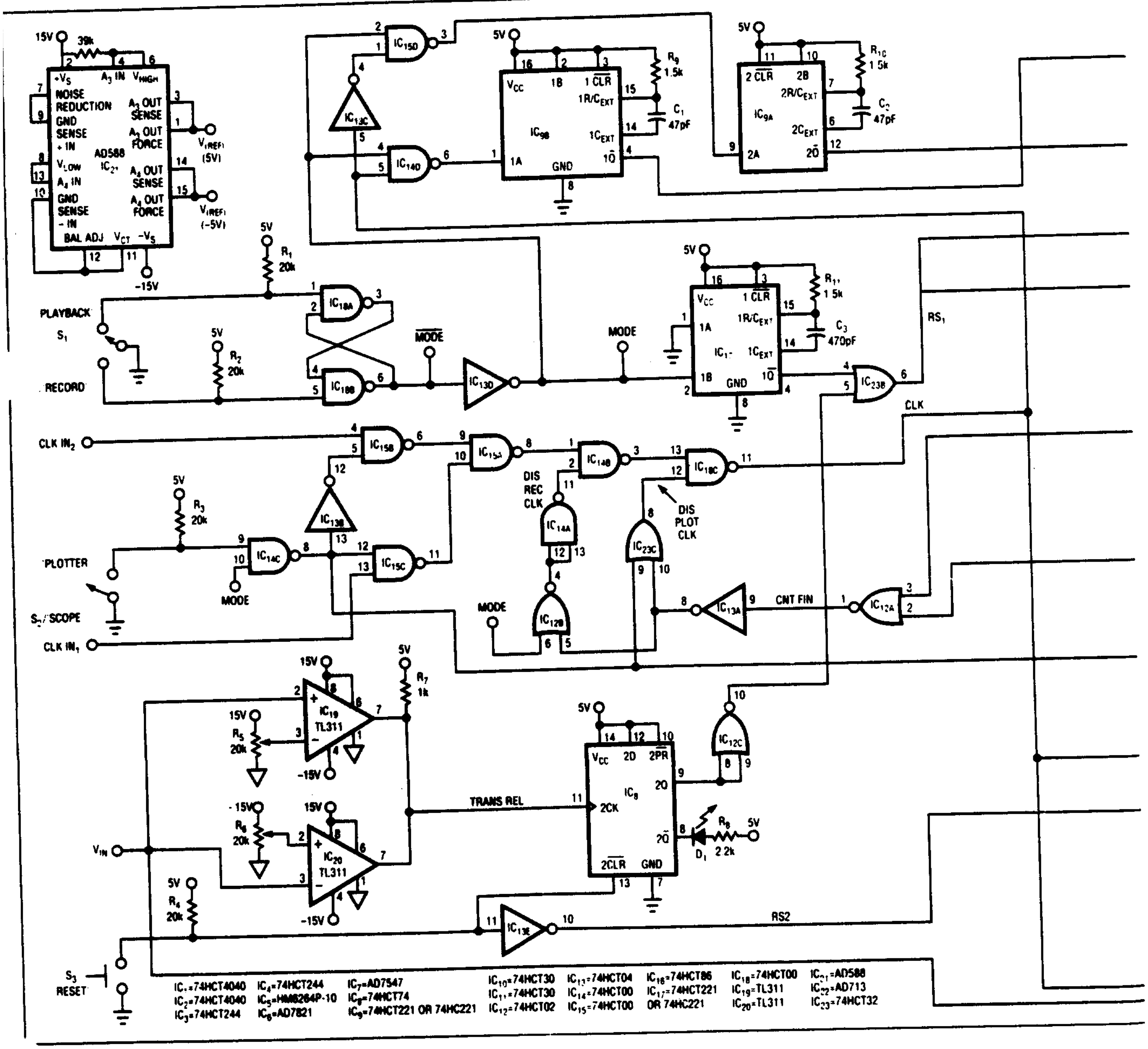
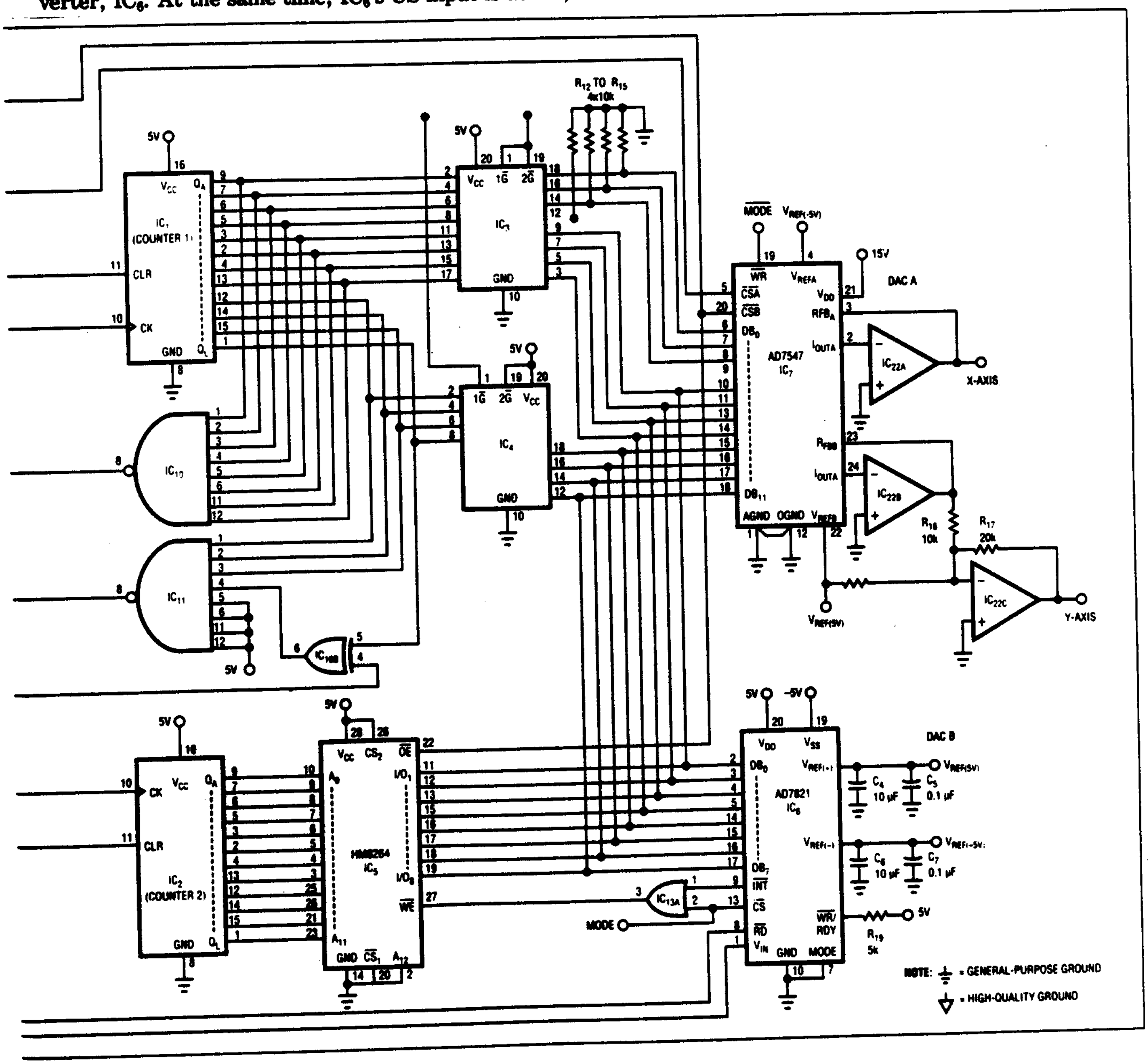


Fig 2—At the component level, the basic transient recorder is a circuit of moderate complexity, requiring 23 ICs.

enable signals of IC_3, IC_4, and IC_5 (the HM6264 memory chip), ensuring that the playback portion of the transient recorder is turned off.

CLK IN_1 serves as the clock source for the counters via IC_{14C}, IC_{-13B}, IC_{15B}, and IC_{15C}. While the MODE signal is low, CLK is the clock input for both counters and provides the $\overline{RD}$ (convert) signal for the A/D converter, IC_6. At the same time, IC_6's $\overline{CS}$ input is active, ensuring that the device is selected. After a reset from S_3 initializes the circuit, counter 2 begins counting. IC_{17} and IC_{23B} hold the reset (CLR) input of counter 1 high from power-up and keep counter 1 in a reset condition until the circuit detects a transient.

You configure the A/D converter by tying its MODE input (pin 7) to GND. (Note that the MODE pin of the AD7821 shown bears no relation to the signal labeled



With an oversampling ratio of 10:1, the filter roll-off need be only about 16 dB/ octave.

MODE in the circuit diagram.) When the CLK signal toggles its $\overline{RD}$ input, the A/D converter executes continuous conversions of the input signal, V_{IN}. Counter 2 provides the memory addresses for the A/D conversion results. Data transfers from the digital outputs of IC_6 to IC_5 employ the $\overline{INT}$ output of IC_6 to drive the $\overline{WE}$ input of IC_5.

The circuit automatically loads the first conversion result after reset into location 0 of memory and the second result into location 1. After transferring the result of the 4096th conversion to memory location 4095, the counter resets and stores the next conversion result in location 0. The memory will therefore always contain the most recent 4096 samples of the input waveform.

Detect fast transients

You apply the input signal to V_{IN}. This terminal connects directly to two TL311 comparators and the analog input of the A/D converter. Comparator IC_{19} detects positive transients, and IC_{20} detects negative ones. To set the threshold level for a positive-going signal, adjust resistor R_5; adjust R_6 for negative-going transients. Wire the outputs of both comparators together to ensure that they produce a rising edge to the clock input of IC_8 when either a negative or a positive transient occurs.

Once the circuit detects a rising edge at pin 11 of IC_8, it illuminates an LED, D_1. At the same time, it releases counter 1 from its reset condition by taking RS_1 low. Now the circuit clocks both counter 1 and counter 2 as A/D conversions continue. Counter 2 counts up from the value it held before the transient was detected. The memory locations determined by the output of counter 2 store the transient data while overwriting the oldest 2048 samples of pretransient data already stored in memory. Counter 1 counts off the 2048 clock states that correspond with the samples.

Because the output of IC_{18B} is always high in the record mode, when counter 1 reaches 2047, all inputs to IC_{10} and IC_{11} are high and both IC's outputs go low. As a result, the output of IC_{12A} goes high, causing the output of IC_{14A} to go low via IC_{13A} and IC_{12B}. This DIS REC CLK signal gates off CLK IN_1 from the rest of the circuit at IC_{14B}. The output of IC_{18C} ensures that the CLK signal is held low, stopping both counters and the A/D converter.

At the end of the transient-record cycle, the memory will contain 4096 samples of the input waveform. One half of these samples are transient data, the other half represent pretransient information. Whatever value is in counter 2 will be the last memory location for the transient data. The next memory location will hold the first of the 2048 words of pretransient data. Now when you start the playback mode, the first output from the counter will correspond to the memory location of the first pretransient sample. (To alter the ratio of transient to pretransient samples, simply alter the connections from counter 1 to IC_{10} and IC_{11}.)

To accurately convert the input waveform to stored data, you must pay close attention to the circuit. Use a precision reference, IC_{21}, to generate 5V and −5V references for the V_{REF+} and V_{REF-} inputs of the A/D converter. Make sure that you properly decouple these reference voltages along with the V_{DD} and V_{SS} lines of the A/D converter. Connect IC_6's GND pin to the star ground of the system (the point in the circuit at which you connect the analog and digital grounds). Make sure that the conductor between the A/D converter and the star ground is as wide as circuit-board layout constraints allow. Further, ensure that the $\overline{WR}$/RDY line is pulled high via R_{19} to avoid noise pickup on this pin.

Play back captured signals

Once you've captured that bothersome transient, you can play it back at any convenient time; the recorder will retain the information as long the power remains on, or until you depress the reset button. Select the playback mode with S_1. Playback takes the MODE signal low, activates the $\overline{WR}$ input to IC_7, and deselects IC_6 by taking its $\overline{CS}$ high. You can display the transient on either an analog oscilloscope or an X-Y plotter, depending on the position of S_2. Make sure to select the oscilloscope or the plotter before starting playback.

If you decide to display the transient on an oscilloscope, the clock source for the circuit is the same as in the record mode. If you use a plotter for playback, the clock frequency is much lower and is applied via the CLK IN_2 input. CLK (from either CLK IN_1 or CLK IN_2) passes through gates IC_{15D} and IC_{14D} because the MODE signal is high. IC_{9A} and IC_{9B} generate the $\overline{CSA}$ and $\overline{CSB}$ pulses for IC_7 from this CLK signal.

IC_{9A} drives the $\overline{CSA}$ input of IC_7 as well as the enable signals for IC_3 and IC_4. When you choose the playback mode, counter 1 resets and starts counting from 0 to 4095. The counter's output is the digital input code to DAC A of IC_7. This DAC drives the X axis of either the oscilloscope or the plotter. DAC A produces

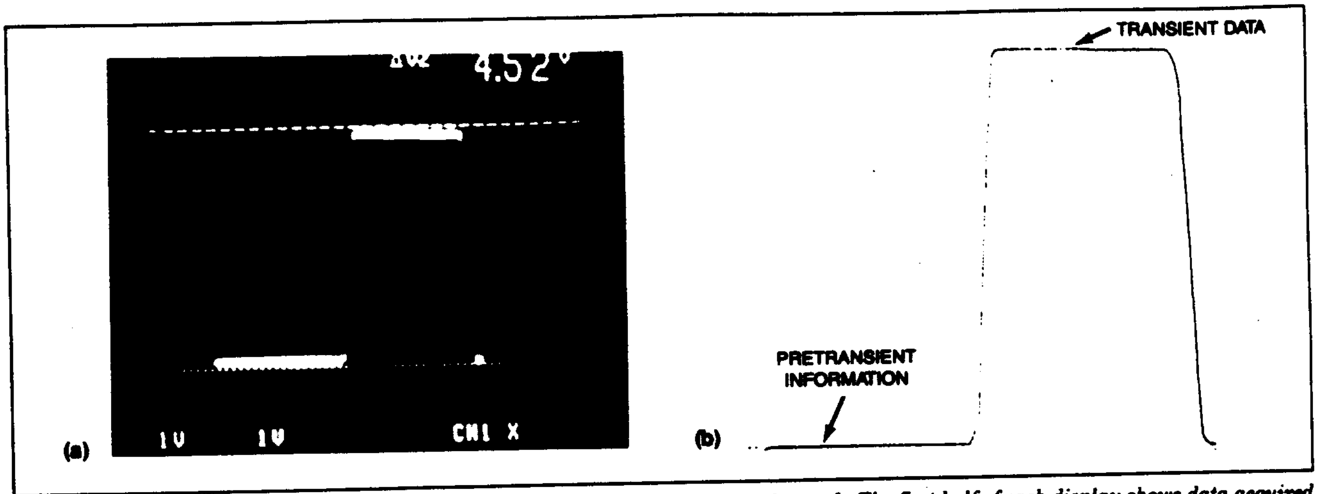


Fig 3—The recorder can display captured data on a scope, a, or on an X-Y pen plotter, b. The first half of each display shows data acquired before the triggering event.

a unipolar output range from 0 to 5V, with a resolution of 4096 steps.

The output of IC_{9B} drives the $\overline{CSB}$ input of IC_7 and also sets the logic level on IC_5's output-enable line, $\overline{OE}$. This action latches the data from memory into DAC B, which drives the Y axis of the oscilloscope or plotter. By using dual supplies, you can set DAC B for a bipolar output range to reconstruct both positive and negative transients.

Counter 2 starts its count from the point at which it stopped at the end of the record mode; the first memory output word to IC_7 is the oldest sample in memory. The scan will then proceed through the 2048 samples of pretransient information and the 2048 samples of transient information. The output of each sample from memory to the Y axis, via DAC B, corresponds to the output of a count value from counter 1 to the X axis via DAC A. In this way, the circuit reconstructs the pretransient and transient waveforms.

For oscilloscope display of waveforms, place S_2 in the scope position. Doing so locks out CLK IN_2 from the rest of the circuit but allows CLK IN_1 to operate as clock signal for the circuit. Unlike the plotter display option, where counter 1 runs through once and then stops, CLK runs continuously. CNT FIN does go high when counter 1 reaches a count of 4095, but because the output of IC_{14C} is high, the DIS PLOT CLK signal does not go low. You can see the typical oscilloscope waveform display in **Fig 3(a)**.

You display the stored waveform on an X-Y plotter by placing S_2 in the plotter position. Doing so locks out the CLK IN_1 input from the rest of the circuit and permits CLK IN_2 to generate the clock signal for the circuit. IC_{16B}, IC_{10}, IC_{11}, and IC_{12A} function in a manner similar to the record mode to generate a high CNT FIN signal. But this time, IC_{10} and IC_{11} go low when counter 1 reaches a count of 4095. IC_{13A} goes low, and, because the output of IC_{14C} is already low, the DIS PLOT CLK signal goes low, turning off CLK IN_2 at IC_{18C} and holding the CLK signal high. **Fig 3(b)** shows a captured transient displayed using a plotter as the display method.

Record-mode timing and clock waveforms

The timing diagrams in **Fig 4** show the logic relationships for the record mode. The MODE signal (not shown) is low and the DIS REC CLK signal is high. The RS_2 signal goes high when the recorder receives a reset command via S_3 resetting counter 2. The next falling edge of the CLK signal clocks out an address for IC_5 from counter 2. A conversion is also initiated on this falling CLK edge, and, within 700 nsec, the $\overline{INT}$ signal of IC_6 goes low, activating the $\overline{WE}$ input of IC_5. The rising edge of CLK resets the $\overline{INT}$ line 50 nsec later.

When the circuit detects a transient, the TRANS REC signal goes high, causing the RS_1 line to go low and releasing counter 1 from its reset state. The next falling edge of CLK clocks out the outputs from counter 1. When the count output from counter 1 reaches 2047, the CNT FIN signal goes high and causes the DIS REC CLK signal to go low, shutting off the CLK signal.

To accurately capture fast events, you need a high-speed A/D converter and a wide-bandwidth track/hold amplifier.

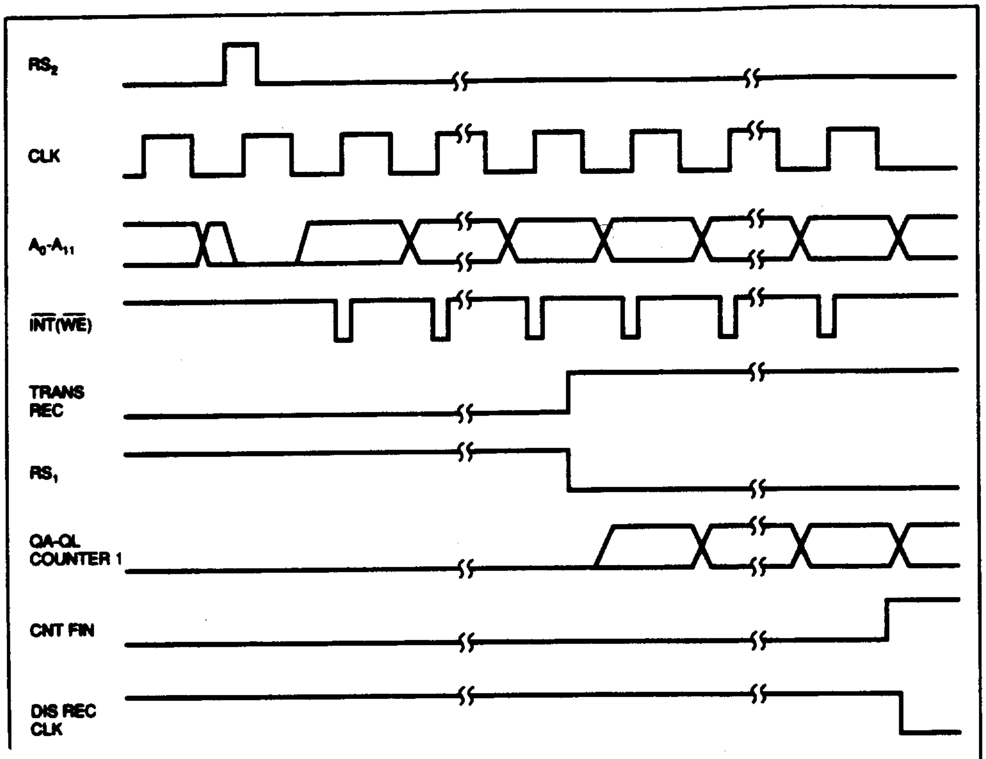


Fig 4—The timing relationships in the record mode show that recording starts on the first falling clock edge after the reset line goes high.

In the record mode in the waveforms shown, the 50/50 mark/space ratio of the CLK signal limits the clock frequency to 660 kHz. You need a CLK-low time of 750 nsec for the A/D converter to perform its conversion correctly and latch the data into IC_5. However, the CLK-high time can be as short as 350 nsec, the time required between conversions by the AD7821. Therefore, if the input to CLK IN_1 has a low time of 750 nsec and a high time of 350 nsec, the circuit can make one conversion every 1100 nsec—equivalent to approximately 900k samples/sec.

Playback to a scope

During playback to an oscilloscope, (**Fig 5(a)**), the MODE signal, the $\overline{WE}$ input of IC_5, and the DIS REC CLK signal are high. When you place S_1 in the playback mode, RS_1 goes high, resetting counter 1. The CLK signal generates a $\overline{CSA}$ signal for IC_7 on its rising edge and a $\overline{CSB}$ signal on its falling edge. The falling edge of the CLK signal clocks data from counter 1, and the rising edge of $\overline{CSA}$ updates the X axis. The falling edge of $\overline{OE}$ outputs stored data from memory, and the rising edge of $\overline{CSB}$ updates the Y axis. The CLK signal runs continuously when the circuit is in the scope-playback mode.

The timing diagram of **Fig 5(b)** shows operation of the circuit for playback on a plotter. Once again, MODE, the $\overline{WE}$ input of IC_5, and the $\overline{\text{DIS REC CLK}}$ signals are high. The circuit generates $\overline{CSA}$ and $\overline{CSB}$ to update the X and Y axes. Compared with scope playback, the difference in the circuit's operation is that when the output count from counter 1 reaches 4095 and the CNT FIN signal goes high, the DIS PLOT CLK signal goes low, forcing the CLK signal into a high state.

Burst-mode event sampling places requirements on an A/D converter similar to those for transient recording. In burst-mode sampling, the recorder looks at the input waveform infrequently, but when it does, it must acquire a large number of samples in a short time. With slower microprocessors or microcontrollers, you'll find that because of instruction- and bus-timing constraints, you can't achieve anything like the A/D converter's maximum throughput.

You can overcome timing limitations in a burst-mode sampler by using a DMA controller to initiate A/D conversions and transfer conversion data to memory. Doing so lets you run the A/D converter at or near its maximum sample rate, permitting high oversampling ratios and the acquisition of short transients.

Building a burst-mode sampler is a simple matter with the popular 8052 microcontroller (**Fig 6**). Al-

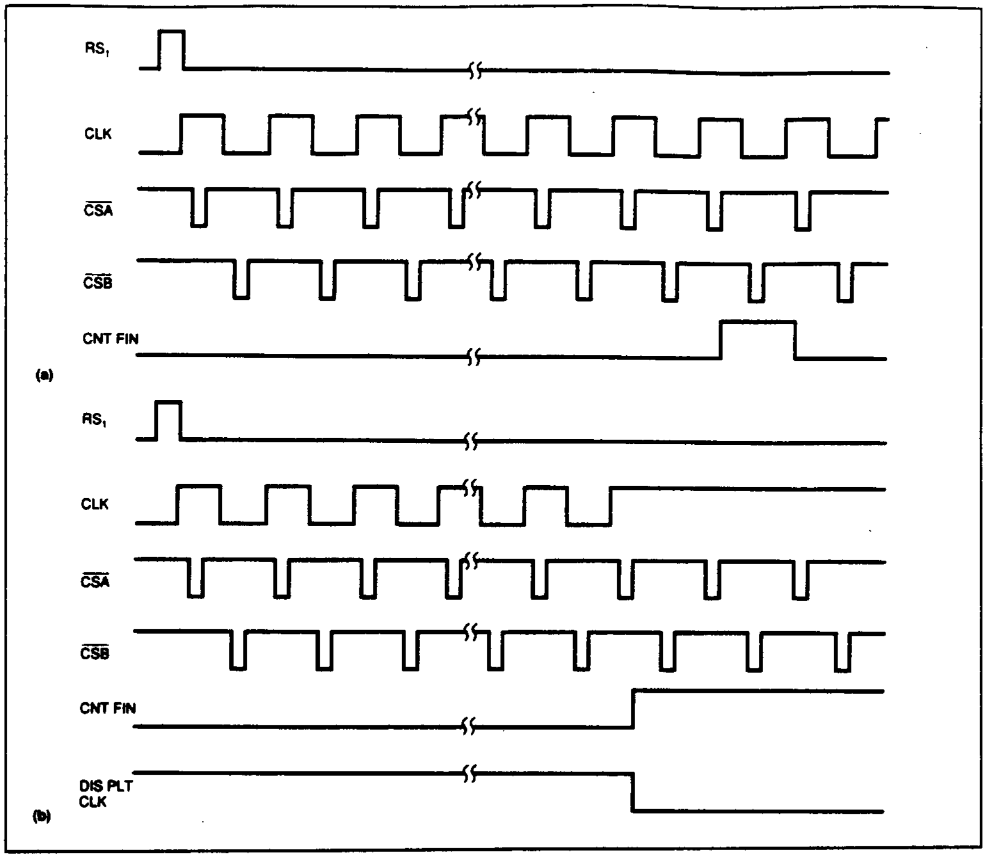


***Fig 5—The timing for waveform playback** is almost the same in the scope mode (a) as in the plotter mode (b). The difference is that the scope playback runs continuously, whereas the circuit produces a plotter output only once.*

though the 8052 does not support hardware DMA, it does support what is termed "fake DMA." However, expect the response time to DMA requests to be much slower than what is possible with microcontrollers that support genuine DMA.

The HM6264P memory chip, IC_3, stores the control program for IC_1. The first part of the control program is the initialization routine. This routine (**Listing 1**) sets up the sense of the DACK0 line of the 8237, IC_2, to be active high. It also loads the starting data address into IC_2 for the first conversion results. IC_1 initializes the counting register to control the number of conversions before IC_2 returns control to IC_1. The program must also set up IC_1 for "fake DMA."

Once you've run the initialization program, IC_2 is ready to take control when requested to do so. Although IC_2 has four interrupt-request lines, this circuit uses only one, DREQ0. An external command signal drives this interrupt line high, telling IC_2 to take control of the circuit and start the A/D converter sampling the input waveform.

After IC_2 receives the DREQ0 request (Fig 7), its $\overline{HRQ}$ line goes high and feeds IC_{14C}, which takes the $\overline{INT0}$ line of IC_1 low. IC_1 responds to this "fake DMA" request by bringing its P1.6 line low and the output of IC_{14A} high, selecting inputs of IC_7, IC_8, IC_9, and IC_{10}. When the output of IC_{14A} goes high, it shuts off IC_1's address and data lines from the rest of the circuit and deselects the output's address decoder, IC_{13}. The inverted P1.6 line also feeds the HLDA input of IC_2, acknowledging IC_2's request for control. IC_2 then takes control of the address and data bus and the sampling of the input waveform.

To reduce pin count, IC_2 multiplexes the eight higher-order address bits on the data lines. You need an external device to latch these address bits. The address strobe signal, ADSTB, takes AEN high and switches the $\overline{OC}$ line of IC_6 low. ADSTB drives the C input of IC_6 to latch the higher address lines to the outputs of IC_6. The inverted AEN line also drives one input of IC_{16D}. The decoded output, Y_0, of IC_{13} controls the other input of this gate. Therefore, either a high on AEN or a low on the decoder output selects IC_3. You need this control logic because both IC_2 and IC_1 must be able to access IC_3.

The DACK0 line goes high at about the same time that ADSTB latches the address and drives one input of IC_{15A}. IC_{15A} and IC_{15B} ensure that the $\overline{CS}$ line of IC_4 goes low only when an input/output read operation of $\underline{IC_2}$ occurs. IC_{15C} provides the correct polarity for the $\overline{RD}$ input and equalizes the delay paths for the $\overline{CS}$ and $\overline{RD}$ lines, ensuring that the circuit obeys the $\overline{CS}$-to-$\overline{RD}$ setup time.

Once IC_4 receives a $\overline{CS}$ signal, it acknowledges receipt of the signal by bringing its RDY line low, placing the controller, IC_2, into a wait state for as long as its READY input is low. When the device completes a conversion, the RDY line goes high, releasing IC_2 from its wait state. Because IC_4's RDY output is an open-drain output, you need to install an external pullup resistor, R_2.

When the circuit releases IC_2 from its wait state,

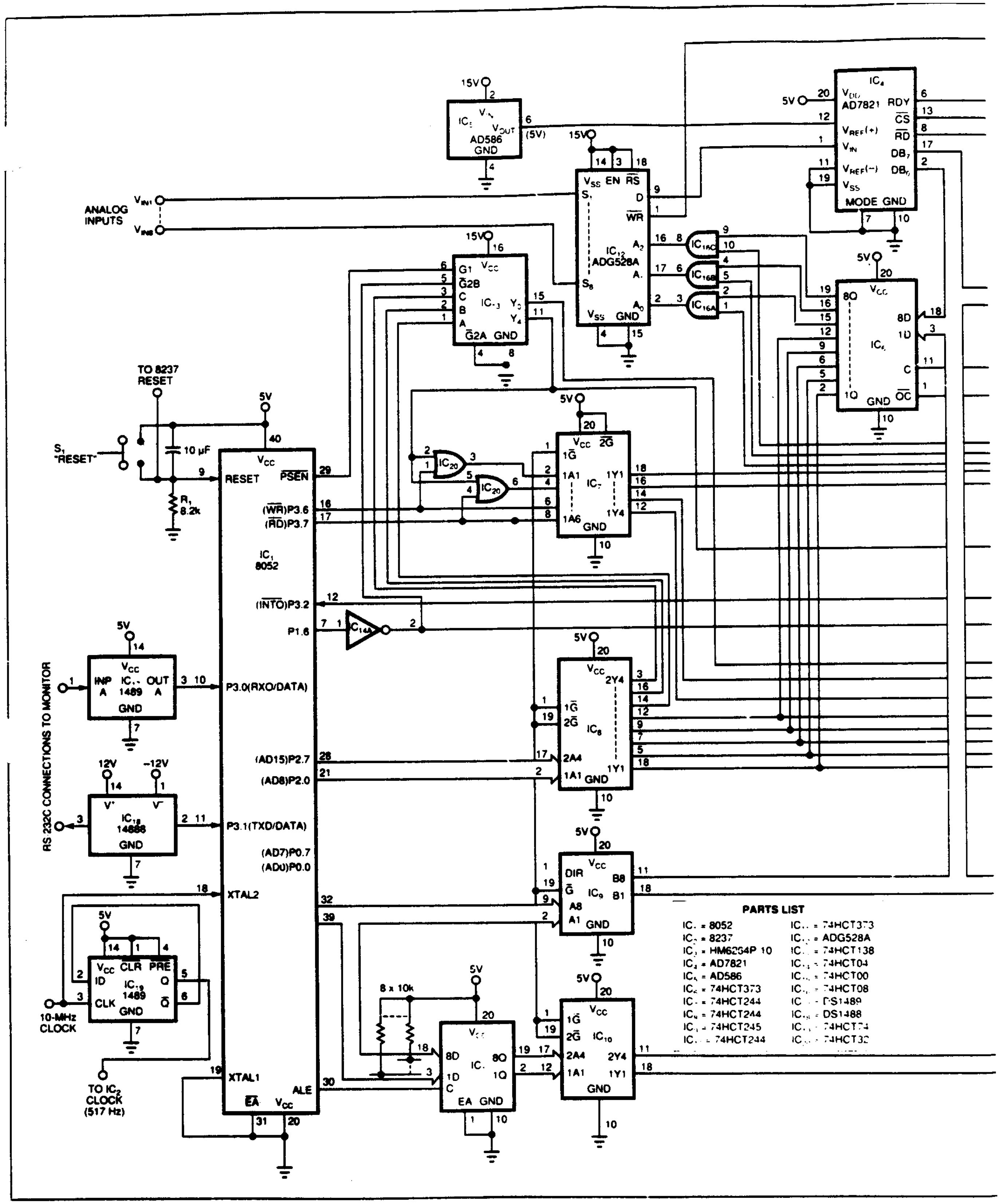
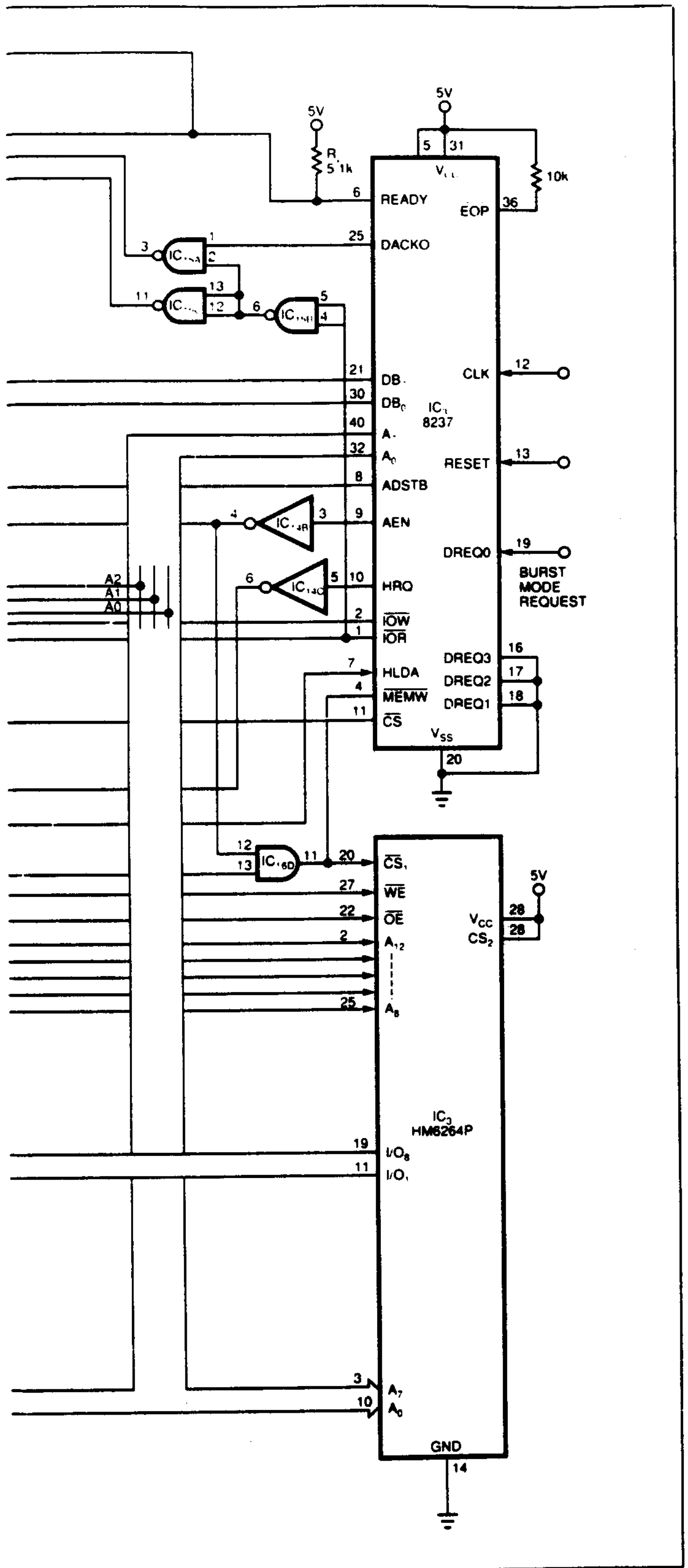


Fig 6—A burst-mode sampler using an 8052 microcontroller is roughly equal in complexity to the transient recorder shown earlier.

data from IC_4 is valid. The address lines of IC_2 determine where data loads into memory. IC_2 performs all of these operations automatically because a memory write accompanies each input/output read. Depending on the value loaded into the counting register, IC_2 will continue to issue read commands to IC_4 until the circuit completes the required number of conversions. IC_2 automatically increments the memory address after every write operation.

The multiplexer, IC_{12}, accommodates eight input



channels. The three upper and three lowest address lines of IC_2, gated through IC_{16A}, IC_{16B}, and IC_{16C}, select the input channel. If the three upper address lines are set to all 1s, IC_4 will convert each channel in sequence, and the conversion results will be stored in consecutive memory locations. For example, if the first conversion takes place on the channel-1 input voltage, V_{IN1}, and the result is stored in location M of IC_3, the next conversion will take place on V_{IN2}, and the result will be stored in location M + 1. If the three uppermost address bits are set to 011, the circuit will sequence through channels 1 to 4 only.

Ready or not

The RDY line of IC_4 drives the $\overline{WR}$ input of IC_{12}, loading the address for the next channel to be converted into the multiplexer. When you have only one input channel to convert, you can use an alternate design: Remove IC_{16A}, IC_{16B}, and IC_{16C}, and drive the A0, A1, and A2 inputs of IC_{12} directly from the three uppermost address lines. Using this scheme, the program chooses the input channel.

IC_1 selects the device it talks to using a 1-of-8 address decoder, IC_{13}. The outputs of IC_{13} provide signals for IC_{12}'s $\overline{WR}$ line, IC_3's $\overline{CS}$ input, and IC_2's $\overline{CS}$ input. One of the outputs also gates the P3.7 ($\overline{RD}$) and the P3.6 ($\overline{WR}$) outputs from IC_1 to drive the $\overline{IOW}$ and $\overline{IOR}$ inputs of IC_2. The upper three address lines of IC_1 select the required device. The lower address lines are multiplexed with the data lines in a manner similar to the way IC_2's address and data lines are multiplexed. IC_{11} demultiplexes the lower eight address lines. IC_1's ALE signal latches these address lines. The 3-state buffers, IC_7, IC_8, and IC_{10}, isolate IC_1 outputs from the address bus when IC_2 takes control. You must use these buffers because IC_1 can't place its address and data buses into a high-impedance state when IC_2 takes control of the circuit. IC_9 also acts as a buffer but is bidirectional because IC_1 must read data from and write data to memory.

IC_1 uses a 10-MHz input-clock frequency. A 74HCT74 counter (IC_{19}) divides down this clock to form the clock input to IC_2. The standard 8237 operates from a 3-MHz maximum clock frequency, so you can divide the 10-MHz clock by 4 to provide IC_2's clock. You'll have a resultant acquisition rate of 608k samples/sec. A faster version of the 8237, the 8237-5, operates from a 5-MHz input clock, allowing you to divide the clock frequency by 2 and enabling the circuit to take 812k samples/sec. If you were to use IC_1 on its own to control the sampling of the input waveform, the best acquisition rate you could obtain would be approximately 100k samples/sec.

The entire circuit operates from 15V and 5V sup-

Listing 1—Initialization Routine

```
10      XBY(8008H) = 80H             : SETS DACK SENSE ACTIVE HIGH
20      XBY(800FH) = 0EH             : CLEARS DREQ0 MASK REGISTER
30      XBY(800BH) = 94H             : SETS MODE REGISTER
40      XBY(800CH) = 00H             : CLEARS FIRST/LAST FLIP-FLOP
                                     :  (ONLY REQUIRED IF 8237 IS
                                     :  NOT RESET BETWEEN DMA REQUESTS)
50      XBY(8000H) = 00H             : LOADS LOWER BYTE OF STARTING DATA
                                     :  ADDRESS TO BASE AND CURRENT ADDRESS
60      XBY(8000H) = 08H             : LOADS HIGHER BYTE OF STARTING DATA
                                     :  ADDRESS TO BASE AND CURRENT ADDRESS
70      XBY(8001H) = 00H             : LOADS LOWER BYTE OF COUNTING NUMBER
                                     :  TO COUNT REGISTER
80      XBY(8001H) = 02H             : LOADS HIGHER BYTE OF COUNTING NUMBER
                                     :  TO COUNT REGISTER
90      DBY(38) = DBY(38).OR.02H
100     IE = IE.OR.81H
110     GOTO 10
```

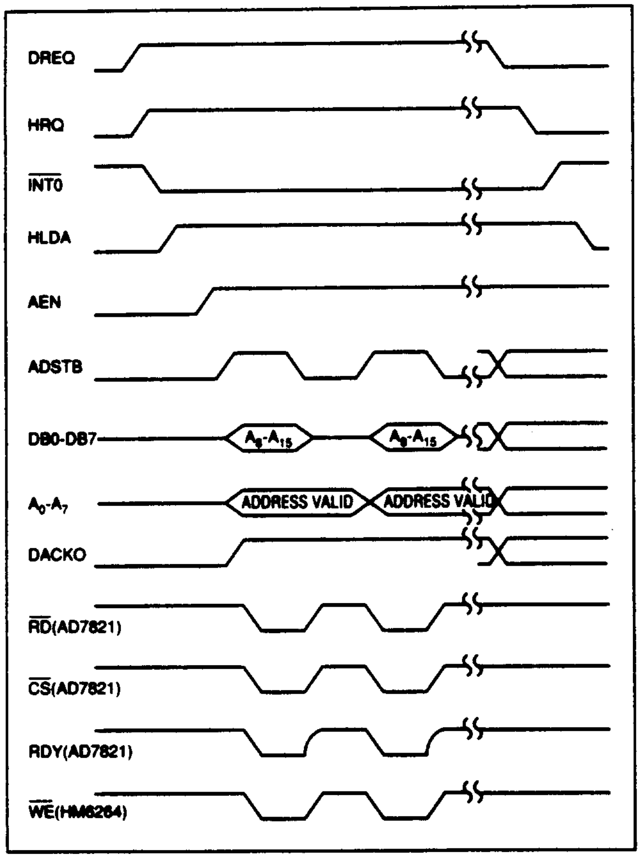


Fig 7—Although the 8052 does not support true DMA, you can create a "fake DMA" mode, which, though not as fast as real DMA, lets you transfer blocks of data directly to memory.

plies. If there isn't a 5V supply in your system, you can add a regulator to generate 5V. In addition, plan to use a precision 5V reference (IC_5) for the A/D converter, allowing an input range of 0 to 5V. To obtain accurate conversion results, you must obey the same guidelines regarding decoupling and grounding as apply to the transient-recorder circuit.

You can use the same design (**Fig 6**) with slow- and medium-speed microprocessors that support DMA requests. With these microprocessors, you'll find the DMA response time will be much faster than the response of the 8052's "fake DMA." Because microprocessors that support genuine DMA will 3-state their address and data lines during a DMA transfer, you can eliminate the 3-state driver chips.