



Next Generation OP07 Ultralow Offset Voltage Operational Amplifier

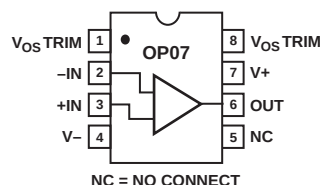
OP77

FEATURES

Outstanding Gain Linearity
Ultrahigh Gain 5000 V/mV Min
Low V_{OS} Over Temperature 60 μ V Max
Excellent TCVos 0.3 μ V/ $^{\circ}$ C Max
High PSRR 3 μ V/V Max
Low Power Consumption 60 mW Max
Fits OP07, 725, 108A/308A, 741 Sockets
Available in Die Form

PIN CONNECTIONS

**Epoxy Mini-Dip (P-Suffix)
8-Pin Hermetic DIP**

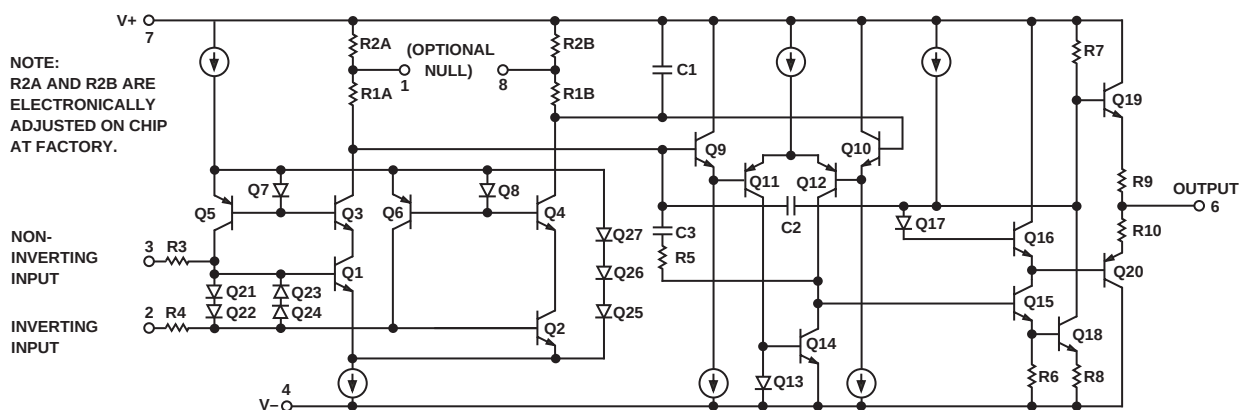
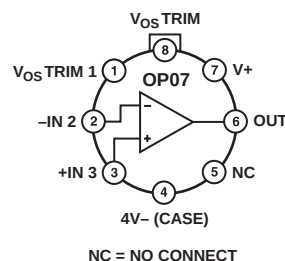


GENERAL DESCRIPTION

The OP77 significantly advances the state-of-the-art in precision op amps. The OP77's outstanding gain of 10,000,000 or more is maintained over the full 10 V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps, and provides superior performance in high closed-loop gain applications. Low initial V_{OS} drift and rapid stabilization time, combined with only 50 mW power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional TCVos of 0.3 μ V/ $^{\circ}$ C maximum and the low V_{OS} of 25 μ V maximum, eliminates the need for V_{OS} adjustment and increases system accuracy over temperature.

PSRR of 3 μ V/V (110 dB) and CMRR of 1.0 μ V/V maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP77 ideally suited for high-resolution instrumentation and other tight error budget systems.

TO-99 (J-Suffix)



NOTE:
R2A AND R2B ARE
ELECTRONICALLY
ADJUSTED ON CHIP
AT FACTORY.

NON-
INVERTING
INPUT
3 R3
2 R4
INVERTING
INPUT

REV. C

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OP77—SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ $V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	OP77A Typ	Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			10	25	μV
LONG-TERM INPUT OFFSET						
VOLTAGE STABILITY ¹	DV_{OS}/Time			0.2		$\mu\text{V}/\text{Mo}$
INPUT OFFSET CURRENT	I_{OS}			0.3		nA
INPUT BIAS CURRENT	I_B		-0.2	1.2	2.0	nA
INPUT NOISE VOLTAGE ²	e_{np-p}	0.1 Hz to 10 Hz		0.35	0.6	$\mu\text{V p-p}$
INPUT NOISE VOLTAGE DENSITY ²	e_n	$f_O = 10\text{ Hz}$ $f_O = 100\text{ Hz}$ $f_O = 1000\text{ Hz}$		10.3 10.0 9.6	18.0 13.0 11.0	$\text{nV}/\sqrt{\text{Hz}}$
INPUT NOISE CURRENT ²	i_{np-p}	0.1 Hz to 10 Hz		14	30	pA p-p
INPUT NOISE CURRENT DENSITY ²	i_n	$f_O = 10\text{ Hz}$ $f_O = 100\text{ Hz}$ $f_O = 1000\text{ Hz}$		0.32 0.14 0.12	0.80 0.23 0.17	$\text{pA}/\sqrt{\text{Hz}}$
INPUT RESISTANCE Differential Mode ³ Common Mode	R_{IN} R_{INCM}		26	45 200		MV GV
INPUT VOLTAGE RANGE	IVR		± 13	± 14		V
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 13\text{ V}$		0.1	1.0	$\mu\text{V}/\text{V}$
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$		0.7	3	$\mu\text{V}/\text{V}$
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	$R_L \geq 2\text{ k}\Omega \geq V_O = \pm 10\text{V}$	5000	12000		V/mV
OUTPUT VOLTAGE SWING	V_O	$R_L \geq 10\text{ k}\Omega$ $R_L \geq 2\text{ k}\Omega$ $R_L \geq 1\text{ k}\Omega$	± 13.5 ± 12.5 ± 12.0	± 14.0 ± 13.0 ± 12.5		V
SLEW RATE ²	SR	$R_L \geq 2\text{ k}\Omega$	0.1	0.3		V/ μs
CLOSED-LOOP BANDWIDTH ²	BW	$A_{VCL} = +1$	0.4	0.6		MHz
OPEN-LOOP OUTPUT RESISTANCE	R_O			60		Ω
POWER CONSUMPTION	P_d	$V_S = \pm 15\text{ V}$, No Load $V_S = \pm 3\text{ V}$, No Load		50 3.5	60 4.5	mW
OFFSET ADJUSTMENT RANGE		$R_P = 20\text{ k}\Omega$		± 3		mV

NOTES

¹Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV .

²Sample tested.

³Guaranteed by design.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ $V_S = \pm 15\text{ V}$, $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	OP77A Typ	Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			25	60	μV
AVERAGE INPUT OFFSET VOLTAGE DRIFT ¹	TCV_{OS}			0.1	0.3	$\mu\text{V}/^\circ\text{C}$
INPUT OFFSET CURRENT	I_{OS}			0.5	2.2	nA
AVERAGE INPUT OFFSET CURRENT DRIFT ²	TCI_{OS}			1.5	25	$\text{pA}/^\circ\text{C}$
INPUT BIAS CURRENT	I_B		-0.2	2.4	4	nA
AVERAGE INPUT BIAS CURRENT DRIFT ²	TCI_B			8	25	$\text{pA}/^\circ\text{C}$
INPUT VOLTAGE RANGE	IVR		± 13	± 13.5	0.6	V
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 13\text{ V}$		0.1	1.0	$\mu\text{V}/\text{V}$
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$		1	3	$\mu\text{V}/\text{V}$
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	$R_L \geq 2\text{ k}\Omega \geq V_O = \pm 10\text{ V}$	2000	6000		V/mV
OUTPUT VOLTAGE SWING	V_O	$R_L \geq 10\text{ k}\Omega$	± 12	± 13.0		V
POWER CONSUMPTION	P_d	$V_S = \pm 15\text{ V}$, No Load		60	75	mW

NOTES

¹OP77A: TCV_{CS} is 100% tested.

²Guaranteed by design.

OP77—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$, $T_A = 125^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	OP77E			OP77F			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE	V_{OS}		10	25		20	60		μV
LONG-TERM STABILITY ¹	V_{OS}/Time		0.3			0.4			$\mu\text{V}/\text{Mo}$
INPUT OFFSET CURRENT	I_{OS}		0.3	1.5		0.3	2.8		nA
INPUT BIAS CURRENT	I_B		−0.2	1.2	2.0	−0.2	1.2	2.8	nA
INPUT NOISE VOLTAGE ²	e_{np-p}	0.1 Hz to 10 Hz	0.35	0.6		0.38	0.65		μV_{p-p}
INPUT NOISE VOLTAGE DENSITY	e_n	$f_O = 10\text{ Hz}$	10.3	18.0		10.5	20.0		$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 100\text{ Hz}^2$	10.0	13.0		10.2	13.5		
		$f_O = 1000\text{ Hz}$	9.6	11.0		9.8	11.5		
INPUT NOISE CURRENT ²	i_{np-p}	0.1 Hz to 10 Hz	14	30		15	35		pA_{p-p}
INPUT NOISE CURRENT DENSITY	i_n	$f_O = 10\text{ Hz}$	0.32	0.80		0.35	0.90		$\text{pA}/\sqrt{\text{Hz}}$
		$f_O = 100\text{ Hz}^2$	0.14	0.23		0.15	0.27		
		$f_O = 1000\text{ Hz}$	0.12	0.17		0.13	0.18		
INPUT RESISTANCE Differential Mode ³ Common Mode	R_{IN} R_{INCM}		26	45 200		18.5	45 200		$\text{M}\Omega$ $\text{G}\Omega$
				200			200		$\text{G}\Omega$
INPUT RESISTANCE Common Mode	R_{INCM}			200			200		$\text{G}\Omega$
INPUT VOLTAGE RANGE	IVR		± 13	± 14		± 13	± 14		V
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 13\text{ V}$	0.1	1.0		0.1	1.6		$\mu\text{V}/\text{V}$
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = 3\text{ V to } 18\text{ V}$	0.7	3.0		0.7	3.0		$\mu\text{V}/\text{V}$
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	$R_L \geq 2\text{ k}\Omega$	5000	12000		2000	6000		V/mV
OUTPUT VOLTAGE SWING	V_O	$R_L \geq 10\text{ k}\Omega$	± 13.5	± 14.0		± 13.5	± 14.0		V
		$R_L \geq 2\text{ k}\Omega$	± 12.5	± 13.0		± 12.5	± 13.0		
		$R_L \geq 1\text{ k}\Omega$	± 12.0	± 12.5		± 12.0	± 12.5		
SLEW RATE ²	SR	$R_L \geq 2\text{ k}\Omega$	0.1	0.3		0.1	0.3		V/ μs
CLOSED-LOOP BANDWIDTH ²	BW	$A_{VCL} 1$	0.4	0.6		0.4	0.6		MHz
OPEN-LOOP OUTPUT RESISTANCE	R_O		60			60			Ω
POWER CONSUMPTION	P_d	$V_S = \pm 15\text{ V}$, No Load	50	60		50	60		mW
		$V_S = \pm 3\text{ V}$, No Load	3.5	4.5		3.5	4.5		
OFFSET ADJUSTMENT RANGE		$R_p = 20\text{ kn}$	± 3			± 3			mV

NOTES

¹Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV .

²Sample tested.

³Guaranteed by design.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$, $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for OP77E/FJ and OP77E/FZ, unless otherwise noted.)

Parameter	Symbol	Conditions	OP77E			OP77F			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE	V	J, Z Packages	10	45		20	100		μV
			10	55		20	100		
AVERAGE INPUT OFFSET VOLTAGE DRIFT ¹	TCV_{OS}	J, Z Packages	0.1	0.3		0.2	0.6		$\mu\text{V}/^\circ\text{C}$
			0.3	0.6		0.4	1.0		
INPUT OFFSET CURRENT	I_{OS}		0.5	2.2		0.5	4.5		nA
AVERAGE INPUT OFFSET CURRENT DRIFT ²	TCI_{OS}		1.5	4.0		1.5	85		$\text{pA}/^\circ\text{C}$
INPUT BIAS CURRENT	I_{B}	E, F	-0.2	2.4	4.0	-0.2	2.4	6.0	nA
AVERAGE INPUT BIAS CURRENT DRIFT ²	TCI_{B}		8	40		15	60		$\text{pA}/^\circ\text{C}$
INPUT VOLTAGE RANGE	IVR		± 13.0	± 13.5		± 13.0	± 13.5		V
COMMON-MODE REJECTION RATIO	CMRR	$V_{\text{CM}} = \pm 13\text{ V}$	0.1	1.0		0.1	3.0		pV/V
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 3\text{ V}$ to $\pm 18\text{ V}$	1.0	3.0		1.0	5.0		$\mu\text{V/V}$
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	$\text{R}_{\text{L}} \geq 2\text{ k}\Omega$ $\text{V}_{\text{O}} = \pm 10\text{ V}$	2000	6000		1000	4000		V/mV
OUTPUT VOLTAGE SWING	V_{O}	$\text{R}_{\text{L}} \geq 2\text{ k}\Omega$	± 12	± 13.0		± 12	± 13.0		V
POWER CONSUMPTION	P_{d}	$V_S = \pm 15\text{ V}$, No Load	60	75		60	75		mW

NOTES

¹OP77E: TCV_{OS} is 100% tested on J and Z packages.

²Guaranteed by end-point limits.

OP77—SPECIFICATIONS

WAFER TEST LIMITS (@ $V_s = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, for OP77N devices, unless otherwise noted.)

Parameter	Symbol	Conditions	OP77N Limit	Unit
INPUT OFFSET VOLTAGE	V_{OS}		40	μV Max
INPUT OFFSET CURRENT	I_{OS}		2.0	nA Max
INPUT BIAS CURRENT	I_B		± 2	nA Max
INPUT RESISTANCE Differential Mode	R_{IN}		26	M Ω Min
INPUT VOLTAGE RANGE	IVR		± 13	V Min
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 13\text{ V}$	1	$\mu\text{V/V}$ Max
POWER SUPPLY REJECTION RATIO	PSRR	$V_s = \pm 3\text{ V to } \pm 18\text{ V}$	3	$\mu\text{V/VMax}$
OUTPUT VOLTAGE SWING	V_O	$R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$ $R_L = 1\text{ k}\Omega$	± 13.5 ± 12.5 ± 12.0	V Min
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	$R_L = 2\text{ k}\Omega$ $V_O = \pm 10\text{ V}$	2000	V/mV Min
DIFFERENTIAL INPUT VOLTAGE			± 30	V Max
POWER CONSUMPTION	P_d	$V_{OUT} = 0\text{ V}$	60	mW Max

NOTES

¹Guaranteed by design.

²Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS (@ $V_s = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	OP77N Limit	Unit
AVERAGE INPUT OFFSET VOLTAGE DRIFT	TCV_{OS}	$R_S = 50\text{ }\Omega$	0.1	$\mu\text{V/}^\circ\text{C}$
NULLED INPUT OFFSET VOLTAGE DRIFT	TCV_{OSn}	$R_S = 50\text{ }\Omega$, $R_p = 20\text{ k}\Omega$	0.1	$\mu\text{V/}^\circ\text{C}$
AVERAGE INPUT OFFSET CURRENT DRIFT	TCI_{OS}		0.5	pA/ $^\circ\text{C}$
SLEW RATE	SR	$R_L \geq 2\text{ k}\Omega$	0.3	V/ μs
BANDWIDTH	BW	$A_{VCL} + 1$	0.6	MHz

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage ²	±22 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J and Z Packages	–65°C to +150°C
Operating Temperature Range	
OP77A	–55°C to +125°C
OP77E, OPP77F (J, Z)	–25°C to +85°C
Junction Temperature (T _j)	–65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES

¹Absolute Maximum Ratings apply to both DICE and packaged parts, unless otherwise noted.

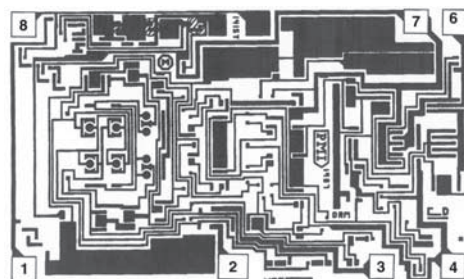
²For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Package Type	θ _{JA} [*]	θ _{JC}	Unit
TO-99 (J)	150	18	°C/W
8-Lead Hermetic DIP (Z)	148	16	°C/W

NOTE

^{*}θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, Cerdip, P-DIP, and PLCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

BONDING DIAGRAM



1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
6. OUTPUT
7. V+
8. BALANCE

DIE SIZE 0.093 × 0.057 inch, 5301 sq. mm
(2.36 × 1.45 mm, 3.42 sq. mm)

ORDERING GUIDE

Package Options		Operating Temperature Range
TO-99	CERDIP [*] 8-Lead	
OP77EJ	OP77AZ	MIL
OP77FJ	OP77EZ	IND
	OP77FZ	IND

^{*}Not for new designs; obsolete April 2002.

For Military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

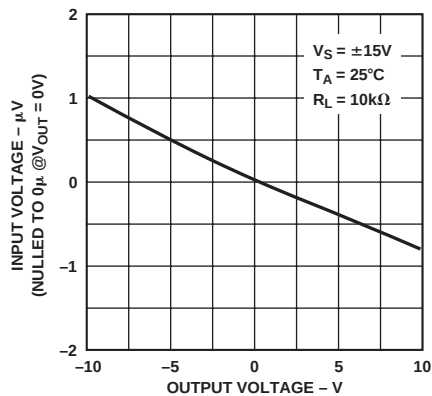
SMD Part Number	ADI Equivalent
5962-87738012A	OP77BRCMDA
5962-8773802GA	OP77AJMDA
5962-8773802PA	OP77AZMDA

CAUTION

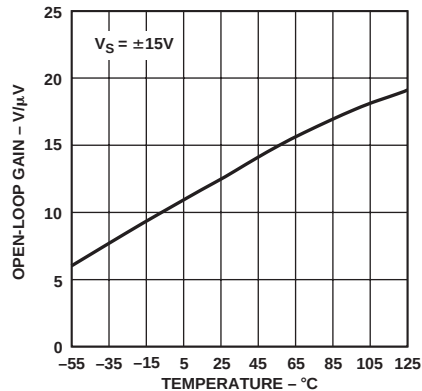
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP77 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



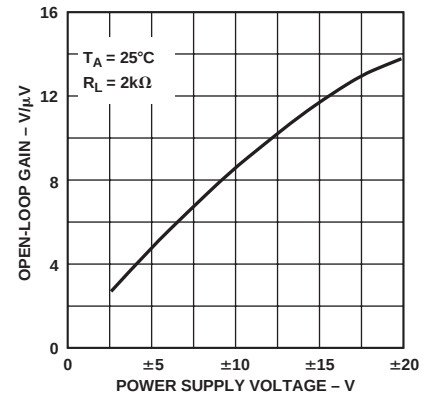
OP77—Typical Performance Characteristics



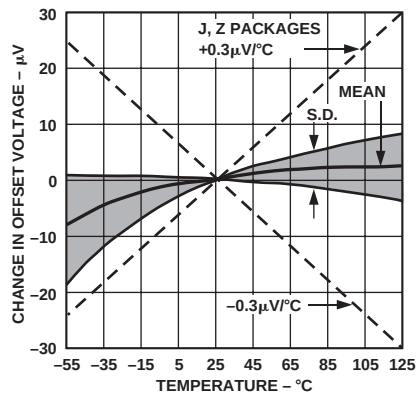
TPC 1. Gain Linearity (Input Voltage vs. Output Voltage)



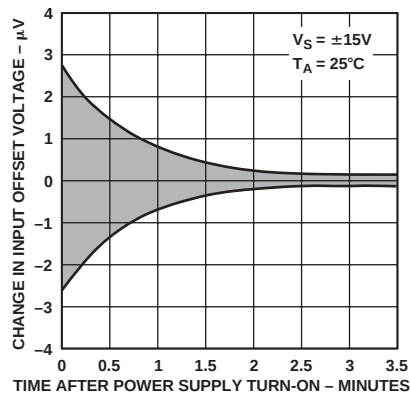
TPC 2. Open-Loop Gain vs. Temperature



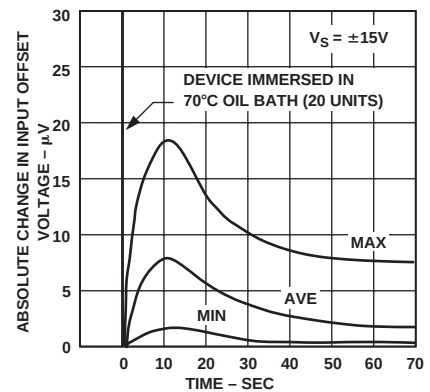
TPC 3. Open-Loop Gain vs. Power Supply Voltage



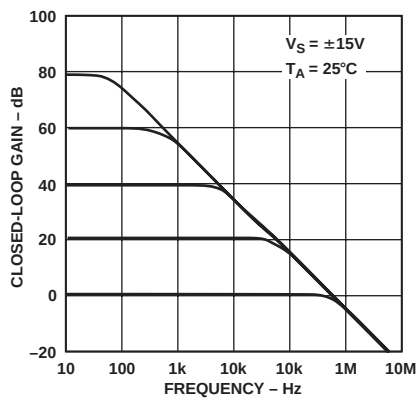
TPC 4. Untrimmed Offset Voltage vs. Temperature



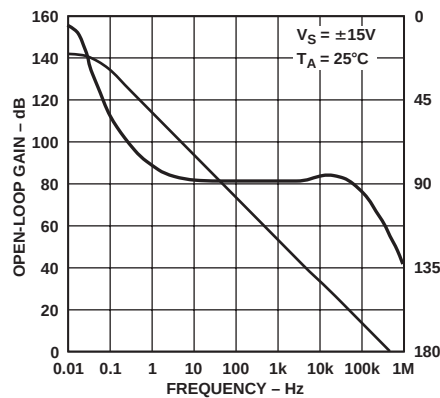
TPC 5. Warm-Up Drift



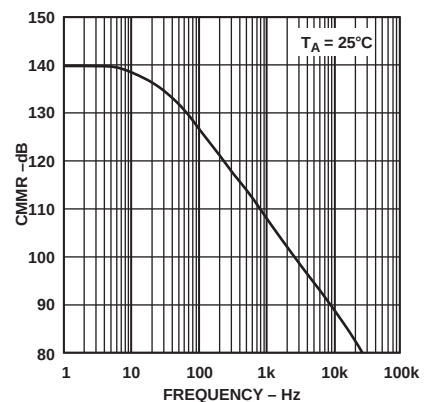
TPC 6. Offset Voltage Change Due to Thermal Shock



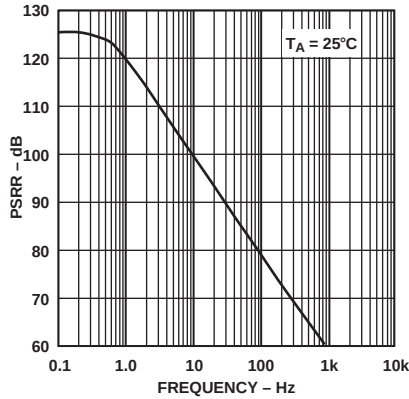
TPC 7. Closed-Loop Response for Various Gain Configurations



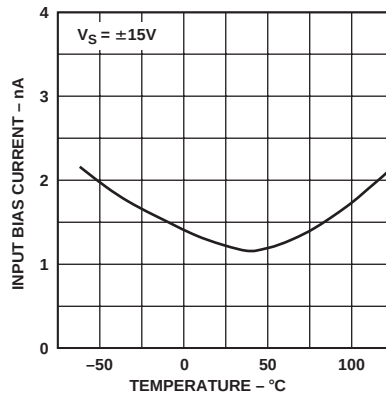
TPC 8. Open-Loop Gain/Phase Response



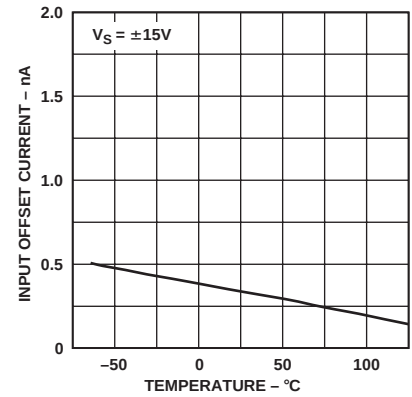
TPC 9. CMRR vs. Frequency



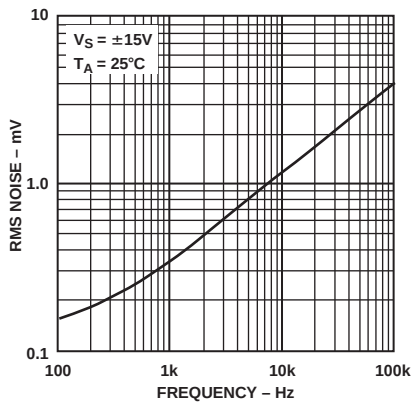
TPC 10. PSRR vs. Frequency



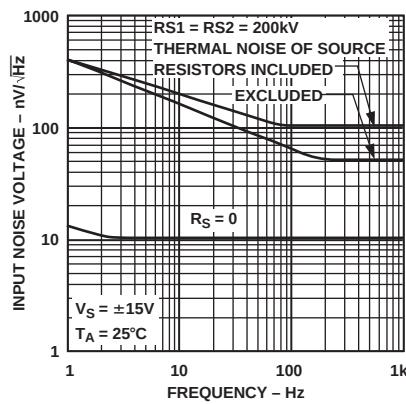
TPC 11. Input Bias Current vs. Temperature



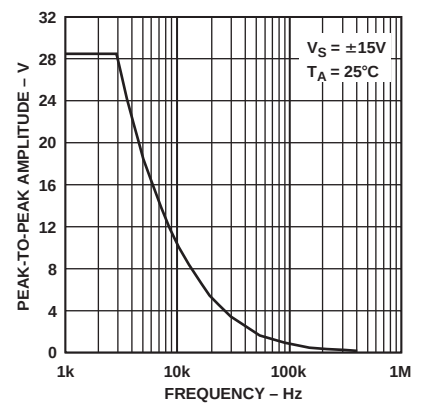
TPC 12. Input Offset Current vs. Temperature



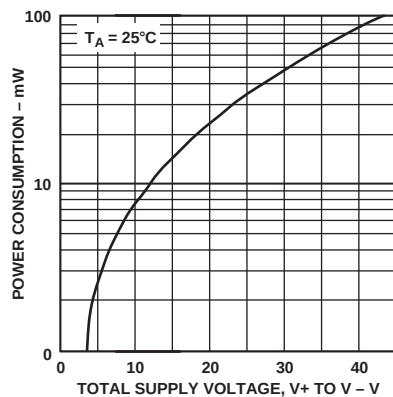
TPC 13. Input Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)



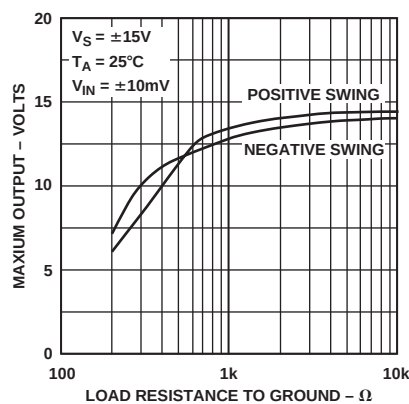
TPC 14. Total Input Noise Voltage vs. Frequency



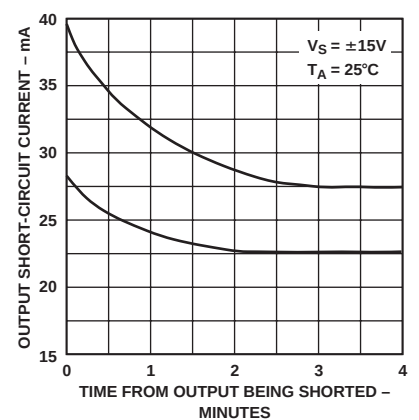
TPC 15. Maximum Output Swing vs. Frequency



TPC 16. Power Consumption vs. Power Supply



TPC 17. Maximum Output Voltage vs. Load Resistance



TPC 18. Output Short-Circuit Current vs. Time

OP77

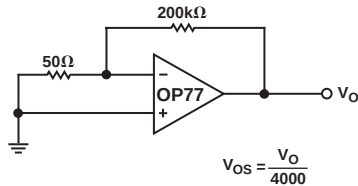


Figure 1. Typical Offset Voltage Test Circuit

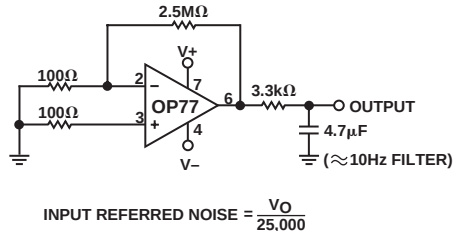


Figure 2. Typical Low-Frequency Noise Test Circuit

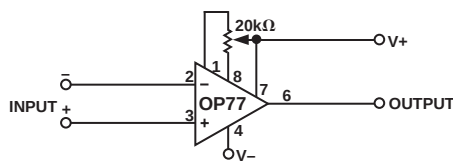


Figure 3. Optional Offset Nulling Circuit

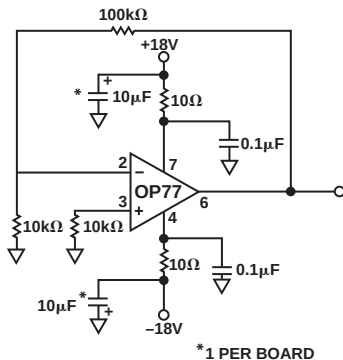
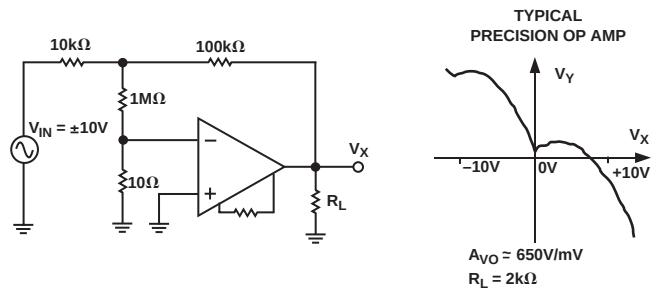


Figure 4. Burn-In Circuit



NOTES

1. GAIN NOT CONSTANT. CAUSES NONLINEAR ERRORS.
2. A_{VO} SPEC IS ONLY PART OF THE SOLUTION.
3. CHECK THE OP AMP PERFORMANCE, ESPECIALLY AT TEMPERATURES.

Figure 5. Open-Loop Gain Linearity

Actual open-loop voltage gain can vary greatly at various output voltages. All automated testers use endpoint testing and therefore only show the average gain. This causes errors in high closed-loop gain circuits. Since this is so difficult for manufacturers to test, users should make their own evaluation. This simple test circuit makes it easy. An ideal op amp would show a horizontal scope trace.

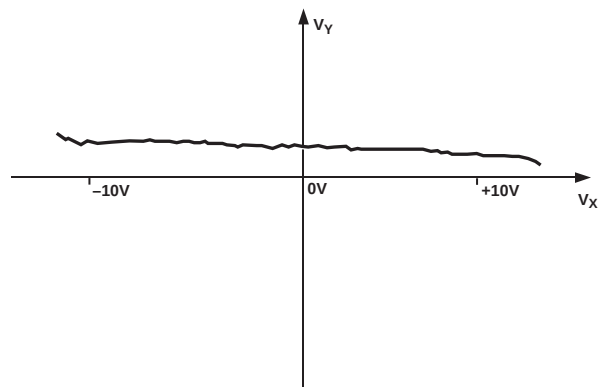


Figure 6. Output Gain Linearity Trace

This is the output gain linearity trace for the new OP77. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. The average open-loop gain is truly impressive—approximately 10,000,000.

APPLICATIONS INFORMATION

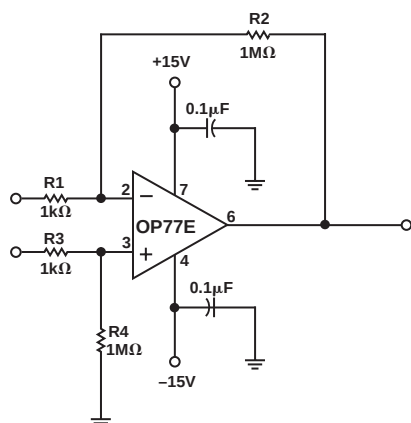


Figure 7. Precision High-Gain Differential Amplifier

The high gain, gain linearity, CMRR, and low TCVOs of the OP77 make it possible to obtain performance not previously available in single-stage very high-gain amplifier applications.

For best CMR, $\frac{R1}{R2}$ must equal $\frac{R3}{R4}$. In this example,

with a 10 mV differential signal, the maximum errors are as listed in Table I.

Table I. Maximum Errors

TYPE	AMOUNT
COMMON-MODE VOLTAGE	0.01%/V
GAIN LINEARITY, WORST CASE	0.02%
TCVOS	0.003%/°C
TCIOS	0.008%/°C

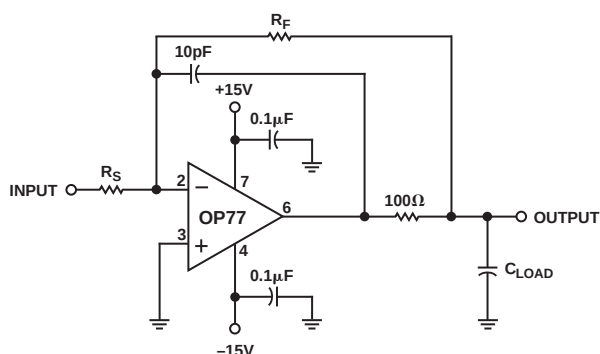


Figure 8. Isolating Large Capacitive Loads

This circuit reduces maximum slew-rate but allows driving capacitive loads of any size without instability. Because the boot resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP77.

Bilateral Current Source

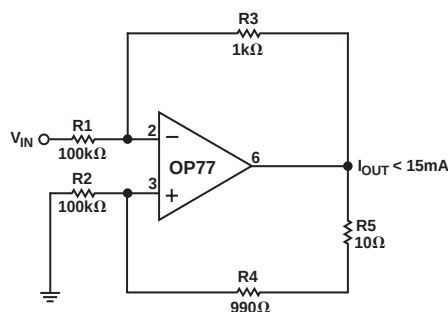


Figure 9. Basic Current Source

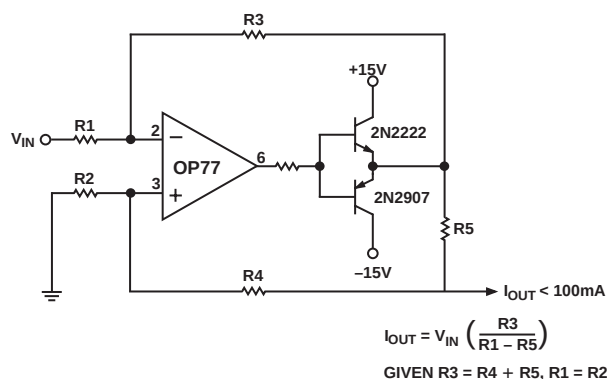


Figure 10. 100 mA Current Source

These current sources will supply both positive and negative current into a grounded load.

$$\text{Note that } Z_O = \frac{R5 \left(\frac{R4}{R2} + 1 \right)}{\frac{R5 + R4}{R2} \frac{R3}{R1}}$$

and that for Z_O to be infinite,

OP77

$$\frac{R5 + R4}{R2} \text{ must} = \frac{R3}{R1}$$

Precision Current Sinks

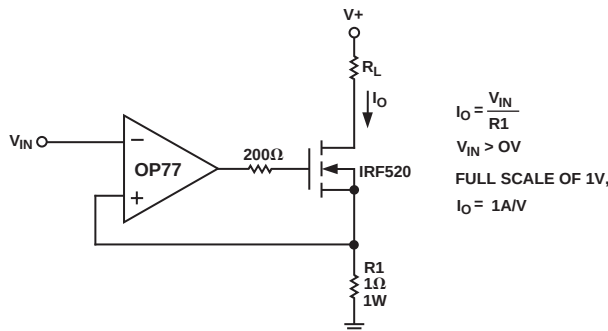


Figure 11. Positive Current Sink

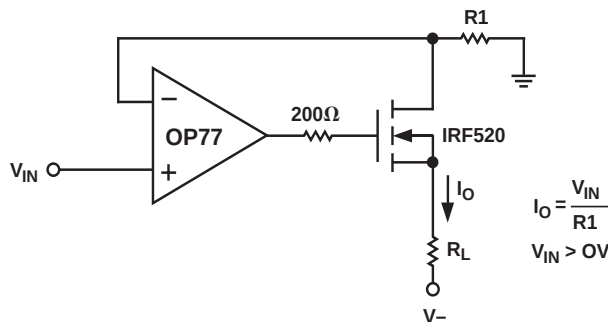


Figure 12. Positive Current Source

These simple high-current sinks require the load to float between the power supply and the sink.

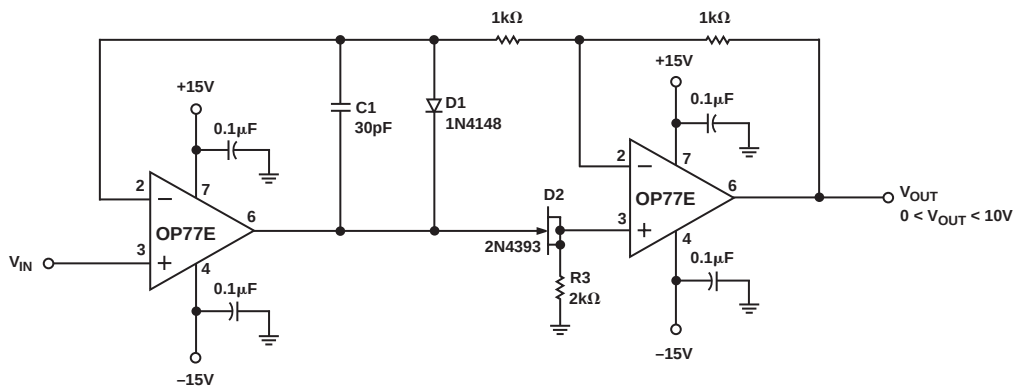


Figure 14. Precision Absolute Value Amplifier

The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always

In these circuits, OP77's high gain, high CMRR, and low TCV_{OS} ensure high accuracy.

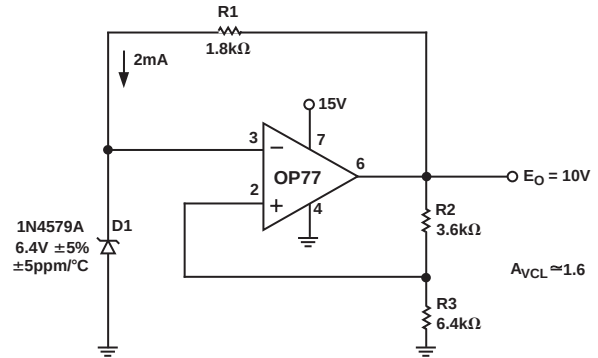


Figure 13. High Stability Voltage Reference

This simple bootstrapped voltage reference provides a precise 10 V virtually independent of changes in power supply voltage, ambient temperature and output loading. Correct Zener operating current of exactly 2 mA is maintained by R1, a selected 5 ppm/°C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: the 5 ppm/°C temperature coefficient of D1, 1 ppm/°C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors.

V_{OS} errors, amplified by 1.6 (A_{VCL}), appear at the output and can be significant with most monolithic amplifiers. For example, an ordinary amplifier with TCV_{OS} of 5 $\mu V/^\circ C$ contributes 0.8 ppm/°C of output error while the OP77, with TCV_{OS} of 0.3 $\mu V/^\circ C$, contributes but 0.05 ppm/°C of output error, thus effectively eliminating TCV_{OS} as an error consideration.

The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always

appears as a common-mode signal to the op amps. The OP77E CMRR of 1 $\mu V/V$ assures errors of less than 2 ppm.

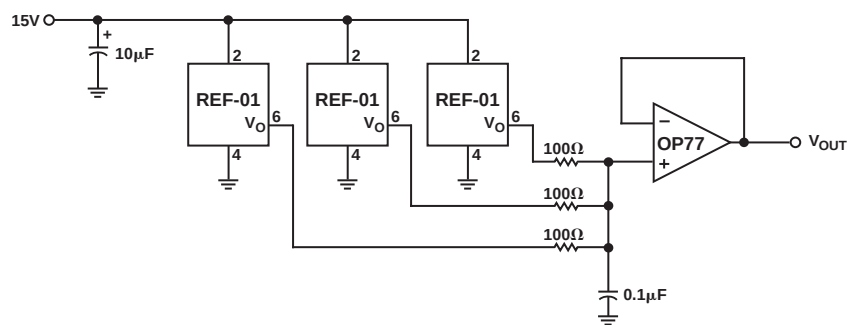


Figure 15. Low Noise Precision Reference

This circuit relies upon OP77's low TCV_{OS} and noise combined with very high CMRR to provide precision buffering of the averaged REF01 voltage outputs.

C_H must be of polystyrene, Teflon*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the AD820.

*Teflon is a registered trademark of the Dupont Company

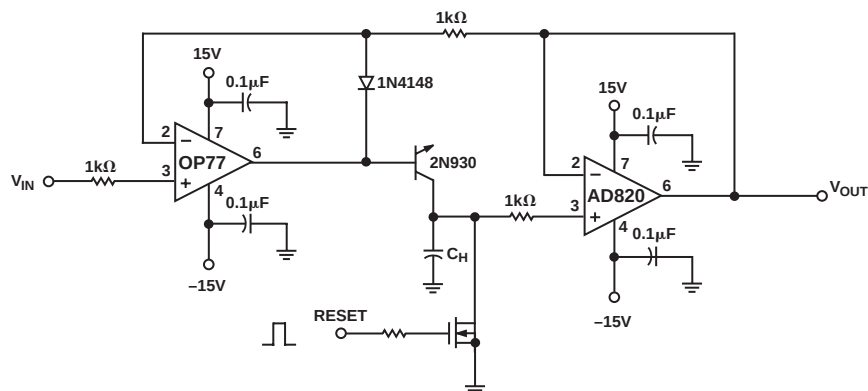


Figure 16. Precision Positive Peak Detector

OP77

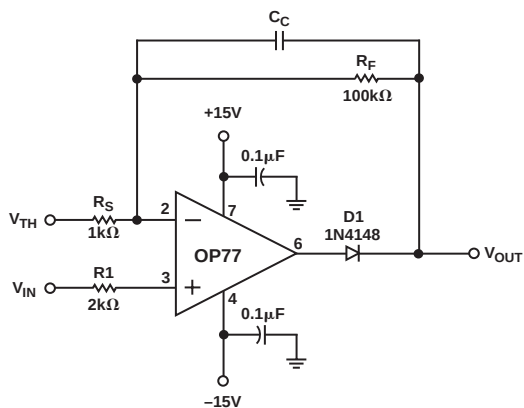


Figure 17. Precision Threshold Detector/Amplifier

When $V_{IN} < V_{TH}$, amplifier output swings negative, reverse biasing diode D1. $V_{OUT} = V_{TH}$ if $R_L = \infty$ when $V_{IN} > V_{TH}$, the loop closes,

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH}) \left(1 + \frac{R_F}{R_S} \right)$$

C_C is selected to smooth the response of the loop.

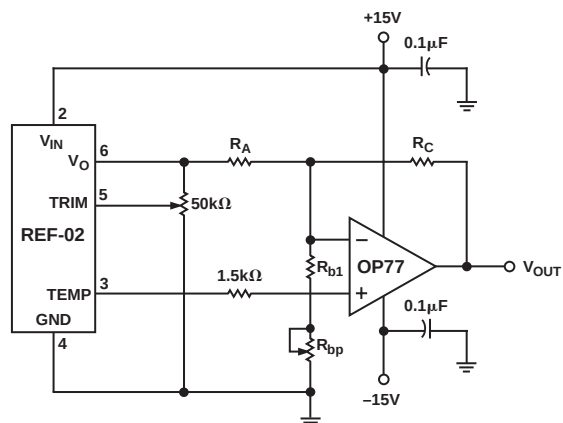


Figure 18. Precision Temperature Sensor

Table II. Resistor Values

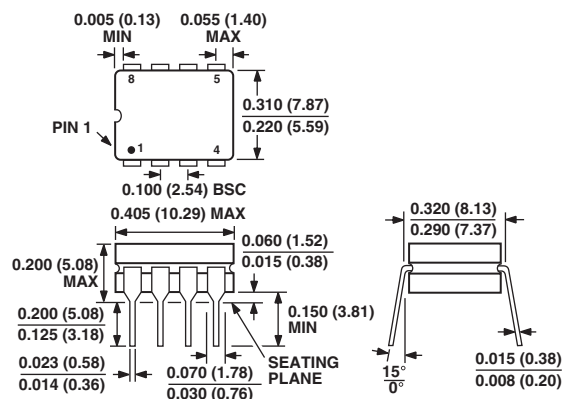
TCV _{OUT} SLOPE (S)	10 mV/°C	100 mV/°C	10 mV/°F
TEMPERATURE RANGE	-55°C to +125°C	-55°C to +125°C	-67°F to +257°C
OUTPUT VOLTAGE RANGE	-0.55 V to +1.25 V	-5.5 V to +12.5V	-0.67 V to +2.57V
ZERO-SCALE	0 V @ 0°C	0 V @ 0°C	0 V @ 0°F
R _a (±1% Resistor)	9.09 kΩ	15 kΩ	7.5 kΩ
R _{b1} (±1% Resistor)	1.5 kΩ	1.82 kΩ	1.21 kΩ
R _{bp} (Potentiometer)	200 Ω	500 Ω	200 Ω
R _c (±1% Resistor)	5.11 kΩ	84.5 kΩ	8.25 kΩ

OUTLINE DIMENSIONS

8-Lead Ceramic Dip – Glass Hermetic Seal [CERDIP]

(Q-8)

Dimensions shown in inches and (millimeters)

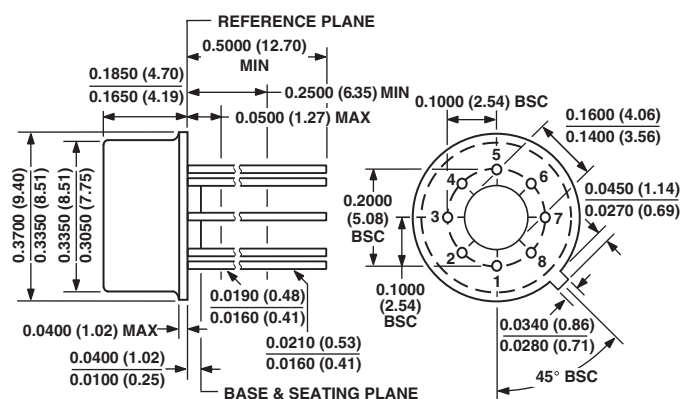


CONTROLLING DIMENSIONS ARE IN INCH; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Metal Can [TO-99]

(H-08)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-002AK
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
10/02—Data Sheet changed from REV. B to REV. C.	
Edits to SPECIFICATIONS	2
Figure 2 Caption Changed	10
Figure 3 Caption Changed	10
Edits to Figure 10	11
Updated OUTLINE DIMENSIONS	15
2/02—Data Sheet changed from REV. A to REV. B.	
Remove 8-Lead SO PIN CONNECTION DIAGRAM	1
Changes to ABSOLUTE MAXIMUM RATINGS	2
Remove OP77B column from SPECIFICATIONS	2
Remove OP77B column from ELECTRICAL CHARACTERISTICS	3–5
Remove OP77G column from WAFER TEST LIMITS	6
Remove OP77G column from TYPICAL ELECTRICAL CHARACTERISTICS	6

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