Functional Description

The functional description gives the necessary formulas to calculate the system. The formulas give a good approximation of the reality.

Reference Oscillator:

The reference oscillator works by charging and discharging the external oscillator capacitor C_{OSC}, the internal parasitic capacitors $C_{OSC,PAR,INT}$ and not forgetting the external parasitic capacitors $C_{OSC,PAR,EXT}$ of the measurement circuit. The external oscillator capacitor C_{OSC} has to be

$$C_{OSC} = 2 \cdot C_{X1} \tag{1}$$

The reference oscillator current I_{OSC} (typ. 10µA) is determined by the external resistor R_{OSC} (typ. 200kΩ) and the reference voltage V_M (typ. 2V):

$$I_{OSC} = \frac{V_M}{R_{OSC}} \tag{2}$$

The frequency of the reference oscillator f_{OSC} is given by

$$f_{OSC} = \frac{K_{OSC} \cdot I_{OSC}}{2 \cdot \left(V_{OSC,HIGH} - V_{OSC,LOW}\right) \cdot \left(C_{OSC} + C_{OSC,PAR,INT} + C_{OSC,PAR,EXT}\right)} \tag{3}$$

whereby $V_{OSC,LOW}$ (typ. 1.6V) and $V_{OSC,HIGH}$ (typ. 3.2V) are the internal threshold voltages of the reference oscillator. The factor K_{OSC} represents the deviation of the ideal oscillator current (in Eq. 2). A value for the internal parasitic capacitor $C_{OSC,PAR,INT}$ is about 6.5pF (simulation result at 25°C).

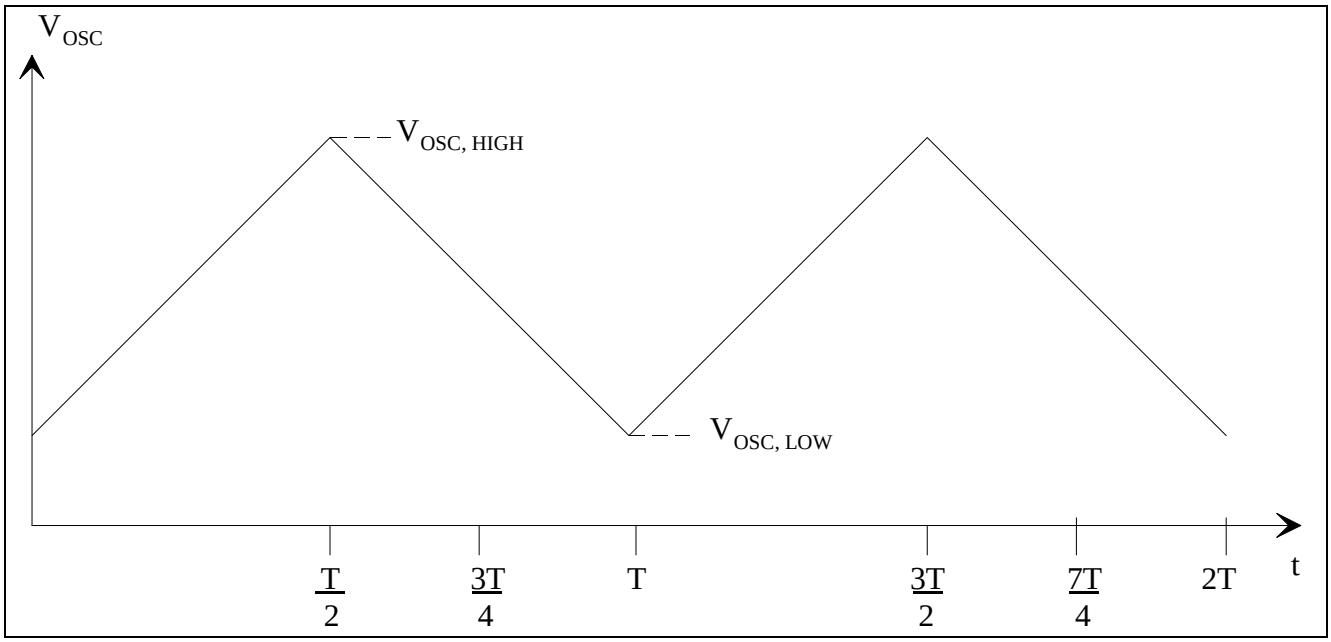

Figure 1

Capacitive Oscillators:

The principle of operation is nearly the same as the behaviour of the reference oscillator. The difference is the time of discharging the capacitors which is twice the time of charging and is clamped at an internal fixed voltage V_{CLAMP} :

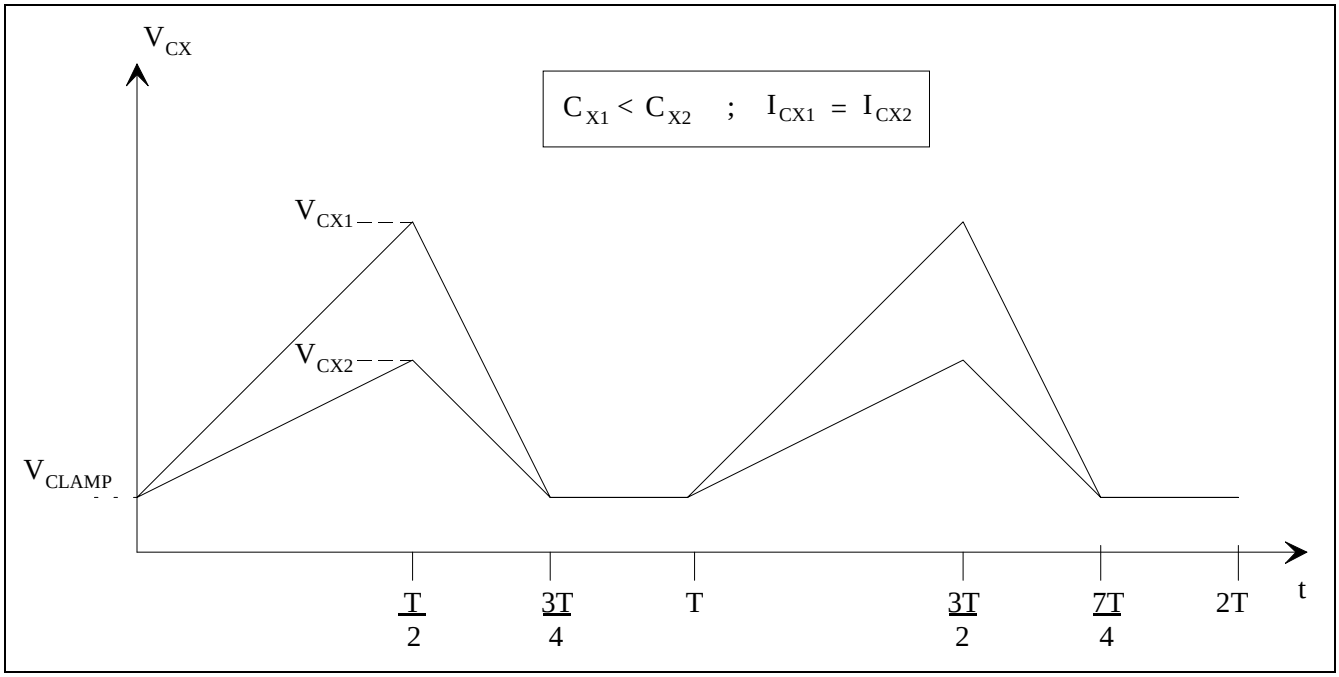

Figure 2

The capacitive oscillator current I_{CX} (typ. 5µA) is determined by the external resistor R_{CX} (typ. 400kΩ) and the reference voltage V_M (typ. 2V):

$$I_{CX} = \frac{V_M}{R_{CX}} \tag{4}$$

The capacitor C_X is charged up to the maximum voltage V_{CX} and can be calculated as follows

$$V_{CX} = \frac{K_{CX} \cdot I_{CX}}{2 \cdot f_{OSC} \cdot \left(C_X + C_{X,PAR,INT} + C_{X,PAR,EXT}\right)} + V_{CLAMP} \tag{5}$$

whereby the value of the internal parasitic capacitor $C_{X,PAR,INT}$ is about 5.5pF (simulation result at 25°C). The factor K_{CX} represents the deviation of the ideal oscillator current (in Eq. 4).

The two voltages over the capacitors C_{X1} and C_{X2} are subtracted and the resulting difference voltage referred to the reference voltage V_M is given by

$$V_{CX,DIFF} = \left(V_{CX1} - V_{CX2}\right) + V_M \tag{6}$$

The difference voltage $V_{CX,DIFF}$ goes directly into the 2nd-order lowpass. The 3dB-corner frequencies f_{C1} and f_{C2} of the two stages are adjusted with the external capacitors C_{L1} and C_{L2} and the internal resistors R_{01} and R_{02} (typ. 20kΩ). The 3dB-corner frequencies have to be chosen in dependence on the reference oscillator frequency f_{OSC} (see Eq. 3) and the desired detection frequency f_{DET} of the entire sensor system. The following relation for the different types of frequencies has to be fulfilled in all cases:

$$f_{DET} < f_C << f_{OSC} \tag{7}$$

The external capacitors for a desired corner frequency are calculated as follows

$$C_L = \frac{1}{2\pi \cdot R_0 \cdot f_C} \tag{8}$$

The output signal of the lowpass with the ideal waveform (shown in Figure 2) becomes

$$V_{LPOUT} = \frac{3}{8} \cdot V_{DIFF} + V_M \tag{9}$$

with

$$V_{DIFF} = \frac{3}{8} \cdot \left(V_{CX1} - V_{CX2}\right) \tag{10}$$

If the output difference voltage V_{DIFF} is too small, it can be amplified with external resistors while using the two internal non-inverting amplifiers of the lowpass.

The maximum amplification of the difference voltage V_{DIFF} is limited by the maximum allowed output voltage V_{LPOUT} (max. 3.3V).

The resulting gain of the two stages is

$$A_{RES} = A_1 \cdot A_2 \tag{11}$$

and thus

$$A_{RES} = \left(1 + \frac{R_{L1}}{R_{L2}}\right) \cdot \left(1 + \frac{R_{L3}}{R_{L4}}\right) \tag{12}$$

Hence it follows for the output signal

$$V_{LPOUT} = \frac{3}{8} \cdot A_{RES} \cdot \left(V_{CX1} - V_{CX2}\right) + V_M \tag{13}$$

The different input bias currents of the amplifiers (caused by the external resistors) force an offset voltage at the input of the amplifiers that is also amplified with the adjusted gain. To reduce the offset voltage, the second stage should have the higher gain

$$A_2 > A_1 \tag{14}$$

A further improvement is to force the same input bias current achieved by an additional resistor R_C . As an example for the first stage, the resistor has to be calculated as follows

$$R_{C1} = R_{01} - \frac{R_{L1} \cdot R_{L2}}{R_{L1} + R_{L2}} \tag{15}$$

The gain of the first stage yield

$$A_1 = \frac{R_{L1} + R_{L2}}{R_{C1} + R_{L2}} \tag{16}$$

The resulting output voltage V_{OUT} is refered to the reference voltage V_M and is given by

$$V_{OUT} = V_{LPOUT} - V_M \tag{17}$$

Example 1

The *Example 1* describes the calculation of a typical application.

The following values are given:

- voltage source V_{CC} : 8.2V
- fixed capacitance C_{X1} : 50pF
- varying capacitance C_{X2} : 48 ... 93pF

Adjustment:

The zero-adjustment is made by the resistors R_{CX1} or R_{CX2} for the case that the varying capacitance has nearly the same (and its smallest) value as the fixed capacitance (C_{X1} = 50pF, C_{X2} = 48pF). Therefore one of this resistors is varied until the output voltage

$$V_{OUT} = V_{LPOUT} - V_M \tag{18}$$

is zero:

$$V_{OUT} = 0 \tag{19}$$

Calculation:

With the equations of the functional description, the following values for the devices can be calculated:

- C_{OSC} : 100pF
- f_{OSC} : 27.3kHz (with $C_{OSC,PAR,EXT}$ = 10pF)
- $V_{CX,DIFF}$: 2.59V (with $C_{X,PAR,EXT}$ = 10pF)
- V_{OUT} : 220mV

The output voltage can be amplified with external resistors (see Eq. 11 – 16) if desired. In this application the gain is

- A_{GES} : 1

The capacitors can be set for the given oscillator frequency f_{OSC} =27.3kHz to:

- C_{L1} , C_{L2} : 10nF ($\rightarrow f_{C1}$ =800Hz)

By increasing the value of the capacitors, the ripple of the filtered output signal and also the detection frequency will be reduced.

Circuit:

The resulting circuit is shown in Figure 3.

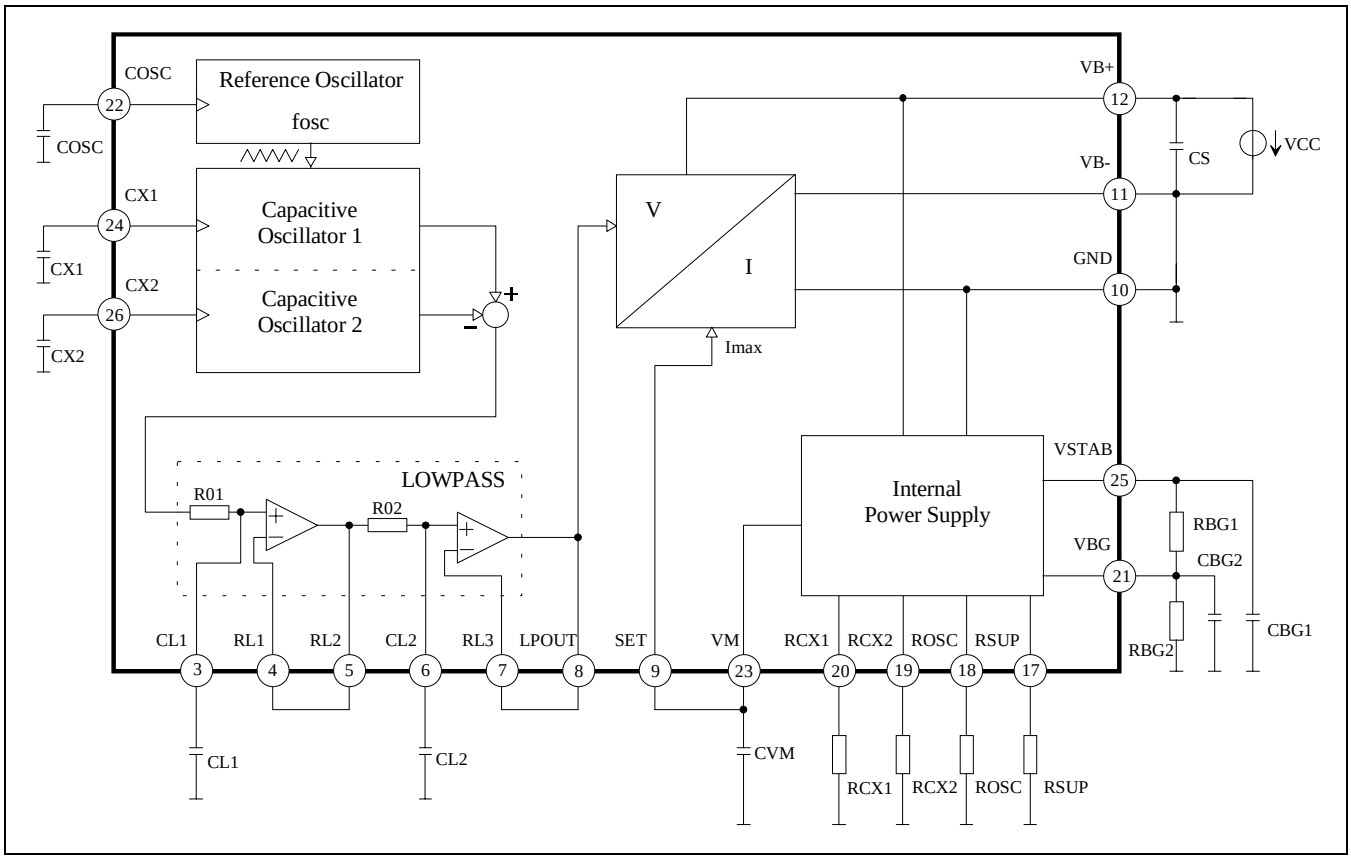

Figure 3

Component List:

Component	Symbol	typ. value	remark
V_M Capacitor	C_{VM}	100nF	
V_{STAB} Capacitor	C_{BG1}	2.2µF	
V_{BG} Capacitor	C_{BG2}	100pF	
V_{CC} Capacitor	C_S	22nF	
Lowpass Capacitor 1	C_{L1}	10nF	
Lowpass Capacitor 2	C_{L2}	10nF	
Oscillator Capacitor	C_{OSC}	100pF	NPO, very small temperature coefficient
Set Resistor 1	R_{CX1}	400kΩ	adjustable, very small temperature coefficient
Set Resistor 2	R_{CX2}	400kΩ	adjustable, very small temperature coefficient
Set Resistor 3	R_{OSC}	200kΩ	very small temperature coefficient
Set Resistor 4	R_{SUP}	400kΩ	very small temperature coefficient
Set Resistor 5	R_{BG1}	249kΩ	small temperature coefficient
Set Resistor 6	R_{BG2}	100kΩ	small temperature coefficient

For the performance of the entire system it is important that all *Set Resistors* have to have a small temperature coefficient. An offset compensation over temperature can only be achieved by choosing the resistors R_{CX1} and R_{CX2} with the same temperature coefficient and a very close placement of them in the entire circuit.

Example 2: Namur

The *Example 2* describes the calculation of the Namur stage. Figure 4 shows the typical 2-wire Namur application.

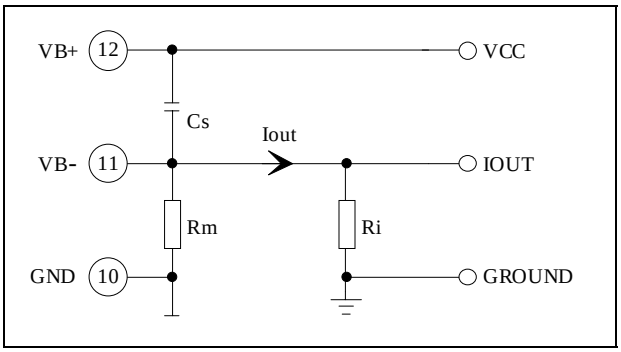

Figure 4

Adjustment:

The Namur stage is adjusted with the given values of

$$V_{LPOUT,\min} = V_M \qquad \text{(at } C_{X1} = C_{X2} \text{ and } \Delta C_{X,\max} = 0\text{)}$$

$$V_{LPOUT,\max} = \frac{3}{8} \cdot A_{RES} \cdot \left(V_{CX1} - V_{CX2}\right) + V_M \qquad \text{(at } C_{X1} \neq C_{X2} \text{ and } \Delta C_{X,\max} = \left(C_{X2} - C_{X1}\right) / C_{X1}\text{)}$$

The gain A_{RES} has to be chosen in the way that the output voltage is

$V_{LPOUT,max}$ = 3.2V

and the maximum current for this voltage has to be

$I_{CC,\max}$ = 2.5mA

1. Connect the Pin V_{SET} with the Pin V_M and make R_M to zero:

   $$V_{SET} = V_M$$

   and

   $$R_M = 0$$

   The measured supply current I_{CC} under this condition represents the value of $I_{CC,min}$.

2. Calculating the resistor R_M

   $$R_M = \frac{V_{LPOUT,\max} - V_{LPOUT,\min}}{10 \cdot \left(I_{CC,\max} - I_{CC,\min}\right)}$$

3. Calculating the voltage V_{SET}

   $$V_{SET} = \frac{1}{11} \cdot \left(V_{LPOUT,\min} - 10 \cdot R_M \cdot I_{CC,\min}\right)$$

   The voltage V_{SET} is adjusted by the resistors R_{N1} and R_{N2} :

   $$\frac{R_{N1}}{R_{N2}} = \frac{V_M}{V_{SET}} - 1$$

Example:

$V_{LPOUT,min} = V_M$ = 2V

$V_{LPOUT,max}$ = 3.2V

$I_{CC,min}$ = 1mA (given by point 1)

$I_{CC,max}$ = 2.5mA

The calculation yields

R_M = 80Ω (given by point 2)

V_{SET} = 109,1mV (given by point 3)

R_{N2} = 5,455kΩ (with R_{N1} = 100kΩ)

The resulting circuit is shown in Figure 5.

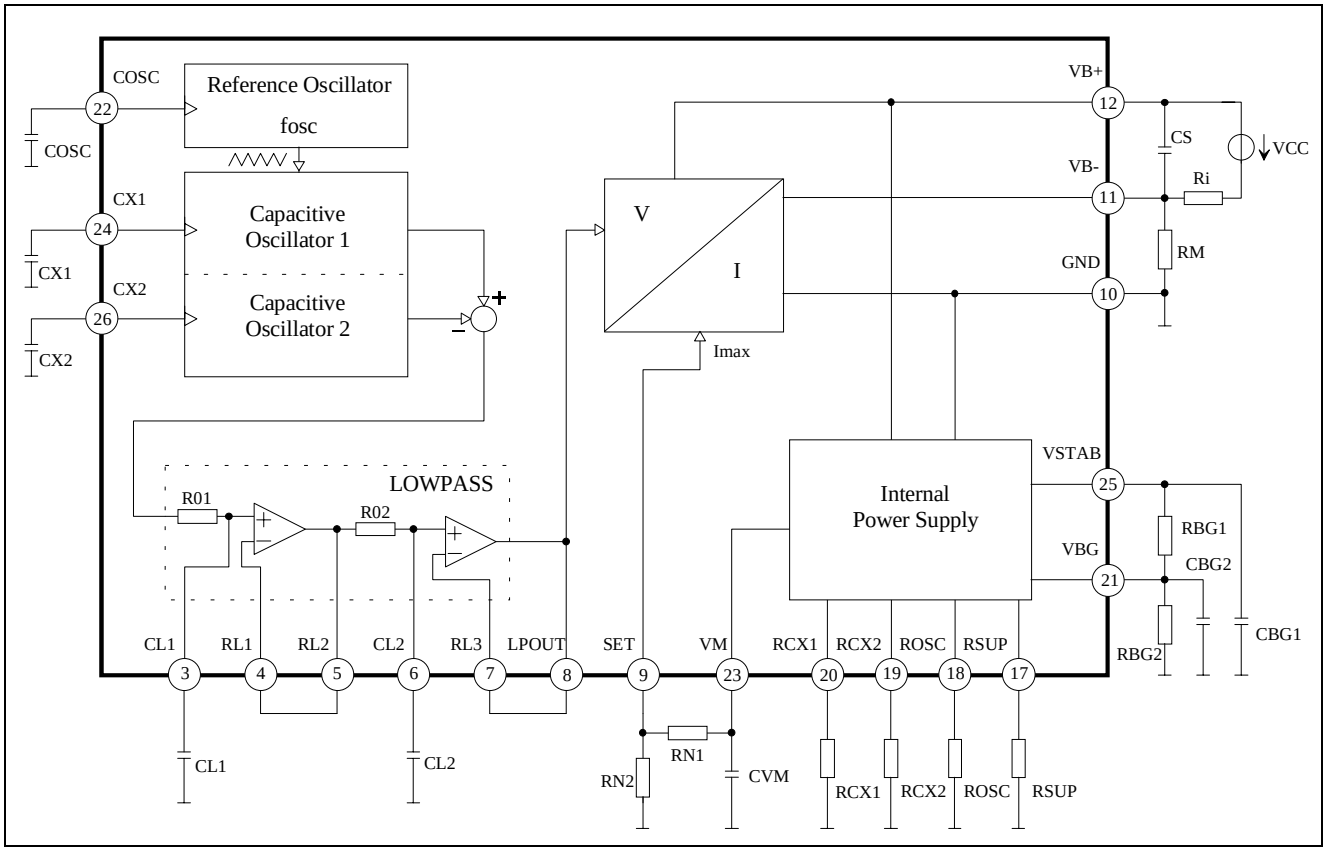

Figure 5