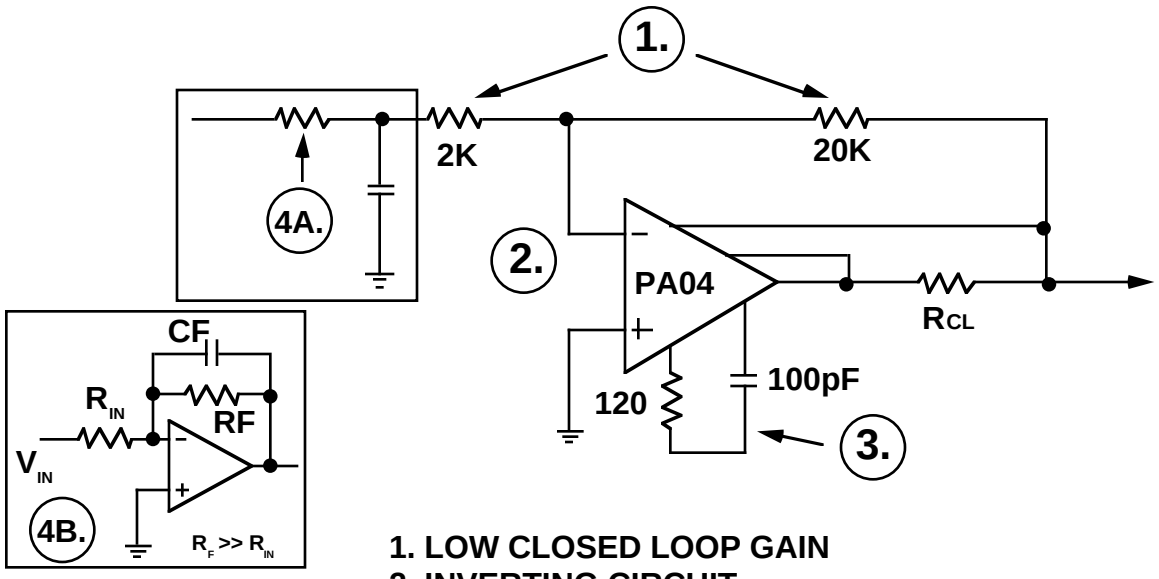
HIGH POWER TECHNIQUES

WIDE BAND - LOW DISTORTION DESIGN



1. LOW CLOSED LOOP GAIN
2. INVERTING CIRCUIT
3. EXTERNAL PHASE COMP
4. SLEW LIMITING

When audio or ATE applications demand the best in distortion and bandwidth, there are four basic rules to follow:

1. Low closed loop gain insures maximum reduction of distortion because of increased loop gain. However, the heavy negative feedback can cause transient response problems during rapid transitions (slew rate overload). Rule #4 will show how to solve the transient response problem.

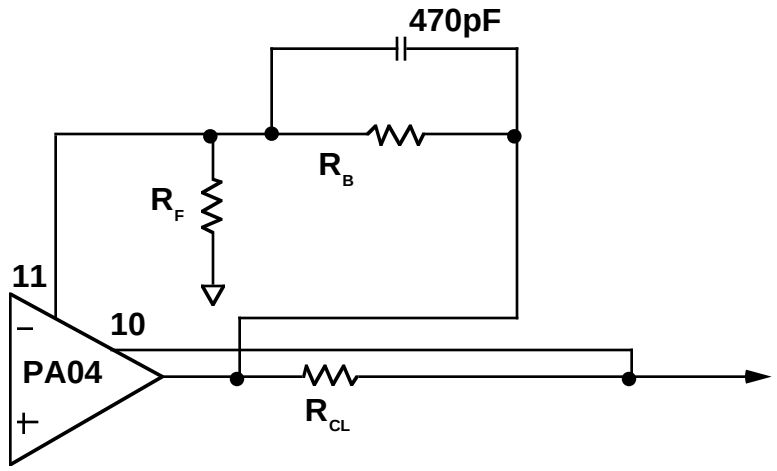
2. The inverting configuration, by forcing both inputs to 0 (remember your basic op amp theory), eliminates common mode signals and the errors (read: nonlinearities) that they cause.

3. External phase compensation allows the designer to tailor the circuit to the minimum acceptable compensation. This increases high frequency loop gain to further reduce distortion, especially at high frequencies. Consider noise gain compensation to improve stability for low gain and small compensation capacitors.

4. Input slew rate limiting (4A) designed to keep input signal transitions within the slew rate limit of the amplifier will eliminate transient overload problems. 4B) You may use an integrator to accomplish this function, while R_F/R_I pre-amplifies the input signal to accomodate a low powerstage gain. Then $C_F = V_{IN}/R_{IN} \bullet A_{CL}/SR$.

FOLD OVER CURRENT LIMITING FOR PA04

DOUBLES
I_{CL} AT V_O MAX



$R_B = 270\ \Omega$ $\qquad R_F = \frac{Vs}{0.0025}$

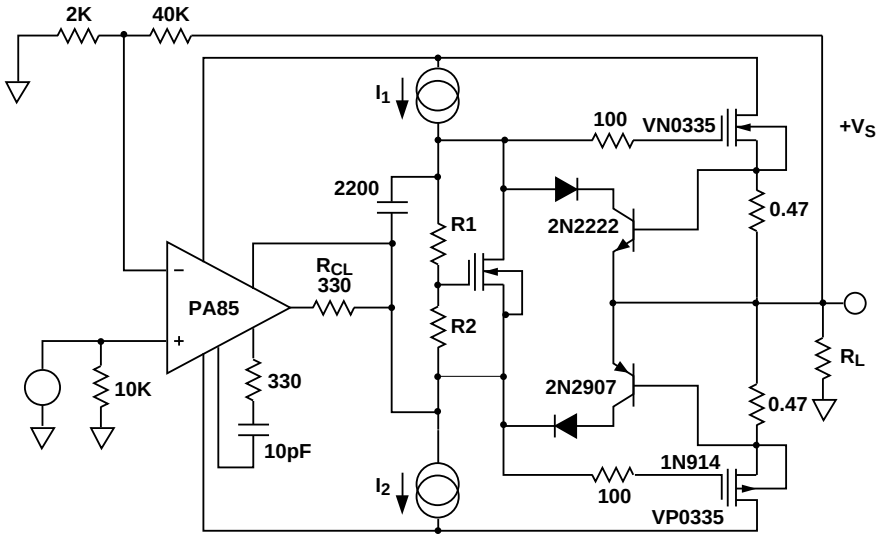
$R_{CL} = \frac{0.7}{I_{CL}}$ for 0 V_{out}

The four wire current limit of PA04 is easily adapted to foldover current limiting with the addition of two external resistors.

This effectively doubles current available at full output swing compared to current available at 0 V out.

This provides an extra margin of safety in audio applications.

COMPLIMENTARY MOSFET BUFFERS



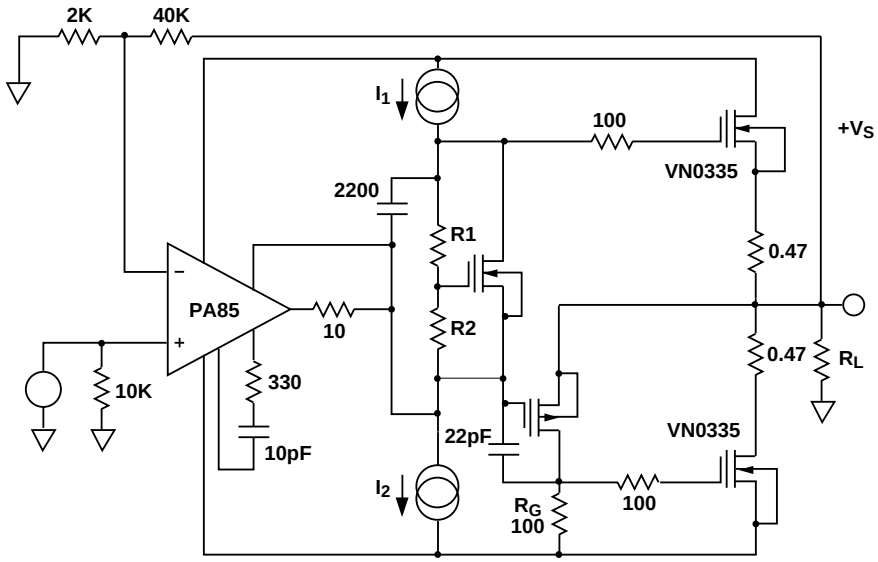
The high power ring generator was able use a simplified version of this slide with no attempt to establish class A/B bias in the MOSFET output stage. In that circuit with no bias, the typical MOSFET threshold of 3V means the op amp must swing 6V during the crossover transition while the final output does not move. The additional circuitry used here will lower distortion and is increasingly important as frequency goes up. Distortion improvements better than an order of magnitude have been achieved.

As most power MOSFET data sheets provide little data on VGS variations at low currents over temperature, it facilitates the design process to have curve tracer data over the temperature range of interest. Design the VGS multiplier empirically. Current sources of 5mA and splitting the current equally between the resistors and the MOSFET area good starting points. Decreasing current in the MOSFET will increase the multiplier TC. Typical designs requiring low distortion will be set up to obtain 2mA or less bias in the output stage. The trade offs are more distortion with low current and danger of thermal runaway on the high end. Be absolutely sure to guardband your high end temperature. The circuit shown here is capable of distortion below .05% at 50KHz and is thermally stable (flat or negative TC of current in the output stage) over the range of -25° to 85°C.

Note that any multiplier voltage at all reduces distortion. Successful designs have even reduced the multiplier circuit to just a diode connected MOSFET. Do NOT use bipolar transistors or diodes for this biasing. Their TCs do not match those of the MOSFETs.

The 100Ω gate resistors prevent local output stage oscillations. It is important they be physically close to the MOSFETs.

QUASI-COMPLIMENTARY MOSFET BUFFERS



Above 300V p-channel high power MOSFETs can be difficult to find. An alternative is to use a quasi-complementary connection on the negative side. Since the required gate drive voltage of the output device appears across RG, its value will set the maximum current through the p-channel MOSFET. Typical maximum gate drive requirements are 10V. This circuit has demonstrated a slew rate of 360V/µs. A second disadvantage of the quasi-complementary design is higher saturation voltage to the negative rail because two gate-source voltages are stacked between the rail and the output.

Connecting the op amp to the top side of the multiplier helps a little but both buffer design approaches can benefit from having the high voltage op amp operate on higher supply rails than the high power MOSFETs. This improves efficiency by allowing better saturation of the buffers.

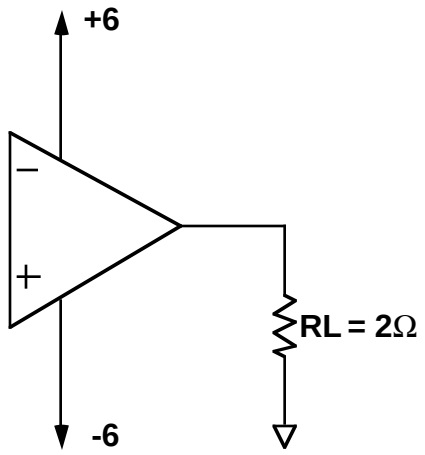
Design criteria for the current sources, current limiters (not shown here) and multiplier are the same as with the complementary version. It is possible to omit one of the current sources in these circuits. However, this places an added heat burden on the high voltage op amp because the entire current of the remaining source must flow through it. When calculating this added dissipation, use the current and the total supply voltage. When both current sources are used the op amp need only make up the difference between them.

BRIDGE POWER CALCULATION

$P_{D\,MAX}$ **FOR EACH AMP:**

$$\frac{2V_S^2}{\pi^2 R_L} = 3.6W$$

TOTAL DISSIPATION = 7.2W



There are several formulae available for calculating worst case power dissipation in a power amplifier (refer to APEX catalog “General Operating Considerations” as well as previous seminar text). These formulae are based on a power op amp using bipolar, symmetrical supplies. The worst case power dissipation formula for driving a resistive load with a sinewave is shown above.

Visualize a PA21 Audio Bridge on a single 12V supply. We wish to calculate the worst case power dissipation for each half of the PA21. We can use the generic power dissipation formula we already have by modifying how we look at each half of the single supply bridge.

Since each half of the bridge swings +/–6V (neglecting saturation voltage) around the 6V midpoint of the power supply, it is equivalent to powering the amplifier from +/–6V with the output swinging symmetrically about zero.

The load itself was given as 4 ohms. In our equivalent model, using +/-6V supplies, for power dissipation calculations we will use one-half of the original load. In the bridge circuit, as the output of the master amplifier swings 1V above the midpoint of the power supply, the output of the slave amplifier swings 1V below the midpoint of the power supply. Across the load then appears twice the voltage output from either amplifier. This doubling of the voltage will double the current driven out from each amplifier. Another way to view this is that each amplifier sees one-half the original load value.

Now our single supply bridge model for power dissipation calculations using symmetrical power supply dissipation equations is complete. Power dissipation for each half of the PA21 is computed to be 7.2W with a total package power dissipation of 14.4W.

HIGH POWER AUDIO DESIGN

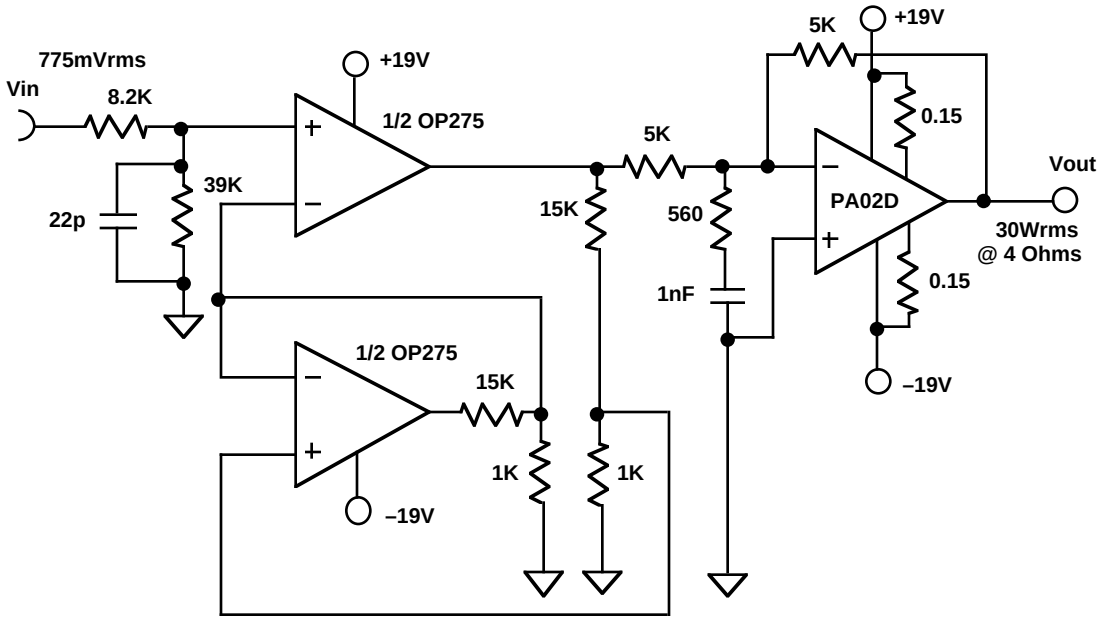
Apex Part #	Preferred Application	Notes
PA02D	Hi-Fi Home Theatre	Bipolar medium power, low distortion
PA03	High Power PA Systems	Bipolar, highest power dissipation
PA04	70V Line Driver, High Power	Fast Power MOSFET Design
PA05	High Power, Wide Bandwidth	Fastest Power MOSFET Design
PA12	Medium Power, subwoofer	Bipolar, High Current
PA26	Home Theatre, Car Audio	Bipolar, low power, low cost bridge
PA41/42/43	MOSFET driver, subwoofer	low cost monolithic MOSFET design
PA85	Fastest Power MOSFET driver	MOSFET Design, Lowest Distortion
PB58	70V Line Driver	MOSFET Booster, Composite Amplifier[1]

[1] Composite Amplifier: See Apex Application Notes 14 and 25 for details.

Audio applications demand both high power output and low distortion. Due to the internal high open loop gain, Apex Power Operational Amplifiers are well suited for this application. Output power is a function of supply voltage and load impedance. Bridge circuit designs almost quadruple output power, as long as the current rating of the amplifier is sufficient. Additionally, this circuit topology avoids GND power returns, which reduces common mode signals. The list above shows preferred Apex op amps for audio design.

The schematic on page 141B features an active feedback technique, which reduces phase shift. One half of a dual monolithic amplifier pre-amplifies the input signal, while the other half compensates the poles and zeros of the first one. Accurate gain matching is as important as the application of a dual amplifier, rather than two individual amps. The key is that as loop gain drops, the differential input voltage is increasing equally for either op amp. The OP275 features extremely low distortion when Vs approaches its maximum rating, while the quiescent current of the PA02D is trimmed for minimum distortion as well. Here are design rules to get optimum audio performance out of Apex power operational amplifiers. In all cases, protection diodes for input, output, and power supplies are recommended. Please consult the “General Operation Considerations” in our Vol. VI data book. Read App Note #19 for a detailed analysis of stability. App Note #25 and our note on “High Voltage Op Amps Driving Power MOSFETs” provide further information on how to apply our PA41/42/43 and PA85 to high power applications.

HIGH POWER AUDIO DESIGN



1. USE MINIMUM GAIN

The difference between open loop and closed loop gain is called loop gain. This is the power the amplifier has available to control the output signal. Lower gain settings will improve distortion and signal accuracy. The accomplish this, you may need a low noise small-signal front end amplifier, such as the ultra-low distortion OP275 dual amplifier, operating of a regulated ±19V supply voltage. This amplifier provides ±15 V input voltage to the PA02D, reducing the minimum gain requirement to A = –1. The second amplifier I recommend to apply as outlined in the schematic to reduce phase shift at high frequencies.

2. USE INVERTING MODE CONFIGURATION

This gives you virtually zero volt common mode contribution to the output signal, because the non-inverting node is connected to GND. Since input bias currents have dropped down to the sub-nA range, discard bias current resistors. They would rather add common mode signals than reduce offset errors. In case you have a single amplifier configuration (in contrast to bridge mode), you may set up a differential amplifier to compensate for voltage drops on the output lines. This is also called “remote sense”.

3. LOW PASS FILTER YOUR INPUT SIGNAL

This avoids TIM distortion related to the amplifier’s slew rate limit. An active or passive low pass filter or an integrating amplifier ensures, that the input stage of the main power amplifier will never saturate. The maximum input signal slew rate is the main amplifier slew rate divided by its signal gain. The low pass filter crossover frequency then is:

$$flp = SR/(2*pi*Vin)$$

According to i/C=du/dt, the feedback capacitor of the integrator will be:

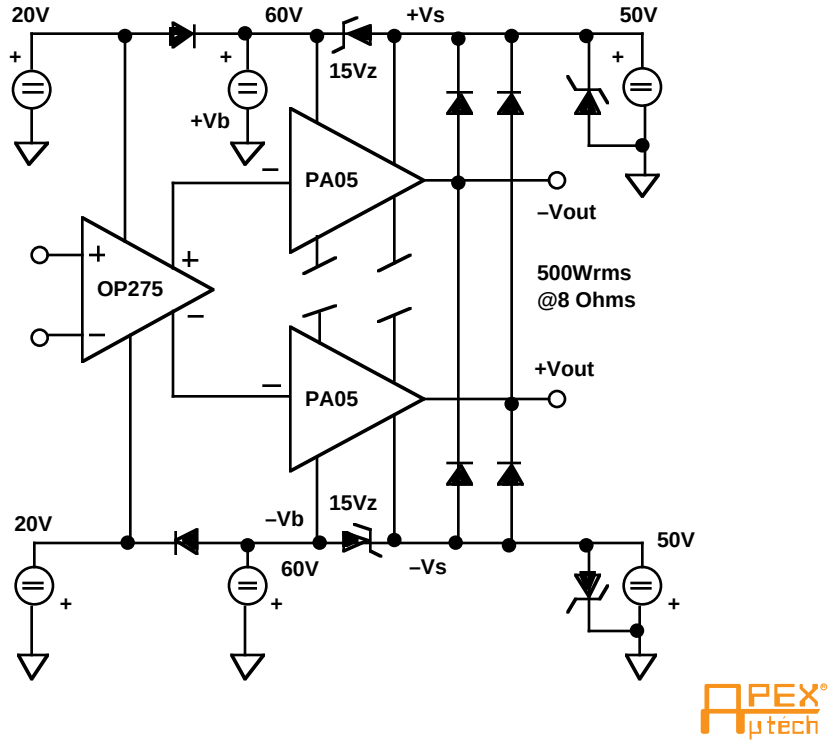
$$Cf = Vin/(Ri*du/dt)$$

Slew rate (SR) calculates to:

$$SR=2*pi*f*Vout/1E6\ [V/\mu s]$$

The PA05 will offer a power bandwidth of approximately 200 kHz. For lower output voltage swings, the power bandwidth is increased accordingly. Note, that slew rate is a large signal parameter. If loop gain drops below 20dB, the amplifier will start to roll-off, regardless of output voltage swing.

HIGH POWER AUDIO DESIGN



4. MINIMIZE COMPENSATION CAPACITANCE

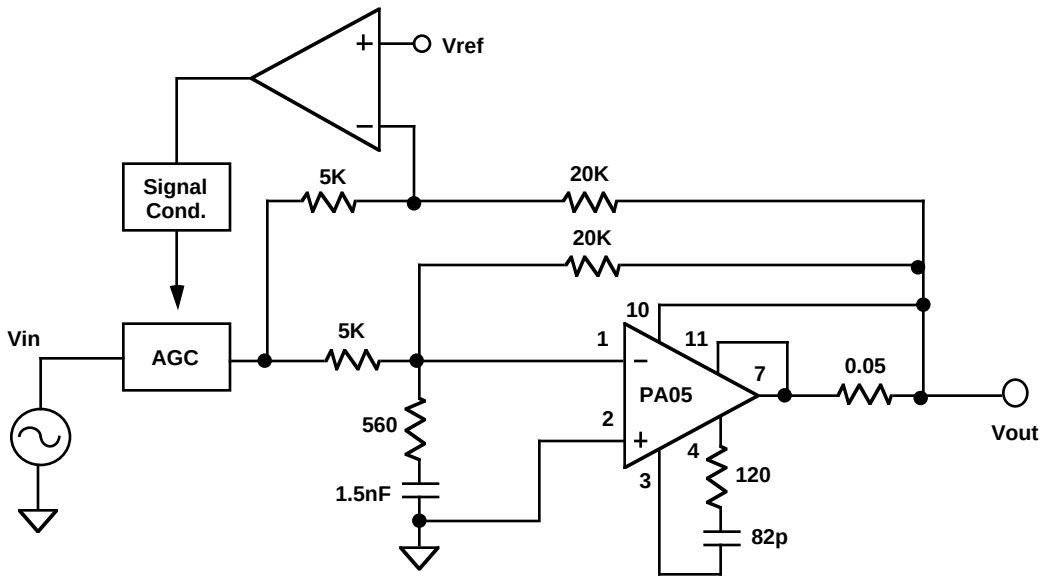
The lower the compensation capacitance (Cc), the higher the amplifiers slew rate. The small-signal open loop gain graph shows, that additionally a smaller size Cc increases the unity gain bandwidth. However, if the capacitors are omitted, overshoot and ringing may occur, dependent on the gain setting and load capacitance. Use additional compensation techniques, such as “noise gain” compensation, to restore stability.

5. VBOOST SUPPLIES

Because of power supply line modulation, prefer regulated power supplies at the Vboost terminals of the PA04 and PA05. Vboost is typically 5V to 10V above the main power supply (Vs) and enhances the output voltage swing. It allows the driver to deliver a higher Vgs voltage to the output MOSFETs, which lowers saturation voltage and improves current output. However, to ensure proper operation of the PA05 thermally limited output stage, supply a minimum of ±15 V. If you use a fixed rather than a floating Vboost supply, apply zener diodes to ensure, that Vboost <=Vs+20V at all times.

The circuit above depicts a high power, wide bandwidth topology, delivering 500Wrms into a 8 Ohm load. It uses a differential input stage, which accepts symmetric (XLR) as well as asymmetric (Chinch/DIN) inputs and a differential output configuration, which provides freedom from GND (floating load). Both PA05 are compensated with the same low compensation capacitor value for maximum slew rate. In contrast to the master-slave configuration (the slave is an inverting buffer), each PA05 is driven simultaneously: there is no delay time between either amplifier’s output signal. Noise gain compensation improves stability at low signal gain settings. For details around the PA05 peripheral components, please refer to the following circuit diagram.

HIGH POWER AUDIO DESIGN



AGC: Automatic Gain Control, i.e., SSM2013

6. SHUTDOWN

Use the shutdown terminal(s) to avoid the “turn-on pop”. All Apex Power Dip amplifiers (PA03, PA04, PA05) are equipped with this feature. A fault condition instantaneously causes non-linear operation, leading to differential input voltage. Use a comparator and a latch to shut down the amplifier.

7. THERMAL LIMIT

In case of overload, the thermally limited output stage of the PA05 and the PA03 will limit the output current, thus leading to visible and audible distortion. If this distortion is measured and relayed to an AGC (automatic gain control) unit, maximum power can be delivered to any load. Use the “false summing node technique” to track linear operation of the amplifier. This safety feature allows much higher power levels and still provides output stage protection. The PA05 will likely withstand short circuits to GND, when its current limit is set below 15A!

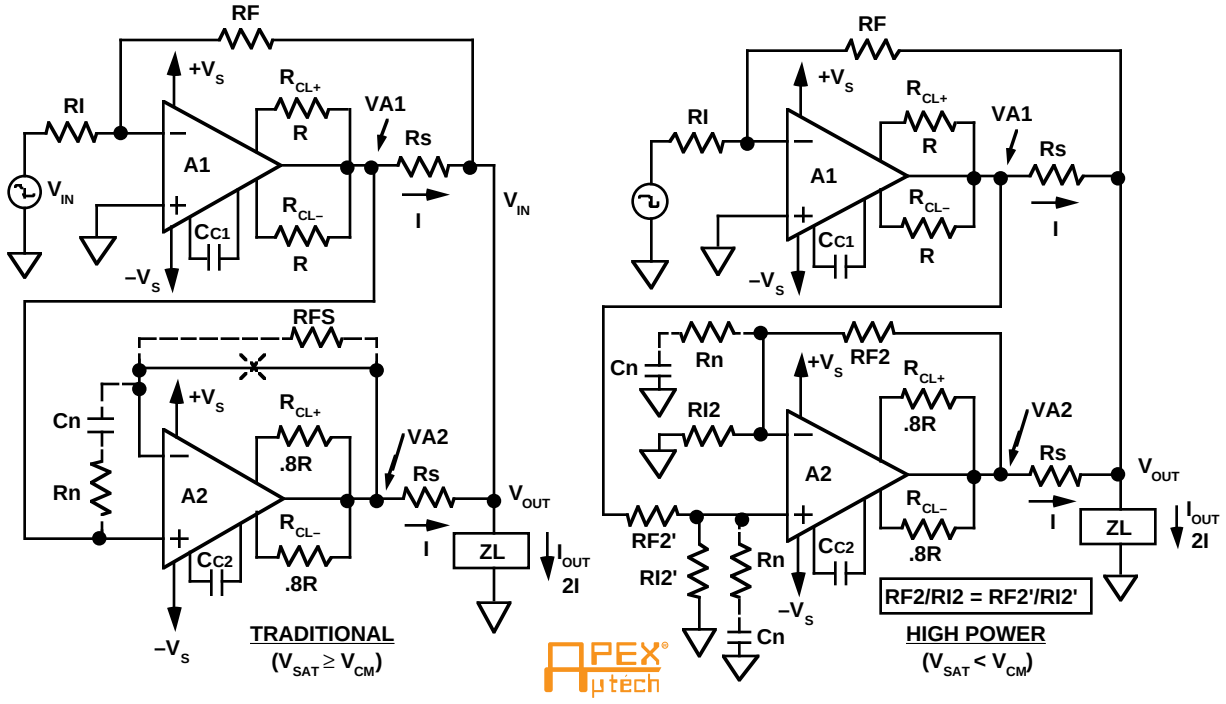
8. HEATSINKING

Loudspeakers can represent a complex impedance with up to 60 degrees load phase angle (typ. phi = 45°). At high power levels, the reactive component will lead to a fair amount of power being dissipated in the amplifier. Use the largest possible heatsink, that your real estate allows for. Consider heat pipes and / or forced air cooling to improve thermal conductivity. This is especially important for rack mounted amplifiers, which are subject to higher internal ambient temperatures, typically 15° to 20° above room temperature. Worst case power dissipation for linear operation is:

$Pd = Vs^2/(2*Zsp)*[4/pi - \cos(phi)]$; Zsp = speaker impedance.

Custom heatsinks must have a flatness equal or better 1mil/inch. Drill individual holes for each pin and use either our thermal washers (TW03, TW05, or TW12) or thermal grease. Stir well before applying the thermal grease, since aging causes sedimentation and those particles will ruin the flatness.

PARALLEL OPERATION



GENERAL COMMENTS:

Occasionally it is desired to extend the SOA of a power op amp or provide higher currents to a load than the amplifier is capable of delivering on its own. Sometimes it is more cost effective to use power op amps in parallel rather than to select a larger power op amp.

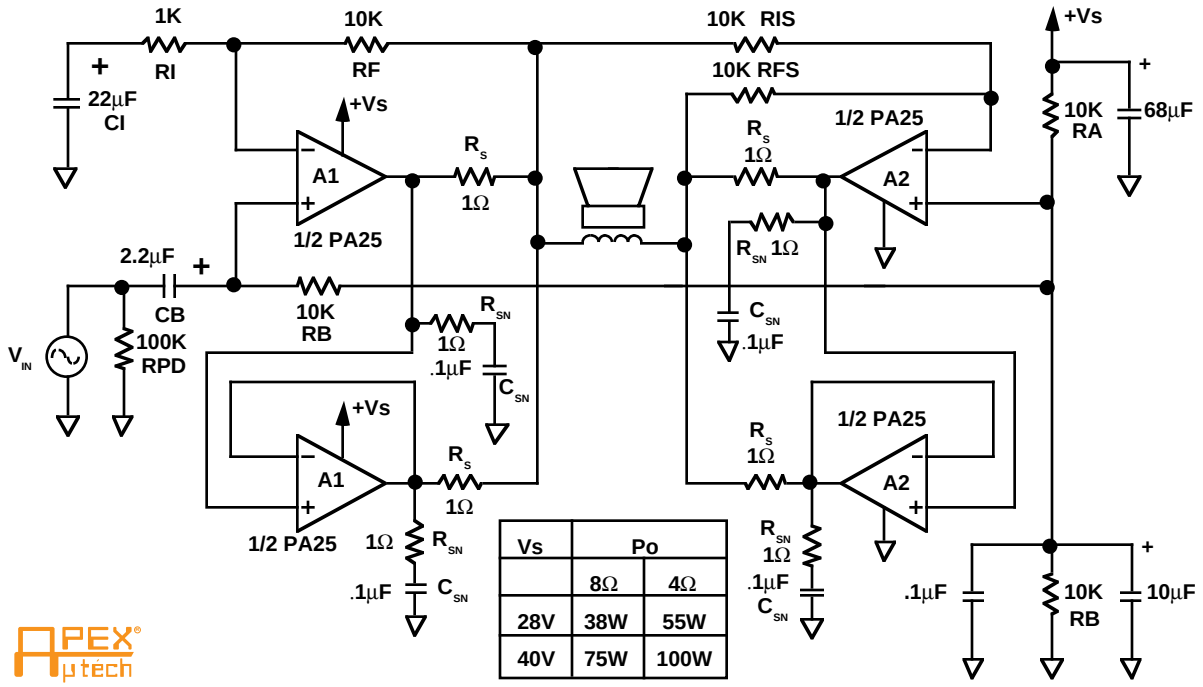
The parallel power op amp circuit will consist of a master amplifier, A1, which sets the V_{OUT}/V_{IN} gain and slave amplifiers, A2 et al, which act as unity gain followers from the master amplifier. For simplicity we will review the case of two power op amps in parallel.

We will need to consider the following key areas when paralleling power op amps:

1) Input offset voltage
2) Slew rate
3) Phase compensation
4) Current limit resistors

If we attempt to hook the outputs of two power op amps directly together the difference in input offset voltages, divided by theoretically zero ohms (a connecting wire), will cause huge circulating currents between the amplifiers, which will lead to rapid destruction. To minimize circulating currents we will need to add ballast resistors, Rs, as shown. The worst case circulating currents now are Icirc = Vos/2Rs. To minimize circulating currents we want Rs to be as large as possible. However, large values of Rs will add an additional voltage drop from the power supply rails and thereby reduce output voltage swing. Large values of Rs will also result in higher power dissipations. A rule of thumb compromise is to set Rs for circulating currents of about 1% of the maximum output current from each amplifier, .01I in our example.

SINGLE SUPPLY PARALLEL BRIDGE



Vs	Po	
	8Ω	4Ω
28V	38W	55W
40V	75W	100W

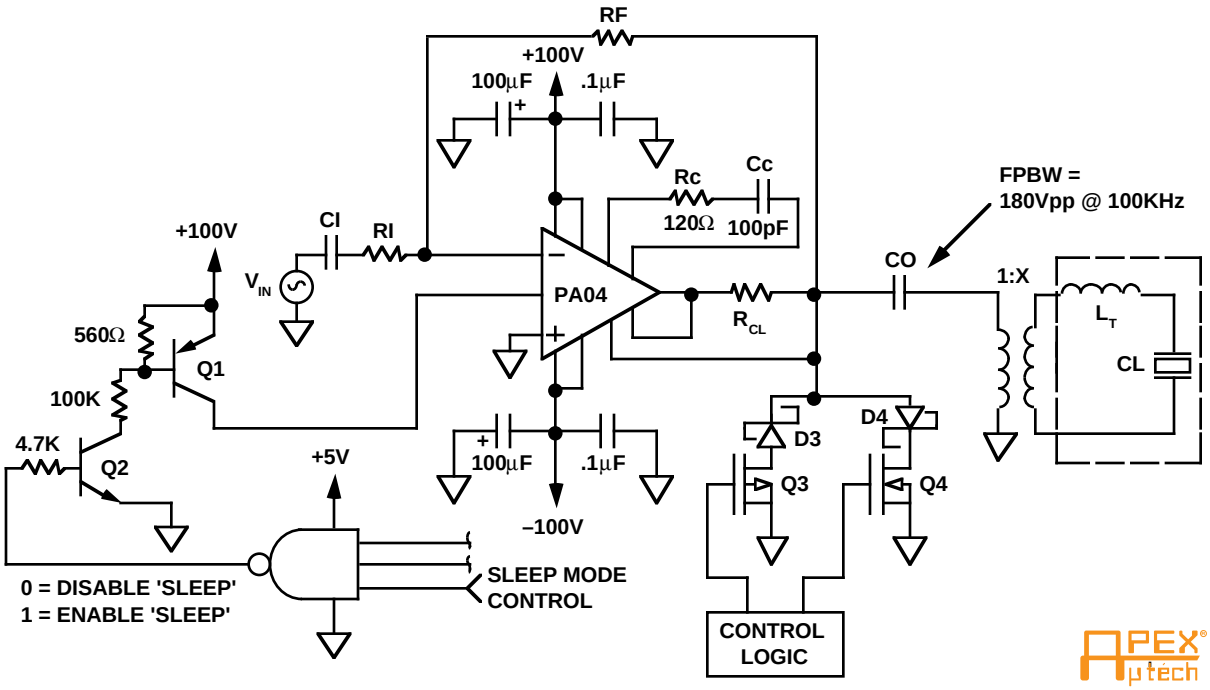
This application utilizes two power op amp circuit tricks—single supply bridge mode to increase output peak-to-peak voltage and parallel power op amps to increase output current.

The PA25 is optimized for single supply operation with its wide input common mode voltage range and low saturation voltage. The parallel combination provides a dual advantage in that we can deliver higher output currents as well as reduce the output saturation voltage since each op amp need only supply one-half the total load current.

AC coupling of V_{IN} provides level shifting of the input signal to swing symmetrically about 1/2Vs. AC coupling through CI ensures the maximum DC offset across the load is only 20mV. RB provides a +input DC bias path for the front end of the master amplifier half of A1. R_{SN} and C_{SN} networks are required on the output of each amplifier section of A1 and A2 to prevent oscillations on the output during negative swings. This is due to the type of output power stage inside the monolithic PA25. A2 is configured as a traditional inverting gain amplifier for single supply bridge mode and uses one half of itself for providing extra current as a slave amplifier in the parallel configuration.

A comparison of output powers for both a 4 ohm and an 8 ohm load are shown for two different power supply voltages.

SONAR TRANSDUCER DRIVE



High current drive capability and wide power bandwidth make the PA04 ideally suited for sonar drive applications.

Often the amplifier is required to drive the primary of a transformer to step-up its output voltage to a desired high voltage for end drive to the sonar transducer. Because transformers do not work well when saturated it is essential to minimize DC current flow in them. AC coupling of the input signal and/or the output minimizes and/or eliminates the DC input offset voltage of the PA04 from becoming gained up by the gain of the amplifier, creating a large DC offset at the output.

Often times, either through the construction of the transformer or through an additional inductor, L_T, the sonar transducer, predominantly capacitive by nature, is tuned to look resistive for a narrow band of frequencies. This minimizes SOA stresses on the PA04. It is a good idea however to consider worst case capacitive loading reflected to the primary of the transformer onto the PA04 for AC stability considerations, should there be a possibility of non-resonant frequencies being applied to the sonar transducer drive circuit.

Another feature of the PA04 which is especially helpful in battery operations is its sleep mode function which can be used to turn the amplifier off during periods of non-use to minimize battery drain. Sleep mode quiescent current is only 5mA and the output is turned off into a high impedance state.

One caution when using sleep mode is to be aware of transients up to the supply rail that can occur during transitions into and out of sleep mode. There is no esoteric way to eliminate these internal to the op amp. If these transients would provide undesired transmissions, the problem can be cured through the use of two Schottky diodes (D3,D4) and two MOSFET switches (Q3,Q4). These components short the output of the PA04 to ground during the sleep mode transitions.

Timing logic going into sleep mode is to first command the input to zero, switch on Q3 and Q4 and then enable sleep mode. Coming out of sleep mode we would first ensure input signal is zero, ensure Q3 and Q4 are on, disable sleep mode, turn off Q3 and Q4, and finally begin transmitting with our input signal. Typical delay time to squelch the sleep mode transients is about 5-10 mS.

As a final note, to minimize SOA stresses it is advised to always start the input signal at zero crossing and exponentially ramp the amplitude if possible, since a transformer really doesn't look like a transformer until we have passed a few cycles of AC through it.