PRINTED CIRCUIT BOARD LAYOUT GUIDELINES

Analog wiring techniques are typically used in functional breadboard design or low quantity manufacturing. These guidelines now apply to printed circuit boards to ensure troublefree operation.

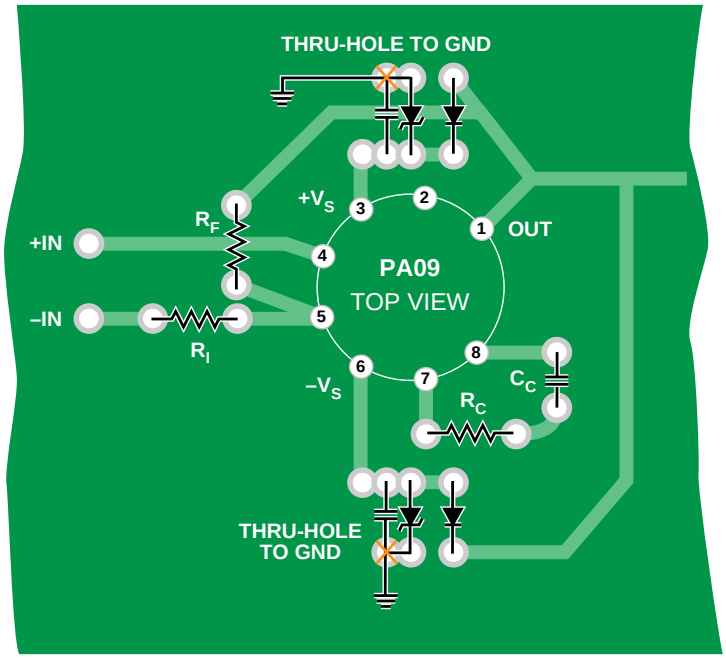
CHOICE OF MATERIAL

Epoxy based PCB's exhibit more than 1,000 times better isolation resistance than hard paper boards. Reduced leakage currents improve crosstalk. High voltage applications, in which supply voltages of more than +100 V are involved, a "conformal coating" prevents arcing between conductive layers and reduces leakage currents. However, care for void free coating, since voids will be prone to arcing and result in potential failures. It is good and clean practise to use double side copper boards, so that signal traces do not interfere with power supply lines. The component side may be used as a "ground plane", for its low impedance and shielding will prevent oscillations.

MULTILAYER BOARDS

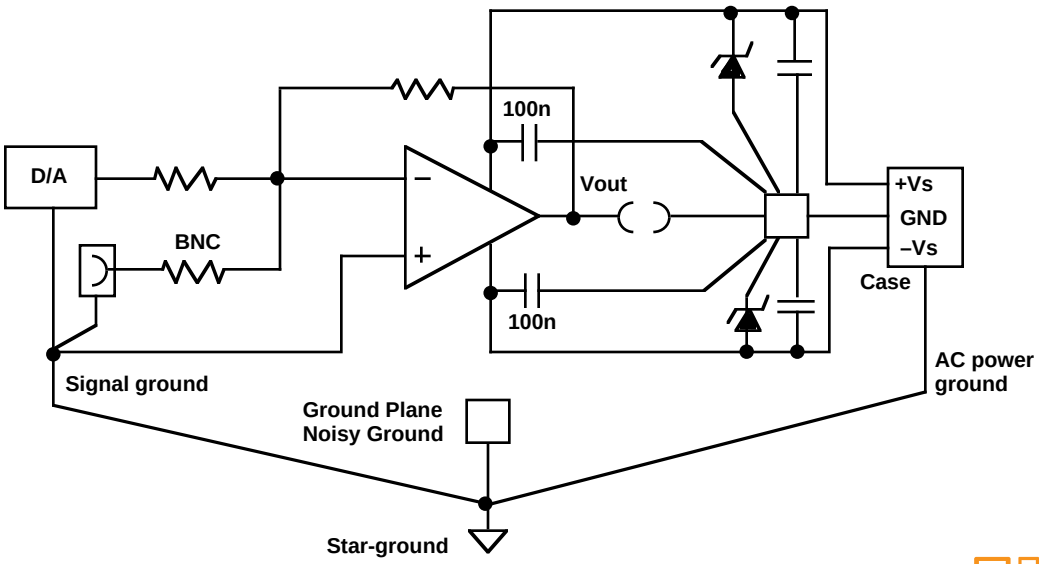
Double-sided PCB's allow strict separation of supply lines from signal paths. Furthermore, larger traces minimize lead resistance. Let traces only cross rectangular to reduce power supply line modulation due to capacitive (high voltage) and inductive (high current) coupling. More than two layers are not recommended for high voltage operation above +22 V supply voltage.

BYPASSING AND PROTECTION DEVICES



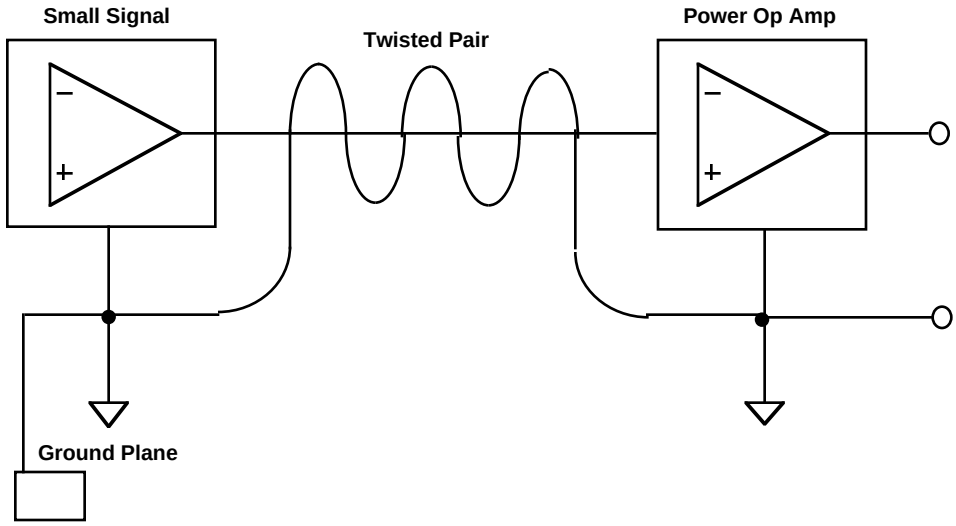
Components, that protect power amplifiers from overvoltage, kickback voltage or bypass supply line noise, are located as close as possible to the amplifier terminals. Lead inductance inhibits transients from being bypassed to GND. All leads must be as short as the device size allows. A separate GND return (noise ground) to power supply ground is keeping transient signals away from sensitive signal ground, which may feed into the non-inverting terminal. “Star-type” ground and power line layout is essential for low intermodulation. Bypass all active components with 100 nF ceramic capacitors and care for short leads. In most cases a lead length of 1 inch suffices. However, wideband and high slew/high power amplifiers, such as the PA04, PA05, PA09, PA19, WA01 and WB05, shall have ceramic bypass capacitors closer than 1/2 inch to their power supply pins.

GROUND REFERENCE



The higher the required bandwidth of a circuit, the more attention needs to be paid to ground planes and grounding elements throughout the circuit. If different systems refer to the the same ground, chose the point of highest sensitivity for a central reference point - such as the analog (AGND) and digital ground (DGND) of analog-to-digital converters or DAC's. Any voltage difference from the power supply GND system will become a common mode signal and thus will be rejected. This techniques works fine for most low frequency applications - up to 1MHz. At this frequency, however, most amplifiers have a significant decrease in common mode rejection ratio, so that the prime goal now is to reduce the loop area enclosed by the conductor.

POWER LINES AND GROUND LOOPS

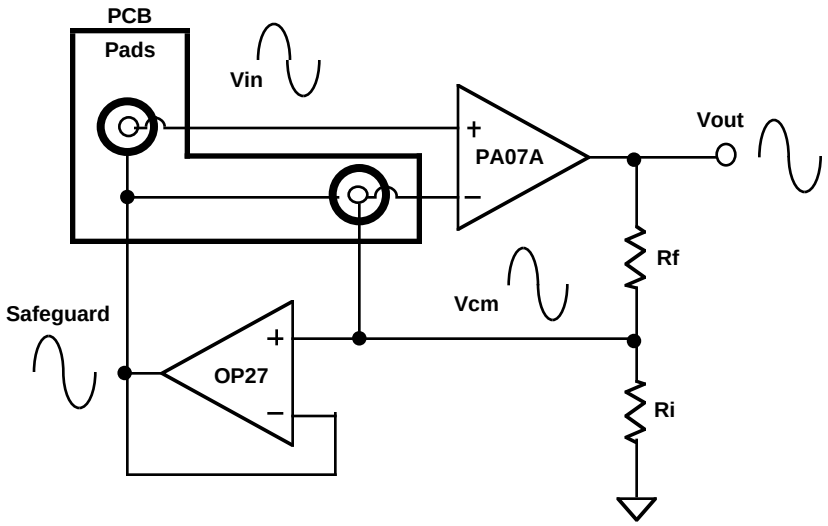


Always consider the area, which is enclosed by the high current carrying conductors: power supply —> power OpAmp —> “hot” wire —> load —> GND return. The larger this area, the higher the inductivity of this loop and oscillations may occur. As a consequence, keep power lines close together and apply the “twisted pair” technique to reduce the loop area of the load interface. Poor GND return paths “feed forward” into the signal ground and produce oscillations. Strive for a direct current return to the power source.

All power supply lines are bypassed with electrolytic plus ceramic capacitors. If the amplifier needs to deliver high current in a few micro seconds, it is wise to replace the electrolytics with polypropylen capacitors, which feature very low dissipation factor at acceptable capacitance ratings. This reduces fire hazard. In high pulse current applications, high ESR ratings lead to overtemperature of capacitors and finally to burn-out.

In high voltage applications above 200 V, provide at least 1/10" distance between all conductors and apply conformal coating. Although different guidelines recommend higher spacing, tests on the Apex EK42 evaluation kit PCB exhibit an isolation barrier of more than 1,000 V. High levels of moist increases leakage currents and encourages arcing. Conformal coating, however, separates moisture from the conductive layer and improves isolation. Apply common sense in high voltage applications and maximize the distance between high voltage supply lines, output connectors, external compensation nodes, and GND.

SENSITIVE COMPONENTS



Parasitic effects of adjacent conductors or layers have serious impact on the circuit performance. This leads from significant reduction in bandwidth to oscillation. The most sensitive junctions in a circuit, which include a power operation amplifier, are its input terminals. The typical input capacitance from 3 pF to 15 pF multiplies, if input and feedback resistors are not mounted closely to the input terminals. In wideband applications a maximum of 1/10th" lead length and surface mount devices are prefered. Applications below 1 MHz closed loop bandwidth may be fine with one inch maximum distance between resistors and terminal. The same guidelines apply for external phase compensation components. They shall be mounted next to the designated terminals. Please note, that the compensation capacitor can see the full supply voltage.

Input stage leakage currents are reduced by applying a "safe-guard" ring, that embraces both input terminals. If this ring is held at the same potential as the input (common mode voltage), leakage currents are absorbed by this ring and isolate the input terminals. For inverting configurations, common mode voltage is zero. Thus this ring is tied to GND.

VOLTAGE CLEARANCE ON PRINTED CIRCUIT BOARDS

VSS [V]	mm	inches	APEX models
0-100	0.13	0.005	Ø
≤ 150	0.25	0.01	PA03
≤ 200	0.44	0.018	PA04, PB50
≤ 300	0.97	0.038	PA08, PA80, PA81, PA82, PA83, PA84, PB58
≤ 400	1.65	0.065	PA41, PA42
≤ 500	2.54	0.1	PA85, PA897, PA88
≤ 600	3.13	0.124	Ø
≤ 800	4.3	0.17	Ø
≤ 1000	5.12	0.20	Ø
≤ 1200	5.8	0.23	PA89

The application of high voltage amplifiers reveals the hazard of arcing due to high energy electrical fields. The demand for narrower lines and closer spacings conflict with the requirements for high voltage isolation. Basically, the resistance between two isolated conductors is dependent on the material, the pollution, the atmosphere, the humidity, and the elevation where the board is operated. As air is a superior insulator, printed circuit boards (PCB) base material creates a leakage path between two lines. Therefore, epoxy PCBs are preferred to hard paper boards. High levels of pollution will encourage breakdown. The above data is based on MIL-STD-275D and IPC-ML-910A. Coated boards require only half the recommended clearance. However, coating defects will lower the breakdown voltage and will degrade the board performance after a breakdown occurs. Because the recommended values incorporate safety factors for worst case, tolerances are considered conservatively, thus leading to a very reliable design. However, it is the intention of this note to highlight the importance of adequate line spacing in high voltage designs.
The pin clearance of an PA87 is already down to 0.1". At a pin width of 0.019", The clearance will yield 0.08", that is 20% less than the recommendation[1]. Rectangular solder pads, 0.02" wide, should be prefered to circular pads to minimize breakdown hazard and still provide sufficient material to solder to the pins.

Vss is the operating voltage from the positive to the negative rail. This voltage can be present especially at the output and across compensation pins. As transients may occur, high voltage spikes may be present on input pins as well. Therefore, input voltage clamping diodes are recommended for high voltage applications and those that implement a feedback capacitor. Please refer to “Protection Diodes for Power Opamps”.

[1] **IPC-TP-333 Charles W. Jennings, Sandia National Labs, Albuquerque, NM**
Apex considers this paper to be very conservative and recommends to evaluate actual environmental conditions before designing the PCB layout.