Application Notes

Application Notes: The Apex Library of Application Notes are written to address specific types of applications rather than specific products. Please consult the Application Notes section for a complete title listing and a cross reference by application topic.

TECHNICAL SUPPORT TO SERVE YOU

Download your Virtual Application Engineer

The Apex Power Design spreadsheet is a lot more than arithmetic. Start with the automated selector guide and continue through automated calculation and graphing of many otherwise tedious design tasks: load and amplifier power levels, load lines, loop stability with reactive loads, current limit (including foldover), frequency sweeps for PWM filters and loads and heatsink-efficiency trade-offs with PWM amplifiers. Liberal use of comments plus the automated circuit analysis examples make Power Design a good learning tool.

Spice Files

Macromodels of most Apex linear products are available on our web site. The models are compatible with a wide variety of Spice simulators.

Technical Seminars

APEX also conducts technical seminars across the U.S. and around the free world. These seminars are designed to provide you with extensive information on PWM and power amplifier applications, in addition to the hows and whys of internal circuits and construction. Pros and cons of various approaches are presented along with potential dangers. Question and answer periods emphasize areas of special interest. These seminars are available to groups of 10 or more engineers interested in APEX products. Contact your local APEX sales representative, or one of us directly about seminar scheduling in your area.

Applications Notes

It is easy to find appropriate Apex Application Notes because design topics rather than model numbers usually title them. Application notes are developed with the help of your questions, suggestions and feedback. Please call us if you have identified and implemented a new useful application and are ready to share the information with others.

Applications Hotline

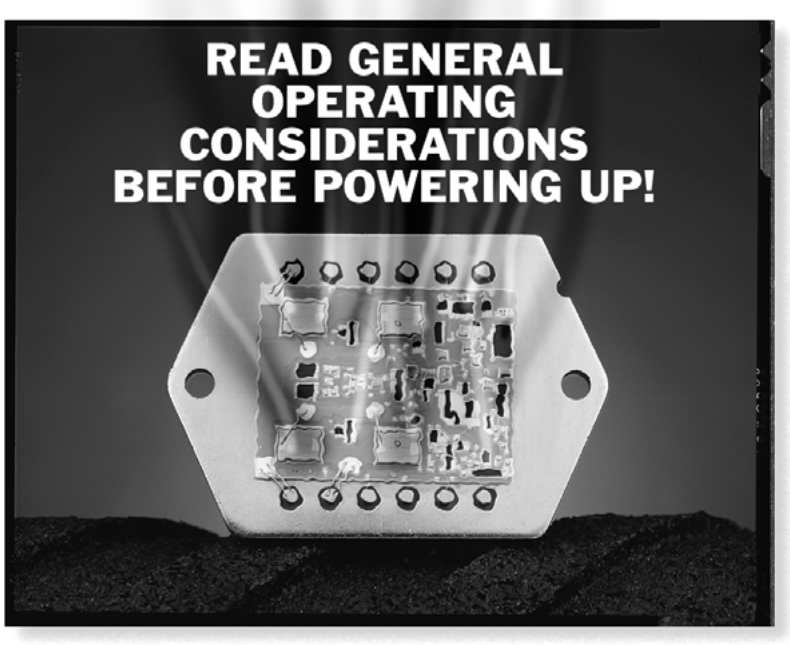
The APEX Applications puts you in touch with a wealth of experience. We can assist you with product selection, design suggestions, schematic review and circuit debugging. Call us directly at 1-800-546-2739.

We are always open to suggestions on products you'd like to see from us.

APPLICATION NOTES CROSS REFERENCE

GENERAL APPLICATION TOPIC	RECOMMENDED APPLICATION NOTE (A/N)
Basics of Power Amplifiers	A/N 1, 30, 31
Motor/Valve/Actuator	A/N 11, 22, 24, 30
Programmable Power Supply	A/N 6, 7, 22, 35
Electromagnetic Deflection	A/N 5, 13
Electrostatic Deflection	A/N 3, 20
Piezo, Electrofluorescent Display, Capacitive Load	A/N 19, 25, 38
Audio	A/N 3, 8, 11, 17, 22
Wideband	A/N 17, Consult Factory
Power Delivery and Power Dissipation	A/N 8, 11, 30, 37, 39
Power Booster or Composite Amplifier Applications	A/N 14, 19
PA12 and PA10 Applications	A/N 9
Safe Operating Area	A/N 16, 22, 37
Bridge Circuit Applications	A/N 3, 20, 30
Stability	A/N 19, 25, 38
Basics of PWM	A/N 30, 39
PWM Low Pass Filtering	A/N 32, 39
Power Design Tool	A/N 37, 38, 39

For further assistance, refer to the subject index located at the back of this data book (page 899).



NOTES:

MOTION CONTROL

Position

Computer controlled motor drive, PA03
Motor position control, PA07
Bidirectional motor drive, PA26
Bidirectional bridge for a single supply, PA12
Multiple antenna elevation and azimuth, SA01

Torque

Current control, solenoid or linear actuator drive, PA26
Dual unipolar solenoid driver, PA26
Limited angle torque control, PA02
Computer controlled motor/programmable torque circuit, PA51
Super power torque drive, PA03
Z-axis voice coil position, SA60

Speed

Simple unidirectional speed control, PA01
Single supply bidirectional motor drive, PA21
3-Phase motor drive, PA26

AUDIO

Aircraft audio, SA07
Vehicular sound system power stage, PA02
Bridge audio amplifier, PA02
Audio bridge , PA26
Standard audio amplifier, PA10
Single supply parallel bridge, PA25
Audio amplifier, SA51

ATE

HV PPS

Telephone ring generator, PA41
High power ring generator, PA44
High Accuracy PPS, PB58
HV PPS, PA89

HC PPS

400 Hz servo supply, PA61
PPS – Fast power driver, PA19
PPS – Remote power sensing, PA61
Hi-power PPS, PA03
High power PPS, SA13
Expandable AC PPS, SA03
Remote sensing PPS, PA07

Pin Drivers

ATE Pin Driver, PA08

DEFLECTION

Electromagnetic

Magnetic deflection, PA09
Electromagnetic deflection amplifier, PA02
Voltage to current deflection, PA07
Horizontal deflection amplifiers, PA45
High current asymmetrical supply, PA02
High current asymmetrical supply, PA10

Electrostatic

CRT dynamic focus, PA85
Electrostatic deflection amplifier, PA84

PIEZO

Sound

Sonar transducer driver, PA04
Sonar transducer driver, PA05
Unipolar bridge, PA41/PA42
Bipolar bridge, PA41/PA42
Simple piezo transducer drive, PA83
Composite piezo transducer drive, PA41
Single bridge, PA41/PA42

Micromovement

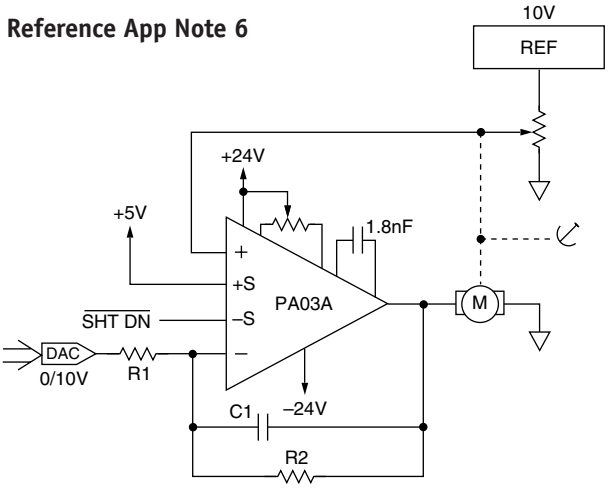
Low cost 660V p-p piezo, PA41/PA42
High accuracy composite output, PA41/PA42
Asymmetrical output, PA41/PA42
Bipolar output, PA41/PA42
Piezo printer driver, PA84
Low power, piezoelectric positioning, PA15
Single axis micro-positioning, PA89
Piezo driver with RISO, PB58
Bridge piezo drive with selectable gain, PA88
Composite piezo transducer drive, PA41
±1160V piezo drive bridge, PA89
860Vpp piezo drive single supply bridge, PA88

Application Notes Cross Reference
#3, #11, #20, #22, #24, #30

POSITION

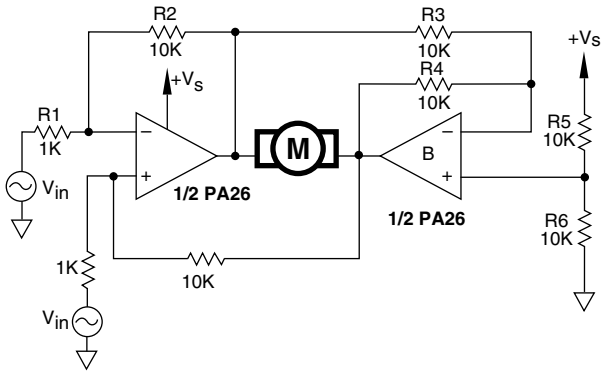
PA03

Reference App Note 6



COMPUTER CONTROLLED MOTOR DRIVE

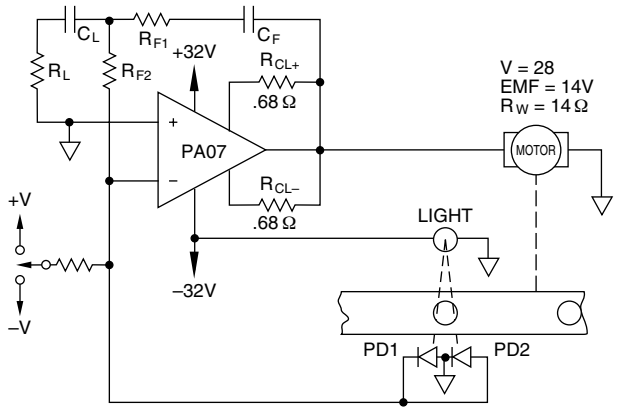
PA26



BIDIRECTIONAL MOTOR DRIVE

PA07

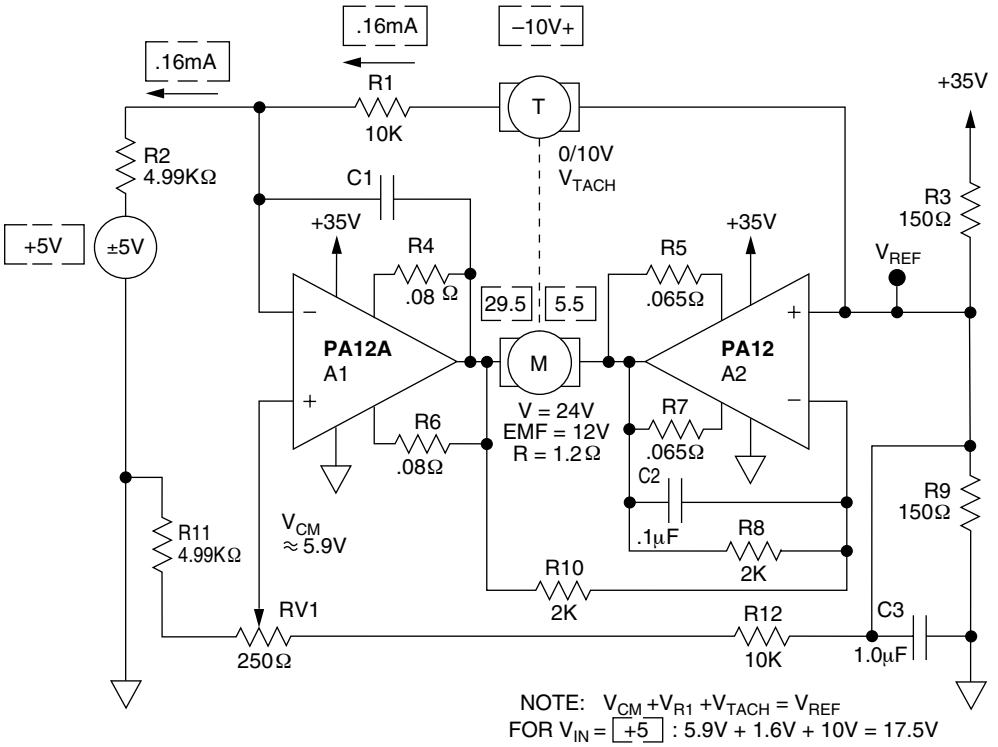
Reference App Note 2



MOTOR POSITION CONTROL

PA12

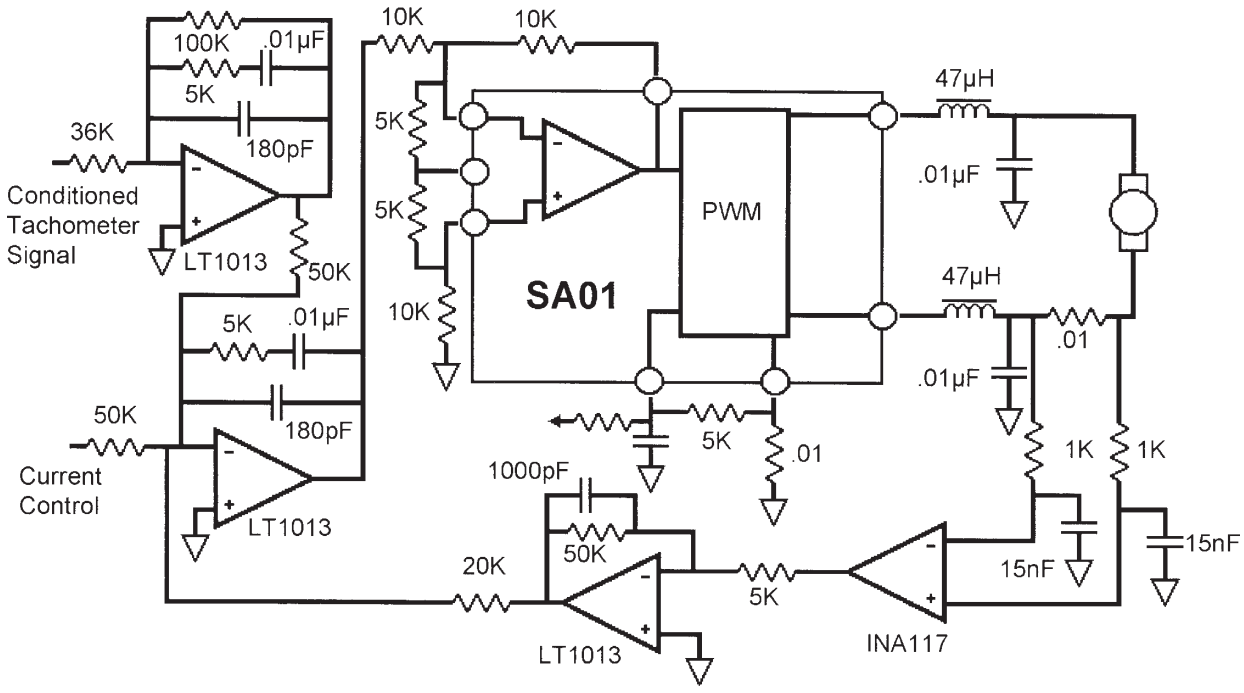
Reference App Note 3



BIDIRECTIONAL BRIDGE FOR A SINGLE SUPPLY

SA01

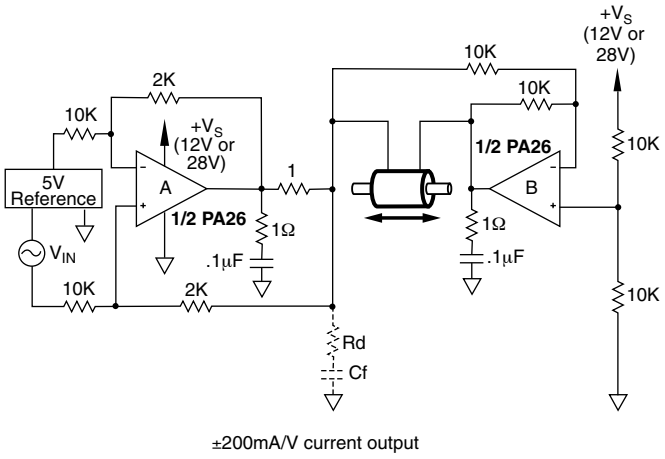
Reference Technical Seminar: Motion



MULTIPLE ANTENNA ELEVATION AND AZIMUTH

TORQUE

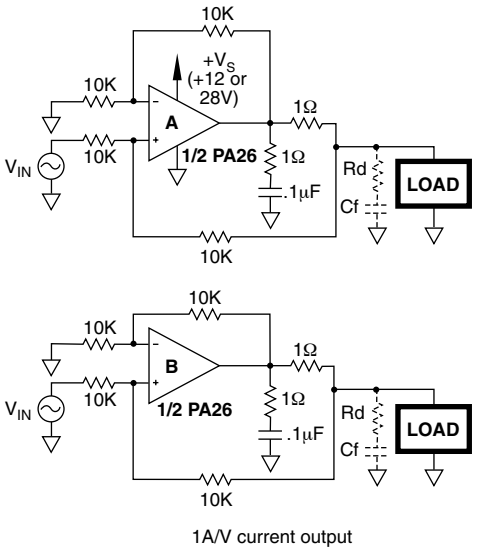
PA26



±200mA/V current output

CURRENT CONTROL, SOLENOID OR LINEAR ACTUATOR DRIVE

PA26

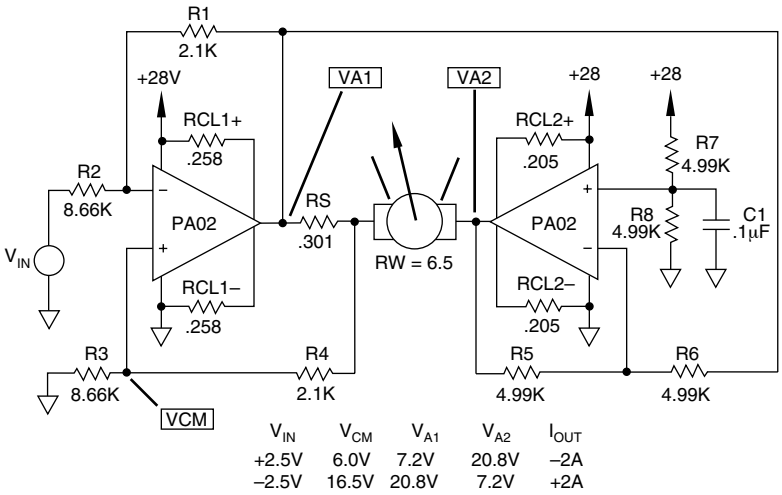


1A/V current output

DUAL UNIPOLAR SOLENOID DRIVER

PA02

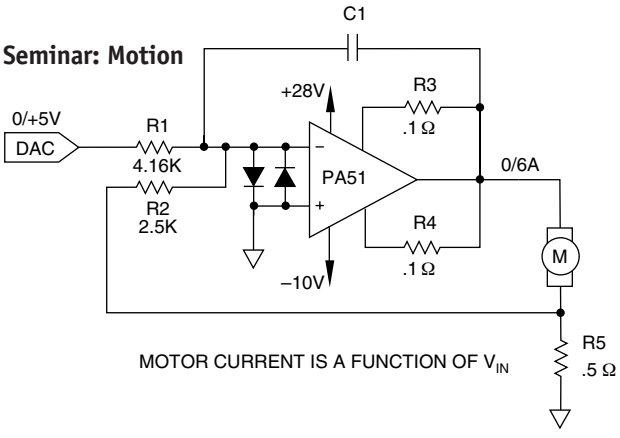
Reference App Note 21



LIMITED ANGLE TORQUE CONTROL

PA51

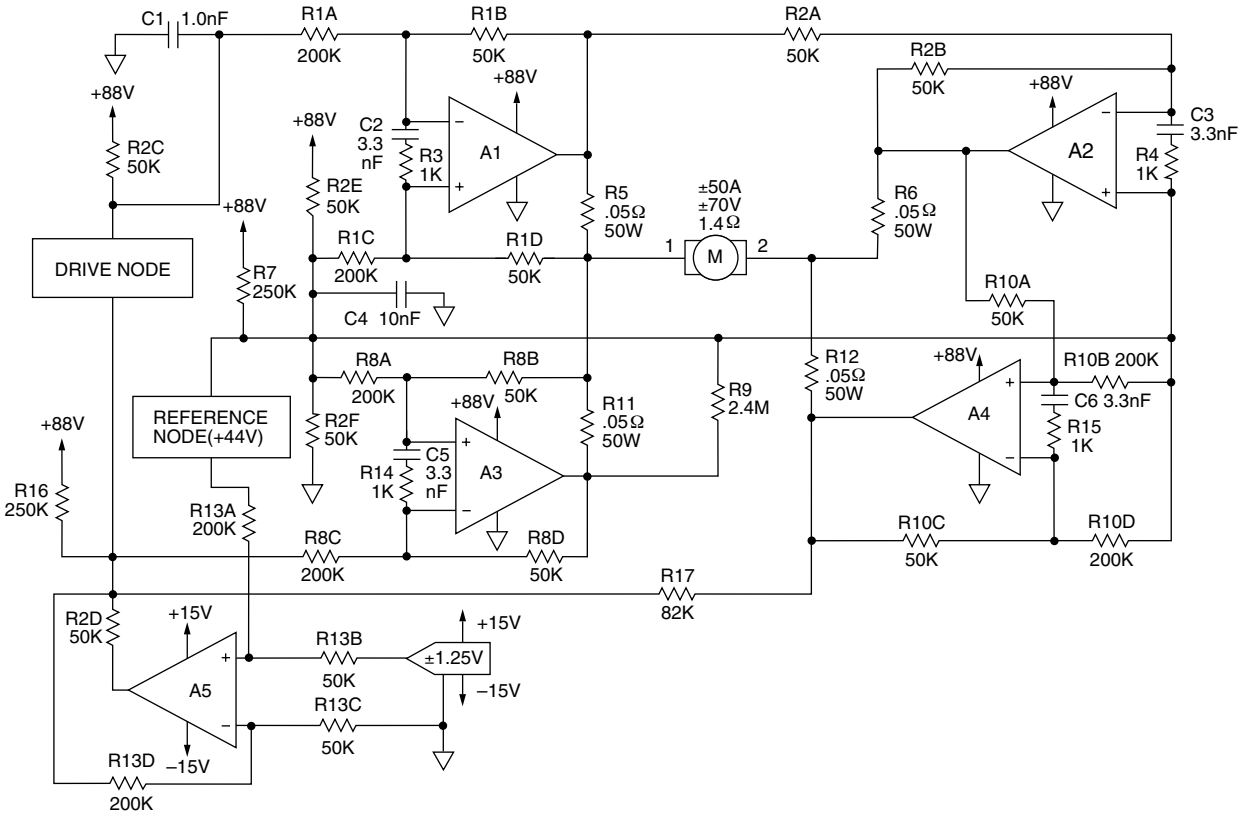
Reference Technical Seminar: Motion



COMPUTER CONTROLLED MOTOR/PROGRAMMABLE TORQUE CIRCUIT

PA03

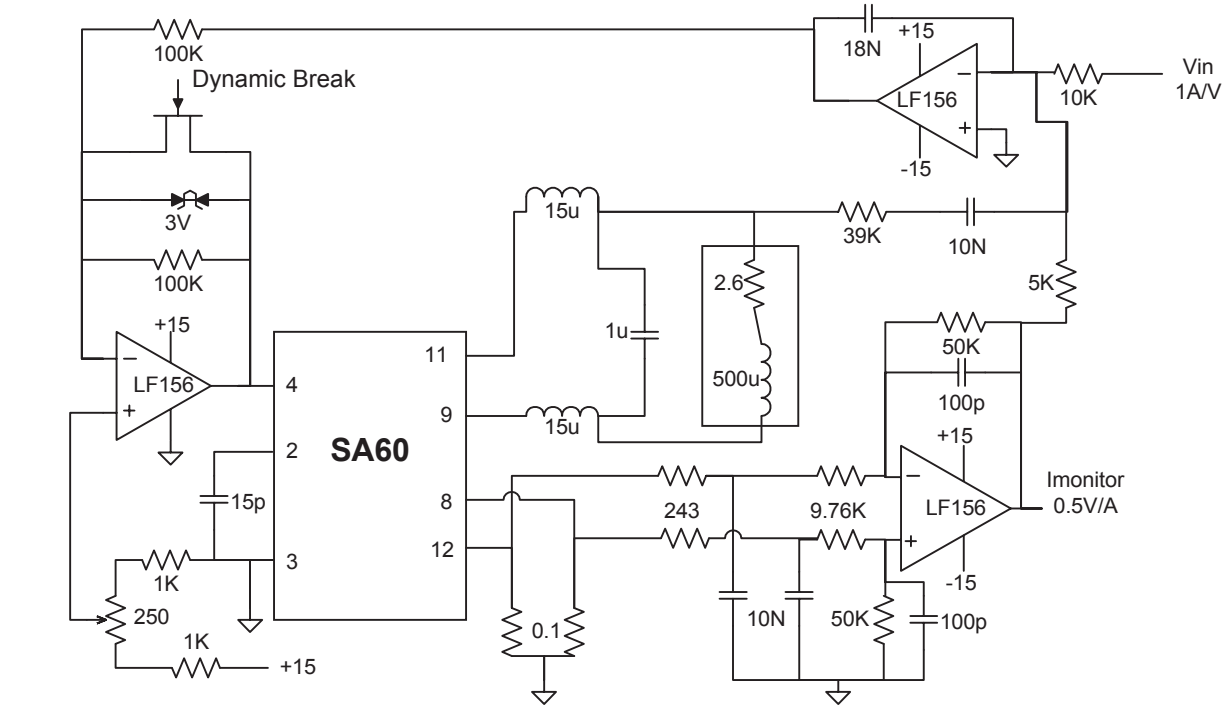
Reference App Note 6



SUPER POWER TORQUE DRIVE

SA60

Reference Technical Seminar: Motion

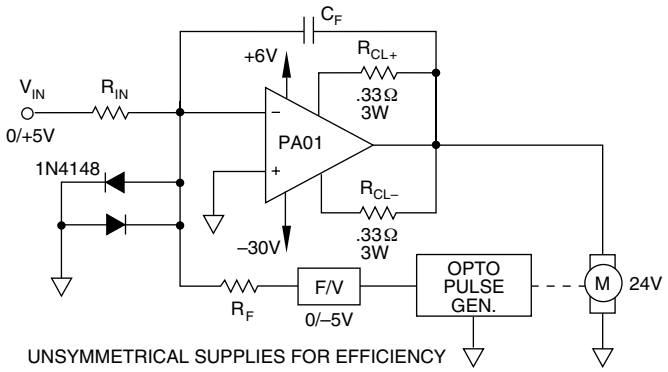


Z-AXIS VOICE COIL POSITION

SPEED

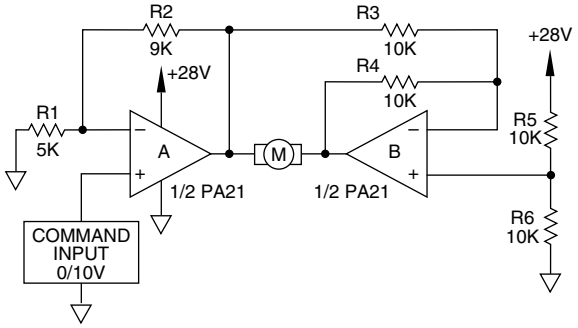
PA01

Reference Technical Seminar: Motion



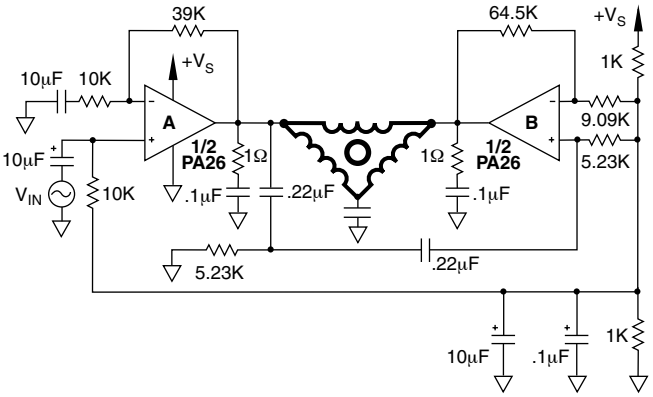
SIMPLE UNIDIRECTIONAL SPEED CONTROL

PA21



SINGLE SUPPLY BIDIRECTIONAL MOTOR DRIVE

PA26

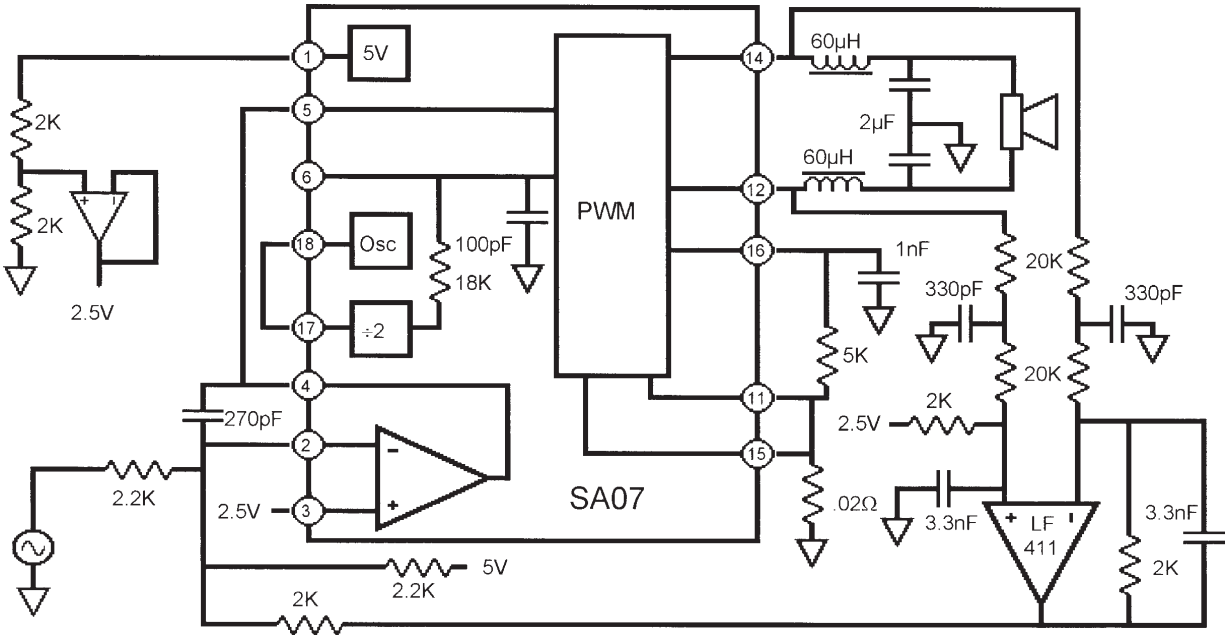


3-PHASE MOTOR DRIVE WITH 120° PHASE SHIFT

Application Notes Cross Reference
#3, #8, #11, #17, #22

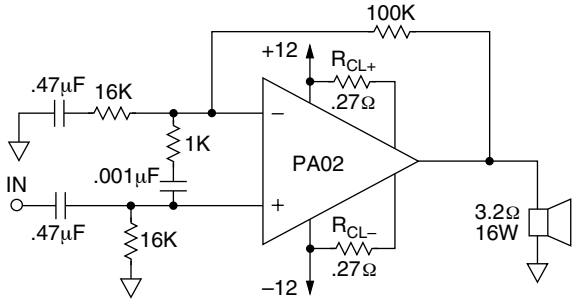
SA07

Reference Technical Seminar: Audio



AIRCRAFT AUDIO

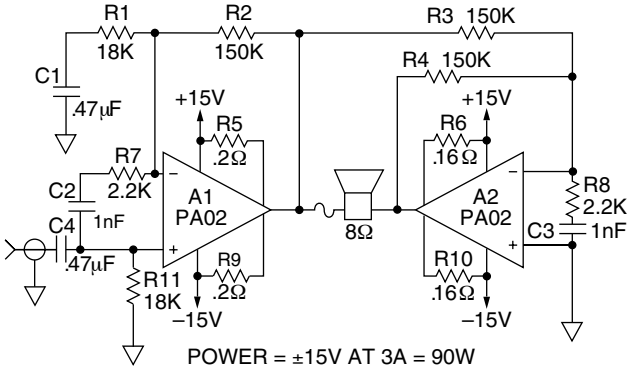
PA02



VEHICULAR SOUND SYSTEM POWER STAGE

PA02

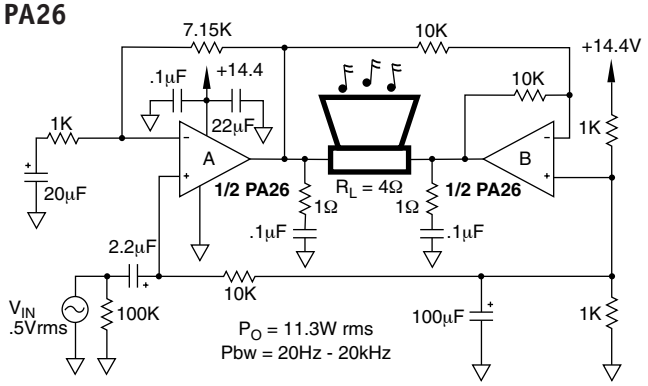
Reference App Note 3



BRIDGE AUDIO AMPLIFIER

G

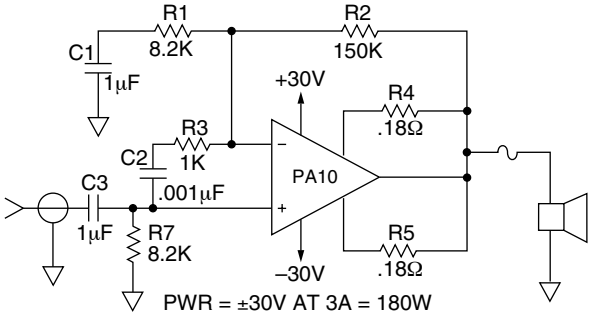
PA26



AUDIO BRIDGE

PA10

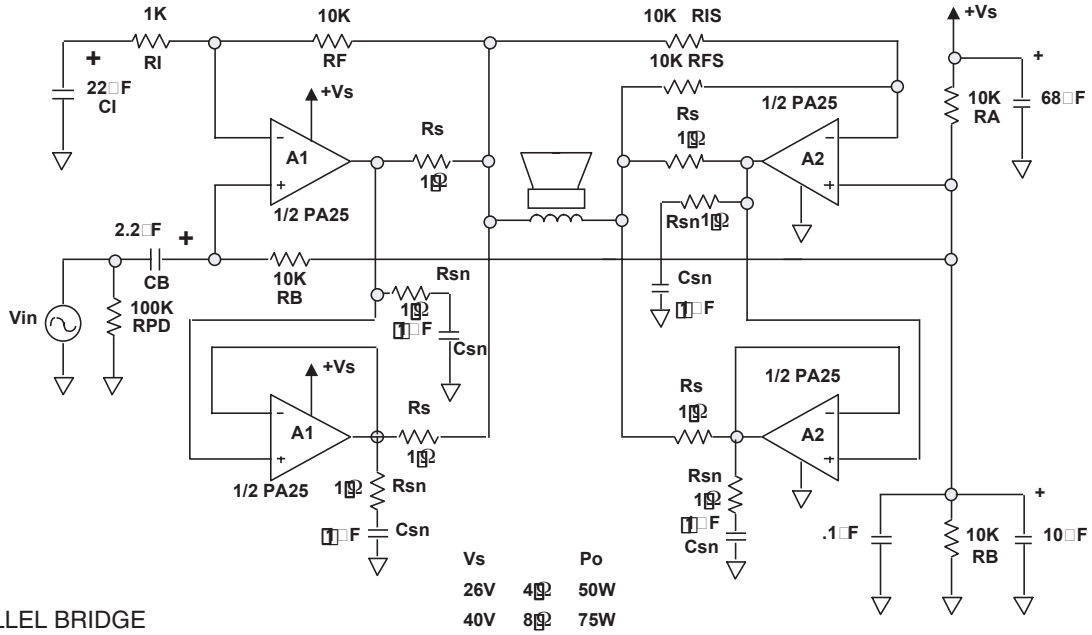
Reference App Note 3



STANDARD AUDIO AMPLIFIER

PA25

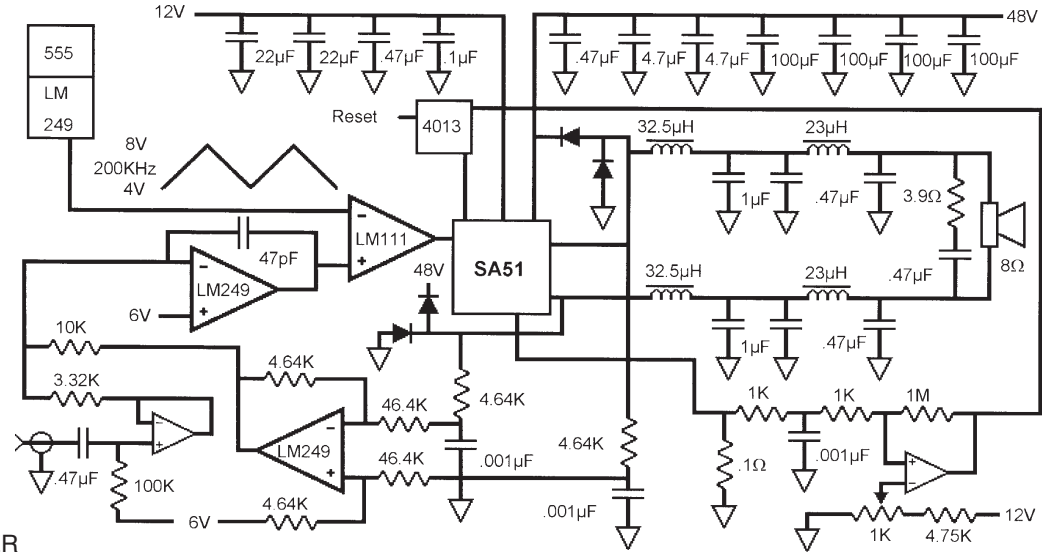
Reference App Note 20, Technical Seminar: High Power



SINGLE SUPPLY PARALLEL BRIDGE

SA51

Reference Technical Seminar: Audio



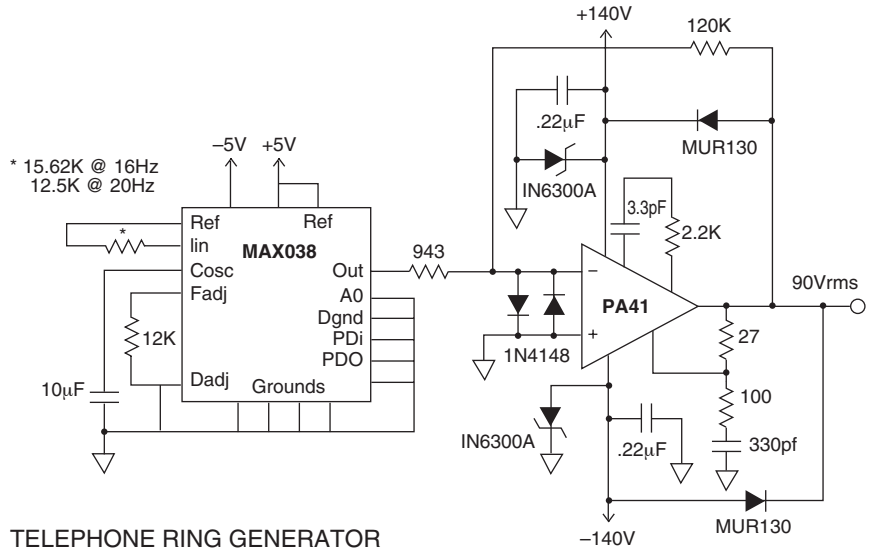
AUDIO AMPLIFIER

Application Notes Cross Reference
#6, #7, #22

HV PPS

PA41

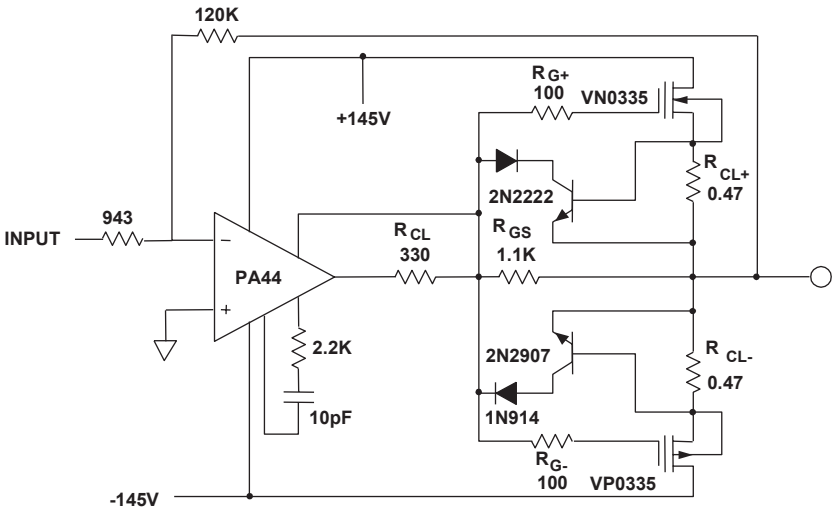
Reference Technical Seminar: Signal Sources



TELEPHONE RING GENERATOR

PA44

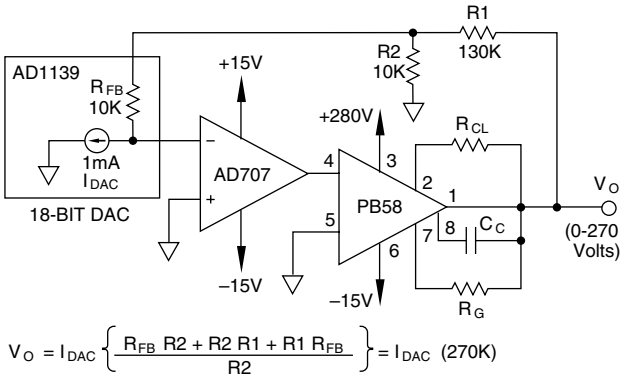
Reference Technical Seminar: Signal Sources



HIGH POWER RING GENERATOR

PB58

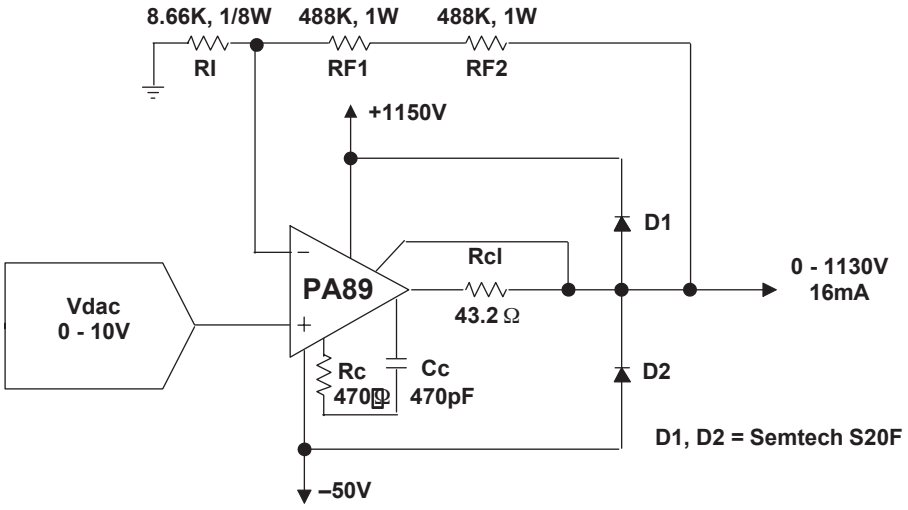
Reference App Note 14



HIGH ACCURACY PPS

PA89

Reference Technical Seminar: ATE

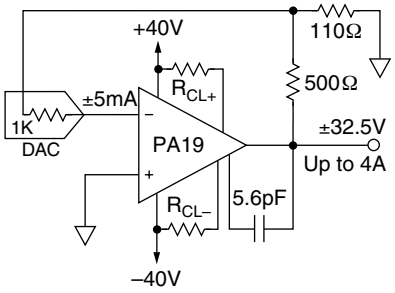


HV PPS

HC PPS

PA19

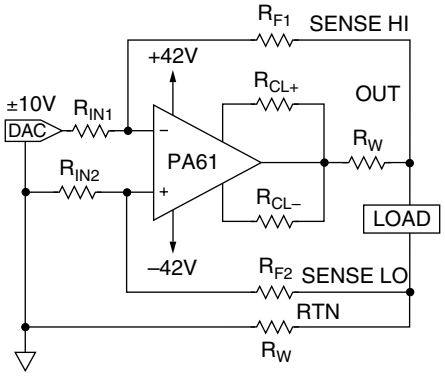
Reference PA19 Data Sheet



PPS – FAST POWER DRIVER

PA61

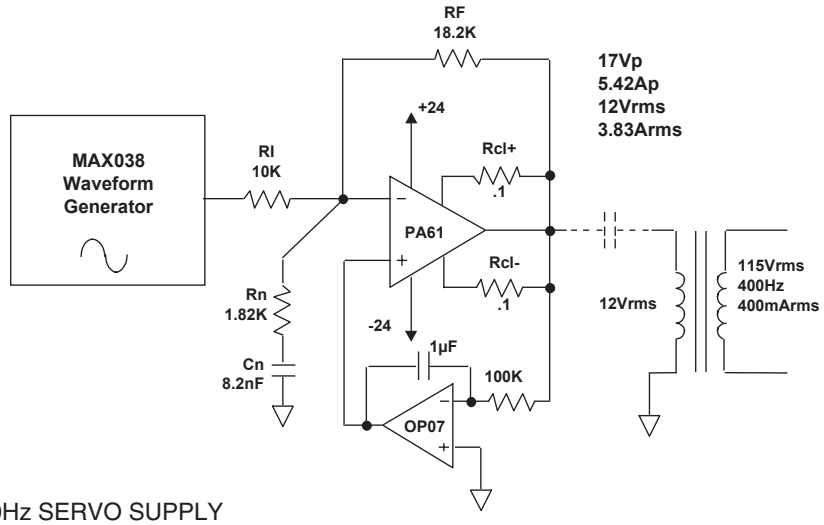
Reference Technical Seminar: ATE, App Note 7



PPS – REMOTE POWER SENSING

PA61

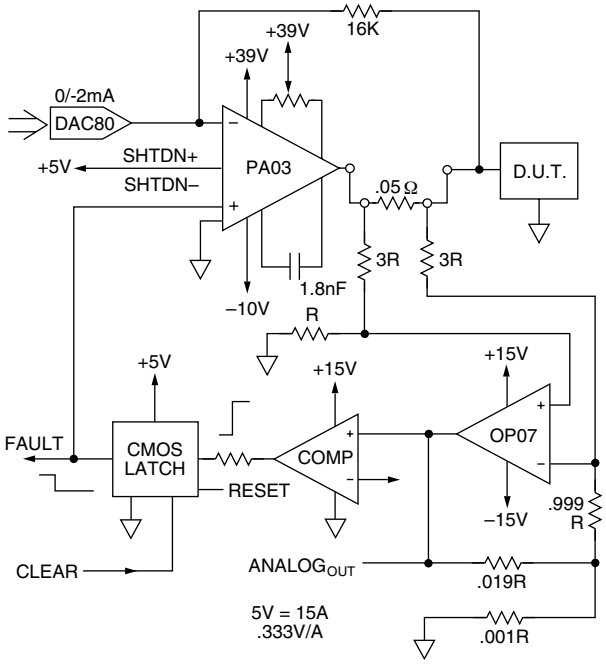
Reference Technical Seminar: Signal Sources



400Hz SERVO SUPPLY

PA03

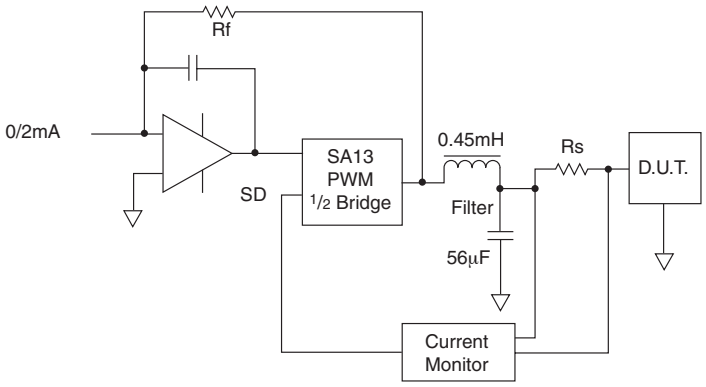
Reference App Note 6



HIGH POWER PPS

SA13

Reference Technical Seminar: ATE

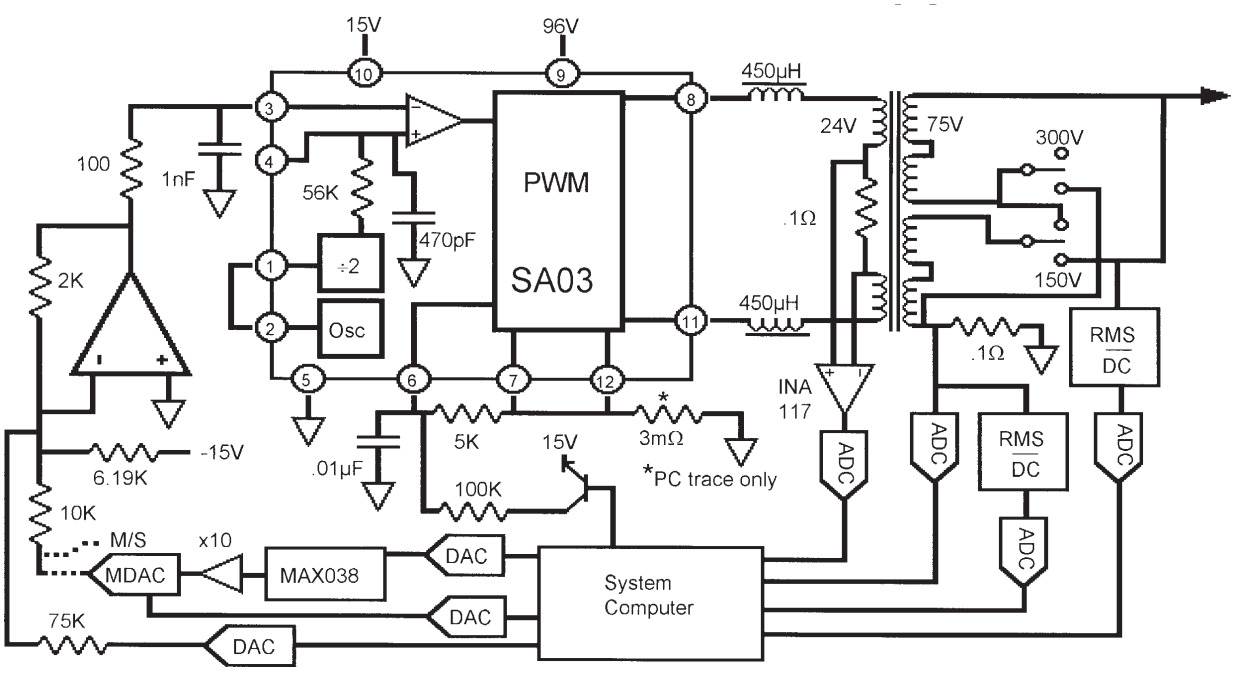


HIGH POWER PPS

G

SA03

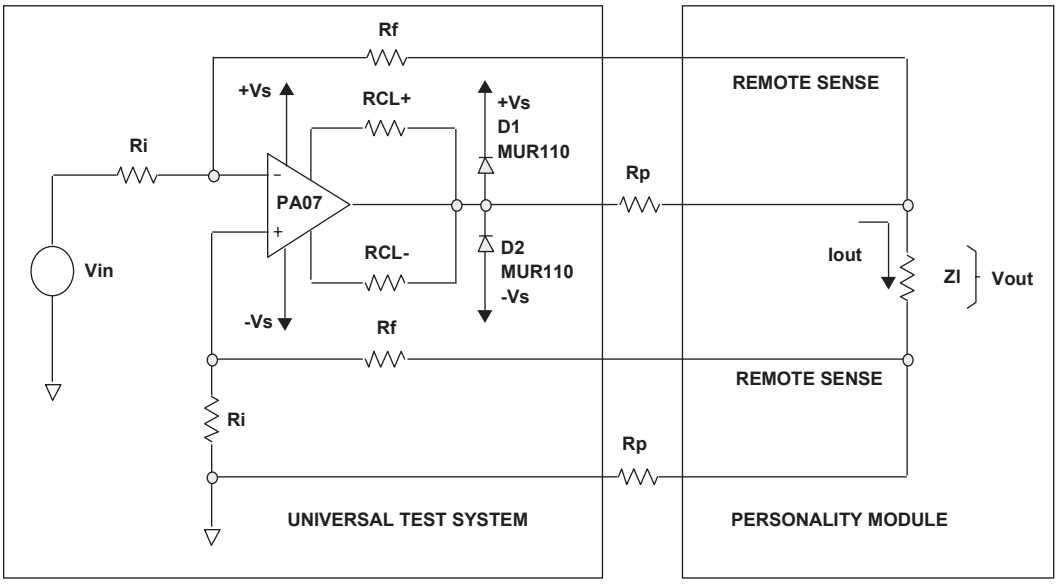
Reference Technical Seminar: ATE



EXPANDABLE PPS

PA07

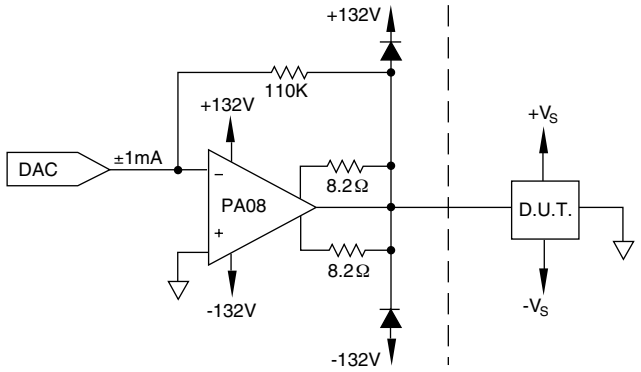
Reference Technical Seminar: ATE



REMOTE SENSING PPS

PA08

Reference PA08 Data Sheet



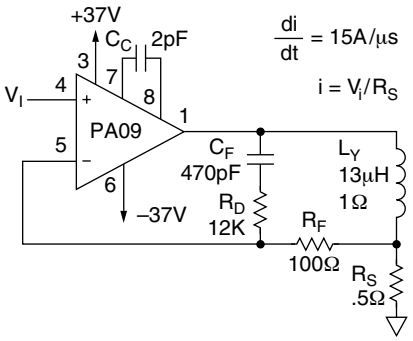
ATE PIN DRIVER

Application Notes Cross Reference
#5, #22

ELECTROMAGNETIC

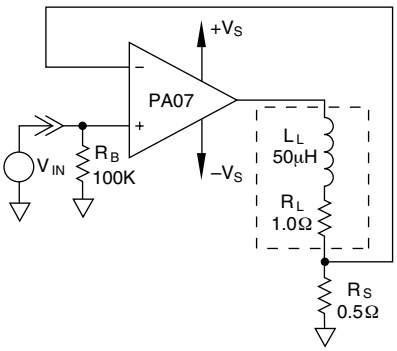
PA09

Reference App Note 5, Technical Seminar: Deflection



MAGNETIC DEFLECTION

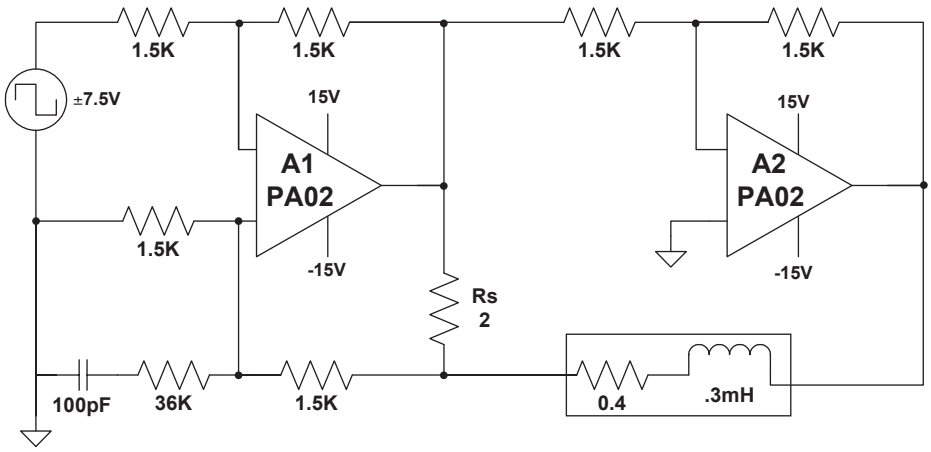
PA07



VOLTAGE TO CURRENT DEFLECTION

PA02

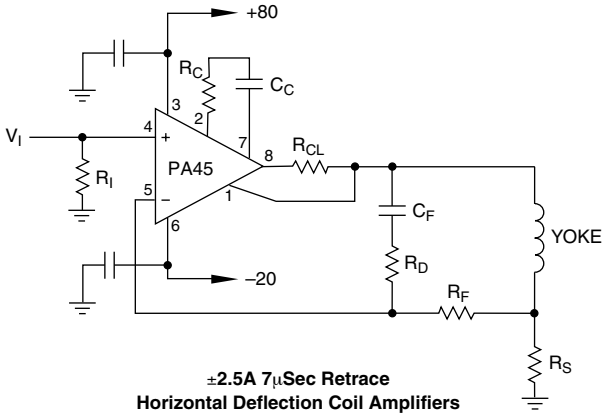
App Note 5, Technical Seminar: Deflection



ELECTROMAGNETIC DEFLECTION AMPLIFIER

PA45

Reference PA45 Data Sheet

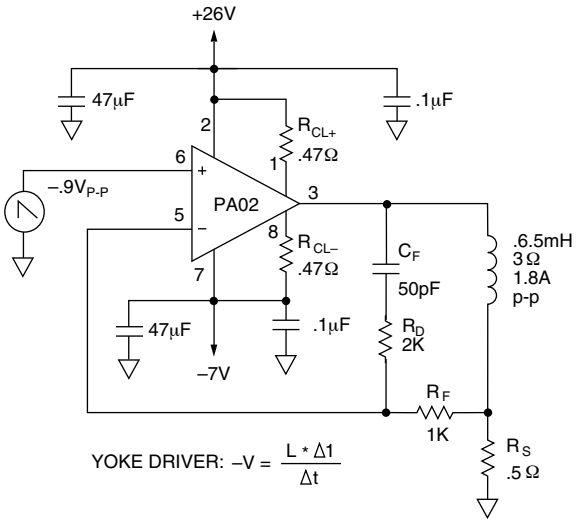


±2.5A 7μSec Retrace
Horizontal Deflection Coil Amplifiers

HORIZONTAL DEFLECTION AMPLIFIERS

PA02

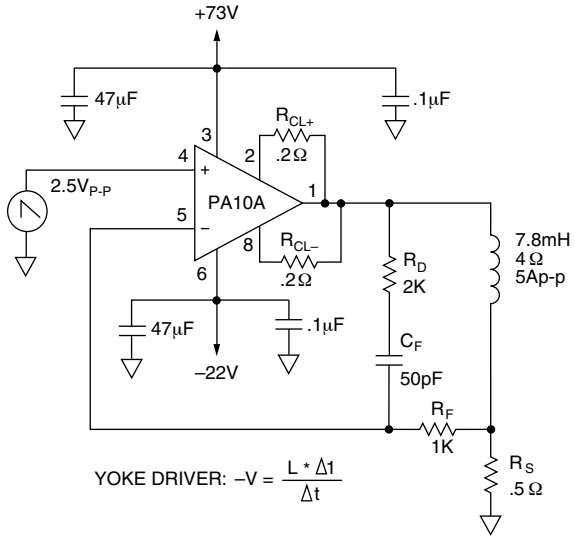
Reference App Note 5



HIGH CURRENT ASYMMETRICAL SUPPLY

PA10

Reference App Note 5



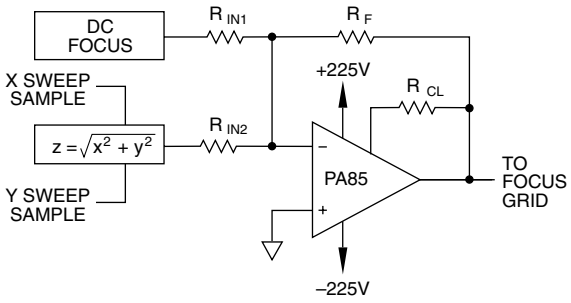
HIGH CURRENT ASYMMETRICAL SUPPLY

G

ELECTROSTATIC

PA85

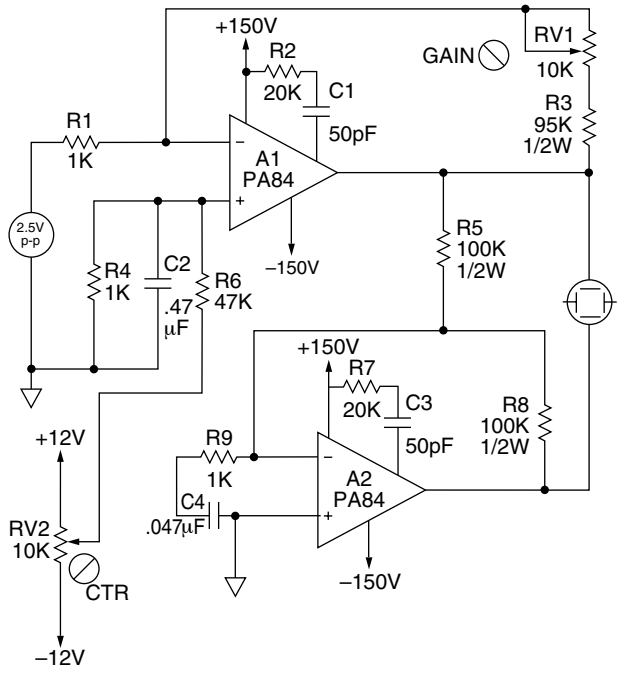
Reference Technical Seminar: Deflection



CRT DYNAMIC FOCUS (VALUES ARE APPLICATION DEPENDENT)

PA84

Reference App Note 3, Technical Seminar: Deflection



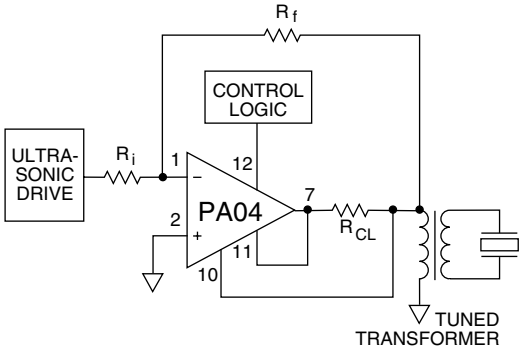
ELECTROSTATIC DEFLECTION AMPLIFIER

Application Notes Cross Reference
#19, #22, #25

SOUND

PA04

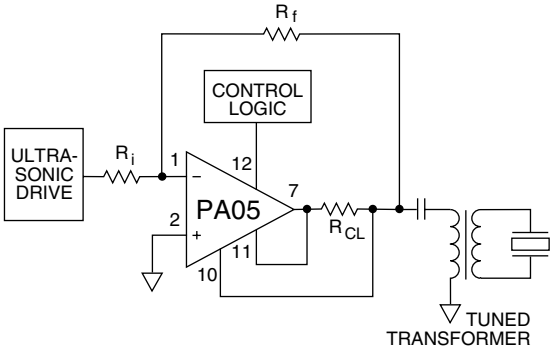
Reference Technical Seminar: Audio



SONAR TRANSDUCER DRIVER

PA05

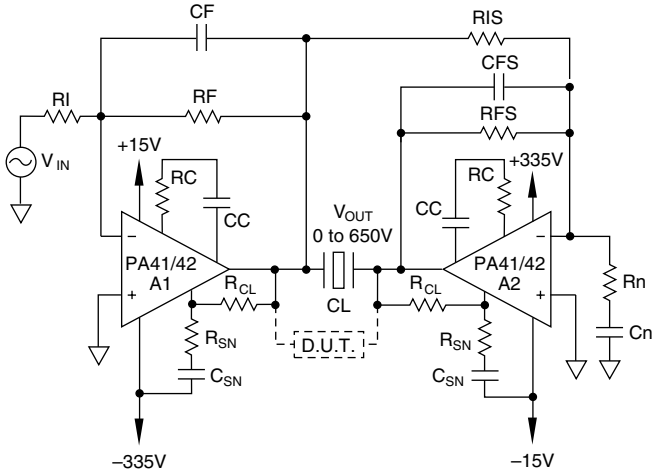
Reference Technical Seminar: Audio



SONAR TRANSDUCER DRIVER

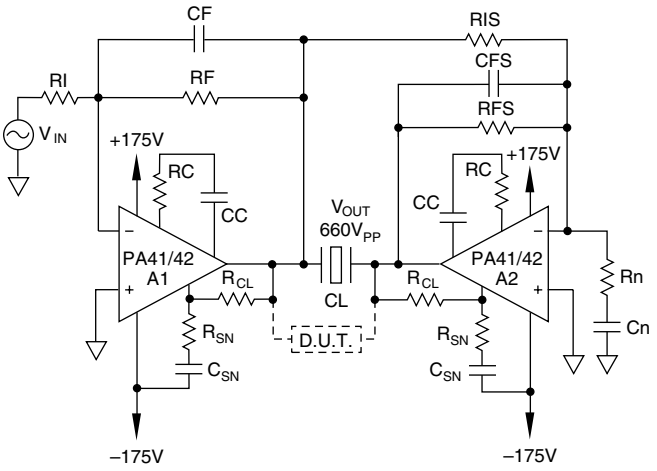
PA41/42

Reference App Note 20



UNIPOLAR BRIDGE

PA41/42

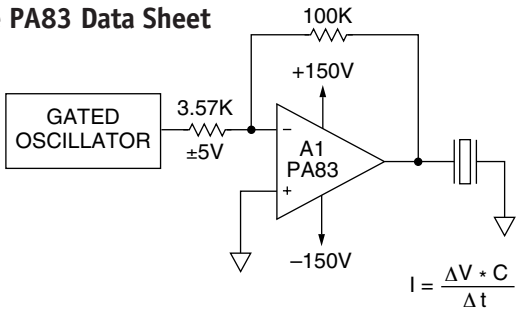


BIIPOLAR BRIDGE

G

PA83

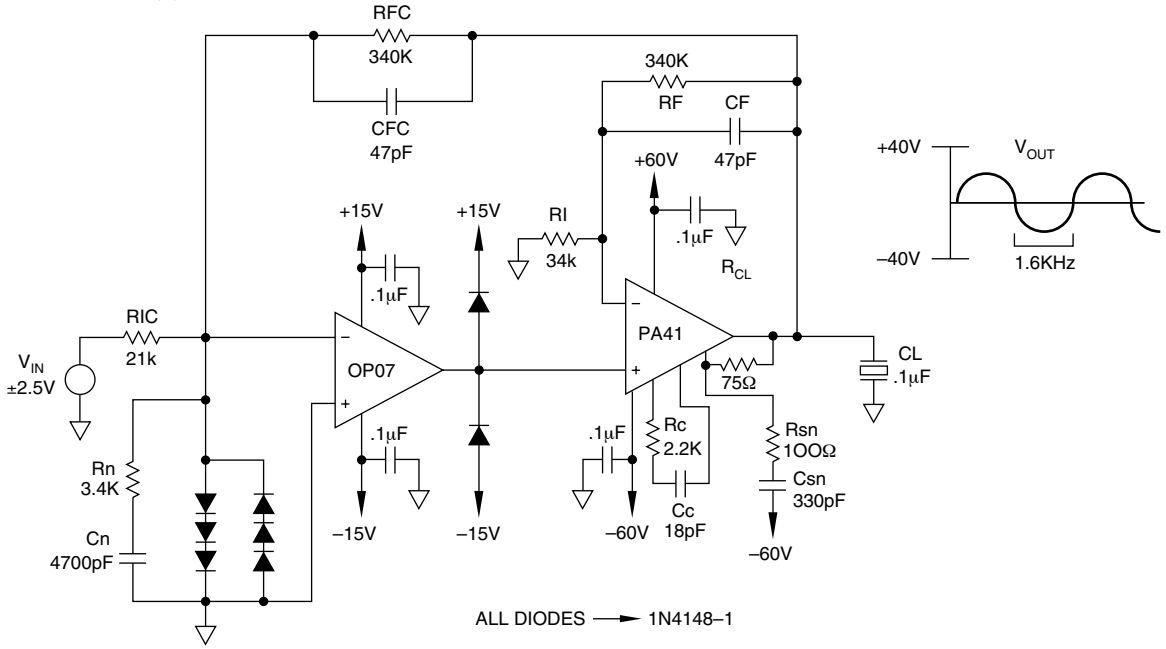
Reference PA83 Data Sheet



SIMPLE PIEZO ELECTRIC TRANSDUCER DRIVE

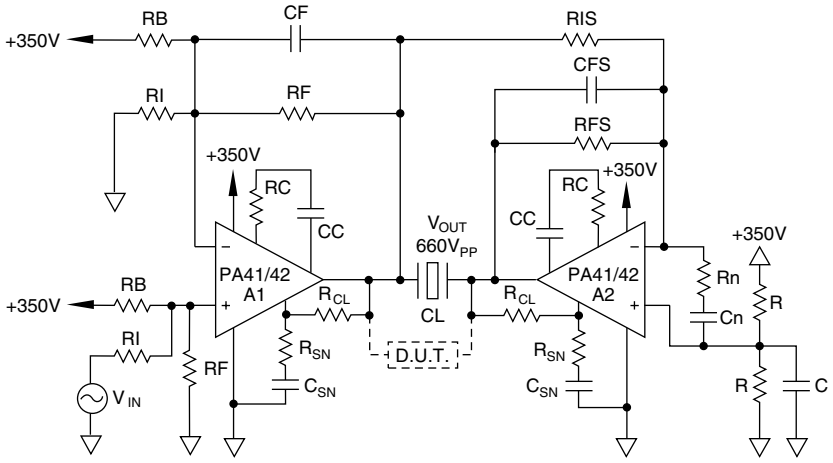
PA41

Reference App Note 25, Technical Seminar: Piezo



COMPOSITE PIEZO TRANSDUCER DRIVE

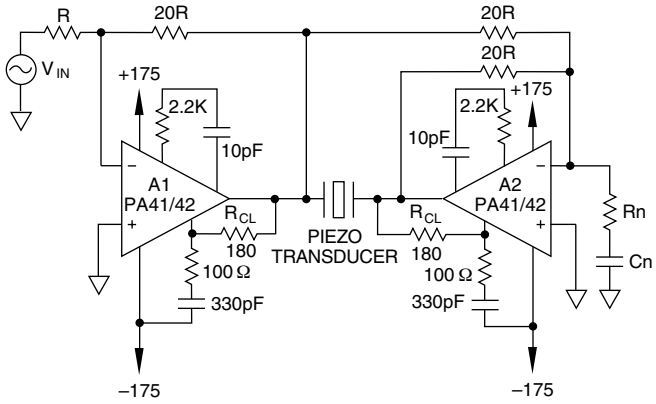
PA41/PA42



SINGLE BRIDGE

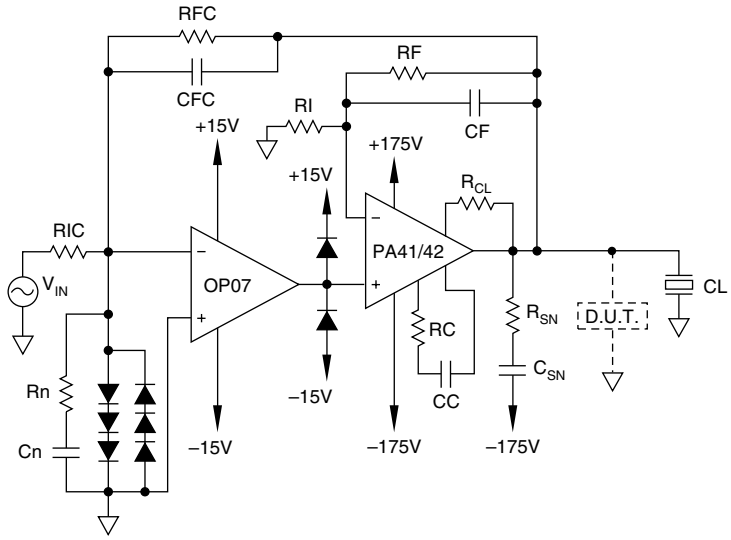
MICROMOVEMENT

PA41/42



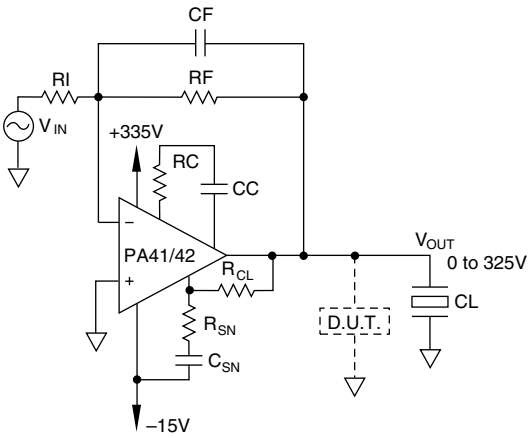
LOW COST 660V p–p PIEZO DRIVE

PA41/PA42



HIGH ACCURACY COMPOSITE

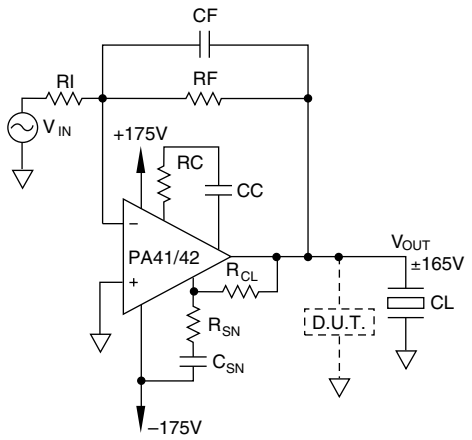
PA41/PA42



ASYMMETRICAL OUTPUT

G

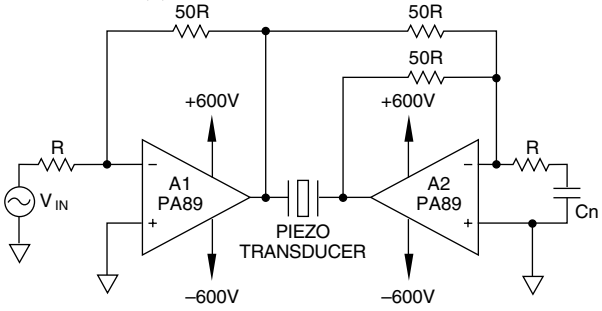
PA41/42



BIPOLAR OUTPUT

PA89

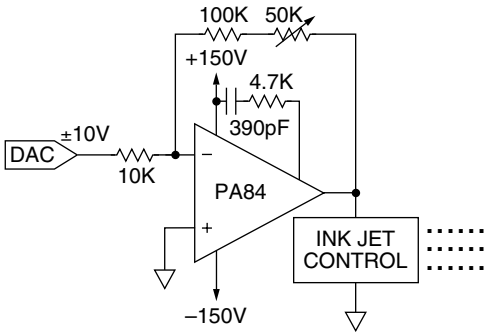
Reference App Note 25



SINGLE AXIS MICRO-POSITIONING, ±1150V

PA84

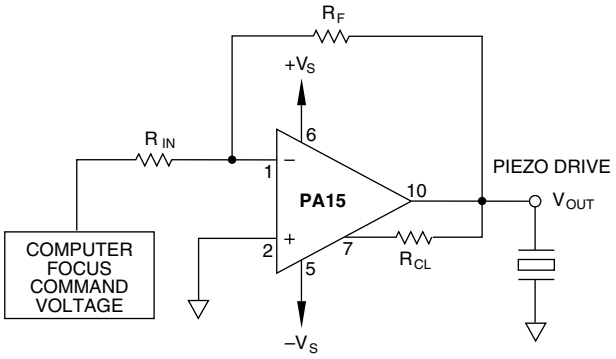
Reference PA84 Data Sheet



PIEZO PRINTER DRIVER

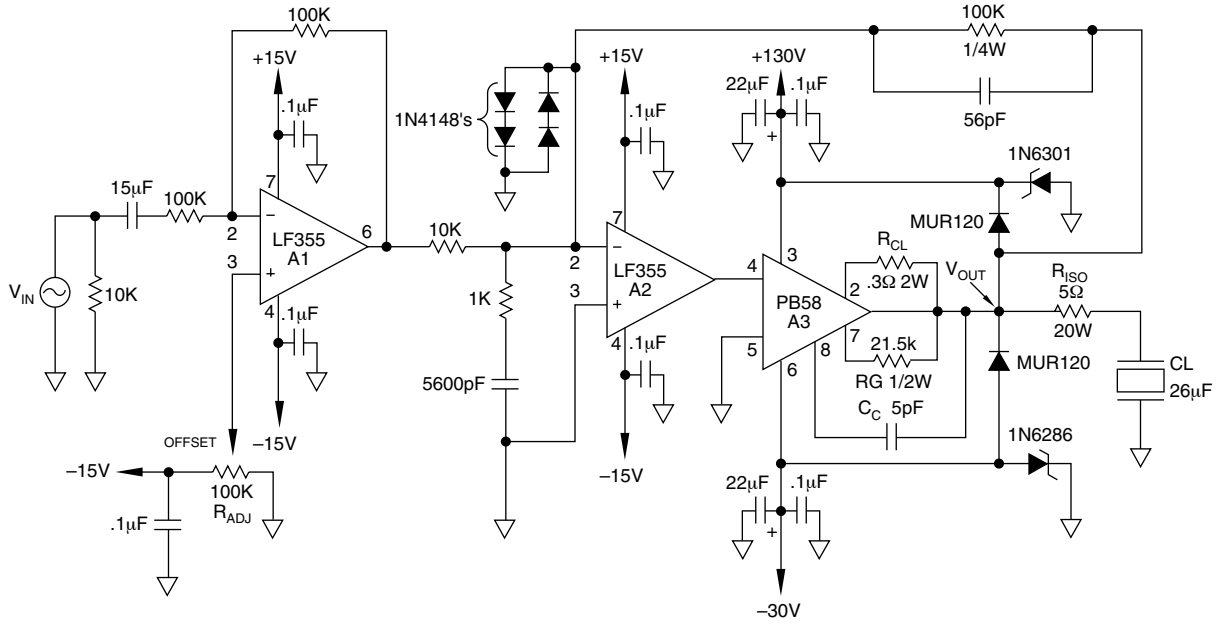
PA15

Reference PA15 Data Sheet



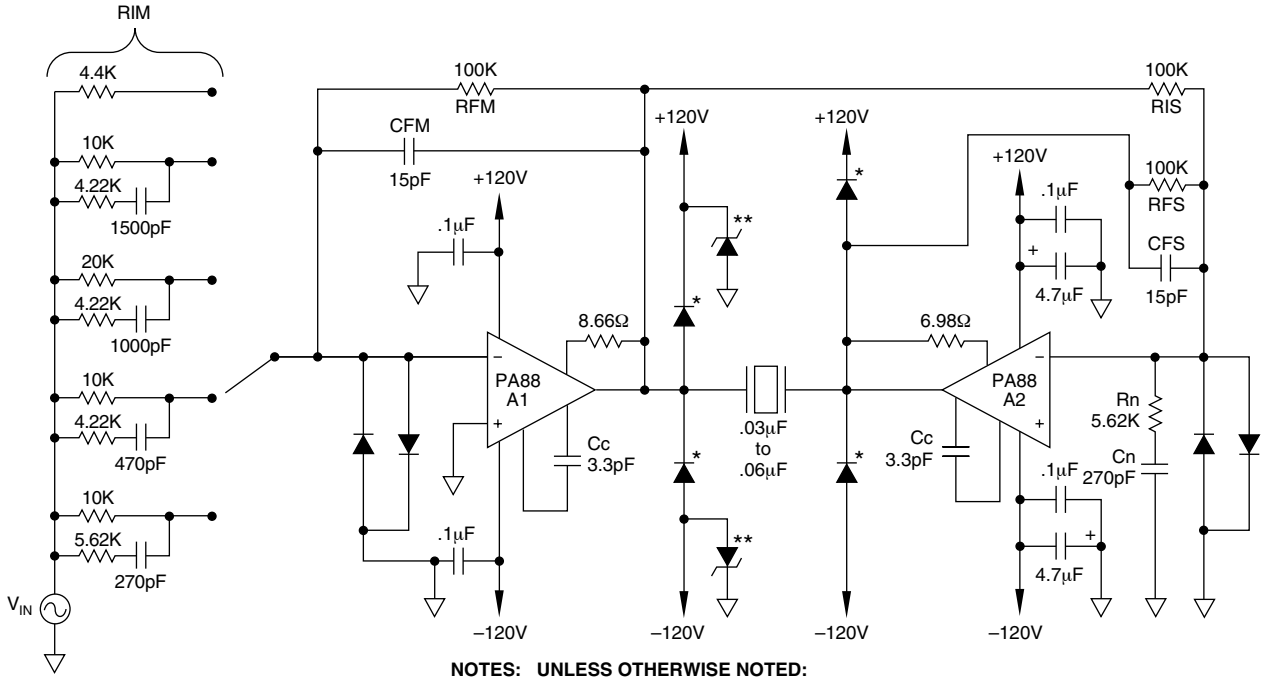
LOW POWER, PIEZOELECTRIC POSITIONING

PB58
Reference App Note 25



PIEZO DRIVER WITH RISO

PA88
Reference App Note 25



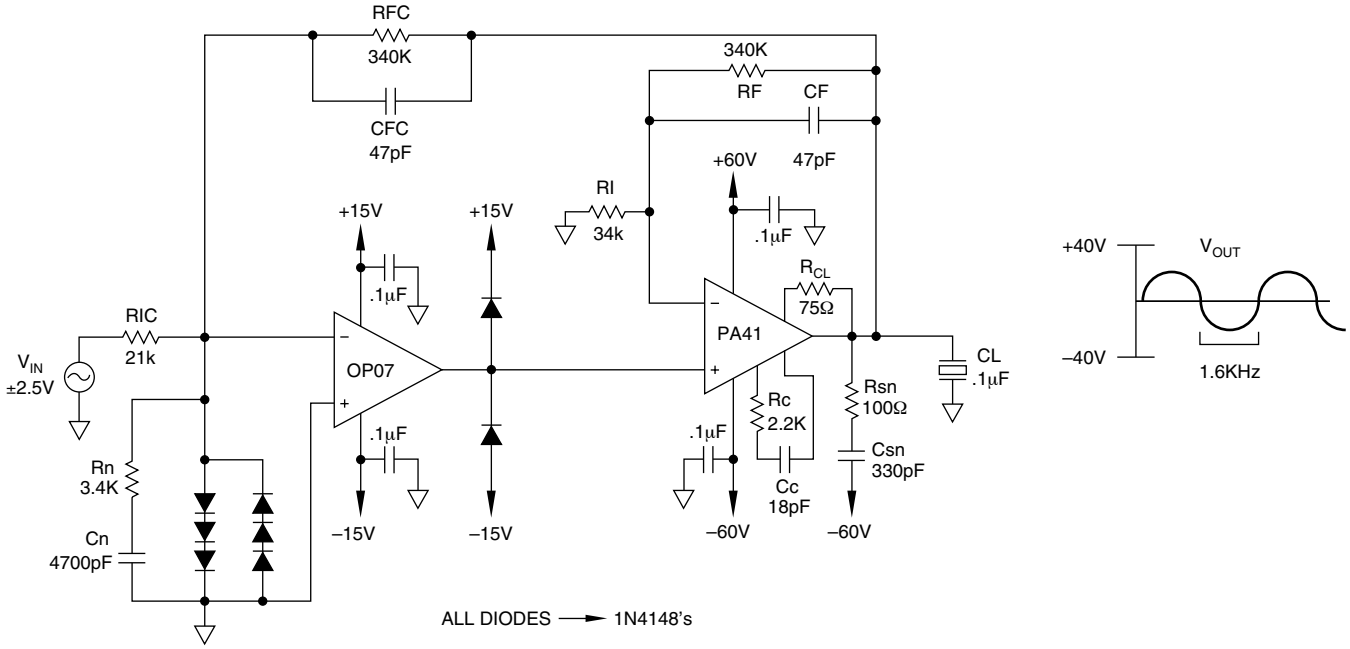
NOTES: UNLESS OTHERWISE NOTED:
1) ALL DIODES ARE 1N4148; *DIODES = 1N5617; **TRANSZORBS = 1N6300 or 1.5KE160
2) USE HS02 HEATSINK @ 25°C AMBIENT

BRIDGE PIEZO DRIVE WITH SELECTABLE GAIN

G

PA41

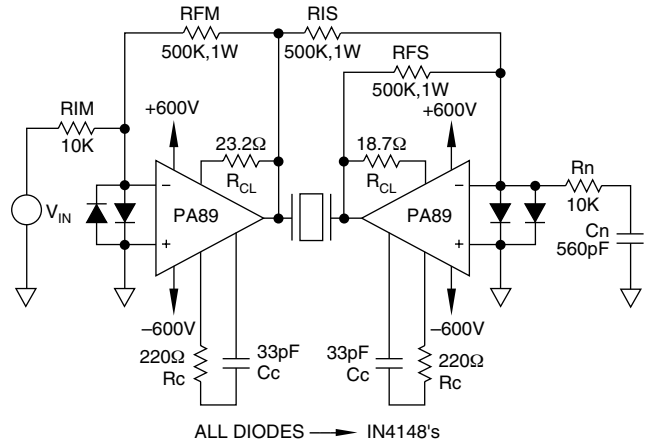
Reference App Note 19, App Note 25, Technical Seminar: Piezo



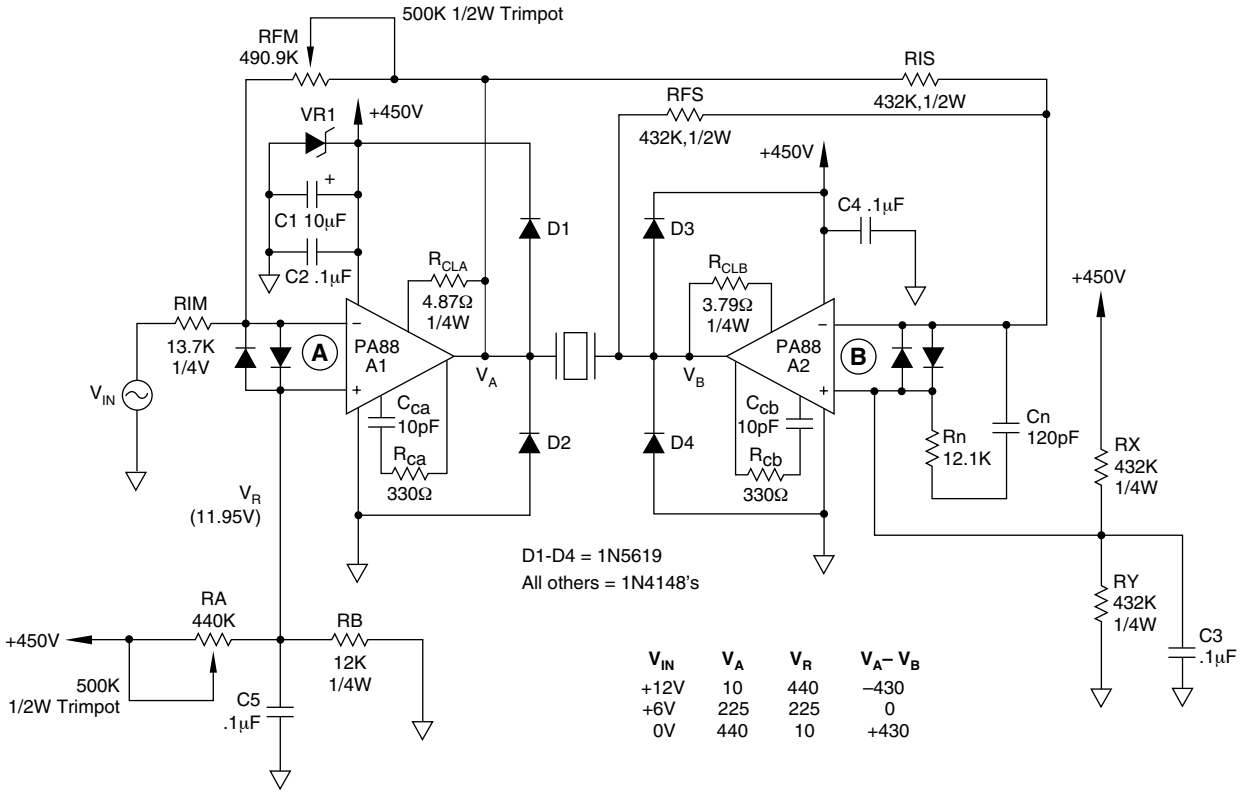
COMPOSITE PIEZO TRANSDUCER DRIVE

PA89

Reference App Note 25, Technical Seminar: Piezo



±1160V PIEZO DRIVE BRIDGE



860Vpp PIEZO DRIVE SINGLE SUPPLY BRIDGE

NOTES:

APPLICATION NOTE 1

SAVE HOURS OF VALUABLE TIME

This applications information is intended to save you hours (maybe days) of hard work and avoid many frustrating experiences with power circuits. We highly recommend that you take the small amount of time required to read this section so that you can avoid the common pitfalls in designing and testing power operational amplifier circuits. As a minimum, you should read all *oblique print* and the first paragraph in each numbered subsection. The majority of these problem areas have been identified from APEX Applications Hotline discussions of actual circuits. They range from higher than expected errors to total destruction of the amplifier.

1.0 ELECTROSTATIC DISCHARGE (ESD) PRECAUTIONS

All APEX amplifiers should be handled using proper ESD precautions! MOSFET amplifiers are especially susceptible to ESD damage and many of our amplifiers are MOSFET designs. Most of our bipolar designs use small geometry transistor input stages, which are vulnerable to ESD.

ESD damage causes a wide range of effects, from increased voltage offset or bias currents to total destruction. APEX manufactures its products in a tightly controlled, anti-static environment and ships its products in anti-static packaging. Strict ESD precautions from receiving inspection through final assembly at your facility must be followed. Some areas which will require ESD prevention measures include personnel, tabletops, stocking containers, floors, soldering irons, and test equipment.

2.0 BEFORE YOU APPLY POWER

In the design/prototype phase of an application, many dangers exist which will be eliminated by the time the circuit is ready for production. Pins may be wired in reverse order, connections may be missing, or test probes may cause momentary shorts. Any of these can destroy power amplifiers or other components in short order.

Five procedures can be employed to substantially reduce these dangers:

1) *Set power supplies to the minimum operating levels allowed by the data sheet.*
2) *Set amplifier current limit to very low levels* (i.e. use a current limit resistor of approximately 2.2 ohms for high current models and 47 ohms for high voltage models). Consult Section 5, **"Current Limit,"** as well as the individual data sheet to determine the proper values for the current limit resistor(s). *Do not depend on the variable current limit feature of your lab power supply for protecting the amplifier.*

   It is much safer to install current limit resistors. Setting the current limit to a low value on a commercial lab supply will not protect the amplifier against the surge current available from the output filter capacitors. Even when average power dissipation is low, SOA violations can occur due to secondary breakdown of bipolar output stages. This mode of output stage destruction results from simultaneous application of high current and voltage to the conducting transistor. See Section 6 on SOA and the individual data sheets to better understand SOA limits.
3) *Check for oscillations.* With low voltage applied and reduced current limits in place, set the input signal to zero and connect a wide bandwidth (100 MHz or greater) oscilloscope to the output of the op amp. With the time base set to the microsecond region, check for oscillations present at any amplitude settings. Next, inject a signal into the circuit and monitor the output for oscillations. Excessive ringing on small signal square wave response indicates marginal stability.

   If an oscillation is found, measure the frequency and amplitude of oscillation. Also note whether the oscillation only shows up on the positive or negative half of the output. Refer to Section 10, **"Stability,"** for diagnosing and fixing the cause of instability.

   With low voltage applied and reduced current limits in place, the basic function of the circuit can be verified. Once the circuit is operating as desired, raise the current limit and check worst case operating conditions, i.e. motor reversal, square wave drive of reactive loads, or driving the output to $V_S/2$ for resistive loads. Only then should you gradually raise the supply voltages to the maximum while checking worst case operation. This procedure not only saves many failures but it also helps to pinpoint problems to specific voltages and power levels.
4) *Use the largest possible heatsink for your prototype work.* This precaution provides the best environment to make thermal measurements on the case of the amplifier during worst case loading conditions without premature failures from thermal overload. Once you verify your calculations, you may decide to use a smaller heatsink for your final circuit. Consult Section 7, **"Internal Power Dissipation And Heatsinking,"** for information on calculating heatsink requirements for your application.
5) *Avoid switching while the circuit is under power.* This includes plugging/unplugging banana jacks, switching relays in high current lines, switching within a feedback loop, etc. See Sections 9.1 and 9.3 for a further discussion of the dangers of switching.
6) When using an externally compensated amplifier, be aware that the compensation capacitor will be stressed to nearly the total supply voltage. A check of the equivalent circuit diagram will show one compensation terminal is within a few volts of one of the supply rails (often connected to the gate of a FET) and the other is very close to the output voltage. At 300V and below, normal voltage margins are adequate. Above this it is advisable to rate the capacitor at twice the supply voltage. In this area, partial discharge and corona effect can take place. A good way to visualize the problem is to think of little packets of energy jumping across the capacitor. The FET gate can be destroyed long before incremental damage to the capacitor is ever seen.

3.0 ABSOLUTE MAXIMUM SPECIFICATIONS

Amplifiers should always operate below their Absolute Maximum Ratings to prevent permanent damage. If operation results in one of these maximums being reached, no permanent damage will result. *Simultaneous application of two or more of these maximum stress levels may result in permanent damage to the amplifier.* Note that proper operation is only guaranteed over the ranges listed in the Specifications table.

Example: Most amplifiers have an Absolute Maximum case temperature rating of +125°C. If the Specifications table gives an operating temperature range of up to +85°C, then the parameter limits in the Specifications table are not valid between +85°C and +125°C. In addition, the amplifier may not even be operational in this range, (for example, the amplifier may latch to one of its supply rails when above +85°C). However, the device will not sustain permanent damage unless the latched condition also violates the safe operating area.

The absolute maximum power dissipation rating used by APEX is the generally accepted industry method which assumes the case temperature of the amplifier is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick when comparing ratings of various manufacturers. However, it is not a reasonable operating point because it requires an ideal (infinite) heatsink. Furthermore, even with the best heatsink, *sustained operation at the maximum rated junction temperature will result in reduced product life.* Refer to Section 7, **"Linear Power Dissipation And Heatsinking,"** for information regarding operating junction temperatures and relative product life. APEX generally recommends operating at a case temperature that keeps maximum junction temperatures at 150°C or below.

Absolute Maximum Common Mode Voltage is another rating that illustrates the difference between the rated absolute maximum and the specified operating range. On many amplifiers, the rated absolute maximum voltage applied to both inputs simultaneously is equal to the power supply voltage. However, the linear operating range is 5V to 30V less than each power supply rail. This means that inputs exceeding the linear range specification will not damage the part but the amplifier may not achieve the specified rejection ratio, may start to distort the signal, or could even latch the output to one of the supply rails.

For more information on specifications and limits, see Section 9, **"Amplifier Protection And Performance Limitations,"** Section 6, **"SOA,"** Section 4, **"Power Supplies,"** and the **"Parameter Definitions"** section.

4.0 POWER SUPPLIES

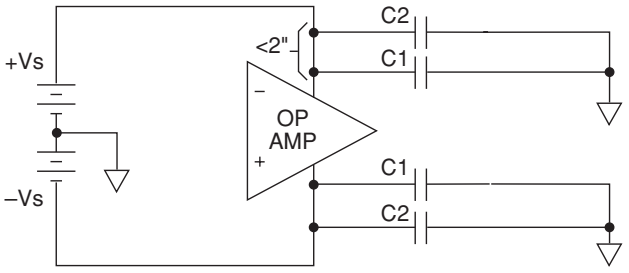
4.1 VOLTAGE SPECIFICATION

The specified voltage (±Vs) applies for a dual supply having equal voltages (±30V). An asymmetrical (+50V/–10V) or a single supply (60V) may be used as long as the total voltage between +Vs and –Vs does not exceed the maximum rating. Never allow reverse voltage on a supply pin. On a dual supply circuit, do not operate with only one supply connected.

4.2 POWER SUPPLY BYPASSING

Inadequate power supply bypassing can lead to power amplifier circuit oscillations. Each supply pin should be bypassed to common with a "low frequency bypass" capacitance of 10µF per Ampere of peak output current. Tantalum capacitors should be used, although computer grade aluminum electrolytics can be substituted for operating temperatures above 0°C.

In addition, a "high frequency bypass," .1µF to 1µF ceramic capacitor, should be added in parallel with the low frequency bypass capacitors from each supply rail to common. Refer to Figure 1. The ceramic capacitors must be mounted as close as possible (1/4" is good) to the supply pins. The larger capacitors should be within a few inches.

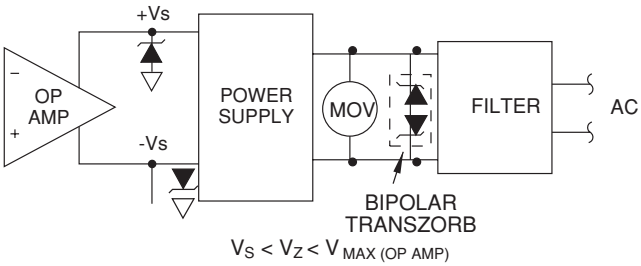


C1 = .1 to .1∝F, Ceramic, High Frequency Bypass
C2 = 10∝F/Amp out (peak), Electrolytic/Tantalum, Low Frequency Bypass

FIGURE 1. POWER SUPPLY BYPASSING

4.3 OVERVOLTAGE PROTECTION

The amplifier should not be stressed beyond its Absolute Maximum supply voltage rating. The amplifier should be protected against any condition that may lead to this voltage stress level. Two common sources of overvoltage are the high energy pulses from an inductive load coupled back through flyback diodes into a high impedance supply and AC main transients passing through a power supply to appear at the op amp supply pins.



$V_S < V_Z < V_{MAX\ (OP\ AMP)}$

FIGURE 2. OVERVOLTAGE PROTECTION

Unipolar devices also protect against reverse polarity. Note that an open supply pin can cause supply reversal and sometimes amplifier destruction. Transient suppressors with a voltage rating greater than the maximum power supply voltage expected but less than the breakdown voltage of the amplifier will prevent the amplifier from damage.

Transients from the AC mains can be clamped through the use of MOVs (Metal Oxide Varistors) such as those made by General Electric, or bipolar TransZorbs. Connect either of these devices across the inputs to the power supply to reduce transients before they reach the power supply. Low pass filtering can be done between the AC main and the power supply to cut down on as much of the high frequency energy as possible. Note that inductors used in power supply filters will pass all high frequency energy and capacitors used in the filter are usually electrolytics which have high ESR. Because of this high ESR, high frequency energy will not be attenuated fully and therefore will avoid the capacitor with little reduction. Refer to Figure 2.

5.0 CURRENT LIMIT

The primary function of current limit is to keep an amplifier within its SOA. See Section 6, **"Safe Operating Area."** Some models of Apex Power Op Amps have an internal current limit, while most of our models have an adjustable limit that is set with one or two external resistors.

Any attempt to limit current with a circuit external to the amplifier must be approached with extreme caution. The pitfalls are generally time related and are often catastrophic. Most power supply current limit circuits are effective only AFTER stored energy in a large output filter capacitor has been depleted. This energy plus energy in local supply bypass capacitors is often more than enough to destroy the amplifier.

Slow response time is also a problem with even the fastest fuses. A 15 second response time to a 200% over current is common. In most applications the amplifier will give its life protecting the fuse. Even if the fuse does blow, the amplifier may still be damaged. The blowing fuse is a mechanical interuption in a current carrying line which can cause voltage spikes above the supply rating of the amplifier.

5.1 CURRENT LIMIT PRECISION

Standard current limit circuitry is not designed to provide a precision current limit function. A rule of thumb is to allow ±20% variation at room temperature. Furthermore, the current limit varies over temperature. This temperature dependence is generally shown in a typical performance graph in the product data sheet. Specific values of the nominal current at any given temperature may be calculated by modifying the 0.65V term of the current limit equation given in Section 5.3 with –2.2mV per degree (Centigrade) of case temperature rise above 25°C. For example, at a case temperature of 125°C, this term becomes 0.43V rather than 0.65V; (650mV–(125°C–25°C)(–2.2mV)). When working with high currents, the impedance of PCB traces, lead lengths and solder joints must be included in the current limit calculations.

5.2 EXTERNALLY ADJUSTABLE CURRENT LIMIT

Models with provisions to adjust current limit externally must have the current limit resistors connected as shown in the external connection diagram.

Current limit should never be set at a value greater than the rated maximum output current of the power op amp. This maximum is due to the current density limitations of conductors in the package and exceeding it can destroy the amplifier. Also, using a very low resistance (such as a jumper wire) will lead to increased bias current in the output stage. This raises power and temperature, while lowering resistance to second breakdown, thereby destroying reliability.

Operation without current limit resistors installed (current limit pins left open) can also cause failures, especially with inductive loads. This includes even a momentary open circuit while switching current limits with mechanical contacts. For the high current series power op amps, minimum programmed limits should be 20mA, while 10mA is minimum for most of the high voltage, low current series. Open circuits or limits below these minimums can cause voltage breakdown of the current limit transistors.

5.3 CALCULATING CURRENT LIMIT

Power op amps with provisions to adjust current limit externally require one or two current limit resistors (R_{CL}) which must be connected as shown in the applicable external connection diagram below. Since output current flows through these resistors, wattage ratings must be considered. For optimum reliability, the resistor values should be set as high as possible. Some amplifier data sheets provide model specific equations, but in general each resistor and its power dissipation is calculated as follows:

$$R_{CL}\ (\text{ohms}) = \frac{0.65}{I_{LIM}\ (\text{A})}$$

$$P_{R_{CL}}(\text{watts}) = 0.65 \bullet I_{LIM}$$

I_{LIM} is the value of current limit desired and should be chosen to provide the amount of protection required for the specific application. For details on choosing "safe" levels of current limit and the protection/performance trade offs involved, see Section 6.3, **"Fault Protection Using Current Limit."**

For two resistor current limit schemes, asymmetrical current limiting ($R_{CL+} \neq RC_{L-}$) is permissible.

Foldover current limit, discussed in detail in AN #9, Current Limiting, provides a lower current limit for short circuit conditions while increasing current limit for load drive. APEX power amplifiers, the PA10, PA12 PA04 and PA05, have this feature. Foldover reduces the protection/performance trade-off inherent in setting current limit. The Power Design Tool will calculate and plot current limit on an SOA graph for most linear amplifier models. It is available free at www.apexmicrotech.com.

6.0 SAFE OPERATING AREA (SOA)

6.1 READING THE SOA GRAPH

The horizontal axis on the SOA curve, V_S–V_O, defines the voltage stress across the output device that is conducting. It does n*ot* define a supply voltage or total supply voltage or the output voltage. V_S–V_O is the magnitude of the differential voltage from the supply to the output across the transistor that is conducting current to the load. Put another way: if the amplifier is sourcing current, use $(+V_S)$–V_O. If the amplifier is sinking current, use $(–V_S)$–V_O. Refer to Figures 3a & 3b.

The vertical axis represents the current that the amplifier is sourcing or sinking through the Output pin.

The Safe Operating Area curves show the limitations on the power handling capability of the amplifier. Refer to Figure 4. There are three basic limitations:

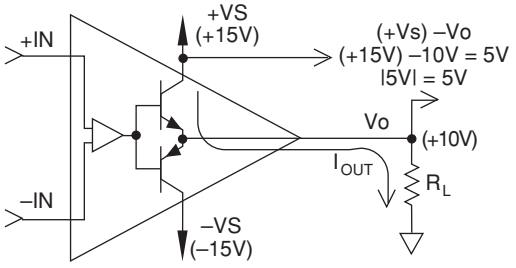


FIGURE 3A. *SOURCING* CURRENT

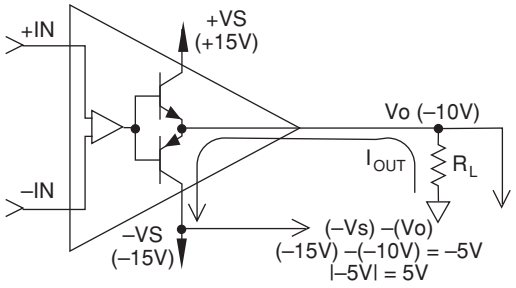


FIGURE 3B. *SINKING* CURRENT

1) *Current handling capability. T*his horizontal line near the top of the SOA CURVE represents the limit on output current imposed by current density constraints in the wire bonds, die junction area and thick film conductors.
2) *Power dissipation capability.* This is the power dissipation capability of the amplifier output stage. Note that the product of output current on the vertical axis and V_S–V_O on the horizontal axis is constant over this line. In other words, this portion of the SOA curve is a "constant power line." For $T_{C\,=}$ 25°C, this line represents the maximum power dissipation capability of the amplifier at maximum junction temperature using an infinite heatsink. As case temperature increases, this constant power/thermal line moves toward the origin. The new constant power line can be determined from the Power Derating curves on the data sheet. The case temperature is primarily a function of the heatsink used. For more details, refer to Section 7, **"Linear Power Dissipation And Heatsinking."**
3) *Second Breakdown.* Second breakdown is a phenomenon exhibited by bipolar transistors when they are simultaneously stressed with high collector-emitter voltage and high collector current. Non-uniform current density in the emitter results in localized heating and "hot spots" at the junction. The temperature dependence of junction current results in increased current density at the hot spots. This concentration of current tends to further increase the temperature. The process is cumulative, leading to thermal runaway and transistor failure. Note that MOSFET power transistors do not have this second breakdown limitation.

The transient second breakdown lines (t = 0.5ms, t = 1ms, and t = 5ms) are based on a 10% duty cycle. For instance, in Figure 4, the amplifier may deliver 1.5A at a V_S–V_O of 60V for 5ms but then must wait for 50ms before repeating this stress level. It is highly recommended to avoid entering the region beyond the DC second breakdown limits. Operation outside steady state limits in transient SOA regions is difficult to analyze adequately enough to insure best possible reliability.

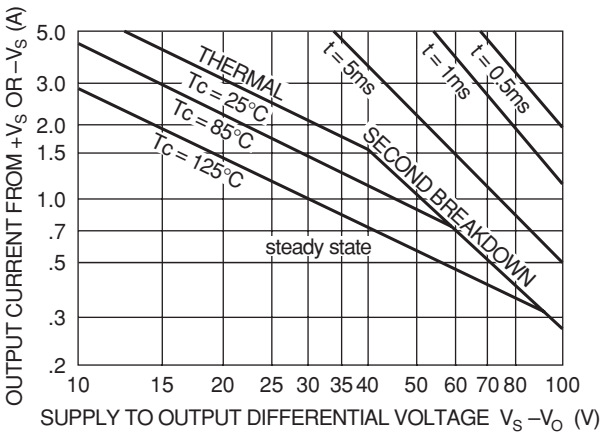


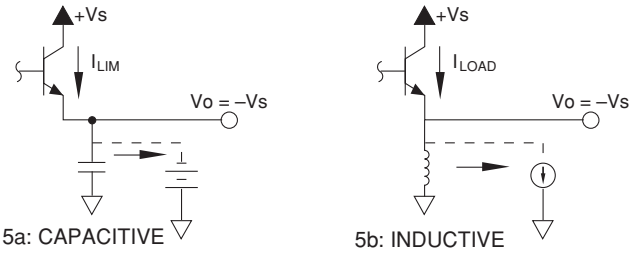
FIGURE 4. TYPICAL SOA CURVE

6.2 HIGH SOA STRESS CONDITIONS

For resistive loads tied to ground, calculating power dissipation in the amplifier is reasonably simple. Refer to Section 7.1, **"DC Power Dissipation,"** and Section 7.2, **"AC Power Dissipation."** However, with reactive loads, the voltage/current phase difference results in higher power being dissipated in the amplifier.

An example of an excessive transient stress condition created by a capacitive load is shown in Figure 5a. In this case the capacitive load has been charged to $–V_S$. Now the amplifier is given a "go positive" signal. Immediately the amplifier will deliver its maximum allowed output current (IL_{IM}) into the capacitor, which can be modeled at time t=0+ as a voltage source. This leads to a voltage stress across the conducting device equal to the rail-to-rail supply voltage. Simultaneously, the amplifier will be conducting its maximum (current-limited) value of current.

Figure 5b shows a similar transient stress condition for an inductive load. For this situation we imagine the output is near the positive supply and current through the inductor has built up to some value I_{LOAD}. Now the amplifier is given a "go negative" signal which causes



5a: CAPACITIVE 5b: INDUCTIVE

FIGURE 5. TRANSIENT STRESS WITH REACTIVE LOADS

the output voltage to swing down to the negative supply. However, the inductor at time t=0+ can be modeled as a current source that requires the amplifier to continue to source $I_{LOAD.}$ This leads to the same situation as before, that is, total supply voltage across a device conducting maximum rated current.

Note also that reactive loads cause higher thermal stress levels than resistive loads even under steady state sinusoidal conditions. *For purely reactive loads, all of the power is dissipated in the amplifier, none in the load.*

6.3 FAULT PROTECTION USING CURRENT LIMIT

With a given supply voltage, current limit can be used to keep the amplifier within its Safe Operating Area. This allows amplifier protection during fault conditions such as shorts to ground or shorts to either supply. The cost of protection is lowered output current capability.

For short-to-ground fault protection, set current limit to the value given by the intersection of the supply voltage and the DC SOA curve for the appropriate case temperature. Simply find the supply voltage on the horizontal axis. When the output is shorted to ground, V_O = 0; therefore, V_S–V_O = V_S, follow up to the SOA curve intersection and then across to the output current. Referring to Figure 6, we see that in this example, a 2A current limit provides short circuit protection to ground at a case temperature of 25°C with ±30V supplies. Note that better heatsinking allows higher values of current limit.

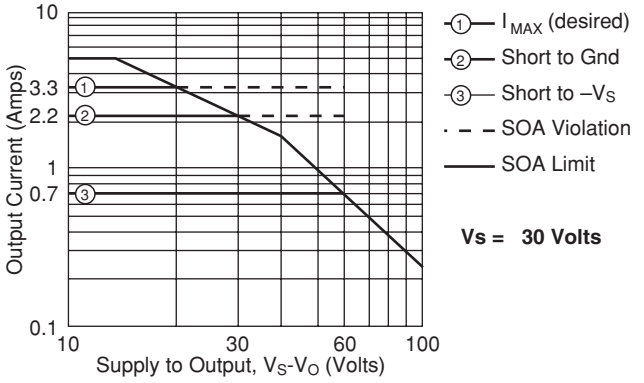


FIGURE 6. CURRENT LIMIT FAULT PROTECTION

For short-to-either supply protection, set current limit to the value given by the intersection of the rail-to-rail supply voltage (V_{SS}) and the DC SOA curve. This requires a significant lowering of current limit. For this type of protection, add the magnitudes of the two supplies used, find that value on the V_S–V_O axis, follow up to the SOA limit for the case temperature anticipated, then follow across to find the correct value of current limit. Referring to Figure 6, we see that in this example, a 0.7A current limit allows short protection to either supply.

It is often the case that requirements for fault protection and maximum output current may conflict. Under these conditions there are only four options. The first is to simply go to an amplifier with a higher power rating. The second is to trim some of the requirements for fault protection. The third is to reduce the requirement for maximum output current. The fourth option is a special type of current limit called "foldover" or "foldback." This is available on some amplifiers such as the PA10 and PA12. For a detailed discussion of foldover current limit and SOA fault protection refer to Application Note 9, "**Current Limiting.**" For an explanation of how to choose current limit resistors to adjust current limit, see Section 5.3, "**Calculating Current Limit.**"

7.0 LINEAR POWER DISSIPATION AND HEATSINKING

It is important to not confuse Internal Power Dissipation with power delivered to the load. These two power levels are equal only at unique signal levels. Low impedance faults or highly reactive loads will likely result in internal power dissipation being the higher level. Well-designed circuits with less reactance will yield higher efficiency.

There are two main steps in the heatsink selection process. First, the maximum internal power dissipation must be calculated. Secondly, the maximum desired junction and case temperatures must be chosen and the thermal model used to calculate the required thermal conductance of the heatsink. The following four sub-paragraphs deal with finding internal power dissipation in the output transistors generated by delivering current to the load only.

For purposes of power dissipation calculation, DC refers to any signal with a frequency below 60HZ. At true DC, heat is generated in only one output transistor and ability to conduct this heat to the surface of the amplifier case is determined by thermal conductance of materials and square area. As frequency increases, our original transistor now has a time variable heat load and the opposite side output transistor now generates the heat on alternate half cycles. This means the wattage figure can move from peak value toward RMS and more square area is used to conduct heat to the case, implying a lower thermal resistance. At 1HZ, internal thermal time constants are so fast compared to the half-second duration of the conduction cycle of each transistor, that no advantage gained. At 1KHZ, conduction cycles are short compared to internal time constants and thermal averaging allows taking advantage of both RMS power levels and the lower thermal resistance. While physics produces a smooth curve between these frequencies, the math is quite cumbersome. Most manufacturers of power op amps have adopted the 60HZ rule: Below 60HZ, use peak power and DC thermal resistance; otherwise use RMS power and AC thermal resistance.

7.1 DC POWER DISSIPATION

Power in the output transistor is the output current multiplied by the voltage across that transistor, or supply-to-output differential, Vs - Vo. For a purely resistive load, maximum power dissipation occurs at Vo = 1/2Vs and has a value of:

$$PD\ (max) = \frac{Vs^2}{4R_L}\ \text{[Purely resistive load only]}$$

Where:

Vs is the supply magnitude of the conducting transistor.

R_L is the load resistance.

For AC signals below 60HZ driving reactive loads, plot the load line to find stress levels. Use the highest power level from the plot for heatsink selection. Application Note 22 discusses SOA and Load Lines. As an example, consider the PA12A, ±48V supplies, ±40V signal at 50HZ driving a 69mH coil with 12.5Ω resistance, mounted on a 0.3°C/W heatsink. Figure 7 is the load line for this circuit with peak internal dissipation of 67.5W at 1.28A. Load impedance is 25Ω at 60° resulting in apparent power of 32VA and a power factor of 0.5. Quite a limitation for an amplifier boasting an ABSOLUTE MAXIMUM RATING of 125W! The software secret behind this plot will be revealed later.

ELECTRICAL MEASUREMENT METHOD

Although we present this under the DC heading and it is primarily used at low frequencies, instrumentation errors are the only limitations on frequency. The ideal way to run this test is to have an amplifier/heatsink combination you are certain is large enough to handle all the power. While this may sound like circular cells in a spreadsheet, the test still has its place. Many loads do not change impedance with changing drive amplitude. If this is true, it is possible to replace the power amp in Figure 8 with a signal generator or a low power amplifier. Set the drive signal to a convenient fraction of

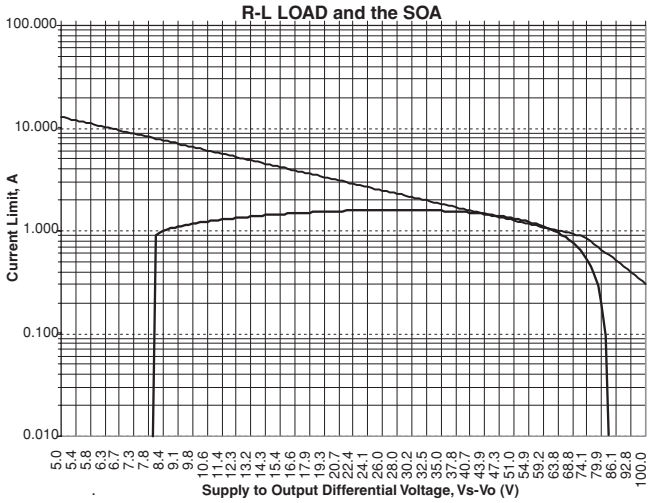


FIGURE 7

the ultimate level, and rescale the voltages and currents measured prior to calculating power levels. If using a programmable signal generator, the actual output amplitude is not likely to match the programmed level because the load impedance is not likely to match

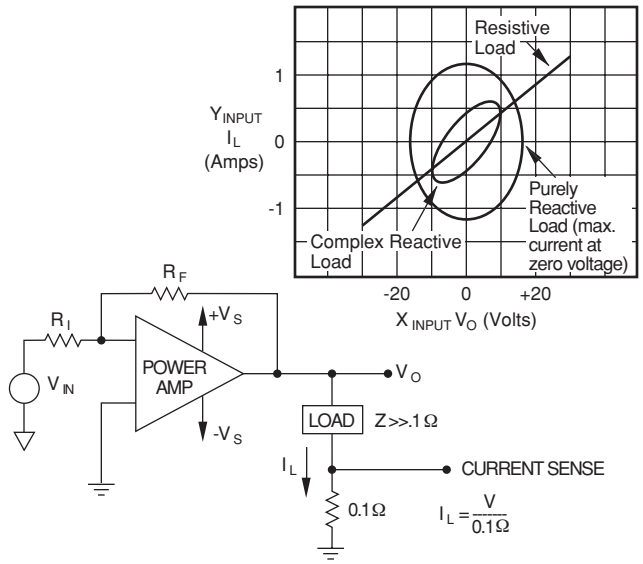


FIGURE 8. AC PD_{OUT} : ELECTRICAL MEASUREMENT

the generator output impedance.

1. Use a small value current sense resistor between the load and ground to develop a voltage proportional to I_L. Use this signal to drive one channel of the X–Y display of an oscilloscope.
2. Use the output voltage of the amplifier, V_O, to drive the other channel of the X–Y display.
3. Calculate instantaneous power dissipation in the amplifier for several points on the ellipse using:

$$PD_{OUT} = (V_S - V_O)I_{LOAD}$$

4. Plot the points on the SOA curve and check for violations.

7.2 AC POWER DISSIPATION

Again, "AC" for the purpose of determining power dissipation means at least 60HZ. For the moment, we will also confine the discussion to sinusoidal signals and symmetric supplies. Starting with the simple: When driving a pure resistance, power dissipation is maximum when the sine wave peak is 0.637*Vs. Refer to Figure 9 to see how the heat load on the amplifier decreases as signal amplitude varies in either direction. This equation yields maximum power:

$$PD(max) = \frac{2V_S^2}{\pi^2 R_L} \text{ [Purely resistive load only]}$$

Where:
V_S is the magnitude of each supply.
R_L is load resistance.

SIMPLE APPROXIMATION FOR REACTIVE LOADS

As loads move from pure resistance toward pure reactance, three changes should be noted:

1) The fraction of Vs corresponding to maximum power dissipation goes from 0.637 toward one. See Figure 10.

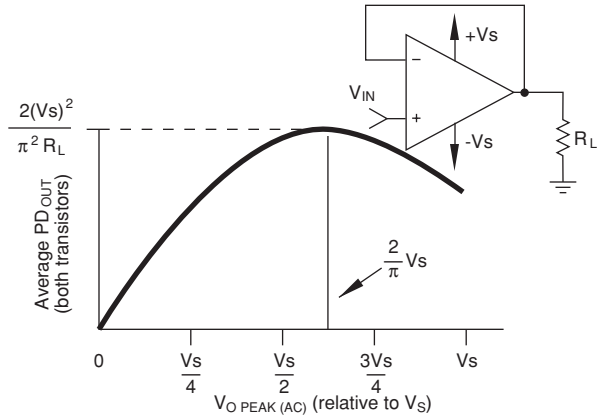


FIGURE 9. AC POWER DISSIPATION VS. PEAK OUTPUT VOLTAGE

2) Power factor goes from one toward zero. With a pure reactance, no heat is generated in the load (no work is done).
3) The difference between load VA and true watts is dissipated in the amplifier.

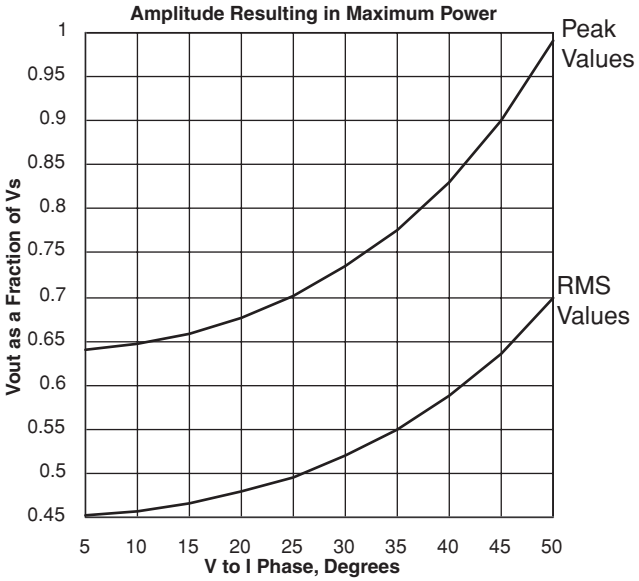


FIGURE 10. AMPLITUDE PRODUCING MAXIMUM POWER MOVES WITH PHASE ANGLE

Even with these changes, one of the two following formulas can be used to approximate internal power dissipation. The key is knowing the phase difference between V & I in the load, to find the power factor, COSØ. With only one reactive element in the load it is easy to determine what frequency will produce the largest power dissipation. With the power factor and load impedance measured or calculated, the formulas are:

G

$$PD(max) = \frac{2V_S^2}{\pi^2 Z_L \cos\varnothing} \quad \text{[Pimarily resistive loads, COSØ<40°]}$$

$$PD(max) = \frac{V_S^2}{2 Z_L} \left[\frac{4}{\pi} - \cos\varnothing \right] \quad \text{[Primarily reactive loads, COSØ>40°]}$$

Where:
V_S is the magnitude of each supply.
Z_L is load impedance magnitude.

MORE ACCURATE METHODS

This method can be used analytically or on the bench as long as the test amplifier and heatsink are large enough to accommodate any errors in the first pass estimate of the circuit operation. Just as in the previous method, phase angle of the load must be known. Not only is it a term of the equations, but it is needed to determine the proper signal amplitude. Find the maximum power producing amplitude from Figure 10. If this is lower than the maximum amplitude your circuit will drive, use it. If not, use the circuit maximum.

1) Find the power delivered TO the amplifier from the supply:

$$P_{IN} = \frac{2V_S I_{PEAK}}{\pi}$$

2) Find the power delivered *from* the amplifier *to* the load:

$$P_{OUT} = (1/2)V_{PEAK}\, I_{PEAK} \cos\varnothing$$

3) Calculate power left in the amplifier:

$$PD_{INT} = P_{IN} - P_{OUT}$$

7.3 "OTHER" POWER DISSIPATION

For waveforms other than sinusoids, or for more complex energy storing loads such as motors, a Spice analysis and an electrical test method as described under DC Power Dissipation is recommended. Application Note 24, Brush Type DC Motor Drive may also prove useful.

7.4 "EASY" POWER DISSIPATION

Power Design is an Excel spreadsheet available free from www.apexmicrotech.com. It remembers all the rules and formulas presented here, has a data base of model capabilities and finds the critical phase angle for you. Answers for simple loads are tabulated and load line plotted as fast as you can enter the data. Frequency sweeps on up to 54 component complex loads take a little longer. It also does calculations in the following paragraphs on heatsink selection plus, has sheets for stability, model selection, PWM filters and PWM power dissipation.

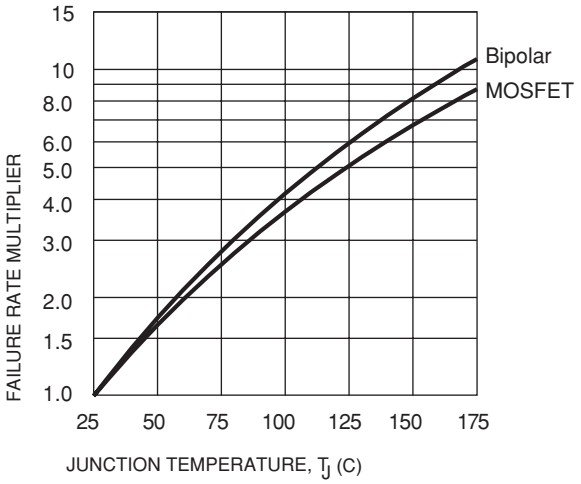
7.5 WHERE TO SET T_J MAX

For that matter, what is $T_J$max? In the ABSOLUTE MAXIMUM RATINGS area of a data sheet, it is the temperature limit set by the transistor manufacturer to insure leakage of that transistor does not become destructive. Especially on older bipolar models, 200°C appears frequently. This is not a good place to be on a continuous basis. From here on, T_J max will mean the design maximum for the circuit.

Reliability is a strong function of temperature. Figure 11, based on data from MIL-HDBK-217F, shows that a bipolar transistor operated a junction temperature of 175°C will have a mean failure rate more than ten times higher than with a junction temperature of 25°C. A MOSFET can be expected to fail almost nine times as often with the same temperature rise.

Apex has seen applications required by military contract to meet a T_J max of 100°C. More often the designer must set T_J max based on application details. Would failure eliminate one bell or whistle on a non-critical piece of equipment, or completely stop a $1M per hour production line? How about consequential damage? Is the amplifier used for 30 seconds each day, or continuously? Can the amplifier be easily replaced, or does this require a space vehicle? Simply trade off these concerns against time, size, weight and cost budgets to arrive at the perfect T_J max.

There are three approaches to lowering junction temperatures. The first is to lower internal power dissipation. Application Note 8,



This data has been extracted from the base failure rate tables of MIL-HDBK-217F, revision of 2 December 1991.

FIGURE 11. MTTF VS. TEMPERATURE

Optimizing Output Power, Notes 3 and 20 on bridge circuits and AN26 on parallel operation may prove helpful here. The second method is to lower the ambient temperature. This may involve placement choices inside an equipment enclosure or the use of a chilled liquid cooling system rather than air-cooling. Last on the list, we must minimize thermal resistance from the transistor junctions to the ambient environment.

7.6 THERMO-ELECTRIC MODELS

Thermo-electric models translate power terms into their electrical equivalent. In these models, power is modeled as current, temperature as voltage and thermal resistance as electrical resistance. Since 1980, Apex has advocated using a simplified calculation of case and junction temperatures of power op amps. This shortcut assumed quiescent power was added to power dissipated due to output current and the total is used to calculate both temperatures. This yields the correct case temperature but predicts output transistor junction temperatures higher than the real world. This error is in the *safe* direction and generally insignificant until the amplifier combines high voltage and high speed causing quiescent power to be a significant percentage of the power rating of the output transistors alone.

The more accurate model shows that adding all the quiescent power to the calculation for the output transistors is an error because quiescent power is spread among all the components of the amplifier. From the data sheet point of view, the POWER DERATING graphs show power handling capability of the output transistors only, but the simple method produces a temperature rise in the output transistors due to current which does not flow in them. In the PA94, maximum quiescent current times maximum supply voltage develops 21.6W, over 70% of the power rating of the output stage. However, less than 1% of this power is in the output stage and the simple method imposes a false but severe limitation on power handling capability of the output transistors. It is very easy to design a reliable PA94 circuit where total power dissipation is greater than that allowed by the POWER DERATING graph.

THE SIMPLE MODEL

In Figure 12, P_D is the total power dissipation, that is P_D (internal dissipation of the output transistors due only to output current) plus quiescent power of the amplifier. Quiescent power (PD_Q) is quiescent current (I_Q) * total supply voltage.

$$PD_Q = I_Q\, (+V_S + |-V_S|)$$

A MORE ACCURATE MODEL

In Figure 13, quiescent power has been split according to the actual transistors generating the heat. PD_{Qout} is only the quiescent current flowing in the output transistors. When appropriate, this specification will appear in the amplifier data sheet. Multiply this output stage quiescent current times the total supply to find worst case $PD_{Qout.}$

$$PD_{Qout} = I_{Qout}\, (+V_S + |-V_S|)$$

PD_{Qother} is the current flowing in all the other components and could be found by subtracting PD_{Qout} from PD_{Q}.

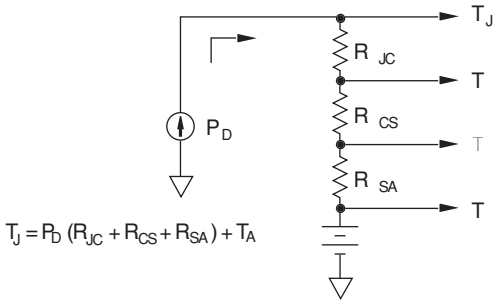


FIGURE 12. SIMPLE THERMO-ELECTRIC MODEL

Note that the data sheet junction-to-case thermal resistance speculations refer to only the output transistors. Thermal resistances and power dissipations of other components vary wildly. Design rules applied by Apex for all these components insure they will be reliable when operating within maximum supply voltage, maximum input voltage and maximum "Meets full range specifications" case temperature.

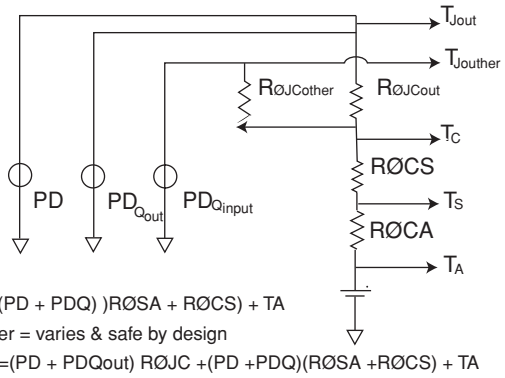


FIGURE 13. MORE ACCURATE THERMO-ELECTRIC MODEL

No matter which model you use, there are three thermal resistances contributing directly to hot junctions. The thermal resistance should be attacked on all three fronts:

1) Buy an amplifier with the lowest possible $R_{ØJC}$.
2) Use good mounting practices-see section 8 below.
3) Use the largest practical heatsink.

The amplifier is often a large portion of the thermal resistance budget. Better amplifiers usually cost more and sometimes are larger. Increased amplifier size is usually of little concern when compared to the size and weight of an adequate heatsink solution. If a larger amplifier can eliminate the need for liquid cooling or a fan, increased amplifier cost may not even be an issue. A reasonable starting point for amplifier selection is to find an ABSOLUTE MAXIMUM RATING of twice the power the circuit will actually dissipate.

$R_{ØCS}$ is often overlooked, but consider this: The PA12 with a AC thermal resistance of 0.9°C/W is mounted on the HS11 liquid cooled heatsink boasting thermal resistance of 0.1°C/W. If T_A is 25° and $R_{ØCS}$ is 0.1, 125W will place junctions at 162.5°C. If a mica or plastic washer is used or the amplifier is mounted bare, power to maintain this junction temperature could be cut to less than 70W! Again, see section 8 below.

The heatsink performance is the last element of the thermal resistance challenge. A quick glance at an SOA curve showing the power handling difference between case temperatures of 85°C and 125°C tells a story; but not the whole story. Data sheet SOA curves always assume $T_J$max is allowed to go to the ABLOLUTE MAXIMUM RATING. If your design is more conservative, the difference in power ratings will be even larger. Also be aware that heatsink ratings should be viewed more a guideline than an absolute.

7.7 HEATSINK SELECTION

Let's start with "the" heatsink rating. The HS03 is rated at 1.7°C/W in free air. True, when power dissipation is about 45W, but check the actual curve at 10W and you'll find a rating more like 2.3°C/W. On top of that, "free air" means no obstructions to air flow and the flat mounting surface must be in the vertical plane. Demands for higher performance in smaller packages can be at odds with optimum heatsinking. Poor installation choices can easily reduce effectiveness 50%.

Adding a fan to your design improves the thermal resistance rating of heatsinks. Please remember: Most fans are rated in cubic delivery and this rating varies with working pressure. A 5-inch diameter fan delivering 100 CFM produces over 700 FPM right at the fan. If this air flows through a 19 x 24 inch rack, theoretical velocity is down to 32 FPM, will vary with location and goes lower as the rack is sealed tighter.

The bottom line: Without case temperature measurements, your design effort is NOT complete!

There are two temperature limitations on power amplifiers. A rating for each limitation must be calculated and numerically lower rating used. The most obvious limitation is the junction temperature of the output transistors. The case temperature must also be limited. In addition to reliability concerns (Figure 11 applies to the front end transistors as well as the output stage), DC error budget items of voltage offset drift and bias current drift are based on case temperature. Allowing a case temperature of 85°C as opposed to 40°C will increase voltage offset change by a factor of 4 and may double the failure rate of front end semiconductors. This would be a good time to recommend reading section 3 where the difference between ABSOLUTE MAXIMUM RATINGS and "Meets full range specifications" is discussed.

Here are some case-to-heatsink thermal resistance ratings ($R_{ØCS}$) of various package styles. These ratings assume the amplifier is mounted with either an Apex aluminum thermal washer or with a thin coating of fresh thermal grease covering the entire mounting surface. If designing the mounting surface, see the ACCESSORIES INFORMATION data sheet for recommended hole sizes.

TO-3	MO-127	PD10	SIP02,3	SIP12, 04, 5 (Kapton)
0.1°C/W	0.05°C/W	0.08°C/W	0.1°C/W	0.2°C/W

Using either thermal model, the heatsink rating based on case temperature limitations is:

$$R_{ØSA} = \frac{T_C - T_A}{PD + PD_Q} - R_{ØCS}$$

Where: T_C = maximum case temperature allowed.
PD = output transistor power dissipation due to load current
PD_Q = Total quiescent power.

THE SIMPLE METHOD

If PD_Q is one tenth of less PD, this simple method will work well. If the amplifier has a slew rate of several hundred volts/microsecond and the application is above 300V, use the more accurate method. The simple formula is:

$$R_{ØSA} = \frac{T_J - T_A}{PD + PD_Q} = R_{ØJC} - R_{ØCS}$$

Where:
T_J = maximum junction temperature allowed
$R_{ØJC}$ = AC or DC thermal rest from the specification table

THE MORE ACCURATE VERSION

With the unique combination of high voltage and speed such as the 900V and 500V/us of the PA94, traditional formulas for heatsink selection will falsely lower the apparent power handling capability of the amplifier. To more accurately predict operating temperatures use the following procedure.

Look for an output stage only quiescent current rating in the data sheet. If the data sheet does not list this specification, it can be estimated as 5% of the total quiescent current.

Find output stage quiescent power (PD_{QOUT}) by multiplying the output stage only quiescent current by the total supply (V_{ss}). Calculate a heatsink rating which will maintain output transistor junctions at 150°C or lower:

$$R_{\emptyset SA} = \frac{T_J - T_A - (PD + PD_{QOUT}) * R_{\emptyset JC}}{PD + PD_Q} - R_{\emptyset CS}$$

Where:
T_J = maximum junction temperature allowed.
$R_{\emptyset JC}$ =AC or DC thermal resistance from the specification table.

THE EASY AND ACCURATE METHOD

1) Set aside the slide ruler and calculator.
2) Start Power Design, an Excel spreadsheet available free from www.apexmicrotech.com
3) Enter amplifier, V_S, min/max frequency, output amplitude and load components.
4) Read load, supply and amplifier power levels, heatsink rating & maybe some warnings.
5) Tweak design as desired.
6) Enter design notes and press Print button for documentation.
7) Ask your boss for a raise.

8.0 AMPLIFIER MOUNTING AND MECHANICAL CONSIDERATIONS

For Power Op Amp designs, high reliability consists of mechanical considerations as well as electrical considerations. Proper mounting is very important for power amplifiers. Once the proper heatsink has been selected as described in Section 7, the following mounting techniques should be used.

All APEX metal can products have either an isolated case, ground connected case or a dedicated pin for the case. This means electrical insulating washers are generally not necessary and will likely increase operating temperatures if used.

In addition, APEX uses a thin beryllia substrate to get the lowest possible thermal resistance. While this leads to cool running, high reliability amplifiers, it is important not to run the risk of cracking this substrate. In order to prevent this, two major precautions must be observed:

1) *Do not use compressible thermal washers.* These are silicon rubber based pads such as Silpad. The amount of compressibility in a washer over 2 mil thick can lead to header flexing, which can crack the substrate. *The use of these washers voids the warranty.* Also, thermal grease has superior thermal properties.
2) *Do not over torque the case. Recommended mounting torque for the TO-3 and SIP packages is 4-7 in-lbs (.45-.79 N-m) and for the MO-127 Power Dip™ packages (PD10 AND PD12) is 8-10 in-lbs*

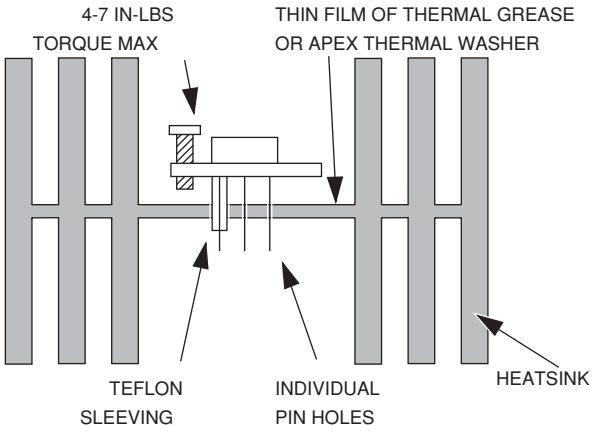


FIGURE 14. MOUNTING CONSIDERATIONS

(.90-1.13 N-m). Refer to Figure 14. Apply a thin, uniform film of thermal grease or an Apex thermal washer between the case and heatsink. Apply small increments of torque alternately between each screw when mounting the amplifier.

Due to dimensional tolerances between heatsink thru-holes and power op amp packages, extreme care must be taken not to let the pins touch the heatsink inside the thru-holes. *Do not count on the anodization for insulation* as it can nick easily, exposing bare aluminum, an excellent electrical conductor. *Use plastic tubing to sleeve at least two opposite pins* if you are using a mating socket or printed circuit board. If you are wiring directly to the pins, it is best to sleeve all pins. *Refer to the Package and Accessories Information section of the Hybrid & IC Handbook for further details on sleeving sizes, mating sockets and cage jacks for PC board mounting of power amplifiers. While teflon covers virtually all applications, the actual requirements are to withstand the maximum case temperatures and total supply voltage of the application.*

Never drill out the entire area inside the pin circle, drill individual holes for each pin. Often, heatsinking is accomplished with a custom heatsink or by directly mounting to a bulkhead. These approaches require the use of heatsink thru-holes for the amplifiers pins. For the 8-Pin TO-3 package, the main path for heat flow occurs inside the circumference of 8 pins. Refer to Figure 15. Therefore, a single, large hole, to allow the 8 pins to pass through, will remove the critical heatsinking from where it is most needed. Instead, 8 separate #46 drill size holes must be drilled.

9.0 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

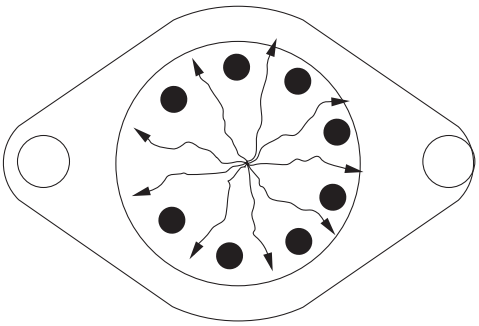


FIGURE 15. MAIN HEAT FLOW PATH: 8-PIN TO 3 PACKAGE

9.1 OUTPUT PROTECTION

Attempting to make sudden changes in current flow in an inductive load will cause large voltage flyback spikes. These flyback spikes appearing on the output of the op amp can destroy the output stage of the amplifier. Brush type DC motors can produce continuous trains of high voltage, high frequency kickback spikes. In addition, mechanical shocks to a piezo-electric transducer will cause it to generate a voltage. Again, this can destroy the output stage of an amplifier.

Although most power amplifiers have some kind of internal flyback protection diodes, these internal diodes should not be counted on to protect the amplifier against sustained high frequency, high energy kickback pulses. Many of these diodes are intrinsic "epi" diodes that occur as a result of the manufacture of the power darlington output transistor. Epi diodes generally have slow reverse recovery times and may have large forward voltage drops. *Under sustained high energy flyback conditions, high speed, fast reverse recovery diodes should be used from the output of the op amps to the supplies to augment the internal diodes.* See Figure 16. These fast recovery diodes should have reverse recovery times of less than 100 nanoseconds and for very high frequency energy should be under 20 nanoseconds.

One other point to note is that the power supply must look like a true low impedance source when current flows in the opposite direction from normal. Otherwise, the flyback energy, coupled back

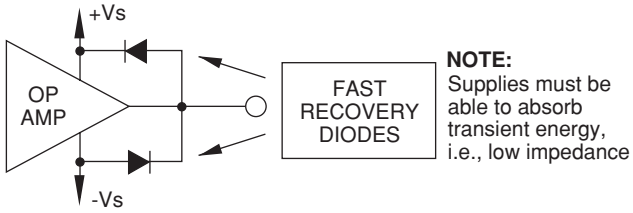


FIGURE 16. OUTPUT PROTECTION

into the supply pin, will merely result in a voltage spike at the supply pin of the op amp. This would lead to an overvoltage condition and possible destruction. Refer to Section 4.3 for information on overvoltage protection.

9.2 COMMON MODE VOLTAGE LIMITATIONS

One of the most widely misunderstood parameters on an op amp data sheet is the *Common Mode Voltage Range*, which specifies how close an input voltage *common to both inputs* may approach either supply rail. *When these limits are exceeded, the amplifier is not guaranteed to perform linearly. The Absolute Maximum Common Mode Voltage* specification on most data sheets refers to the voltage above which *the inputs may not exceed or damage will result to the amplifier*.

There are two cases which clearly illustrate the constraints of common mode voltage specifications: single supply operation and asymmetrical supply operation.

Example:

The APEX PA82J has a Common Mode Voltage Range of ±Vs – 10. This implies that if the PA82J is to be operated from a single supply, both inputs must be biased at least 10 volts above ground. Figure 17 illustrates an implementation of this which keeps both inputs above 10 volts for the given range of input voltages. Note that for single supply operation, the output of the amplifier is never capable of swinging all the way down to ground. This is due to the output saturation voltage of the amplifier.

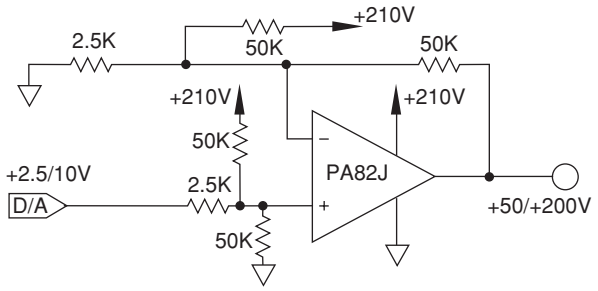


FIGURE 17. SINGLE SUPPLY OPERATION: V_{CM} CONSIDERATIONS

Figure 18 illustrates a very practical deviation from true single supply operation. The availability of the second low voltage source allows ground (common) referenced signals but also maximizes the high voltage capability of the unipolar supply. As long as the amplifier remains in the linear region of operation, the common mode voltage will be zero. With the 12V supply the allowed positive common mode voltage range is from 0 to 2V. Note the output of the PA81J can swing all the way to zero now also. The 12V supply in this case need only supply the quiescent current of the power op amp. If the load is reactive or EMF generating, the low voltage supply must also be able to absorb the reverse currents generated by the load.

9.3 DIFFERENTIAL INPUT VOLTAGE LIMITATIONS AND PROTECTION

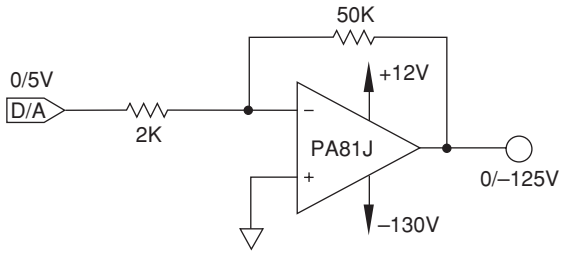


FIGURE 18. NON-SYMMETRICAL SUPPLY OPERATION

Exceeding the Absolute Maximum Differential Input Voltage specified on the data sheet can cause permanent damage to the differential input stage. Failure modes range from increased V_{OS} and V_{OS} drift, I_B and I_B drift, and input offset current, up to input stage destruction. Although the differential input voltage (V_{ID}) under normal closed loop conditions is microvolts, several conditions can cause it to be in the Volt range. Causes of V_{ID}:

1) Fast rise-time inputs.
2) Signal input while not under power.
3) High impedance output states (current limit, thermal shutdown, sleep mode).
4) Switching within the feedback loop.

An example of condition 4 is shown in Figure 19a.

This configuration is often used in ATE systems for changing the gain of an op amp. The amplifier's full scale transition time

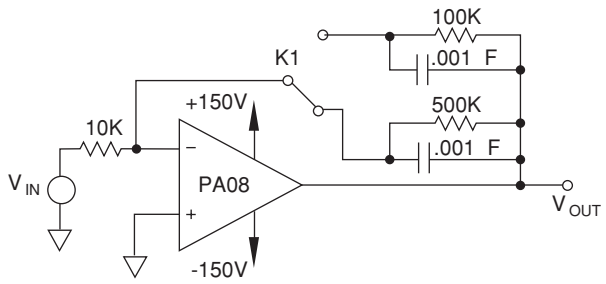


FIGURE 19a. GAIN SWITCHING AND V_{ID} *VIOLATION*

(microseconds) is faster than the typical relay switching time (milliseconds); therefore when the relay opens the feedback loop, the Aol of the amplifier will drive the output to one of the supply rails. In the example shown, the output will approach 150V while the relay is still switching. Because the 100K feedback resistor has completely discharged its associated rolloff capacitor, the relay will connect 150V directly to the input. Since the Absolute Maximum V_{ID} for the PA08 is ±50V, the input stage will be destroyed.

Effective input protection networks provide two functions:

1) Limit differential voltage to less than the reverse breakdown voltage of the input transistors base-emitter junction, typically ~6V.
2) Limit input transient current flow to less than 150mA.

Figure 19b shows an example of an input V_{ID} protection network. The diodes should be high speed devices such as 1N4148 and the series impedance should limit instantaneous current to a maximum of 150mA.

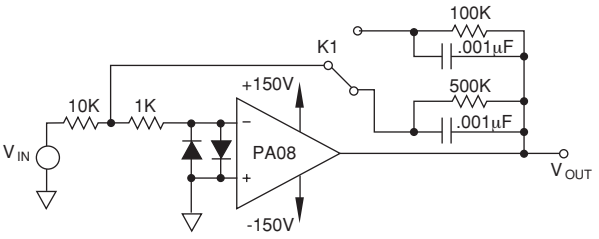


FIGURE 19b. GAIN SWITCHING AND V_{ID} PROTECTION

10.0 STABILITY

The most common application problem when working with power op amps is stability. Although most power op amps are compensated for unity gain stability, they are frequently required to drive reactive loads, deliver high currents, or use high impedances due to high voltage. These conditions make stability more difficult to achieve. However, EVERY circuit can be stabilized if the guidelines given here are followed. Table 1 provides a troubleshooting guide for stability problems. The **"Probable Cause / Possible Solution Key"** gives insight into the origin of the problem and provides guidance as to the appropriate fix.

An amplifier becomes an oscillator when two conditions are met: total phase shift reaches 360° and the amplifier has gain at this frequency. With operational amplifiers using negative feedback, half the required phase shift is provided by the inverting nature of the circuit. This means phase shift from all other sources totals a second 180° when oscillating. The crucial element here is to examine phase shift at frequencies all the way out to the intersection of open and closed loop gains. Putting it another way, just because the circuit is designed for DC only, does not preclude it from oscillating at 1MHz. Most Apex amplifiers have gain well into the MHz region and phase shifts of both amplifiers and parasitic elements grow rapidly in this area.

G

CONDITION AND PROBABLE CAUSE TABLE

fosc Oscillation Frequency	Oscillates unloaded?	Oscillates with V_{IN} = 0?	Loop Check† fixes oscillation?	Probable Cause(s) (in order of probability)
CLBW f_{osc} UGBW	N	Y	N	A, C, D, B
CLBW f_{osc} UGBW	Y	Y	Y	K, E, F, J
CLBW f_{osc} UGBW	–	N	Y	G
f_{osc} CLBW	N	Y	Y	D
f_{osc} = UGBW	Y	Y	N*	J, C
f_{osc} ≪ UGBW	Y	Y	N	L, C
f_{osc} > UGBW	N	Y	N	B, A
f_{osc} > UGBW	N	N**	N	A, B, I, H

TABLE 1.

CLBW = Closed Loop Bandwidth
UGBW = Unity Gain Bandwidth
† See Figure 20 for loop check circuit.
— Indeterminate; may or may not make a difference.
*Loop check (Figure 20) will stop oscillation if Rn << |Zcf| at UGBW
**Only oscillates over a portion of the output cycle.

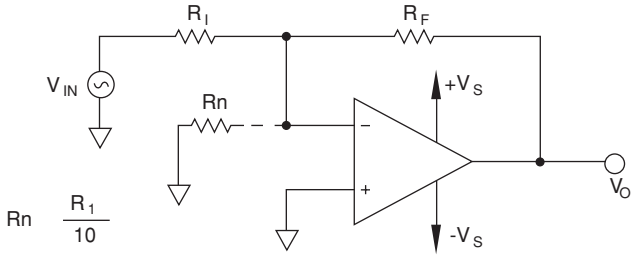


FIGURE 20. LOOP CHECK CIRCUIT

KEY TO PROBABLE CAUSE / POSSIBLE SOLUTION

A. Cause: Supply feedback loop (insufficient supply bypassing).
Solution: Bypass power supplies. See Section 4.2.
B. Cause: Supply lead inductance.
Solution: Bypass power supplies. See Section 4.2.
C. Cause: Ground loops.
Solution: Use **"Star"** grounding. See Figure 21.
D. Cause: Capacitive load reacting with output impedance (Aol pole).
Solution: Raise gain or use input R–C compensation network. See Figure 24.
E. Cause: Inductor within the feedback loop (noise gain zero).
Solution: Use alternate feedback path. See AN#5, **"Precision Magnetic Deflection,"** or AN#13, **"V–I Conversion."**
F. Cause: Input capacitance reacting with high R_F (noise gain zero).
Solution: Use Cf in parallel with Rf. (Cf =~Cin). Do not use too much Cf, or you may get problem J.
G. Cause: Output to input coupling.
Solution: Run output traces away from input traces, ground the case, bypass or eliminate R_B (the bias current compen- sation resistor from –IN to ground)
H. Cause: Emitter follower output reacting with capacitive load.
Solution: Use output **"snubber"** network. See Section 10.1.
I. Cause: **"Composite PNP"** output stage with reactive load.
Solution: Use output **"snubber network."** See Section 10.1.
J. Cause: Feedback capacitance around amplifier that is not unity gain stable (integrator instability).
Solution: Reduce Cf and/or increase Cc for unity gain stability.
K. Cause: Insufficient compensation capacitance for closed loop gain used.
Solution: Increase Cc or increase gain and/or use input R–C compensation network. See Figure 24.
L. Cause: Servo loop stability problem.
Solution: Compensate the **"front end"** or **"servo amplifier."**

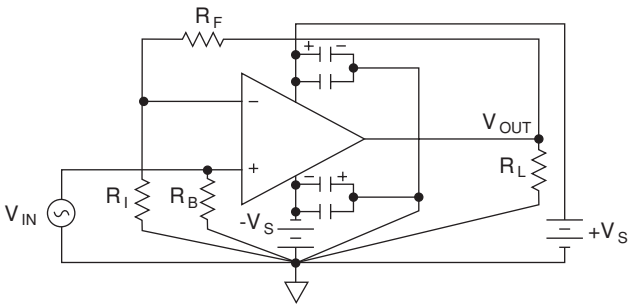


FIGURE 21. BASIC REQUIREMENTS FOR STABILITY

10.1 BASICS OF STABILITY

Some basic practices must be followed to ensure stability. Proper ground practices are mandatory and are illustrated in Figure 21. Improper grounding can lead to oscillations near the unity gain bandwidth frequency of the amplifier. Proper bypassing of power supplies is also illustrated in Figure 21. The local bypassing close to the amplifier with a small electrolytic and ceramic capacitor insure good high frequency grounding of the supply lines. The internal phase compensation on op amps will be referred to one of the supply lines and this is the reason for the importance of good local bypassing.

Table 1 shows the frequency of an oscillation is the most important clue about its source. For frequencies above unity gain the amplifier, try a snubber network as shown in Figure 22. For frequencies near the intersection of open and closed loop gains, check for weak high frequency supply bypass or for ground loops. For lower frequencies, perform a loop analysis using Application Notes 19 and 25

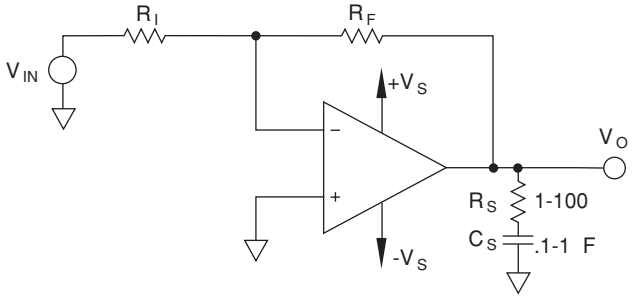


FIGURE 22. OUTPUT R-C-NETWORK ("SNUBBER")

10.2 COMMON SOURCES OF NON-LOOP INSTABILITY

The following is a list of the most common instability situations reported:

1) Large electrolytic or tantalum capacitors are installed close to the amplifier pins as recommended, but small ceramic bypass capacitors are omitted. The circuit may oscillate because the high frequency impedance of the large capacitors is not low enough to decouple the power supplies.
2) A prototype circuit is checked out and approved. A printed circuit board is built and all modes of operation test okay. A step and repeat technique then uses this same artwork to generate a multiple amplifier board. When tested, every amplifier on the board oscillates. Cross coupling through the supplies is a major problem in multiple amplifier circuits. Use lots of bypass capacitors, ground the case, and consider all items in the following section.
3) Ungrounded cases can cause oscillations, especially with faster amplifiers. The cases of most APEX metal can amplifiers are electrically isolated to provide mounting flexibility. The case is in close proximity to all the internal nodes of the amplifier and can act as an antenna. Providing a connection to ground prevents noise pickup, cross-coupling or positive feedback leading to oscillations. Some models have heatsink tabs connected to $–V_S$, serving the same purpose as long as $–V_S$ is clean.
4) A standard inverting circuit includes an impedance matching resistor in series with the non-inverting input to take advantage of the improved input offset current specification. The high impedance input becomes an antenna, receiving positive feedback, causing

oscillation. Calculate the errors without using the resistor (some amplifiers have equal bias and offset currents negating the effect of the resistor). If the resistor is required, bypass it with a ceramic capacitor of at least .01uF.

10.3 LOOP STABILITY ISSUES

A majority of loop instability problems are due to one or more of the following:

1) Amplifier compensation not matched to the circuit closed loop gain. This includes using amplifiers below their recommended gain, choosing the wrong external compensation or failure to realize high frequency (not DC) gain is what counts. (A feedback of integrating capacitor lowers gain at high frequency).
2) The use of large impedance values for input or feedback networks allows parasitic elements too much control. Consider a 100KΩ feedback resister with a parasitic of 3pF. This places a pole (with an additional 45° phase shift) at about 53KHz!
3) Capacitive loads reacting with amplifier output impedance, effectively adding a pole and corresponding phase shift to the amplifier.
4) Voltage-to-current phase shift of an inductor is inside the feedback loop of current output circuits.
5) Too many amplifiers inside a single loop. Each amplifier contributes to the total as you go around the loop.

Solutions for these include one or more of the following:

1) Change to an amplifier suitable for lower gain, increase external phase compensation, or modify the circuit.
2) Lower impedance values.
3) Add an isolation resistor outside the feedback loop to defeat the effect of the capacitive load as shown in Figure 23. This is the simplest external component soulution and has surprisingly little effect on circuit performance.

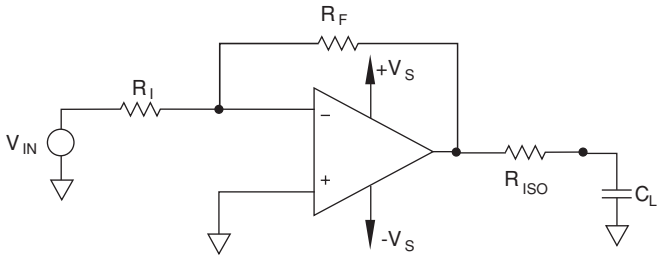


FIGURE 23. CAPACITIVE LOAD ISOLATION

4) Increase DC closed loop gain.
5) Increase AC gain only with noise gain compensation as shown in Figure 24. This technique works well with inverting circuits but is not recommendd for non-inverting circuits.
6) Lower the intersection rate of open and closed loop gains with a properly sized roll off capacitor. Usually, bigger is not better.

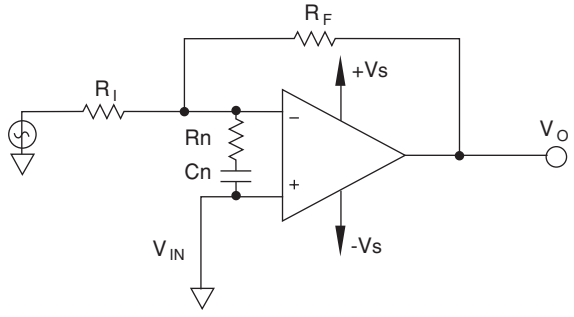


FIGURE 24. INPUT R-C NETWORK COMPENSATION

7) Add an AC voltage gain limiter to the current output circuit. At the higher frequencies where the inductor demnds very high voltages, this R-C network puts the amplifier into a voltage feedback mode.
8) Lower amplifier count.

Most of these solutions tend to negatively impact bandwidth, especially in the current output circuits. Apex has been known to boast, "Any circuit can be made stable". Notice that bandwidth trade offs were not part of the quotation; this is where the engineering work lies. Upon looking at the Application Notes mentioned above, some of you may be thinking about the amount of this work, with phrases we can't print here. Have no fear, Power Design takes care of all the tedious math and graphing for you making design interations a snap.

10.4 A FINAL STABILITY NOTE

When you're at your wits end trying to solve an oscillation problem, don't give up because you have it down to an "acceptably low" level. A circuit either oscillates or it doesn't, and no amount of oscillation is acceptable. Apply these techniques and ideas under your worst case load conditions and you can conquer your oscillation problems.

The APEX Applications Hotline

The APEX Applications Hotline provides technical support all the way through your project. In many cases, specific failure prevention can be suggested immediately. In some instances we will need the amplifier to be sent to APEX for a failure analysis. The results of the analysis can pinpoint the area of damage which then narrows down the circuit problem.

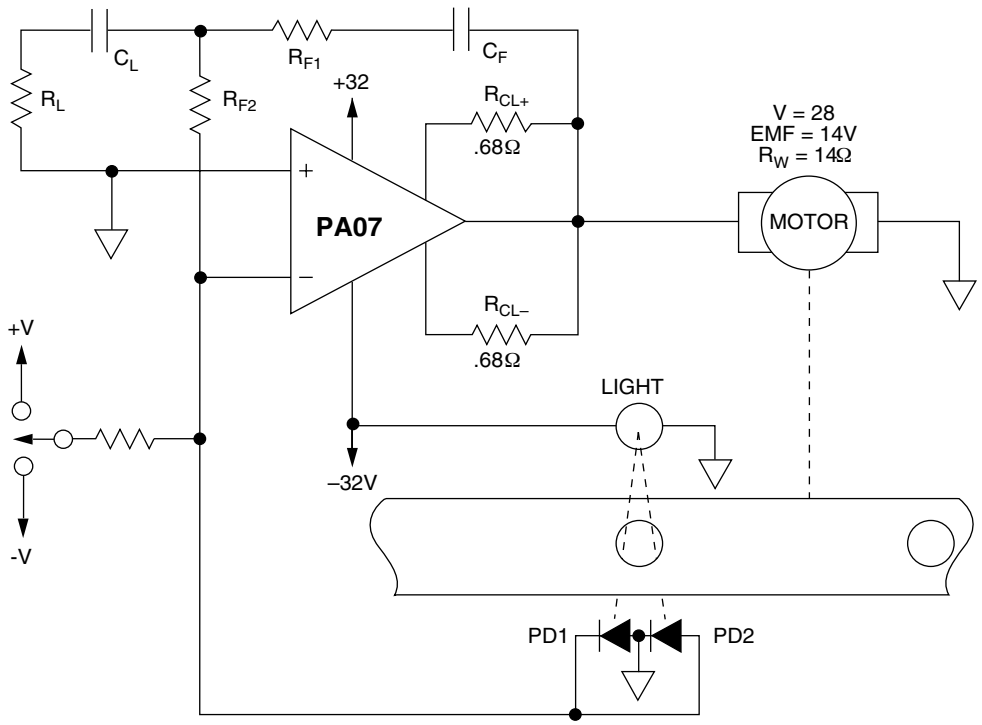


FIGURE 1. SEQUENTIAL POSITION CONTROL

INTRODUCTION

Power Op Amps are ideally suited for position control because their response time is fast compared to any mechanical drive train. The optoelectronic technique of position control can move to and maintain fixed index points on linear or rotary motion components while adding no linkages or independently moving parts. The resulting system features high reliability, accuracy and repeatability. If the integration of photodiode currents is required, select a power amplifier with an FET input to maintain very low bias current levels such that the integrating capacitor voltage will remain constant during periods when both photodiodes are not illuminated. Further selection criteria should be based on motor ratings and/or available power.

SEQUENTIAL POSITION CONTROL

In the circuit shown in Figure 1, the PA07 integrates the differential output of the pair of photodiodes and drives the motor in the proper direction until the photodiode currents are equal. This differential configuration negates the well known temperature and time instabilities of optoelectronic devices. To move between index points, a fixed input current is momentarily switched to the amplifier input causing the amplifier to drive the motor in the desired direction. The charge on C_F will maintain motor drive as the input current is switched off prior to reaching the index point. As the first photodiode is illuminated, its output reinforces the current direction of motion. As the second photodiode is illuminated, its current will reverse the motor drive, causing the system to lock to the index point.

As motor response and system inertia vary widely, C_F and R_F must be selected for the individual application to provide proper damping. C_F must be small enough to allow drive reversal before the index point passes the second photodiode or the system will continue on to the next index. Very small values of C_F can cause severe overshoot or oscillation leading to motor burnout and/or drive train failure. R_{F1} and R_{F2} are required to stabilize the control loop at the unity gain point and to minimize overshoot. R_L and C_L form a lead network which may be included to improve response time by enabling the amplifier to modify the motor drive based on a change of the sensor output. In this manner, a braking force can be applied to the motor prior to reaching the index point. The motor shown in Figure 1, having EMF of 14V, will apply a 46V stress across the conducting output transistor when reversed. With a duration longer than 5ms, the steady state secondary breakdown line of the SOA for the PA07 curves requires the current limits to be set to 1A. See PA07 data sheet.

SINGLE POINT POSITION CONTROL

A variation of the above technique shown in Figure 2 can be used to return a wheel to a single index point after rotating in either direction. The low inertia, fast response system will take the shorter route to the index point when switched from run to stop. The PA12A was selected for this application because it provides high power while keeping bias current levels low with respect to the photodiode currents. To improve response time, the lead network compensates for motor response lagging behind any change in drive voltage. A run control current of sufficient amplitude to override the photodiode currents is fed to the amplifier inverting input. Removal of this current restores control to the photosensors.

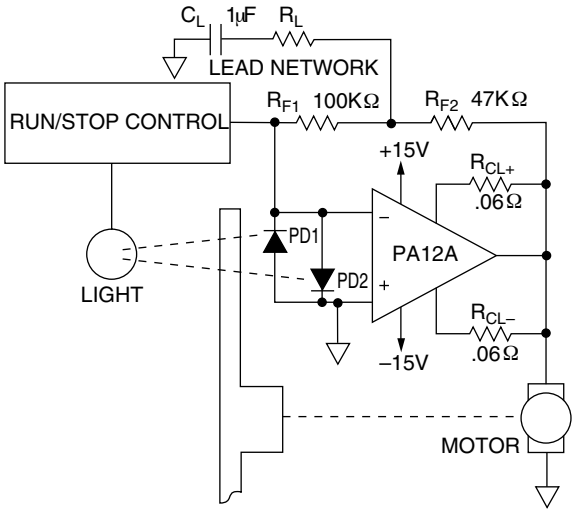


FIGURE 2. SINGLE POINT POSITION CONTROL

POSITION CONTROL MASK

Figure 3 shows details of the wheel preparation and sensor placements at the stop index. Arrows indicate direction of rotation when the corresponding photodiode has the higher output. While it is theoretically possible to achieve a stable position on the opposite side of the wheel, system noise or a slight movement will imbalance the equal photodiode currents and the higher current sensor will receive even more light. This causes the wheel to seek the desired index point. Masking of the wheel at an angle to the radial softens the control function and prevents overshoot.

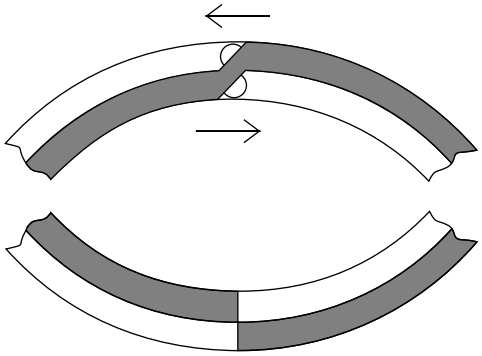


FIGURE 3. SINGLE INDEX POINT DISK

SPOT SIZE

Optimum relationship of beam size to active areas of the photodetectors is shown in Figure 4. A centered beam should illuminate half the photosensitive area of each diode. Too large a beam will produce no change of sensor output for a range of positions, while a smaller beam will produce a nonlinear transfer function near the center line between the photosensitive areas. This makes selection of C_F to dampen the circuit difficult and requires a higher intensity light source.

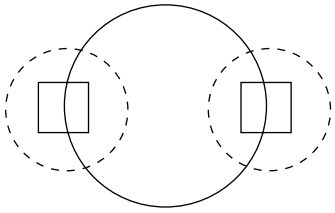


FIGURE 4. BEAM-SENSOR ALIGNMENT

DIGITAL INTERFACING

For systems with digital control, Figure 5 illustrates a method not requiring generation of bipolar control signals thus saving the cost of digital to analog conversion. When logic lines are low, the signal diodes will not conduct. This condition leaves control to the photodiodes. A high level on line 2 will cause current to flow to the summing junction and the amplifier will swing negative. A high level on line 1 will raise the summing junction voltage above ground, and the amplifier will swing positive. Select a resistance value such that a high logic level will provide at least twice the maximum current from each photodiode to insure control override regardless of photodiode signals.

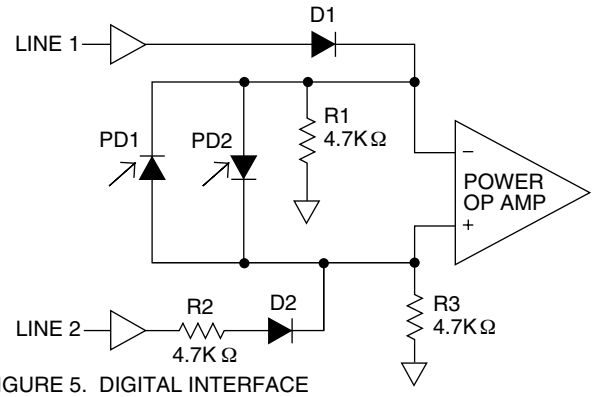


FIGURE 5. DIGITAL INTERFACE

DUAL SENSORS

For applications requiring high precision, the use of a dual element position sensing PD1(Figure 5) will allow smaller beam size, tighter beam control and provide better thermal equilibrium. The specified resolution of the detector recommended for this application is better than .0127mm (.0005 inch). The detector is a three terminal device requiring a current inverter as shown in Figure 6 to achieve the differential configuration. Two equal resistors, R1 and R2, should be scaled to the maximum photodiode current and swing capability of the signal amplifier.

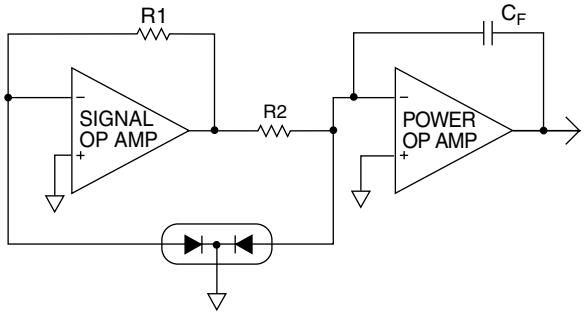


FIGURE 6. CURRENT INVERSION

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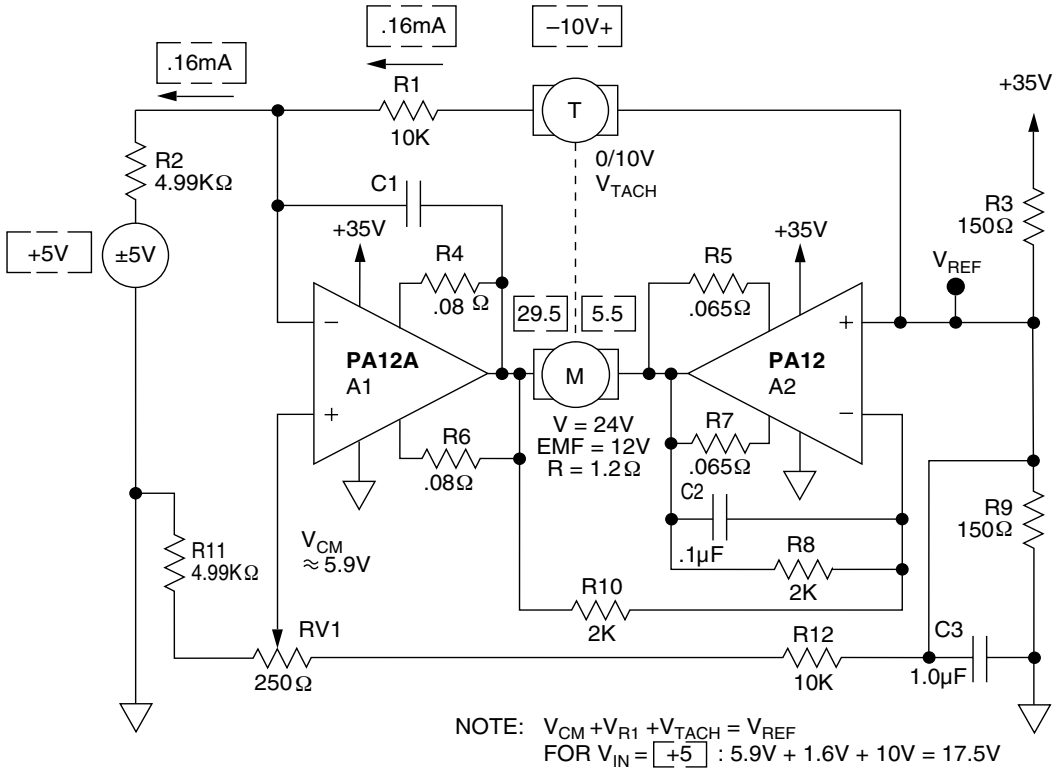

FIGURE 1. BI-DIRECTIONAL BRIDGE FOR A SINGLE SUPPLY

INTRODUCTION

Two power op amps configured in a bridge circuit can provide substantial performance advantages:

1. Bi-directional output with a single supply
2. Twice the output voltage
3. Twice the slew rate
4. Twice the output power
5. Half the power supply requirement

Low current outputs can reach the kilovolt range or mulitple ampere outputs of hundreds of volts can be obtained. To achieve these levels of performance, both terminals of the load must be driven and extra components are required.

BI-DIRECTIONAL DRIVE ON A SINGLE SUPPLY

Figure 1 depicts a bi-directional motor speed control using a single supply which features ground referenced bipolar input signals. A mid-supply reference created by R3 and R9 establishes the DC operating levels for A1 and A2. Inverter A2 drives the load equally in the opposite direction with respect to the output of input amplifier A1. This configuration places both load terminals at the reference voltage with a zero input condition and prevents premature saturation of either amplifier.

To understand the operation of the circuit, consider A1 as having two sets of inputs:

1. Voltage dividers from the supply voltage to establish common mode bias.
2. Actual input signal and tachometer feedback.

One sixth of any supply voltage variation will appear equally at both inputs of the amplifier. However, the common mode rejection (CMR) of the op amp will reduce its response by four orders of magnitude at low frequencies. The low pass function of C3 insures optimum rejection by keeping the common mode inputs in the low frequency spectrum. The common mode voltage (CMV) range of the amplifier sets the minimum common mode bias at the inputs of A1. The circuit shown provides a nominal 5.9V from the supply rail (ground) which allows power supply variations to 10% below nominal.

For the actual input signal, C1, R1, R2, and A1 form an integrator (non-inverting input is constant). With the control voltage applied across R2 and the tachometer voltage applied across R1, integration forces the motor speed to be proportional to the input voltage. The value of C1 must be selected for proper damping of the total system which includes the mechanical characteristics of the drive train.

Resistors R4 and R6 set current limits of A1 to 7.5A. When A1 current limits, A2 will reduce its output voltage equal to the voltage change of A1. By insuring A1 will limit prior to A2, power stress levels of the two amplifiers are equalized. In addition to amplifier protection, this programmability is being utilized to limit the temperature rise in the motor, thereby increasing expected life of the system. Maximum continuous load rating of the motor shown is 10A and locked rotor (stall) current is 20A. Since locked rotor ratings generally refer to abnormal conditions, the motor is being used near capacity while maintaining a comfortable safety margin for motor and drive circuit.

The key to accuracy of this circuit lies in matching the division ratios from the reference voltage to ground for both the inverting and non-inverting inputs of A1. The inverting side division ratio is affected by the impedances of the control signal and tachometer. Normally, the

impedance of a voltage output DAC and the winding impedance of the tachometer are negligible. This allows use of cost effective 1% resistors and requires only trimpot RV1 to provide precision adjustment. Ratio match errors will appear as tachometer output errors. These errors will be of a size equal to the ratio of mismatch times the reference voltage.

The second major accuracy consideration of this circuit is the voltage offset of A1. As this error will appear at the tachometer at a gain of three, the PA12A was selected for its improved specification of 3mV compared to 6mV for the regular PA12.

Changes of input voltage range, RPM range or tachometer output ratings are easily accommodated. Lowering the values of R1 and R12 (ratio match still required) will re-scale smaller tachometer voltage

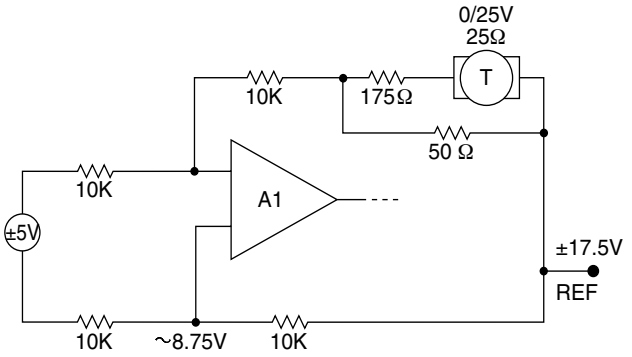

FIGURE 2. HIGH OUTPUT TACHOMETER

spans or lower RPM ranges to the ±5V input level. While increased input signal levels could be re-scaled in the same manner, increasing R2 and R11 provides the required re-scaling with the added benefit of lowering control signal drive requirements.

Higher voltage tachometer voltage spans require a different approach to re-scaling due to the CMV limitations at the inputs of A1. Figure 2 illustrates a technique using a 25V tachometer which will maintain adequate CMV for A1 with supply voltages down to 20V. Calculations for the divide by five network at the tachometer includes winding impedance to achieve accurate scaling to the ±5 input signal. For error budgets, this factor of five must be applied to both the ratio mismatch errors and voltage offset errors as above. Total gain for calculating offset errors will be 10.

ELECTROSTATIC DEFLECTION

The cathode ray tube (CRT) shown in Figure 3 requires 500Vpp nominal drive. Allowing for a ±5% gain error plus a 10% (of full scale) centering voltage tolerance, brings the desired deflection voltage swing to 575Vpp. Two PA84 high voltage power op amps provide this differential voltage swing. Slew rates of 400 volts per microsecond at the CRT enable the beam to traverse the face plate in less than 1.5 microseconds.

The gain of A1 is set by (R3+RV1)/R1 at 100. The circuit provides for both gain adjustment (RV1) and beam centering (RV2). For proper scaling, R4 and R6 reduce the centering control voltage of trimpot RV2 to ±250mV. C2 provides the desired low AC impedance to ground to enhance stability and eliminate noise pickup. A2 inverts the output of A1 at unity gain (set by R8/R5), to yield an overall gain of 200 for single ended input signals measured at the differential output. R9 and C4 constitute a second input to A2 with an AC gain of 100 (R9/R8). Using ground as an input has no direct signal contribution, but it does allow both amplifiers to use the phase compensation recommended at a gain of 100 (20K, 50pF), thereby achieving a large power bandwidth of 250kHz.

TRANSIMPEDANCE BRIDGE FOR MAGNETIC DEFLECTION

The circuit shown in Figure 4 drives the electro-magnetic deflection yoke of a precision x-y display. Two factors constitute the design challenge of this circuit:

1. Greater than 15V drive levels are required to change current magnitude and polarity to achieve fast endpoint-to-endpoint display transition times.

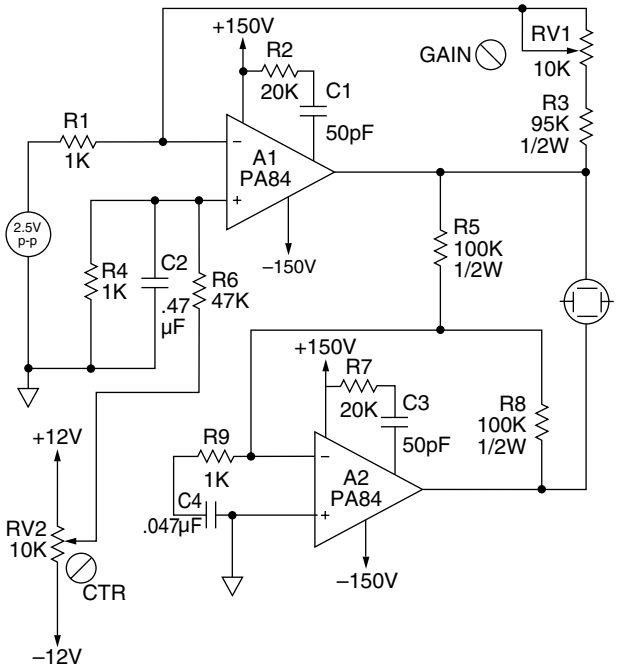

FIGURE 3. ELECTROSTATIC DEFLECTION AMPLIFIER

2. Only ±15V power supplies are available in the system.

The bridge circuit can drive almost double the single power supply voltage, thereby eliminating the need of separate supplies solely for CRT deflection. The maximum transition time between any two points is 100µs for display ratings of:

Yoke inductance = 0.3mH
Full scale current = ±3.75A
DC coil resistance = 0.4 ohms

The voltage required to change the current in an inductor is proportional to current change and inductance, but inversely proportional to transition time.

V = di*L/dt
V = 7.5A*0.3mH/100µs = 22.5V

The Apex low voltage power op amp PA02 is an ideal choice for this circuit due to its high slew rate and ability to drive the load close to the supply rail. A1 in Figure 4 is configured as a Howland Current Pump.

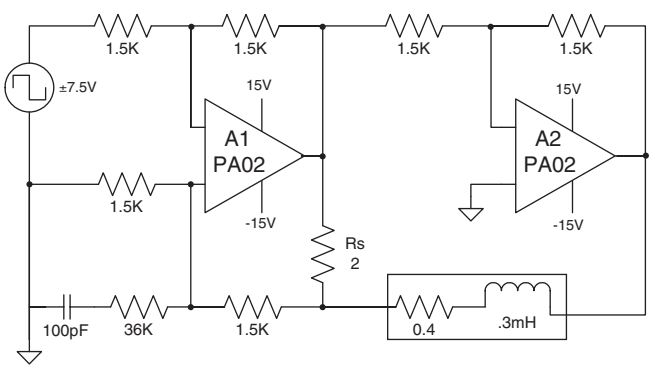

FIGURE 4. ELECTROMAGNETIC DEFLECTION AMPLIFIER

Voltage on the bottom of the sense resistor is applied directly to the load; voltage at the top is the applied voltage plus a voltage proportional to load current. With both these points for feedback, the amplifier sees a common function of load voltage on both inputs which it can reject (CMR), but sees a function of load current differentially. In this arrangement, A1 drives the load anywhere required (with in saturation limits) to achieve load current commanded by the input signal. As ratio match between the two feedback paths around A1 is critical, these four resistors are often implemented with a resistor network to achieve both precision match and tracking over temperature. A2 provides a gain of -1 to drive the opposite terminal of the coil. Gain setting resistors for A2 are not nearly as critical, a mismatch here simply means one amplifier works a little harder than the other. Starting values for the R-C compensation network come from the Apex Power Design tool and are fine tuned with bench measurements.

A first glance, it might appear the choice of 2Ω for the sense resistor is quite large because the peak voltage drop across it is 7.5V, or half the supply voltage.

If one were to add to this the peak voltage drop across the coil resistance (1.5V) and the sense resistor (7.5V), it would be easy to assume a total swing of 31.5V or greater than 15V at 3.75A would be required of each amplifier.

Salvation for this problem lies in analyzing current flow direction.

In the middle graph of Figure 5, we find the large sense resistor does not destroy the circuit drive capability. The main portion of the transition is complete in about 80μs and settles nicely.

In the top graph, we find a surprise; both amplifiers are actually swinging OUTSIDE their supply rails. The "upside down" topology of the output transistors in the PA02 allows energy stored in the inductor to fly back, turning on the internal protection diodes. The result is peak voltages in the first portion of the transition greater than total supply.

In the bottom graph, we find stored energy in the inductor develops voltage across the sense resistor, which ADDS to the op amp voltage until current crosses zero. In this manner, peak voltage across the coil is nearly 40V!

The seemingly large value of sense resistor did not kill us on voltage drive requirements and gives two benefits: First, internal power dissipation is lower than with a smaller resistor. Secondly, with larger feedback signal levels, the amplifier closed loop gain is lower; loop gain is larger; fidelity of the current output is better; and voltage offset contributes a lower current offset error.

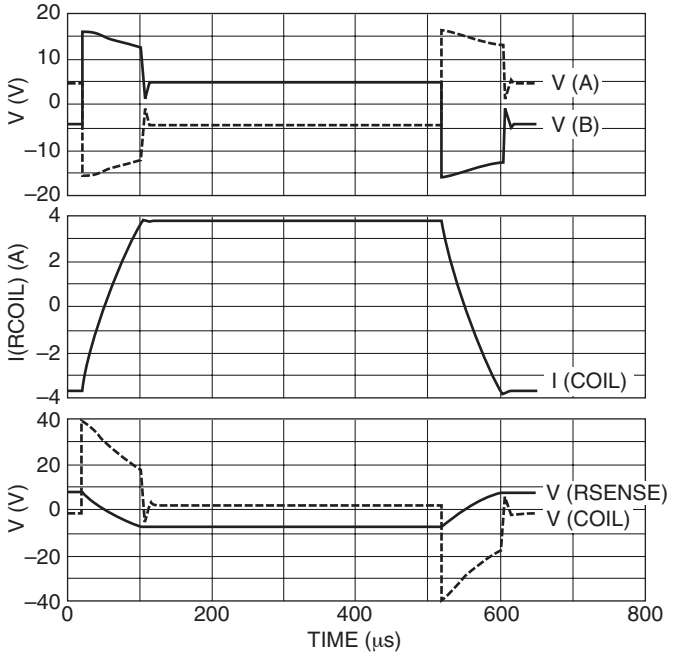

FIGURE 5. MAGNETIC DEFLECTION VOLTAGE AND CURRENT WAVEFORMS

EFFICIENT USE OF POWER SUPPLIES

To illustrate the advantages of the bridge circuit, Figures 6 and 7 show two high performance audio amplifier designs with equal output power, but substantially different supply requirements. In the circuit of Figure 6, the instantaneous load current will appear on only one supply rail. This means each supply rail must support the total wattage requirement and utilization is only 50% at peak outputs. In contrast, the equal and opposite drive characteristic of the bridge circuit shown in Figure 7 loads both positive and negative supply rails equally during each half cycle of the signal. This improved utilization reduces size, weight and cost of the power supply for the circuit in Figure 7 even though input and output power ratings are essentially equal.

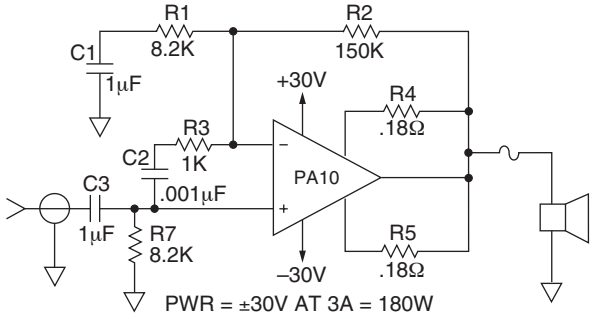

FIGURE 6. STANDARD AUDIO AMPLIFIER

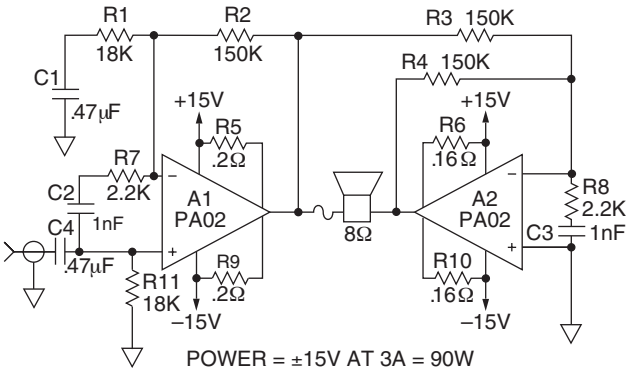

FIGURE 7. BRIDGE AUDIO AMPLIFIER

CONCLUSION

Bridge circuits can make the difference when performance requirements exceed voltage limitations of either the available power supplies or the power op amps. The input section of these circuits consists of a standard amplifier circuit for driving a single ended load. The added amplifier serves merely as an inverter. It doubles drive voltage by providing an equal and opposite output, thereby making the output fully differential. The performance increases usually outweigh the increased cost and complexity.

APPLICATION NOTE 5

POWER OPERATIONAL AMPLIFIER

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INTRODUCTION

Closed loop power op amp circuits offer distinct advantages in current control over open loop systems. Using a power op amp in the conventional voltage to current conversion circuit, the negative feedback forces the coil current to stay exactly proportional to the control voltage. The resulting accuracy makes many new applications feasible. For example, by placing the non-linear impedance of the deflection yoke inside the feedback loop, steady state positioning, which is difficult, if not impossible, to achieve with open loop circuits, can easily be implemented with a power op amp. In addition, sweep systems with substantially improved linearity can be designed using power op amps.

Typical applications include: heads-up displays, which require random beam positioning or E-beam lithography; and other complex data displays which can achieve the needed accuracy with a power op amp. Moreover, the versatility and ease of use of power op amps will help speed up the design process while at the same time reducing development cost. The final result will be a more accurate and reliable display using fewer parts.

HIGH RESOLUTION AND HIGH EFFICIENCY

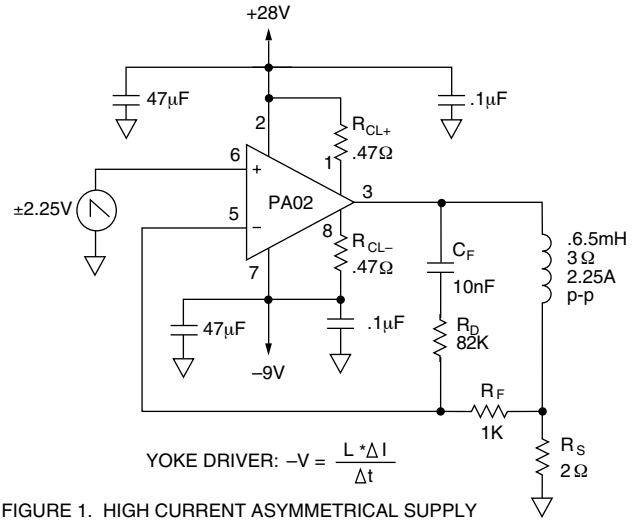

FIGURE 1. HIGH CURRENT ASYMMETRICAL SUPPLY

The vertical deflection circuit of Figure 1 was designed to drive a high efficiency RCA CODY II tube. The PA02 was selected for this configuration because of its exceptional linearity and other advantages such as high slew rate, fast settling time, low crossover distortion, and low internal losses. All of these advantages contribute to a superior resolution display.

The key to this circuit is the sense resistor (R_S) which converts the yoke current to a voltage for op amp feedback. With the feedback applied to the inverting input and the position control voltage applied to the non-inverting input, the summing junction's virtual ground characteristic assures the voltage across R_S is equal to the input voltage. Thus, the highly linear control of the voltage across R_S insures accurate beam positioning.

The value assigned to R_S has significant impact on the circuit performance. All op amp input errors such as voltage offset, imperfect common mode rejection, offset drift, etc., will appear across the sense resistor, producing current errors. While it is easy to see large sense resistors minimize DC errors, it takes a little more study to realize they help dynamic response also. The R_S value is a major player in setting the loop gain of the circuit. Larger feedback voltages will result in noticeable improvements in power bandwidth and settling time. The limiting factors on raising R_S values are brought on by the fact that load current flows through them; voltage drive capability decreases; and power dissipation in this resistor increases.

Weighing these trade-offs between errors, bandwidth, and efficiency in the selection of R_S value will produce the optimum choice for each application. The voltage drive requirements will then be defined by inductance, transition times and current. This display must operate at 50Hz or 60Hz with retrace times of 730µs and coil currents of $2.25A_{P-P}$.

The drive voltage required to change the current in an inductor is proportional to both current change and inductance, but inversely proportional to transition time.

$$V_{DRIVE} = \Delta I * L/\Delta t \quad (1)$$
$$V_{DRIVE} = 2.25A_{P-P} * 6.5mH/15.93ms = .918V \quad (2)$$
$$V_{DRIVE} = 2.25A_{P-P} * 6.5mH/730\mu s = 20.03V \quad (3)$$

To determine the power supply levels, add the supply-to-output differential rating of the power op amp (from the Amplifier Data Sheet) and the voltage dropped across the combined values of the sense resistor plus the coil resistance, to these drive requirements to arrive at +28V and -9V as follows:

$$V_{DROP} = I_{PK} * (R_S + R_L) \quad (4)$$
$$V_{DROP} = 1.125A_{PK} * (2\Omega + 3\Omega) = 5.625V \quad (5)$$
$$V_S = V_{DRIVE} + (V_S - V_O) + V_{DROP} \quad (6)$$
$$V_S = .918V + 2V + 5.625V \cong 8.6V \text{ (sweep)} \quad (7)$$
$$V_S = 20.03V + 2V + 5.625V \cong 27.7V \text{ (retrace)} \quad (8)$$

Caution should be exercised when using asymmetric power supplies, because the inductive load has the potential to store energy from the higher supply. This could be initiated by an abnormal condition causing the high output voltage to remain on the yoke longer than the normal retrace time. After such an occurrence, the collapsing magnetic field would discharge the stored energy into the lower voltage supply via the inductive kickback protection diodes in the power op amp. This will produce a voltage transient on the supply rail with its amplitude a function of stored energy and the transient impedance of the power supply. If this transient added to the supply voltage exceeds the rail-to-rail voltage rating of the amplifier, the result will be destructive. In such cases, a zener clamp on the amplifier output should be used.

A note of caution when using modular construction. Instruction manuals always specify, **"power down first, then remove the module."** However, because this doesn't always happen, protective action should be taken. The mechanical break of the connection to any inductance, coil or wire, causes high voltage flyback pulses. The stored energy must be absorbed somewhere. It's much better to use the zener clamp than to risk the op amp.

STABILITY CONCERNS

Since the current control capabilities of this circuit rely on feedback from the current-to -voltage conversion sense resistor, phase shift due to the inductance of the yoke will be evident in the feedback signal. Because the phase shift approaches 90° on a perfect inductor and the phase margin of an op amp is always less than 90°, design adaptations are required to prevent oscillation.

The network consisting of R_D, R_F and C_F, serves to shift from a current feedback via R_S to a direct voltage feedback at the upper frequencies. This bypasses the extra phase shift caused by the inductor. In selecting component values for this network, R_F should be much larger than R_S, but should not exceed 1KΩ for the PA02, because the input capacitance of the op amp would otherwise add phase shift. In selecting values of R_D and C_F, start with values prescribed by the Apex Power Design tool which will yield a stable circuit. Spice analysis and bench measurements will usually allow impedance of both these components to increase and speed up the circuit.

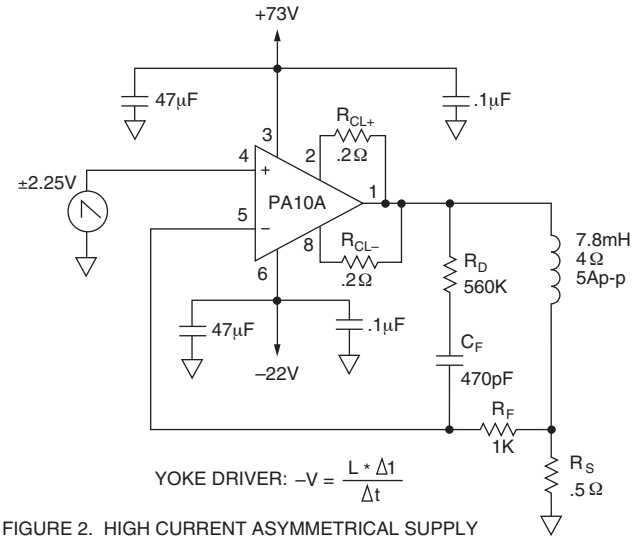

FIGURE 2. HIGH CURRENT ASYMMETRICAL SUPPLY

For an even more powerful version of this circuit, the PA10 power op amp can be used, as shown in Figure 2. With this device, a 7.8mH 4Ω coil can be driven at $5A_{P-P}$ with the same timing requirements. Calculations for this design are:

$$V_{DRIVE} = 5A_{P-P} * 7.8mH/15.93ms = 2.45V \quad (9)$$
$$V_{DRIVE} = 5A_{P-P} * 7.8mH/730\mu s = 53.43V \quad (10)$$
$$V_{DROP} = 2.5APK * (1\Omega + 4\Omega) = 12.5V \quad (11)$$
$$V_S = 2.45V + 6.5V + 12.5V \cong 21.5V \quad \text{(sweep)} \quad (12)$$
$$V_S = 53.43V + 6.5V + 12.5V \cong 72.5V \quad \text{(retrace)} \quad (13)$$

Both of the circuits illustrated have a 730µs retrace time requirement, met easily by the op amp's slew rate and settling time which is substantially faster.

To better understand this and other applications, Figure 3 illustrates input and output waveforms. Traces prior to time A, are the end of the sweep portion where current is changing at a relatively slow rate. The peak output voltage at time A is roughly the sum of equations 9 and 11.

Retracing begins at time A; the electron beam is turned off; and the amplifier starts running open loop because output current is not keeping up with the input command. Circuit slew rate is displayed between time A and time B where the output saturates. This slew rate is usually somewhat less than the amplifier rating because overdrive is small and the R_D/C_F network is a feedback path at the equivalent high frequency signal. At time C, the output current has caught up with the command signal, so the op amp begins closing the loop and settling. Time D is the end of the allotted retrace time and the electron beam is turned back on. Note the non-linearity of the current waveform between times C and D will not cause problems because of this timing.

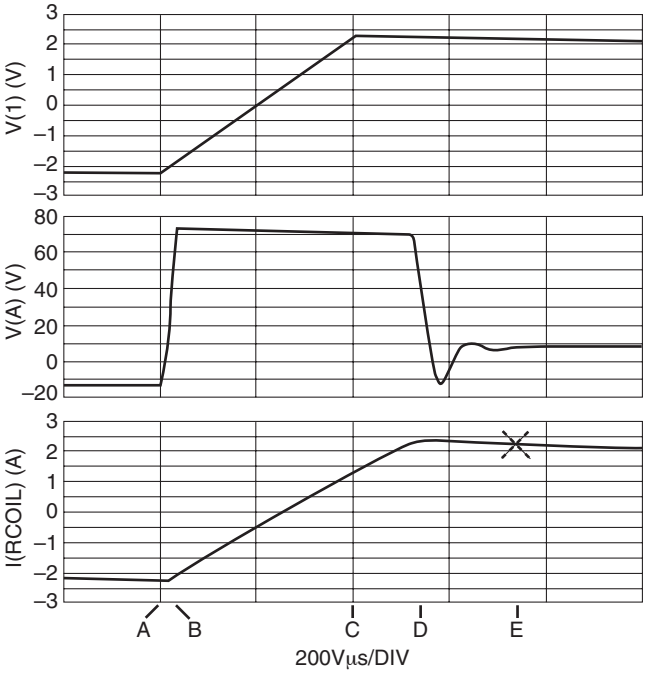

FIGURE 3. RETRACE WAVEFORMS

Note that we calculated a supply voltage requirement of about 73V to change current 5A in 730µs, but most of this change takes place in about 550µs. The first thing making this possible is shown in the amplifier output voltage trace of Figure 3, where saturation voltage of the amplifier is much better than the 6.5V level of the calculations. At time B, current is still flowing through the negative side output transistor, NOT the positive side. The stored energy in the inductor is actually helping the op amp swing closer to the rail. A second factor helping reduce current slew time is again related to stored energy. From time B until current reaches zero, voltage developed across the sense resistor adds to the op amp voltage rather than subtracting from it. Spice analysis indicates peak voltage across the coil at time B is 74.6V.

If a circuit does not include offset and amplitude adjustment capability, the positive peak of the input signal needs to be increased by an amount equal to the normal current change between the actual input peak and time D. From Figure 3 this would be about 5A/15.93ms * .32ms ≅ 0.1A, or 2.35_{VPK} input.

When evaluating slew rates of potential amplifiers for these circuits, note that the amplifier is required to swing nearly twice the peak-to-peak output in a small fraction of the total retrace time. In this example, voltage slewing time was about 10% of the retrace time.

Both the PA02 used in Figure 1, and the PA10 used in Figure 2, have raised accuracy levels by placing the non-linear inductive element inside the op amp feedback loop. The very high gain of the op amp and the use of negative feedback produces superior linearity.

RAPID TRANSITION FOR HEADS-UP DISPLAY

Heads-up displays demand swift transition between any two points on the screen. The waveforms of Figure 4 depict the input drive voltage and required current to the yoke to achieve a single full-scale step in beam position for the circuit in Figure 5. The 3V levels sustain the steady state current through the coil resistance and the sense resistors. The 29V level corresponds to the peak output voltage required for a position change.

Starting with amplifier slew rates and settling times from the data sheet, it is determined what percentage of the total transition time will be required for slewing and settling. A reasonable starting point would be to allow 50% of the total transition time.

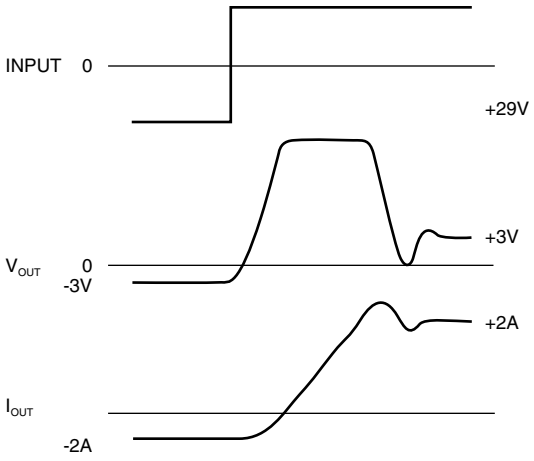

FIGURE 4. FULL SCALE STEP FUNCTION WAVEFORMS

This circuit was designed for a maximum transition time of 4µs when delivering $2A_{PK}$ currents to the 13µH coil. While the fundamentals of this circuit are the same as previously detailed, there are differences due to the higher speed. To achieve rapid transitions, amplifier slew rates must be optimized. As a rule of thumb, compensation for this type circuit should not be lighter than that specified for a gain of 100. Again, the Power Design tool will help selecting values for R_D and C_F. With high speed circuits, it is even more important to analyze performance on the bench to insure parasitics don't spoil the circuit.

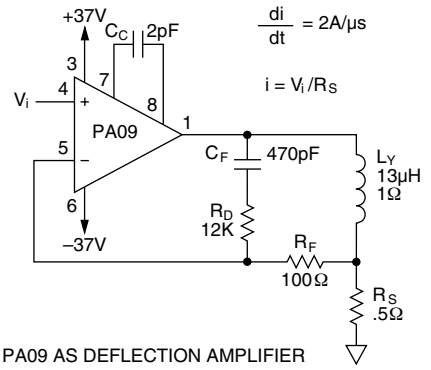

FIGURE 5. PA09 AS DEFLECTION AMPLIFIER

If 50% of the total transition time is allowed for slewing and settling, 2µs will remain to change the yoke current with full voltage applied to the coil. Voltage requirements are calculated as follows:

$$V = di^* L/dt \quad (14)$$
$$V = 4A^*13\mu H/2\mu s = 26V \quad (15)$$
$$V_{DROP} = 2A^* (.5\Omega + 1\Omega) = 3V \quad (16)$$
$$V_{DRIVE} = 26V + 3V = 29V \quad (17)$$
$$V_S = 29V + 8V = 37V \quad (18)$$

With the external compensation selected, the PA09 Data Sheet indicates the amplifier slew rate will be 400V per microsecond. For a calculated swing of 58V, the required voltage slewing time is 145 nanoseconds. Adding the settling time to 0.01% of 1.2µs, the total is comfortably below the 50% allotment of 2 microseconds.

When the circuit was tested, values were further optimized for best performance. The value of R_D had a considerable effect on damping of the circuit. This could be predicted because R_D affects the corner frequency where the roll off slope must be flattened near the unity gain point. The value of C_F was not critical; however, a compensation capacitor of 2pF, as opposed to the data sheet recommendation of 5pF, helped to increase the slew rate without significant affect on stability.

Due to the high speed of PA09, specific precautions are recommended to insure that optimum stability and accuracy are maintained:

1. To help prevent current feedback, use single point grounding for the entire circuit or utilize a solid ground plane.
2. To insure adequate decoupling at high frequency, bypass each power supply with a tantalum capacitor of at least 10µF per ampere of load current, plus a .47µF ceramic capacitor connected in parallel. The ceramic capacitors should be connected directly between each of the two amplifier supply pins and the ground plane. The larger capacitors should be situated as close as possible.
3. Use short leads to minimize trace capacitance at the input pins. Input impedances of 500Ω or less combined with the PA09 input capacitance of approximately 6pF will maintain low phase shift and promote stability and accuracy.
4. The output leads should also be kept as short as possible. In the video frequency range, even a few inches of wire have significant inductance, thereby raising the interconnection impedance and limiting the output slew rate. Also, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.
5. The amplifier case must be connected to an AC ground (signal common). Even though it is isolated, it can act as an antenna in the video frequency range and cause errors or even oscillation.

TRANSIMPEDANCE BRIDGE FOR HIGHER DRIVE VOLTAGE

The circuit illustrated in Figure 8 drives the deflection yoke of a precision x-y display from an available ±15V supply. Only the bridge configuration can provide the high voltage drive levels required with the power supplies available. This enables the system to drive double the single amplifier output voltage. Consequently, the need for separate power supplies solely for CRT deflection is eliminated.

A1 in Figure 6 is configured as a Howland Current Pump. Voltage on the bottom of the sense resistor is applied directly to the load; voltage at the top is the applied voltage plus a voltage proportional to load current. With both these points for feedback, the amplifier sees a common function of load voltage on both inputs which it can reject (CMR), but sees a function of load current differentially. In this arrangement, A1 drives the load anywhere required (with in saturation limits) to achieve load current commanded by the input signal. As ratio match between the two feedback paths around A1 is critical, these four resistors are often implemented with a resistor network to achieve both precision match and tracking over temperature. A2 provides a gain of -1 to drive the opposite terminal of the coil. Gain setting resistors for A2 are not nearly as critical, a mismatch here simply means one amplifier works a little harder than the other. The PA02 brings a unique combination of high slew rate and low saturation voltage to this circuit. Starting values for the R-C compensation network come from Power Design and are fine tuned with bench measurements.

At first glance, it might appear the choice of 2Ω for the sense resistor is quite large because the peak voltage drop across it is 7.5V, or half the supply voltage.

Voltage across the inductor required to move the beam is given by:

$$V_L = 300\mu H * 7.5A / 100\mu s = 22.5V \quad (19)$$

If one were to add to this the peak voltage drop across the coil resistance (1.5V) and the sense resistor (7.5V), it would be easy to assume a total swing of 31.5V or greater than 15V at 3.75A would be required of each amplifier.

Salvation for this problem lies in analyzing current flow direction.

In the middle graph of Figure 7, we find the large sense resistor does not destroy the circuit drive capability. The main portion of the transition is complete in about 80µs and settles nicely.

In the top graph, we find a surprise; both amplifiers are actually swinging OUTSIDE their supply rails. The "upside down" topology of the output transistors in the PA02 allows energy stored in the inductor to fly back, turning on the internal protection diodes. The result is peak voltages in the first portion of the transition greater than total supply.

In the bottom graph, we find stored energy in the inductor develops voltage across the sense resistor, which ADDS to the op amp voltage until current crosses zero. In this manner, peak voltage across the coil is nearly 40V!

The seemingly large value of sense resistor did not kill us on voltage drive requirements and gives two benefits: First, internal power dissipation is lower than with a smaller resistor. Secondly, with larger feedback signal levels, the amplifier closed loop gain is lower; loop gain is larger; fidelity of the current output is better; and voltage offset contributes a lower current offset error.

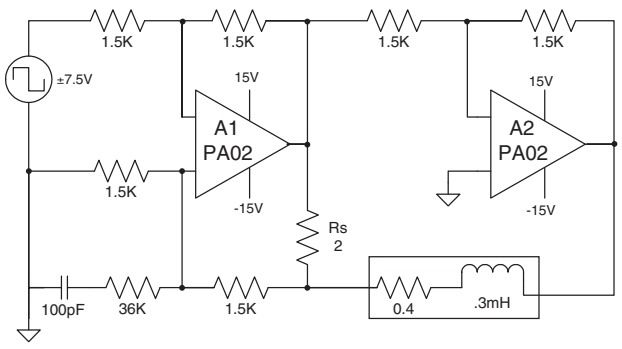

FIGURE 6. CURRENT-OUT BRIDGE DRIVE

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CONCLUSION

The capabilities of the power op amp provide higher accuracy levels, the ability to position beams in any desired position and to retain a steady state position. Having both the power and signals stage in one compact package offers space/weight advantages. The lower parts count increase reliability.

Power op amps are comparatively inexpensive and easy to use. They represent the most efficient solution to reducing development costs and decreasing design time.

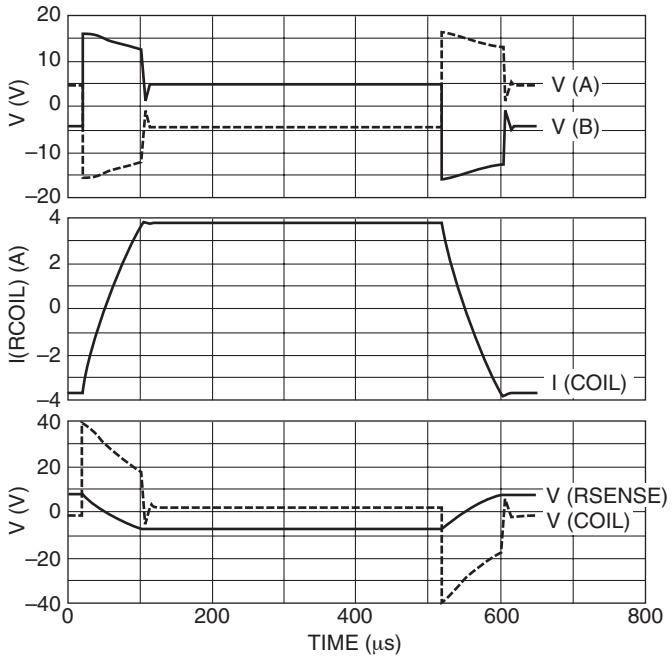

FIGURE 7. BRIDGE DRIVE CURRENTS AND VOLTAGES

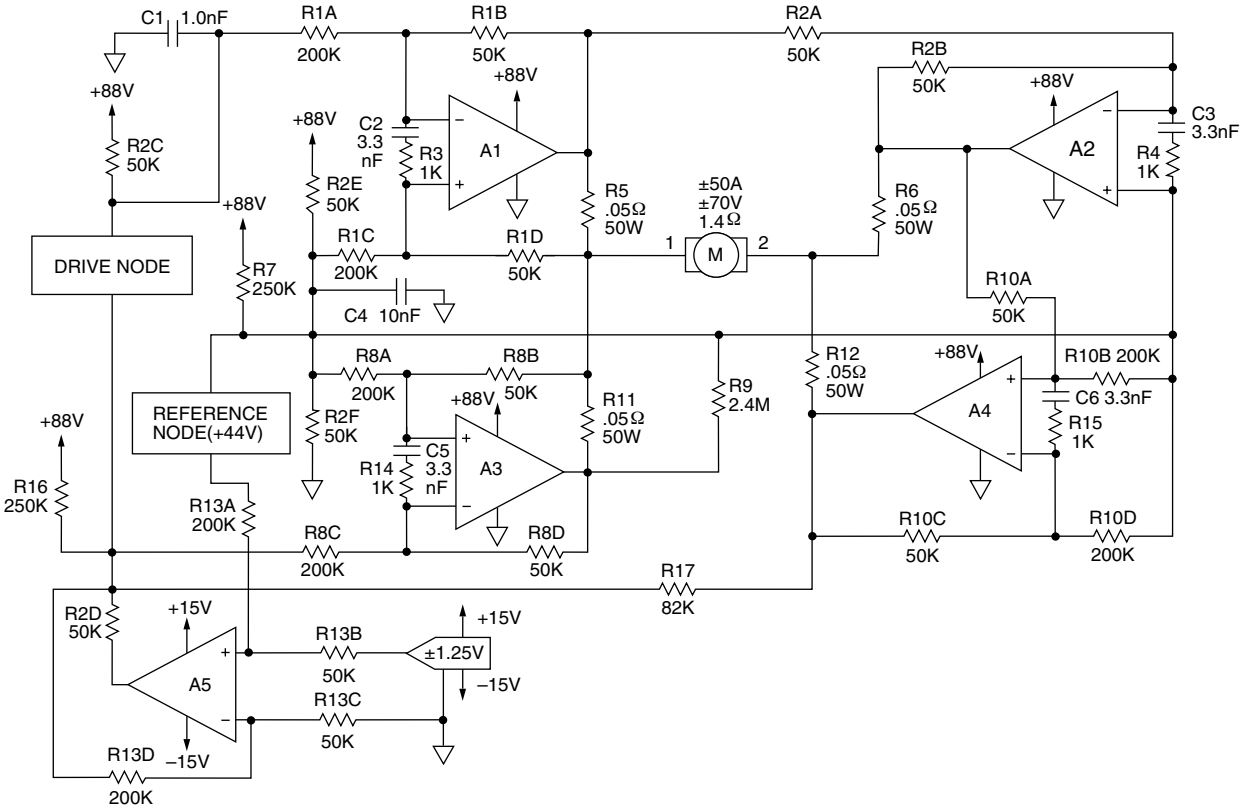

FIGURE 1. APPLYING THE SUPER POWER PA03

INTRODUCTION

The super power PA03 is the result of a design effort to substantially increase output power without sacrificing the high performance engineers are accustomed to when using small signal op amps. Thus, this new building block can perform accurate and complex tasks previously reserved to modular and rack mount devices.

The major applications for the PA03 will be in single ended circuits where up to 1,000W must be delivered to the load or in bridge motor servo systems delivering up to 2,000W peak. Linear motion control, magnetic deflection, programmable power supplies, and power transducer drives are typical of these applications. High power sonar, such as phased array, is another key application made possible by the accurate phase response and linearity of the class A/B output stage. Robot, motion control, and other high current applications which were previously impossible to implement with IC Power Op Amps because of power limits, are now possible using the PA03 as a building block.

The most powerful TO-3 hybrid IC's currently available can dissipate up to 125W and drive loads up to 250W (APEX PA12), while available monolithic IC's handle less. Where peak power requirements for dynamic motor control exceed 250W, three approaches were commonly used to increase power output: (1) parallel or bridge operation of two or more power op amps; (2) external booster transistors; (3) modular or rack mount power op amps.

While these options extend power capabilities, they can have major drawbacks in increased cost, excessive weight and reduced reliability. Furthermore, the large size can be a cumbersome design burden. System designers need a small, reliable power op amp capable of producing up to 1,000W while maintaining top notch performance. The PA03 meets this challenge!

Using the super power PA03 offers many advantages. With an internal power dissipation of up to 500W, the PA03's ratings top the previously most powerful op amp (Apex PA12) by a factor of *four*, and *one* PA03 is more cost effective and far more reliable than *four* less powerful op amps. Its thermal tracking of internal bias components makes the PA03 much safer to use under abnormal conditions than several units in parallel. Moreover, internal protection circuits insure that almost any power level not violating the 2,400W, 1ms Safe Operating Area (SOA) is safe. The amplifier will shut down upon overload, avoiding self-destruction. Internal current limiting resistors eliminate bulky, expensive milliohm external resistors which are normally required for power op amps. The common collector complementary output stage allows the output to swing within 4V of the supply rail at 12A and within 6V at 30A and has full shut-down control. This gives the designer a tool to protect sensitive loads or to minimize power consumption under battery operation. By operating in class A/B, it exhibits low crossover distortion, a feature hard to implement without the inherent thermal tracking of single package construction.

An external balance control option allows the already low offset voltage to be zeroed. The PA03's high overall accuracy makes it suitable for interfacing directly to photo-diodes; to build long time period integrators; or to design 12 bit and better resolution programmable power supplies.

The super power PA03 is a hybrid IC housed in the innovative Power-Dip dual in-line package. It has .060 pins on .200 centers to accommodate higher currents and allows layout on the standard 0.100 grid. The Power-Dip copper header of the PA03 provides 8.5 times the thermal conductivity, and three times the area of the conventional steel TO-3 package.

A SUPER POWER TORQUE DRIVE

The parallel bridge circuit in Figure 1 is shown to demonstrate several possible power enhancement techniques in one application. It operates in the transimpedance mode to drive the torque motor. This allows the D to A converter (DAC) to be programmed directly for delivered torque, since motor torque is directly proportional to armature current. The bridge uses an economic and efficient single output power supply and doubles delivered power levels again by increasing the current drive capability. Delete A3 and A4, and associated components if this option is not required.

Looking at the bridge configuration first, A2 and A4 invert the output of A1 and A3 with respect to the mid-supply reference node. Therefore, A2 and A4 drive the load equal to A1 and A3 in the opposite direction about the mid-supply reference point. The mid-supply node assures that neither amplifier saturates prematurely. Figure 2 shows the actual output voltages of A1/A3 and A2/A4 when delivering full scale output currents to the torque motor.

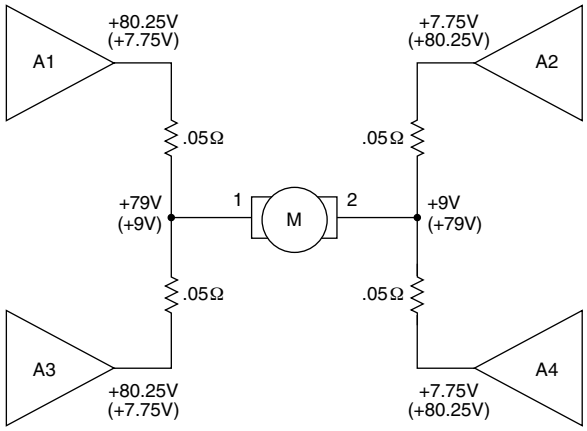

FIGURE 2. FULL SCALE DRIVE VOLTAGES

A5 (Figure 1) configured as a level shifter at a gain of 4, takes the 1.25V input from the DAC and swings the drive node to ±5V with respect to the reference node. A1 and A3 each amplify this differential 5V signal to a ±25A output level driving terminal 1 of the motor. A4 is a unity gain follower of the A2 output voltage. Since A2 and A4 have equal output voltages and equal current control resistors, they share the total 50A current equally.

The very low bias current of the PA03 FET input stage makes it possible to keep power dissipation low by using relatively large value precision resistors. This not only minimizes temperature variations in the resistive networks, but also reduces power dissipation in A5. Current balancing for both the reference and drive nodes is used to prevent level shifting of the high impedance nodes as a function of drive voltage. This is an easy task because of the symmetric drive levels with respect to the reference node.

Figure 3 shows a breakdown of the currents associated with the reference node. R2E and R2F form the basic voltage divider. At a zero drive level, the current through R13A and R13B will match the current through R7. The voltages applied to R1, R8, R9, and R10 will all be zero with respect to the 44V reference so the circuit is balanced. The voltages shown correspond to full scale drive level. R7 roughly balances the current through R13A and R13B to the +1.25V DAC input. R10A, R10B, R10C, and R10D current will nearly match the currents of R1C and R1D plus R8A and R8B. The differences encountered so far total 15 microamps, which is provided by R9 to insure the reference node remains at 44V.

Figure 4 illustrates currents associated with the drive node where R2C and R2D form the basic voltage divider. At zero drive, no voltage is applied to R17, R1 and R8, and the output of A5 will be zero and the drive node voltage will be 44 volts. This means currents of R2C and R2D balance. The currents in R16 balance the currents of R13C and R13D and the remaining resistor currents are zero. For a full scale input of +1.25V, A5 will drive to approximately +10V. The currents through R16, R13C and R13D are no longer balanced because the drive node voltage has risen to 49V. The currents through R1A and R1B, plus R8C and R8D, make the node even less balanced. R17 was selected to slightly over compensate the current imbalance. Since the differential circuit of A5 (Figure 1) controls drive node voltage, its

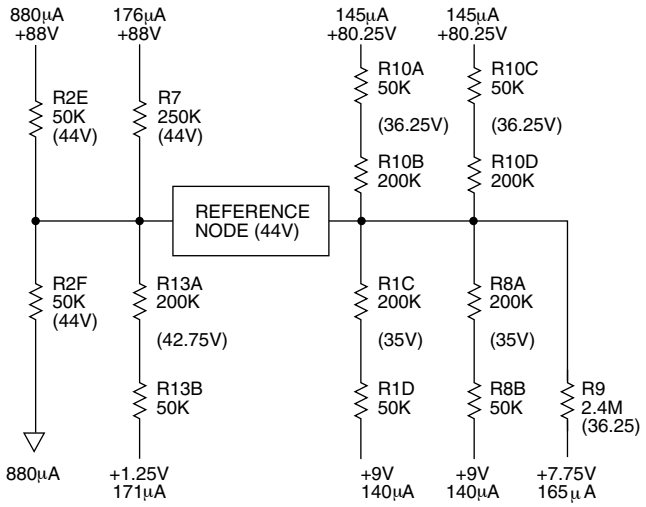

FIGURE 3. CURRENT BALANCING OF THE REFERENCE NODE

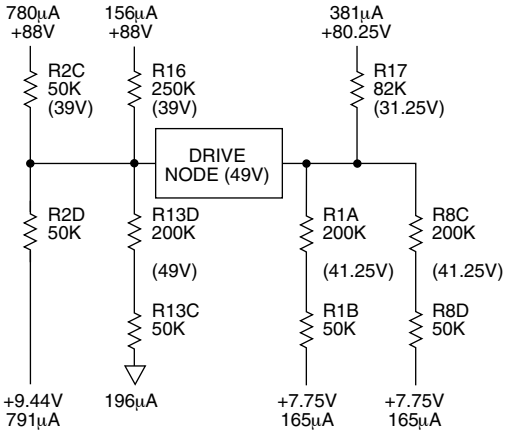

FIGURE 4. CURRENT BALANCING OF THE DRIVE NODE

nominal swing will be a 9.44V, correcting the overall current imbalance of 12µA. Thus the overcompensation of R17 insures A5 will not be required to swing beyond its rated 10V due to component tolerances.

There are a lot of resistor networks in the circuit, but each has a critical task. The ratios are most important to insure gain accuracy. In addition, ratio matching provides common mode rejection and differential voltage amplification. Specifically, the R13 quad around A5 sets drive node swing to +5V with respect to the reference voltage even though the reference changes with supply variations. Similarly, the R1 quad and the R8 quad set the full scale voltage across sense resistors R5 and R11 at ±1.25V. The ±35V output swings across the impedance of the torque motor are rejected as a common mode signal to maintain the programmed voltage to current transfer function. Thus impedance variations of the motor winding and the associated connections do not affect accuracy. R10 fixes the gain of A4 to unity while keeping its input pins about 4V closer to the reference than the amplifier's output voltage. With the output swinging to within nearly 7V of the supply rails, the common mode voltage requirement of ±Vs –10V is satisfied.

A PROGRAMMABLE POWER SUPPLY USING THE PA03

Figure 5 shows the PA03 in a simple, reliable programmable power supply which utilizes the PA03's shutdown features. It requires little calibration because the current to voltage conversion of the D to A converter output is done by the power op amp itself, and the 12 bit DAC80 provides accuracy levels high enough to eliminate the need for adjustments.

The programmable power supply is designed to test DC-to-DC converter modules drawing up to 15A. The majority of tests are

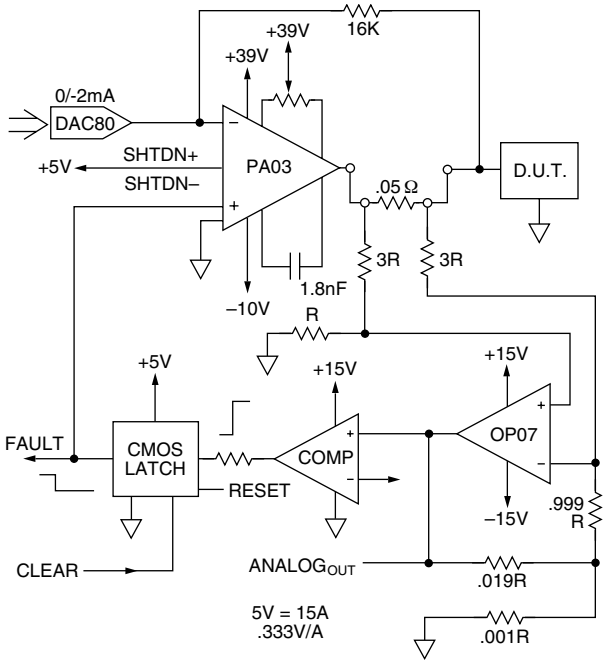

FIGURE 5. HI-POWER PROGRAMMABLE POWER SUPPLY APPLICATION

performed at 28V. High and low limits of 18.5V and 32V will be applied for 500ms. The outputs must be accurate to within 0.5% and survive an occasional short circuit to ground.

The OP07 differential amplifier circuit senses the D.U.T. current on the four-terminal shunt resistor, and provides a signal of 0.333V/A to the comparator. The comparator will trip at a current of 18A, setting the latch, and the latch then shuts down the PA03 until the fault is cleared and the latch is reset. This safety circuit limits arcing hazards in the test socket.

The feedback resistor of 16KΩ yields the required 32V full-scale output when the DAC output is 2mA. The 0.05Ω current sense resistor develops a 0.75V signal at the full-scale output current of 15A. This amplitude is a compromise between monitoring the current accurately without imposing an excessively high power rating on the sense resistor. However, the sense resistor still must be mounted on a heatsink due to 11.25W dissipation at 15A and the possible 88W at the built-in maximum current limit of 42A.

To derive the power supply voltage needed, the 0.75V drop on the sense resistor must be added to the headroom (supply-to-output differential) required by the op amp. From the PA03 specifications (a drop of 7V at 30A and 5V at 12A), a maximum drop of 6V at 15A can safely be assumed. Selecting a positive voltage of 39V leaves a margin of 0.25V. Without remote sensing, such a conservative approach is best due to potential IR drops in the high current leads. For the negative supply, a minimum operating voltage of 10V is required to satisfy the input common mode voltage specifications.

Four power levels must be examined to determine the worst case maximum power dissipation of the power op amp. The first three are the output voltage levels for the devices under test at the maximum current of 15A. Calculating all three shows the 18.5V output to be the worst case scenario. The 18.5V output plus the 0.75V drop across the sense resistor leaves a voltage of 19.75V across the output stage of the PA03. At 15A, this produces an internal power dissipation (including quiescent power of 9.8W) of 306W and a junction to case temperature rise of 92°C (PA03 =0.3°C/W).

Because the worst case power demand exists only for 500ms, an examination of average power and thermal time constants will help to reduce the heatsink size. Figure 6 shows the general test plan and the specific testing sequence with the resulting power dissipation levels demanded of the PA03. The 32V output level requires 103.6W (39V supply less 32V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for 500ms. The 28V level amounts to 163.6W (39V supply less 28V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for another 500ms.

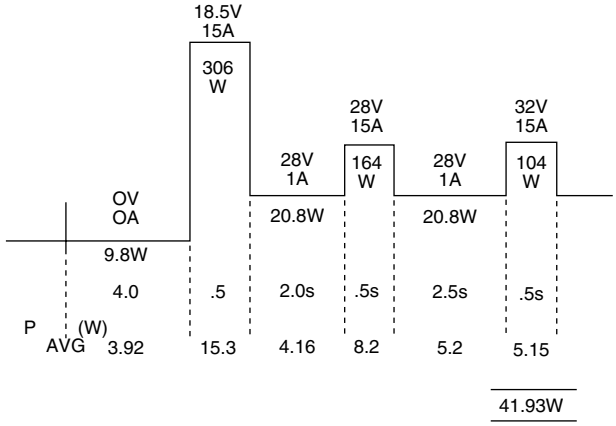

FIGURE 6. PROGRAMMABLE POWER SUPPLY INTERNAL POWER DISSIPATION

For the balance of the test of 4.5s, the maximum current of 1A amounts to 20.8W. During the minimum removal/insertion time of 4s, the power dissipation is only the quiescent power of 9.8W. This means the average power dissipated is only 41.9W. With a heatsink that has a thermal time constant of ten seconds, the highest peak (306W for 500ms) amounts to 5% of the time constant, or 4.9% of the rise for 306W continuously. Adding this spike equivalent of 15W to the 41.9W average will bring the peak short term equivalent power to 57.23W (though this peak could vary slightly depending upon the exact timing).

If, for reliability, a peak junction temperature of 150°C is selected, and a maximum ambient temperature of 38°C is assumed, the allowable temperature rise of the heatsink is 18°C (150°C– 38°C–92°C). At a peak short term equivalent of 52.2W, this requires a heatsink rated at 0.35°C/W. The Apex HS06 (0.6°C/W free air) with a forced air velocity of 500 ft/min can provide the required rating.

In this application, if abnormal situations arise due to faulty timing or defective test units, short term operation at the 306W level will not destroy the PA03 because the thermal shutdown will limit the temperature rise. The worst case would be a short in the test socket which could push the PA03 to a maximum current limit of 42A. At this current, the sense resistor (R_S) would drop 2.1V leaving 36.9V across the PA03. These current and voltage levels (1.55KW) are well within the PA03's 1ms second breakdown line of the SOA curve. Therefore, the fast response of the PA03's thermal shutdown circuit will protect the power op amp for the time required to eliminate the short.

REMOTE SITE MOON BOUNCE ANTENNA MOTOR DRIVE

Power conservation is essential for solar powered data gathering, while a considerable amount of motive force is required for positioning a 40 Ft dish antenna.

With a 3° beam angle and a position accuracy of 0.5°, the lunar angular velocity of 14.4°/Hr allows a position update only once per minute. The PA03's shutdown control used for intermittent operation combined with a worm gear drive to hold position during shutdown periods, facilitates an energy efficient positioning system.

The D to A Converter in Figure 7 converts position data to a voltage which is fed to the inverting input of the PA03 configured as an integrator by feedback capacitor C1 and input resistor R1. The precision reference and potentiometer apply a feedback voltage equivalent to actual position to the non-inverting input. The PA03 drives the motor with the integrated difference between the desired and actual positions. R2 acts as a damping element limiting the integration time constant to minimize overshoot.

The shutdown control is released for six seconds after each position update, which allows the PA03 sufficient time to position the antenna and reduces the standby power to 2W for 54 seconds or 90% of the time.

The normal current requirement of the motor is 8A, but under high wind conditions, up to 17A may be drawn. In this application, the amplifier output will be decaying pulse; thus driving the motor to a new position once a minute. Because the amplifier is at maximum

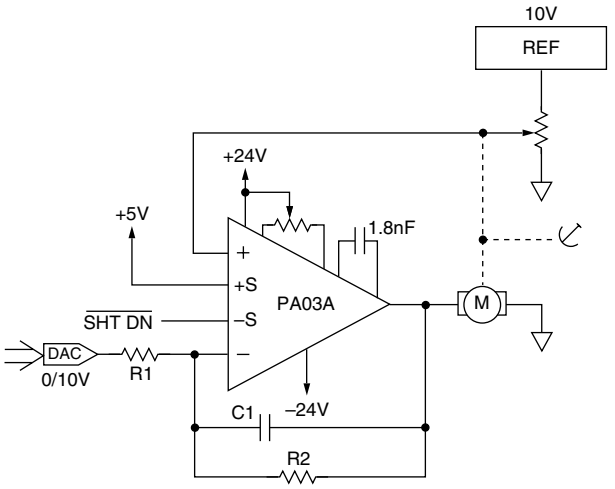

FIGURE 7. REMOTE SITE MOON BOUNCE APPLICATION

output (saturated) most of the time, the power dissipation at the full output voltage is the appropriate level to calculate.

At 17A the PA03 will drive to within 5.5V of the supply voltage (rail) dissipation of 93.5W. The quiescent current of 0.2A times the total supply voltage of 48V adds another 9.6W for a total of 103.1W dissipated in the amplifier. At the maximum ambient temperature of 45°C and a maximum junction temperature of 140°C, the allowable rise is 95°, which requires a thermal resistance for the heatsink as follows:

Q_{HS}= 95/103.1– 0.3 = 0.62°/W.

The Apex HS06 meets this criteria.

Under normal low wind conditions, the peak battery drain will be 201.6W. However, due to the 10% maximum duty cycle and the power-saving shutdown feature of the PA03, the average power consumption will be only:

P_{AV} = 0.1 (24*8+48*0.2) +0.9 (48 *0.040) = 22W

To further reduce standby power to 2W, the shutdown feature can be activated only when communications are required.

USING THE PA03 IN YOUR APPLICATION

To achieve maximum efficiency, the power supply voltage should be selected for the minimum voltage necessary to produce the required output.

For example, to obtain a ±45V output at 12A, add the supply-to-output differential as specified on the Data Sheet (±5V) to produce ±50V.

Dual supplies may be as high as ±75V and asymmetric or single supply operation is permitted as long as the total rail-to-rail voltage doesn't exceed 150V. Input voltages must always be at least 10V less than the power supply voltage due to the common mode voltage specification being supply voltage minus 10V.

Because of the greater power levels involved, the thermal path to remove the heat from the amplifier is of great importance to the successful application of the PA03. A 1°C/W rated heatsink may be suitable to remove 20-50W, but it is insufficient to handle 500W. For the PA03, a heatsink with a thermal resistance on the order of 0.1°C/W is often required such as: very large surfaces, forced air cooling, or even water cooling. Fortunately, if insufficient heatsinking is provided, the unique safety circuits of the PA03 will generally result in thermal shutdown rather than destruction. Destructive power levels are so high that in most applications they need not be of any concern.

As with all high current Power Op Amps, precautions must be taken to avoid current feedback due to voltage drops in the wiring of electromagnetic radiation. This is especially true when using the PA03 because of its higher current rating. The wiring for all supply and output leads must be done with wire equivalent to 12 gauge or thicker, as the PA03 has a higher current capacity than most branch circuits in residential wiring.

To avoid feedback through the power supplies, they must be bypassed with a ceramic capacitor of 0.47μF or greater, in parallel with a 10μF per ampere of peak output current (up to 300μF), mounted not more than 1.5 inches from the supply lines.

Even when using excellent bypassing components, good layout techniques and quality power supplies can easily cause substantial AC ripple. Ripple must be considered as a possible source of error. Positive feedback can also occur if the power supply also powers other circuit elements.

WATCH THE POWER DISSIPATION

The internal power dissipation (P) in a DC circuit is:

$$P = (V_S - V_O)\, I_O + (|+V_S| + |-V_S|)\, I_Q$$

where: I_O: OUTPUT CURRENT
I_Q: QUIESCENT CURRENT
V_O: OUTPUT VOLTAGE
V_S: SUPPLY VOLTAGE

Errors often arise in the calculation if the wrong supply voltage is used. The voltage (V_S) must be the one at the supply pin sinking or sourcing the current. Incorrect selection of the worst case conditions (short to ground or supplies) can also create errors.

When driving reactive loads, due to the phase shift between output voltage and current, the power dissipation may be several times higher than the equivalent resistive loads. These have a totally different, but equally simple approach that can be used to obtain the correct power dissipation (P):

$$P = P_I - P_O$$

where: P_I = POWER DRAWN FROM THE POWER SUPPLY
P_O = POWER DELIVERED TO THE LOAD

Keep in mind that using purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier.

JUNCTION TEMPERATURES

The absolute maximum power dissipation of the PA03 is 500W and was derived using the industry standard derating procedure. This assumes operation at maximum junction temperatures (175°C) with the case at 25°C.

With the power dissipation and the maximum ambient temperature (T_A) of the application known, the operating temperatures of both case (T_C) and junction (T_J) of the power transistors can be determined:

$$T_C = T_A + P \cdot \Theta_{HS}$$

where: Θ_{HS} = THERMAL RESISTANCE FROM THE HEATSINK MOUNTING SURFACE TO AMBIENT AIR

Θ_{JS} = INTERNAL THERMAL RESISTANCE, JUNCTION TO CASE

Apply this to the PA03 by following these steps:

1. Calculate the maximum internal power dissipation (P).
2. Determine the maximum junction temperature allowable to achieve the desired reliability of the PA03. This must be less than 175°C. Apex recommends 150°C or less.
3. Calculate T_J– T_A, the allowable rise of the junction temperature above the maximum ambient temperature.
4. Calculate the required thermal resistance of the heatsink:
$\Theta_{HS} = (T_J - T_A)/P - \Theta_{JC}$

For example, in a circuit dissipating 300W at an ambient temperature of 30°C and the junction temperature not to exceed 150°C:

Θ_{HS} = (150 – 30)/300 – 0.3 = 0.1°C/W

HOW THE PA03 WORKS

The circuit diagram shown in Figure 8 shows that the input section of the PA03 is similar to most Apex FET input hybrid power op amps. Q21, D1 and D4 form voltage references to bias both input and output stages of the amplifier. Q31 is the current source for the input stage which consists of Q20A and Q20B (the FET input pair), Q17 and Q18 (the cascode transistors), and Q2 and Q3 (the half dynamic load). The current through Q5 sets the operating voltage (source-drain) for the FET input pair. Q12 acts as an impedance buffer between the high

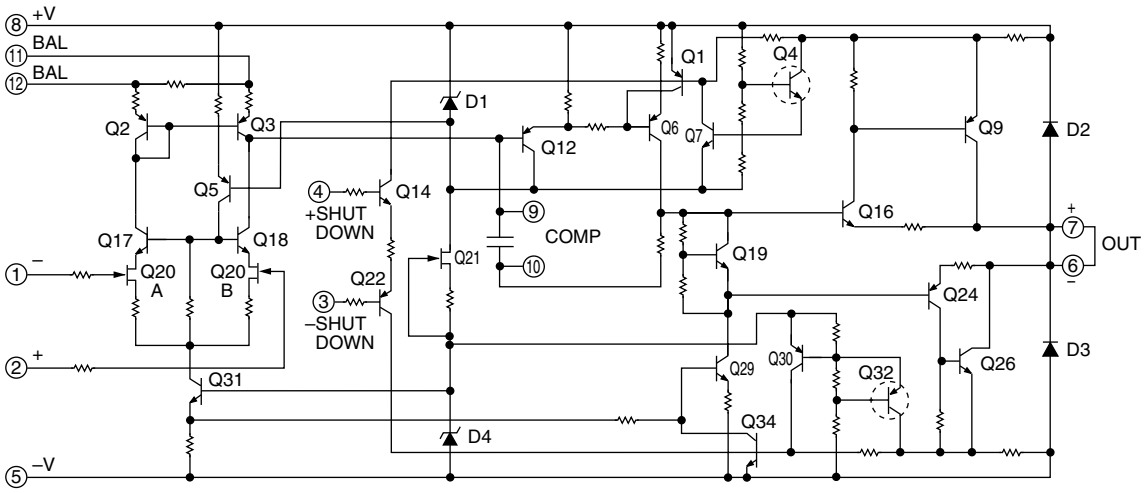

FIGURE 8. PA03 EQUIVALENT SCHEMATIC

output impedance of the input stage and Q6, the output driver.

The collector load of output driver Q6 consists of current source, Q29, and the output stage consisting of Q16, Q9, Q24, and Q26. The common collector configuration of Q9 and Q26 enable the PA03 output to swing close to the supply rails. Inverters Q16 and Q24, form local feedback networks which cause the output stage to be linear like an emitter follower with very high input impedance. The V_{BE} multiplier Q19, provides DC bias for the output transistors via Q16 and Q24, and is thermally coupled to the power dissipating transistors in the output stage. In addition, the V_{BE} multiplier utilizes thermistors to fine tune the temperature stability of the quiescent current through output transistors Q9 and Q26. This class A/B stage provides low crossover distortion, as well as stability of the quiescent current over the full temperature range.

D2 and D3 are high speed diodes which protect the output stage from inductive kickback by bypassing it into the supply rails. The 18.6 milliohm emitter resistors of Q9 and Q26 sense the output current of the amplifier. Currents in excess of 35 amps will develop .65 volts, thereby turning on Q1 or Q34. In turn, these transistors rob the base drive from Q6 or Q29, thus limiting the output currents to 35A. Q4 and Q32 are the sensors for the innovative SOA protection of the PA03. These two transistors are mounted directly on top of power transistors Q9 and Q26, eliminating thermal gradients and minimizing the response time to temperature changes in the output transistor junctions. The emitters of the sensors are connected to Q7 and Q30 which act as level translators to turn on current limit transistors Q1 and Q34, respectively. The complementary pair Q14 and Q22 activate the shut down of the PA03. While common mode voltage is rejected, differential voltages applied between these two transistors turn on the current limit circuit consisting of Q1 and Q34, thereby shutting down the entire output stage. In this mode the output pins appear as a high impedance to the load. Figure 9 illustrates the physical arrangements to achieve fast and reliable thermal shut down.

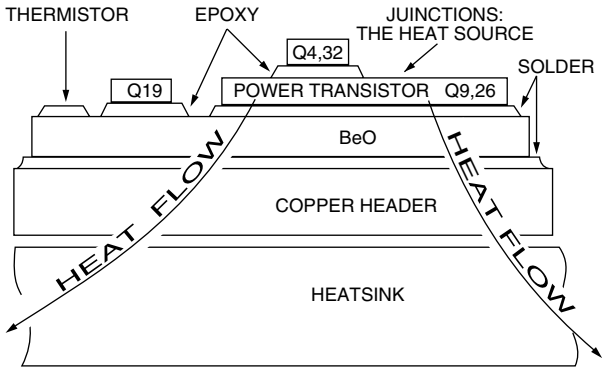

FIGURE 9. THERMO-MECHANICAL DESIGN

CONCLUSION

The PA03 is a versatile new building block which eases many design tasks and overcomes size and weight barriers which previously prevented implementation of linear power controls in limited space. The giant step up in power levels, improved protection circuits and high performance small signal characteristics make the PA03 a very cost effective innovation.

G

APPLICATION NOTE 7

POWER OPERATIONAL AMPLIFIER

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INTRODUCTION

The programmable power supply (PPS) is not only a key element in automated test equipment, but it is also used in fields as diverse as industrial controls, scientific research and vehicular controls. When coupled to a computer, it bridges the gap from the software to the control task at hand. This application note examines the basic operation of the PPS, the multitude of possible configurations and the key accuracy considerations.

VOLTAGE OUTPUT VERSIONS

The most basic and often most accurate version of the PPS requires only a current output Digital to Analog Converter (DAC), a power op amp and a feedback resistor as illustrated in Figure 1. According to op amp theory, the voltage at the inverting input (summing junction) will be zero and op amp input current will be zero. As a result, all current from the DAC flows through the feedback resistor R_F. Ohm's law then causes the circuit to provide a precise output voltage as function of DAC output current. Given a perfect DAC and feedback resistor, only two op amp parameters contribute significantly to the output voltage errors. These are voltage offset (V_{OS}), modeled by the battery, and bias current (I_B), represented by the current source. Due to the high output impedance of the current output DAC in relation to R_F, V_{OS} errors appear at the output without gain.

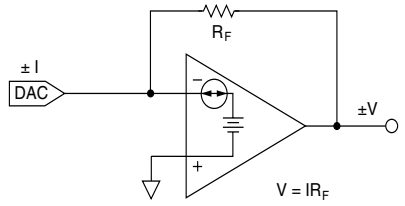

FIGURE 1. CURRENT TO VOLT CONVERSION

For a 10V output and op amp offset of 5mV, this error contributes only 0.05%. For a 100V output, a 0.5mV offset contributes an error of only 5ppm. Clearly, the DAC can easily be the major error source.

Op amp bias currents add to the DAC output current. The majority of available DAC's have full scale currents of ±1mA or 0/2mA. Most of today's bipolar input power op amps feature bias currents of less than 50nA. This results in errors of only 25 ppm maximum of the full scale range (FSR). FET input bias currents at 25°C are seldom over 100 pA and are specified as low as 10pA. These errors translate to 0.05ppm and 0.005 ppm. Since FET bias currents are generally characterized as doubling every 10°C, the bias current of the two examples could become 100nA and 10nA at 125°C, producing errors of 50ppm and 5.4ppm, respectively. Again,the DAC is the critical error source.

To determine the significance of the error contribution of a specific power op amp to the performance of various systems, refer to Table 1, next page. The least significant bit (LSB) is the value of the smallest step change of output. Comparing the calculated errors to the LSB values reveals system compatibility. For current output, DACs op amp bias currents compare directly with the DAC current LSB and V_{OS} errors compare directly with the full scale output voltage. Thus, the importance of low bias currents is dependent solely on system resolution. However, the significance of voltage offset specifications varies with both resolution and full scale voltage range.

USING VOLTAGE OUTPUT DACs

When using a voltage output DAC, the power op amp can be added with either inverting or non-inverting gain to form the PPS. It usually costs more than implementation with a current output DAC, and has less accuracy. However, system or logistic factors may dictate the use of the voltage output DAC.

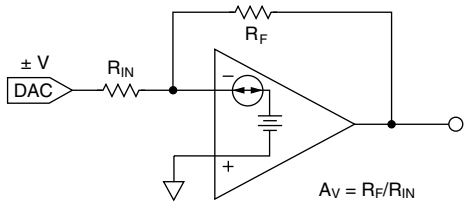

FIGURE 2. INVERTING VOLTAGE GAIN

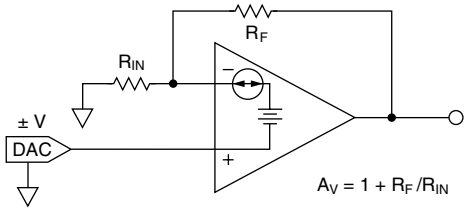

FIGURE 3. NON-INVERTING VOLTAGE GAIN

Figure 2 illustrates the basic inverting gain version and Figure 3 shows a non-inverting setup. Error calculations are still simple even though some new variables have been added. Voltage offset errors appear at the output multiplied by the gain of the circuit (A_v+1 for inverting circuits). To maximize accuracy, the highest output DAC's should be used with minimum voltage gains in the op amp configuration. When using ±10V DAC's, a direct Vos to LSB comparison can be made using the 20V FSR values listed in Table 1. Also, bias currents flow through the feedback resistor producing output voltage errors; thus, values of R_F and R_{IN} are usually kept as low as possible.

A CASE FOR REMOTE SENSING

The circuit of Figure 4 shows the wire resistance (R_W) from the power op amp to the load and back to the local ground via the power return line. A 5A load current across only 0.05Ω in each line would produce a 0.5V IR drop. Without remote sensing, this would become an error at the load. With the addition of the second ratio matched R_F/R_{IN} pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop; therefore, as long as the power op amp has the voltage drive capability to overcome the IR losses, accuracy remains high.

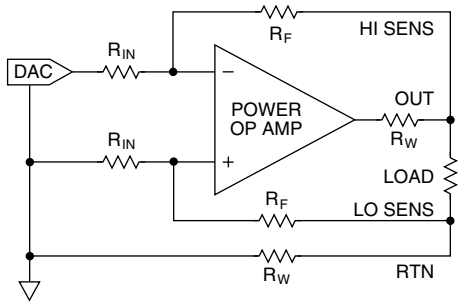

FIGURE 4. REMOTE SENSING PROGRAMMABLE POWER SUPPLY

CURRENT OUTPUT VERSIONS

A current output PPS using a current output DAC can be implemented as shown in Figure 5. Another version of the current output PPS is shown in Figure 6. This allows the load to be grounded, but is more complex and has additional errors. Especially if the output currents are relatively low, the current through the lower R_F/R_{IN} pair may become significant because it is also sensed by R_S. Major errors can be caused by ratio mismatching between the R_F/R_{IN} pairs. The resulting voltage errors across the sense resistor equal the output voltage times the ratio mismatch. For example, consider a 0.2Ω sense resistor, a 5A output requiring a 20V drive and a ratio mismatch of only 0.1% causes an error of 2%. Even an 8-bit LSB is only 0.39%!

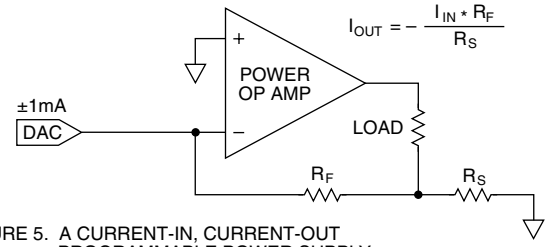

FIGURE 5. A CURRENT-IN, CURRENT-OUT PROGRAMMABLE POWER SUPPLY

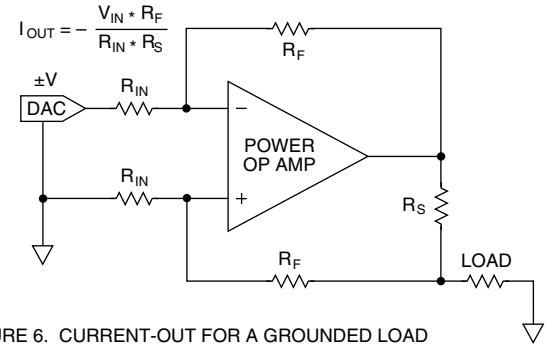

FIGURE 6. CURRENT-OUT FOR A GROUNDED LOAD

In all of the current output circuits discussed, errors due to voltage offset appear across the sense resistor at a gain of one or more. This means higher sense resistor values will minimize output current errors at the expense of increased power dissipation in R_S, the power op amp and system power supplies. One other word of caution, if the load contains inductive elements, refer to Applications Note 5 which discusses maintaining stability in precision current output circuits having reactive loads such as deflection coils. A current output PPS using a voltage output DAC is shown in Figure 7. The power op amp drives current through the load until voltage on the sense resistor (R_S) equals the input voltage. To achieve high efficiency (low voltage across R_S compared to the load voltage), this circuit requires a low voltage DAC or a high voltage op amp. If neither is possible, the circuit of Figure 8 allows the sense resistor voltage drop to be lower than the input voltage.

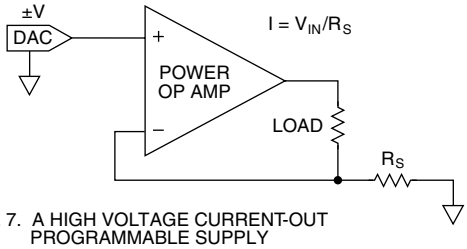

FIGURE 7. A HIGH VOLTAGE CURRENT-OUT PROGRAMMABLE SUPPLY

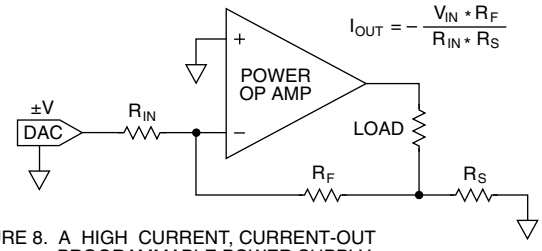

FIGURE 8. A HIGH CURRENT, CURRENT-OUT PROGRAMMABLE POWER SUPPLY

PROGRAMMABLE ACTIVE LOADS

To obtain the V-I characteristics of a power source, it may be desirable to control the output voltage and measure the output current or visa versa. The current output circuits shown are suitable as active current loads. The circuit of Figure 9 performs voltage loading of a solar cell panel. The power op amp forces the DAC voltage to appear across the panel and also performs an I to V conversion providing the data to plot V-I characteristics.

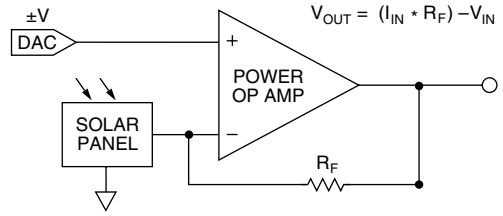

FIGURE 9. SOLAR PANEL TESTER

Due to its flexibility, accuracy and ease of use, the power op amp is the leading choice when programmable power supplies are called for. They greatly simplify circuits requiring unipolar outputs and are very cost effective when designing bipolar power supplies. The only remaining question is whether to buy the power op amp or to make one in discrete form. For low quantity production runs, the required design effort renders the "make" option too expensive. For high volume runs, the question is more involved. In many applications, the smaller size and lower weight plus high reliability, make the "buy" decision the only reasonable choice. (See "The Advantages of IC power op amps.") In all applications, the hybrid power op amp enhances design quality, speeds assembly and reduces overhead costs.

		FULL SCALE RANGE			
BITS	PPM	2mA	20V	50V	200V
8	3906	7.8μA	78mV	195mV	.78V
10	977	1.95μA	19.5mV	48.8mV	195mV
12	244	488nA	4.88mV	12.2mV	48.8mV
14	61	122nA	1.22mV	3.05mV	12.2mV
16	15.3	30.5nA	305μV	.763mV	3.05mV

TABLE 1. LSB VALUES FOR VARIOUS OUTPUT LEVELS

G

APPLICATION NOTE 8

POWER OPERATIONAL AMPLIFIER

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THE MODERN POWER OP AMP

Power op amps are attractive because they reduce circuit design time enormously. Assembly costs of the power op amp design amount to a fraction of the discrete counterpart due to vastly reduced parts count. Careful attention to the power aspects of a circuit is required, as the well known op amp design rules based on low power devices. The objectives are to maximize reliability plus optimize output power and system efficiency. This application note points out some optimizing techniques and some areas to be especially watchful.

INTERPRETING SPECIFICATIONS

The first step in achieving high power levels is to operate within specifications. This means check the data sheet first. Apex data sheets are divided into product description, absolute maximum ratings, specification table, typical performance graphs, and application hints. Each section should be checked for relevant information.

Absolute maximum ratings are stress levels which, when applied to the amplifier one at a time, will not cause permanent damage. However, proper operation is only guaranteed over the ranges listed in the specifications table. For example, most amplifiers have an absolute maximum case temperature range of –55°C to 125°C. If the specified operating temperature range is less, i.e. –25°C to 85°C, an amplifier may latch to one of its supply rails when operating above that temperature (+85°C). However, the device will not sustain permanent damage unless the latched condition also violates the safe operating area. Simultaneous application of two or more of these maximum stress levels, such as maximum power and temperature, may induce permanent damage to the amplifier.

The generally accepted industry method of specifying absolute maximum power dissipation assumes the case temperature is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick to compare ratings of various manufacturers. However, it is not a reliable operating point. An ideal heatsink is required, and even with the best heatsink, it would still result in reduced product life due to operation at extreme temperatures. APEX recommends maximum junction temperature of 150° or less.

The specifications table should be the prime working document while designing the application. In addition to the minimum/maximum parameters (voltage offset, output capability, etc.), this table contains the guaranteed linear operating ranges: common mode voltage, temperature ranges, power supplies, etc.

Typical performance graphs are most useful in determining performance variation as operating conditions change. For example, all amplifiers are specified for a minimum voltage output at maximum current rating. If your application needs only 75% of this current, you might determine from the typical graph you will gain 0.5V at this level. A safe design will assume output capability of 0.5V better than the specification table, not the actual number on the typical graph. Bear in mind, if your design is based on the typical performance graphs, it will statistically work 50% of the time.

OPTIMIZING THE POWER SUPPLY

To deliver the most output power and achieve maximum efficiency, internal power dissipation must be minimized. This condition is met if the power supply voltage is selected for the minimum voltage necessary to produce the required output. Internal power dissipation is the sum of quiescent power *plus* the product of output current *and* the supply to output differential. Supply voltage is the only variable for the designer to optimize. Refer to the product data sheet's specified minimum supply to output differential voltage. Each extra volt here dissipates one more watt for every ampere of output current. Trade-offs in this area are not recommended. Deriving required outputs from existing system supplies reduces efficiency if the difference between supply and required output exceeds the supply to output differential of the op amp. Also, this supply vs. efficiency trade-off must be considered when contemplating the use of unregulated supplies. When using unregulated supplies, line and load variations must be taken into consideration along with the ripple content of the supply. The result is a voltage band above the minimum operating voltage required by the power op amp to produce the required output. Power in this band must be dissipated. Voltage above the minimum operating voltage decreases the power handling capability of the power op amp.

The choice is whether to dissipate the power in the power op amp or in a separate regulator. As current levels increase, the dollar per watt cost generally rises faster for the power op amp than it does for a DC regulator.

Usually, unregulated supplies are not economical because they lack transient protection. Power lines are notorious for being extremely noisy. They have high voltage, high speed spikes riding on the sine wave which pass right through the power transformer. Furthermore, the large electrolytic capacitors used for filtering often do not have low equivalent series resistances at those high frequencies. A 1K volt spike on the incoming line can result in an excessive voltage spike at the amplifier supply pin. Destruction of the op amp may be the result. Therefore, line filters and zener clamps are required to eliminate the voltage spikes; thus, the economy of unregulated supplies is reduced.

Once the minimum supply voltages above have been selected, steps need to be taken to minimize IR losses. Some of today's modern hybrid power op amps handle currents higher than most branch circuits in residential wiring. Losses can be kept to a minimum, especially as frequencies increase, if leads are as short as possible between supply and amplifier, as well as between the amplifier and the load. In the video frequency range, where even a few inches of wire have significant inductance, and the skin effect increases the resistance of heavy wires at high frequency, multi-strand litz wire is recommended.

SINGLE OR ASYMMETRIC SUPPLY OPERATION

Asymmetric output swings present another opportunity to optimize power supplies. Consider the circuit of Figure 1. If the symmetric power supplies were used, power dissipation would be substantially increased, a power op amp with a higher voltage rating would be necessary and output power would be reduced.

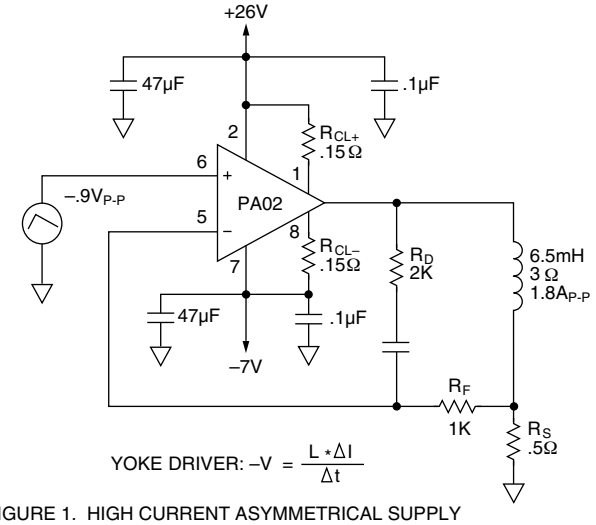


FIGURE 1. HIGH CURRENT ASYMMETRICAL SUPPLY

Fortunately, most power op amps are suitable for operation from a single supply voltage. The common mode operating requirements do, however, impose the limitation that the input voltages not approach

closer than 5 to 10 volts to either supply rail (determined by the common mode voltage specification). Thus, single supply operation requires the input signals to be biased 5 to 10V from either supply rail. Figure 2A illustrates one bias technique to achieve this.

Figure 2A illustrates a very practical alternative to single supply operation, a second low voltage supply. This allows ground referenced input signals, but also maximizes the voltage swing of the unipolar output. The 12 volt supply in Figure 2B must usually supply only the quiescent current of the power op amp unless the load is reactive or EMF producing.

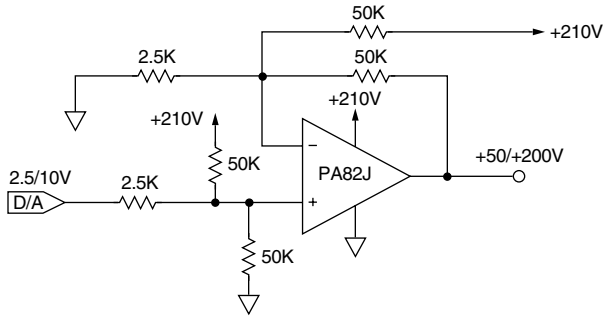


FIGURE 2A. TRUE SINGLE SUPPLY OPERATION

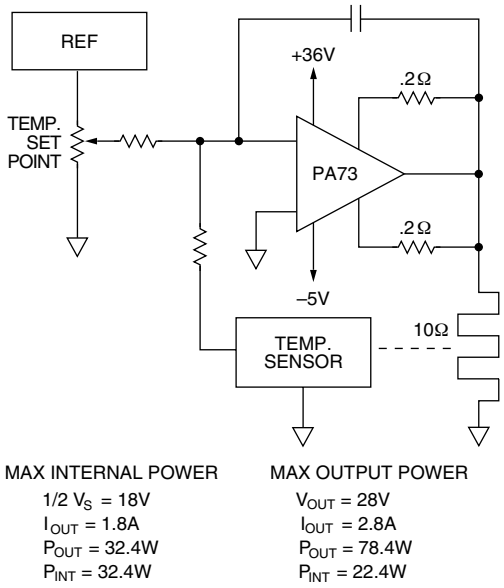


FIGURE 3. TEMPERATURE CONTROL CIRCUIT POWER LEVEL

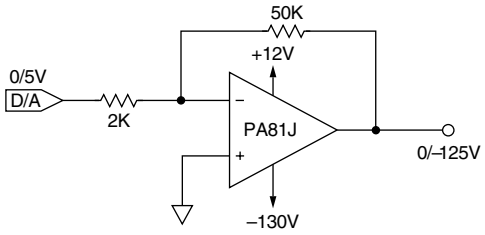


FIGURE 2B. ASYMMETRIC SUPPLIES

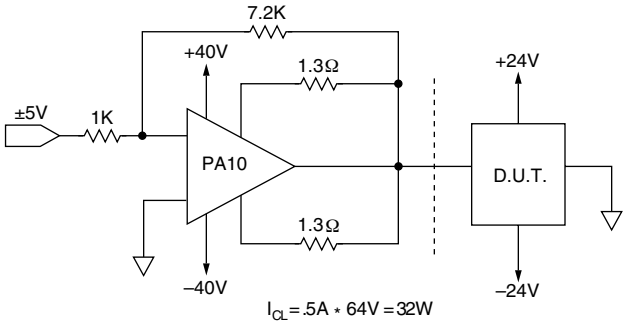


FIGURE 4. PPS POWER DISSIPATION CONSIDERATIONS

KNOW YOUR POWER DISSIPATION

Power requirements of the load are most often well known, but calculating the power dissipated inside the amplifier is not always simple.

For purely resistive loads, maximum internal power dissipation occurs when the output voltage equals half the supply voltage. This is the worst case to analyze if the amplifier does not have to withstand short circuits. An example of DC application is the temperature controller in Figure 3.

Programmable power supplies (PPS) for automated test equipment must often tolerate short circuits in the device under test. For the PPS shown in Figure 4, the worst case dissipation will occur with a short to one of the 24V DUT supplies if the PPS is programmed to the opposite voltage. Assuming the current limit of the 24V supply is greater than the PPS limit, the PPS goes into current limit with considerably higher power levels than encountered under normal operation. Worst case for the amplifier could be its supply voltage plus the DUT supply voltage times the current limit.

AC OUTPUTS ALLOW HIGH POWER LEVELS

If an AC drive has a frequency of 60Hz or greater, the halfwave period of the power dissipating waveform is shorter than the thermal time constant of the power amplifier. The resultant power averaging between the output transistors results in a lower thermal resistance. This lower thermal resistance immediately increases the power handling capability of a given amplifier.

Apex data sheets provide both AC and DC ratings of thermal resistance. Power levels specified on both the absolute maximum rating and the power derating typical performance graphs are based on DC thermal resistance. This means an AC only application is capable of delivering more power or running cooler (more reliably).

Sine wave circuits share a similarity with DC circuits. Maximum internal RMS power dissipation occurs when the peak output voltage swings to 63.7% of supply voltage. Maximum internal power may be calculated as follows:

$$P = V_{SS}^2/(2\pi^2 * R_L)$$

Where: V_{SS} = total rail-to-rail supply voltage
R_L = load resistance

REACTIVE LOADS INCREASE DISSIPATION

When driving reactive loads, more caution is required due to the phase difference between V_O and I_O. The actual power dissipation may be several times higher than the equivalent resistive loads. In such cases, It is best to use a totally different, but equally simple, approach to calculate power dissipation (P):

$$P = P_1 - P_O$$

Where: P_1 = Power drawn from the power supply
P_O = Real power delivered to the load

In calculating P_1, use DC supply voltage and RMS output current. For example, a 1A RMS output, with supplies of ±15V, means 15W plus quiescent current * 30V.

Driving purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier because the load power factor is reduced to zero.

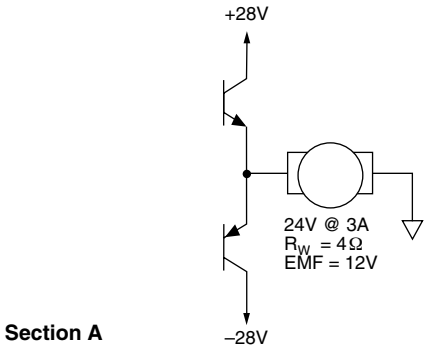
DEALING WITH MOTOR DRIVES

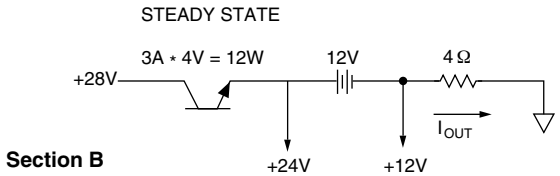
Motor control applications often place brutal requirements on the driving circuit. Section A of Figure 5 shows two output transistors of a power amplifier and the motor with its ratings. It is important to recognize that the winding resistance and the voltage rating of the motor alone do not determine the running current. The back EMF of the motor must also be considered when calculating the running current. This EMF can be modeled as a battery whose voltage is proportional to instantaneous velocity as shown in Section B of Figure 5.

When the amplifier is given a reversal command, it changes its output very quickly while the actual speed and EMF can diminish only as fast as mechanical system inertia is dissipated. The initial result of the vastly different response times between the electronics and the mechanics is shown in Section C of Figure 5. The amplifier has responded to its new drive command, but the EMF has not yet had time to change.

The model shows that if the amplifier could produce the programmed output level of –24V, a total of 36V would be applied across the winding resistance developing a current on 9A. In this situation, the output voltage is determined by the current limit of the amplifier rather than the control voltage. The programmed limit of 4A through the winding resistance produces 16V. Adding the initial 12V EMF places the amplifier output voltage at -4V. With 24V across the conducting transistor, the internal power dissipation is eight times the level encountered in steady state operation. Failure to analyze this situation has taken the lives of many power op amps.

A useful technique to maximize available power for steady state running requirements is to limit the rate of change of the drive voltage to approximately the same limitation imposed by the inertia of the mechanical system. In this manner, the extremely high power levels described can be avoided. In other words, fast reversal times can be traded off for high levels of running torque.





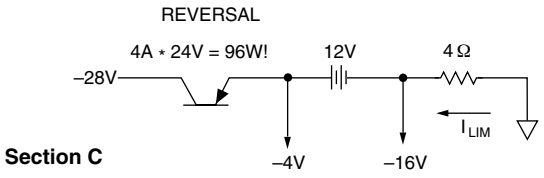


FIGURE 5. POWER DISSIPATION IN MOTOR DRIVES

CIRCUIT DESIGNS TO INCREASE OUTPUT POWER

Two power op amps configured in a bridge circuit can double power levels. To illustrate the advantages of the bridge circuit, Figure 6 shows a composite where alternate connections transform the circuit from single ended to a bridge. A1 is a standard single ended power op amp which would drive the 4 ohm speaker. If A2 is added, it completes a bridge circuit. The resulting doubling of the voltage drive would be suitable for an 8 ohm speaker. With this trick, not only are power levels doubled, but the same supply is capable of powering either circuit. This is possible because the single ended circuit peak current demand utilizes only 50% of the supply capability. In contrast, the equal and opposite drive characteristics of the bridge circuit loads both positive and negative supply rails equally during each half cycle of the signal.

Parallel operation is often used to increase output current or wattage. However, due to their low output impedance, power op amps cannot be connected in parallel without modifying the circuits. Figure 7 illustrates one method of doing this. This uncommitted *master* amplifier, configured as required to satisfy the circuit function, has a small sense resistor inside its feedback loop. The *slave* amplifier is a unity gain buffer. Thus, the output voltages of the two amplifiers are equal. If the two sense resistors connected to the load are equal, the amplifiers share current equally. More slaves may be added as desired.

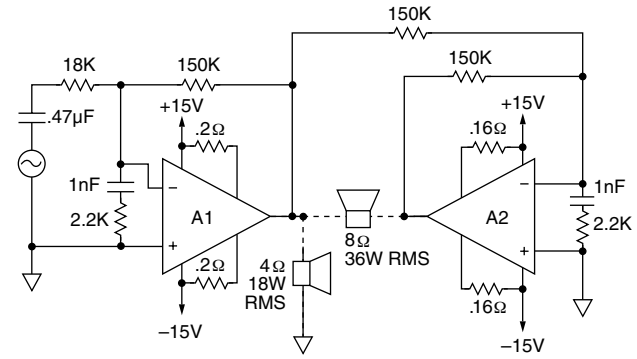


FIGURE 6. DOUBLING POWER WITH A BRIDGE

There are two factors to consider in the selection of the sense resistors. First, the output current will produce a voltage drop which adds to the supply requirements. Second, the voltage offset of the slave appears across the sum of the two sense resistors. Thus, a small current will circulate strictly between the two amplifiers. This wastes power. When this technique is used, it is recommended that inputs be limited in such a way that they demand only 50% of the typical slew rate of the amplifier. This prevents two amplifiers with different slew rates from generating large currents between each other during fast transitions.

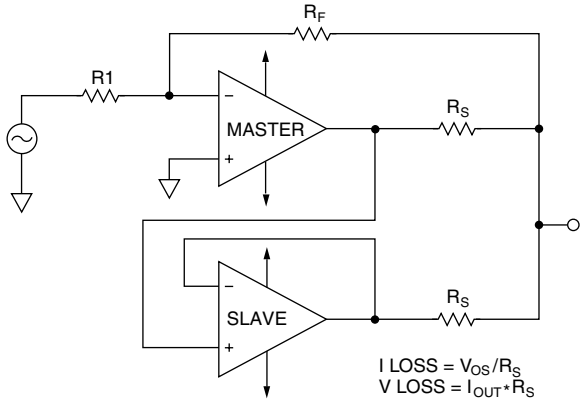


FIGURE 7. PARALLEL OPERATION

PROPER HEATSINKS INCREASE OUTPUT POWER

With a given power op amp, the larger the heatsink is, the higher attainable output power can be. Furthermore, as power levels increase, it is more cost effective to use a larger heatsink.

To minimize space and weight, forced air cooling or even liquid cooling is often used with power amplifiers. While obviously easier to implement, forced air cooling gives a maximum improvement of only about 2:1. At higher power levels, liquid cooling becomes a more attractive option. Reasonable heatsink ratings, which can be achieved given an area 6 inches square and 2 inches tall, are 0.85°C per watt for free air cooling, 0.4°C per watt for forced air, and 0.05°C per watt for a liquid cooled system. See the Apex application note on heatsinking for more information.

THERMAL SHUTDOWN CAN HELP

Internal thermal protection can increase output power under nominal operating conditions because the amplifier shuts off when the substrate temperature exceeds safe limits. This allows the amplifier circuit design to be based solely on normal conditions but prevents excessive temperature during abnormally high power conditions.

The thermal shutdown feature is especially valuable in circuits such as programmable power supplies (PPS). Here the output voltage is the normal operating voltage of the unit under test. Occasionally the unit under test will be defective which may short the output of the PPS to ground; thus, power levels increase substantially. Thermal shutdown will simply shut the device off rather than lead to destruction. Thermal shutdown is not a panacea for all problems. It does not mean to disregard the second breakdown curves of the safe operating area. Assume the time constant for operation of the thermal shutdown is 250-500ms. This means the worst case power levels should not exceed the steady state second breakdown line of the SOA curve.

OPTIMIZING IS A TEAM EFFORT

Apex power op amps employ unique thermistor circuits that provide superior control of internal currents and offer exceptional specifications plus a superb quality record. With careful attention to design of the application, the end result will be advanced products of greater value.

INTRODUCTION

Power op amp circuits without suitable current limiting can be compared to putting a gun in the hands of a child – you may get away with it but disaster is waiting to strike. While elaborate circuits have been used, most power op amps use a simple and cost effective circuit which still requires engineering homework to be safe. The objective is delivering desired power to the load without violating the SOA.

BASIC CURRENT LIMITING

Current limiting circuits in power op amps are local to only the output stage so they can very quickly (sub microsecond) reduce output current to a predetermined level. There are at least four reasons to incorporate such a limit:

1. The output transistors of the amplifiers are almost always capable of delivering more current than the ABSOLUTE MAXIMUM RATING of the amplifier. Exceeding this limit can destroy metal, usually a wire bond to the supply or the output pin fuses. A common mistake is to rely on the power supply current limit for this protection. Do NOT fall into this trap. Filter capacitors (both inside the supply and local to the op amp) often store plenty of energy to vaporize a wire bond.
2. Loads with variable impedance may need protection against possible fault conditions. A mechanical jam on a motor drive is a good example.
3. Current limit can prevent overloading power supplies. This may be critical if other circuits share the same supply.
4. Observing the Safe Operating Area (SOA) of the power amplifier keeps junction temperatures to a reasonable level. Output current is one term of the power equation.

A fixed current limit is usually adequate for the first three reasons. A simple and cost effective approach to current limiting is shown in Figure 1. Current through the output transistor Q1 is converted to a voltage by the sense resistor Rcl. When this voltage exceeds the Vbe of the current limit transistor Q2, drive current from the preceding stage is diverted to the output to shut down Q1. In addition to being an amplifier, Q2 serves as an imperfect voltage reference for the current limit set point. At room temperature the typical value is around 0.65V. Rb along with the capacitance of Q2 slow the circuit just enough to prevent oscillation. In equation form:

$$Icl = 0.65/Rcl \quad (1)$$

or

$$Rcl = 0.65/Icl \quad (2)$$

where Icl is the current limit in amperes and Rcl is the current limit resistor in ohms.

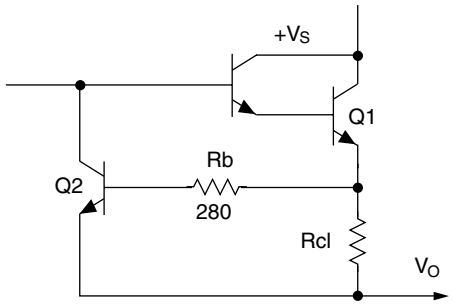


FIGURE 1. CLASSIC CURRENT LIMIT CIRCUIT

The fourth reason is more complex. Figures 2 and 3 illustrate the challenge of meeting SOA limitations with fixed current limit. First, note that the X axis labeling of the PA10 SOA graph is NOT output voltage but the stress voltage across the conducting transistor. Assume DC signals and a case temperature of 25°C for the following. The resistive load implies stress voltage is limited to single supply voltage and that maximum heat in the output transistor occurs at an output of 50% of supply. At 25V the SOA graph tells us maximum current is 2.7A. This implies a minimum load of about 9.3 ohms will limit current to safe levels at any output voltage. Maximum current will be 4.75A (44V/9.3 ohms) and maximum output power will be 209W. Note: The voltage swing specification of the PA10A is Vs-6V at 5A. However, if the application must survive a shorted component or cable on the output, the stress voltage jumps to 50 and maximum safe current is only 1.05A. Once this current limit is set output power is limited to 46W peak into 44 ohms. For energy storing loads, assume an initial voltage of nearly -50V and a positive going signal. Initial supply to output stress is nearly 100V and maximum safe current is less than .3A.

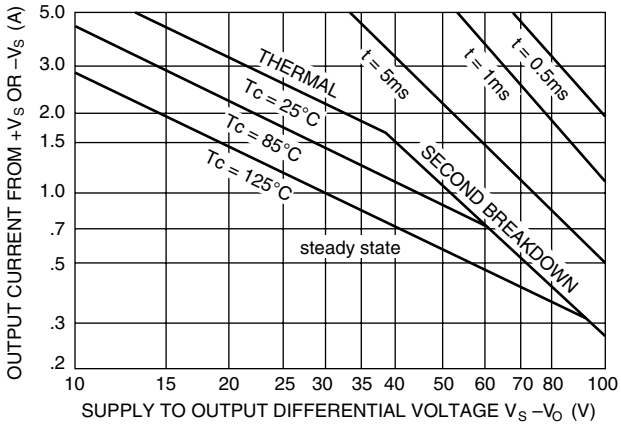


FIGURE 2. SOA GRAPH OF PA10

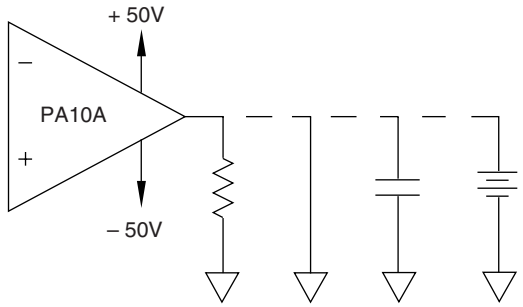


FIGURE 3. DIFFICULT LOADS OR POSSIBLE FAULT CONDITIONS

CURRENT LIMIT IS A MOVING TARGET

The largest variable of the current limit circuit is the temperature coefficient of the imperfect reference voltage, the Vbe of Q2. It decreases approximately 2.2mV for each degree C increase in case temperature. Thus the 0.65 term ranges from 0.826 at -55°C to 0.43 at 125°C. From an steady state power dissipation point of view, this slope is in the right direction but it is still possible to get in trouble. Comparing this slope to our initial reasons to limit current:

1. The reason does not vary with temperature.
2. The reason is load dependent.
3. The reason is supply dependent.
4. The reason does not vary with temperature.

It is best to plot the limit on the SOA graph and compare to other requirements of the system. To this end, visit the Apex web site at www.apexmicrotech.com or contact Apex applications engineering for software to automate the task.

Looking again at Figure 1, we can find several reasons actual current limit varies from the equations presented. When in the limiting mode, Q2 is shunting drive stage current away from Q1 directly to the output. This means actual current limit can not be less than drive stage capability. Some data sheets give a minimum practical current limit. Operation in this region is unusual because drive stage current is so much less than output capability that being in this region implies amplifier capability is likely an overkill for the application.

Now consider that when Q2 is conducting there will be base current flowing through Rb which effectively increases the reference voltage. On some amplifiers this effect is large enough that the specific data sheet will give a unique value greater than 0.65 to use in the equations.

Although it is not immediately obvious looking at figure 1, resistance of internal wire bonds, solder joints, wiring traces and the leads of Rcl all add to the rated value of Rcl unless pins are provided to implement four wire current sensing. In high current applications, measurements of prototype circuits may be the best way to finalize the design.

We now have a very wide range of "safe" currents depending on loads or fault conditions which must be tolerated. We have also seen that while simple and cost effective, these limiting circuits are not reference standards; think in the area of +/-20%. The sad part is that the fixed current limit set to protect for worst case fault condition also limits current for the non-fault condition. It is also interesting to note that we assumed an unrealistic heatsink and safe currents are still only a fraction of the absolute maximum for the amplifier. This shows the importance of both heatsinking and current limiting. An ideal solution for SOA protection might be the addition of a stress voltage sensor and multiplier for each output transistor such that limiting could be based on watts. If all this circuitry is fast enough, SOA concerns would be no more. This approach is quite rare because the cost measured in components, design time and space is almost always more than that of using a larger amplifier. Clearly, an affordable improvement in current limit technique is called for.

FOLDOVER CURRENT LIMIT BASICS

Apex models PA04, PA05, PA10 and PA12 can take advantage of foldover current limiting. Adding only one resistor to the classic current limiting circuit (Figure 4) provides dynamic response to output voltage swing. Realizing that Rcl is typically three orders of magnitude below Rb, it is reasonable to ignore Rcl and say Rb and Rfo form a voltage divider between ground and the output voltage. With Rfo typically being a couple orders of magnitude larger than Rb, the divider adds a very small portion of the output voltage in series with the base of Q2. With a 0V output, current limit will be the same as the classic circuit. However, as the output goes positive, the addition of the divider voltage effectively increases the reference voltage (Vbe of Q2) allowing more current to flow. For negative output voltages (Q1 is still conducting), the very small fraction of the negative output added reduces current flow. Another way to view this would be state we have added a term to the current limit equation based on output voltage but modifying current limit in an inversely proportional manner to voltage stress on the conducting transistor. While this is still a long way from the ideal of a multiplier calculating watts, and it does nothing in the case of variable supplies, it does add a desirable slope to the current limit function. In equation form:

$$I_{CL} = \frac{0.65 + V_O * \left(\frac{Rb}{R_{FO} + R_B}\right)}{R_{CL}} \quad (3)$$

$$R_{CL} = \frac{0.65 + V_O * \left(\frac{Rb}{R_{FO} + R_B}\right)}{I_{CL}} \quad (4)$$

where Vo is output voltage in volts and resistors are from Figure 4 and in ohms.

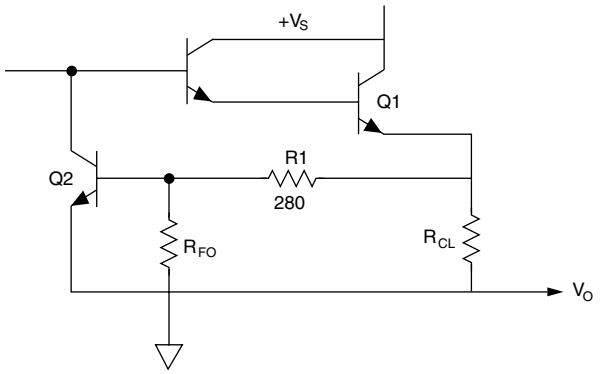


FIGURE 4. BASIC FOLDOVER CURRENT LIMIT CIRCUIT

Looking again at the case of the resistive load driver which must tolerate a short on the output, let us further assume the objective is to drive 22 ohms to 88W peak (44Wrms, 44V pk and 2A pk). Start with an Rb of 280 ohms and Rfo of 20Kohms and use Equation 4 to calculate Rcl = 0.629 ohms for peak current at peak voltage. Use a 0.62 ohm resistor. Equation 1 now shows us current during the short fault condition is limited to 1.05A. Plotting the current limit on the SOA graph as shown in Figure 5 reveals that this current limit is safe for any output voltage from zero to supply. Using foldover instead of fixed current limit has nearly doubled the power delivery capability.

In the case of the energy storing load, Equation 3 shows us this foldover circuit current limit crosses zero and turns negative within the swing capability of the amplifier at all temperatures above 25°C. This can cause amplifier latch-up and MUST be avoided. A lower supply voltage or a larger foldover resistor will solve this problem.

Even though we know the current limit is safe for a short to ground and for the full 100V stress level, Figure 5 shows that at 25°C and colder allowable current crosses above the SOA line in between these points. Increasing Rcl will lower current limit at all output voltages and solve this problem.

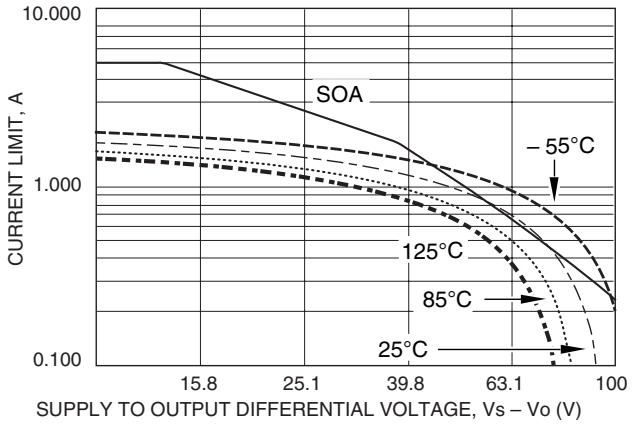


FIGURE 5. FOLDOVER ILIMIT VS. VOUT

TWO TYPES OF FOLDOVER

The PA10 and PA12 have an internal Rb of 280 ohms and internal Rfo of 20K for both the positive and negative current limit transistors. The two 20K resistors tie together at pin 7 where the user may ground the pin for maximum foldover slope or add an additional resistor in series from pin 7 to ground for less foldover action. Since both 280 ohm resistors tie essentially to Vo and the two series networks of 0.28K + 20K are essentially in parallel, the equations specific to the PA10 and PA12 are more complex than the previous example:

$$I_{CL} = \frac{\left|0.65 + V_O\right| * \left(\frac{10.14}{10.14 + R_{FO}}\right) * \left(\frac{.28}{20.28}\right)}{R_{CL}} \quad (5)$$

$$R_{CL} = \frac{\left|0.65 + V_O\right| * \left(\frac{10.14}{10.14 + R_{FO}}\right) * \left(\frac{.28}{20.28}\right)}{I_{CL}} \quad (6)$$

where Icl is in amperes, Vo is in volts Rcl is in ohms and Rfo is the PA10 or PA12 external foldover resistor and is in Kohms.

Foldover connections for the PA04 or PA05 are shown in Figure 6. Use 270 ohms for Rb and use equations 3 and 4. Beware that even momentary shorts directly at pin 10 can destroy the amplifier now that pin 10 is isolated from the output by the 270 ohms.

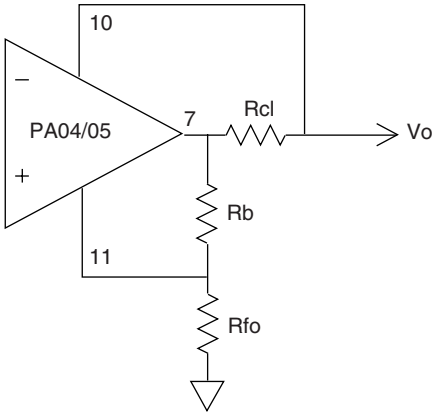


FIGURE 6. FOLDOVER CIRCUIT FOR PA04 OR PA05

CONCLUSION

Current limit is to the power op amp as survival instinct is to an animal; a REALLY good thing to have. While basic current limiting is simple, adding temperature variations and circuit options such as foldover make the job of checking all the points of possible danger quite a chore. First comes the math, then data plotting on the SOA graph with those log scales we all love so well. This drudgery has become history with the spreadsheet automation. Get your copy from the Apex web site at www.apexmicrotech.com or call Apex applications.

APPLICATION NOTE 10

INTRODUCTION

In the design of power amp circuits, the need often arises for a power amp model with specified output impedance. Most often, this requirement revolves around the need to accurately predict the phase performance of power amp circuits.

Output impedance of any op amp is modified by the feedback network present around the device. In voltage source type circuits, the effect of the network is to reduce the output impedance by a factor equal to the ratio of open loop gain to closed loop gain. In power amps, the net result is an effective output impedance of milliohm levels at frequencies below 1kHz. Wiring and interconnections often create larger impedances than the output impedance of the closed loop power amp. Therefore, output impedance will play a minor role in the phase performance at low frequencies. At high frequencies, reactive load considerations are already addressed by capacitive load specifications given on many power amplifiers.

Current control circuits, or current sources, include the load as a series element in the feedback loop with a sense resistor developing a voltage proportional to load current. Figure 1 shows a generalized example of just such a circuit. The load often consists of an inductive element such as a deflection yoke which can have up to 90° of phase shift at higher frequencies. Totally accurate prediction of phase in the feedback loop might at first seem to involve the series equivalent of output impedance and yoke impedance. In reality, it's because the feedback the op amp is operating as a true current source with an impedance approaching infinity. A realistic approach to stabilizing the circuit merely involves an auxiliary feedback whose effect dominates before the combination of yoke feedback and amplifier phase approaches 180°. Output impedance is not necessary to determine stability.

It is also important to realize that output impedance of a power op amp is not related in any way to power delivery capability or internal losses. A model of a power amp with the output resistance in series with the output will develop inordinate losses which are not observed in real world op amps.

Output impedance is dependent on several variables such as frequency, loading and output level. Often, the impedance will rise at higher frequencies. A class C amplifier, such as PA51 or PA61, will exhibit higher impedances at lower levels due to bulk emitter resistance effects in the emitter follower outputs.

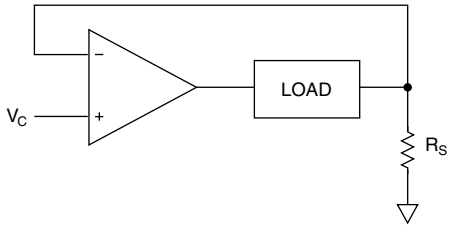


FIGURE 1. GENERALIZED CURRENT CONTROL CIRCUIT

OUTPUT IMPEDANCE MEASUREMENT

Several methods are available to measure output impedance. The simplest method is to measure open loop gain in loaded and unloaded conditions. This method measures the dynamic impedance in series with a perfect voltage source. Variations in output with loading are due to this impedance.

A more direct method is to generate a signal which is impressed into the output of an amplifier operating under open loop conditions. A measurement of current will determine the effective impedance that this signal is looking into.

ACTUAL IMPEDANCE VALUES

Several Apex power amplifiers were measured using the gain variation with loading method. The test circuit of Figure 2 was loaded with 10 ohms. To establish uniformity of measurement, the smallest possible amplitude at 10Hz was used. Where a range of values is shown, it represents a range observed for several devices.

PA02: 10-15 ohms
PA07: 1.5-3 ohms
PA08: 1500-1900 ohms (high voltage amplifier)
PA09: 15-19 ohms
PA10: 2.5-8 ohms
PA12: 2.5-8 ohms
PA19: 30-40 ohms
PA51: 1.5-8 ohms
PA61: 1.5-8 ohms
PA84: 1400-1800 ohms (high voltage amplifier)

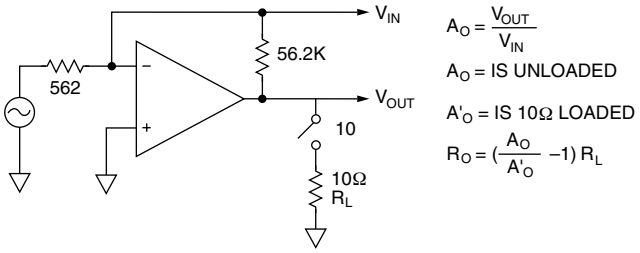


FIGURE 2. OUTPUT IMPEDANCE MEASUREMENT CIRCUIT

The high voltage amplifiers are much lower in current capability than the high current amplifiers. As a result, the higher impedance is to be expected.

The high impedance shown for PA19 is a result of the drain output MOSFET circuit without local feedback at the output stage. This is an example of how this parameter can be misleading. If 30 to 40 ohms of resistance were in series with the output, then the PA19 would never be capable of greater than 1 amp of output current. Under closed loop conditions, the output impedance is reduced to milliohm levels like any other power amplifier. Keep in mind the output impedance is an abstract term as far as output voltage and current capability are concerned.

To demonstrate the effect of output impedance when modeling, use the highest and lowest expected values. The results will verify that output impedance plays an insignificant role in power amp performance.

APPLICATION NOTE 11

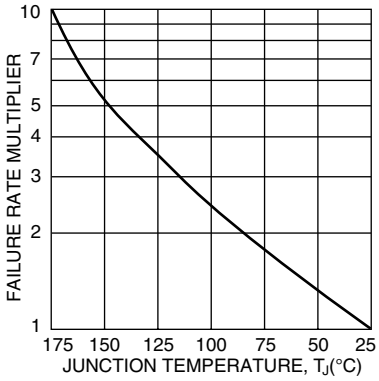
POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

THERMAL MANAGEMENT

As power op amps shrink in size and become more powerful, the importance of a good thermal design is more critical than ever. Most importantly, reliability is a direct function of internal component temperatures and dissipated power. Furthermore, as the amplifier case rises above 25°C, derating factors do not just reduce the allowable power level. Voltage and current offsets drift, current limits change and, sometimes even dynamic performance is affected. This application note discusses thermal management starting with actual dissipation vs. allowable dissipation, the common cooling options, how to achieve maximum performance with sound mounting techniques, as well as the benefits of thermal capacity.

Thermal management techniques must be applied to remove as much heat as possible from the semiconductor junction, thereby maintaining minimum operating temperatures and maximum reliability. A further goal is to minimize the effects of the removed heat on other devices. Figure 1 shows the average of NPN and PNP power transistor failure rates at elevated temperatures relative to operation at 25°C. All electronic components encounter similar increased failure rates.



This data was extracted from the base failure rate tables of MIL-HDBK-217C, revision of 1 May 1980.

FIGURE 1. MTTF VS. TEMPERATURE

MAXIMUM POWER RATING

$\theta_{JC}$is the thermal resistance from junction to case. A great deal of effort has been put into minimizing this thermal resistance. It is the major specification affecting power handling capability. When allowing for a case temperature of 25°C and maximum junction temperature, the maximum internal dissipation rating is developed.

$$P_{MAX} = (T_{JMAX} — 25°C) / \theta_{JC} \quad (1)$$

This rating is consistent with rating methods of most transistor manufacturers and should not be confused with advertised output power which is highly application dependent. Before using this rating, check for factors which might degrade the rating such as actual ambient temperature (T_R), heatsink thermal resistance (θ_{HS}) mounting, and in some cases, an isolation washer.

The optimum heatsink to case thermal resistance (θ_{HSC}) for a TO-3, using thermal grease and a mica isolation washer, is 0.375°C/watt. With thermal grease only or with the Apex TW03 washer, this is reduced to 0.2°C/W. Several references cite 0.1°C/W for a TO-3, but this data is for transistors with only two leads. With eight holes and insulating glass restricting heat flow outside the pin circle, design with the higher number. Allow 0.1°C/W for the MO-127 package. APEX amplifiers have an isolated case which negates the need for isolating the mounting surface and the mounting screws. Some vendors require isolation washers.

$$P_{MAX} = (T_{JMAX} — T_A)/(\theta_{JC} + \theta_{HS} + \theta_{HSC}) \quad (2)$$

To illustrate the importance of analyzing θ_{JC}, rather than using advertised ratings, Table 1 compares a 150W (output) rated amplifier (non-isolated) to the APEX PA12 rated at 125W (dissipation). For a stipulated audio application, the thermal resistance used is the typical AC rating and the power level is 100W for both devices. The table shows the 150W (output) device junction rises nearly twice as much resulting in questionable reliability at just 100W. An ideal ambient temperature and infinite heatsink are assumed.

	150W Output	125W Dissipation
θ_{JC}	1.6	.8
θ_{CS}	.375	.2
Delta T_C	37.5	20
Delta T_J	197.5	100

TABLE 1. COMPARING TEMPERATURE RISE

SYSTEM LAYOUT

Thermal management starts with determination of actual dissipation and should result in a layout of an optimized thermal system to convey the heat to the ambient environment. In systems using natural convection, heat sources should be separated as widely as possible. In contrast, systems using high velocity air or liquid cooling perform optimally when localizing these devices. Understanding convection and radiation may help avoid layout related problems. Since convected heat rises, it is best to place the heat sources near the top of the enclosure and avoid having temperature sensitive circuits above or near the heat sources. The hot air should flow in its natural vertical direction using vertical board and fin orientation. Heatsinks should be oriented so air can pass freely over all the fins.

MOUNTING THE AMPLIFIER

The thermal joint from the case to heat sink, θ_{HSC}, is very important from both design and production points of view. Extreme care must be taken in this small but critical area. Heat generation occurs near the top of the silicon chip and typically spreads downward at an angle of 45° as it travels through the various materials to the heatsink. The 8 pins of the package surround the heat source. Unfortunately, the glass seals present a high thermal resistance to heat flow toward the outer edges of the package. To maintain optimum heat flow, heatsink material should never be removed from the inside of the pin circle. For example, drilling one large hole rather than eight small holes to mount an amplifier will increase thermal resistance dramatically.

Figure 2 illustrates a common mounting setup employing direct wiring, using cage jacks and mating sockets. A consistent and stable thermal joint vs. time, including temperature cycling, is an absolute must. Compression washers will help to accomplish this. The washers have a spring-like quality that maintains a constant pressure over temperature. Steel screws should be torqued from 4 to 7 inch-pounds. If the assembly process includes a flow or wave solder step after the device has been mounted and torqued down, re-torquing is required. Torque control is one of the least expensive but more effective ways to maintain the thermal resistance over time.

There are a number of thermal compounds that have been successfully used for years to fill tiny gaps between cases and heatsinks. Most of these products work well, but a word of caution is in order. The shelf life for most thermal greases is indefinite when sealed in its container, but the vehicle and the thermally conductive part may separate. If the separated material is used, the resultant joint will have poor thermal properties. Mixing the components back into solution restores the material's thermal properties. To make the re-combination easier, it is best to purchase the grease in a jar instead of the more common tube. In one year, life tests at 100°C with compression washers, the thermal joint did not degrade. However, this vehicle evaporated leaving a dry joint. This does not degrade the thermal resistance provided the joint is not loosened.

For the heatsink, a vast array of devices are available. The proper match of heatsink to actual power dissipation, in accordance with "Heatsink" in "General Operating Considerations" section, will main-

tain a safe junction temperature and determine whether the circuit is "indestructible" or has unpredictable failures. Please note that altitude, air pressure, flow rate, and power level all have a major influence on heatsink efficiency. Also, a word of caution: forced air heatsink ratings are usually functions of linear feet per minute (FPM) or air flow, while fan ratings are usually given in cubic feet per minute (CFM). For example, a four inch diameter fan at 50 CFM pushes that volume through only 0.087ft^2 producing 573 FPM at the fan. Also keep in mind that if you reduce the airflow cross section below that of the fan, you must consult its static pressure curves.

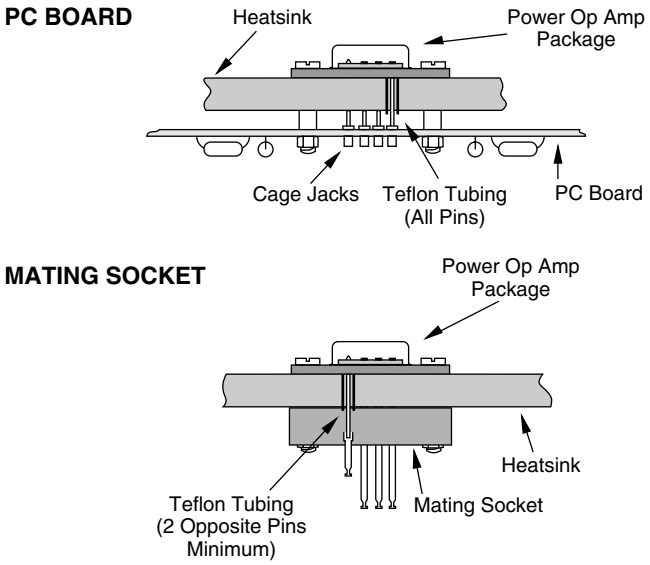


FIGURE 2. MOUNTING TECHNIQUES (CROSS SECTION VIEWS)

When utilizing structural elements to dissipate heat, it is advisable to check the proposed mounting area. Surfaces must be flat and have a smooth finish. The extrusion flatness of 4mils/inch and a surface finish of 63 micro inches are typical of commercial heatsinks. This is perfectly acceptable in applications using TO-3 packages where heatsink compound is used and results in a θ_{HSC} of 0.2°C/W as noted under power rating. For high power applications or packages larger than the TO-3, a surface flatness of 1 mil/inch is recommended.

THERMAL CAPACITY

The power levels that can be achieved in the pulse mode of operation are elevated far above those of steady state operation. This is due to the thermal capacity of the heatsink. As heat is first applied, the rate at which the case temperature increases can be compared to its electrical equivalent, the voltage build up on a capacitor of a R-C network. Figure 3 displays this analogy.

The thermal capacity of a mass is the product of its density, specific heat and volume. In most tables, the density is given in gm/cm^3(multiplied by 16.39 to yield gm/in^3). The specific heat is usually in units cal/cm–°C. To obtain the more familiar units of watts-sec/°C, convert by multiplying by 4.1819. The thermal time constant (Tau) is equal to the product of thermal resistance and the thermal capacitance. This time constant defines the rate at which the material reaches thermal equilibrium. The time required to achieve 95% of the equilibrium temperature is 3 times the thermal time constant.

To illustrate the principle, aluminum has a density of 2.7gm/cm^3(44.245gm/in$_3$), and specific heat of .220cal/gm–°C, yielding 9.734cal/°C or 40.71 watt-second/°C per cubic inch. Using the conversion factor of 10.22 cubic inches per pound, and the Apex HS05 heatsink weight of 1.04 pounds, results in a volume of 10.63 cubic inches and a thermal capacity of 434 watt-second/°C. The time constant for this heatsink is the thermal resistance of 1.1°C/W x 434 watt-second/°C, or approximately 346 seconds. The thermal resistance rating used above is for a free air mounting only because application of forced air reduces both thermal resistance and thermal time constant. Thermal capacity remains constant.

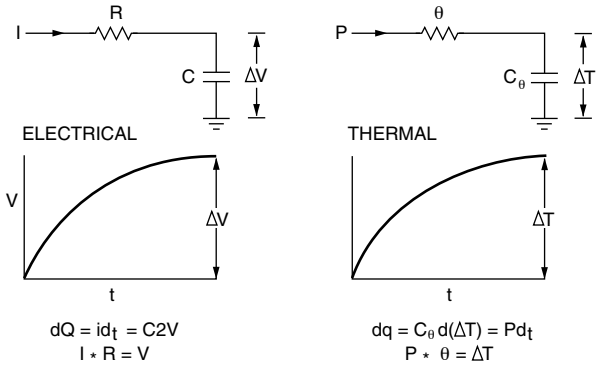


FIGURE 3. ELECTRICAL AND THERMAL MODELS

If power is applied as a single pulse, the case temperature follows the curve in Figure 4. The delta T in °C for both heating and cooling follow these equations :

$$\text{delta } T_{HEAT} = W*\theta_{HS}\,(1-e^{-t/tau}) \quad (3)$$

$$\text{delta } T_{COOL} = \text{delta } T_{HEAT}(e^{-t/tau}) \quad (4)$$

The Figure 4 curve indicates that thermal capacity plays a major role when the duty cycle is extremely low.

Figure 5 shows the initial response to application of repetitive pulses. The pulse train is repetitive when the duty cycle does not allow the circuit to return to its initial temperature between pulses. The following procedure will predict operating temperatures after the heatsink has reached equilibrium. Peak power is multiplied by duty

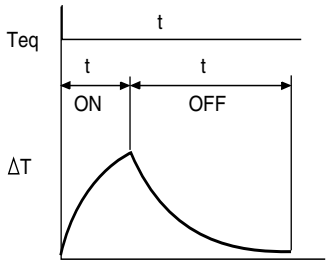


FIGURE 4. SINGLE PULSE RESPONSE

cycle to arrive at average power. The average temperature of the case will be $T_A + (P_{AVERAGE} * \theta_{HS})$. To determine the peak power, the pulse duration and time constant are substituted into equation 3 above. Then 1/2 delta heating is added to average temperature to yield the maximum case temperature. This case temperature should be used in conjunction with the SOA curves to determine the maximum power available from the device.

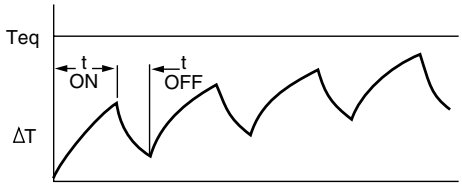


FIGURE 5. REPETITIVE PULSE RESPONSE

CONCLUSION

Thermal management optimizes space, cost and size for your power levels and temperature range. When properly applied, it will get the heat out and keep your circuits cool; thereby, maintaining the highest possible reliability and performance.

VOLTAGE TO CURRENT CONVERSION

Voltage controlled current sources (or VCCS's) can be useful for applications such as active loads for use in component testing or torque control for motors. Torque control is simplified since torque is a direct function of current in a motor. Current drive in servo loops reduces the phase lag due to motor inductance and simplifies stabilizing of the loop.

VCCS's using power op amps will assume one of two basic forms, depending on whether or not the load needs to be grounded.

CURRENT SOURCE: FLOATING LOAD

Figure 1A illustrates the basic circuit of a VCCS for a floating load. The load is actually in the feedback path. R_S is a current sense resistor that develops a voltage proportional to load current.

Note the inclusion of resistor R_B in Figure 1A and subsequent figures where non-inverting VCCS's are described. This resistor is present to prevent the non-inverting input from floating when the input voltage source is disconnected or goes to high impedance during the power on cycle. R_B provides a path for input bias current of the amplifier and commands the amplifier output current to zero in cases where V_{IN} is disconnected or goes to a high impedance. Figure 1B shows an implementation of a VCCS for a floating load. At low frequencies the added components Cf, Rd, and R_F have no effect and are included only to insure stability. Considerations for these components are discussed in the section on "Stabilizing the Floating Load VCCS" covered later in this application note.

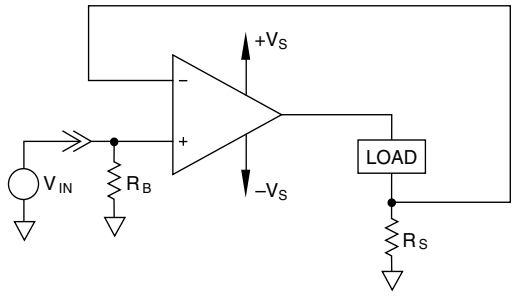


FIGURE 1A. BASIC VCCS FOR FLOATING LOAD

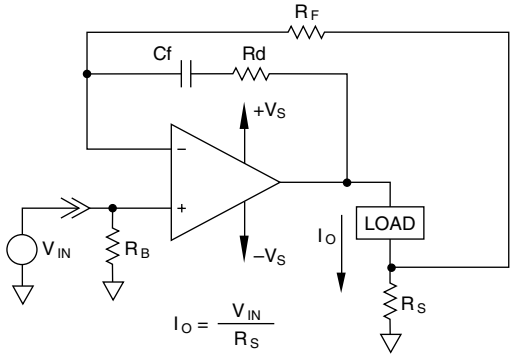


FIGURE 1B. VCCS FOR FLOATING LOAD WITH STABILITY COMPENSATION

The amplifier's loop gain will force the voltage across R_S to assume a value equal to the voltage applied to the non-inverting input, resulting in a transfer function of:

$$I_O = V_{IN}/R_S$$

Several variations are possible for this basic circuit. It is not necessary to have a direct feedback connection from R_S to the inverting input; components can be included to raise the gain of the circuit. Figure 2 shows a higher gain version with its equivalent transfer function. Higher gain circuits will lose some accuracy and bandwidth, but can be easier to stabilize.

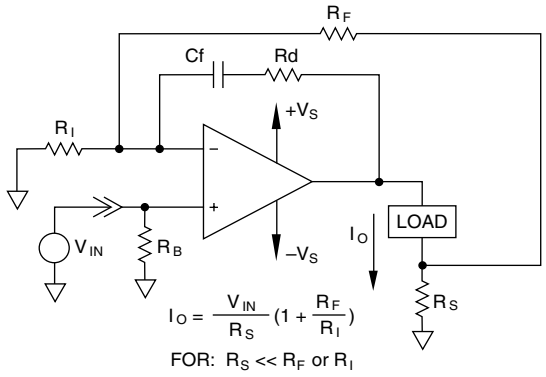


FIGURE 2. VCCS FOR FLOATING LOAD; INCREASED GAIN CONFIGURATION

Figure 3 shows an inverting VCCS. The input voltage results in an opposite polarity of current output. Just as in the case of inverting voltage amplifiers, the advantage of not having any common mode variation at the amplifier input is higher accuracy and lower distortion.

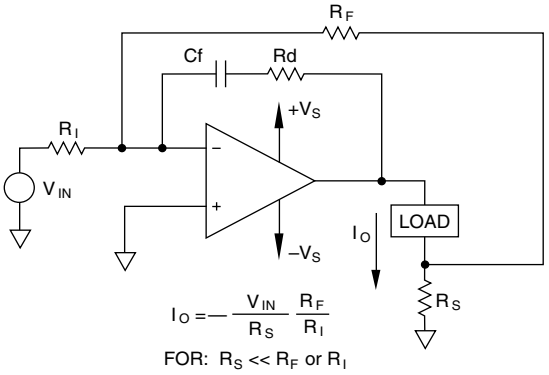


FIGURE 3. VCCS FOR FLOATING LOAD; INVERTING CONFIGURATION

Figure 4 is a current input version which is actually a CCCS, or current controlled current source. This is truly a current amplifier. This circuit could be useful with current output Digital-to-Analog Converters (DAC's), or in any application where a current is available as an input.

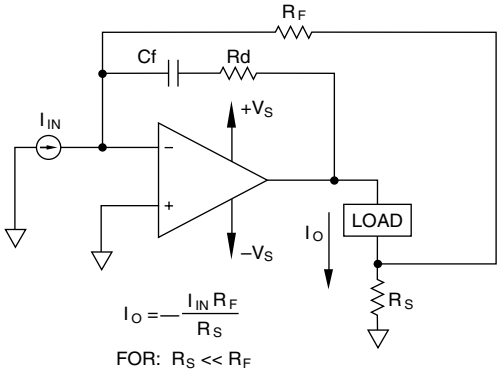


FIGURE 4. CCCS FOR FLOATING LOAD; INVERTING CONFIGURATION

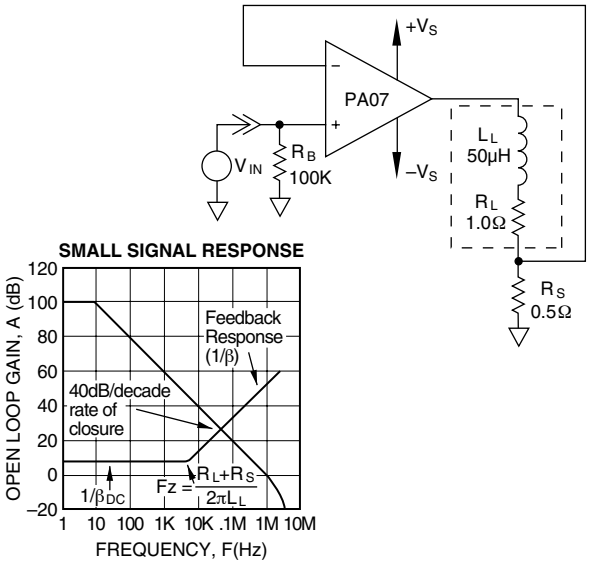
STABILIZING THE FLOATING LOAD VCCS

Because the load is in the feedback loop on all of these circuits, it will have a significant effect on stability. If the load was always purely resistive, the analysis would be simple and many circuits would not require any additional components (such as Cf and Rd) to insure stability. In the real world however, we usually find ourselves using these circuits to drive such complex loads as magnetic coils and motors.

Stability analysis is most easily accomplished using **"Rate of Closure"** techniques where the response of the the feedback is plotted against the amplifier open loop gain. This technique uses information easily obtained on any amplifier data sheet.

Rate-of-closure refers to how the response of the feedback and amplifier Aol intersect. If the slope of the combined intersection is not over 20 dB per decade, the circuit will be stable.

For an example, consider the amplifier of Figure 1A. Assume a PA07 amplifier with a 0.5 ohm current sense resistor will be used to drive a 50 μH coil with 1 ohm of series resistance. In Figure 5 we have superimposed on the Aol graph of the PA07 the response of the load and sense resistor.



$$\beta_{DC} = \frac{.5\Omega}{1.5\Omega} = .333 \rightarrow 1/\beta = 9.5dB \qquad Fz = \frac{1.0\Omega + .5\Omega}{2\pi\ 50\mu H} = 4.77kHz$$

FIGURE 5. PLOTTING FEEDBACK RESPONSES

The intersection of the responses exhibits a combined slope of 40 dB per decade, leading to ringing or outright oscillation. Let's refer to that point as the **"critical intersection frequency."** Compensation for this circuit is best accomplished with an alternate feedback path; the response of which will dominate at the critical intersection frequency.

A good criteria for the response of the alternate feedback would be:

1. A response which dominates by at least an order of magnitude (20 dB) at the critical intersection frequency.
2. The alternate feedback response should have a corner occurring at a frequency an order of magnitude less than the critical intersection frequency.

To provide this response, the alternate feedback components have been selected to provide the compensating response illustrated in Figure 6. A_B in Figure 6 is the dominant feedback path the amplifier will see in its closed loop configuration. R_F merely acts as a ground leg return impedance for the alternate feedback loop, and should be a low value between 100 and 1000 ohms. Rd is then selected to provide the desired high frequency gain, and Cf is selected for the alternate feedback corner.

Note that these are similar to techniques used to stabilize magnetic deflection amplifiers described in Apex AN #5, **"Precision Magnetic Deflection."**

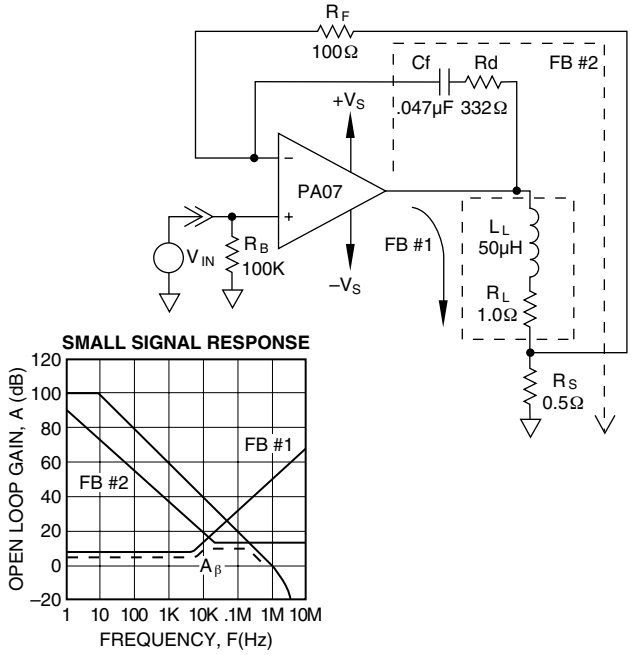


FIGURE 6. COMPENSATING THE AMPLIFIER

CURRENT OUTPUT FOR GROUNDED LOAD

The VCCS for a grounded load is sometimes referred to as the **"Improved Howland Current Pump."** It is actually a differential amplifier which senses both input signal and feedback differentially.

Figure 7 shows a general example for this VCCS with its associated transfer function .

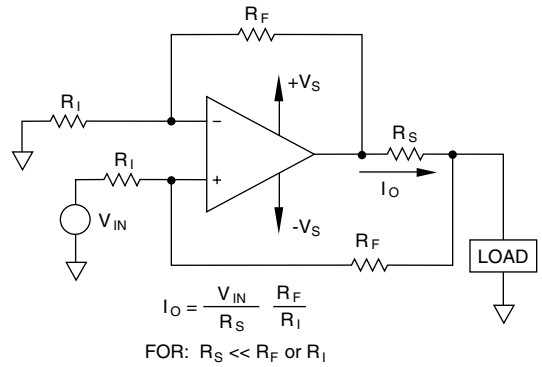


FIGURE 7. VCCS FOR A GROUNDED LOAD

First among the special considerations for this circuit is that the two input resistors (R_I), and the two feedback resistors (R_F), must be closely matched. Even slight mismatching will cause large errors in the transfer function and degrade the output impedance causing the circuit

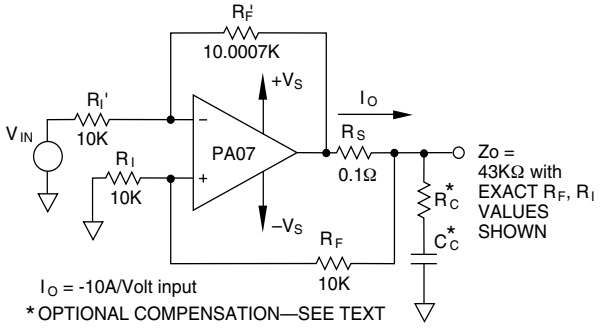


FIGURE 8. ACTUAL PA07 VCCS

to become less of a true current source.

As an example of the matching requirement, consider the actual example using PA07 in Figure 8. Matching the resistors as closely as tolerances permitted produced an output impedance of 43 K ohms. A 1% mismatch reduced output impedance to 200 ohms and introduced nearly 20% error into the transfer function.

This suggests that matching to better than 0.1% is required which is probably best accomplished with prepackaged resistor networks with excellent ratio match. The circuit of Figure 8 actually required a slight amount of mismatch in the two (R_F) resistors to compensate for mismatches elsewhere, suggesting that the inclusion of a trimpot may be necessary to obtain maximum performance.

STABILITY WITH THE GROUNDED LOAD CIRCUIT

The grounded load circuit is remarkably forgiving from a stability standpoint. Generally, no additional measures need to be taken to insure stability.

Any stability problems that do arise are likely to be a result of the output impedance of the circuit appearing capacitive. The equivalent capacitance can be expressed as follows:

$$Ceq = \frac{R_I + R_F}{2\pi fo R_I R_S}$$

Where: fo = THE GAIN-BANDWIDTH PRODUCT OF THE AMPLIFIER

This capacitance can resonate with inductive loads, resulting most often in ringing problems with rapid transitions. The only effective compensation is a simple **"Q-snubber"** technique: determine the resonant frequency of the inductive load and output capacitance of the circuit. Then, select a resistor value one-tenth the reactance of the inductor at the resonant frequency. Add a series capacitor with a reactance at the resonant frequency equal to one-tenth of the resistor value. An alternate method would be to put a small inductor and damping resistor in series with R_S.

Also keep in mind that the equation favors larger values of R_I and R_S, and the use of op amps with better gain-bandwidth to reduce effective capacitance. In circuits where good high frequency performance is required, this will necessitate increasing either or both R_I and R_S with the upper limits being established where stray capacitance and amplifier input capacitance become significant.

An infrequent second cause of instability in this circuit is due to negative resistance in the output impedance characteristic of the circuit. This problem can be solved by trimming the feedback resistors to improve matching.

THE CURRENT MIRROR

The current mirror circuit is a handy device for generating a second current that is proportional to input current but opposite in direction.

The mirror in Figure 9 must be driven from a true current source in order to have flexible voltage compliance at the input. Any input current will attempt to develop a drop across R1 which will be matched by the drop across R2 causing the current through R2 to be ratioed to that in R1. For example, if R1 were 1.0 K ohm and R2 were 1 ohm, then 1 mA of input current will produce 1 Amp of output current.

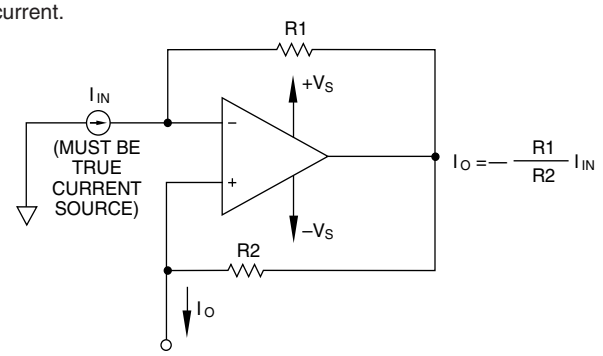


FIGURE 9. CURRENT MIRROR

APPENDIX A.

RATE-OF-CLOSURE AND FEEDBACK RESPONSE

Rate-of-closure stability analysis techniques are a method of plotting feedback response against amplifier response to determine stability.

The closed loop gain of any feedback amplifier is given by:

$$Acl = Aol/(1-\beta Aol)$$

Where: Aol IS THE OPEN-LOOP GAIN OF THE AMPLIFIER, AND Acl IS THE RESULTANT CLOSED LOOP GAIN

β is a term describing the attenuation from the output signal to the signal fed back to the input (see Figure 10). In other words, β is the ratio of voltage fed back to the amplifier over the amplifier's output voltage. (Vfeedback=βVout)

In the examples used in this application note, the plotting of β versus amplifier response is facilitated by plotting an equivalent closed loop response ($1/\beta$) of the amplifier circuit and superimposing this response on the amplifier open loop response. This **"equivalent closed loop response"** is also referred to as noise gain, Av (n).

In the example in Figure 5, the curve referred to as feedback response is actually representative of the closed loop noise gain response of the amplifier due to the feedback network consisting of yoke and sense resistor. In Figure 6, an additional feedback response for Cf, Rd, and R_F is plotted independently of all other responses. There are several important points to be noted in the use of these graphs:

1. In the case of multiple feedback networks such as in Figure 6, the response with the lowest noise gain at any given frequency will be the dominant feedback path. In Figure 6 this dominant feedback path is labelled A_β.
2. Whenever the noise gain and open loop gain intersect with a combined slope, or rate of closure, exceeding 20 dB/decade, poor stability will result. 40 dB/decade will definitely oscillate since this represents 180 degrees of phase shift. An example of this is shown in Figure 5.

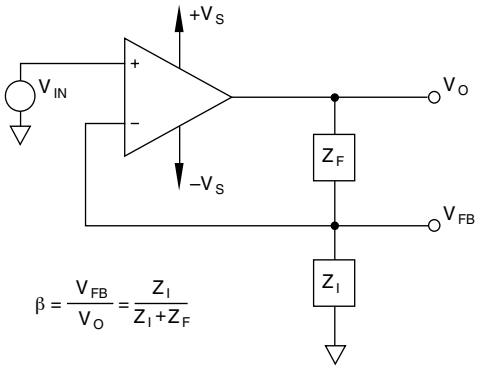


FIGURE 10. FEEDBACK FACTOR, β

APPLICATION NOTE 14

POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

The Apex PB series of power booster amplifiers, PB50 and PB58, are high performance, yet economical and flexible, solutions to a wide variety of applications. Their voltage and current ratings of up to 200 volts at 2 amps for the PB50, and 300 volts at 1.5 amps for the PB58, satisfy most high voltage and high current requirements. In addition, the PB series is fast. The 100 V/μs slew rate these boosters offer is matched or exceeded by only a few expensive power or high voltage op amps. If accuracy, in the form of low offset, drift, and/or bias current, is the system requirement, the PB series, with the proper choice of driver amplifier, can deliver high voltage performance with accuracy equal to the best small-signal op amps available on the market, and do it economically.

DESIGNING WITH BOOSTER AMPLIFIERS: BASIC CONNECTIONS

Power supply requirements for the PB50 dictate that the negative supply rail must be at least 30 Volts below the COMMON terminal (pin 5), setting the minimum supply voltage at +/-30 V. The PB58 can operate from supplies as low as +/-15 volts.

The INPUT terminal of the PB series devices is a low impedance input typically on the order of 50 KΩ. Maximum safe input voltage range must be limited to less than +/-15 volts. These power boosters will always have an offset of typically .75 volts as a result of the common base bipolar input stage. When used with a driver amplifier, this offset will subtract from the swing available from the driver. For example, a driver op amp that is required to swing 20 volts peak-to-peak will actually swing -10.75 and +9.25 volts. This offset has no effect on offset of the total driver and booster circuit since this offset is effectively reduced by the open loop gain of the driver amplifier. Remember that this offset will always be apparent when used without a driver amplifier.

The COMMON terminal provides a ground reference for the internal input and feedback circuitry. It might be noted that it is possible to use this "ground" terminal as an input; however, the PB series has not been characterized for such usage. The ground terminal would appear as a low impedance inverting input which must be driven from a low impedance source such as an op amp output.

The GAIN terminal allows the connection of additional resistance in series with the built-in feedback resistor of the PB series. The compensation capacitor connected to COMP, pin 8, is in parallel with the feedback resistor. Designers can predict the frequency response of the PB series amplifiers for any compensation by simply calculating the pole frequency of the parallel connection of feedback resistor, R_G, and compensation capacitor. The pole frequency is given by:

$$F_P = \frac{1}{2\pi(R_G+6.2K)C_C}$$

Where: R_G = EXTERNAL FEEDB ACK RESISTANCE
C_C = EXTERNAL COMPENSATION CAPACITOR

For example, a 22 pF compensation capacitor across the 6.2 K ohm feedback resistor results in a pole frequency of 1.2 MHz. This corresponds with the Closed Loop Small Signal Response graph on the PB50 data sheet. A gain of 10 will require placing a 22 K ohm resistor in series with the built-in 6.2 K ohm internal feedback for a total feedback resistance of approximately 28 K ohm. In this case a 22 pF compensation capacitor produces a rolloff at 260 kHz, again corresponding to the PB50 small signal response graph.

COMPOSITE AMPLIFIER STABILITY CONSIDERATIONS

The PB series data sheets provide 4 guidelines for insuring the stability of circuits designed with these boosters. Use of these guidelines can be complemented by the use of standard techniques such as plotting the overall gain response of the driver/booster combination and superimposing the feedback network response.

An example for determining the Aol (open loop gain) response of the composite amplifier is illustrated in Figure 1. At any given point on the frequency response, the overall gain is the sum of the gains (in dB) of the two amplifiers.

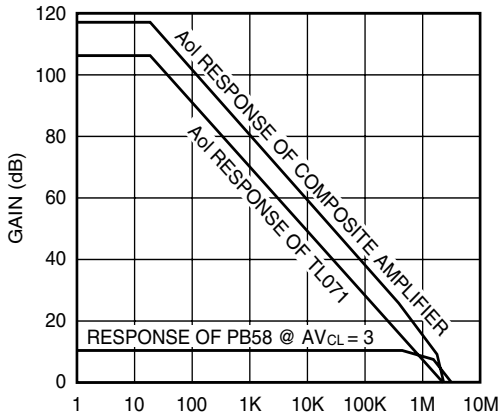


FIGURE 1. PLOTTING Aol FOR THE COMPOSITE AMPLIFIER

Figure 2 shows an example of such a plot for the deflection amplifier described in this application note. As a general rule, the intersection of the feedback response and open loop response should equate to a slope of no greater than 20 dB/decade to insure stability.

The particular deflection amplifier described in this application note is a testament to the ease with which the PB series devices can be designed into circuits where stability is usually a problem. The magnetic deflection circuit, which is a current source with an inductive load inside the feedback loop, is inherently unstable. The composite amplifier responded quite well to standard techniques used to stabilize deflection amplifiers (see AN #5, **"Precision Magnetic Deflection"**) and presented no special stability problems.

The designer who may be apprehensive about using a booster (buffer with gain) need have no reservations when using PB50 or PB58.

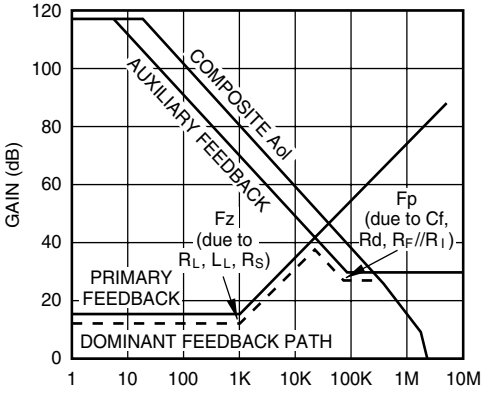
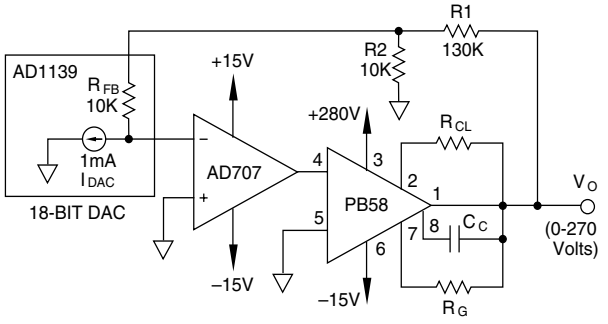


FIGURE 2. DEFLECTION AMPLIFIER FEEDBACK (I/β)

APPLICATION EXAMPLES: PROGRAMMABLE POWER SUPPLIES

The programmable power supply (PPS) application is useful to demonstrate the versatility of the PB series boosters. Along with the need to supply high voltages and currents, programmable power supplies often need high accuracy and low drift, while at other times they may need to be fast-responding. The PB series allows the

designer to optimize the circuit for these choices. Figure 3 is an example of a high accuracy PPS. An AD707 is selected as the driver amplifier to provide the extremely low offset required to obtain best possible performance from a high accuracy 18-bit DAC. The divider network on the output, R1 and R2, scale the output swing down to the full-scale range of the DAC. Accuracy will be affected by this divider, necessitating the use of high quality, low temperature coefficient (TC) resistors. If a packaged network can be used, then absolute TC is not nearly as important as TC ratio between R1 and R2. The use of this divider is preferable to the alternative technique of using an external DAC feedback resistor, since using the internal DAC feedback resistor insures the best possible temperature drift performance of the DAC itself. Most DAC's can exhibit up to 300 ppm/°C drift with external feedback resistors.



$$V_O = I_{DAC}\left\{\frac{R_{FB}\ R2 + R2\ R1 + R1\ R_{FB}}{R2}\right\} = I_{DAC}\ (270K)$$

FIGURE 3. HIGH ACCURACY PPS

APPLICATIONS AT LESS THAN FULL VOLTAGE AND CURRENT

The PB series do not have to be used at high voltages to realize all their performance benefits. Presently, only a few expensive IC power amplifiers can match these parts for slew rate and power bandwidth. Magnetic deflection applications require amplifiers with good speed performance at current levels often within those that the PB series can supply. While these applications don't always require high supply voltages, the high voltage capability of the PB series is useful when fast transitions are required with high inductance yokes, necessitating high supply voltages as a result of the yoke energy requirement:

$$V = L\ \frac{dI}{dt}$$

The basic techniques of magnetic deflection amplifier design are detailed in AN#5, **"Precision Magnetic Deflection."** Figure 4 is an example of these techniques put to use in the design of a magnetic deflection amplifier using the PB58. This circuit forces a yoke current proportional to input voltage by including the yoke within a current sensing feedback loop. In this example, the feedback resistors R_F and R_I are configured for a minimum gain of 5 to compensate for the added booster gain, thereby easing stability considerations. The auxiliary feedback network Cf and Rd act to bypass the 90° phase shift of the yoke/sense resistor feedback at higher frequencies ensuring stability with best transition times. The fastest transition time in any magnetic deflection amplifier is determined by the available voltage swing and yoke inductance. In the circuit of Figure 4, nearly 140 volts could be made available for the 200 microhenry yoke, resulting in a minimum possible transition time of 2 microseconds. The TL071 and PB58 combination can slew at 40 V/microsecond which means the amplifier requires an additional 4 microseconds to provide full voltage swing. The end result is a circuit that can deliver total transition times of less than 6 microseconds, equating to sweep speeds of 83 kHz.

An important advantage of a separate booster amplifier in deflection applications is the ability to swing the output stage supply rails to improve efficiency. Slower sweep speeds can use lower power supply voltages than higher speeds. In addition, during a high speed sweep the high voltage is only needed for a short period of time until yoke current builds and can then be switched to a lower value. Using the lower supply voltages whenever possible improves efficiency and reduces dissipation. In applications where the supply rails will be **"flexed"** in this manner, only the rails connected to the power booster need to be flexed. The constant supply available at the driver

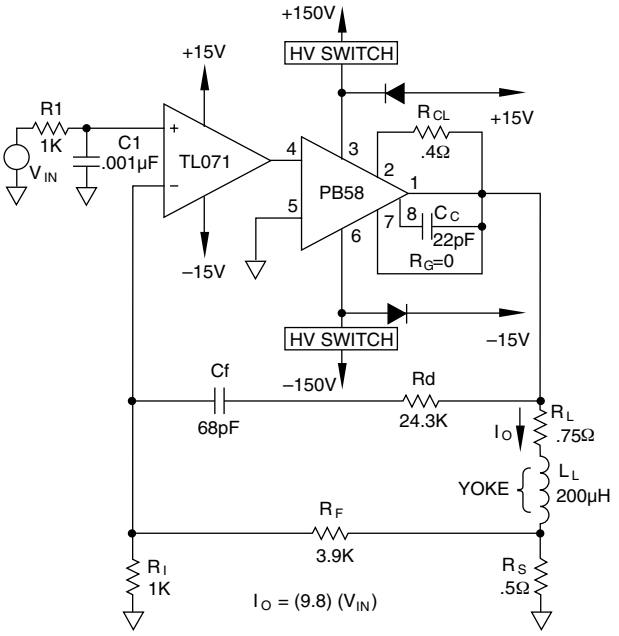


FIGURE 4. ELECTROMAGNETIC DEFLECTION AMPLIFIER

amplifier enhances the driver amplifier's ability to maintain overall loop control by preventing the coupling of supply switching transients into the input section of the amplifier.

Figure 4 provides a general idea of the circuitry involved in switching the supply rails. The actual implementation could take on many forms that are beyond the scope of this application note.

A final performance consideration in magnetic deflection amplifiers is avoidance of slew rate overload (or any condition which could result in input overload). This problem actually occurs during the rapid retrace transition, but shows up during the trace interval. The evidence of input overload is ringing during the trace interval. To eliminate this problem, reduce the transition time of the retrace portion of the input waveform to a rate which is within the slew rate specification of the amplifier. Slower transition times do not necessarily reduce circuit performance since the amplifier was overloaded to begin with, and eliminating ringing is actually an improvement on settling time when returning to the trace interval. Controlling input slew rate can be accomplished in many ways. If the actual risetime of the input signal itself cannot be controlled, a simple lowpass R-C filter at the input of the amplifier will suffice. In the example shown in Figure 4., R1 and C1 provide a filter which limits the slew rate of any input signal rise time to within the amplifier's slew rate.

Selection of the correct filter time constant takes into account both amplifier slew rate and gain of the circuit. In the case of a magnetic deflection amplifier, the appropriate value for gain would be the effective gain of the alternate feedback path Cf and Rd.

$$t = \frac{V_{IN}\ Av}{SR}$$

Where: V_{IN} = PEAK TO PEAK INPUT VOLTAGE
Av = COMPOSITE AMPLIFIER CLOSED LOOP GAIN
SR = RATED SLEW RATE OF THE AMPLIFIER

BOOSTER WITH NO DRIVER

It is entirely possible to use power boosters without an external driver. This could be done for simplicity or economy. It also provides the best slew rate and bandwidth performance possible with the PB series. All of this is made possible due to the boosters' self-contained internal feedback loop.

When used without a driver, the PB50 will have an inherent offset of typically 750 millivolts. Harmonic distortion remains under 0.5% at up to 30 kHz. Input impedance will be 25 K ohms minimum. Power bandwidth will typically be the full 320 kHz at the 100 Volts P-P output the PB50 is capable of.

The ground terminal on pin 5 of the PB50 presents possibilities as an additional input. Some improvement in bandwidth would be noted if this terminal were used as an input with the actual input terminal grounded. This forces the input transistor into a cascode connection. It is possible to utilize the booster as if it had true op amp type inverting and non-inverting inputs.

NEW MOSFET POWER OP AMPS EASE SAFE OPERATING AREA LIMITATIONS

Hybrid power op amps continue to provide higher levels of performance and power handling than their monolithic counterparts. Power MOSFET's promise to continue the dominance of the hybrid power op amp in terms of power delivery and Safe Operating Area (SOA).

Protection issues must not be neglected regardless of amplifier choice, but the compromises required to protect the amplifier are eased with MOSFET designs. Protection of an amplifier is a matter of keeping it within its SOA under all expected conditions including faults such as short circuits.

An example of a common mistake in selecting an amplifier for a motor drive application is to use a 5A rated amplifier to drive a 1A motor. Specifying an amplifier for a motor drive application is not that simple, and stall or reversal conditions could overstress the amplifier.

Here is an illustration using a motor with the following specifications:

Winding resistance: 1.24 ohms
Voltage constant: 7.41V/K RPM
Torque constant: 10oz/in/A

The actual running current depends on the required torque. Of most concern is the worst-case current requirements that occur under stall and acceleration conditions. Under stall conditions, the amplifier is presented with a load equal to the winding resistance of the motor. This condition must be within the SOA of the amplifier.

The motor's speed determines the applied voltage. If there are sudden reversals, the motor back EMF could theoretically reach a value equal to the full applied voltage or equal to the amplifiers supply rails. This would be equivalent to shorting the amplifier output to one of its supply rails with only the motor winding resistance in series.

While the MOSFET power op amps are often featured for their high speeds, motor drive applications can take advantage of the MOSFET SOA that is free from second breakdown. Second breakdown is a limitation of all bipolar output power op amps. Second breakdown severely limits an op amp's current capacity under conditions of high voltage stress. The MOSFET on the other hand is strictly limited by its power dissipation, or thermal limits. Figure 1compares the 25°C SOA of the PA04 MOSFET amplifier with the bipolar PA03. While the PA03 is rated for higher currents and dissipation, the PA04 has greater current capacity when there is more than 110V stress on the output devices.

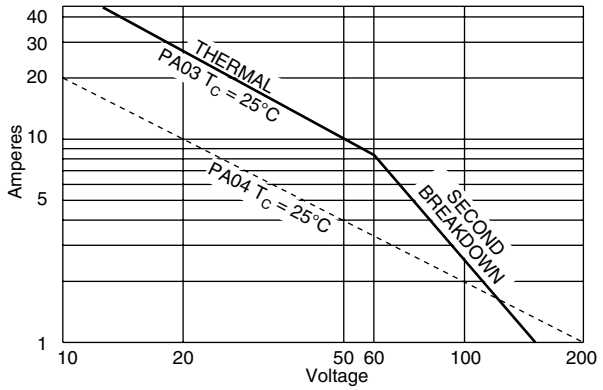


FIGURE 1. COMPARISON OF SOA FOR BIPOLAR (PA03) AND POWER MOSFET (PA04) POWER OP AMPS

For 25°C SOA calculations with a MOSFET amplifier an SOA graph is not even necessary. As long as the product of voltage and current stress is within the power dissipation rating, the amplifier is safe. MOSFET's, to reiterate, are strictly power limited.

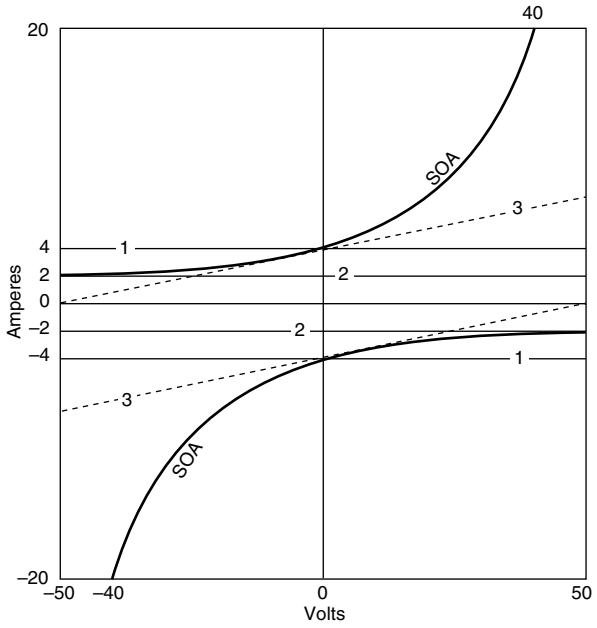


FIGURE 2. PLOT OF OUTPUT VOLTAGE AND CURRENT WITH SOA SUPERIMPOSED

Proper selection of current limit will determine if an amplifier is safe under fault conditions. One way of viewing this limitation is to draw a graph of output voltage and current, and superimpose SOA limits as shown in Figure 2. This graph (PA04 and ±50V supplies shown) illustrates how greater currents are available when the output voltage swings closest to the rail supplying the current. The tradeoff occurs when setting current limits, usually for either of two fault conditions: shorts to ground or shorts to either supply rail. A stalled motor is equivalent to a short to ground through the motor winding resistance, while a reversal could assume the stresses of a short to either rail.

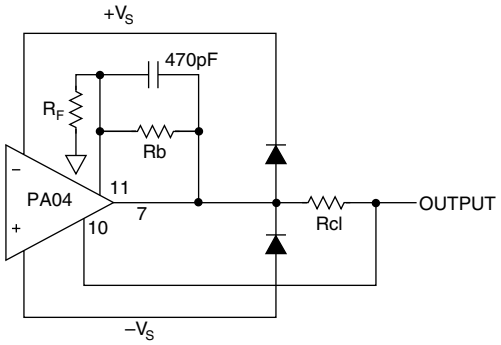


FIGURE 3. FOLDOVER CURRENT LIMITING CIRCUIT

From Figure 2, line 1, a limit safe for shorts to ground would be 4A (4A*50V=200W). This is well below the amplifier's full 20A capability. Even more stringent is the current limit for a short to either rail of 2A indicated by line 2 of Figure 2. A 2A limit, combined with external flyback diodes, would result in an amplifier tolerant of virtually any short or voltage kickback stress on its output. Keep in mind that this brief example uses as its basis, the 25°C SOA limits. In reality, internal dissipation and heatsinking limitations elevate temperatures, further reducing safe current levels.

G

FOLDOVER CURRENT LIMITING

The PA04 features four-wire current limit to overcome sensing errors occurring when working with such low resistances. While this four-wire current limit is useful in improving accuracy of current limit, it also facilitates implementing foldover current limiting. This limiting is known as load line limiting.

Foldover current limit allows more amplifier current as the output swings closer to the rail supplying the current shown by line 3 in Figure 2. Figure 3 shows the circuit to implement foldover current limiting. Rb and Rf configure a voltage divider that reduces the signal to the current limit transistors as the output swings closer to the current-supplying rail. Rf determines the slope of the foldover function. The value selected for Rb corresponds to the similar resistor internal to PA12 (actually 280 ohms) so that equations and methods developed for use with PA12 foldover limiting would be easily applied to PA04 external foldover limiting. The capacitor across Rb prevents stability problems while in current limit.

The foldover slope must not be too steep, or latching may occur. This sets a limit to the value of Rf equal to V_S/.0025 which results in a foldover characteristic where current available when the voltage output has swung fully to the rail opposite to the one supplying current is zero. The current available when the output is closest to the rail supplying current is twice that available when the output is at zero volts. When using PA12 equations, substitute this value of Rf, in Kohms.

A PA04 incorporating foldover limiting at ±50V and requiring safety for a short to ground, would have R_{CL} selected for a 4A limit (this presumes the amplifier case can be maintained at 25°C for the duration of the short, otherwise it would have to be reduced further to stay within temperature limitations). The foldover limiting would then allow 8A at full output swing, or near zero current when delivering current from the rail opposite the output voltage polarity. A bipolar amplifier such as PA12 would be limited to 3.2A under the same criteria. The most powerful monolithic would be limited to 300mA because it is configured only for simple single resistor current limiting.

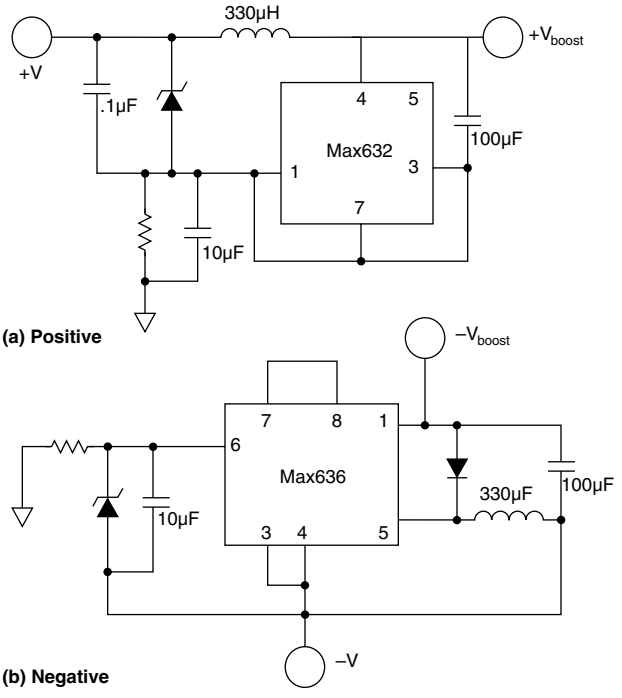


FIGURE 4. VOLTAGE BOOST CIRCUITS

SATURATION VOLTAGE AND BOOST PINS

In motor drive applications at lower voltages, the saturation voltage, described on the data sheet as *voltage swing*, the PA04 could result in considerable power dissipation. At 15A, the PA04 output can only swing to within 8.8 volts of the rail resulting in 132W of dissipation. Boost pins are provided on the PA04 to power the front-end of the amplifier on voltages higher than the output stage, thus improving saturation. Using these terminals reduces the swing-to-rail to 5.3V at 20A for 106W dissipation. At 15A it is 4.7V for 60.5W dissipation.

Several methods can be used to supply the higher voltage required by the front-end. Additional power transformers, or additional taps on existing power transformers, or additional regulated supplies are obvious options. Modern voltage converter IC's make it inexpensive to develop these voltages under almost any condition. In Figure 4, zener regulated voltages are referred to each rail and provide power to Maxim voltage converter IC's to develop the boost potentials.

MOSFET ADVANTAGES AT HIGHER VOLTAGES

The PA04 is rated at ±100V or 200V rail-to-rail. This is twice the rating of any bipolar hybrid power op amp other than PA03, and 2.5 times the rating of any monolithic power op amp.

MOSFET's have made possible this increase in voltage ratings and this can be useful in motor drive applications at high voltages. Surprisingly, some DC motors require voltages around 100 volts. The PB50 power booster is a low-cost hybrid *buffer with gain* that gives the same ±100 volt capability of PA04 with a maximum current of 2A. Because the PB50 is a MOSFET device, it can still provide 200mA at a full 200V stress.

An upgrade to the PB50 is the PB58 providing voltage capability up to ±150 volts. While PB58 is rated 1.5A, the premium PB58A is specified up to 2A. A key advantage of PB58, especially for motor drives, is its 87W dissipation. Operated at ±100V, the PB58 can provide 435mA with complete safety. At ±50V, PB58 can deliver up to 870mA. This is well over twice what could be tolerated from an amplifier such as the PA12 under the same conditions, much less from monolithic power op amps.

Both PB50 and PB58 are power booster amplifiers, not stand alone op amps. Refer to PB50 and PB58 data sheets for typical examples of actual composite amplifier circuits. Several alternatives are given. They range from low speed, high accuracy circuits, to high speed circuits.

ADVANCED AMPLIFIER PROTECTION

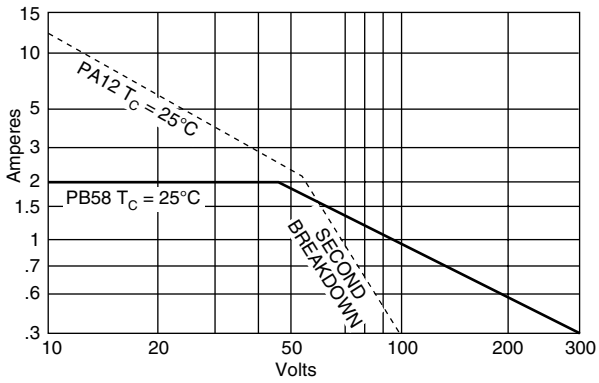


FIGURE 5. COMPARISON OF SOA FOR PA12 AND PB58

The PA04's adaptability to foldover current limiting is important but not the last word in protection. Prior efforts at SOA protection have been based on bipolar transistor designs sensing output transistor temperature combined with current limiting. These techniques have shortcomings when overstress occurs while operating in the second breakdown region of bipolar power devices. The isolated hot spot occurring during second breakdown can escape sensing by the temperature sensor.

For example, PA03 senses power transistor temperature to provide a high degree of protection. But at total rail-to-rail voltages in excess of 60V (±30V), second breakdown still makes the amplifier prone to failure in extreme stresses.

In a MOSFET power output device, if a local hot spot occurs, the local transconductance decreases along with an increase in Rds at the hot spot. This facilitates thermal spreading rather than concentrating heat. As a result thermal sensing should prove extremely effective with power MOSFET's. Apex is developing such amplifiers and early testing has shown that this may be the key to ultimate amplifier protection.

WIDEBAND, LOW DISTORTION TECHNIQUES FOR MOSFET POWER AMPS

Shake table systems, function generators and acoustic instruments all have requirements similar to quality audio amplifiers: wide bandwidths along with low distortion. In the past, industrial grade power op amps have traded off bandwidth to insure unity gain stability, and the bipolar designs have not always met the linearity requirements of demanding applications. The PA04 changes all this with a MOSFET based architecture that sets new standards for bandwidth and linearity of integrated circuit power amplifiers.

The development of the PA04 was driven by sonar application requirements for a highly linear, high power amplifier with a power bandwidth in excess of 100 kHz. MOSFET's are the optimum choice power device to provide this performance, and in the PA04 Apex goes several steps further in using MOSFET's in all active gain stages. While this application note will focus on getting best bandwidth and linearity from the PA04, the techniques described apply to any power op amp.

Op amps depend on negative feedback to improve performance in all ways including accuracy, linearity and bandwidth. The ideal condition is to use feedback around a design which has inherently good open loop characteristics. Evaluation of prospective amplifiers under open loop conditions quickly reveals linearity and bandwidth deficiencies. Even a simple distortion measurement under open loop conditions will give rapid comparative evaluation. Alternatively, an X-Y comparison using an oscilloscope and the circuit of Figure1, which multiplies summing node error by 100, will give a visual display of amplifier linearity. The circuit of Figure 1 will reveal that PA04 has an inherently linear characteristic while even the best bipolar designs such as PA07 have quite a bit of curvature in their open loop linearity. This is traceable to the better inherent linearity of MOSFET devices in comparison to bipolar transistors.

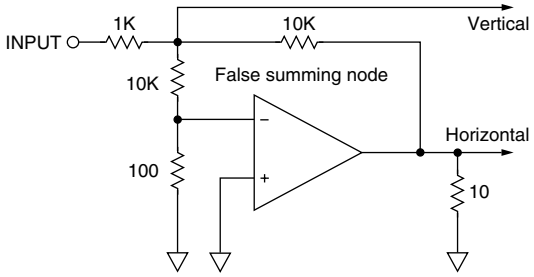


FIGURE 1. SIMPLE TEST CIRCUIT

CIRCUIT CONSIDERATIONS

The design considerations desirable for wideband, low distortion designs can be summed up with four guidelines:

1. Lowest possible closed loop gain.
2. Inverting configuration.
3. External phase compensation.
4. Input slew-rate limiting.

Distortion reduction in an op amp circuit is proportional to the amount of feedback, and this corresponds to lower gain circuits having reduced distortion. Distortion reduction is described mathematically as:

$$Df = D\left(\frac{Af}{A}\right)$$

Where: Df = % DISTORTION WITH FEEDBACK
D = % DISTORTION OPEN LOOP
A = OPEN LOOP GAIN
Af = CLOSED LOOP GAIN

It is obvious that open loop distortion is an important criteria in amplifier selection. A high open loop gain is also desirable, but op amps with high open loop gains most often have a severe tradeoff in gain-bandwidth.

The minimum useful closed loop gain is determined by the amplitude of the drive signal available to the power op amp circuit. Most often this drive is likely to come from a small signal op amp with the customary ±10 V peak drive capability. If for example a PA04 power op amp is being designed which operates at the full ±100 V supply rail limit of the PA04, this will require a minimum gain of 10.

In the event the drive signal is not a full ±10V peak, a tradeoff must be made as to whether the power op amp should be operated at a higher gain, or an additional small signal op amp be included for additional gain. Consider that the additional small signal op amp will result in insignificant contributions to distortion as long as its gain is low (<30). The light loading of the power amp circuit further minimizes distortion from the small signal op amp. These considerations favor this multiple op amp approach with a lower gain power op amp compared to a single high gain power op amp.

Low closed loop gain in the power op amp equates to increased amounts of negative feedback. This condition occasionally meets with unfounded objections when the requirement is low distortion, especially under transient conditions. However, this is dealt with by slew rate limiting to be discussed later.

The inverting amplifier configuration forces common mode potentials to zero. By doing so, non-linearities due to common-mode effects are also reduced to zero. The main advantage a non-inverting configuration would have is greater freedom of design regarding input impedance of the power op amp circuit along with the obvious lack of inversion.

Although the inverting configuration reduces input impedance, the two amplifier approach insures that the power amp circuit is driven by a source adequate to handle the resultant impedance. The cascade of two inverting amplifiers yields a non-inverting circuit. A further possible useful feature of the inverting power amp circuit is that the summing node can be monitored and any voltage detected used to indicate fault or non-linear conditions.

EXTERNAL PHASE COMPENSATION

Many power op amps are internally compensated for unity gain stability. However, this trades off gain-bandwidth product for stability under all operating conditions. Since distortion reduction is proportional to the ratio of open loop to closed loop gain, it is desirable to have as high as possible open-loop gain at high frequencies. Since it is unlikely that the power op amp will be configured for unity gain, the external phase compensation allows for a reduced compensation, yielding improved distortion and slew performance.

The small signal response curve for PA04 shown in Figure 2 helps to illustrate the comparative advantage of external phase compensation. The straight line at 20dB represents a gain of 10 amplifier which if the PA04 were compensated for unity gain would provide a 200 kHz rolloff. Decompensation for a gain of 10 results in a 700 kHz rolloff. In addition, note that loop gain for the unity-gain compensation is only 22 dB at 20 kHz, while it is 30 dB for the gain of 10 compensation. This increase in loop gain results in 2.5 times less distortion at 20 kHz.

The large amount of feedback at low gains obviously reduces distortion. Problems can occur however under transient conditions. If a step function is applied to the input of the amplifier circuit, the output can only change as fast as the amplifier slew rate allows. During this slew interval the input summing node will develop a large differential voltage. This nonlinear condition and input overload can cause a host of difficulties including a slow and poorly behaved recovery from this overload.

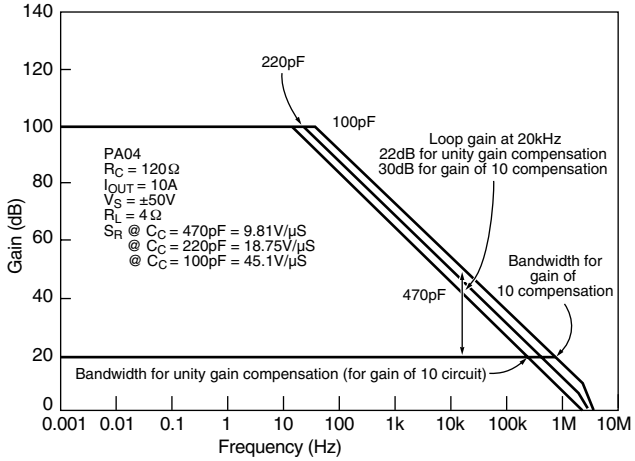


FIGURE 2. THE SMALL SIGNAL RESPONSE FOR THE PA04

Restriction of the input slew rate can avoid these transient distortion problems. The input should never be allowed to slew faster than the amplifier output can follow. If the actual slew rate of the source cannot be predicted or controlled, then simple low pass filtering at the amplifier input will prevent transient distortion.

The filter time constant is a function of amplifier slew rate. The maximum acceptable rate-of-change on the input signal is limited to a value less than the amplifier slew rate divided by the amplifier gain. With a known maximum step function input, the maximum rate-of-change at the low pass filters output occurs at t=0 and is determined by:

$$dv/dt = (V/R)/C$$

The RC time constant trc required at the amplifier input is:

$$trc = (V_{IN}A_V)/S_R$$

Where: V_{IN} = PEAK-TO-PEAK INPUT VOLTAGE
A_V = CLOSED LOOP GAIN
S_R = SPECIFIED AMPLIFIER SLEW RATE

Note that there is some reduction in bandwidth with this filter. However, with the PA04 this still permits a 40 kHz bandwidth. This limitation again favors the use of the fastest possible power amplifiers. Keep in mind that transient behavior is actually enhanced by the addition of the input filter.

STABILITY CONSIDERATIONS

When a power amplifier drives a capacitive load, the interaction between output resistance and capacitive load creates an additional pole and attendant phase shift in amplifier response (Figure 3). Inductive loads can result in stability problems due to rising impedances at high frequencies. Most follower type output stages are immune to the effects of inductive loads, but collector output, drain output and quasi-complementary output stages with local feedback loops are susceptible to parasitic oscillations driving inductive loads.

Figure 4 shows several measures are available to improve stability, each with some advantage and disadvantage: (a.) Capacitor across feedback resistor. This provides a compensating phase lead in the feedback path to counteract the effects of additional poles. This technique generally requires a unity-gain stable amplifier. (b.) Parallel inductor-resistor combination in series with amplifier output. Feedback

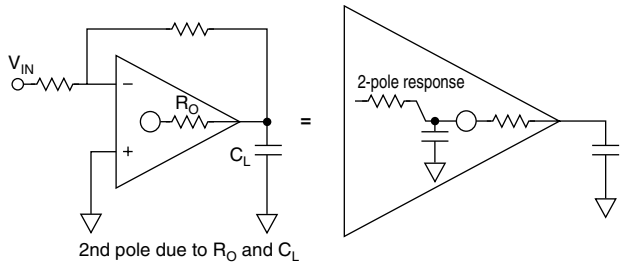


FIGURE 3. CAPACITIVE OP AMP LOADS

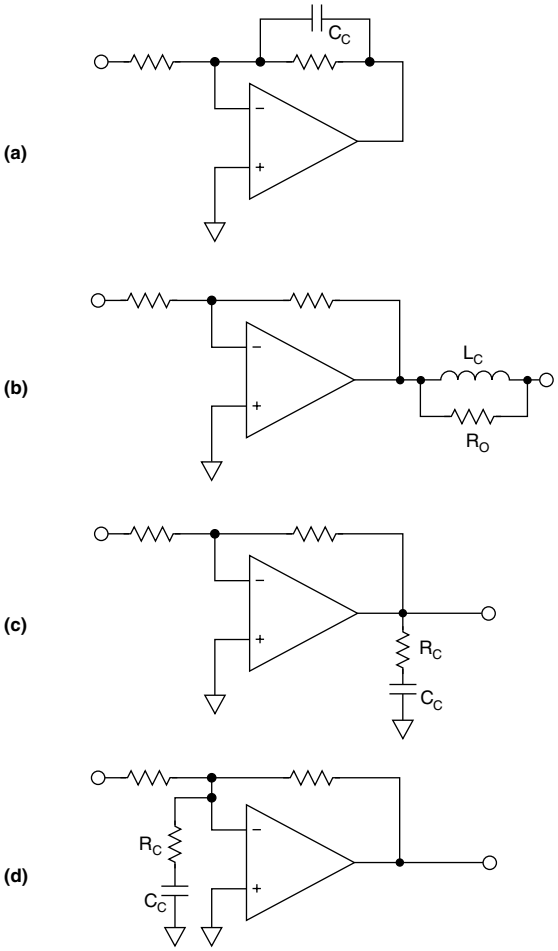


FIGURE 4. STABILITY ENHANCING TECHNIQUES

must be taken directly at output of amplifier so that inductor-resistor has the effect of isolating the amplifier and feedback network from the capacitive load. (c.) Series resistor and capacitor from amplifier output to ground, often referred to as a *snubber*. Used only in situations where amplifiers are sensitive to inductive loads. Insures a low, resistive load impedance at high frequencies. (d.) Series R-C network across op amp inputs, often referred to as *noise-gain compensation*. Simply described, this technique reduces feedback at high frequencies to the point where stability is not a problem.

Methods a and b offer the best overall bandwidth performance and transient behavior. Method a has been mentioned already as having the tradeoff of requiring a unity gain stable amplifier. However, with proper attention to design, it is possible to incorporate method a with any amplifier to help control overshoot and ringing behavior.

Method d, the noise gain compensation, will have the effect of reducing the closed loop bandwidth of the resultant circuit to the same effective closed loop bandwidth corresponding to the noise gain. To illustrate, consider a gain of 10 amplifier with a network across the inputs configured for a high frequency noise gain of 100. If the gain of 10 amplifier had an uncompensated bandwidth of 100 kHz, with the noise gain compensation, the bandwidth would be reduced to 10 kHz. In addition, the response curve peaks near the high frequency limit resulting in overshoots in the square wave response.

All amplifiers vary in their ability to tolerate capacitive loading before stability problems occur. PA04 is especially good in this regard tolerating well over 1 uF while operating at a gain of 10. In the case of PA04, no additional stability enhancement measures are required and this is the ideal case for best frequency response.

TYPICAL DESIGN EXAMPLE

A design utilizing all of the guidelines described here would be constructed around a PA04 in an inverting gain of 10 configuration as shown in Figure 5. For additional gain the PA04 is preceded by a small signal op amp also operating at an inverting gain of 10. Many choices

are available for this op amp such as the 5534 or OP37. The PA04's tolerance of reactive loads negates the need for additional stability enhancement components.

With an 8 ohm load this circuit can supply over 300W at up to 150 kHz with the input slew rate filter bypassed. With the filter in place, gain begins to rolloff at 40kHz, although full output swing is available up to 150kHz. Distortion never exceeds 0.02% THD. Power supplies will need to be capable of at least 7A to support 8 ohm loads in ac coupled applications. Regulated supplies aren't necessary but are desirable from a reliability standpoint.

When designing for low distortion with PA04, the impedance of the feedback and input networks around the op amp should be kept as low as possible. The input MOSFET's of the PA04 cause it to have a large input capacitance which is nonlinear with variations in input signal. Excessive impedances will increase distortion due to these higher order capacitance effects. The 2K ohm input resistor of Figure 5 is high enough to avoid excessive loading of the small signal op amp and low enough to avoid distortion effects with the PA04.

Several basic practices are important to implement when using PA04. Power supply bypassing consisting of good high frequency capacitors, generally ceramic, must be connected from each supply rail to ground. Unless these capacitors are physically close to the amplifier, parasitic oscillations may occur. Even an inch away from the socket pins is too far. Be sure to read and observe all ESD precautions on the PA04 data sheet, and those shipped with PA04.

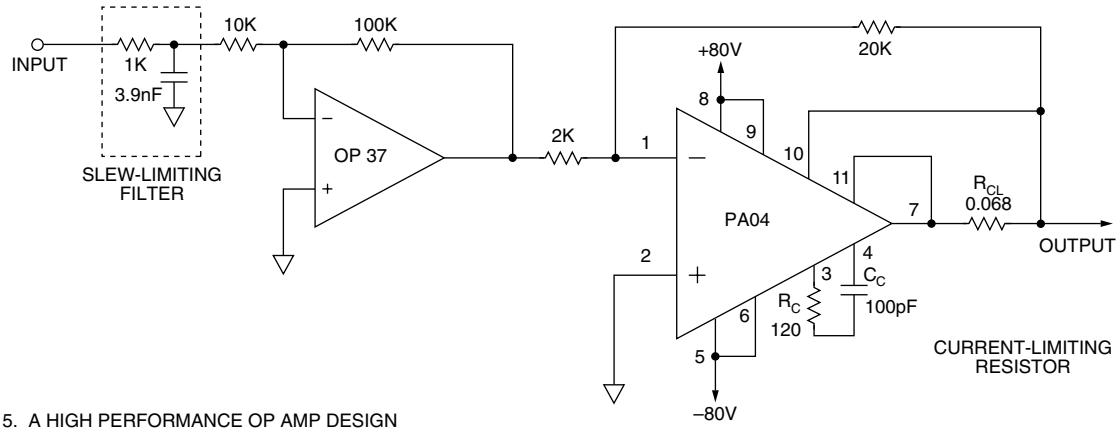


FIGURE 5. A HIGH PERFORMANCE OP AMP DESIGN

1.0 LOOP STABILITY Vs NON-LOOP STABILITY

There are two major categories for stability considerations — Non-Loop Stability and Loop Stability.

Non-Loop Stability covers design areas not related to feedback around the op amp that can cause oscillations in power op amp circuits such as layout, power supply bypassing, and proper grounding.

Loop Stability is concerned with using negative feedback around the amplifier and ensuring that the voltage fed back to the amplifier is less than an additional –180 phase shifted from the input voltage.

The two key factors to troubleshooting an oscillation problem are:

1) What is the frequency of oscillation? (refer to Figure 1 for definitions of UGBW (Unity Gain Bandwidth) and CLBW (Closed Loop Bandwidth) to be used throughout this text)
2) When does the oscillation occur?

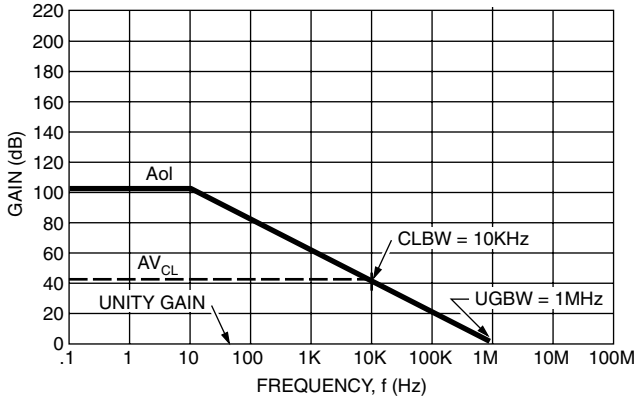


FIGURE 1. DEFINITION OF CLBW & UGBW

The answers to these two questions, along with the sections that follow, should enable you to identify and solve most power op amp stability problems. More importantly, by applying the recommendations in the following sections, you can design power op amp circuits free of oscillation.

2.0 NON-LOOP STABILITY

2.1 CASE GROUNDING

* fosc < UGBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—may or may not

Ungrounded cases of power op amps can cause oscillations, especially with faster amplifiers. The cases of all APEX amplifiers are electrically isolated to allow for mounting flexibility. Because the case is in close proximity to all the internal nodes of the amplifier, it can act as an antenna. Providing a connection from case to ground forms a Faraday shield around the power op amp's internal circuitry that prevents noise pickup and cross coupling or positive feedback.

2.2 RB+ BIAS RESISTOR

* fosc < UGBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—may or may not

Figure 2 is a standard inverting op amp circuit which includes an input bias current matching resistor on the noninverting input. The purpose of this resistor is to reduce input offset voltage errors due to bias current drops across the equivalent impedance as seen by the inverting and non-inverting input nodes. RB+ can form a high impedance node on the noninverting input which will act as an antenna

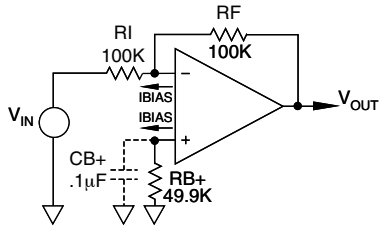


FIGURE 2. RB+

receiving unwanted positive feedback. Calculate your DC errors without the resistor. Some op amps have input bias current cancellation negating the effect of RB+. Some op amps have such low input bias currents that the error is insignificant when compared with the initial input offset voltage. Leave RB+ out, grounding the + input, if possible. If the resistor is required, bypass it with a .1 uF capacitor in parallel with RB+ as shown in Figure 2.

2.3 POWER SUPPLY BYPASSING

* fosc < UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?—may or may not

Supply loops are a common source of oscillation problems. Figure 3 shows a case where the load current flows through the supply source resistance and parasitic wiring or trace resistance. This causes a modulated supply voltage to be seen at the power supply pin of the op amp. This modulated signal is then coupled back into a gain stage of the op amp via the compensation capacitor. The compensation

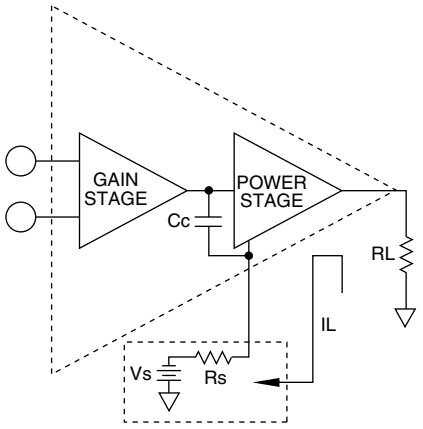


FIGURE 3. IL MODULATION

capacitor is usually referred to one of the supply lines as an AC ground.

Figure 4 shows a second case for supply loop oscillation problems. Power supply lead inductance interacts with a capacitive load forming an oscillatory LC, high Q, tank circuit.

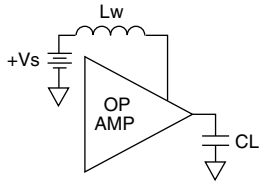
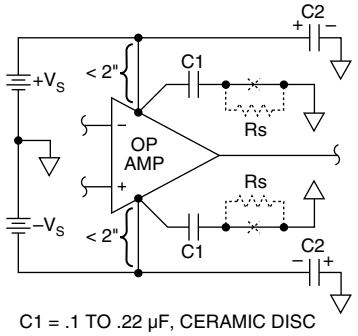


FIGURE 4. LC OSCILLATION

Fortunately, both of the above supply line related problems can be eliminated through the use of proper power supply bypass techniques. Each supply pin must be bypassed to common with a "high frequency bypass" .1uF to .22uF ceramic capacitor. These capacitors must be located directly at the power op amp supply pins. In rare cases where power supply line inductance is high, it may be necessary to add 1 to 10 ohms of resistance in series with the high frequency bypass capacitor to dampen the Q of the resultant LC tank circuit. This additional resistor will probably only be necessary when using a wideband amplifier since amplifiers of 5 MHz unity gain bandwidth or less will not respond to the high frequency oscillation caused by line inductance interacting with the high frequency bypass capacitor. Refer to Figure 5.



C1 = .1 TO .22 µF, CERAMIC DISC
C2 = 10 µF/AMP OUT (PEAK), ELECTROLYTIC
Rs = 3 –10Ω (PROVISIONAL–
HIGHLY INDUCTIVE P.S. LINES)

FIGURE 5. POWER SUPPLY BYPASSING

In addition, a "low frequency bypass" capacitor, minimum value of 10uF per Ampere of peak output current, should be added in parallel with the high frequency bypass capacitors from each supply rail to common. Tantalum capacitors should be used when possible due to their low leakage, low ESR and good thermal characteristics. Aluminum Electrolytic capacitors are acceptable for operating temperatures above 0°C. These capacitors should be located within 2" of the power op amp supply pins. Refer to Figure 5.

2.4 MULTIPLE AMPLIFIER BOARDS

* fosc < UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} =0?—yes

A prototype circuit is built and bench tested to confirm desired performance. Several channels of the same circuit are used on a printed circuit board layout. Much to the dismay of the design engineer, the amplifier circuits on the printed circuit board oscillate. Cross coupling through the power supply lines can be a major problem on multiple amplifier printed circuit boards. Ground the case of each amplifier and ensure each amplifier has its own power supply bypassing per Section 2.3.

2.5 OUTPUT STAGE OSCILLATIONS / OUTPUT R-C SNUBBER

* fosc > UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?— no, only oscillates over a portion of the output cycle

Sometimes output stages of power op amps can contain local feedback loops that give rise to oscillations. The first type of output stage instability problem arises from a tendency of emitter followers to appear inductive when looking back into their emitter. This occurs if they are driven from a low impedance source and can create output stage oscillations if capacitance is present on the amplifier's output. Refer to Figure 6. This type of instability is rare and usually only shows up when driving load capacitances within a limited range of values.

The second, more common type of output stage oscillation is due to non-emitter follower output type stages. These stages have heavy local feedback paths. Refer to Figure 7 which is an example of a composite PNP type output stage. This stage is typical of monolithic

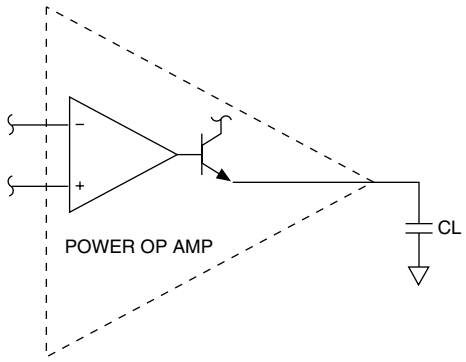


FIGURE 6. EMITTER FOLLOWER WITH C LOAD

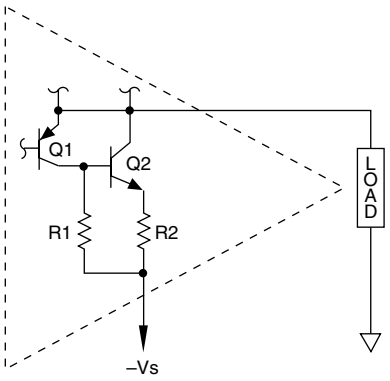


FIGURE 7. COMPOSITE OUTPUT STAGE

power op amps where high current PNP transistors are not readily available. The local feedback in the Q1, Q2 loop will cause output stage oscillations when the output swings negative under reactive loading.

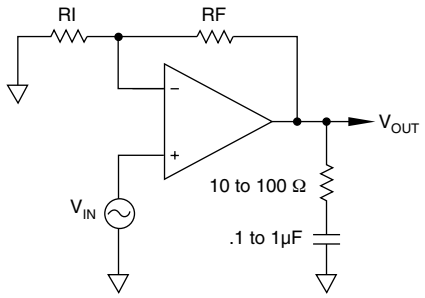


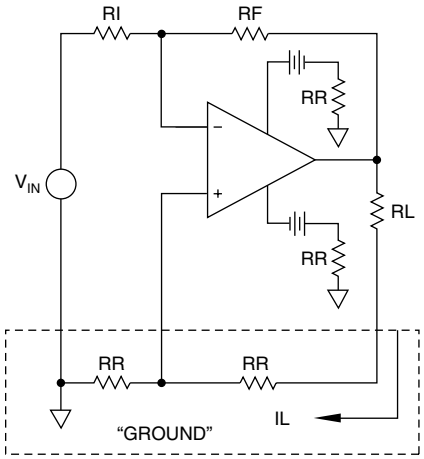
FIGURE 8. OUTPUT R–C SNUBBER

Both of these output stage problems can be fixed by using an R-C Snubber on the output of the op amp to ground or the negative supply rail. This is provided the negative supply rail is properly bypassed per Section 2.3. The Snubber network consists of a 10 to 100 ohm resistor in series with a capacitor of .1 to 1 µF (refer to Figure 8). This network lowers the high frequency gain of the output stage preventing unwanted high frequency oscillations.

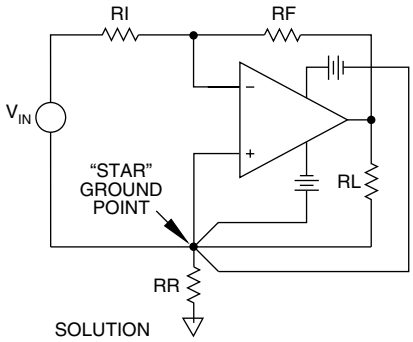
2.6 GROUND LOOPS

* fosc < UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?—yes

Ground loops come about from load current flowing through parasitic layout resistances and wiring. If the phase of the output signal is in phase with the signal at the node it is fed back to, it will result in positive feedback and oscillation. Although these parasitic resistances (RR in Figure 9) in the load current return line cannot be eliminated, they can be made to appear as a common mode signal to the amplifier.



PROBLEM



SOLUTION

FIGURE 9. GROUND LOOPS

This is done by the use of a "star ground" approach. Refer to Figure 9. The star ground is a point that all grounds are referenced to. It is a common point for load ground, amplifier ground, signal ground and power supply ground.

2.7 PRINTED CIRCUIT BOARD LAYOUT

* fosc < UGBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—no

High current output traces routed near input traces can cause oscillations. This is especially true when the output is adjacent to the positive input, giving undesirable positive feedback through capacitive coupling between the adjacent traces. Feedback, input, and bypass components, along with current limit sense resistors, should be located in close proximity to the amplifier.

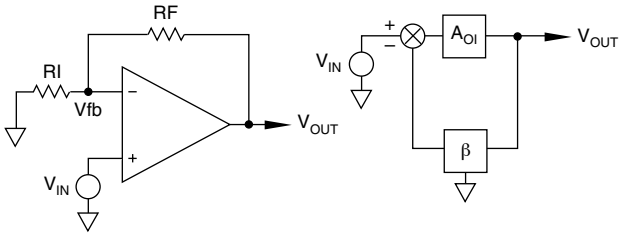
If a printed circuit board has both a high current output trace and a return trace for that high current, then these traces should be routed adjacent to each other (on top of each other on a multi-layer printed circuit board) so they form a twisted pair type of layout. This will help cancel EMI generated outside from feeding back into the amplifier circuit.

3.0 LOOP STABILITY

3.1 BETA β - FEEDBACK FACTOR

Control theory is applicable to closing the loop around a power op amp. The block diagram in Figure 10 consists of a circle with an X, which represents a voltage differencing circuit. The rectangle with Aol represents the amplifier open loop gain. The rectangle with the β represents the feedback network. The value of β is defined as the fraction of the output voltage that is fed back to the input; therefore, β can range from 0 (no feedback) to 1 (100% feedback).

The term Aol β that appears in the V_{OUT}/V_{IN} equation in Figure 10, has been called "loop gain" because this can be thought of as a signal propagating around the loop that consists of the Aol and β networks.



$$Vfb = \frac{V_{OUT}\ RI}{RI + RF}$$

$$Vfb = \beta\ V_{OUT}$$

$$\beta = \frac{RI}{RI + RF}$$

$$V_{OUT} = V_{IN}\ Aol - Aol\ \beta\ V_{OUT}$$

$$\frac{V_{OUT} + Aol\ \beta\ V_{OUT}}{V_{IN}} = Aol$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{Aol}{1 + Aol\ \beta} = \frac{1}{\beta}$$

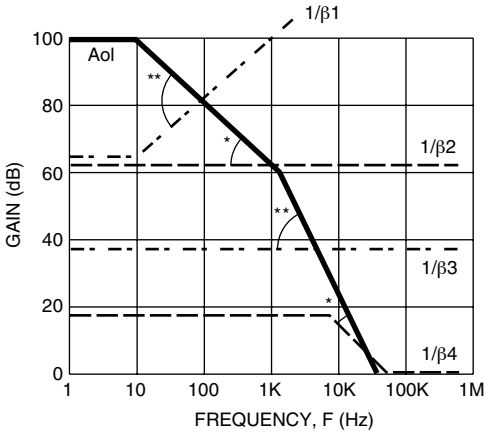
(FOR: Aol β >> 1)

FIGURE 10. BETA (β) – FEEDBACK FACTOR

If Aol β is large, there is a lot of feedback. If Aol β is small, there is not much feedback.

3.2 RATE OF CLOSURE & STABILITY

Refer to Figure 11. Aol is the amplifier's open loop gain curve. 1/β is the closed loop AC small signal gain in which the amplifier is operating. The difference between the Aol curve and the 1/β curve is



* 20 dB/ DECADE RATE OF CLOSURE → "STABILITY"
** 40 dB/ DECADE RATE OF CLOSURE → "MARGINAL STABILITY"

FIGURE 11. RATE OF CLOSURE & STABILITY

the "loop gain". Loop gain is the amount of signal available to be used as feedback to reduce errors and non-linearities.

A first order check for stability is to ensure when loop gain goes to zero, open loop phase shift must be less than 180 degrees where the 1/β curve intersects the Aol curve. Another way of viewing that same criteria is to say at the intersection of the 1/β curve and the Aol curve the difference in the slopes of the two curves, or the RATE OF CLOSURE, is less than or equal to 20 dB per decade. This is a powerful first check for stability. It is, however, not a complete check. For a complete check we will need to check the open loop phase shift of the amplifier throughout its loop gain bandwidth.

A 40 dB per decade RATE OF CLOSURE indicates marginal stability with a high probability of destructive oscillations in your circuit. Figure 11 contains several examples of both stable (20 dB per decade) and marginally stable (40 dB per decade) rates of closure.

3.3 EXTERNAL PHASE COMPENSATION

External phase compensation is often available on an op amp as a method of tailoring the op amp's performance for a given application. The lower the value of compensation capacitor used the higher the slew rate of the op amp. This is due to fixed current sources inside the front end stages of the op amp. Since current is fixed, we see from the relationship of I = CdV/dt that a lower value of capacitance will yield a faster voltage slew rate.

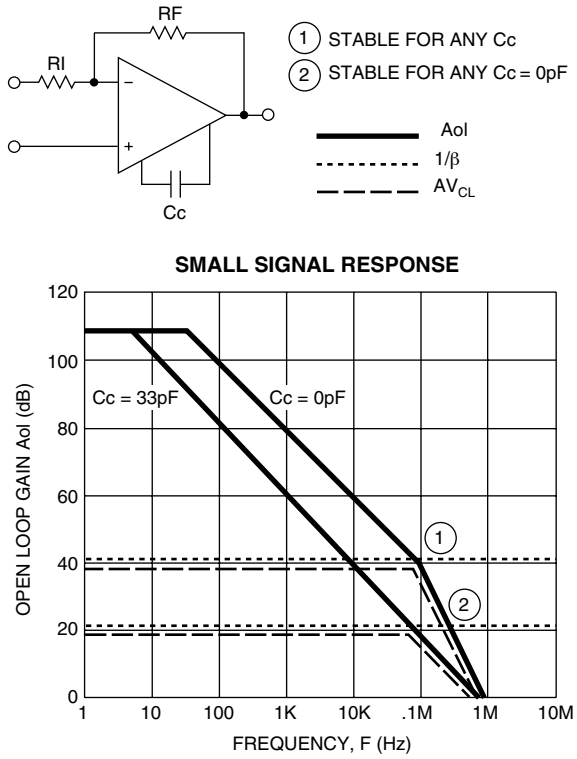


FIGURE 12. EXTERNAL PHASE COMPENSATION

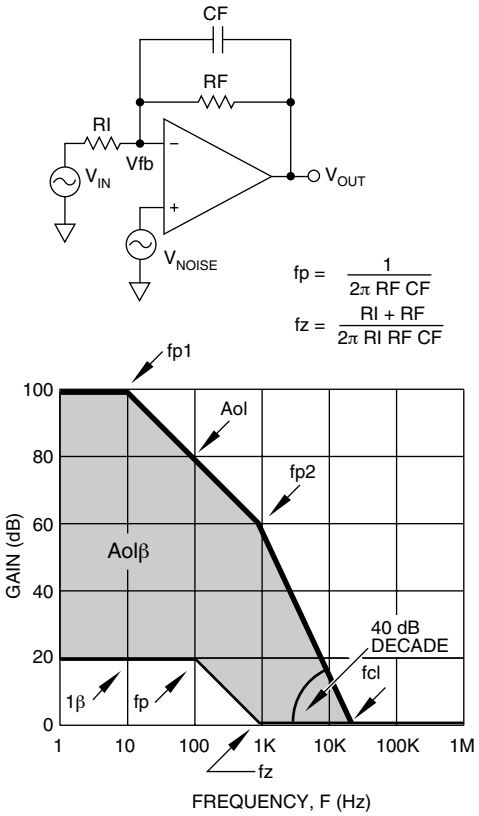


FIGURE 13. STABILITY– RATE OF CLOSURE

However, the advantage of a faster slew rate has to be weighed against AC small signal stability. In Figure 12 we see the Aol curve for an op amp with external phase compensation. If we use no compensation capacitor, the Aol curve changes from a single pole response with Cc = 33pF, to a two pole response with Cc = 0pF. Curve 1 illustrates that for 1/β of 40 dB the op amp is stable for any value of external compensation capacitor (20 dB/decade rate of closure for either Aol curve, Cc = 33pF or Cc = 0pF). Notice that 1/β curve continues on past the intersection of the Aol curve. At the intersection of 1/β and Aol, the AV_{CL} closed loop gain curve, or V_{OUT}/V_{IN} gain begins to roll off and follow the Aol curve. This is because there is no loop gain left to keep the closed loop gain flat at higher frequencies.

Curve 2 illustrates that for 1/β of 20 dB and Cc = 0pF, there is a 40 dB/decade rate of closure or marginal stability. To have stability with Cc = 0pF minimum gain must be set at 40dB. This requires a designer to not only look at slew rate advantages of decompensating the op amp, but also at the gain necessary for stability and the resultant small signal bandwidth.

3.4 STABILITY - RATE OF CLOSURE

Figure 13 shows a typical single pole op amp configuration in the inverting gain configuration. Notice the additional V_{NOISE} voltage source shown at the +input of the op amp. This is shown to aid in conceptually viewing the 1/β plot.

An inverting amplifier with its +input grounded, will always have potential for a noise source to be present on the +input . Therefore, when one computes the 1/β plot, the amplifier will appear to run in a gain of 1 + RF/RI for small signal AC. The V_{OUT}/V_{IN} relationship will still be –RF/RI. This is also why an amplifier can never run at a gain of less than one for small signal AC stability considerations.

The plot in Figure 13 shows the open loop poles from the amplifier's Aol curve, as well as the poles and zeroes from the 1/β curve. The locations of fp and fz are important to note as we will see that poles in the 1/β plot will become zeroes and zeroes in the 1/β plot will become poles in the open loop stability check.

Notice that at fcl the RATE OF CLOSURE is 40 dB per decade indicating a marginal stability condition. The difference between the Aol curve and 1/β curve is labelled Aol β which is also known as loop gain.

3.5 STABILITY - OPEN LOOP

Stability checks are easily performed by breaking the feedback path around the amplifier and plotting the open loop magnitude and phase response. Refer to Figure 14. This open loop stability check has the first order criteria that the slope of the magnitude plot as it crosses 0 dB must be 20 dB per decade for guaranteed stability.

The 20 dB per decade is to ensure the open loop phase does not dip to –180 degrees before the amplifier circuit runs out of loop gain. If the phase did reach -180, the output voltage would now be fed back in phase with the input voltage (-180 degrees phase shift from negative feedback plus -180 degrees phase shift from feedback network components would yield -360 degrees phase shift). This condition would continue to feed upon itself causing the amplifier circuit to break into uncontrollable oscillations.

Notice in Figure 14 this open loop plot is really a plot of Aol β. The slope of the open loop curve at fcl is 40 dB per decade indicating a marginally stable circuit. As shown, the zero from the 1/β plot in Figure 13 became a pole in the open loop plot in Figure 14 and likewise the pole from the 1/β plot in Figure 13 became a zero in the open loop plot of Figure 14. We will use this knowledge to plot the open loop phase plot to check for stability. This plot of the open loop phase will provide a complete stability check for the amplifier circuit. All the information we need will be available from the 1/β curve and the Aol curve.

4.0 STABILITY & THE INPUT POLE / INPUT & FEEDBACK IMPEDANCE

* fosc < CLBW
* oscillates unloaded?—yes
* oscillates with V_{IN} = 0?—yes

All op amps have some input capacitance, typically 6-10 pF. Printed circuit layout and component leads can introduce additional input stray capacitances. When high values of feedback and input resistors are used, this input capacitance will contribute an additional pole to the loop gain response (a zero in the 1/β plot, a pole in the open loop phase check for stability, or a pole in the Aol β, loop gain, plot).

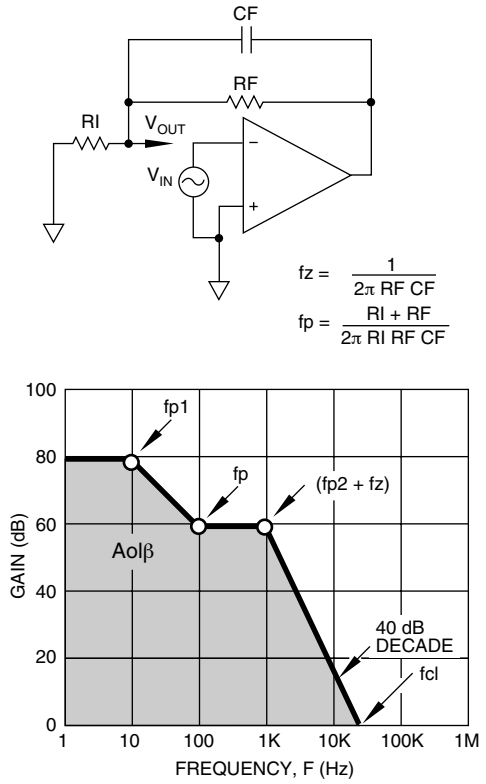


FIGURE 14. STABILITY– OPEN LOOP

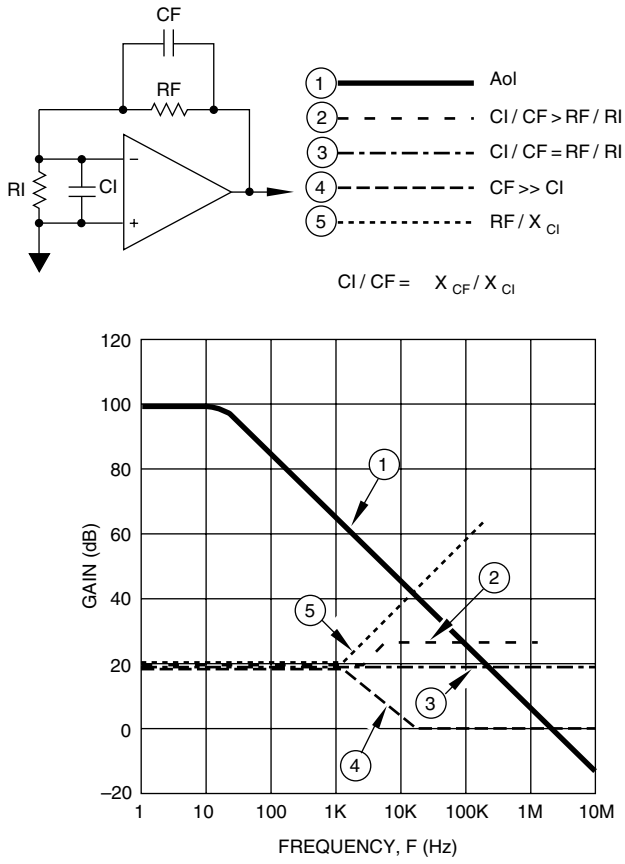


FIGURE 15. THE INPUT POLE

We will refer to Figure 15 for a detailed look at the input pole and stability. Remember, our first order criteria for stability is a Rate Of Closure of 20dB per decade or less. Curve 1 is the op amp's Aol plot. Curve 5 shows the effect of input capacitance with no CF feedback capacitor. We see the rate of closure is 40 dB per decade and marginal stability exists. With just CI present, as frequency increases, the impedance from the -input of the op amp decreases, thereby causing the 1/β plot to increase (remember $X_{CI} = 1/2\pi fCI$). If we now add some small value of CF as in Curve 2 we see the 1/β plot flatten out to intersect the Aol at a rate of closure 20 dB per decade implying stability. If we further increase CF, as in Curve 3, such that both breakpoints are the same frequency, we will have ZF/ZI constant over frequency and the 1/β plot will be flat with frequency. This yields the ever-stable 20 dB per decade rate of closure. If we then continue to increase CF as in Curve 4, we will see CFdominate as frequency increases and the net result is a low pass filter frequency roll-off. For this case the op amp must be unity gain stable, since the op amp operates at a gain of one for frequencies above 10KHz.

Often you will see CF recommended to be used to decrease overshoot and improve settling time for a transient input into a given op amp circuit. In the AC small signal domain, we are merely optimizing the circuit for stability.

Minimize values of feedback and input resistor values. This will reduce the effect of the input pole as well as help reduce DC errors by keeping voltage drops due to bias currents low. A summing node of an op amp can pick up unwanted AC signals and amplify them if that node is high impedance. Keeping the feedback and input resistance values low will reduce the impedance at the summing nodes and minimize stray signal pick up. Practical values for feedback and input resistance values are from 100 ohms to 1 megaohm.

5.0 LOOP STABILITY EXAMPLES

5.1 VOLTAGE TO CURRENT CONVERSION— FLOATING LOAD

* fosc < CLBW
* oscillates unloaded ? — yes
* oscillates with V_{IN} = 0 ? — yes

Figure 16 illustrates a common voltage to current conversion circuit. The input command voltage of +/-10V is scaled to control -/+1.67A of output current through the load.

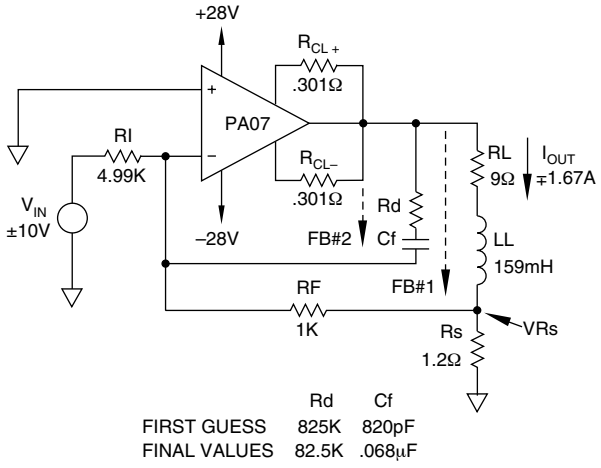


FIGURE 16. V-I CIRCUIT AND STABILITY

This V-I (Voltage to Current) topology is a floating load drive. Neither end of the load, series RL and LL, is connected to ground.

The easiest way to view the voltage feedback for load current control in this circuit is to look at the point of feedback which is the top of Rs. The voltage gain VRs/Vin is simply -RF/RI which translates to (–1K/4.99K = -.2004). The Iout/Vin relationship is then VRs/Rs or Iout = - Vin (RF/RI)/Rs which for this circuit is (Iout = -.167 Vin). We will use our knowledge of 1/β, Rate of Closure, and open loop stability phase plots, to design this V-I circuit for stable operation. There are two voltage feedback paths around the amplifier, FB#1 and FB#2. We will analyze FB#1 first and then see why FB#2 is necessary for guaranteed stability.

STABILITY SOLUTION FOR V-I CIRCUIT

STEP 1: On Figure 17 plot the op amp's Aol curve as given by the manufacturer.

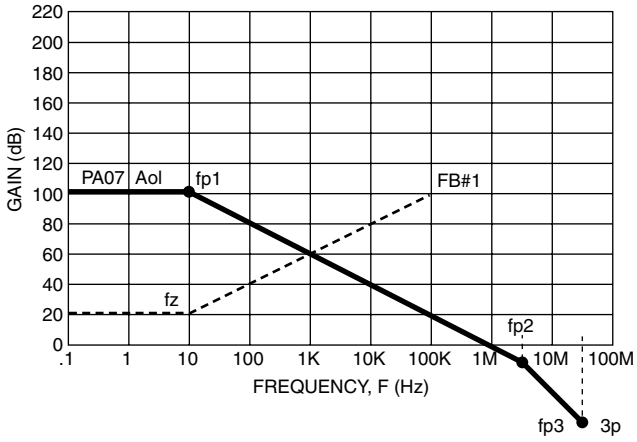


FIGURE 17. Aol AND FB # 1 – MAGNITUDE PLOT FOR STABILITY

STEP 2: On Figure 17 plot FB#1. Refer to Figure 18 for calculation of FB#1. At DC, LL is a short and so β is a voltage divider through resistors as shown in Figure 18. As we go to higher frequencies, the reactance of LL will increase ($XL = 2\pi fL$). This will increase the net load impedance which will cause β to decrease and $1/\beta$ to increase as frequency increases. Since we are working with a single reactive element the increase of that gain will be 20 dB per decade. Figure 18 details the breakpoint fz where this increase begins. We see that at the intersection of FB#1 and the PA07 Aol curves the rate of closure is 40 dB per decade indicating marginal stability.

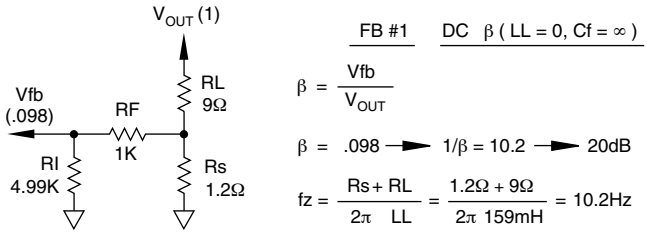


FIGURE 18. FEEDBACK NO.1 (FB #1)

STEP 3: Refer to Figure 19 which repeats PA07 Aol and FB#1. We will add FB #2 to force the high frequency part of the $1/\beta$ curve to flatten out and intersect the PA07 Aol curve at 20 dB per decade. FB #2 will dominate at frequencies above 1 KHz. Although our V-I circuit has two feedback paths, the op amp will follow whichever feedback path is dominant. This means the larger β is, the more voltage is fed back from the output to the -input as negative feedback (Remember $\beta = Vfb/V_{OUT}$). With a larger β, $1/\beta$ will become smaller; therefore, the dominant feedback path out of FB#1 and FB#2 will be the lowest gain path.

Plot a desired feedback path for FB#2. At high frequencies, FB#2 will be a flat line since Cf will be a short leaving a pure resistive divider for β. At DC, FB#2 will be infinite since Cf is an open. This will be limited by the PA07 Aol curve. Since we only have one reactive element in FB#2, we will have a 20 dB per decade slope from low to high frequency. Set fz1 one half to one decade below the intersection of FB#1 and FB#2. This "Decade" rule of thumb ensures that as component values and Aol curves vary we will not get into stability trouble—more about this later.

STEP 4: In Figure 19 the long-dashed line represents the $1/\beta$ feedback path that the PA07 operates in for small signal AC. According to our first order check for stability we see a 20 dB per decade rate of closure indicating a stable design. But let's do our complete stability check by using the $1/\beta$ curve

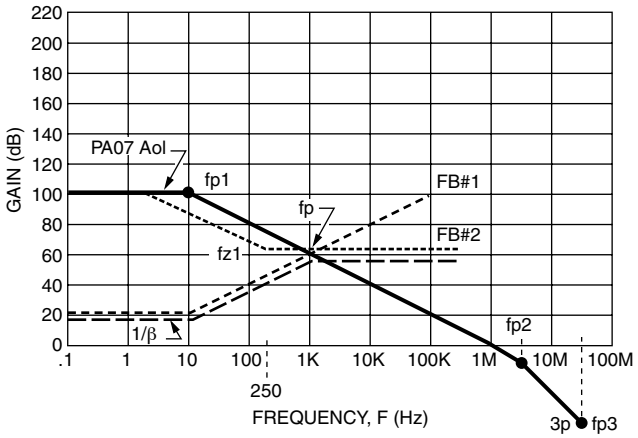


FIGURE 19. FIRST GUESS MAGNITUDE PLOT FOR STABILITY

and PA07 Aol curve to plot the open loop phase plot. Remember the following rules when plotting open loop phase plots for stability checks.

RULES FOR PLOTTING OPEN LOOP PHASE PLOTS

1) Poles in $1/\beta$ plot become zeroes in the open loop stability check.

2) Zeroes in $1/\beta$ plot become poles in the open loop stability check.

3) Poles and zeroes in the Aol curve of the op amp remain respectively poles and zeroes in the open loop stability check since the op amp Aol curve is an open loop curve already.

4) Phase for poles is represented by a -45 degree phase shift at the frequency of the pole with a -45 degree per decade slope, extending this line with 0 degree and -90 degree horizontal lines.

5) Phase for zeroes is represented by a +45 degree phase shift at the frequency of the zero with a +45 degree per decade slope, extending this line with 0 degree and +90 degree horizontal lines.

Figure 20 is the resultant open loop phase plot using the information from Figure 19. After plotting individual open loop poles and zeroes, and drawing the appropriate slopes, we graphically add the slopes to yield a resultant open loop phase as shown in Figure 20. Notice fp3 in Figure 20 is a triple pole. It is easier to plot this as shown in Figure 20 as three poles "on top" of each other. This makes it easier to add graphically for a resultant open loop phase plot. As shown in Figure 20, our open loop phase dips to -180 at 100Hz. Our first attempt at compensation was not successful since we desire at least 45 degrees of phase margin (open loop phase should not dip to less than -135 degrees).

STEP 5: We need to revisit FB#2 to make this V-I circuit stable. Figure 21 shows a new FB#2 and the resultant $1/\beta$ plot. Before we look at the open loop phase plot, let's discuss Figure 21. We see that in the PA07 Aol curve there is a pole at fp1, 10Hz, which will be a pole in our open loop phase plot. We also see a zero at fz, 10Hz, in the $1/\beta$ plot, which will become a pole in our open loop phase plot. Now we have two poles at 10Hz in our open loop phase plot. To keep the open loop phase from reaching -180, we must add a zero at 100Hz to get 45 degrees of phase margin. Poles and zeroes a decade beyond fcl, the intersection of $1/\beta$ and PA07 Aol, are of no concern for stability since at fcl the loop gain is zero. The reason we must look a decade beyond fcl on the magnitude plot is that poles and zeroes have an effect on phase plus or minus a decade away from their physical location on the magnitude plot.

Viewing the magnitude plot in this way can help us save iterative steps in compensating to guarantee good stability. Refer to Figure 22 (see second page following this one) for final open loop phase plot stability. Once the open loop phase plot verifies stability, it is time to compute final values for FB#2 components Rd and Cf. Figure 23 details these

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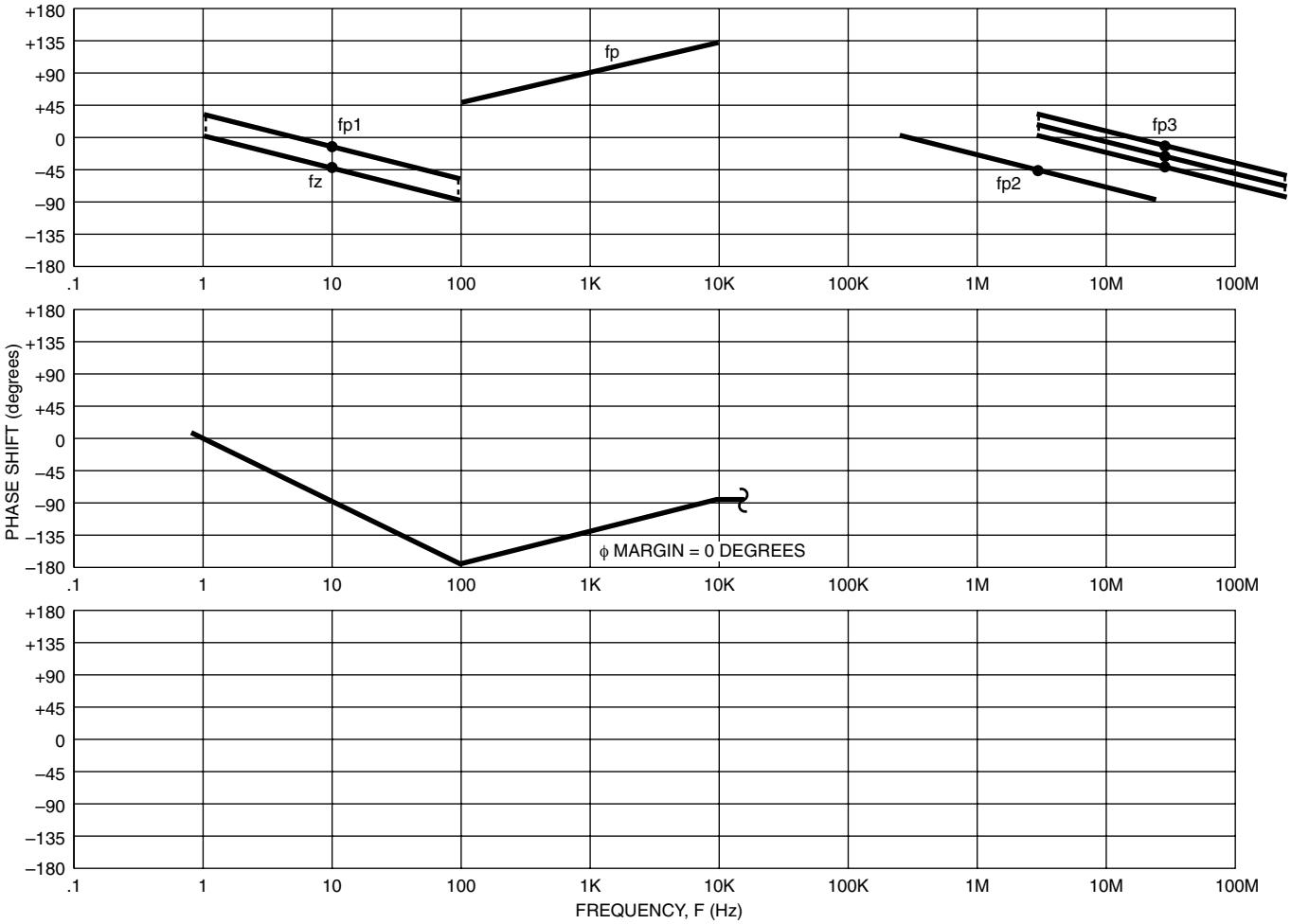


FIGURE 20. FIRST GUESS OPEN LOOP PHASE PLOT FOR STABILITY

calculations. Notice in Figure 23 that to work with β it is easiest to set Vout to 1 which then allows us to easily use voltage dividers and currents to calculate values for Rd. Cf is computed as given by the formula in Figure 23.

OPEN LOOP PHASE PLOTS FOR STABILITY — FINAL NOTE: This hand plotting technique is a linear graphical method. Actual magnitude plots run on such analog circuit simulations as SPICE will be 3 dB different and actual phase plots will be 6 degrees different.

5.2 CAPACITIVE LOADING & STABILITY

* fosc < CLBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?—yes

5.2.1 CAPACITIVE LOADING - GENERAL

Refer to Figure 24 (see second page follwong this one) for discussion of power op amps and capacitive loading. The output impedance of a power op amp, Ro, can interact with capacitive loads and form an additional high frequency pole in the op amp's Aol curve. This modified Aol curve is what we must look at for stability checks. In Figure 24, we see a modified Aol curve whose slope changes from 20 dB per decade to 40 dB per decade at 10 kHz. Note that the rate of closure for this circuit is 40 dB per decade indicating marginal stability.

5.2.2 CABLE AND CAPACITIVE LOADING

Beware of coaxial cables which can appear capacitive. A coaxial cable appears capacitive, instead of its characteristic impedance, resistive, if the length of the cable is less than one-fortieth of the wavelength in the cable at the frequency of interest, f. This length, l, is given by:

$$l \leq \frac{1}{40} \frac{Kc}{f} \text{ meters}$$

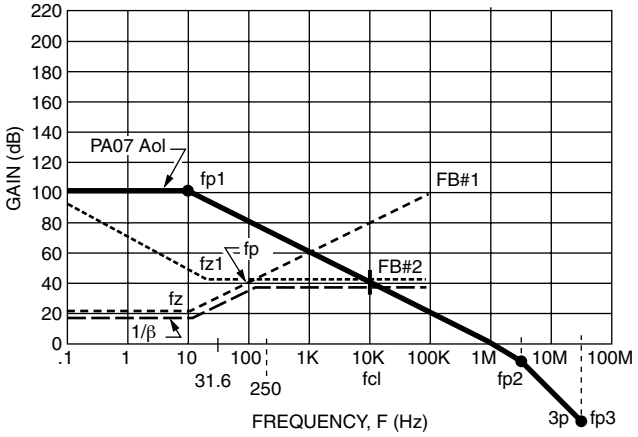


FIGURE 21. FINAL VALUE MAGNITUDE PLOT FOR STABILITY

where K is a propagation constant that is sometimes called the velocity factor (0.66 for coaxial cable) and c is the velocity of light (3.00 X10^8 m/s).

EXAMPLE: If f = 10KHz:

$$l \leq \frac{1}{40} \frac{(0.66)\ (3x10^8)}{10^4} = 495 \text{ meters } (1624 \text{ feet})$$

Cables less than 495 meters will appear capacitive for 10 kHz signals at the rate of 95 pF/meter (29 pF/foot) for RG-58A/U, a commonly used coaxial cable.

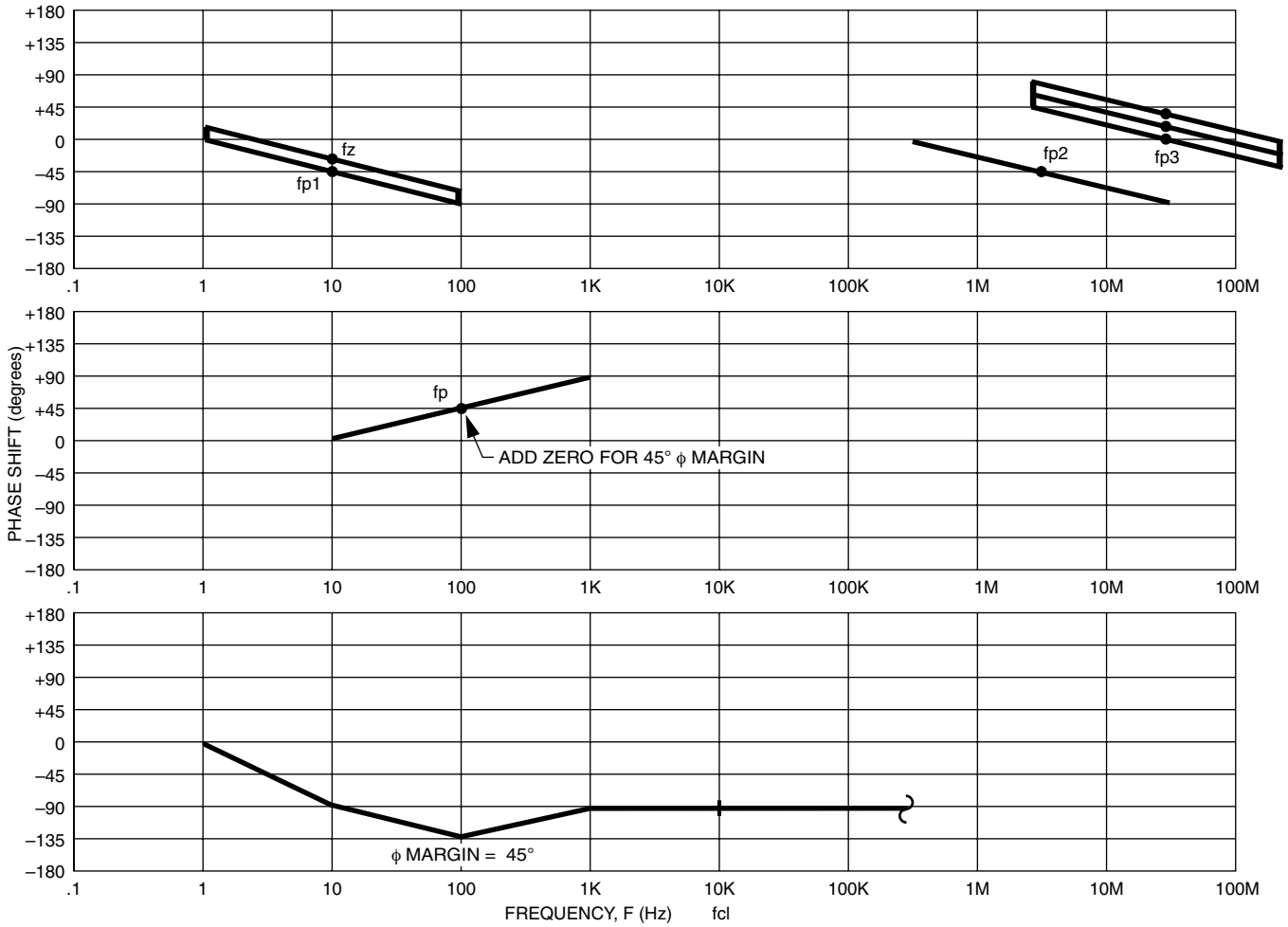


FIGURE 22. FINAL VALUE OPEN LOOP PHASE PLOT FOR STABILITY

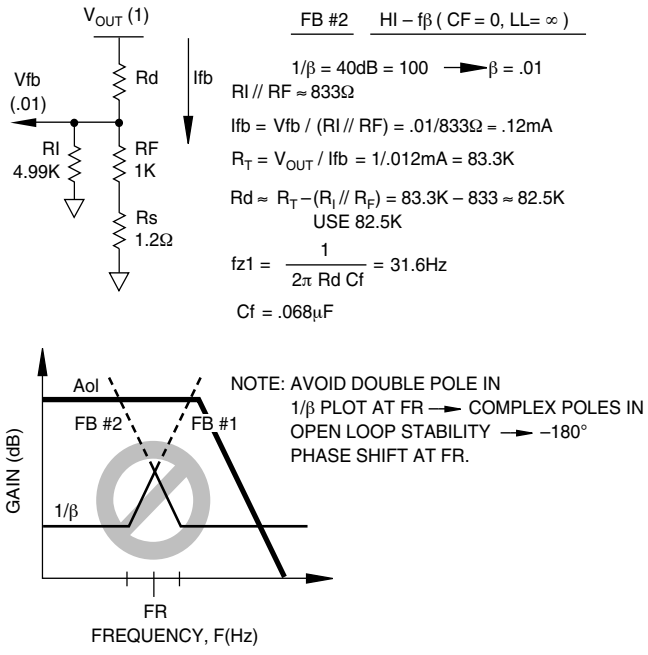


FIGURE 23. FEEDBACK NO. 2 (FB #2) FINAL VALUE CALCULATIONS

5.2.3 AMPLIFIER OUTPUT IMPEDANCE, Ro AND CAPACITIVE LOADING

In the design of power amp circuits, the need often arises for a power amp model with specified output impedance. Most often, this requirement revolves around the need to accurately predict the phase performance of power amp circuits.

Output impedance of any op amp is modified by the feedback network present around the device. In voltage source type circuits, the effect of the network is to reduce the output impedance by a factor equal to the ratio of open loop gain to closed loop gain. In power amps, the net result is an effective output impedance of milliohm levels at frequencies below 1kHz. Wiring and interconnections often create larger impedances than the output impedance of the closed loop power amp. Therefore, output impedance will play a minor role in the phase performance at low frequencies. At high frequencies, reactive load considerations are already addressed by capacitive load specifications given on many power amplifiers.

Within the bandwidth of the amplifier the output impedance of most APEX power op amps appears predominantly resistive. As an output stage drives higher currents, its output impedance changes when compared to the low current or unloaded output impedance. In general, this impedance reduces as current is driven through the output stage.

When compensating circuits with capacitive loading we will use the low current or unloaded output impedance for Ro. This will be the highest value of Ro causing the lowest frequency additional pole which modifies an amplifier's Aol curve when driving a capacitive load. Many designs in the past have verified that compensating for this condition will give the best stability for all conditions when driving capacitive loads.

The following is a list of output impedances for APEX power op amps and boosters.

OP AMP OR BOOSTER	OUTPUT IMPEDANCE
PA01	2.5-8.0 ohms
PA02	10-15 ohms
PA03	25 ohms
PA04	2.0 ohms
PA05	5 ohms
PA07	1.5-3.0 ohms
PA08	1.5K-1.9K ohms
PA09	15-19 ohms
PA10	2.5-8.0 ohms
PA12	2.5-8.0 ohms
PA19	30-40 ohms
PA21, 25, 26	10 ohms
PA41, PA42	150 ohms
PA45	150 ohms
PA51	1.5-1.8 ohms
PA61	1.5-1.8 ohms
PA73	1.5-1.8 ohms
PA81J	1.4K-1.8K ohms
PA82J	1.4K-1.8K ohms
PA83	1.4K-1.8K ohms
PA84	1.4K-1.8K ohms
PA85	50 ohms
PA88	100 ohms
PA89	100 ohms
PB50	35 ohms
PB58	35 ohms

5.2.4 COMPENSATING CAPACITIVE LOADS

There are two main ways to compensate for capacitive loads or two pole Aol curves. The "Feedback Zero" and "Noise Gain" or "Input R-C Network" compensation techniques for capacitive loads will both be discussed.

The "Feedback Zero" technique uses a pole in the 1/β plot (a zero in the open loop phase check for stability or a zero in the Aol β, loop gain, plot) to compensate for the additional pole due to capacitive loading in the amplifier's modified Aol curve. Refer to Figure 25. Note that in Curve 1 there is both a pole and zero in this 1/β plot. The pole is due to the interaction of Rf and Cf. The zero can be found by graphically extending the 1/β plot to zero dB. Remember from previous discussion that an op amp cannot operate at a gain of less than 1 for small signal AC.

The "Noise Gain" compensation technique raises the small signal AC gain of the amplifier to run at a gain that is high enough to ignore the additional high frequency pole in the Aol curve due to capacitive loading. Refer to Figure 25. Curve 2 shows the 1/β plot for noise gain compensation.

Notice in Figure 25 that both Curve 1 and Curve 2 yield a 20 dB per decade rate of closure implying stability; whereas, with just resistive feedback at the given gains the circuits would be unstable with a 40 dB per decade rate of closure.

5.2.4.1 FEEDBACK ZERO COMPENSATION

Figure 26 illustrates a circuit utilizing Feedback Zero Compensation for stability when driving a capacitive load. Figure 27 is our magnitude plot to work with for stability. The following procedure will ensure a logical approach to optimize stability:

STEP 1: Modify the PA88 Aol due to CL. Here we use the output impedance number for the PA88 of Ro = 100 ohms.

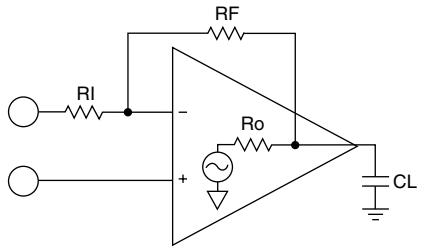
$$fp2 = \frac{1}{2\pi\ Ro\ CL} = \frac{1}{2\pi\ 100\ 159nF} = 10\ kHz$$

The higher frequency poles of the unmodified PA88 Aol must be added into the modified Aol as shown in Figure 26.

STEP 2: Calculate DC β for circuit.

DC β = RI/(RF + RI) = 10K/(316K+10K) = .030674846
DC 1/β = 20 Log (1/.030674846) = 30.26 dB

STEP 3: Plot DC 1/β. Add pole in 1/β plot to compensate for fp2. Ensure fp5 is one-half to one decade away from fcl such that if the modified Aol plot in the real world moves to the left towards lower frequency we will not be back at a 40 dB per decade rate of closure. Note in Figure 27 that the 1/β plot has fp5 and fz1. The feedback network continues to feed back output voltage beyond fcl until we reach 0 dB. Then the 1/β plot flattens out at 0 dB. It is important to include fz1 since it will be a pole in our open loop phase check and will affect phase at frequencies lower than fcl. At fcl loop gain is zero and beyond fcl we are not concerned with phase shift to



UNITY GAIN STABLE AMPLIFIER
BUT: UNSTABLE 40 dB/DECADE WITH CL

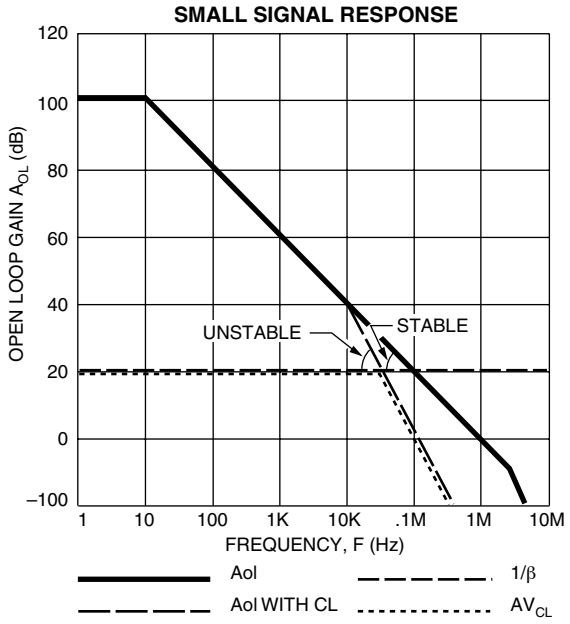
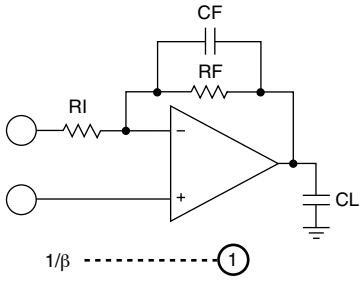
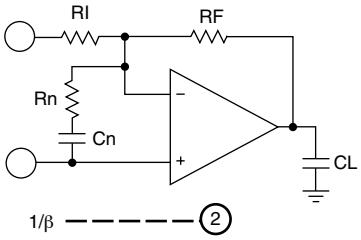


FIGURE 24. CAPACITIVE LOADING



FEEDBACK ZERO COMPENSATION



NOISE GAIN COMPENSATION

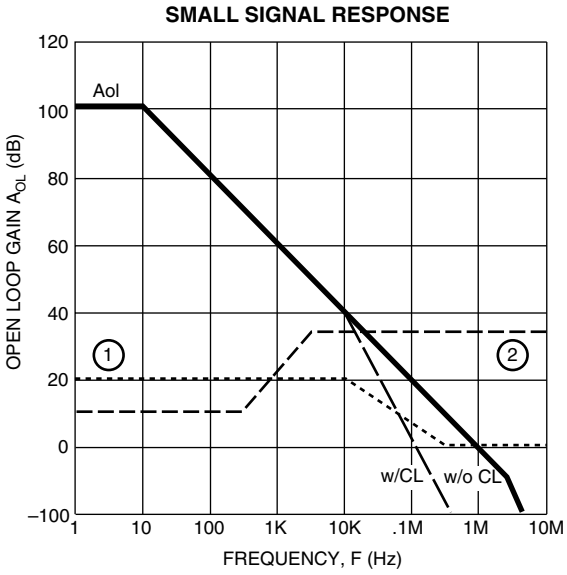


FIGURE 25. CAPACITIVE LOAD COMPENSATION

guarantee stability. Note that the V_O/V_{IN} plot follows the 1/β plot until at which point there is no loop gain and V_O/V_{IN} will follow the Aol curve on down in gain.

STEP 4: Plot open loop phase as in Figure 28. We see we have 67 degrees of phase margin and therefore guaranteed stability.

STEP 5: Once you have chosen CF to get the fp5 you want you automatically set fz1. fz1 can be gotten graphically from the 1/β plot. For those of you who want exact breakpoints, here are the formulae for the 1/β plot in Figure 27.

$$fp5 = \frac{1}{2\pi\ RF\ CF}$$

$$fz1 = \frac{RI + RF}{2\pi\ CF\ RI\ RF}$$

5.2.4.2 NOISE GAIN COMPENSATION

Figure 29 illustrates how Noise Gain compensation works. One way to view noise gain circuits is to treat the amplifier as a summing amplifier. There are two input signals into this inverting summing amplifier. One is V_{IN} and the other is a noise source summed in via

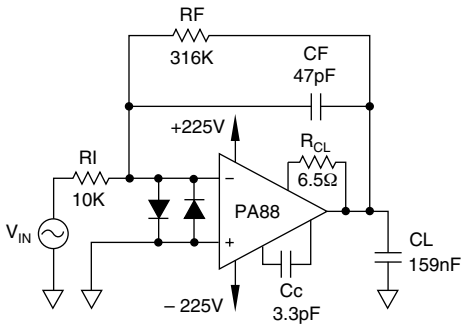


FIGURE 26. FEEDBACK ZERO COMPENSATION FOR CL

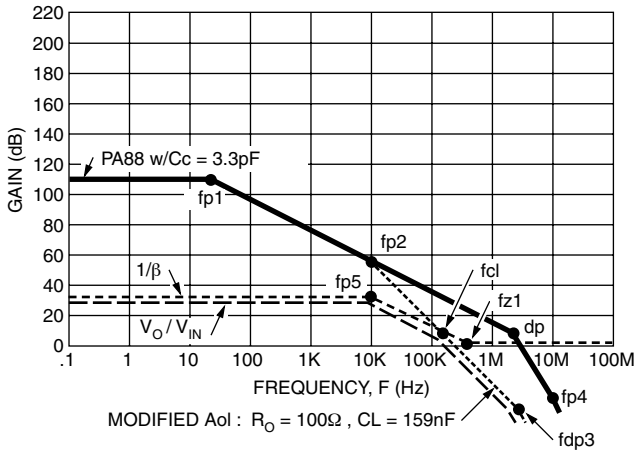


FIGURE 27. FEEDBACK ZERO COMPENSATION FOR CL MAGNITUDE PLOT FOR STABILITY

ground through the series combination of Rn and Cn. Since this is a summing amplifier, V_O/V_{IN} will be unaffected if we sum zero into the Rn-Cn network. However, in the small signal AC domain, we will be changing the 1/β plot of the feedback as when Cn becomes a short and if Rn << RI the gain will be set by RF/Rn. Figure 29 shows the equivalent circuits for AC small signal analysis at low and high frequencies.

Notice in Figure 29 that the V_O/V_{IN} relationship is flat until the Noise Gain forces the loop gain to zero. At that point, fcl, the V_O/V_{IN} curve follows the Aol curve since loop gain is gone to zero. Since noise gain introduces a pole and a zero in the 1/β plot, here are a few tips to keep phase under control for guaranteed stability. Keep the high frequency flat part of the noise gain no higher in magnitude than 20 dB greater than the low frequency gain. This will force fp and fz in Figure 29 to be no more than a decade apart. This will also keep the phase from dipping to -135 since there is usually an additional low frequency pole due to the amplifier's Aol already contributing an additional -90 degrees in the open loop phase plot. Keep fp one half to one decade below fcl to prevent a rate of closure of 40 dB per decade and prevent instability if the Aol curve shifts to the left which can happen in the real world.

Usually one selects the high frequency gain and sets fp. fz can be gotten graphically from the 1/β plot. Once again for completeness, here are the formulae for noise gain poles and zeroes:

$$fp = \frac{1}{2\pi\ Rn\ Cn} \qquad fz = \frac{RF + RI}{(2\pi)\ (Cn)\ (RFRI + RFRn + RIRn)}$$

Figure 30 (see second page following this one) illustrates a circuit utilizing noise gain compensation for stability when driving a capacitive load. Figure 31 is our magnitude plot to work with for stability.

The following procedure will ensure a logical approach to optimize stability:

STEP 1: Modify the PA88 Aol due to CL. Here we use the output impedance number for the PA88 of Ro = 100 ohms

G

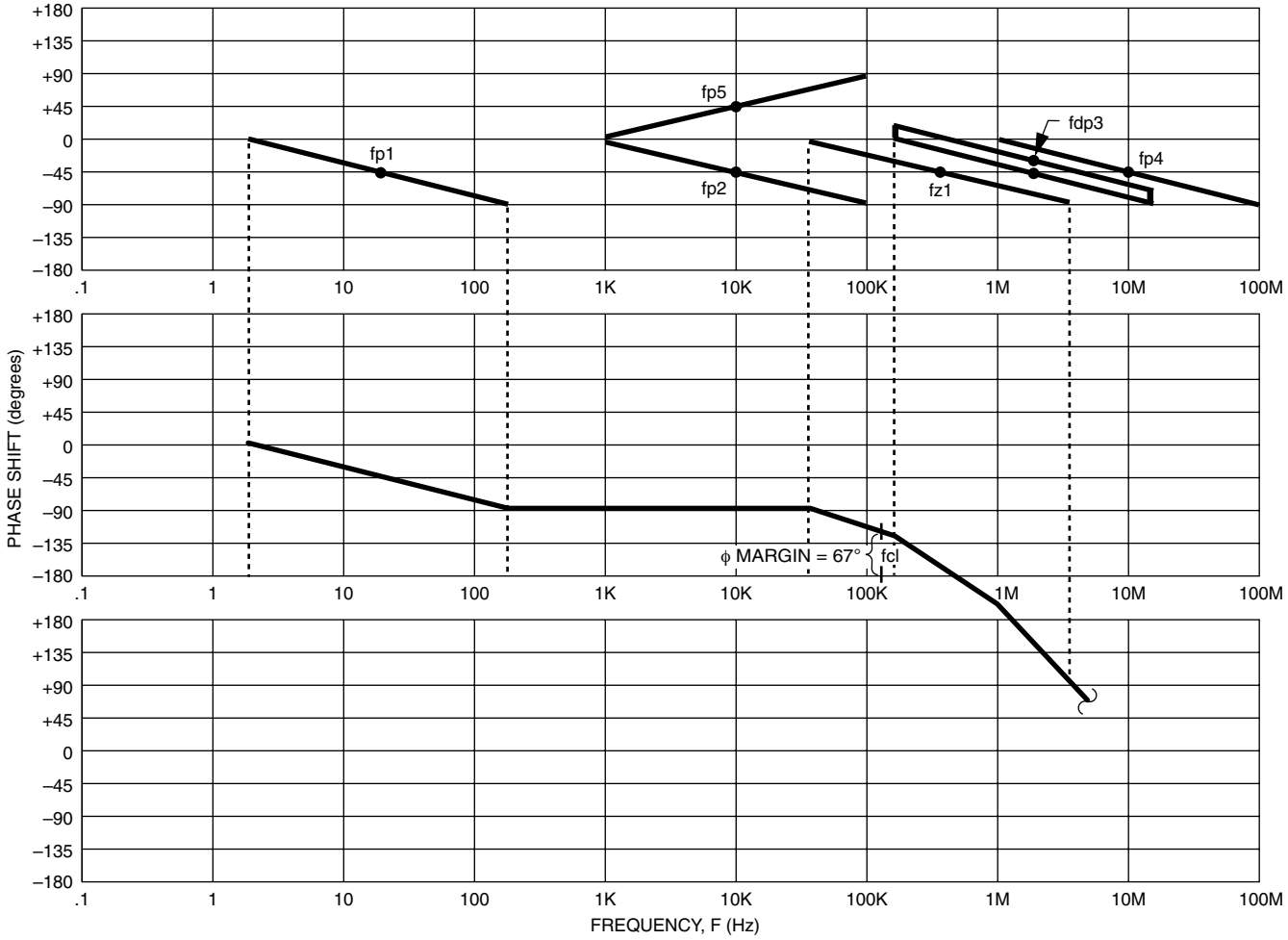
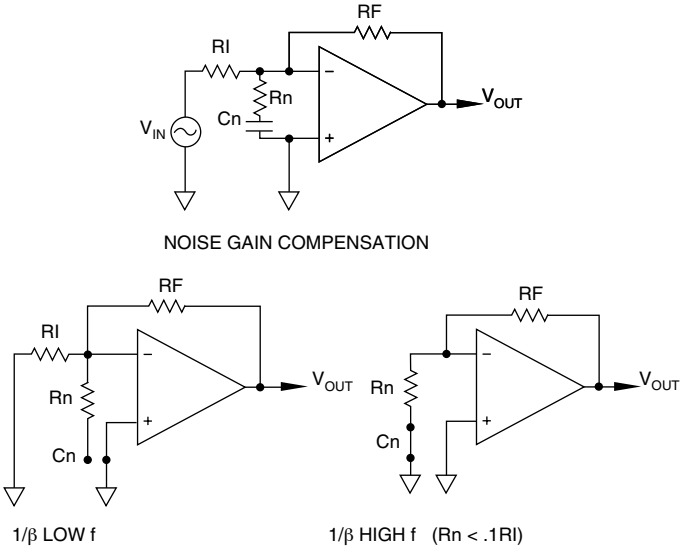


FIGURE 28. FEEDBACK ZERO COMPENSATION FOR CL
OPEN LOOP PHASE PLOT FOR STABILITY



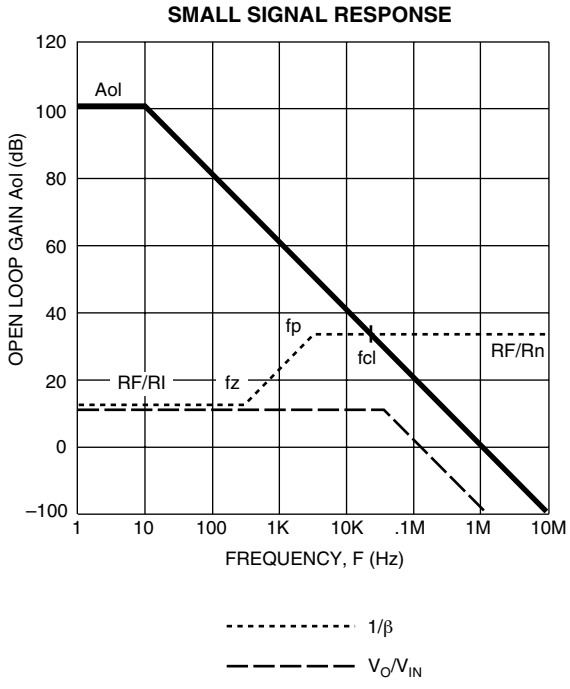


FIGURE 29. NOISE-GAIN COMPENSATION

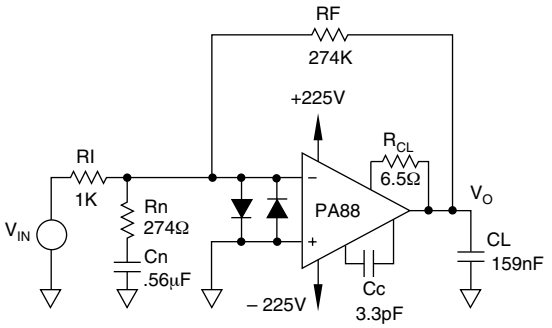


FIGURE 30. NOISE GAIN COMPENSATION FOR CL

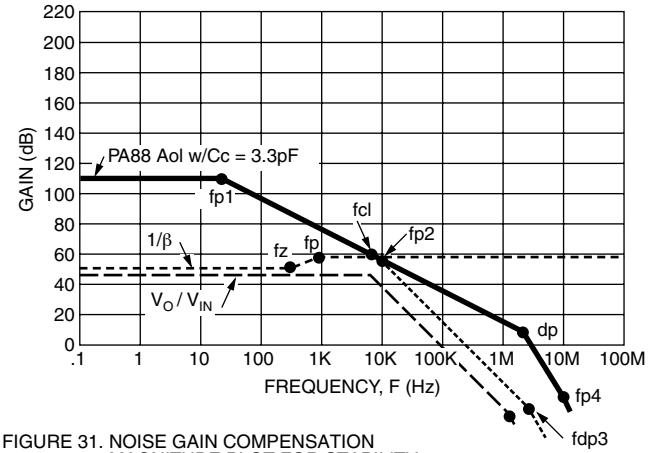


FIGURE 31. NOISE GAIN COMPENSATION MAGNITUDE PLOT FOR STABILITY

$$fp2 = \frac{1}{2\pi\ Ro\ CL} = \frac{1}{2\pi\ 100\ 159nF} = 10KHz$$

The higher frequency poles of the unmodified PA88 Aol must be added into the modified Aol as shown in Figure 31.

STEP 2: Calculate DC β for circuit, Cn is an open for DC.

DC β = RI/(RF+RI) = 1K/(274K+1K) = .003636363
DC 1/β = 20 Log (1/.03636363) = 48.79 dB

STEP 3: Plot DC 1/β. Add noise gain compensation using the hints given above. Things look okay. We have 20 dB per decade rate of closure. fp is a decade away from fcl. High frequency 1/β is less than 20 dB greater than low frequency 1/β, and fz is less than a decade spaced from fp.

STEP 4: Plot open loop phase plot as in Figure 32 (see following page) from the information given in Figure 31. We see from this plot we have 45 degrees of phase margin.

5.3 COMPOSITE AMPLIFIER & STABILITY

* fosc < CLBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—yes

There are design cases where the input characteristics of a power op amp may not be sufficient to meet required specifications. In these cases one can still have the advantages of using the power op amp for linear analog control, but can optimize the front end of the circuit to meet the required specifications. A composite amplifier such as Figure 33 (see following page) will provide a highly accurate 75uV input offset voltage versus the 60 mV input offset voltage of the PA41. In the composite amplifier, the PA41 acts as a booster running in a closed loop gain of 11. The PA41 "booster"" and the OP07 form a new composite amplifier with the feedback from output all the way back to the input of the OP07.

The application in Figure 33 provides an excellent opportunity for us to utilize our knowledge of stabilizing circuits with capacitive loads, as well as acquire new techniques for dealing with stability and composite amplifiers.

The following steps will provide a simple, logical approach to attacking composite amplifier stability problems:

STEP 1: Given specifications:

V_{IN} = ± 2.5 VOLTS
DC ≤ fin ≤ 1.6 KHz
CL = .1μF
V_{OUT} = –/+ 40 VOLTS
± 15 Volts available in system
Input offset voltage ≤ 100 μV

STEP 2: From given specifications determine maximum slew rate needed to track highest frequency output.

S.R. [V/μs] = 2(π)f Vopk ($1x10^{-6}$)
S.R. = 2(π) (1.6K) 40V ($1x10^{-6}$) = .4V/μs

STEP 3: From calculated slew rate and given CL, determine current needed to drive capacitive load.

I = C dV/dt
I = .1 μF (.4V/μs) = 40mA

STEP 4: Select power op amp and host amplifier.

PA41 is the lowest cost power op amp with 60mA of output capability; a slew Rate of 10V/us with Cc =18 pF, and Vsat of 12 volts at 40mA out.

OP07 will provide 75μV of input offset voltage; a slew rate of .17 V/μs; and an output voltage swing of +/-12V from +/-15V supplies. The maximum output voltage swing of the host times the booster gain must meet the desired output voltage swing. Here there is no problem since +/-12V out of OP07 times 11 (booster gain) will yield potential for +/-120V out of the composite amplifier configuration.

The slew rate of the host amplifier times the booster gain should be less than or equal to the booster slew rate. If it is greater than the booster slew rate, the host amplifier can "outrun" the booster during high slew rate demands and consequently the composite amplifier will be running open loop and hence non-linearities and distortion will be uncontrolled.

Host S.R. x Booster Gain = .17/μs x 11 = 1.87V/μs
1.87V/μs < 10V/μs (Booster S.R.)

We will run the booster amplifier in a closed loop gain of 11 as shown in Figure 33 to allow more margin to work with when compensating the capacitive load. We know this from experience in designing many power op amp circuits with capacitive loads on the output.

STEP 5: Draw PA41 Aol curve for Cc = 18pF. The higher frequency poles can be "reverse engineered" from the PA41 open loop phase plot. Note in Figure 34 the pole at 10MHz is labeled "fdp4". This "dp" nomenclature will denote at this frequency there are two poles (double pole).

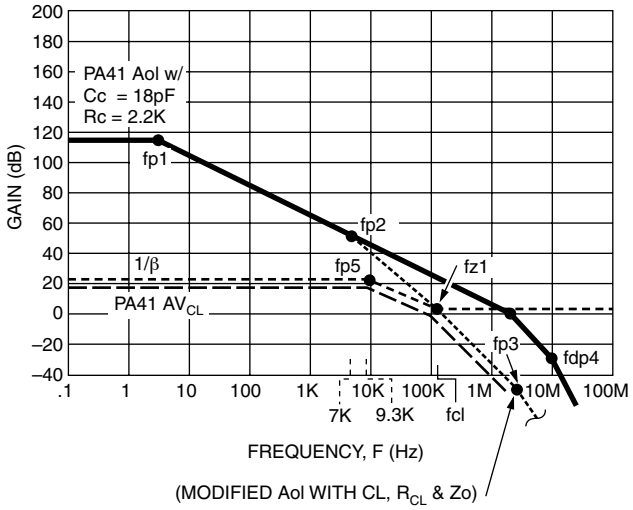


FIGURE 34. POWER OP AMP MAGNITUDE PLOT FOR STABILITY

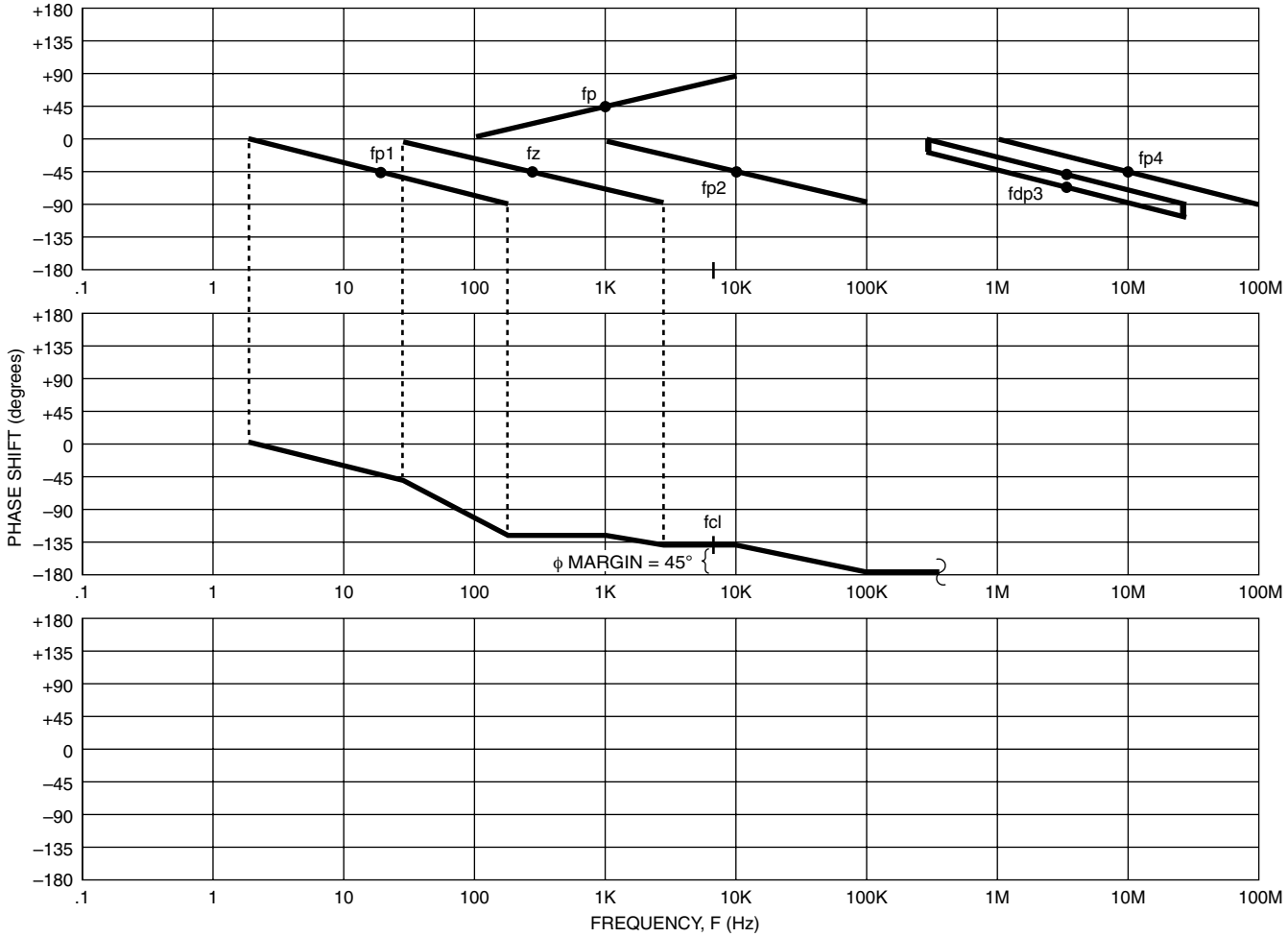


FIGURE 32. NOISE GAIN COMPENSATION
OPEN LOOP PHASE PLOT FOR STABILITY

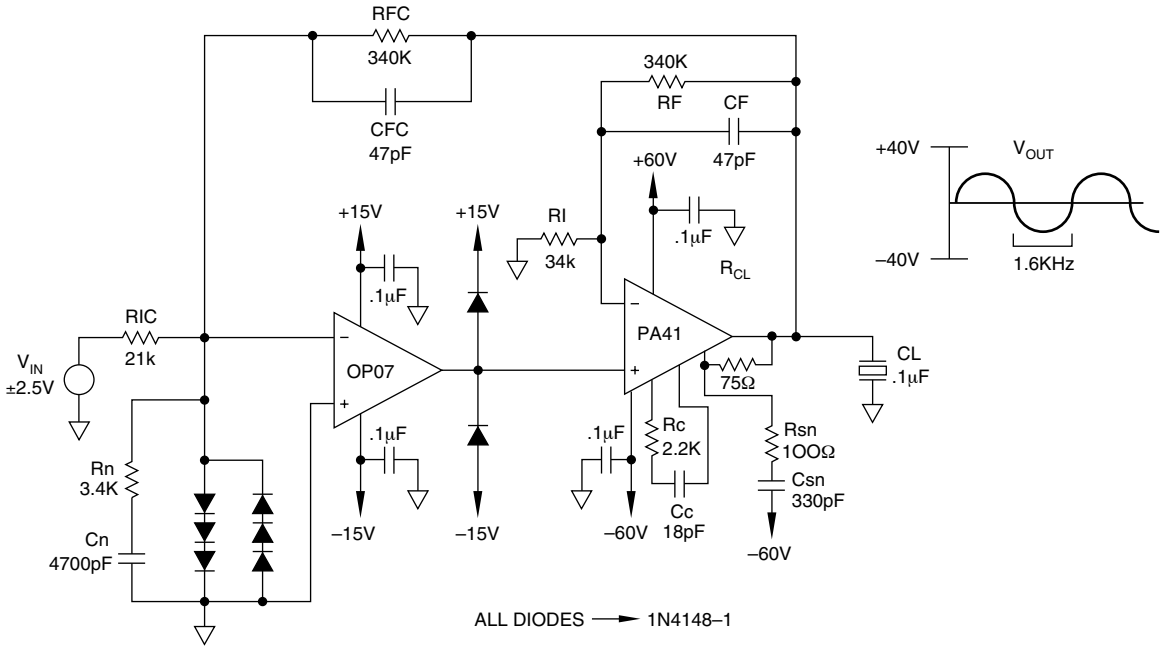


FIGURE 33. PA41 COMPOSITE PIEZO TRANSDUCER DRIVE

STEP 6: Modify PA41 Aol curve for capacitive load of .1μF. PA41 Ro =150 ohms, R^{CL} = 75 ohms. Total output impedance, Zo = 225 ohms.

$$fp2 = \frac{1}{2(\pi)\ Zo\ CL} = \frac{1}{2(\pi)\ 225\ .1\mu F} = 7.07\ kHz$$

fp3 and fdp4 in the modified PA41 Aol are contributions from the original PA41 Aol curve. Refer to Figure 34.

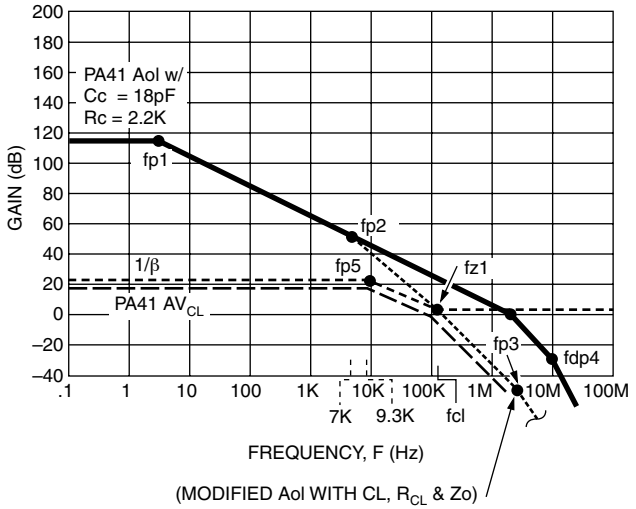


FIGURE 34. POWER OP AMP MAGNITUDE PLOT FOR STABILITY

STEP 7: Compensate PA41 booster for stability with capacitive load. If the booster stage is not locally stable, we have no chance at stabilizing the entire composite amplifier loop. We will add a feedback zero at 9.3 kHz. This will also add a zero in the 1/β plot at fz1. Refer to Figure 34. Now plot the open loop phase plot of the booster amplifier as shown in Figure 35 (see following page). We see 67 degrees of phase margin for the booster amplifier loop.

STEP 8: Create new Composite Aol from OP07 Aol and PA41 AV_{CL}. Remember that if we add log functions it is the same as multiplying gains. If we add the OP07 Aol plot to the PA41 AV_{CL} plot from Figure 34, we obtain the Composite Aol plot as shown in Figure 36.

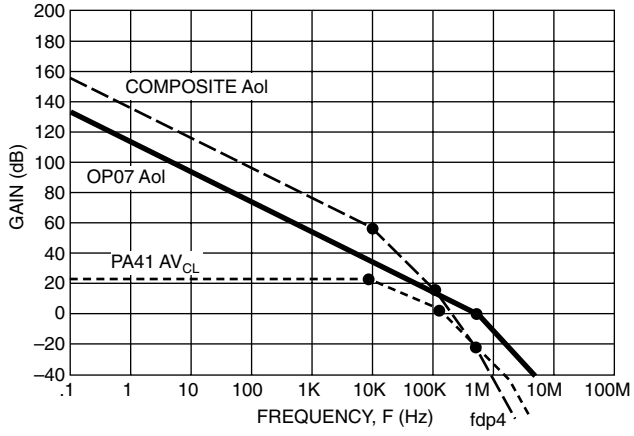


FIGURE 36. COMPOSITE AMPLIFIER Aol MAGNITUDE PLOT

STEP 9: Compensate the composite amplifier for stability. With reference to Figure 37 we have repeated only the Composite Aol for clarity. We see that if we leave just a composite gain of 17, 25 dB, we will have a 40 dB per decade rate of closure and instability. If we try to use just Feedback Zero Compensation the 1/β plot will intersect the composite Aol slope that is 60 dB per decade with a 20 dB per decade slope yielding a resultant 40 dB per decade rate of closure. Our optimum compensation will then use both Noise Gain Compensation as well as Feedback Zero Compensation.

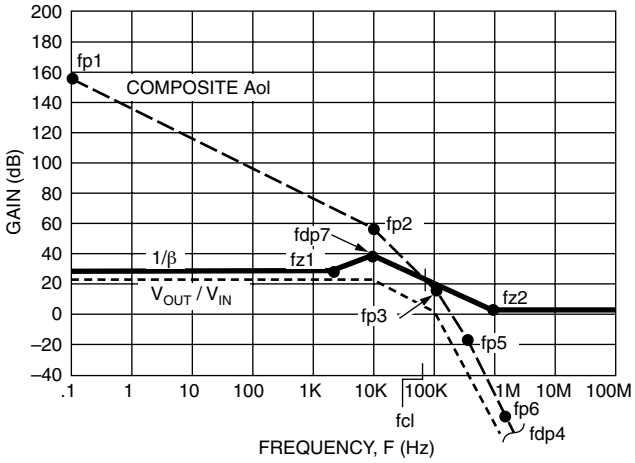


FIGURE 37. COMPOSITE AMPLIFIER MAGNITUDE PLOT FOR STABILITY

We will use Noise Gain to raise the 1/β curve to 40 dB and then use the Feedback Zero Compensation to roll the 1/β plot off to 20 dB per decade slope to intersect the Composite Aol at a resultant rate of closure that is 20 dB per decade. Refer to Figure 37. Notice that the V_{OUT}/V_{IN} relationship is flat until the feedback zero at fdp7 (in the V_{OUT}/V_{IN} relationship this is the pole at f = 1/(2π RFC CFC) begins to roll it off at 20 dB per decade. When the 1/β intersects the Composite Aol, loop gain has gone to zero and V_{OUT}/V_{IN} follows the composite Aol curve on down.

Once again our final stability check is completed by the open loop phase plot for the composite amplifier as shown in Figure 38. (see second page following this one.) The resultant 50 degrees of phase margin guarantees a stable composite amplifier configuration.

P.S. — Refer to Figure 33. The 1N4148-1 diodes on the input of the OP07 provide differential and common mode overvoltage protection from transients through CFC. Piezo elements being electromechanical devices can generate high voltages if shocked mechanically. Output diodes of the OP07 prevent overvoltage transients that occur through CF and shunted through PA41 internal input protection diodes, from damaging the output of the OP07 connected to +input of PA41.

6.0 REAL WORLD STABILITY TESTS

We have devoted much text to discussing how to design stable circuits. Once a circuit is designed and built it is often difficult to open the feedback path in the real world and measure open loop phase margin for stability.

The following Real World Stability Tests offer methods to verify if predicted open loop phase margins actually make it to the real world implementation of the design. Although the curves shown for these tests are only exact for a second order system, they provide a good source of data since most power op amp circuits possess a dominant pair of poles that will be the controlling factor in system response.

6.1 AVcl PEAKING TEST

Figure 39 illustrates the AVcl Peaking Test for measuring open loop phase margin in the real world closed loop domain. From the closed loop Bode plot, we can measure the peaking in the region of gain roll-off. This will directly correlate to open loop phase margin as shown.

6.2 SQUARE WAVE TEST

Figure 40 illustrates the Square Wave Test for measuring open loop phase margin by closed loop tests. The output amplitude of the square wave is adjusted to be 2 Vpp at a frequency of 1 kHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can be compared to the graph in Figure 40 to yield open loop phase margin.

A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use.

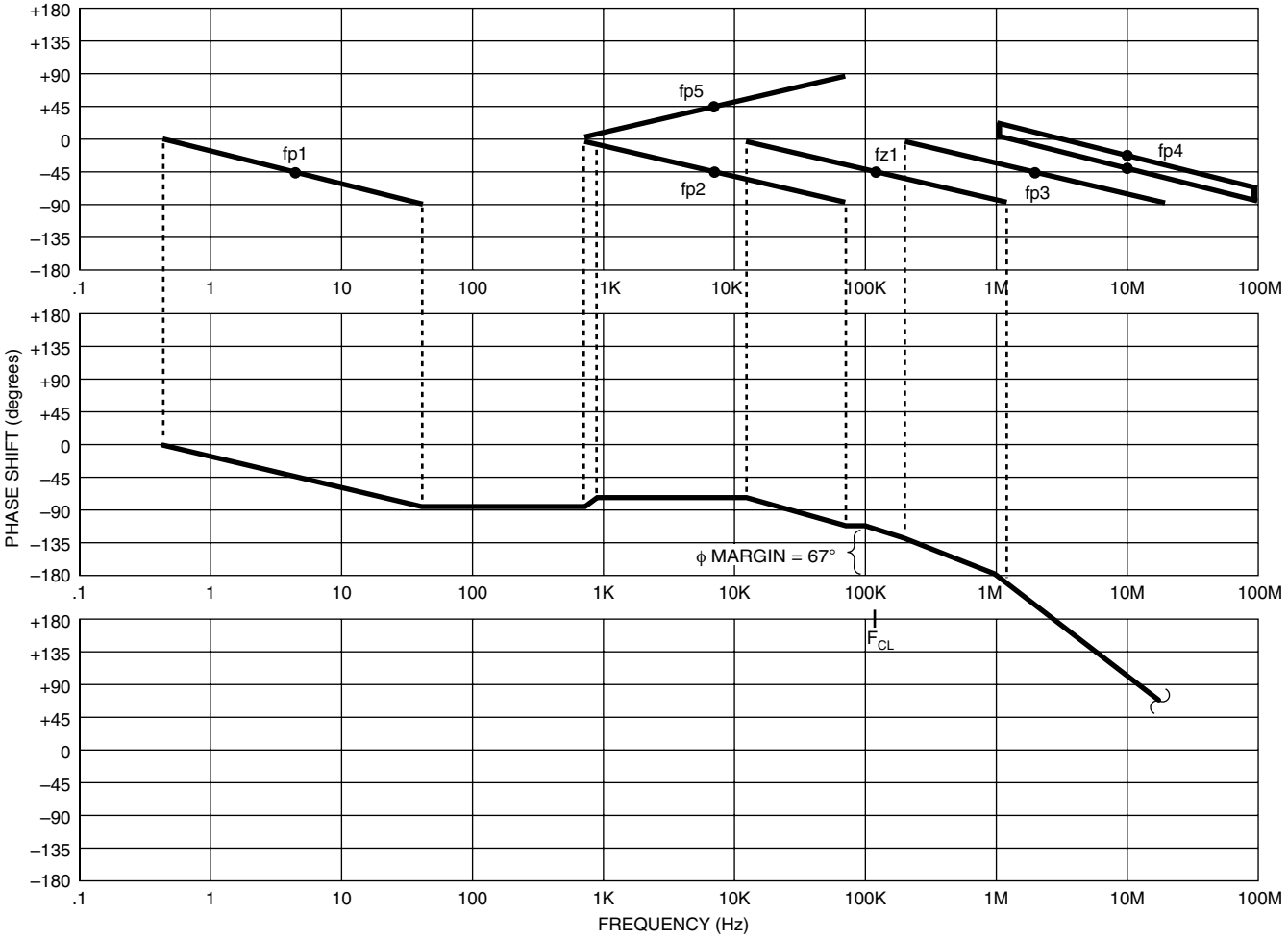


FIGURE 35. POWER OP AMP OPEN LOOP PHASE PLOT FOR STABILITY

6.3 DYNAMIC STABILITY TEST

An expansion on the Square Wave Test is shown in Figure 41(see second page following this one). The Dynamic Stability Test superimposes a small signal AC square wave on a low frequency, large signal AC sinewave to dynamically test the power op amp circuit under all operating point conditions. The resultant ringing on the square wave can be compared to the graph in Figure 40 for relation to open loop phase margin. Note that R1 // R2 in Figure 41 must be much greater than RIN or the input summing test impedances will affect the compensation of the power op amp circuit under test.

7.0 STABILITY TROUBLESHOOTING GUIDE

Figure 42 (see third page following this one) provides a troubleshooting guide for the most common stability problems. The "Probable Cause/Possible Solution Key" gives insight into the origin of the problem and provides guidance as to the appropriate fix.

8.0 FINAL STABILITY NOTE

When you're at your wits end trying to solve an oscillation problem, don't give up because you have it down to an "acceptably low" level. A circuit either oscillates or it doesn't, and no amount of oscillation is acceptable. Apply the techniques and ideas in this Application Note under your worst case load conditions and you can conquer your oscillation problems.

If time is short or you can't see the forest from the trees, APEX would be happy to provide Technical Support via FAX, 602-888-7003, or via the Applications Hotline, 800-421-1865 (USA & CANADA, outside Arizona only). Or call direct, 602-690-8600. More importantly, as we tell all our customers, we would be happy to review your schematic for stability considerations, etc., before you ever build a circuit or even buy a power op amp.

9.0 REFERENCES

1) Frederiksen, Thomas M. : INTUITIVE IC OP AMPS, R.R. Donnelley & Sons, 1984.
2) Huelsman, Lawrence P. : BASIC CIRCUIT THEORY WITH DIGITAL COMPUTATIONS, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1972.
3) Faulkenberry, Luces M. : AN INTRODUCTION TO OPERATIONAL AMPLIFIERS WITH LINEAR IC APPLICATIONS, John Wiley & Sons, New York, 1982.
4) Dorf, Richard C. : MODERN CONTROL SYSTEMS (Third Edition), Addison-Wesley Publishing Company, Reading, Massachusetts, 1980.

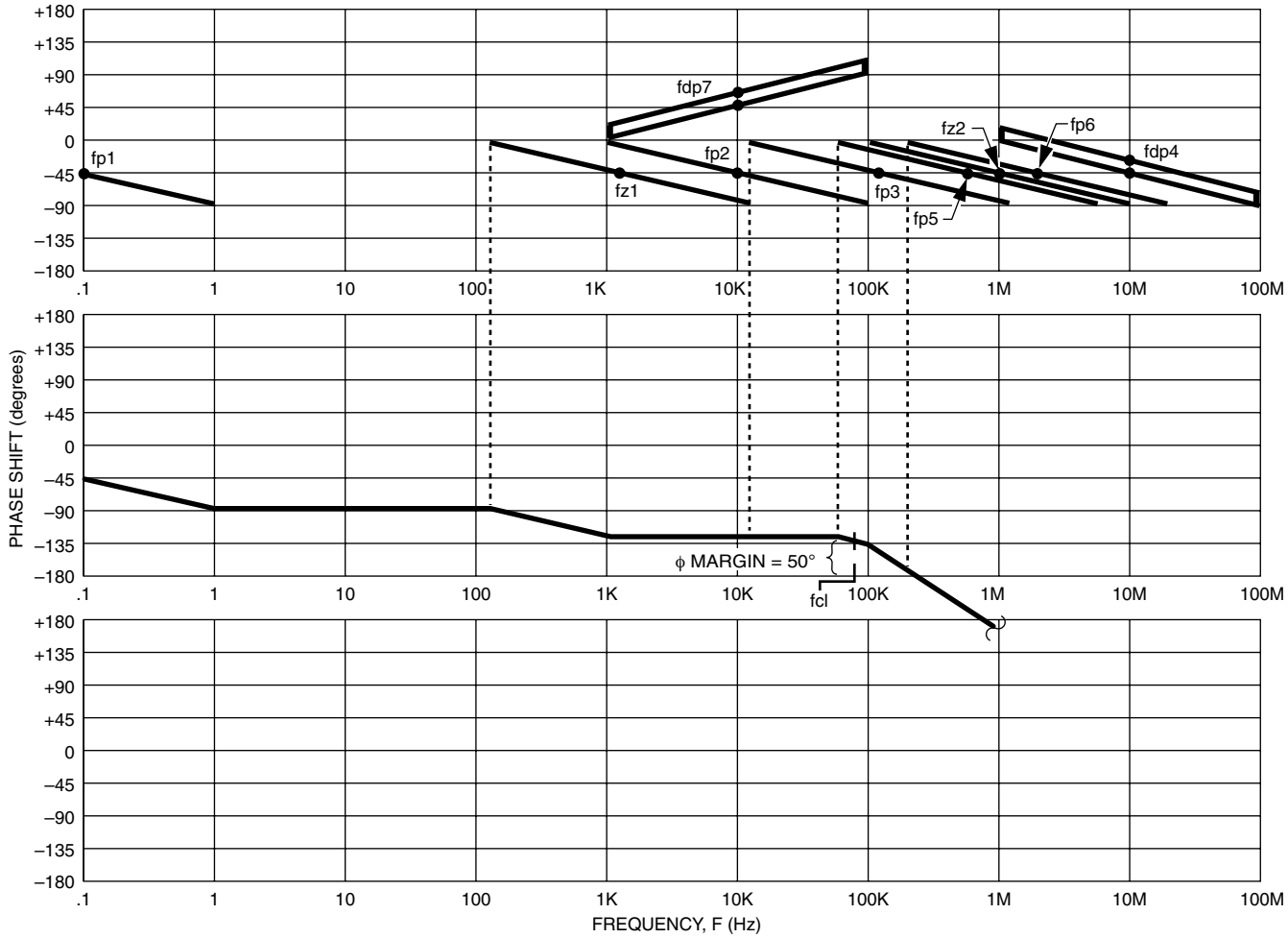


FIGURE 38. COMPOSITE AMPLIFIER OPEN LOOP PHASE PLOT FOR STABILITY

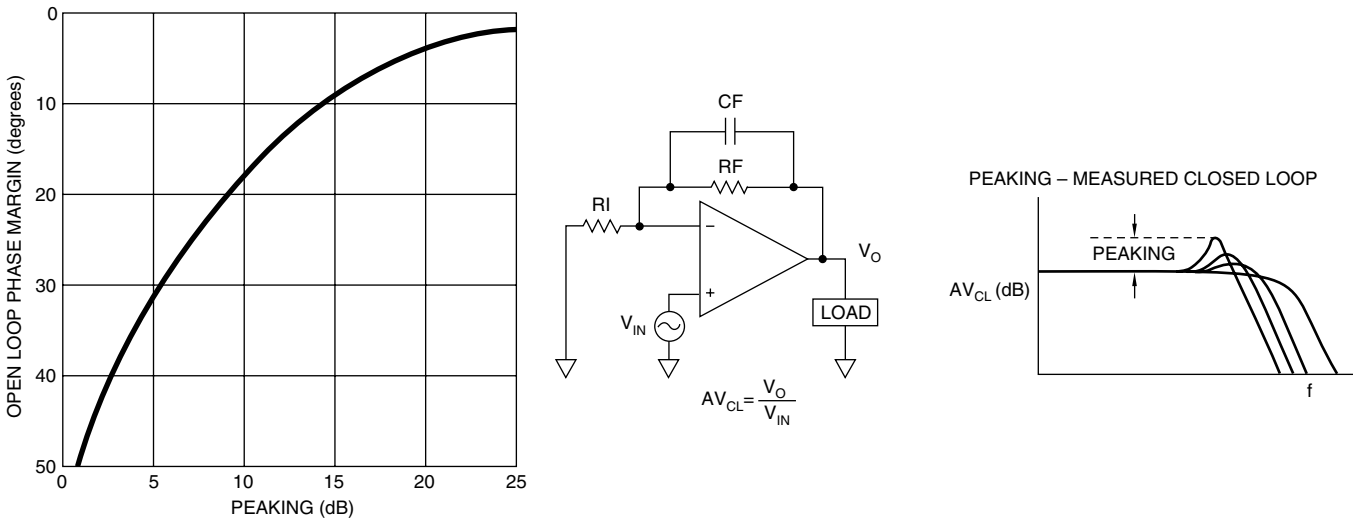
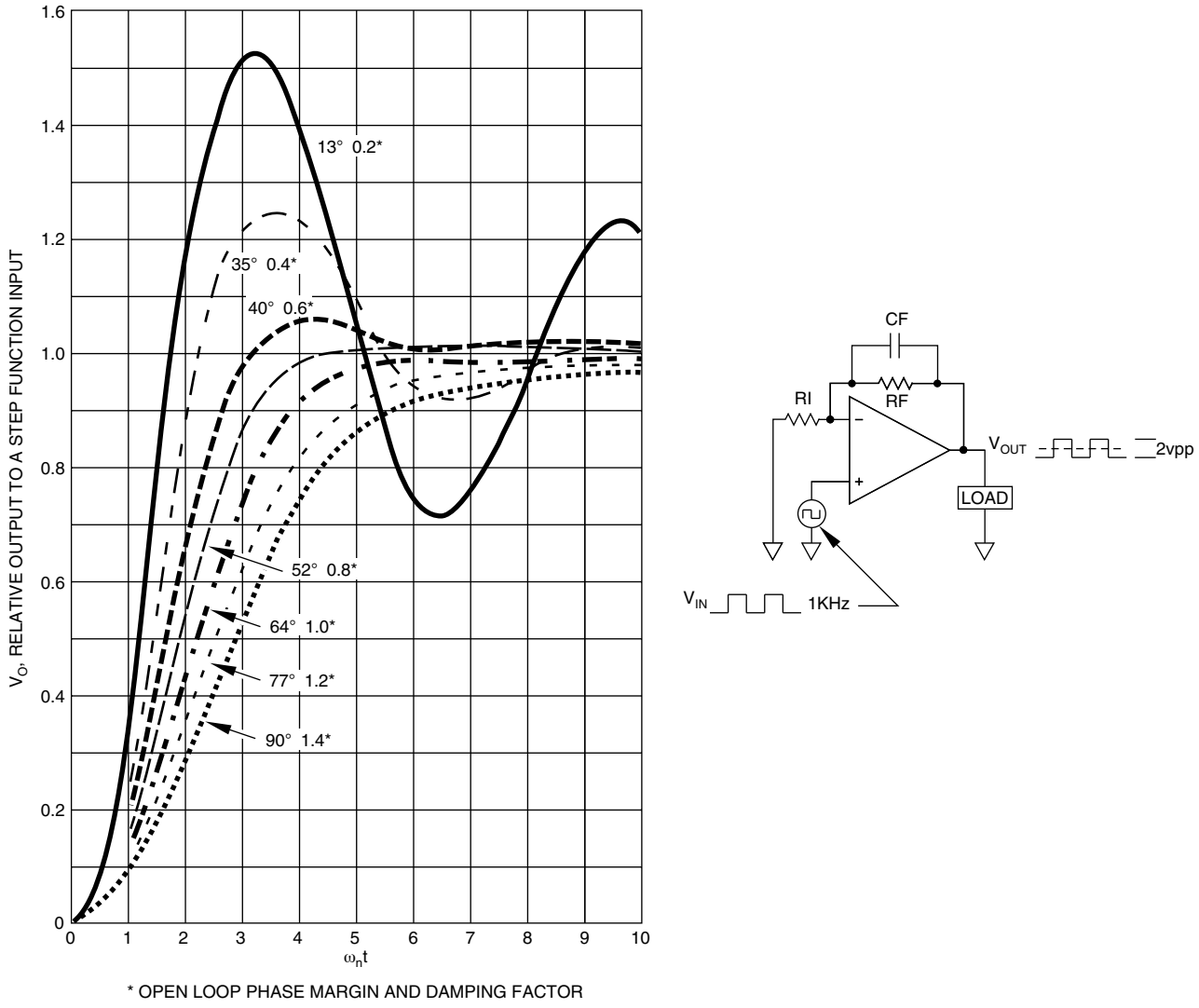


FIGURE 39. AV_{CL} PEAKING TEST



* OPEN LOOP PHASE MARGIN AND DAMPING FACTOR

FIGURE 40. SQUARE WAVE TEST

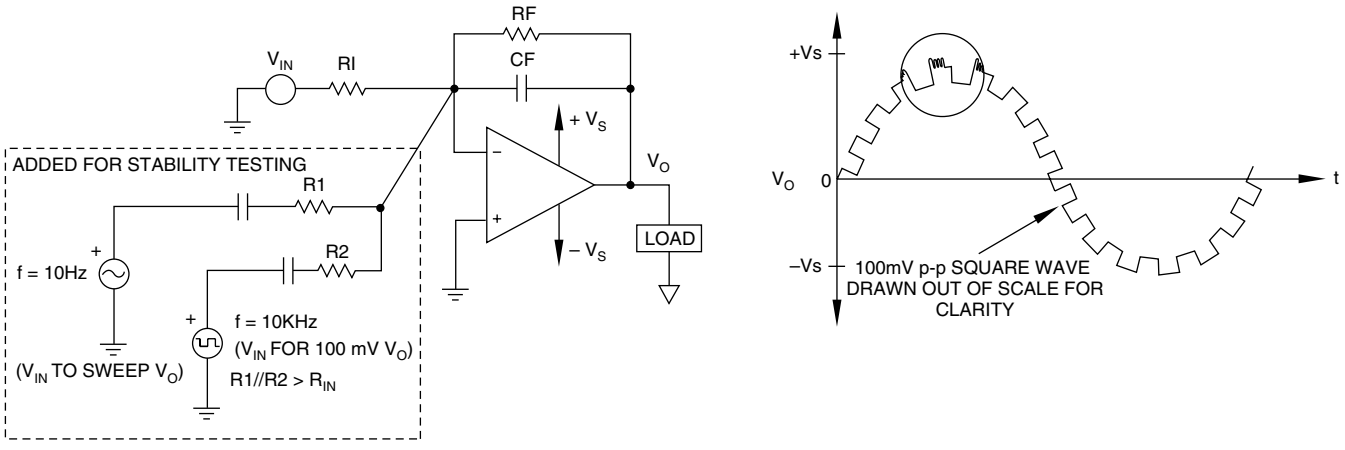


FIGURE 41. DYNAMIC STABILITY TEST

CONDITION AND PROBABLE CAUSE TABLE

Oscillation Frequency	Oscillates unloaded?	Oscillates with V_{IN} = 0?	Loop Check† fixes oscillation?	Probable Cause(s) (in order of probability)
$f_{osc} \leq$ UGBW	N	Y	N	C, D
$f_{osc} \leq$ CLBW	Y	Y	Y	K, E, F, J
$f_{osc} \leq$ UGBW	–	–	N	G, A, M, B
$f_{osc} \leq$ CLBW	N	Y	Y	D
$f_{osc} \leq$ UGBW	Y	Y	N*	J, C
$f_{osc} \leq$ CLBW	Y	Y	N	L, C
$f_{osc} >$ UGBW	N	Y	N	B, A
$f_{osc} >$ UGBW	N	N**	N	A, B, I, H

CLBW = Closed Loop Bandwidth
UGBW = Unity Gain Bandwidth
† See Figure 42A for loop check circuit.
— Indeterminate; may or may not make a difference.
*Loop check (Figure 42A) will stop oscillation if Rn << $|X_{CF}|$ at UGBW.
**Only oscillates over a portion of the output cycle.

KEY TO PROBABLE CAUSE / POSSIBLE SOLUTION

A. Cause: Supply feedback loop (insufficient supply bypassing).
Solution: Bypass power supplies. See Section 2.3.
B. Cause: Supply lead inductance.
Solution: Bypass power supplies. See Section 2.3.
C. Cause: Ground loops.
Solution: Use **"Star"** grounding. See Figure 9.
D. Cause: Capacitive load reacting with output impedance (Aol pole).
Solution: Raise gain or use Noise Gain Compensation network. See section 5.2.4.2.
E. Cause: Inductor within the feedback loop (loop gain pole).
Solution: Use alternate feedback path. See section 5.1.
F. Cause: Input capacitance reacting with high RF (noise gain zero).
Solution: Use CF in parallel with RF. (CF =~Cin). Do not use too much CF, or you may get problem J.
G. Cause: Output to input coupling.
Solution: Run output traces away from input traces, ground the case, bypass or eliminate RB+ (the bias current compensation resistor from +IN to ground)
H. Cause: Emitter follower output reacting with capacitive load.
Solution: Use output **"snubber"** network. See Section 2.5.
I. Cause: **"Composite PNP"** output stage with reactive load.
Solution: Use output **"snubber network."** See Section 2.5.
J. Cause: Feedback capacitance around amplifier that is not unity gain stable (integrator instability).
Solution: Reduce CF and/or increase Cc for unity gain stability.
K. Cause: Insufficient compensation capacitance for closed loop gain used.
Solution: Increase Cc or increase gain and/or use Noise Gain Compensation network. See section 5.2.4.2.
L. Cause: Servo loop stability problem.
Solution: Compensate the **"front end"** or **"servo amplifier."**
M. Cause: Unwanted signals coupling into op amp through case.
Solution: Ground the case.

FIGURE 42. STABILITY TROUBLESHOOTING GUIDE

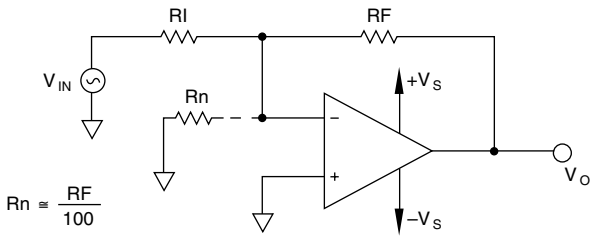


FIGURE 42A. LOOP CHECK CIRCUIT

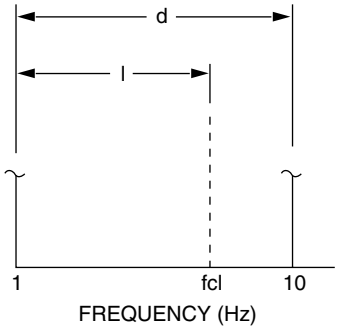
10.0 APPENDIX

This appendix contains some handy tools for plotting magnitude and phase plots for stability analyses. The "Log Scaling Technique" covers an easy way to read exact frequency locations of poles and zeroes from magnitude plots for stability. Included, as well, are blank magnitude and phase plots for copying and using to plot phase and magnitude plots for stability.

One final tip. Once a magnitude plot has been plotted containing the Aol curve and 1/β, it is easy to translate the poles and zeroes to an open loop phase plot for stability. Simply use a light table (ours is very basic — a piece of plexiglass that fits over a 60W incandescent desk light !) to trace the locations of poles and zeroes. Remember poles and zeroes in the Aol curve are poles and zeroes in the open loop phase check for stability. But poles in the 1/β plot become zeroes, and zeroes in the 1/β plot become poles in the open loop phase check for stability.

LOG SCALING TECHNIQUE

When using rate-of-closure graphical techniques it is convenient to measure what frequency fp or fz might be at without detailed calculation. This handy reminder about log scale will give you that power:



$\frac{l}{d}$ = LOG (fcl)

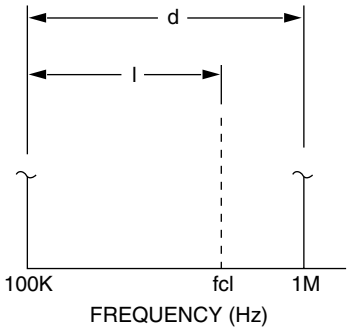
$fcl = LOG^{-1}\left(\frac{l}{d}\right)$

*$fcl = 10^{(l/d)}$

$fcl = 10^{(1.4"/2")} = 5.012Hz$

* This can be used between any decade of frequencies by normalization of scale for 1 to 10.

Definition by example is easiest →
What frequency is fcl below?



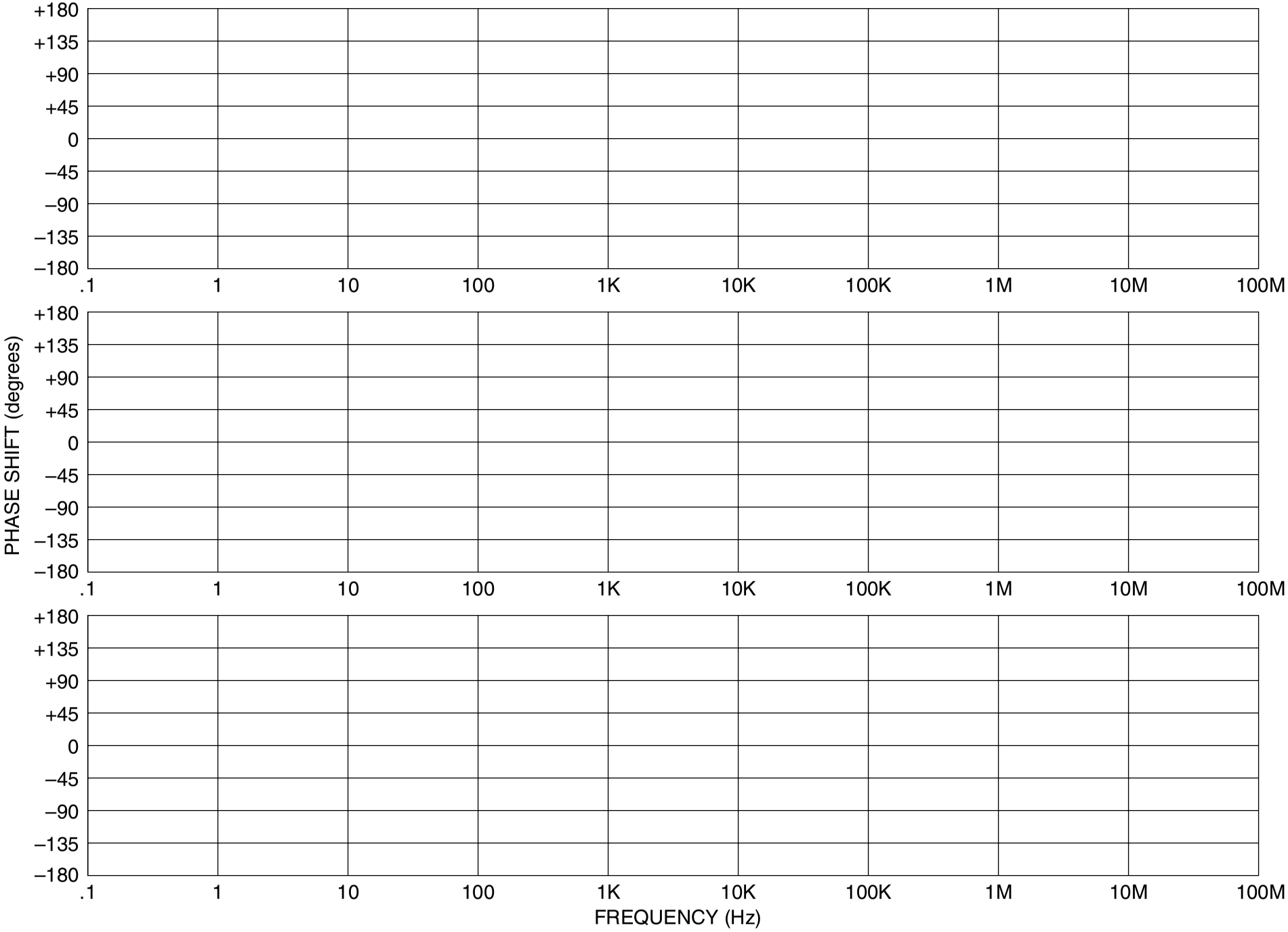
$fcl = 10^{(1.4"/2")} = 5.012Hz$

fcl = 501.2 KHz

Scale is normalized for 1 to 10 by dividing by 100. Answer to fcl is multiplied by 100 to yield final answer in KHz.

G

GAIN (dB)
240
220
200
180
160
140
120
100
80
60
40
20
0
.1
1
10
100
1K
10K
100K
1M
10M
100M
FREQUENCY (Hz)



APPLICATION NOTE 20

POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

1.0 ADVANTAGES OF THE BRIDGE CONNECTION

The bridge connection of two power op amps provide's output voltage swings twice that of one op amp. And it is the only way to obtain bipolar DC coupled drive in single supply applications. Two possible situations where this is an advantage would be in applications with low supply voltages, or applications that operate amplifiers near their maximum voltage ratings in which a single amplifier could not provide sufficient drive.

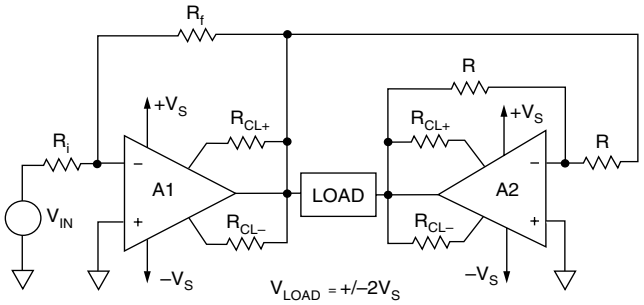
There are other incidental advantages of the bridge connection. It effectively doubles the slew rate, and non-linearities become symmetrical reducing second harmonic distortion in comparison to a single amplifier circuit.

2.0 BRIDGE CONCEPTS AND TERMINOLOGY

Figure 1 is a circuit diagram for the most common variation of a bridge connection using power op amps. To clarify the discussion of this circuit, we'll refer to the left hand amplifier A1 as the master amplifier, and A2 as the slave. The master amplifier accepts the input signal and provides the gain necessary to develop full output swing from the input signal. The total gain across the load will be twice the gain of the master amplifier.

The master amplifier can be set up in virtually any op amp type circuit: inverting or non-inverting, differential amplifier, or as a current source such as an Improved Howland Current Pump.

Always configure the slave as a unity gain inverting amplifier and drive it from the output of the master. Later discussions in connection with Safe Operating Area (SOA) and protection will show the importance of this point.



• PREVENT SOA VIOLATIONS
SET I_{LIM} (A2) > 1.2 • I_{LIM} (A1)

• BANDWIDTH MISMATCH

FIGURE 1. BRIDGE MODE WITH DUAL SUPPLIES (MASTER/SLAVE)

3.0 PROTECTION AND SOA

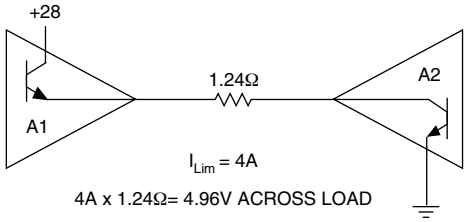
In the following discussions that all general precautions in using power op amps, such as the need for external flyback diodes, transient protection, input protection, etc., must be addressed. These subjects are dealt with in "GENERAL OPERATING CONSIDERATIONS". The following discussion will concern itself only with specific protection issues related to bridge connections.

The concept of driving the slave from the output of the master power op amp is essential for proper protection. The best illustration of the value of that configuration is shown with an example such as Figure 1 where op amps with adjustable external current limiting have been used. With externally settable current limit, set the master to current limit 20% lower than the slave. If the master cannot be reduced, then raise the slave 20% above the master to provide better overall protection than leaving them equal. If a fault occurs in the load such as a short across the load, this will cause the master to current limit and it's output will clip. Since the master is driving the slave, we are effectively clipping the drive to the slave also. Under these conditions the SOA voltage stress will be equally shared between the two amplifiers.

Op amps such as the PA21, PA25, PA03, PA83, PA84, and others, have fixed internal current limits and it is impossible to insure that the master current limits first. This is not a total disaster, it just means that under load fault conditions it cannot be guaranteed that the amplifiers will share the SOA voltage stress, and it must be assumed that one amplifier could bear the entire stress.

Figure 2 is a simplification of output stages to give examples of amplifier stress under a difficult (low resistance such as a stalled DC motor) load condition. The worst case stress must be used where amplifier current limiting cannot be controlled. From this example it can be seen that proper setting of current limiting, when possible, can halve stresses under fault conditions.

Consider each amplifier individually for load analysis, SOA plotting and power dissipation calculations by halving the actual load impedance. Each individual amplifier cannot "see" the amplifier connected to the other end of the load. The other amplifier doubles the voltage, and thus the current, in the load.



4A x 1.24Ω= 4.96V ACROSS LOAD

28-4.96 = 23.0V
23V WORST CASE STRESS

11.5V IF AI CURRENT LIMITS FIRST OR IF CURRENT LIMITS MATCH PERFECTLY

FIGURE 2. EVALUATION AGAINST SOA

4.0 STABILITY

4.1 STABILITY CONSIDERATIONS FOR THE SLAVE

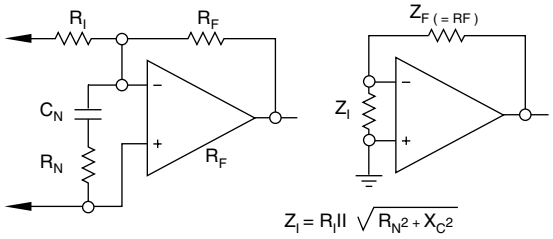
Because the slave amplifier must operate as a unity gain inverter it will be the most critical with regards to stability. Stability enhancement methods invariably involve a tradeoff of frequency response. Fortunately, in the case of the bridge, the master amplifier bandwidth is naturally restricted by operating at higher gains (as well as easing stability considerations for the master). Usually the slave can be compensated such that the resultant circuit will have matching bandwidths on both halves.

Noise gain compensation is the favored method of enhancing stability. Keep in mind that noise gain compensation depends on the non-inverting input being connected to a low impedance (< 0.1Rn). This is not a problem when the non-inverting input can be grounded, as in split supply applications, but it must be considered in single supply applications as the half supply voltage reference point must be a good AC ground. The simplest way to insure a good AC ground is by good bypassing in the form of a tantalum or electrolytic capacitor in parallel with a ceramic capacitor.

4.2 NOISE GAIN COMPENSATION

As shown in Figure 3, a simple way of visualizing the effect of noise-gain compensation is that it raises the apparent gain that the amplifier "sees" (or in other words, reduces feedback) while not affecting the actual signal gain. Select Rn such that Rn > = 0.1Ri to limit the phase shift added by the noise gain compensation. Note from the graph in Figure 3 that, in the example shown, the noise gain compensation

introduces a pole in the feedback path. In this case, at approximately 300 Hz. At 3000 Hz there is a zero in the feedback path. The region between these points should be kept to less than a decade in frequency wide, and a maximum gain difference of 20 dB is implicit in that requirement. In short, noise gain for the slave (which has an uncompensated noise gain of 2, or 6 dB) must be ≤ = 20, or 26 dB.



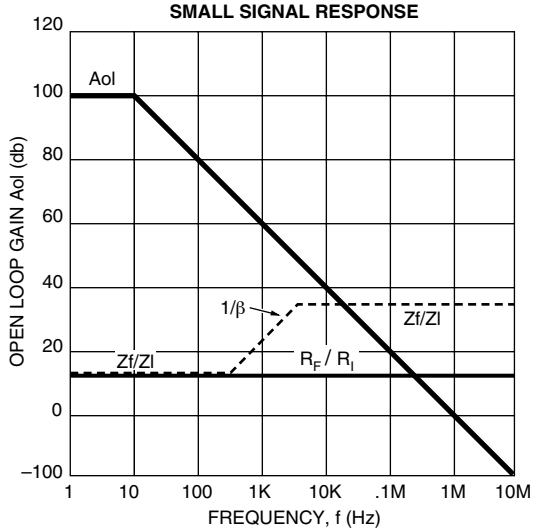


FIGURE 3. NOISE-GAIN COMPENSATION

Another consideration that could be given to the selection of Rn is in regard to frequency response (gain vs. frequency). From Figure 3, the signal gain of a circuit using noise gain compensation rolls off at the point where the noise gain intersects the amplifier Aol. In the case of Figure 3, the normal bandwidth would be about 250 KHz, with compensation about 25 KHz. Without compensation, the slave would have wider bandwidth than the master which is operated at higher gains.

An ideal value for Rn would be one which makes the noise gain of the slave match the signal gain of the master, assuming there is not greater than 20 dB of difference, and the noise gain limit of 26 dB in the slave is not exceeded. In the event the master will also require noise gain compensation for stability, the same principle of matching the noise gain will help to insure matched bandwidths.

The upper corner frequency of the noise gain compensation, or

$$V_N = \frac{1}{2\pi \cdot F \cdot R_N}$$

zero, is determined by Cn such that :

where F= desired zero frequency. Cn should be selected so that the zero is lower than one-tenth the frequency where the high frequency noise gain crosses the Aol.

4.3 STABILITY CONSIDERATIONS FOR THE MASTER

In the case of the master, as well as the slave, capacitive loads should also be considered. The only time the master would need noise gain compensation would be for very low gains, capacitive loading, or when using amplifiers with minimal phase margin such as the PA10 and PA12. Methods of analysis for capacitive loads are discussed in detail in "STABILITY FOR POWER OP AMPS", Application Note 19.

Amplifiers with emitter follower or source follower outputs generally do not have problems with inductive loads. However, collector or drain output amplifiers such as the PA19, PA03 and especially the PA02, with it's local feedback loop in the output stage, can oscillate into inductive loads. Monolithic amplifiers with quasi-complementary output stages, such as the PA25 and PA41 can also be sensitive to inductive loading. Compensate these amplifiers with a series R-C "snubber" from each amplifier output to ground (these are built into the PA21). For power amplifiers the resistors typically run 1 to 10 ohms and capacitors 0.1 to 1.0 μF. For the monolithic PA41 refer to the PA41 data sheet.

5.0 SPECIAL CASES OF THE BRIDGE CONNECTION

5.1 CURRENT OUTPUT

The bridge connection can be a useful tool in a current output circuit. The maximum rate-of-change of current in an inductor, as would be used in a deflection application, is a function of available voltage. For that reason the bridge circuit could double the speed of a magnetic deflection application.

In a current source configuration, the slave remains as an inverting voltage amplifier. Only one amplifier needs to be (or should be) a current source. Of the available ways of configuring an op amp for current output, only the Improved Howland Current Pump is practical for a power op amp bridge.

In Figure 4, the master amplifier is configured as the current pump. R8 is the current sensing resistor. The Improved Howland Current Pump has many special considerations which will not be discussed here, but it will suffice to say that generally the feedback and input resistors should be very closely matched, usually better than 0.1%.

For details on voltage and current waveforms of this circuit, refer to Applications Note 5, Precision Magnetic Deflection.

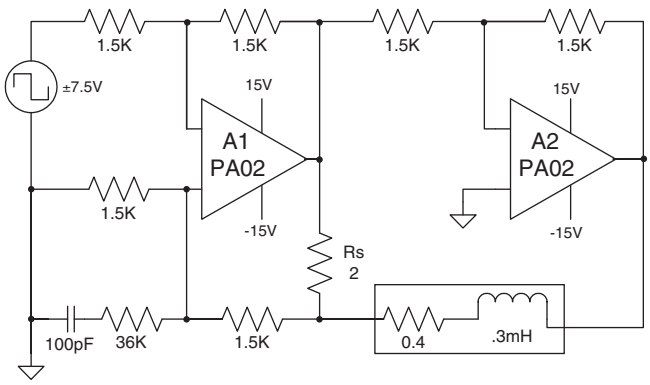


FIGURE 4. ELECTRO-MAGNETIC DEFLECTION (BRIDGE AMPLIFIER)

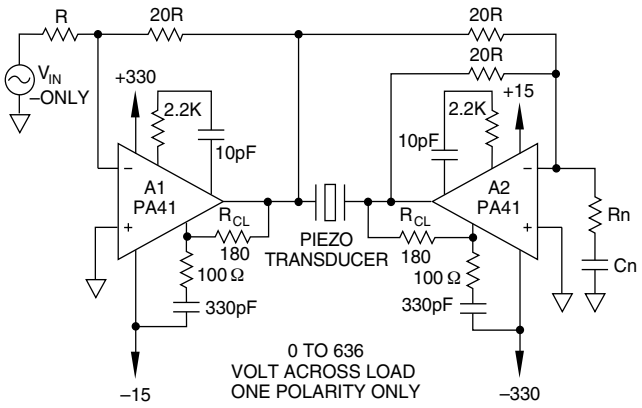


FIGURE 5.

5.2 UNIPOLAR OUTPUT

A particularly powerful way of applying the bridge is in the unipolar bridge. By unipolar, we mean that the output can only swing from 0 to one polarity. Figure 5 is used to illustrate this technique.

The master is a PA41 operating on supply rails of +330 and -15 volts. The slave is operated at +15 and -330 volts. The lower voltage supplies need only be large enough to respect the linear COMMON MODE voltage range requirements of whatever amplifier is used (12 volts in the case of the PA41).

The circuit is designed to accommodate positive going inputs only. At full output swing the master can reach +318 volts while at the same time the slave is at –318 volts for a total voltage across the load of 636 volts. The full dynamic range with regard to the load is 0 to 636 volts unipolar.

The circuit could also be designed such that it accepts negative going inputs and the output of the master swings negative and the slave positive by reversing the supplies.

5.3 SINGLE SUPPLY APPLICATIONS

In the single supply circuit shown in Figure 6, connect the slave's non-inverting input to a pair of equal value resistors connected between supply and ground. This provides a 1/2 supply center operating point for the entire bridge. This point should be well by-passed.

The simplest way to understand the configuration for the master is to delete the resistors Ro, upon which the master becomes the standard circuit for a differential amplifier. The two Rf resistors should be reasonably matched to each other, and the two Ri resistors matched to each other. An advantage of this configuration is that the gain is simply the ratio of Rf/Ri.

Now consider the Ro resistors. Their sole purpose is to provide an equal DC bias on each input and to get the quiescent DC level within the amplifiers COMMON MODE voltage range requirements. This is generally anywhere from 5 to 12 volts inside of each supply rail and is given on all amplifier data sheets. For example, using PA05 on a 90 volt supply, the COMMON MODE VOLTAGE RANGE of the PA05 dictates that the inputs must never come closer than within 8 volts of either rail. So the objective is to select Ro, to set the amplifier inputs to at least 8 but not more than 82 volts, and to stay within these limits under normal input swings. As far as exactly what voltage? It could be argued that half supply is the optimum common-mode point assuming this doesn't cause excessive current to flow in the Ri resistors. In higher voltage applications the range of 5 to 15 volts is more practical though.The PA21 and PA25 are especially easy to use in single supply applications. Since these amplifiers common-mode range includes the negative rail, or ground, their inputs can be driven directly without additional biasing components. The slave must still have it's noninverting input biased at 1/2 supply for proper bridge operation.

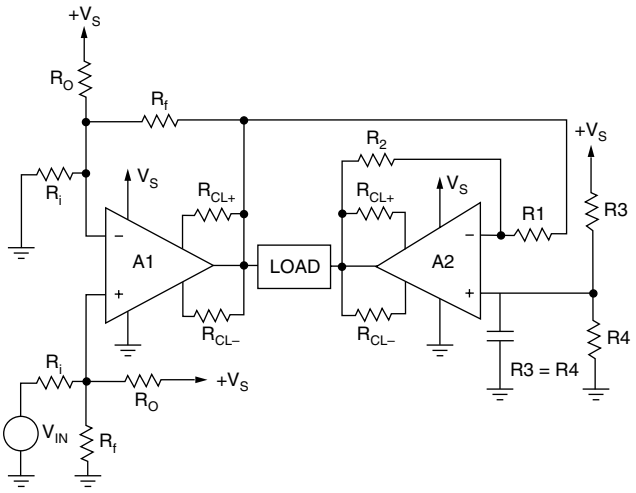


FIGURE 6. BRIDGE MODE WITH SINGLE SUPPLY (OTHER THAN PA21)

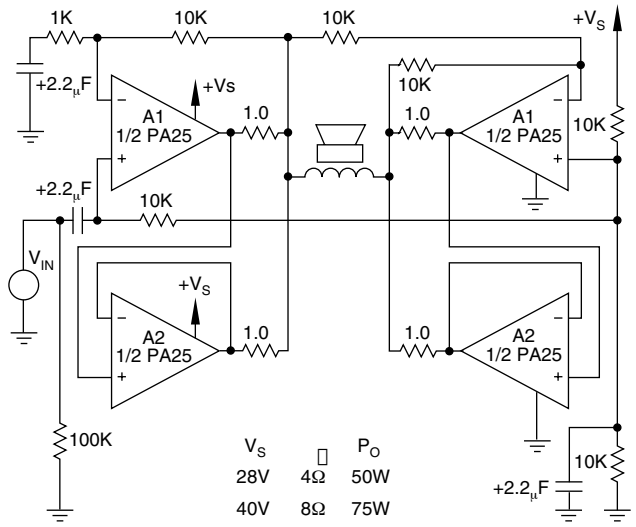


FIGURE 7. SINGLE SUPPLY PARALLEL BRIDGE

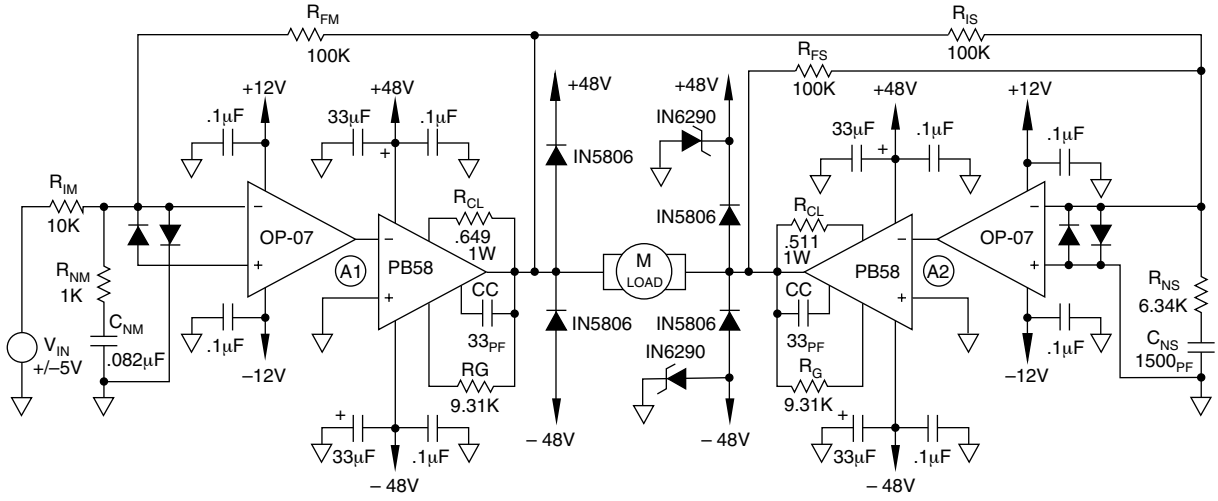


FIGURE 8. PB58A MOTOR DRIVE BRIDGE

5.4 PARALLEL CONNECTION

The bridge circuit can also be combined with the parallel connection of power op amps. Figure 7 shows how substantial audio power outputs can be obtained along with improved reliability since the parallel connection spreads the load among more amplifiers.

Note that in the parallel connection, the pair of paralleled amplifiers are labeled as master and slave also. Because the slave amplifier operates as a unity gain buffer, an amplifier must be selected which has a COMMON MODE voltage range that exceeds its output voltage swing capability. If this cannot be done, configure the slave as a differential amplifier with 4 equal valued and closely matched resistors.

Stability can also be a problem with the slave in the parallel amplifier. A resistor may have to be inserted in the feedback to allow for the use of noise gain compensation. (Noise gain compensation does absolutely nothing when placed across the inputs of a unity gain buffer with no series resistance in the feedback path)

5.5 BRIDGES USING POWER BOOSTERS

A bridge circuit using the PB50 or PB58 would require a composite amplifier for both master and slave. The composite amplifier is not an optimum configuration to operate at unity gain when stability is considered. Use noise gain compensation to establish an adequately high noise gain at high frequencies. Note that observing the criteria previously discussed regarding noise gain would typically dictate that the noise gain for the slave be ≤ 26 dB (Gain = 20). See Figure 8 for a bridge circuit using power boosters.

APPLICATION NOTE 21

POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

1.0 SINGLE SUPPLY OPERATION INTRODUCTION

Single supply operation of power op amps is most often done out of necessity. Examples of such applications are battery powered applications or circuits operating from vehicular power systems.

Single supply operation improves the efficiency of power supply usage. In split supply applications, current is drawn from only one supply at a time, with the opposite supply sitting idle unless bridge circuits are used.

This application note deals exclusively with applications operating off of positive supplies as this occurs 95% of the time. Negative supply principles are identical except for the reversal of polarity.

2.0 RESTRICTIONS OF SINGLE SUPPLY OPERATION

2.1 COMMON-MODE RESTRICTIONS

Keeping op amp inputs biased to within their linear common-mode voltage range is the most important requirement in single supply circuits. The actual value required varies for each amplifier model, and is described in individual model data sheets under SPECIFICATIONS, COMMON MODE VOLTAGE RANGE. DO NOT USE the specification given in the ABSOLUTE MAXIMUM RATINGS block of the data sheet.

2.2 LOAD CONNECTION TO GROUND

There will be several options available for load connection, as shown in Fig. 1. The first option shown in Fig. 1A, is a load connected to ground. Obviously only positive going outputs are possible. Note that when the output voltage the load "sees" is near zero, the amplifier considers its output to be swung to its negative rail.

Note also that amplifiers have limits as to how close they can swing to either rail. So the output for the grounded load can never actually go to zero. It has been observed that substantial current is available under these non-zero conditions, and that the amplifier has full source and sink capability. As an example, a PA12 in a single positive supply will swing as low as 2.5 volts on the output. If a load is connected from output to ground, even with the amplifier overdriven in a negative direction, it will supply substantial positive current, on the order of amps, and up to the current limit, into the load.

2.3 BRIDGE LOAD CONNECTION

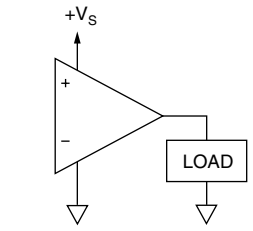
The bridge load connection using two amplifiers, as shown in Fig. 1B, permits bipolar swings across the load. For DC coupled loads this is the only practical way to obtain bipolar swings. Note that the bridge effectively doubles the gain of the circuit.

2.4 LOAD TO HALF SUPPLY

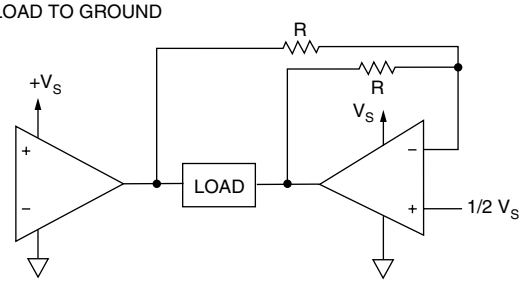
Bipolar drive is possible if the load can be referred to a point at half supply, as in Fig. 1C. This is usually not practical, nor efficient, as the half supply point must have the current capacity to support the load requirements. It might be possible to use a second power op amp as a high current source and sink regulator for this point, but this second op amp would be much more efficiently utilized as the second half of a bridge.

2.5 CAPACITIVE COUPLED LOAD

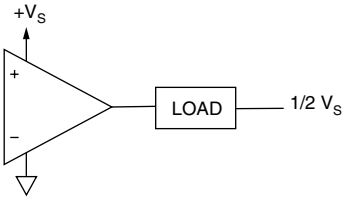
In applications such as audio, it is possible and often desirable to AC couple the load with a capacitor. A simple series capacitor allows driving a ground connected load, as in Fig. 1D. An alternative is to connect the ground side of the load to two large electrolytics, as in Fig. 1E. The only possible advantage of Fig. 1E is the possible reduction of turn-on "pop" in circuits where this may be a problem.



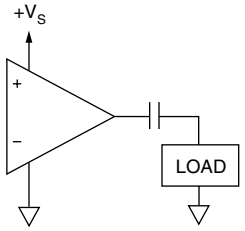
A. LOAD TO GROUND



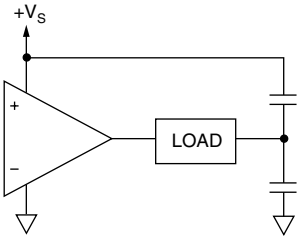
B. BRIDGE



C.1/2 SUPPLY



D. AC COUPLED SINGLE CAP



E. AC COUPLED DUAL CAP

FIGURE 1. LOAD CONNECTION OPTIONS

3.0 CIRCUIT TOPOLOGIES

3.1 UNSYMMETRICAL SUPPLY

Oddly enough, the first option that should be considered is to not use a single supply. Many applications such as those using high voltage amplifiers require a single large high voltage supply and unipolar

output swings. This is to allow incorporation into systems which already have lower bipolar supplies such as ±15 or ±12 volts present. Should this be the case, then use the –15 or –12 volt supply on the negative rail of the op amp (more than a few high voltage applications have large negative supplies along with 12 or 15 volt bipolar supplies).

As shown in Fig. 2, as long as the small supply is large enough to accommodate the common-mode requirements of the amplifier over the range of normal inputs, then no other additional components are required.

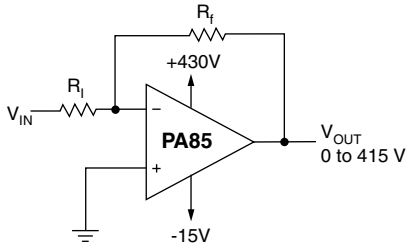
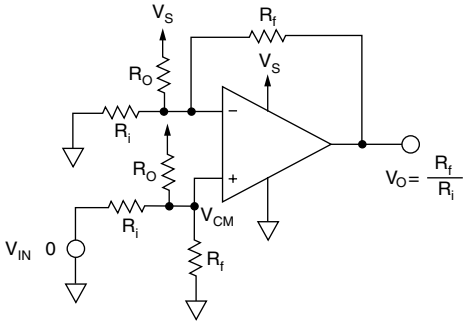


FIGURE 2. UNSYMMETRICAL SUPPLIES

3.2 DIFFERENTIAL CONFIGURATION

The most universally useful single supply circuit is the differential configuration shown in Fig. 3. This topology makes it possible to set the gain simply as the ratio of R_F/R_I where each R_F pair and R_I pair are matched to each other. It is feasible to use the circuit either non-inverting or inverting, but keep in mind that noninverting will accommodate inputs which go positive only with respect to ground, and non-inverting negative only with respect to ground. Also note that the R_O pair must be closely matched to each other.



For $V_{IN} = 0$:

$$V_{CM} = \frac{V_S \ (R_i//R_f)}{R_O + (R_i//R_f)}$$

$$V_{CM\Delta} = \frac{V_{IN} \ (R_O//R_f)}{R_i + (R_O//R_f)}$$

For $V_{IN} > 0$:

$$V_{CM} = V_{CM} @ V_{IN} = 0 \ + V_{CM\Delta}$$

FIGURE 3. SINGLE SUPPLY NON-INVERTING CONFIGURATION

The R_O resistors provide the input common-mode biasing to keep the amplifier linear. An advantage of this method is that (assuming adequate resistor matching) the output would be unaffected by variations in power supply voltage. Normally this inherent supply rejection is desirable, but in the case of the bridge amplifier, this could be a problem since the slave of the bridge is referred to a voltage divider operating from supply voltage. That divider is subject to supply fluctuations, and if the master amplifier of the bridge was equally subject to such fluctuations, it would appear as a common-mode signal across the load and be rejected.

R_O needs to be selected to satisfy common mode voltage requirements, and it turns out this encompasses a wide range of acceptable values for any given circuit. The designer is confronted with the question of just exactly what common mode voltage to set the inputs to. It could be set anywhere within the common mode range, but there will be some practical limitations even within that range.

To illustrate, assume the use of a PA85 with +450 volt supplies. R_O can be selected for anything from 12 volts to 438 volts for linear operation. It could be argued that the ideal value is half supply, or 225 volts, but such a selection would require unreasonably large values for R_i to keep currents within reasonable values. A very large R_i would require an even larger R_F, and the net overall impedance would be so high that stray capacitance and amplifier input capacitance would create enormous bandwidth and stability problems. For high voltage applications, minimum values such as 12 to 15 volts of common mode biasing are easier to accommodate.

When selecting R_O, consider it part of a voltage divider where the ground leg of the divider is the parallel resistance of R_F and R_I. Using that assumption, at full negative input voltage swing in conjunction with full theoretical negative output swing of zero, you will be designing to meet common mode requirements. Dynamically, the inputs will only move positive from this point, simplifying worst-case analysis to double checking the most positive excursion. R_O selection can be aided with the following equation:

$$R_O = \frac{(V_S - V_{CM})}{\left(\frac{V_{CM}}{R_I \,||\, R_F}\right)}$$

V_{CM} is the desired common mode voltage. Once a value is settled on for R_O and the common mode bias point, it should be rechecked over the expected range of input signal values to verify common mode restrictions are met dynamically and readjusted if necessary. Also consider that part of the R_O current flows in R_I and through the source driving the input. The source must be able to accommodate this current.

The differential configuration is so useful that in section 7.0, several design examples will be explored. Appendix A outlines a procedure for the design of this circuit.

4.0 EXPANDED TECHNIQUES

4.1 BRIDGE CONNECTION

The bridge connection shown in Fig. 4 uses the differential configuration for the master, A1 amplifier, and a unity gain inverter for the slave, A2 amplifier. The slave non-inverting input is referred to a point on a divider at half supply voltage. Since this divider is referred to the supply, there will be susceptibility to power supply variation. Note that the zero output point is defined as the point where both amplifier outputs are equal, and this point is set by the non-inverting input of the slave.

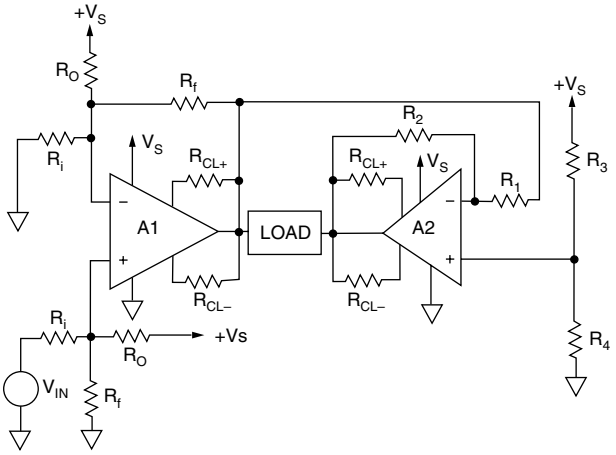


FIGURE 4. BRIDGE MODE WITH SINGLE SUPPLY OTHER THAN PA21

The preferred way of improving the bridge circuit tolerance to power supply variations would be to regulate the half supply point. In the event this is not possible or desirable, Fig. 5 shows a bridge topology that reduces sensitivity to supply variations. The ratio of R2/R1 should be ratio matched to the ratio of R7/R8. Note that gain of A1 will be:

$$A_V = ((R4/R3)+1) \ * \ (R2/(R2+R1))$$

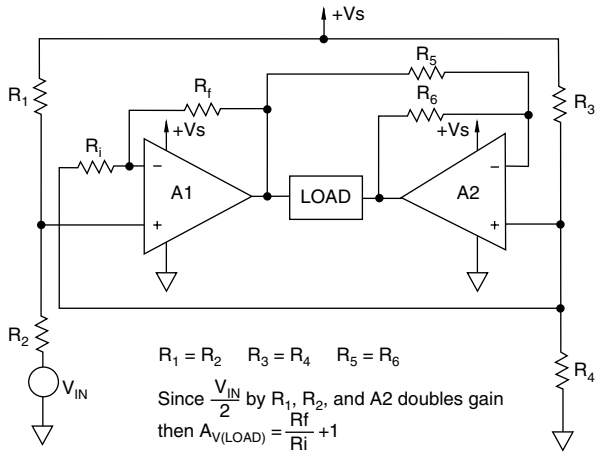


FIGURE 5. MODIFIED SINGLE-SUPPLY BRIDGE FOR IMPROVED SUPPLY REJECTION

Or, consider that while R1/R2 attenuate the input signal by half, and the bridge circuit effectively doubles circuit gain with respect to the load, then A_V is equal to the non-inverting gain of A1, or R_F/R_I+1.

The AC coupled bridge is a special case of the single supply bridge amplifier circuit, and is especially useful for audio where a stable DC operating point is desirable. Fig. 6 depicts such a circuit. Note that both non-inverting inputs use the half supply point as a bias reference. C1 AC couples the input signal. C2 blocks the DC ground path in the feedback loop insuring a unity gain for A1 at DC.

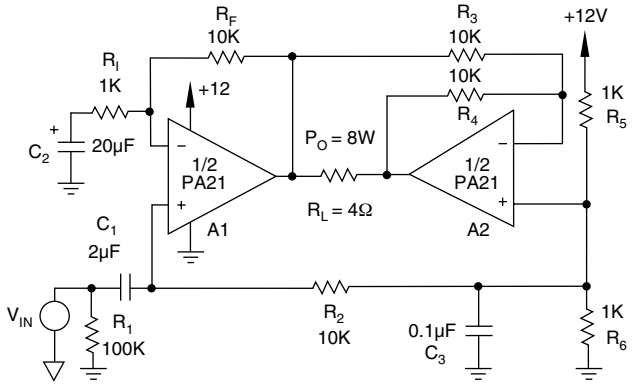


FIGURE 6. AC COUPLED BRIDGE

4.2 CURRENT OUTPUT CONFIGURATION

Any voltage to current configuration is possible in the single supply environment, as long as common mode restrictions are met. The floating load current source will be restricted to unipolar outputs although the output cannot swing to zero current. Of course a bridge topology has many benefits including bipolar output, the ability to deliver zero current, and more voltage available to the load. In magnetic deflection applications, the higher voltages make for faster current transitions.

Since the Improved Howland Current Pump resembles a differential amplifier, it easily lends itself to single supply applications. The only modification will be the addition of the R_O common mode biasing resistors. The Howland is subject to wide dynamic range variations on both input and amplifier output with an infinite number of possibilities when various gains are factored in. Suffice to say the designer must analyze input common mode values at the four extremes of dynamic range:

1. Most positive input, most positive output
2. Most positive input, most negative output
3. Most negative input, most negative output
4. Most negative input, most positive input.

5.0 SPECIAL OP AMP CASES

5.1 PA02 SINGLE SUPPLY BEHAVIOR

A PA02 presents a special problem in single supply application. Like all BiFET input op amps, a negative common mode violation on either or both inputs causes the output to go full positive. Common mode violations are inherent in power up conditions in all op amp circuits since common mode is measured with respect to the supply rail.

In the case of a PA02, when the inputs are closer than 6 volts to either supply rail there is a common mode violation. It is implicit in this requirement that until total rail-to-rail supply voltage has reached at least 12 volts, the amplifier will not be linear. With a PA02 in particular, until the negative supply rail is at least 5 to 6 volts more negative than BOTH inputs, the output will be hard positive. This causes PA02 output to go full positive during power up in single supply applications. When used as an audio amplifier, this results in a loud "pop" from the speaker during power up.

There is no elegant solution to this problem. If the speaker is AC coupled and returned to positive supply rather than ground, this may help some. But most applications have shown the only dependable solution would be a relay that closes the circuit to the speaker once full supply voltage has been reached.

5.2 PA21 SINGLE SUPPLY CONSIDERATIONS

A PA21 is without a doubt the easiest power op amp to use on single supplies since the input common mode range can actually go more negative than the negative rail. Inputs can be applied to a PA21 in single supply applications without the need for additional biasing circuitry. The circuit shown on the front of the PA21 data sheet illustrates just how easy it is to apply for unipolar inputs in a DC motor drive application.

5.3 COMMON MODE BEHAVIOR IN GENERAL

It is helpful if the designer has some idea of which amplifiers are subject to unusual behavior during common mode violations. Like the BiFET PA02 described above, any FET input power op amp can exhibit polarity reversals during common mode violations. The polarity of most FET input stages, such as a PA07, all high voltage op amps, and Burr-Brown's OPA541, are such that a positive common mode violation will cause a reversal of output polarity. This occurs since gate to drain of input FETs becomes forward biased under these conditions and the signal effectively bypasses the FET and its normal inversion.

5.4 AMPLIFIERS WHERE SINGLE SUPPLY OPERATION IS NOT RECOMMENDED

The use of a PA89 in single supply circuits is discouraged. The input common mode voltage range dictates the inputs must always operate at least 50 volts inside of either supply rail, an impractical value to establish bias in the differential configuration. Unsymmetrical supply techniques are more applicable for getting large unipolar swings out of PA89 circuits. In the case of a PA89, the smaller supply needs to be at least 50 volts.

The power boosters PB50 and PB58 also present unique problems. For example, the ground pin of these parts must "see" a clean analog ground with low impedance over a wide bandwidth. This can be difficult to insure in a single supply environment. A PB50 must operate with its ground pin 30 volts more positive than the negative rail, while a PB58 must operate at least 15 volts, and preferably 20 volts more positive than the negative rail. While it is possible to use these parts in a single supply environment, it is far preferable to use them with split or unsymmetrical supplies.

6.0 TURN ON "POPS"

Regardless of amplifier choice, audio applications where the load is AC coupled and connected to ground will always be susceptible to turn on "pops". The two main reasons this occurs are: the amplifier is not linear until supply voltage is high enough; and the amplifier output inherently must go from zero to about half supply.

A bridge configuration will often improve (reduce) the likelihood of pops. Or as mentioned above, a relay which closes the circuit to the load once full supply voltage has been reached can help; although, with an AC coupled grounded load the output capacitor must still be

charged.

Controlling power supply rise time to be sufficiently slow can also alleviate this problem. It may require slowing it such that it even takes seconds. Even this technique will add a relay or some type of solid state switch. The easiest way to implement a slow rise supply is with a sufficiently large resistor in series with a filter capacitor.

7.0 DESIGN EXAMPLES

7.1 DESIGN SPECIFICATIONS:

Supply voltage = 28 volts. Input signal range = 0 to 5 volts. Unipolar output, single ended.

A PA12 has been selected for a unipolar voltage output motor drive. Differential configuration is selected, see Fig. 7. (Note that many details will not be discussed here, but are covered in other app notes, such as current limit resistors, flyback diodes, and power supply bypassing.)

Select R_F/R_I: This requires arbitrarily fixing one of these resistor

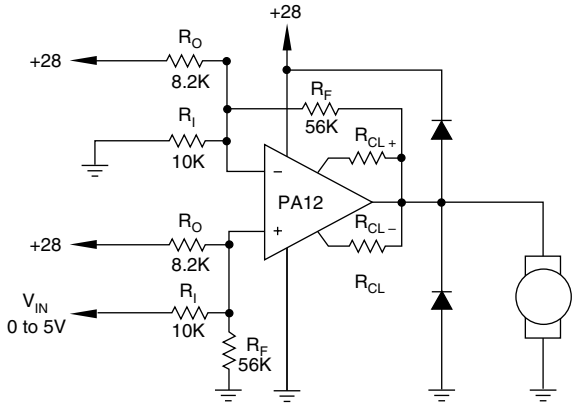


FIGURE 7. UNIPOLAR MOTOR DRIVE EXAMPLE

values. In general, the best practice is to fix R_I at about 10K ohms, as this is an impedance that most any small signal source will drive with no problem.

dV_{IN} has been established at 5 volts. While it is true that an op amp

$$\frac{R_F}{R_I} = \frac{dV_{OUT}}{dV_{IN}}$$

output cannot actually swing exactly to each rail, the circuit scaling should be selected as if it could; therefore, on a 28 volt supply, dV_{OUT}=28 volts. This results in a value for R_F of 56K ohm.

Now R_O must be selected to respect PA12 common mode requirements which dictate that the inputs must be kept 5 volts inside of either supply rail. So the inputs could be set anywhere from 5 to 23 volts. An ideal value would be 14 volts. Let's try an R_O value based on that and see if currents through the input resistors and input terminals remains reasonable. From the equation in 3.2 above, this would result in an R_O value of approximately 8.48K ohms, nearest standard value 8.2K ohms. This would result in 1.65mA flowing to the input terminals and no inordinate power dissipation in any of the input circuit resistors.

Since the process used to select R_O is based on worst case negative voltage input/output relationships, the common mode should be re-checked for full positive inputs and outputs. Assuming +5 volts at the input and a theoretical +28 volts at the amplifier output, the circuit simplifies to R_O and R_F being in parallel to +28 volts and forming a voltage divider with RI as the ground leg. This results in a voltage at the amplifier input of 16.32V, that is within the maximum positive common mode restriction of 23 volts.

7.2 DESIGN SPECIFICATIONS:

Supply voltage = 28 volts. Input voltage -2.5 to +2.5 volts. Voltage in, current output (will require Improved Howland Current Pump). Output range ±2A.

A PA02 is selected for this application along with a bridge circuit. Referring to Fig. 8, the R1, R2 and R4, R3 ratios were selected to provide the required transfer function based on a 0.301 ohm current sense resistor, R_S. Note that over the expected normal range of input signals and output voltages that common mode requirements are met. While true for this application, each one should be checked to verify the voltages are within acceptable limits. Note that even on this circuit that exceeding the ±2.5 volt dynamic range on the inputs will cause common mode violations to occur.

7.3 DESIGN SPECIFICATIONS:

Supply voltage = 450 volts. Input voltage 0 to 10 volts. High voltage bridge for piezo drive. Low power consumption.

A PA88 is selected to meet low consumption requirements, the

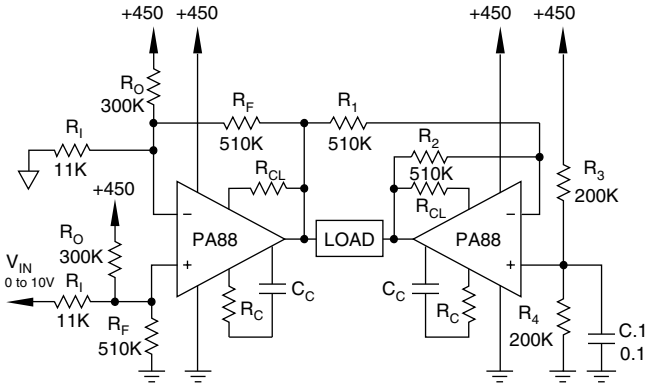
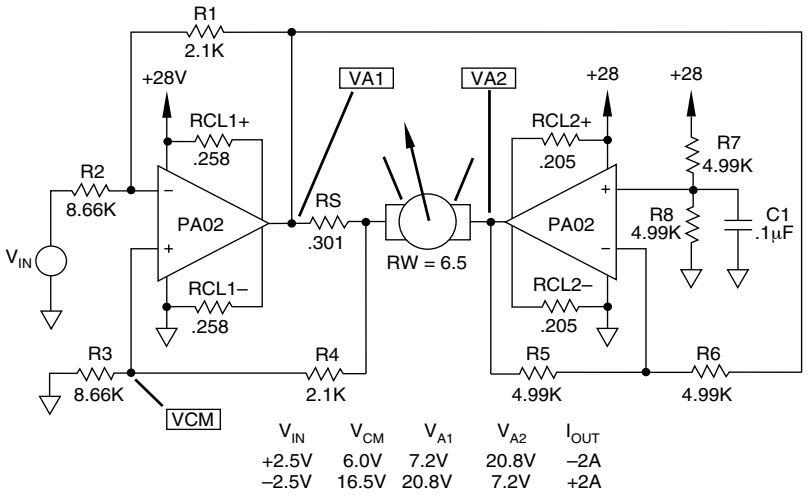


FIGURE 9. PA88 H.V. BRIDGE



V_{IN}	V_{CM}	V_{A1}	V_{A2}	I_{OUT}
+2.5V	6.0V	7.2V	20.8V	–2A
–2.5V	16.5V	20.8V	7.2V	+2A

FIGURE 8. LIMITED ANGLE TORQUE CONTROL (SINGLE SUPPLY)

circuit is shown in Fig. 9. R_F and R_I must provide a gain on the master amplifier of 45. In the process of minimizing power consumption and maintaining a reasonable physical size for components, consider there can be as much as 450 volts across R_F. In order to use a half watt resistor, R_F would need to be 510K ohms. For a gain of 45, R_I would then be 11K ohms.

In this high voltage application, it is wise to design for the minimum acceptable common mode voltage which is 12 volts for a PA88. 15 volts will be used to provide a little margin. 300K ohms will be required for R_O. 510K ohms will also be required for both gain setting resistors on the slave.

The half supply reference point resistors will each have 225 volts across them. The minimum acceptable value for half watt resistors would be 101K ohms each, but to minimize consumption, 200K ohms each is used. These must be bypassed.

With the large value feedback components around the slave, amplifier problems can result from feedback poles being created by amplifier input capacitance and stray capacitance. This may require a small compensation capacitor from 2 to 20 pF across the feedback resistor.

7.4 DESIGN SPECIFICATIONS:

Supply voltage = 450 volts. Input voltage 0 to 10 volts. Wide band high voltage driver. Single ended.

The circuit in Fig. 10 contrasts with the previous example in that it is a wideband circuit and requires the lowest possible impedances at all modes. The standard differential configuration will be used. This is an example where minimum common mode bias will have to be set to avoid excessive current and dissipation problems in resistors.

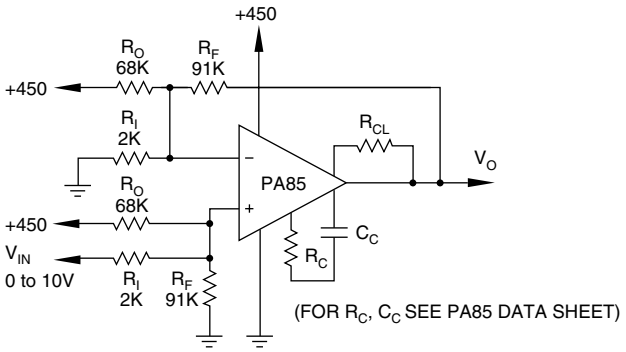


FIGURE 10. PA85 H.V. DRIVE

Gain for this circuit will be 45. In order to use the lowest possible value for R_F to insure good bandwidth, a 5 watt resistor will be used. Assuming worst case voltage stress across R_F to be 450 volts, the lowest permissible standard value is 43K ohms. For a gain of 45 volts, R_I must be (nearest standard value) 910 ohms. Because of such low impedances, a minimum common mode bias (from the PA85 data sheet) of 12 volts must be set.

Solving for R_O, assuming 12 volts of common mode bias, with an input of 0 volts and theoretical 0 volt output, the value is (nearest next lowest standard value) 30K ohms. This resistor will have 438 volts across it and will dissipate 6.4 watts.In addition, 15mA will flow through the input terminal. These values will be difficult, if not impossible, to work with. It may be possible to scale up by a factor of two and have sufficient bandwidth.

Re-calculating using 91K ohms R_F, and 2K ohms R_I, R_O solves to 68K ohms, the nearest standard value. Dissipation in R_O is now 2.8 watts and 6.3mA flows to the input resistor. While these numbers are better, they could still be a problem. Further scaling up of impedances will aggravate bandwidth problems as the effects of parasitic and amplifier input capacitance become significant.

This design example has been shown to be feasible in the design of a single supply circuit. But use of a –15 volt supply for the negative rail will eliminate the impedance constraints and permit the circuit to be designed for maximum possible bandwidth with a conventional circuit.

APPENDIX A: PROCEDURE FOR DESIGN OF DIFFERENTIAL CONFIGURATION

1. Select R_F and Ri:

$$\text{GAIN} = \frac{R_F}{R_I} = \frac{dV_O}{dV_I}$$

In general, R_I should be the resistor value on which all others "pivot." This is because R_I essentially represents the load presented to the input signal. Most small signal op amps work best if R_I is 10K ohms or larger, but many would permit R_I to drop as low as 1K or 2K ohms if necessary.

2. Select R_O:

$$R_O \quad \frac{V_S - V_{CM}}{\left(\frac{V_{CM}}{R_I \,||\, R_F}\right)} \text{ (MIN, from amplifier data sheet)}$$

3. Check dissipation in Ro. If too high, all resistor values need to be re-scaled upward.
4. Re-check V_{CM} at all four possible extremes of both input signal and amplifier output voltage. Although some of these operating conditions may not actually occur, it is wise to have a circuit that has linear common mode bias under all conditions if for no other reason than it is the only hope the op amp has to recover from the following conditions:
   a. Full negative input (usually 0), full negative output (theoretical 0). This condition is accounted for in the equation to select R_O.
   b. Full negative input, full positive output (assume theoretical maximum equal to supply voltage).
   c. Full positive input (don't forget that most small signal op amps could swing beyond their 10 volt linear limit, often up to a full 15 volts), full negative output.
   d. Full positive input, full positive output.

   If any of these four conditions do not meet common mode restrictions, adjust R_O accordingly. For instance, if a violation is more negative than minimum allowable common mode bias, reduce R_O (most common likely problem). If the violation is positive, which is unlikely with most realistic bias levels, then R_O should be increased.
5. If being used in a bridge, it is recommended that the slave amplifier noninverting half supply bias point be regulated, either with a zener diode or derived from some regulated voltage.

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APPLICATION NOTE 22

1.0 MEANING OF SOA GRAPH

SOA (Safe-Operating-Area) graphs define the acceptable limits of stresses to which power op amps can be subjected. Figure 1 depicts a typical SOA graph.

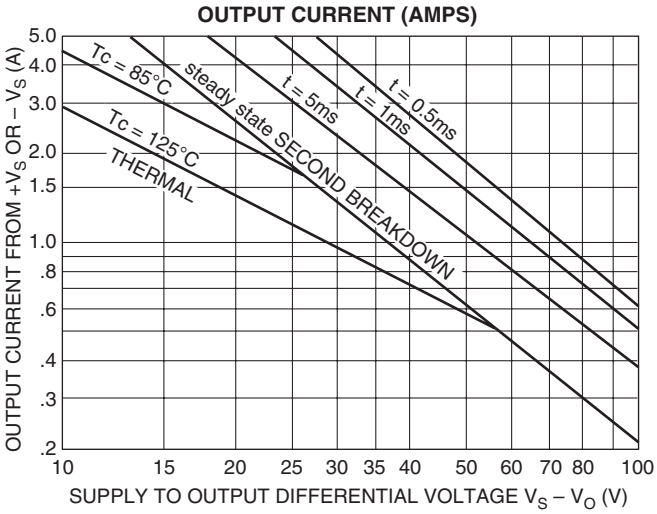


FIGURE 1. TYPICAL SOA PLOT

The voltage value on the right of the graph defines the maximum with no regard to output current or device temperature. Note that this voltage is related to the output voltage but is different; these two voltages are NOT interchangeable. The current value at the top of the graph defines maximum; again, with no regard to temperature or voltage. Inside the graph area will be one or more curves with a slope of -1 (as voltage doubles, current drops to half) labeled with a case temperature. These are constant power lines defined by DC thermal resistance and the rise from case temperature to maximum junction temperature (2.6°C/W and 200°C in this case). Lines with a steeper slope (about -1.5 in this case) are unique to bipolar output transistors. The steady state second breakdown reduces the amplifier's ability to dissipate DC power as voltage becomes more dominant in the power equation. Fortunately, the lines with time labels indicate higher power stress levels are allowed as long as duration of the power stress does not exceed the time label.

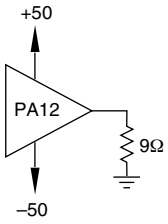
Transient SOA limits shown on data sheets are based on a 10% duty cycle pulse starting with junctions at 25°C. The repetition rate then would logically be defined by the time required for the junction to return to 25°C between pulses. Some amplifiers such as PA85 allow transient currents beyond the maximum continuous current rating. Most often though, the transient ratings are based on power or second breakdown restrictions.

2.0 ANALYTICAL METHODS

2.1 PLOTTING RESISTIVE LOAD LINES

Resistive load lines can be plotted quite easily. Keep in mind that since SOA graphs are log-log graphs, the resistive load line will have a curvature, so several points should be calculated and plotted.

Output voltage and current will always have the same polarity with a resistive load, so calculations can be performed at all times from 0 to 90° of the output cycle. Figure 2 depicts an example of resistive load line. It is interesting to note that this is a safe load which can require a 5 amp peak capability. If the output of the PA12 is unintentionally shorted to ground the voltage stress on the output will be 50 volts, which is not safe at the 5 amp current limit required to drive the load.



V_O	$V_S–V_O$	I_O
0	50	0
5	45	.556
10	40	1.11
15	35	1.67
20	30	2.22
25	25	2.78
30	20	3.33
35	15	3.89
40	10	4.44
45	5	5.00

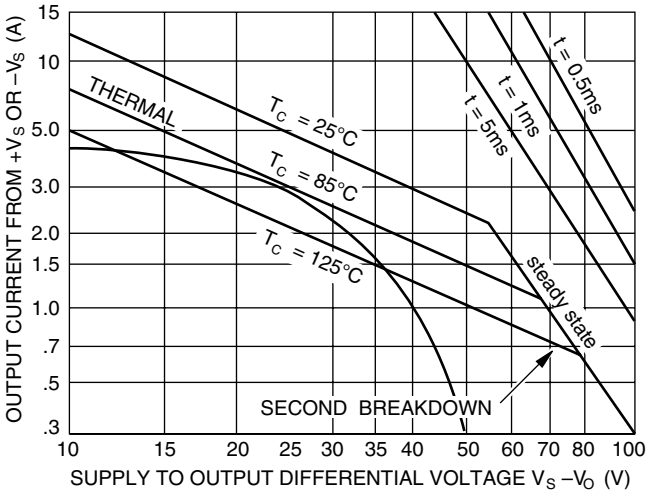


FIGURE 2. PLOTTING RESISTIVE LOAD LINE

In applications where the amplifier output would not be subject to abuse these operating conditions are acceptable. Foldback current limiting can be used to improve on the safety of this situation.

2.2 PLOTTING REACTIVE LOAD LINES

Reactive load lines of any phase angle can be plotted with the methods shown here. A completely reactive load line almost looks like an ellipse on the SOA graph since current stresses will occur at two different levels of voltage stress.

The voltage output waveform will define the reference phase angles for all point-by-point stress calculations. The waveform shown in Figure 3, starts at –90°, since current in capacitive loads will lead in phase. The waveform ends at 270° since that corresponds to the maximum phase lag of the current in an inductive load. All calculations will be within the limits of these angles.

Calculations proceed according to the steps in Figure 4. Currents will only need to be calculated over 180° since the load line for each half of the amplifier is a mirror image. Capacitive loads will start at –90° and progress through +90°. Inductive load calculations will start at +90° and progress to +270°. Step 2 in the procedure defines the starting angle for calculations based on the load phase angle. For example, a –45° load would start at –45° and continue to +135°. A 45° load will start at 45° and continue to 225°

Example of a typical load calculation:

In the resistive load example the load line of a 9 ohm resistive load was plotted and was quite safe. For this example let's use the same impedance but with a 60° phase angle.

G

VOLTAGE WAVE FORM ESTABLISHES REFERENCE PHASE ANGLE FOR ALL LOAD LINE CALCULATIONS. SHADED AREA REPRESENTS CALCULATION REGIONS

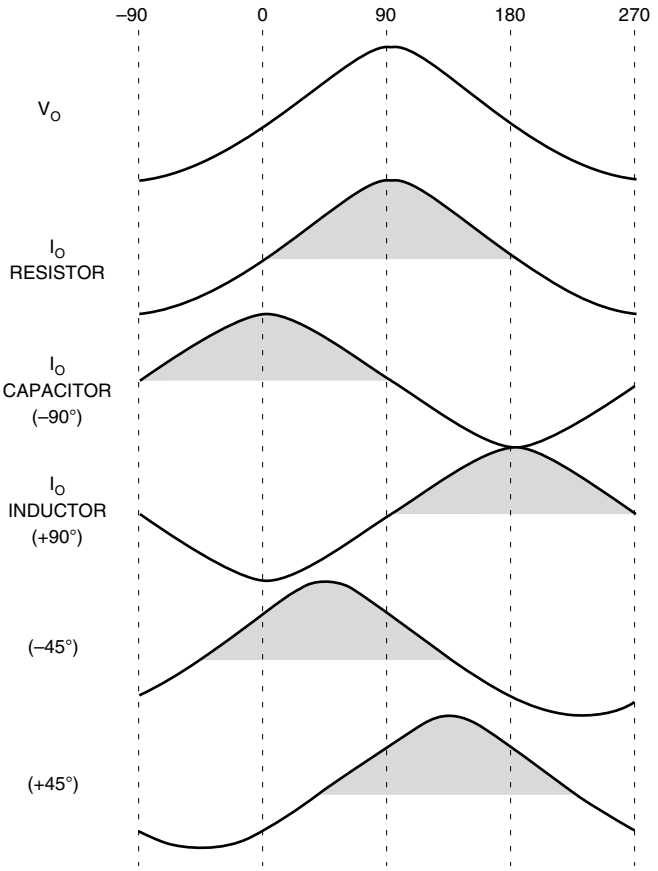


FIGURE 3. TYPICAL WAVEFORMS ASSOCIATED WITH REACTIVE LOAD LINE ANALYSIS

1. KNOWN: Vp , Z_L, θ_L
2. BEGIN POINT CALCULATIONS WITH θ_L AT 0° + θ_L AND PLOT FOR NEXT 180° IN WHATEVER INCREMENTS NEEDED FOR DESIRED ACCURACY (15° OR 30° INCREMENTS RECOMMENDED.)
3. Ipk = $\frac{Vp}{Z_L}$ CALCULATE ONLY ONCE
4. CALCULATE EACH INCREMENT: I = Ipk (sin (θ_V – θ_L))
5. CALCULATE EACH INCREMENT: Vd = Vs – Vp (sin θ_V)

FIGURE 4. REACTIVE LOAD CALCULATIONS

Figure 5 shows a PA12 driving an inductive load of 9 ohm at 60°. From step 2 of our procedure we know we begin calculating current at 60° and continue to 60+180 or 240°. For this example we will use 15° increments. Actually, it is only necessary to perform the step-by-step calculations for current up to the point where peak current occurs, in this case 150°. The increments back down to 240° will be a mirror image of what was just calculated. However, don't get this lazy with the voltage calculations we have yet to do.

Even though the point of maximum voltage stress occurring at full negative output swings is not evident in the voltage stress calculations, it is inconsequential since we have established that no current flows through the output device at that time. As long as the amplifier itself is within its voltage ratings, all will be well.

After all points are calculated, they may be plotted on the SOA graph. In this particular case note there are significant excursions beyond the steady state 25°C SOA limit. Is this acceptable? Consider the following factors to help make the decision: 1. The area beyond the continuous SOA is quite sizeable. 2. A calculation of maximum

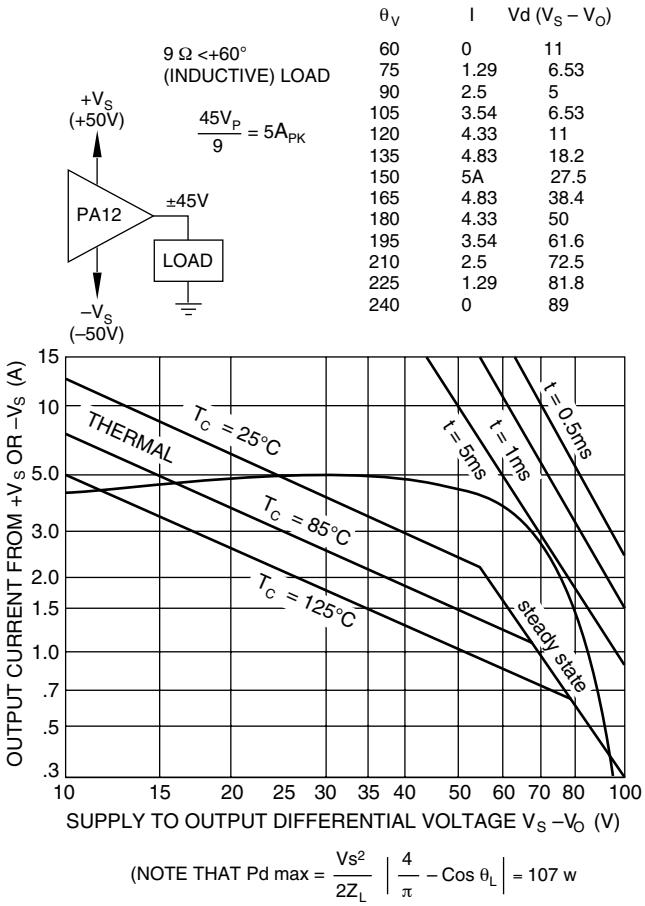


FIGURE 5. TYPICAL LOAD LINE CALCULATIONS

average power dissipation using the formula shown in Fig 5 (refer to General Operating Considerations for background on this calculation) shows the amplifier dissipating 107 watts.

The 107 watt dissipation will certainly cause the amplifier to operate at significantly elevated temperatures, even with a generous heatsink. Realistically the SOA limits are being reduced by the heating. We can even define exactly how badly. Assume a 25°C ambient (that's pretty optimistic). Using an HS05 heatsink rated 0.85°C/watt results in an amplifier case temperature 91°C. It is evident that the PA12 is not well suited for this application. The alternatives include either paralleling PA12s or upgrading to a PA05.

2.3 SPECIAL CASES OF LOAD LINE PLOTTING AND OTHER GENERALIZATIONS

For parallel connected amplifiers, assume each amplifier drives a load rated at half the current of the total load. In essence, double the load impedance. Do just the opposite for a bridge circuit.

Some simple relationships to keep in mind: for totally reactive loads maximum current occurs at a voltage stress corresponding to Vs and maximum dissipation occurs at a voltage stress of Vs+(0.707Vs), where current is also 0.707*Ipeak. In a resistive load, stresses are much less with maximum current occurring at maximum output voltage swing. This generally corresponds to the maximum swing specification given in every amplifier data sheet.

Also keep in mind that there are many load lines which will fit well within an amplifier SOA and be quite safe to drive. Yet these same loads can demand current capability that requires current limits be set so high the amplifier output will not be able to tolerate inadvertent shorts on its output. This is usually acceptable in applications with committed loads; however, applications where the amplifier output terminals are accessible to poorly defined loads or fault conditions demand fault tolerance on the part of the amplifier. A good example is a set of screw terminals like those found as the output connectors of an audio amplifier.

The methods shown here calculate load lines for reactive loads at only one frequency. For inductive loads worst case stresses will occur at the lowest frequency of interest with the opposite true for capacitive loads.

MOSFET amplifiers have an important difference from bipolar amplifiers regarding SOA limits: MOSFETs are only limited by power dissipation, or the product of V*I stress. Bipolar amplifiers are power limited up to certain voltages indicated on the SOA graphs, where second breakdown imposes even lower limits on safe current than power dissipation would allow.

2.4 PLOTTING AMPLIFIER CURRENT LIMITS

Additional information which can be plotted on the SOA graph to help assess amplifier safety is the current limit of the amplifier. Simple fixed current limiting is simply plotted along the current corresponding to that limit. Any load line excursions beyond that level can be disregarded. They are simply not possible.

Figure 6A depicts the SOA graph from Figure 5 with a fixed current limit drawn in. The fixed limit is set to 1.5 amps to provide short circuit safety at up to 85°C case temperature. It is obvious the load line is totally outside this current limit. The maximum available output will be set by the 1.5 amp current limit and impedance of the load. Or in the case of a resistive load, the lowest load impedance is a function of maximum output voltage and current limit.

Foldover current limiting can also be plotted on an SOA graph. This is important with inductive loads since foldover limiting in conjunction with inductive loads can cause more problems than it solves unless applied carefully. When foldover current limiting occurs with an inductive load, a violent flyback spike occurs that transitions all the way up to one of the supply rails. External ultra-fast recovery flyback diodes are a must when combining foldover limiting and inductive loads. It is also possible for relaxation oscillation to occur. This can be prevented by insuring that the normal inductive load line is well within all limiting values.

Figure 6B portrays foldover limiting according to formulas contained in Application Note 9 or the PA12 data sheet. The load of Figure 5 obviously cannot be driven. Note that with foldover limiting a peak current of 2.8 amps is available yet short circuit current is limited to 1.5 amps making it possible to safely drive a 16 ohm resistive load. To determine the minimum acceptable value for a reactive load, consider that 70.7% of peak current occurs at a voltage stress of Vs+(0.707Vs). A reactive load line within that operating point will likely be within all operating points and representative of minimum acceptable load.

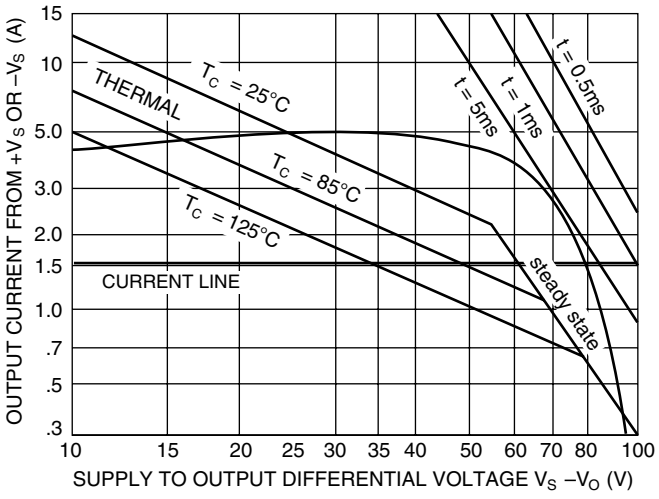
Figure 6B depicts the worst case acceptable reactive load. It really doesn't fill up much of the permissible operating region, but such are the trade-offs involved in driving difficult loads.

3.0 BENCH TESTING SOA

An oscilloscope can be used to do real world plotting of load lines on actual working circuits. The SOA limits can be drawn in on the scope screen if necessary. First, the SOA limits should be redrawn on linear-linear graph paper. This results in an SOA graph as shown in Figure 7A. The graph shown is for a PA12 bipolar amplifier, and second breakdown causes the break in the shape at 55 volts. MOSFET amplifiers will have a continuous curve representative of power dissipation. This can then be transferred to a transparency sized to properly fit on a scope screen.

The easiest method of connecting a scope to plot actual output device stresses will be to refer the scope ground to the negative supply of the circuit as shown in Figure 7B. This connection results in the proper phases for easy viewing on the oscilloscope. Since the oscilloscope ground is connected to the negative supply line, be certain there is ground isolation either in the amplifier power supply or the oscilloscope is connected to an isolation transformer.

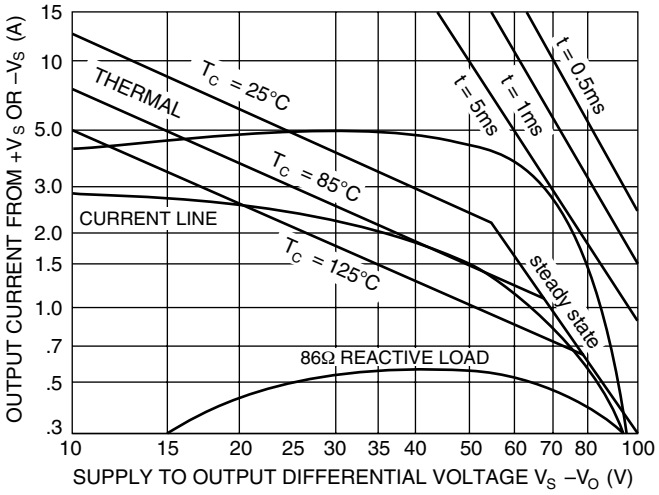
Rs is a current sensing resistor. When possible, use of a 1 ohm resistor provides a direct scale factor on the vertical input of volts = amps. If other values must be used consider scaling accordingly. The current sense resistor must be right at the amplifier power pin. This is one of those rare cases where it is temporarily necessary to violate the rules of proper power supply bypassing. Any capacitance present at the node, where the resistor meets the amplifier will interfere with high frequency measurements. If an oscilloscope current probe is available it is certainly preferable to the current sensing resistor since it provides accuracy and speed without having to disrupt the circuit.



A FIXED 15A CURRENT LIMIT

Max V_O(PEAK) REACTIVE = I_{LIM} x Z_L

$$\text{LOWEST POSSIBLE } R_L = \frac{V_O(pK)}{I_{LIM}} = \frac{45}{1.5} = 30\Omega$$



B FOLDOVER CURRENT LIMIT

R_{CL}= 0.433Ω PIN 7 OF PA12 GROUNDED

$$I_O = \frac{.65 + V_O\left(\frac{.28}{20}\right)}{R_{CL}}$$

$$\text{LOWEST POSSIBLE } R_L = \frac{45}{2.8} = 16\Omega$$

REACTIVE LOAD

$0.707\ I_{PK}$ @ $V_S + 0.707\ (V_S) = 50 + 35 = 85V$

I_{LIM}@ 85v = 370 mA

$$\frac{0.707\ V_O}{0.37A} = \frac{0.707 \times 45}{0.37} = 86\Omega$$

FIGURE 6. PLOTTING CURRENT LIMITS

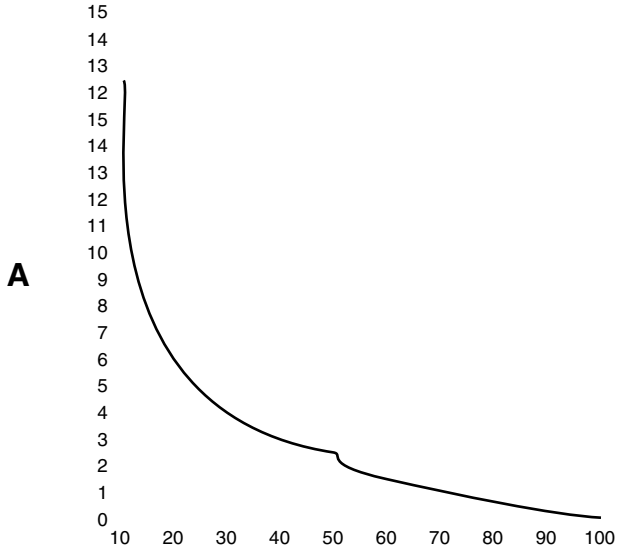
4.0 SOA MEASUREMENT CIRCUITS

Another means of analyzing SOA stresses in operating circuits uses an analog multiplier to calculate real time instantaneous power dissipation. This method is especially applicable where second breakdown is not encountered. For example, working with MOSFET amplifiers under any condition or most bipolar amplifiers at total rail-to-rail supply voltages of less than 30 volts.

The circuit shown in Figure 8 senses output device current and voltage stress as is done with an oscilloscope. Differential amplifiers with wide common-mode ranges are used for sensing these values

and levels, translating them to be applied to an analog multiplier. The output of the multiplier will be the product of the voltage and current stress on the output device. The Rs current sense resistor must be in the supply line so current is measured in only the output device corresponding to the voltage stress measurement.

This circuit provides a signal indicating instantaneous power dissipation. When working with a MOSFET amplifier such as the PA04, the designer should be concerned that this output be within the 200 watt dissipation of the PA04, or less if elevated temperatures are considered.



PAI2 PLOT OF 25°C STEADY STATE SOA ON LINEAR GRAPH

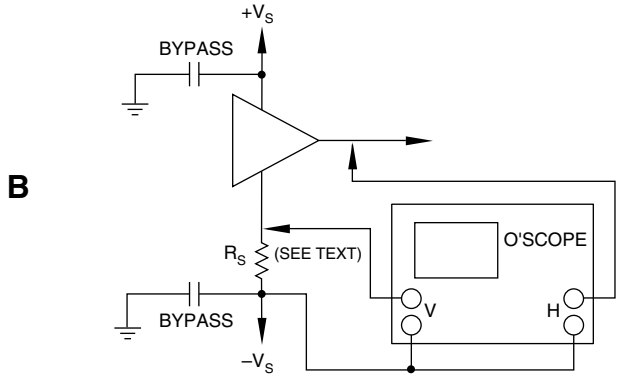


FIGURE 7. OSCILLOSCOPE TESTING OF SOA

5.0 OTHER FACTORS FOR DETERMINING SOA FIT

Since different SOA limits are shown for different temperatures, it is helpful to be able to predict the amplifier temperature. One factor that only the designer can define is ambient temperature. In particular, maximum ambient temperature.

Amplifier power dissipation will also be a factor in determining case temperature. Equations for predicting power dissipation maximums are discussed in the Apex Handbook, "General Operating Considerations", section 7.0, and the equations are shown here for convenience:

$$Z_L = |Z_L|$$

$$P_{D\,(OUT)MAX} = \frac{2Vs^2}{\pi^2 Z_L \cos\theta}\ ,\ \theta < 40°$$

$$P_{D\,(OUT)MAX} = \frac{Vs^2}{2Z_L}\left[\frac{4}{\pi} - \cos\theta\right]\ \ \theta > 40°$$

$$P_{TOTAL} = P_{D(OUT)MAX} + P_{D(IQ)}$$

Once worst case dissipation is known, use the heat sink thermal resistance and ambient temperature to calculate amplifier case temperature since SOA temperature limits are based on case temperature.

Effects of current limiting with reactive loads can also be evaluated when plotting load lines. Current limit lines can be drawn on the SOA representing current limit values. If reactive loads exceed these limits, distortion will occur. Often an inductive load causes what appears at first to be crossover distortion when viewing an amplifier output. In fact, what is actually occurring is that the current peaks when voltage transitions through zero and a light excursion into current limit looks much like crossover distortion.

Foldover current limits can be plotted on SOA graphs point by point as is done with load lines. Again, reactive loads must fit well within current limits. This is especially important when relaxation oscillation can occur if current limits are exceeded. In such cases the foldover effect must be reduced or even eliminated.

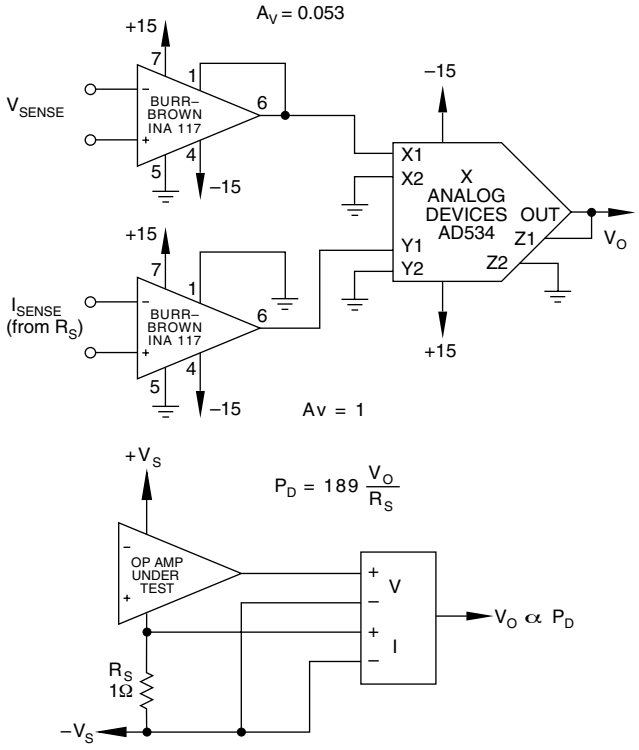


FIGURE 8. INSTANTANEOUS POWER DISSIPATION TESTER

6.0 AUTOMATED LOAD LINES

For DC and sine wave outputs, use Power Design[1] to plot a load line. Make sure the load line does not cross the shortest time curve and that excursions beyond any other second breakdown curve do not exceed the time label, and have a duty cycle of no more than 10%.

[1] Note 1. Power Design is a self-extracting Excel spreadsheet available free from www.apexmicrotech.com.

APPLICATION NOTE 24

1.0 AMPLIFIER SELECTION

One of the most entertaining moments as a power op amp applications engineer is when a customer calls up asking for an op amp to drive a 24V, 2A motor and has already settled on a 5 amp amplifier. It's just not that simple. This current rating could have many meanings, and actually there are two current rating conditions to be considered when designing a reliable application: stall current and reversal current.

Reversing a motor is about the most stressful application to which power op amps are subjected. It's important to establish from the outset if it will be necessary to sustain reversals. Some applications can disregard this; a good example being a simple speed control for a motor always rotating the same direction.

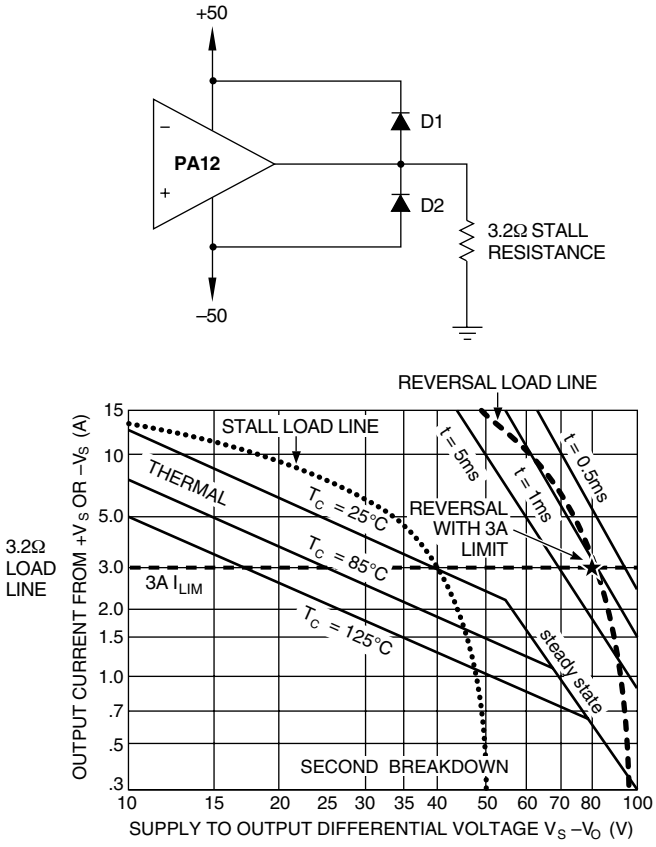


FIGURE 1. EXAMPLE OF MOTOR DRIVE LOAD LINE ANALYSIS

1.1 STALL RESISTANCE

Every motor will be stalled. This is the required state of transition to get a motor rotating. And it is doubtful any mechanical system can be devised which is guaranteed to never jam.

A single operating point for the stalled condition can be plotted. The location of the point is defined by several factors: 1) If the product of current limit and stall resistance is greater than maximum output voltage swing ((Ilim*Rs)>Vomax) the amplifier output will be at maximum swing; or 2) If the product of current limit and stall resistance is less than maximum swing, then the amplifier output voltage will be at the value of Ilim*Rs. To calculate dissipation, subtract this voltage from the supply voltage and multiply by current limit: Pd = (Vs-Vo)*Ilim

Alternatively, stall resistance can be plotted as a load line on the SOA graph. On the SOA graph, current limit should also be plotted. This is useful for conditions where the amplifier output will be attempting to go to some other value than full output voltage under stall conditions. Remember, maximum dissipation occurs at an output voltage one half way between zero and the supply rail.

Figure 1 shows just such an example of a calculation. This example uses a PA12A along with a motor which has a 3.2 ohm stall resistance and bipolar ±50V power supplies. If we simply plot the condition where the amplifier is against the rail, we have approximately 44V at the output and 13.8A of current flow. The supply to output differential and current result is a dissipation of 6 * 13.8, or 82.5W, which is within the amplifier SOA. If the amplifier output voltage were commanded to one half supply rail or 25V under a stalled condition, the power dissipation would be 195W, which is beyond the continuous SOA.

This illustrates the value in plotting the stall resistance load line. Both the low output and full output conditions are within the SOA, but intermediate values create excessive dissipation and this is immediately apparent by plotting the load line. The point where the load line exceeds the 25°C continuous SOA is a good value for maximum acceptable current limit.

In summary, design for stalled conditions should at least plot the resistive load line to determine proper setting of current limits. If the load line completely falls within the SOA, then other fault conditions of shorts from output to ground or output to either rail will take precedence in determining current limit values in the event these faults must be accounted for.

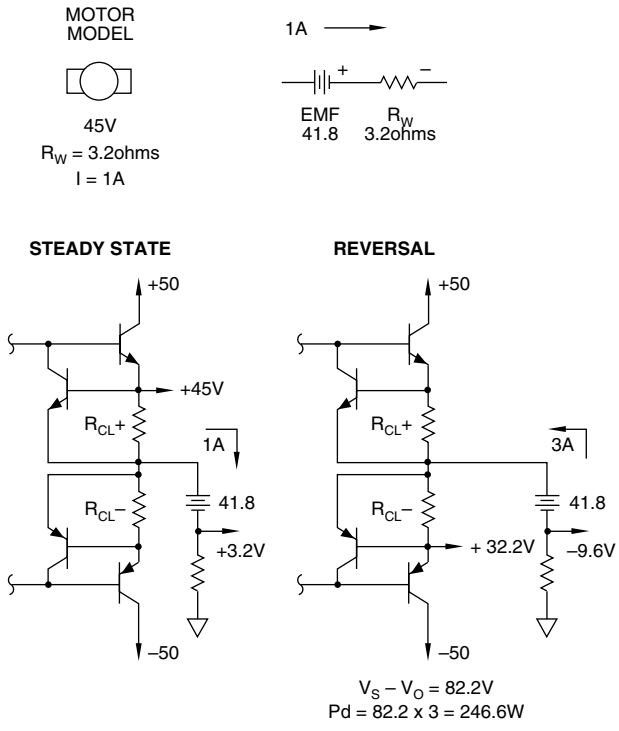


FIGURE 2. MOTOR REVERSAL

1.2 REVERSAL

Reversal brings the back EMF of the motor into the stress equation. The back EMF is equivalent to a new source of voltage with a polarity

such that it adds to the supply voltage and increases voltage stress on the output devices. As in the stalled condition, motor resistance also plays a part.

Determining back EMF may seem difficult, but most motor data sheets shed some light on determining its value. Knowing the motor resistance and current draw permits exact calculation of back EMF: it is the applied voltage, less the drop across the motor resistance. Worst case assumption for back EMF should assume it could be equal to applied voltage, and this would be true for any motor drawing negligible current.

The schematic in Figure 2 shows an example of what happens to the circuit in Figure 1 during reversal—assuming the amplifier current limit is set at 3 amps. Motor operating current is a function of load. So for this example, let's assume the motor requires 1A under normal running conditions. Maximum output from the PA12 could be up to 45V. Subtract 3.2V for the drop across the motor resistance for a back EMF of 41.8V. Upon command to reverse the negative half goes into 3A current limit. The resulting voltage drop across the motor resistance subtracts from the back EMF, providing the values shown during the reversal. The dissipation during this event is 246W—clearly outside the PA12 SOA. Motor reversal by nature is a transient condition. If it can be assured the motor can reverse within an amount of time equivalent to transient stress limits on the SOA graph, then the application could be safe.

1.2.1 PLOTTING REVERSAL LOAD LINE

Just as stall load lines can be plotted, so can reversal load lines. The process of plotting a worst-case reversal load line starts with the assumption that back EMF is equal to maximum amplifier output voltage. An even worse assumption is that it is equal to the supply voltage of one of the rails.

Plot the load line by:

1. Calculate the drop across the motor resistance at various currents within the SOA.
2. Subtract that voltage from the back EMF to result in the amplifier output voltage.
3. Take the resulting difference between supply rail and output as the stress point.

Figure 1 also shows its reversal load line. This load line indicates that it is not within the continuous SOA unless current is limited to approximately less than 400mA. If this application were required to tolerate reversal, an amplifier with better SOA should probably be used.

Load lines that exceed the continuous SOA, but are within transient SOA, may be safe if the time conditions are met with certainty. This is difficult to assess, and usually requires a judgement call when any signal other than pulse is present. In general, as in any case, life is simpler and more reliable if we at least make the effort to keep within continuous SOA limits.

1.3 NOMINAL OPERATING CONDITIONS

Nominal operating conditions can only be determined on a by application basis. All motor data sheets shows torque and RPM constants allowing the engineer to determine required voltage and current once the load is known. The worst case normal operating point will be when the amplifier output is halfway between zero and the supply rail.

2.0 AMPLIFIER PROTECTION AND HEATSINKING

As has already been shown, the load lines must be within the amplifiers capabilities or current limit must be configured to restrict operation to within the SOA. However, the SOA shrinks with increasing temperature. Therefore, either adequate (read: generous) heatsinking must be provided for, or SOA analysis should consider limits of higher case temperature curves. Using standard heatsink formulae the exact amplifier case temperature can be determined under any operating condition (as well as junction temperature).

2.1 FOLDBACK CURRENT LIMITING

Current limit, as demonstrated, is truly a good thing and necessary. But designers must not be lured into the attraction of using foldback current limiting as available on PA10, PA12 and can be used on PA04, PA05. Reason being that foldover current limiting causes more problems than it solves when used with nonlinear loads. For instance, with inductive loads (and motors are very inductive), the amplifier can go into relaxation oscillation. And with an inductive load, when the amplifier goes into current limit, it generates a violent pulse all the way up to the supply rail (limited only by flyback diodes, without which it would go beyond the rail).

If a designer insists on experimenting with foldover current limiting, then it would be wise to plot the current limit line on the SOA along with the expected load lines. If the load lines are within the current limit boundaries, then you're OK. Keep in mind that foldover current limiting slope can be varied and sometimes a gentle foldover characteristic can provide adequate protection.

2.2 FLYBACK DIODES

Brush type DC motors generate a continuous pulse train of inductive kick-back due to brush commutation. This inductive kickback must be clamped within the limits set by the power supply rails by flyback diodes as shown in Fig. 1.

Many amplifier schematics show these diodes internally, but this does not mean they can be depended upon in motor drive applications. In most bipolar, darlington, emitter-follower output stages, these diodes are the substrate diodes of the darlington output transistors. This causes the diodes to exhibit slow recovery, which will in turn overheat under the stress of a continuous pulse train of inductive kickback.

Amplifiers with no diodes, or slow recovery diodes, internally must have external fast or ultra-fast recovery diodes added. If these are not available, then standard recovery is better than nothing. The diodes must be rated for voltage well in excess of the total rail-to-rail voltage. Current requirements are not demanding. One amp types will suffice.

All APEX amplifiers require external flyback diodes except the MOSFET output amplifiers PA04, PA05, PA09, PA19; and the PA02 and PA03 which are bipolar amplifiers with built-in high speed flyback diodes. In general, on any APEX data sheet schematic or in the Apex data book, if the flyback diodes have a different part numeral than the output transistor, then they are separate fast recovery diodes. Diodes with the same part number as the output transistor are slow recovery diodes and external additions will be needed. For example in the PA12, the upper output transistor is Q2A and Q2B and the flyback diode is D2. If you're not sure, there is no harm in adding them even if they are not needed.

3.0 AMPLIFIER PERFORMANCE

3.1 VOLTAGE VS CURRENT OUTPUT BEHAVIOR

Voltage output configurations are generally used for speed control. Although a voltage output configuration can be incorporated within a larger current control loop. The importance of voltage output in the amplifier itself relates to output impedance, which will be very low. As such, the output voltage as seen on a scope will generally be quiet and steady under steady state conditions.

Current output can be implemented as mentioned above with a larger current sense loop that incorporates a voltage output power amp. Alternatively, current output circuits can be implemented within the feedback loop around the op amp alone. When this is done, the amplifier apparently exhibits a very high output impedance. A current source should do this by definition. This is mentioned because if the output of such a circuit is scoped, the flyback pulses will be exaggerated by this high impedance — a perfectly normal behavior for current output.

There is no performance advantage in selecting voltage or current output, at least not due to power op amp circuit choice alone. Many other factors will play a part in which choice provides the best performance. In general, without using larger control loops, the voltage output configuration is preferred for speed control, and the current output for torque control.

APPLICATION NOTE 25

1.0 INTRODUCTION

High voltage power op amps are often selected to drive capacitive loads, such as **PIEZO TRANSDUCERS, CAPACITORS, ELECTRO-LUMINESCENT DISPLAYS, ELECTROFLUORESCENT LIGHTING, ELECTROSTATIC DEFLECTION**, etc. There are some special considerations when designing circuits to meet your high voltage needs.

We will look in detail at the selection of the power op amp, stability considerations, power dissipation in the op amp and heatsink selection, support components for the circuit, and power supplies and their effect on circuit performance. When we complete these areas of investigation we will look at some alternative power op amp circuits for attaining high voltage control across capacitive loads.

The format of our information will be "definition by example" along with generic formulae for your specific design.

2.0 EXAMPLE DESIGN FOR DRIVING A CAPACITIVE LOAD

GIVEN: +/-Vs= +/-200Vdc
frequency = DC to 10KHz (sinewave)
V_{IN} = +/-10V
piezo load with CL = 10.6nF
V_{OUT} = 360Vpp
Tambient = 25°C, free air convection cooling only
Inverting gain okay

FIND: Power op amp, heatsink and recommended schematic for piezo drive.

SOLUTION: Sections 2.1 thru 2.6 will provide a detailed, logical approach to designing a solution for this capacitive load drive problem.

2.1 POWER OP AMP SELECTION

STEP 1: Define capacitive load. Here we are given CL = 10.6nF

STEP 2: Calculate large signal response (slew rate) using highest frequency and largest voltage swing. The required slew rate to track a sinewave at a given frequency for a given output amplitude is as follows:

S.R. = 2π f Vop (1×10^{-6})
Slew Rate [V/μs] = 2 X π X frequency X V_{OUT} peak X (1×10^{-6})
S.R. = 2π10KHz 180 (1×10^{-6}) = 11.3V/μs

STEP 3: Calculate maximum current requirements. This will occur at highest frequency with capacitive loads.

METHOD 1: Calculate Xc @ highest frequency.

$$Xc = \frac{1}{2 \pi f CL}$$

$$Xc = \frac{1}{2 \pi \ 10\ KHz\ 10.6nF} = 1.5K\Omega$$

$$Iop = \frac{Vop}{Xc} = \frac{180V}{1.5K\Omega} = 120mAp$$

METHOD 2: Use highest slew rate and largest voltage swing.

$$Iop = CL \frac{dV}{dt}$$

$$Iop = 10.6nF \frac{11.3V}{\mu s} = 120mAp$$

STEP 4: Do a first pass worst case power dissipation calculation. For details on derivation of this formula see "General Operating Considerations."

$$P_{DOUT}\ max = \frac{Vs^2}{2\ ZL}\left[\frac{4}{\pi} - \cos\theta\right]$$

For capacitive load applications this formula reduces to:

$$P_{DOUT}\ max = \frac{4\ Vs^2}{2 \pi Xc} = \frac{4\ (200)^2}{2 \pi\ 1.5K\Omega} = 17W$$

STEP 5: Summarize what we know and pick power op amp.
+/-Vs = +/-200Vdc
S.R. = 11.3V/μs
Iop = 120mAp
Vop = 180Vp
$P_{DOUT\ MAX}$ = 17W
In viewing the APEX High Voltage Selector Guide there is only one likely candidate for this design—PA85.

STEP 6: Review the chosen amplifier's data sheets for details.
Figure 1: Contains relevant excerpts from the PA85 data sheet.
Figure 1A: From the output specifications, a worst case saturation voltage of 10V at 200mA is identified. Therefore we can meet 180Vp out at 120mAp without a problem.
Figure 1B: From the power response curve we see 360Vpp at 10KHz is within the power response curve for any value of Cc (PA85 compensation capacitor).
Figure 1C: Since we want 180Vp out for 10Vp in we will be operating at a gain of 18. This is close enough to 20 to choose Cc = 10pF and Rc = 330Ω. This will maximize small signal bandwidth as well as slew rate should a last minute decision require more performance out of the design.
Figure 1D: At Cc =10pF the slew rate is about 400V/μs, so there is no question about meeting the requirement for an 11.3V/μs slew rate.
Figure 1E: At a closed loop gain of 18, (25 dB), it can be determined that for Cc =10pF the closed loop bandwidth of this circuit (fcl) is about 2MHz. This first check says not only can a 10KHz sinewave be tracked in the large signal domain, but the PA85 will also have enough bandwidth to have a flat response at 10KHz in the small signal domain.
Figure 1F: From our previous calculation $P_{DOUT\ MAX}$ = 17W. An Applications Engineer's rule of thumb for power derating curves works as follows:

> For a 25°C ambient temperature you can find a heatsink that will allow you to keep the case temperature at 85°C using free air convection cooling.

Therefore, 17W output power dissipation almost intersects with the Tc = 85°C line on the power derating curve. This means our first look says we should be able to heatsink the PA85 for this design.

Now it would seem the work is done and you can proceed to build a breadboard or commit to printed circuit board layout. But first you must proceed to look at other key issues for driving capacitive loads with power op amps such as stability.

2.2 SMALL SIGNAL STABILITY

Figure 2 (see second page following this one) is a complete schematic of our PA85 drive circuit. The gain of -18 will give us 360Vpp out for 20Vpp in. We will now look at the details for selecting stability components Rn, Cn, and CF.

2.2.1 MODIFIED Aol FOR CAPACITIVE LOADS

Figure 3 (see second page following this one) illustrates how the amplifier's Aol curve gets modified by Ro, the amplifier's unloaded output impedance, and CL, the capacitive load. Output impedance, Ro, of the amplifier, is flat within the bandwidth of the amplifier and predominantly resistive. Refer to Apex Application Note 19 for a detailed discussion of this issue.

Figure 4 (see second page following this one) lists high voltage Apex amplifiers and boosters most commonly used to drive capacitive loads and their corresponding output impedance.

FIGURE 1A

OUTPUT		MIN	TYP	MAX
VOLTAGE SWING	I_O = ±200mA	±Vs – 10	±Vs – 6.5	V
VOLTAGE SWING	I_O = ±75mA	±Vs – 8.5	±Vs – 6.0	V
VOLTAGE SWING	I_O = ±20mA	±Vs – 7.5	±Vs – 5.5	V
CURRENT, continuous	T_C = 85°C	±200		mA
SLEW RATE, A_V = 20	C_C = 10pf		400	V/μs
SLEW RATE, A_V = 100	C_C = OPEN		1000	V/μs
CAPACITIVE LOAD, A_V = +1	Full Temperature Range	470		pf
SETTLING TIME to .1%	C_C = 10pf, 2V step		1	μs
RESISTANCE, no load	R_{CL} = 0		50	Ω

FIGURE 1B

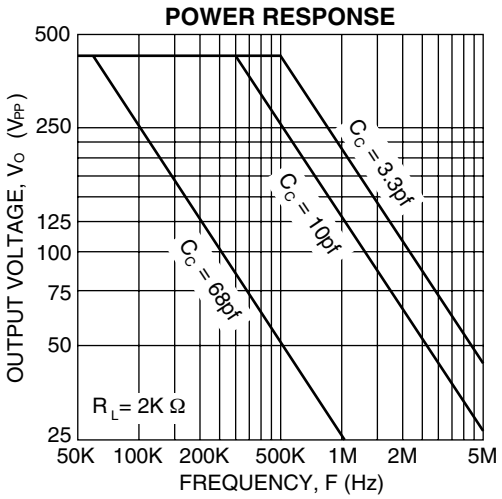


FIGURE 1E

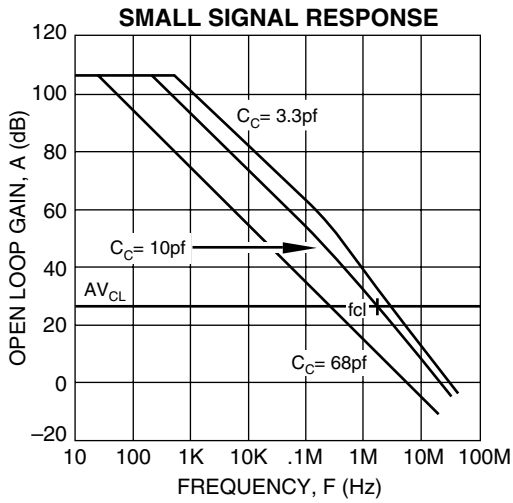
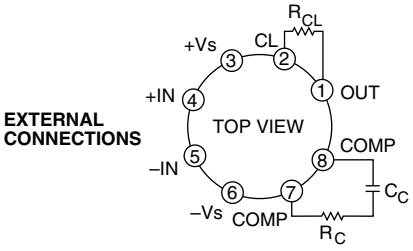


FIGURE 1C



EXTERNAL CONNECTIONS

PHASE COMPENSATION

Gain	C_C	R_C
1	68pf	100Ω
20	10pf	330Ω
100	3.3pf	0Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

FIGURE 1D

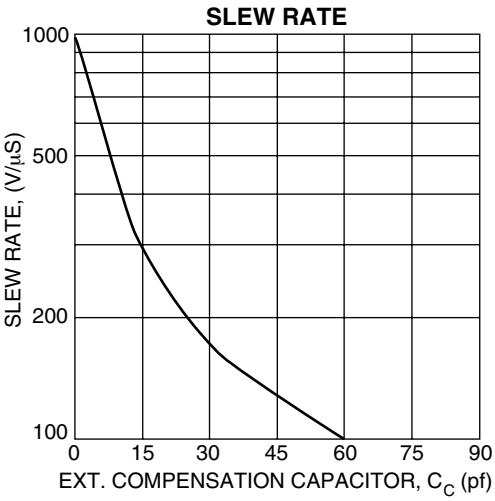


FIGURE 1F

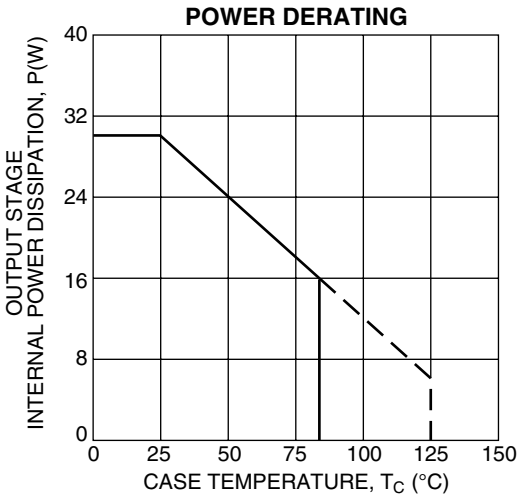


FIGURE 1. PA85 DATA SHEET EXCERPTS

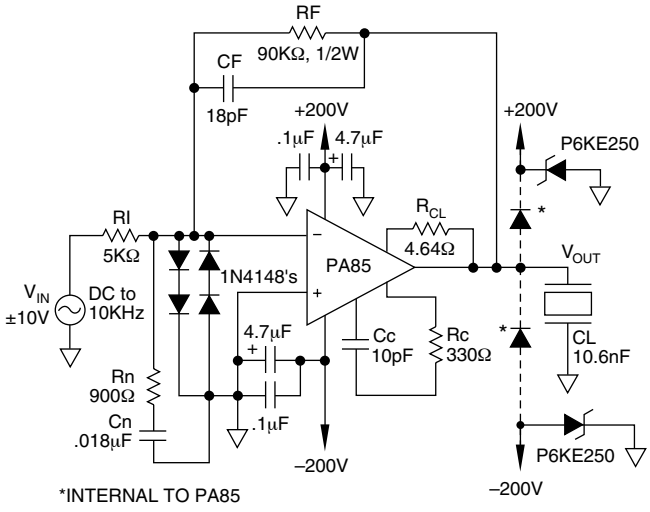
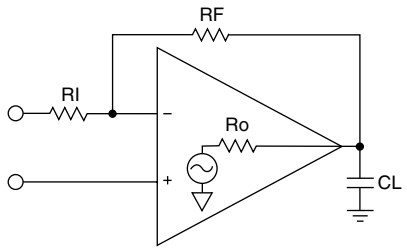


FIGURE 2. PA85 PIEZO TRANSDUCER DRIVE



UNITY GAIN STABLE AMPLIFIER
UNSTABLE 40 dB/DECADE WITH CL

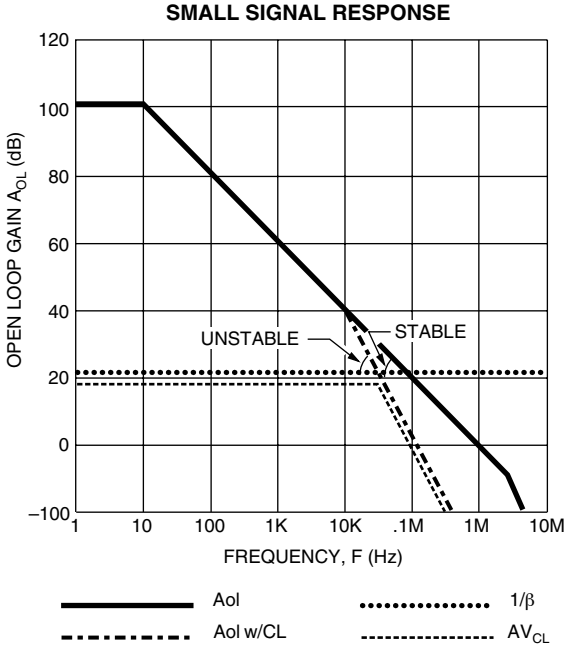


FIGURE 3. CAPACITIVE LOADING

OP AMP OR BOOSTER	OUTPUT IMPEDANCE
PA41	150 ohms
PA81J	1.4K-1.8K ohms
PA82J	1.4K-1.8K ohms
PA83	1.4K-1.8Kohms
PA84	1.4K-1.8K ohms
PA85	50 ohms
PA88	100 ohms
PA89	100 ohms
PB50	35 ohms
PB58	35 ohms

FIGURE 4. OUTPUT IMPEDANCE
HIGH VOLTAGE OP AMPS AND BOOSTERS

2.2.2 STABILITY PLOTS

Figure 5 illustrates the magnitude plot for stability needed to analyze and check for good stability on our PA85 drive circuit. The low frequency pole for the Aol curve can be determined from the "Small Signal Response" curve, and the high frequency pole can be extrapolated from the "Phase Response" curve in the APEX data sheet for the PA85.

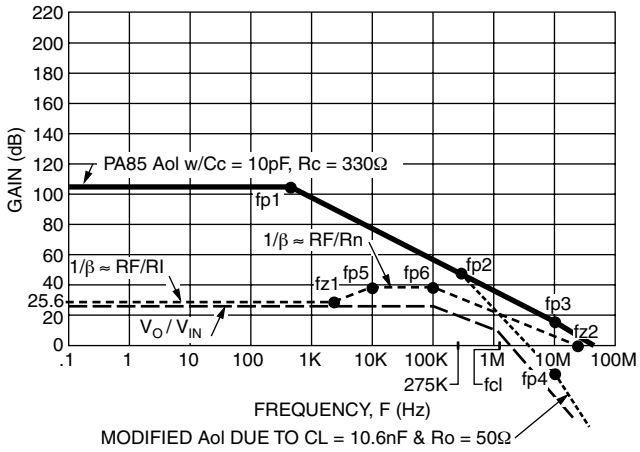


FIGURE 5. MAGNITUDE PLOT FOR STABILITY
(PA85 PIEZO TRANSDUCER DRIVE)

STEP 1: Modify Aol due to capacitive load and amplifier's output impedance:

$$fp2 = \frac{1}{2\,\pi\,(Ro + R_{CL})\,CL} = \frac{1}{2\,\pi\,(50\Omega + 4.64\Omega)\,10.6nF} = 275\ KHz$$

fp4 = 10MHz pole from amplifier's original Aol plot (fp3)

STEP 2: Check 1/β for resistive feedback alone:
1/β [1/(beta)] is the small signal AC gain at which the op amp runs. Refer to Apex Application Note 19 for details. First order stability criteria for magnitude plots states that the Rate-of-Closure (difference between the slopes of Modified Aol and the 1/β plot) be 20dB per decade at fcl. Refer to Apex Application Note 19 for details on Rate-of-Closure. With AC small signal gain set only by RF and RI the 1/β plot will be a flat line at 25.6dB. At the intersection of modified Aol and 25.6dB the Rate-of-Closure will be 40 dB per decade indicating marginal stability and potentially destructive oscillations.

STEP 3: Add Noise Gain Compensation as a first step towards good stability:
Rn and Cn will form a noise gain compensation network which will raise the gain of the 1/β plot without directly affecting the V_{OUT}/V_{IN} relationship. Refer to Apex Application Note 19 for details.
Noise Gain equations:
High frequency gain = RF/Rn = 90KΩ/900Ω = 100 ==> 40dB

$$fp5 = \frac{1}{2\,\pi\,Rn\,Cn} = \frac{1}{2\,\pi\,900\Omega\,.018\mu F} = 9.8\ KHz$$

fz1 ==> Can be obtained graphically using +20dB per decade slope starting at the intersection of fp5 and the high frequency gain of the noise gain compensation and proceeding towards the DC gain.

Even though we have raised the higher frequency portion of the 1/β curve to 40dB, it will still intersect the modified AoI at 40dB per decade Rate-of-Closure.

STEP 4: Add feedback zero (1/β pole) to 1/β plot to gain best AC small signal stability (Refer to Apex Application Note 19 for details):

$$fp6 = \frac{1}{2\pi\ RF\ CF} = \frac{1}{2\pi\ 90k\ 18pF} = 98\ KHz$$

Now at fcl, you have the desired 20dB per decade Rate-of-Closure and good stability according to our first order criteria for magnitude plots. You will now need to plot the open loop phase plot for a complete stability check.

STEP 5: Review of rules for open loop phase plots:

1) Poles in the 1/β plot become zeros in the open loop stability check.

2) Zeros in the 1/β plot become poles in the open loop stability check.

3) Poles and zeros in the AoI curve or modified AoI curve of the op amp remain respectively poles and zeros in the open loop stability check since the op amp AoI curve is an open loop curve already.

4) Phase for zeros is represented by a +45 degree phase shift at the frequency of the zero with +45 degree per decade slope, extending this line with 0 degree and +90 degree horizontal lines.

5) Phase for poles is represented by a –45 degree phase shift at the frequency of the pole with a –45 degree per decade slope, extending this line with 0 degree and –90 degree horizontal lines. Refer to Apex Application Note 19 for further details.

STEP 6: Plot open loop phase using information from magnitude plot: Figure 6 is the open loop phase plot for our PA85 drive circuit.

Notice in Figure 5 that the 1/β plot continues beyond fcl all the way until it intersects at 0dB forming fz2 in the 1/β plot. An amplifier will not run in an AC small signal gain of less than 0dB. You must account for an additional high frequency pole in the open loop phase check. This pole is easily read graphically from Figure 5 rather than calculating it from lengthy derivations.

A review of Figure 6 shows graphical addition of the contributions from all poles and zeros to yield a net open loop phase plot. The phase margin from DC to fcl is never less than 45 degrees which implies good stability for this circuit.

2.2.2.1 RULES OF THUMB FOR STABILITY PLOTS

Now that we know we have good stability, let's return to the magnitude plot in Figure 5 for a few handy rules of thumb:

1) Think of open loop phase when you play with the 1/β plot: Notice that fp1 (pole in open loop) is spaced about a decade away from fz1 (pole in open loop). If you don't add fp5 (zero in open loop) within a decade of fz1, (pole in open loop) the open loop phase margin will dip to less than 45 degrees.

2) As you run out of loop gain (difference between AoI curve and 1/β plot), keep poles and zeros one-half to one decade away from zero loop gain. Notice that fp6 is about one-half decade away from the modified AoI curve near fp2. This allows "Real World" AoI curves and component tolerances to stack against you without creating stability nightmares.

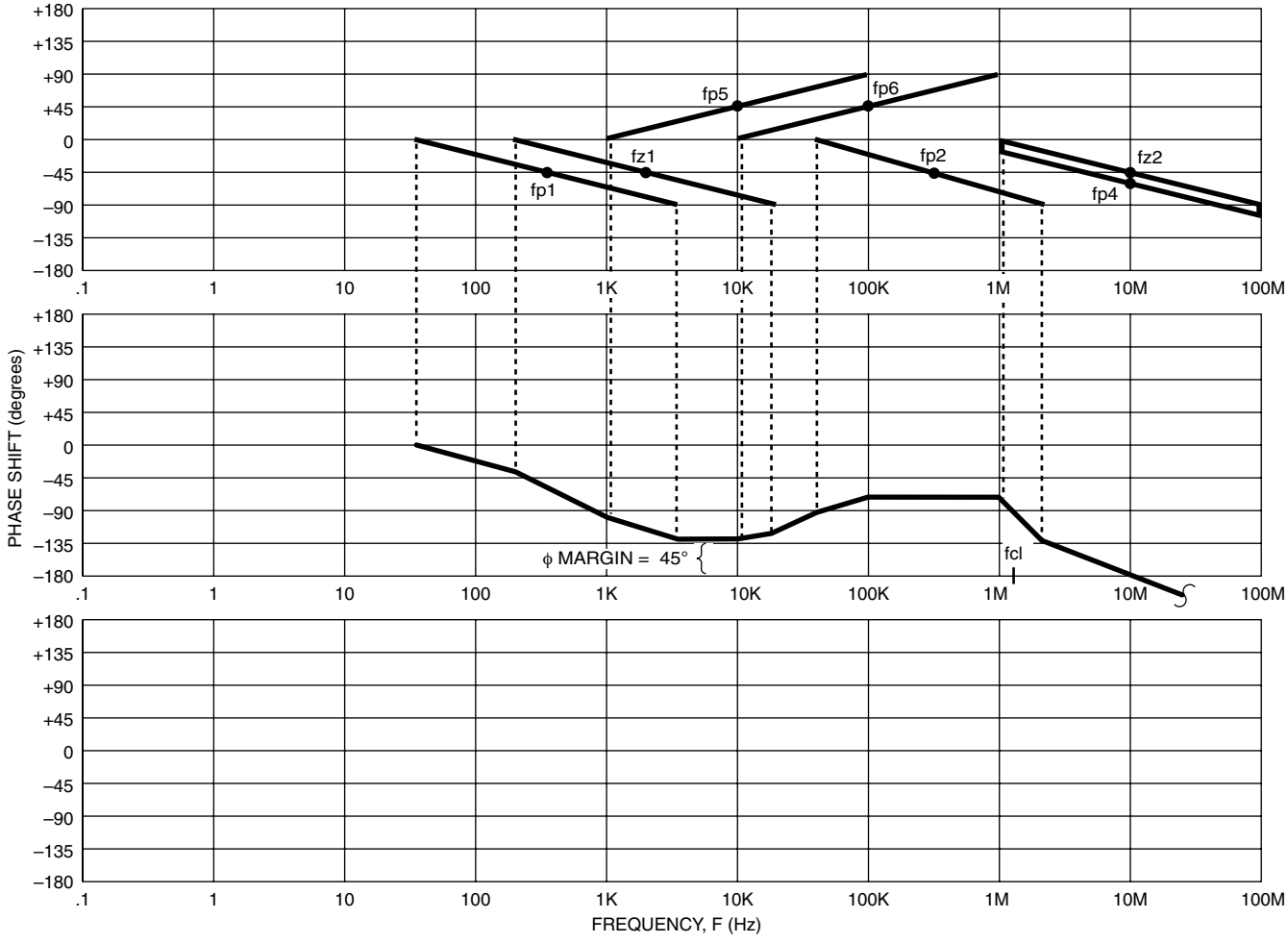


FIGURE 6. OPEN LOOP PHASE CHECK FOR STABILITY (PA85 PIEZO TRANSDUCER DRIVE)

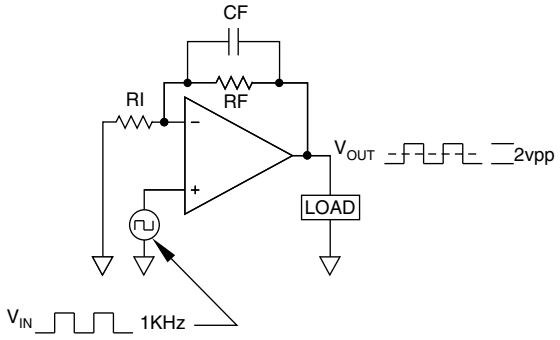
3) Always design your circuits, using these stability techniques, for 45 degrees of phase margin in the open loop phase check for stability. This is because the first order linear approximations for phase have a six degree error. As well, there is no guarantee you will consistently receive op amps with the typical Aol graph.

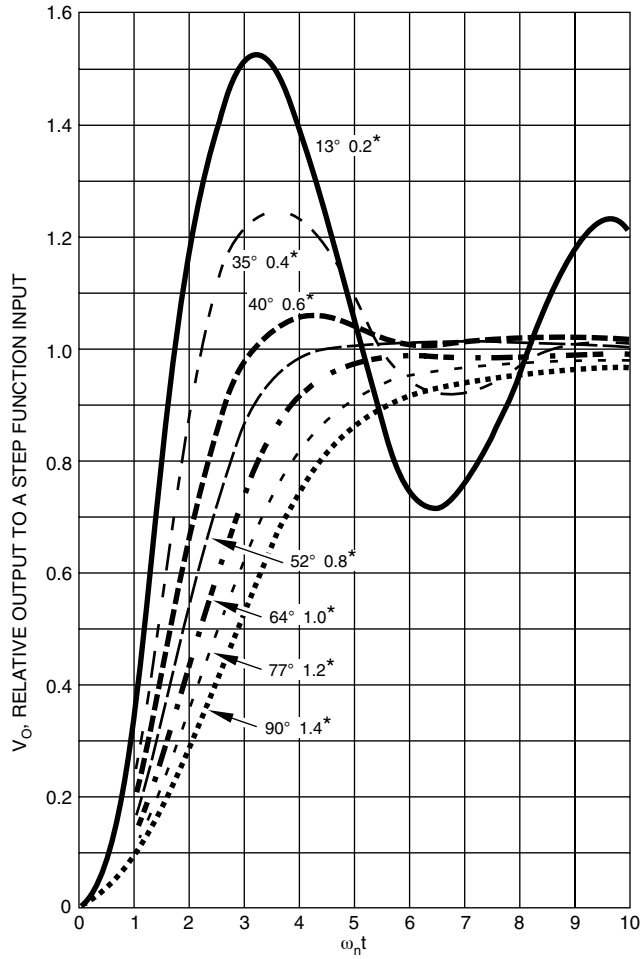
In a typical design procedure, you will plot magnitude plots for stability first, do an open loop phase plot, and then return to calculate final component values to create the desired magnitude plot that yields 45 degrees open loop phase margin for stability.

Refer to Apex Application Note 19 for handy tips and short cuts for plotting magnitude and phase plots.

2.2.3 "REAL WORLD" STABILITY TEST

Once a circuit is built, there is a relatively easy test you can run to verify if the predicted open loop phase margin made it from design to the "real world".





* OPEN LOOP PHASE MARGIN AND DAMPING FACTOR

FIGURE 7. SQUARE WAVE TEST

Figure 7 details the Square Wave Test for measuring open loop phase margin by closed loop testing. The output amplitude of the square wave is adjusted to be 2Vpp at a frequency of 1 KHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can then be compared to the graph in Figure 7 to yield a reading for open loop phase margin.

A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use.

Refer to Apex Application Note 19 for more involved closed loop tests for measuring open loop phase margin and checking "real world" stability.

2.3 CLOSED LOOP RESPONSE

From Figure 5 the V_{OUT}/V_{IN} relationship for our PA85 circuit is seen as flat from DC to 100 KHz, where it begins to roll at 20dB per decade. It continues until we reach 1.33 MHz where it rolls off at 40dB per decade until reaching 10MHz, where our slope changes to 60dB per decade.

The V_{OUT}/V_{IN} phase shift for any given frequency is given by the following:

$$\text{Phase Shift} = -\text{Tan}^{-1}\frac{f}{fp6} \quad -\text{Tan}^{-1}\frac{f}{fcl} \quad -\text{Tan}^{-1}\frac{f}{fp4}$$

where f = frequency of interest for phase shift

For our upper frequency of interest of 10 KHz let's see what the V_{OUT}/V_{IN} phase shift is:

$$\text{Phase Shift} = -\text{Tan}^{-1}\frac{10\text{ KHz}}{100\text{ KHz}} \quad -\text{Tan}^{-1}\frac{10\text{ KHz}}{1.33\text{MHz}}$$

$$-\text{Tan}^{-1}\frac{10\text{ KHz}}{10\text{MHz}} = -6.2\text{ degrees}$$

The formula above can be expanded to include any number of poles. If the V_{OUT}/V_{IN} relationship has zeros simply add the following for each zero:

$$+\text{Tan}^{-1}\frac{f}{fz}\text{; where fz is the frequency of the zero}$$

2.4 POWER DISSIPATION AND HEATSINKING

Power dissipation inside the amplifier consists of two components, P_{DQ}, quiescent power dissipation, and P_{DOUT}, output stage power dissipation. Simply compute $P_{DQ} = Iq[+Vs - (-Vs)]$ and add the worst case power dissipation for the output stage to this to form P_{DINT}, total internal power dissipation. Figure 8 shows the Thermo-Electric Model that is applicable for this situation.

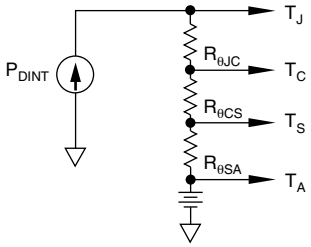


FIGURE 8. THERMO–ELECTRIC MODEL

In our PA85 design case we have AC power dissipation in the output stage. From Section 2.1, Step 4, that power dissipation is:

$$P_{DOUT}\text{ max} = \frac{4\ Vs^2}{2\ \pi\ Xc} = \frac{4\ (200)^2}{2\ \pi\ 1.5K\Omega} = 17W$$

Quiescent power is:

$$P_{DQ} = Iq\ [+Vs - (-Vs)] = 25mA\ [+200 - (-200)] = 10W$$

There are two thermal requirements we must meet in this application. First, the case temperature must be kept below 85°C. Second, the junction temperature must be kept below 150°C. We know the application is dissipating a total of 27W, but the data sheet contains three different thermal resistance ratings which vary substantially. The first is an AC rating where the two output transistors share the heat load at a frequency of 60Hz or greater. When the power is dissipated in mainly one output transistor, use the DC thermal resistance. The last rating is applied only if no heatsink is used.

This is a rare practice with power op amps. Let us briefly pursue the possibility we might be able to not heatsink the amplifier in this application. Figure 9 models this case. TO-3 packages are rated at 30°C/W. When the case of the amplifier must be kept below 85°C, this imposes a maximum power dissipation of 2W even with an ideal ambient temperature of 25°C. At 27W our PA85 would burn up very quickly without a heatsink.

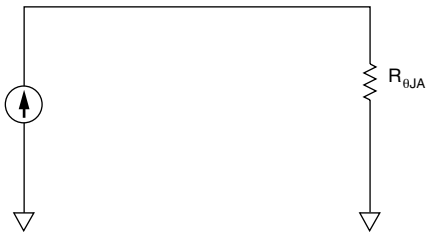


FIGURE 9. THERMO–ELECTRIC MODEL (NO HEATSINK)

The PA85 data sheet tells us the AC thermal resistance is 2.5°C/W. We will allow 0.2°C/W for $R_{\theta CS}$ and use the following to determine a maximum heatsink rating.

$$R_{\theta SA} \le \frac{T_J - T_A}{PD_{INT}(max)} - R_{\theta JC} - R_{\theta CS}$$

$$\le \frac{(150-25)°C}{27W} - 2.5°C/W - 0.2°C/W$$

$$R_{\theta SA} \le 1.9°C/W$$

Select APEX HS03; $R_{\theta SA}$ = 1.7°C/W with forced air flow at 100 ft/min.

As a last check, multiply the total power times the sum of the thermal resistance of the heatsink and the mounting interface and add to ambient temperature to verify the case temperature does not exceed 85°C.

$$27W * (1.7°C/W + 0.2°C/W) + 25°C = 76.3°C$$

Refer to **"Package and Accessories Information"** section of APEX Amplifier Handbook.See APEX catalog "GENERAL OPERATING CONSIDERATIONS" for details on heatsinking and mounting the amplifier.

2.5 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS

High voltage op amps require some special considerations when selecting support components for completion of your circuit design. The following list covers these critical areas of concern:

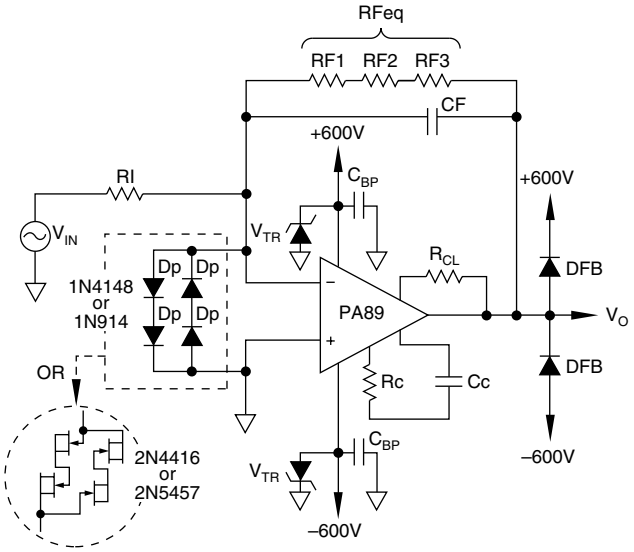


FIGURE 10. HIGH VOLTAGE SUPPORT COMPONENTS

1) ESD Handling Precautions:
All APEX high voltage amplifiers are rated Class 1 for ESD sensitivity, as defined in MIL-H-38534. This requires that proper ESD handling precautions be observed from receiving through manufacturing until the device is installed in a properly designed circuit. Areas which will require strict ESD control include, but are not limited to, personnel, tabletops, stocking containers, floors, soldering irons, and test equipment.

2) Input Protection (Refer to Figure 10):
Most high voltage amplifiers have a differential input voltage rating of +/-25V. It is easier on high voltage amplifiers to cause differential input overvoltages than on lower voltage op amps. These overvoltages on the input can occur during power cycling or can be transients fed back through CF from the output to the input.
The input diodes, Dp, clamp the maximum input differential voltage to +/-1.4V while allowing sufficient differential voltage for overdrive when demanding maximum slew rate from the amplifier. The diodes shown are low capacitance fast signal diodes. If lower leakage and lower capacitance diodes are desired, J-FETs may be connected as diodes as shown.

3) Output Diodes (Refer to Figure 10):
MOSFET high voltage amplifiers have internal, intrinsic diodes that are connected from the output to each supply rail. High voltage Bipolar amplifiers do not have these diodes and must be added externally as shown. The MOSFET amplifiers' internal diodes are sufficient for an occasional transient that may be created in a piezo drive situation where the piezo element is stressed mechanically, thereby creating an electrical voltage. For applications where there is potential for sustained high energy flyback, in ATE applications, where everything that is not supposed to happen usually can and does, or in applications where Kilovolt flashovers can occur and be inmpressed onto the amplifier's output, it is recommended to use fast (500nS or less depending upon the anticipated flyback energy frequency) reverse recovery diodes, DFB, external to the amplifier. Remember to size the diodes for a Peak Reverse Voltage rating of at least the rail to rail supplies the amplifier is operating at (for Vs=+/–200V ==> 400V Peak Reverse Voltage rated diode).

4) Transient Voltage Suppressors (See Figure 10):
Transient Voltage Suppressors, V_{TR}, can be added to the supply lines to provide protection from undesired transients on the power supply line. The first is power supply overvoltage on power cycling. Secondly, when energy is dumped into the supplies from DFB, if the power supply terminals at the amplifier do not look like a low impedance for the frequency of that energy, the amplifier could

become overvoltaged. Transient suppressors, such as TRANSZORBS, manufactured by General Semiconductor Industries, Inc, will provide a low impedance path for this energy. If you use unipolar transient suppressors, they will prevent polarity reversal across the amplifier since they will become a forward biased diode if supplies are reversed.

Selection of the transient suppressors may require a series string of devices to reach the desired reverse stand-off voltage rating for higher voltage op amps. Choose the transient suppressor for a reverse stand-off voltage slightly greater than the maximum DC or continuous peak operating voltage level. This selected device will then have an actual breakdown voltage that is typically 1.1 to 1.36 times higher. For example, a P6KE250 has a reverse stand-off voltage of 202V with a breakdown voltage of 225V to 275V. Herein lies the trade-offs of transient suppressors. They are excellent devices with a sharp breakdown curve and can dissipate large amounts of power for short periods of time. The problem is the exact breakdown voltage is not a tightly controlled parameter for any given model.

A typical design dilemma is the case where an engineer desires to use a part at its full power supply rating and still provide transient voltage protection on the supply lines. Now you ask, how high is APEX's Absolute Maximum Rating for Supply Voltage, REALLY? Well, the guaranteed Absolute Maximum Rating for Supply Voltage is exactly what our vendors guarantee to us. Lawyers aside, it is known in the electronics industry that a 400V transistor may actually breakdown at 500V from a given lot. In a nutshell, you are in no-man's land above the Absolute Maximum Rating; however, it is much better to limit the transient voltages to as low as possible than to not limit at all!

5) Power Supply Bypassing (See Figure 10):

The rule of thumb is .1μF ceramics directly at the op amp with 10μF/Ampere of peak output current in parallel within 2 inches or so of each amplifier. Many of the high voltage amplifiers are less than 200mA and the .1μF ceramic is all that will be needed. In cases of PA89, +/600V supplies, .01μF seems to be more readily available and this is adequate for high frequency bypassing on the power supply line. Watch the voltage ratings for these capacitors!

6) Compensation Capacitor and Resistor (See Figure 10):

Cc must be rated for the rail-to-rail supply voltage at which the amplifier is operating. In this case a 1200V rating. It is recommended that the compensation capacitor be a temperature stable capacitor for reliable performance over temperature. Mepco / Centralab, Inc, series D and S type capacitors are available in 50Vdc through 6KVdc ratings in various temperature characteristics.

Rc will normally see little or no voltage since most of the voltage stresses will be across Cc. Rc then can be a standard 1/8W metal film resistor.

7) Feedback and Input Components (See Figure 10):

RI will generally have little voltage stress or power dissipation since most input signals are less than 10 volts peak. Standard metal film resistors will work fine.

CF can have up to one supply impressed across it. In this case it would need to be a 600Vdc minimum rated capacitor.

RF1, RF2, and RF3 will need some special considerations. Power dissipation will become of prime importance since up to one of the supply rails can be impressed across these resistors at a given time. This could yield power dissipations of: $P_D = Vs^2 / RFeq$. The second consideration is voltage coefficient of resistance. This is a parameter that defines how a resistor changes its resistance with applied voltage. At low voltages this characteristic is not a dominant factor. At higher voltages it can become a more significant factor causing reductions in gain for a given resistor ratio or increased distortion. Dale RNX, ROX, FHV, MVW, and HVX series resistors are well characterized for high voltage use. The power dissipation factors and voltage coefficient of resistance may require several resistors to be used in series in the feedback path of the op amp.

8) Current Limit Resistor (See Figure 10):

Remember that all the load current flows through the current limit resistor, R_{CL}, and therefore size it according to the value of current limit, Ilim, by $P_D = (Ilim^2)(R_{CL})$. Maximum voltage stress across R_{CL} will be about +/-.7V for most amplifiers. Check the "Current Limit" section of the applicable data sheet for exceptions to this.

9) PWB Layout:

Higher voltages will require wider spacings between traces on a printed circuit board layout as well as spacings between ground planes and other conductive layers. Mil-Std-275 provides some guidelines in these areas.

10) Probing, Plugging and Powering:

Be extremely careful when probing a high voltage amplifier with the power on. An inadvertent slip of a probe can destroy a high voltage amplifier. There are often compensation pins adjacent to power supply pins. Those compensation pins are often connected to the gates of MOSFETs which do not take kindly to the full power supply being impressed upon them.

Do not plug or unplug an amplifier into a live, powered socket. The transients generated can destroy the high voltage amplifier.

Do not use fuses in the power supply lines of high voltage amplifiers or ever power them with one supply disconnected and no path to ground for that disconnected power supply. This can lead to a sneak path for permanent destruction on several of the high voltage amplifiers.

PA85
POWER SUPPLY REJECTION

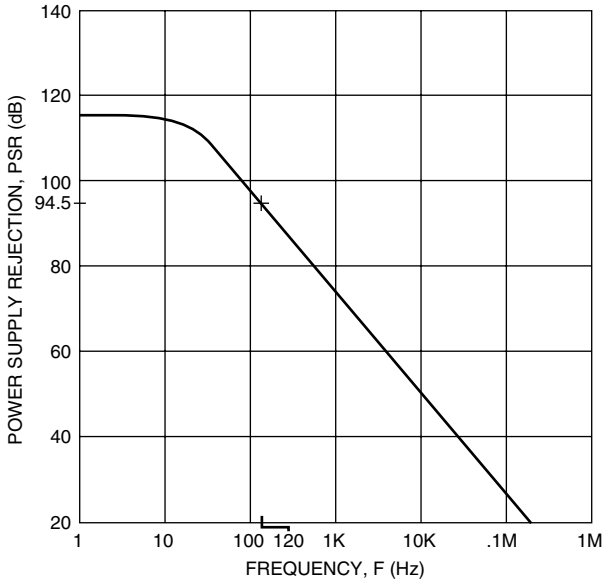


FIGURE 11. PA85 PSR

2.6 POWER SUPPLIES

2.6.1 POWER SUPPLY REJECTION

Often times high voltage amplifiers require the use of either a switching power supply or a simple AC full-wave bridge rectified supply (make real sure you use transient suppressors if you use this type of supply). The question then is asked what will be the effect on the output of the amplifier due to the ripple of the power supply?

Figure 11 is the Power Supply Rejection curve for the PA85. We will use this and our familiar circuit of Figure 2 to understand power supply ripple effect on amplifier output. Figure 11 is a referred-to-input specification. Let's assume there is a 1Vpp, 120Hz ripple on the power supply line. From Figure 11 this implies PSR of 94.5dB. Since this is a rejection curve, the gain is actually -94.5dB which is a gain of .000018836. This gain times 1Vpp on the power supply line means you will see .018836mVpp appear as an input offset voltage in the circuit. At a gain of 19 this means our output will see .358mVpp ripple at 120Hz due to power supply fluctuations.

2.6.2 HIGH VOLTAGE POWER SUPPLIES

See the last few pages of the ACCESSORIES INFORMATION data sheet for a list of manufacturers of high voltage supplies. As a group, these vendors offer AC and DC inputs, standard and custom units in linear and switching topologies. No matter what supply you use, check it for possible overshoot at power up, power down and even power cycling. Beware that many high voltage supplies feature foldback or

foldover current limiting. In these circuits, current limit is reduced at low voltages compared to full output voltage. Current sources in Apex high voltage amplifiers draw their rated quiescent current at somewhere around half their minimum supply voltage rating. For example, the PA85 is likely to draw over 20mA as soon as the supplies reach +/-7 to 10V. If a foldback feature does not allow this operating point, the system will latch up.

3.0 HIGH VOLTAGE AMPLIFIER VARIATIONS

3.1 RESISTOR ISOLATION FOR CAPACITIVE LOADS

In Section 2.2.2 one method for stabilizing capacitive loads was discussed. There is another common way to isolate capacitive loads and thereby acquire good stability.

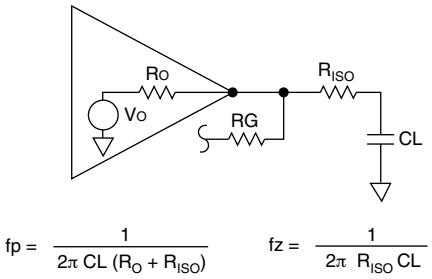


FIGURE 12A: R_{ISO} & CL

Figure 12A illustrates a technique for isolating the capacitive load through the use of R_{ISO}. This isolates the point of feedback, where RG is connected, from the capacitive load. The addition of R_{ISO} adds a zero in the modified Aol plot to counteract the pole formed by Ro and CL. Figure 12A also contains the equations for the modified Aol curve defining fp and fz.

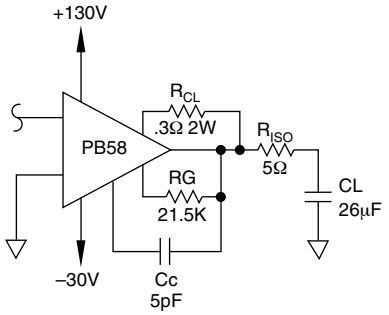


FIGURE 12B: PB58 w/ R_{ISO} & CL

Figure 12B will be part of a real world design for a PIEZO DRIVE CIRCUIT. Here a PB58 will be required to drive a 26μF capacitive load. Figure 13 illustrates the modified Aol curve with and without the use of Riso. From Figure 14 (see next page) we see –28 degrees of phase margin without R_{ISO}. However, in Figure 15 (see second page following this one) we have 90 degrees of phase margin through the use of R_{ISO}.

STEPS FOR CALCULATING R_{ISO} (refer to Figure 13):

STEP 1: Calculate initial fp: Use Ro and CL which are given by virtue of the load for the application and the choice of power op amp. Plot location of fp.

STEP 2: Graphically choose fz: From plot of fp and fp1 you can see a 40 dB/decade slope heading towards 0 dB gain. Choose fz at a location such that it will change slope of modified Aol from 40 dB/decade to 20 dB/decade for at least a decade above AV_{CL} and within a decade of fp1.

STEP 3: Calculate final value for R_{ISO}: Calculate from formula for fz in Figure 12A the value for R_{ISO} from fz location in Figure 13. Recalculate final value for fp and plot final modified Aol ensuring final location of fz meets criteria in STEP 2.

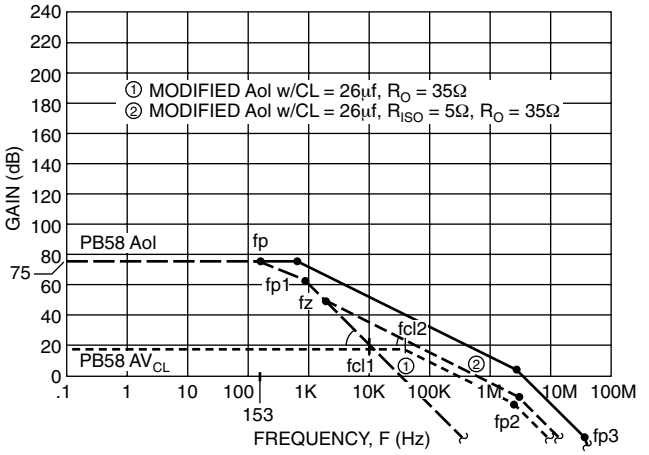


FIGURE 13. R_{ISO} & CAPACITIVE LOAD EFFECTS

One disadvantage with the use of R_{ISO} is that the point of feedback is not directly at the capacitive load. This means that accurate control of the voltage at CL is not obtained. This is usually not a problem since most piezo drives are used inside of an outer control loop such as position feedback into a microprocessor which will then generate an error command to the input of the PB58 piezo drive circuit. The major advantage of R_{ISO} is that a wide range of capacitive loads can now be driven with good stability.

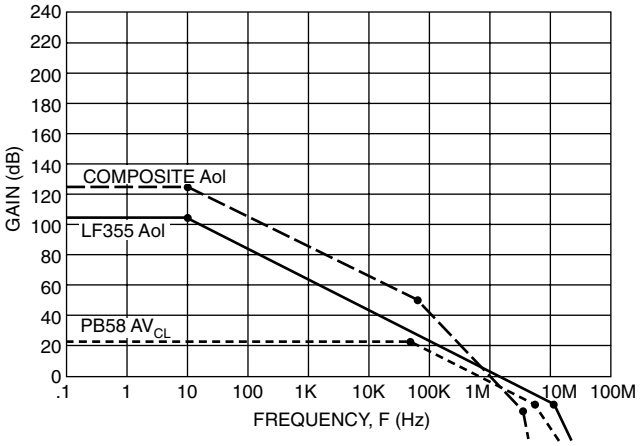


FIGURE 17. CREATION OF COMPOSITE Aol

3.1.1 PB58 PIEZO DRIVE WITH R_{ISO}

Figure 16 (see next page) is a piezo drive amplifier using the PB58 and our R_{ISO} technique for capacitive load stability.

The design goal for this amplifier was to have an adjustable DC offset and still allow an AC input signal to swing about the DC offset. Amplifier A1 AC couples V_{IN} and offsets it around the selected DC offset set by R_{ADJ}.

The stability of the PB58 composite amplifier begins with first ensuring the PB58 itself is stable. This is accomplished with the use of R_{ISO} in Section 3.1 and Figure 13. Figure 17 creates the composite Aol by adding the closed loop voltage gain of the PB58 to the open loop gain of the LF355 front end amplifier. For details on stabilizing

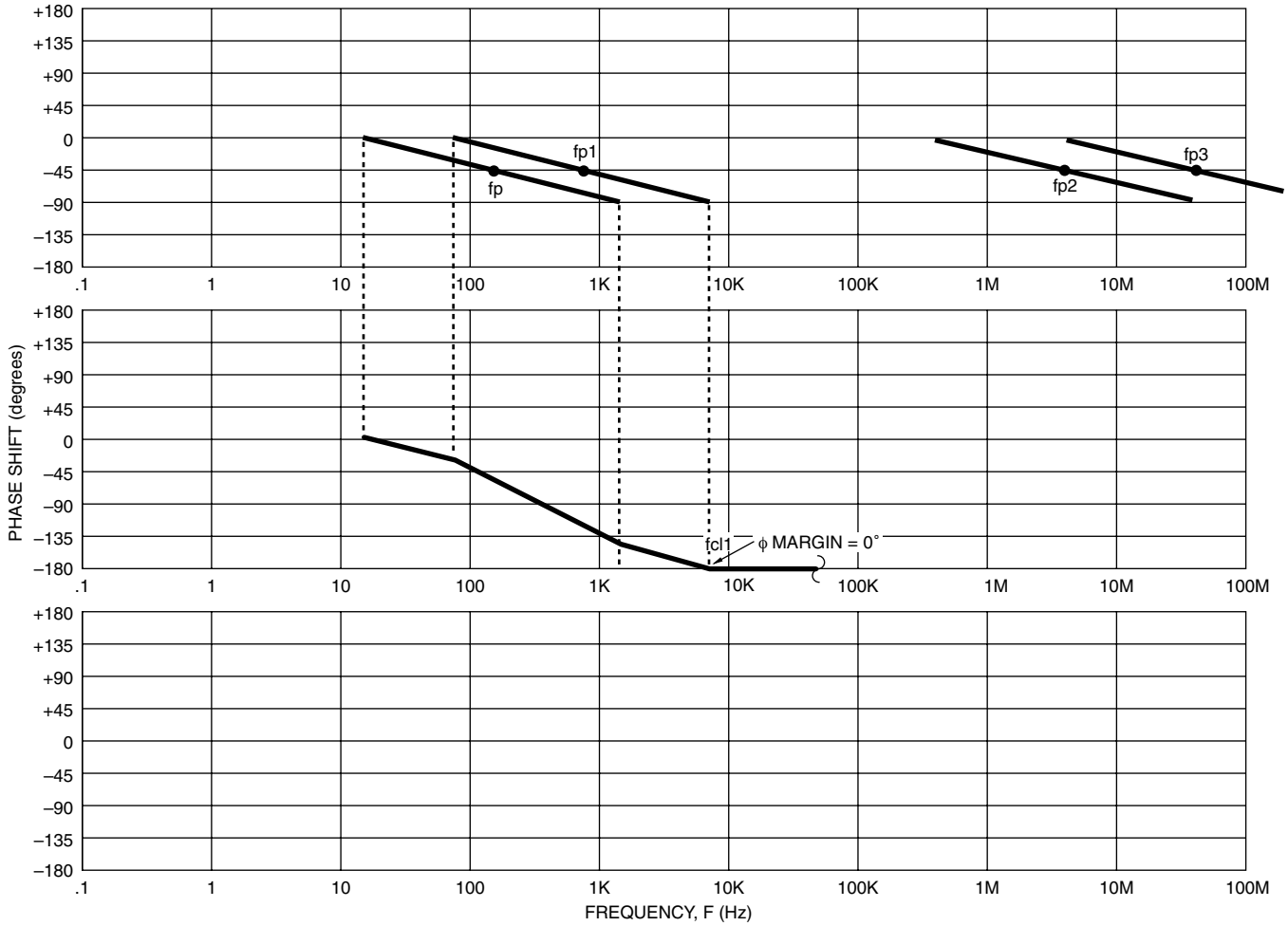


FIGURE 14. OPEN LOOP PHASE PLOT FOR STABILITY
CURVE ① (w/o R_{ISO})

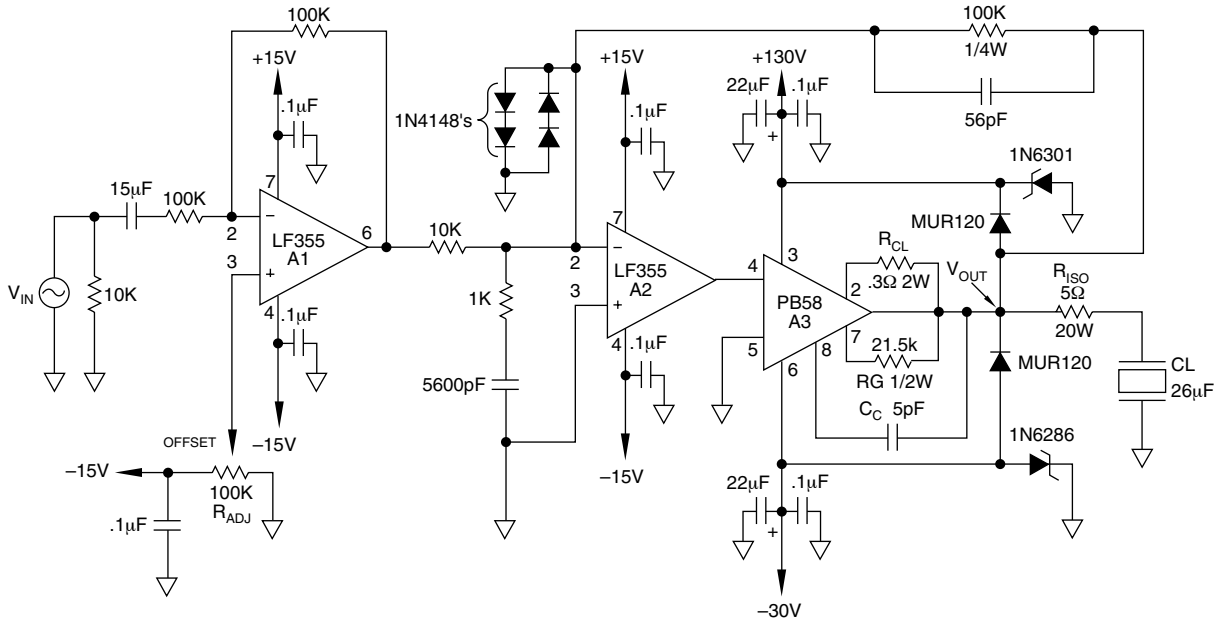


FIGURE 16. PB58 PIEZO DRIVE w/R_{ISO}

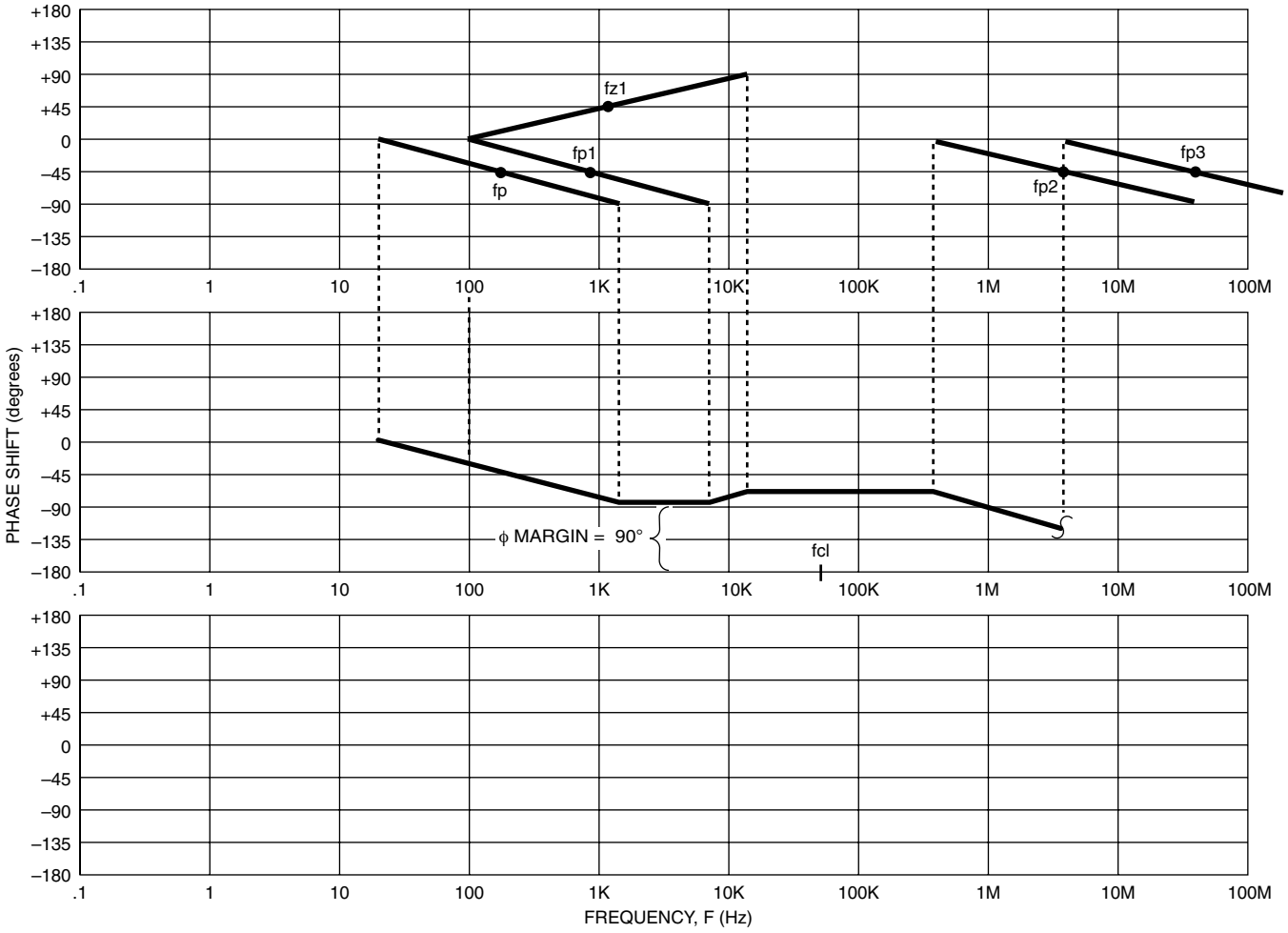


FIGURE 15. OPEN LOOP PHASE PLOT FOR STABILITY
CURVE ② (w/R_{ISO})

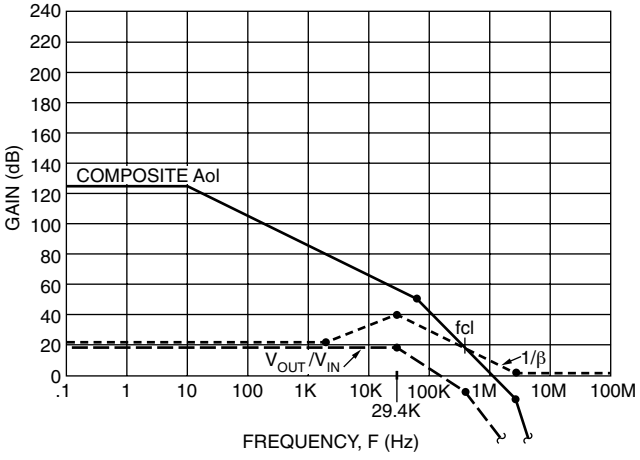


FIGURE 18. COMPOSITE MAGNITUDE PLOT FOR STABILITY

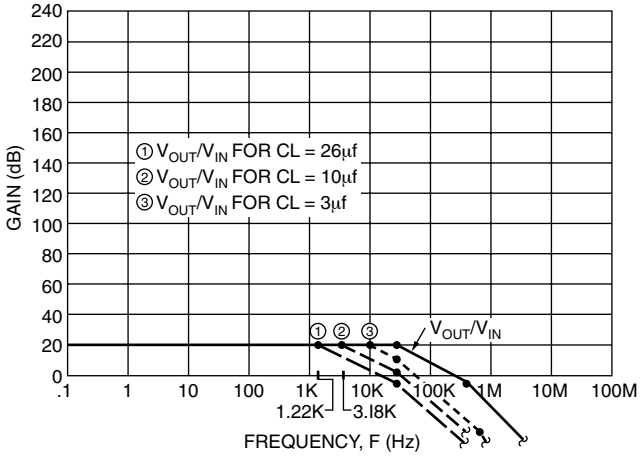


FIGURE 20. V_{OUT}/V_{IN} FOR VARIOUS CL

composite amplifiers, refer to APEX Application Note 19. Figure 18 (see second page following this one) illustrates the 1/β plot selected for good stability. Note the V_{OUT}/V_{IN} relationship which will be discussed later. Figure 19 (see second page following this one) verifies good stability through the open loop phase plot.

Since output voltage across CL is not controlled directly, it is of interest to see how the V_{OUT}/V_{IN} relationship changes with capacitive loads. Figure 20 shows the V_{OUT}/V_{IN} which is at the output of the amplifier. Curves 1 thru 3 show the effect of the additional V_{OUT}/V_{IN} pole formed by R_{ISO} and CL. As the capacitive load is decreased it's possible to gain a wider bandwidth since the additional pole due to R_{ISO} and CL is moving out higher in frequency.

So far the small signal response for this amplifier has been examined. The large signal response has two limitations. The first is slew rate. The slew rate for the composite is limited to slew rate of the front end times the booster gain. In this case S.R. = 5V/μS X 10 = 50V/μS. The upper frequency of a sinewave we can track is a 120Vpp sinewave of 133KHz from S.R.=2 π f V_{OP}. This is not a limiting factor for this circuit

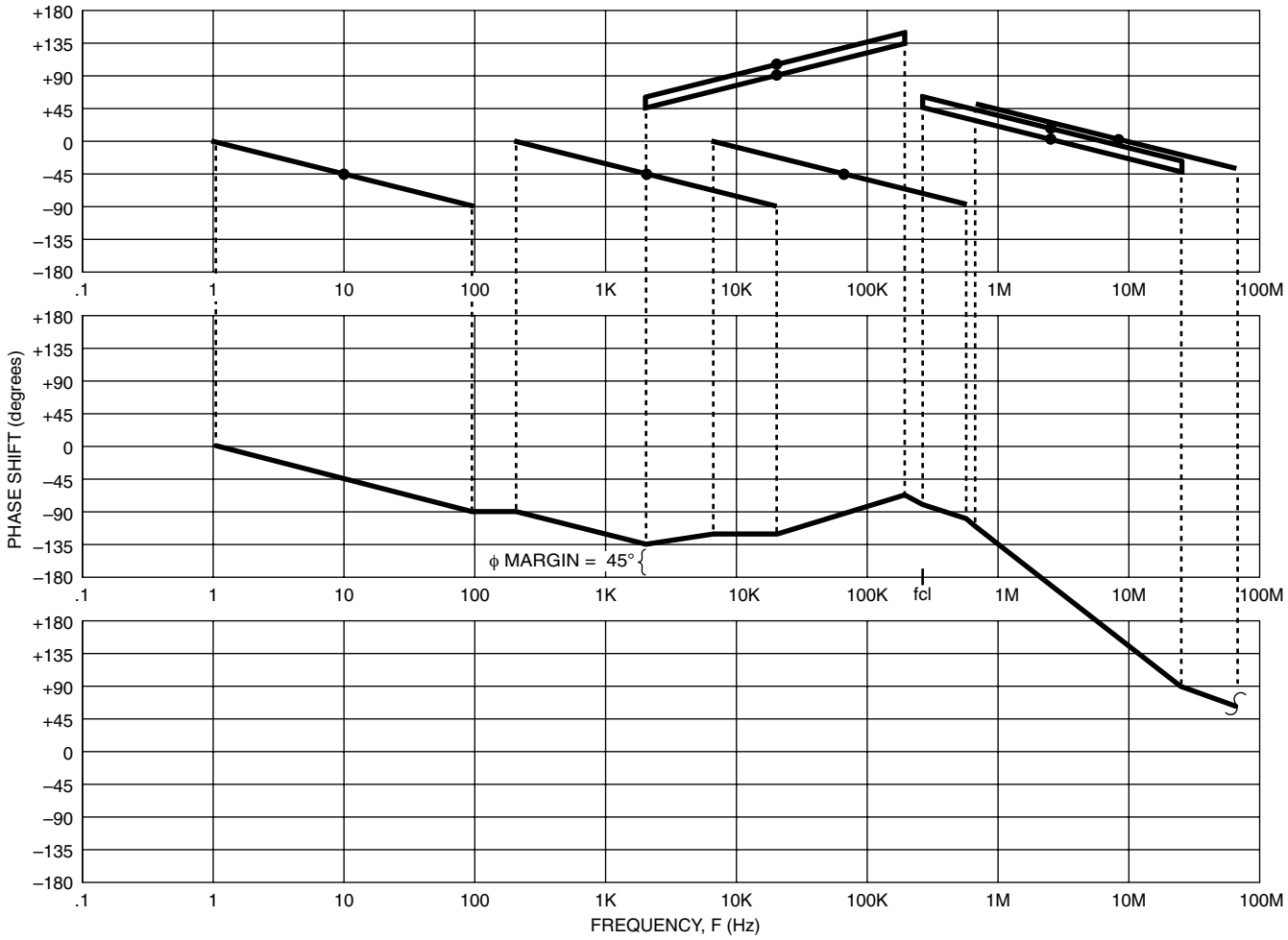


FIGURE 19. COMPOSITE OPEN LOOP PHASE PLOT FOR STABILITY

since the small signal bandwidth begins to roll off at 28.4 KHz for V_{OUT}/V_{IN} (refer to Figure 20). The second large signal limitation is current drive capability. As the capacitive load is increased, the impedance is lowered as the frequency increases. This translates to higher currents.

The following is lab data taken on the circuit of Figure 16 for power response:

POWER RESPONSE (Ilim = 1.3A)

CL = 10μF	f	V_{OUT}
	400Hz	100Vpp
	700Hz	50Vpp
	4KHz	10Vpp
CL = 22μF	f	V_{OUT}
	200Hz	100Vpp
	400Hz	50Vpp
	2KHz	10Vpp

Of equal interest is the power supply rejection for this composite since the choice of front end amplifier will change this number to some degree. The following lab data for the circuit of Figure 16 illustrates the PSR for the positive supply.

POSITIVE POWER SUPPLY REJECTION
(DC set for +Vs = +110V, AC set for 2Vpp Ripple)

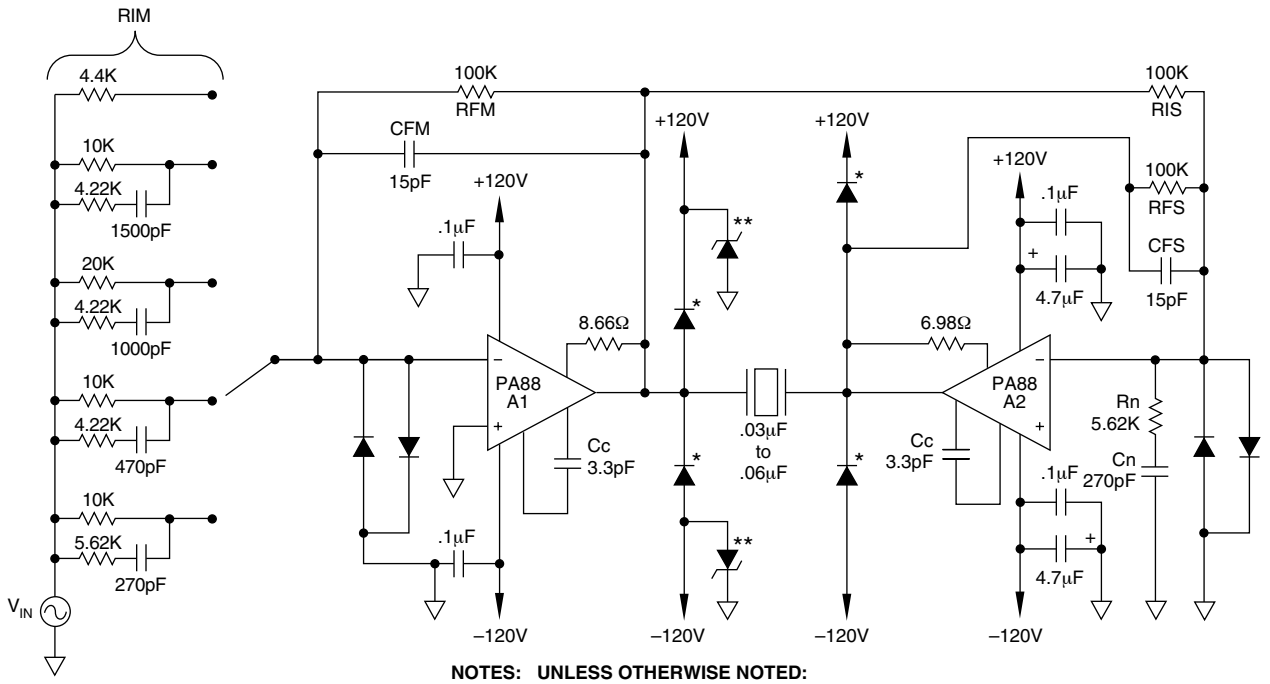
f	V_{OUT} Ripple	Attenuation	Referred to input	PSR
1KHz	30mVpp	.015	.0015	–56.5db
10KHz	290mVpp	.145	.0145	–36.8db
100KHz	420mVpp	.210	.0210	–33.6db

3.2 CAPACITIVE LOADS AND GAIN SWITCHING

Often times in an end product or test system a customer desires control over the gain setting for the amplifier. With any load this raises some important questions. Capacitive loads only complicate matters somewhat.

Figure 21(see next page) shows a bridge circuit for driving piezo transducers. The bridge circuit allows up to twice the peak voltage across the load than driving the load ground referenced. This is because as A1 goes towards +120V, A2 drives towards -120V yielding up to twice the peak voltage across the load. Correspondingly, the bridge circuit also doubles the voltage slew rate across the load for the same reason. Forcing the master amplifier, A1, to current limit first, equally distributes SOA stresses between A1 and A2 in case of a shorted load.

A range of loads was defined for this amplifier as shown in Figure 21. The key to successfully changing the gains in this circuit is to change the noise gain compensation components as the input resistor is changed to select the desired gain setting. It is HIGHLY RECOMMENDED NOT to switch in different values of Cc around the PA88 amplifier A1 as gains are changed. There are MOSFET gates that are connected to the compensation pins that could be destroyed with compensation capacitor switching. It is also critical for stability that Cc be located directly at the amplifier which does not yield itself easily to switching. Figure 22 (see second page following this one) illustrates the 1/β plots for stability for all selectable gain settings. Notice that the stability technique applied here uses both noise gain compensation on the input along with the feedback zero to maximize phase margin for stability. The modified Aol curves are shown for CL =.06μF and CL =.03μF. Output impedance for the PA88 of 100 ohms was used. Figures 23,(see next page) 24,(see second page following this one) and 25 (see third page following this one) prove through open loop phase plots that good stability is guaranteed. Open loop phase plot for



NOTES: UNLESS OTHERWISE NOTED:

1) ALL DIODES ARE 1N4148; *DIODES = 1N5617; **TRANSZORBS = 1N6300 or 1.5KE160

2) USE HS02 HEATSINK @ 25°C AMBIENT

FIGURE 21. PA88 BRIDGE PZT DRIVE WITH SELECTABLE GAIN

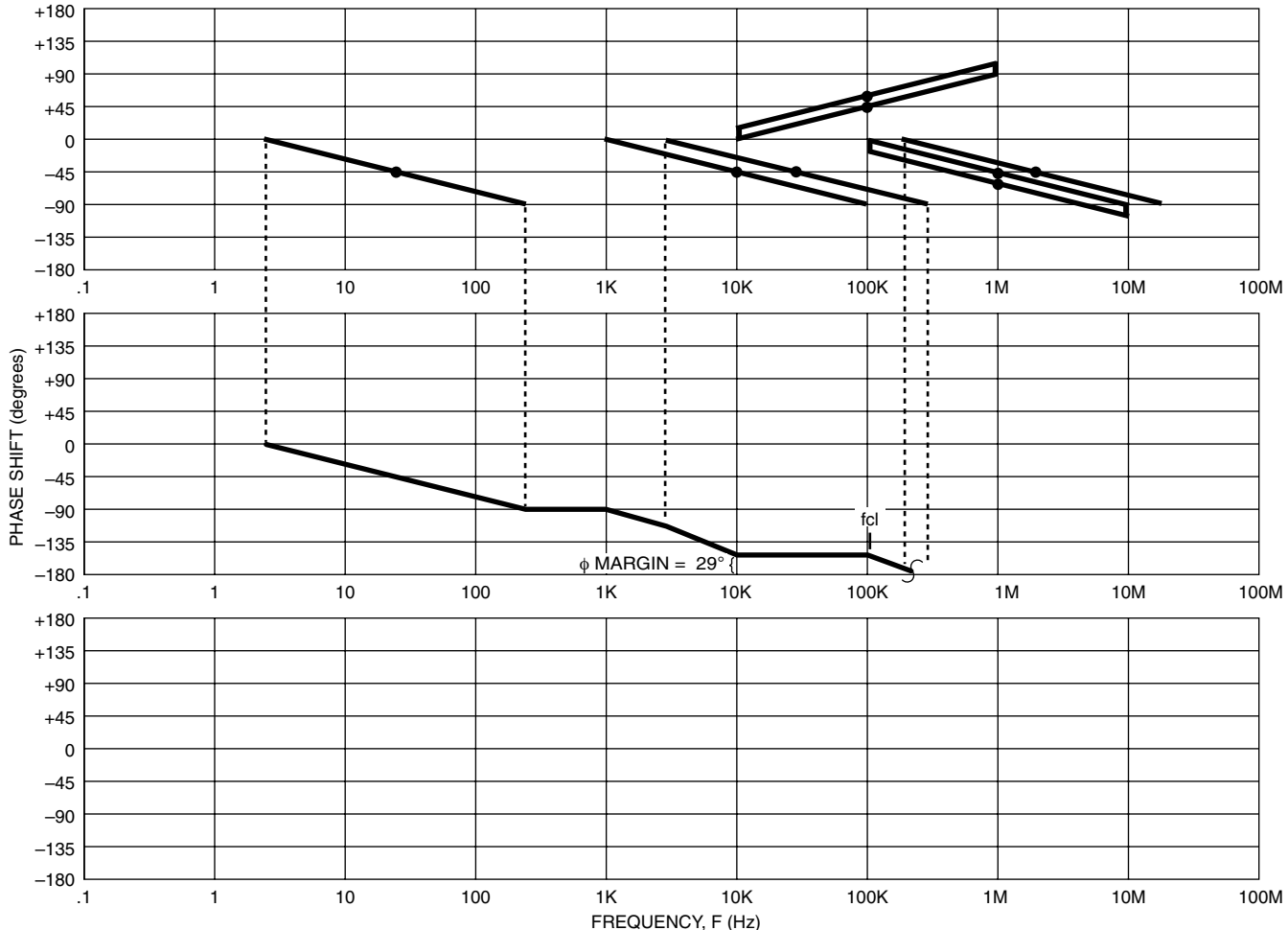


FIGURE 23. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT
CL = .06μf GAIN = 6dB

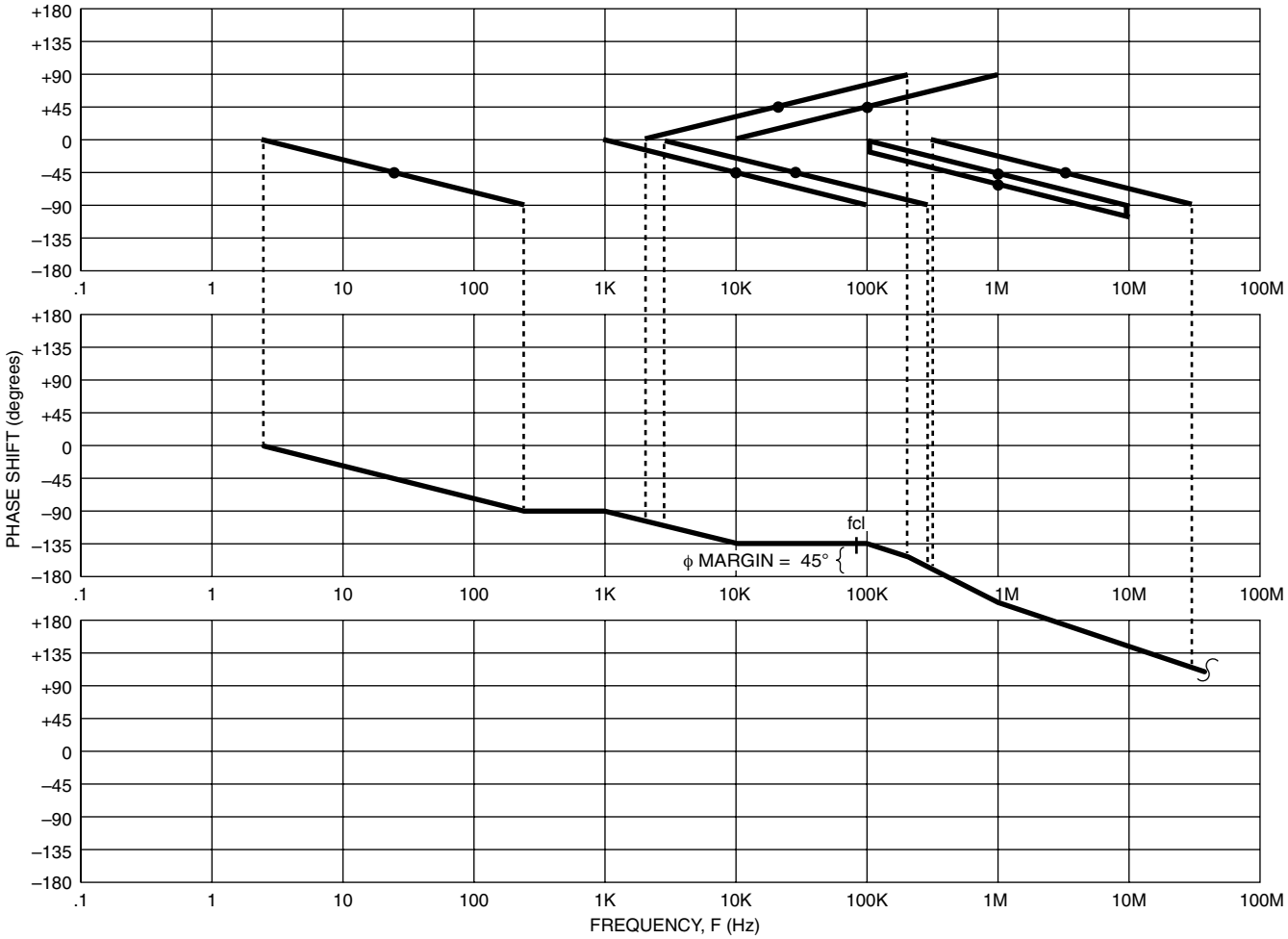


FIGURE 24. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT
CL = .06μf GAIN = 20dB

A2 will be the same as Figure 23.

3.3 HIGH ACCURACY, HIGH VOLTAGE, LOW COST PZT DRIVE

Figure 26 (see next page) is an example of a high accuracy (input offset = 60μV), low drift high voltage amplifier. Though only used here at +/-60V, the PA41 can be used up to +/-175V supplies. The PA41 is a low cost monolithic ASIC designed for high voltage. The limitations of the high voltage ASIC technology do not allow for optimization of input characteristics, thus the PA41 has a 60mV input offset voltage. In high voltage applications where low drift or high accuracy are desired this can be accomplished through the use of a composite amplifier which uses a low cost monolithic front end amplifier to control accuracy and drift. The PA41 now acts as a voltage and current booster.

There are three simple steps to stabilize a composite with a capacitive load:

STEP 1: Compensate PA41 for stability first: Refer to Figure 27(see second page following this one) which shows how capacitive load modifies Aol. Figure 28 (see second page following this one) confirms that the selected 1/β plot will guarantee stability for the PA41.

STEP 2: Create composite Aol: Refer to Figure 29 (see second page following this one) which shows addition of closed loop gain of PA41 to OP07 Aol on dB plot to yield net Composite Aol.

STEP 3: Compensate composite op amp: Figure 30 (see third page following this one) shows the selected 1/β plot to stabilize composite amplifier. Both noise gain compensation and feedback zero compensation are used to maximize stability. Figure 31 (see third page following this one) plots the open loop phase for the composite amplifier yielding 50 degrees phase margin and good stability.

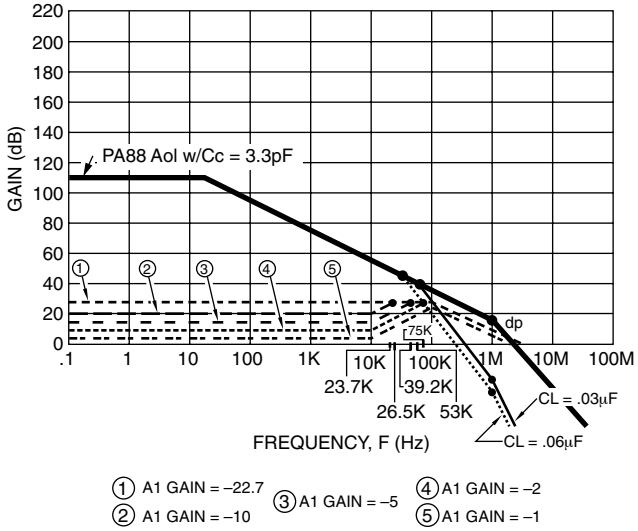


FIGURE 22. A1: MASTER AMPLIFIER MAGNITUDE PLOT FOR STABILITY

3.4 HIGH HIGH VOLTAGE AMPLIFIER CIRCUIT

Figure 32 (see third page following this one) illustrates the current state of the industry with regards to highest voltage available using op amps. This bridge circuit will give us up to +/-1160V across the load.

Remember when using the PA89 to pay particular attention to input protection, heatsinking (low quiescent current times high voltage ==> power dissipation!), components (power dissipation and voltage coef-

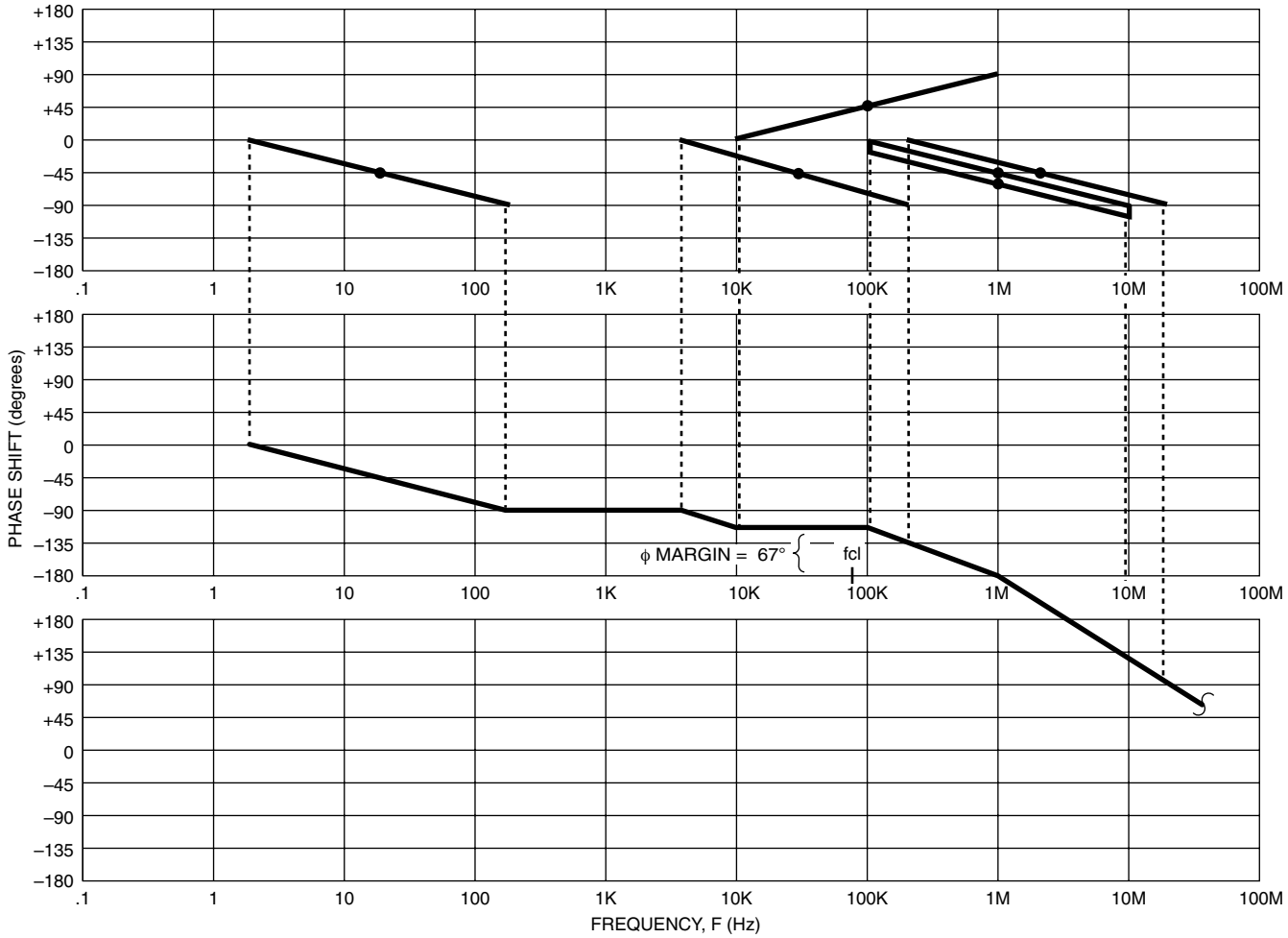


FIGURE 25. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT
CL = .06μf GAIN = 27.5 dB

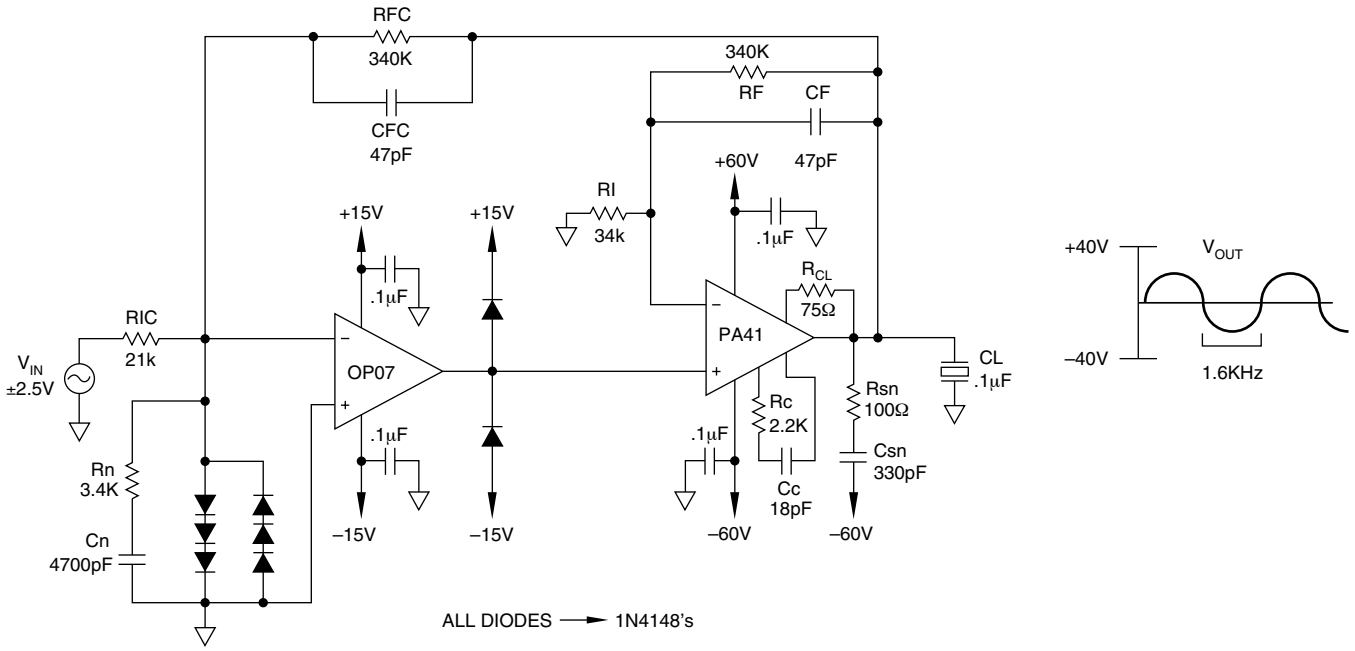


FIGURE 26. PA41 COMPOSITE PIEZO TRANSDUCER DRIVE

ficient of resistance), and compensation capacitor (1200V rating necessary).

3.5 860Vpp SINGLE SUPPLY PIEZO DRIVE

Occasionally it is desired to provide a bipolar drive to a capacitive load using only a single supply. This will reduce area and cost by only requiring one power supply. It will however require the use of a bridge circuit with two high voltage amplifiers.

Figure 33 (see second page following this one) is an implementation of an 860Vpp piezo drive. There are four simple steps to setting up the single supply scaling:

STEP 1: Define maximum V_{OP}:
MAX V_{OP} = +Vs - VsatA - VsatB
MAX V_{OP} = +450 - 10V -10V = 430Vp

STEP 2: Calculate gain:
Gain = V_{OPP} / V_{INPP} = (VA - VB)pp / V_{INPP}

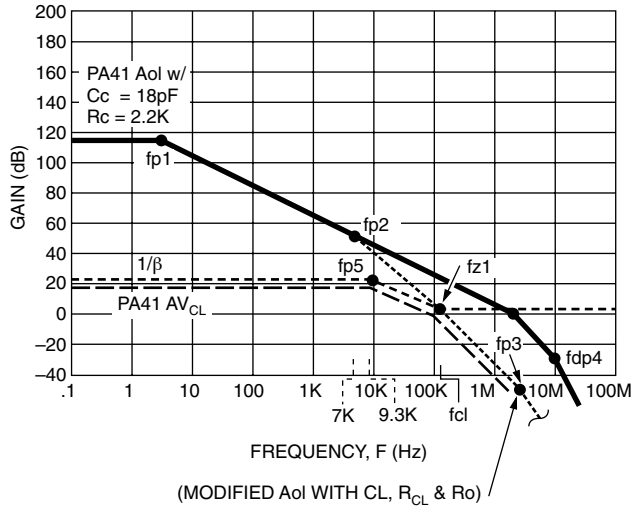


FIGURE 27. POWER OP AMP MAGNITUDE PLOT FOR STABILITY

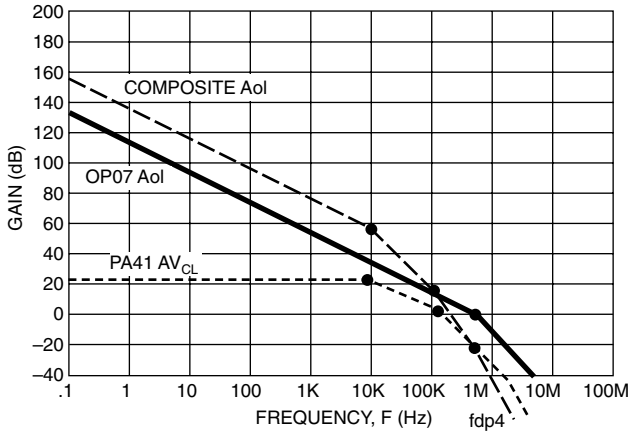


FIGURE 29. COMPOSITE AMPLIFIER Aol MAGNITUDE PLOT

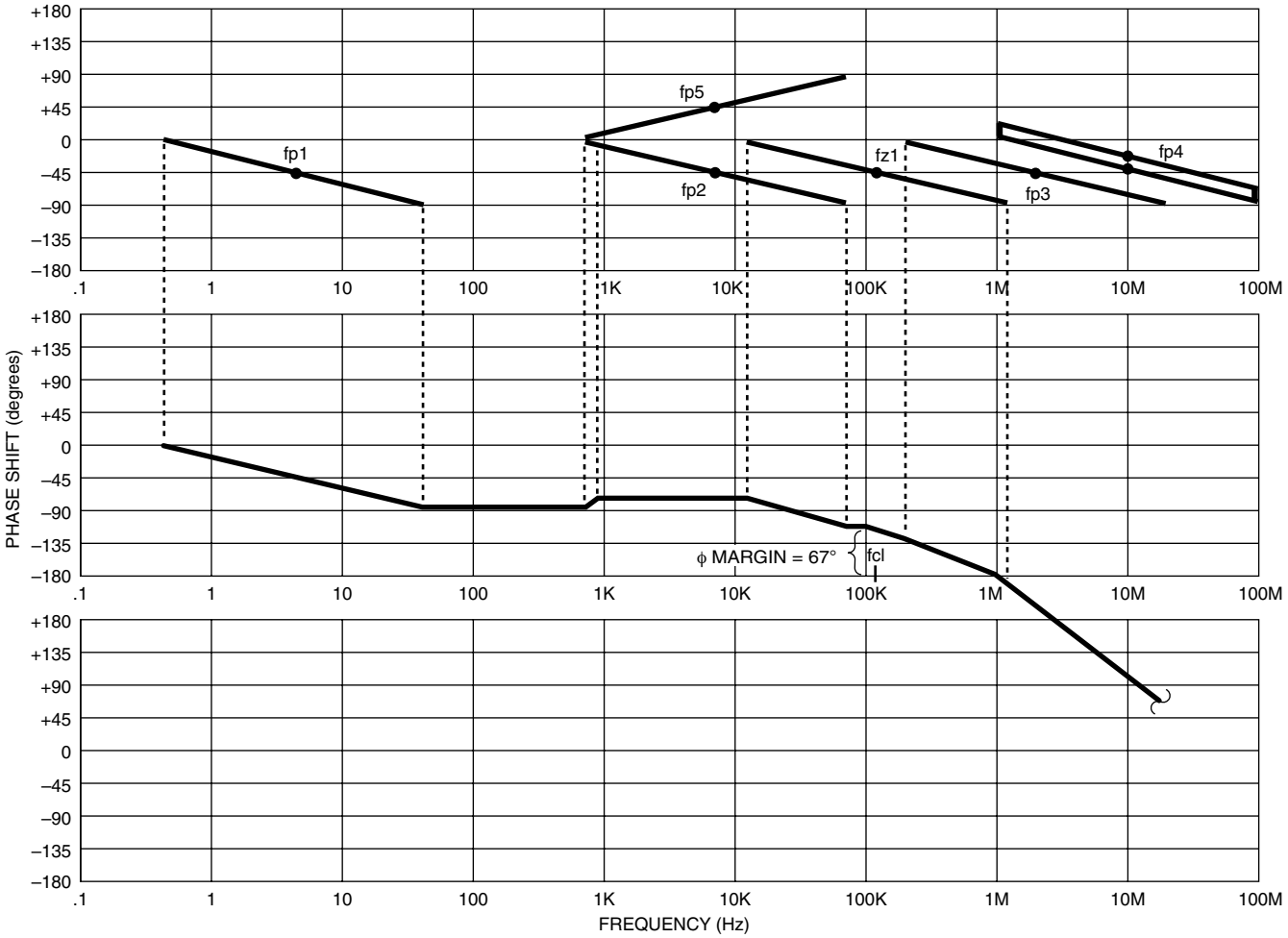


FIGURE 28. POWER OP AMP OPEN LOOP PHASE PLOT FOR STABILITY

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Gain = 860Vpp / 12Vpp = 71.67
Gain = 2 RF/RI with the bridge configuration. That is the voltage gain across the load is twice that of the master amplifier, A, since +1V out of amplifier A yields -1V out of amplifier B, relative to the midpoint power supply reference of +225V. Therefore: RF/RI = 71.67/2 = 35.833

STEP 3: Calculate offset:

$$VA - VB = +Vs(2\ (1+ RF/RI)\left(\frac{RB}{RA + RB}\right) - 1) - 2(RF/RI)V_{IN}$$

But when V_{IN} = 0 then VA-VB =+430V
Using RF/RI = 35.833 and solving above equation yields RA = 36.669RB
Choosing RB = 12K implies RA = 440K

STEP 4: Check for common mode voltage compliance:

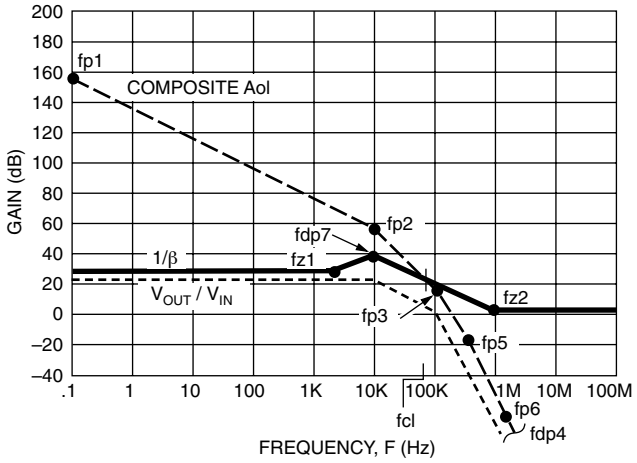

FIGURE 30. COMPOSITE AMPLIFIER MAGNITUDE PLOT FOR STABILITY

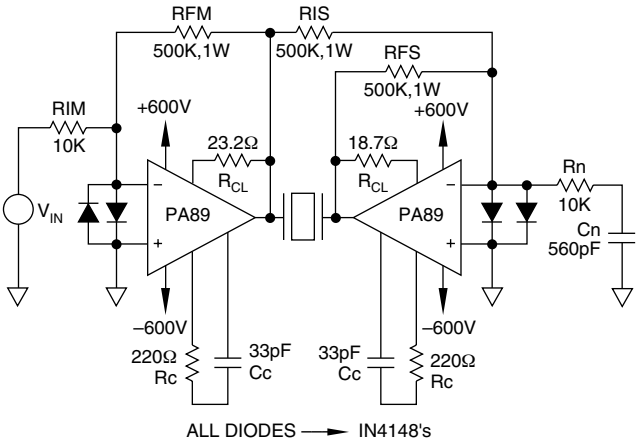

FIGURE 32. ±1160V PIEZO DRIVE BRIDGE

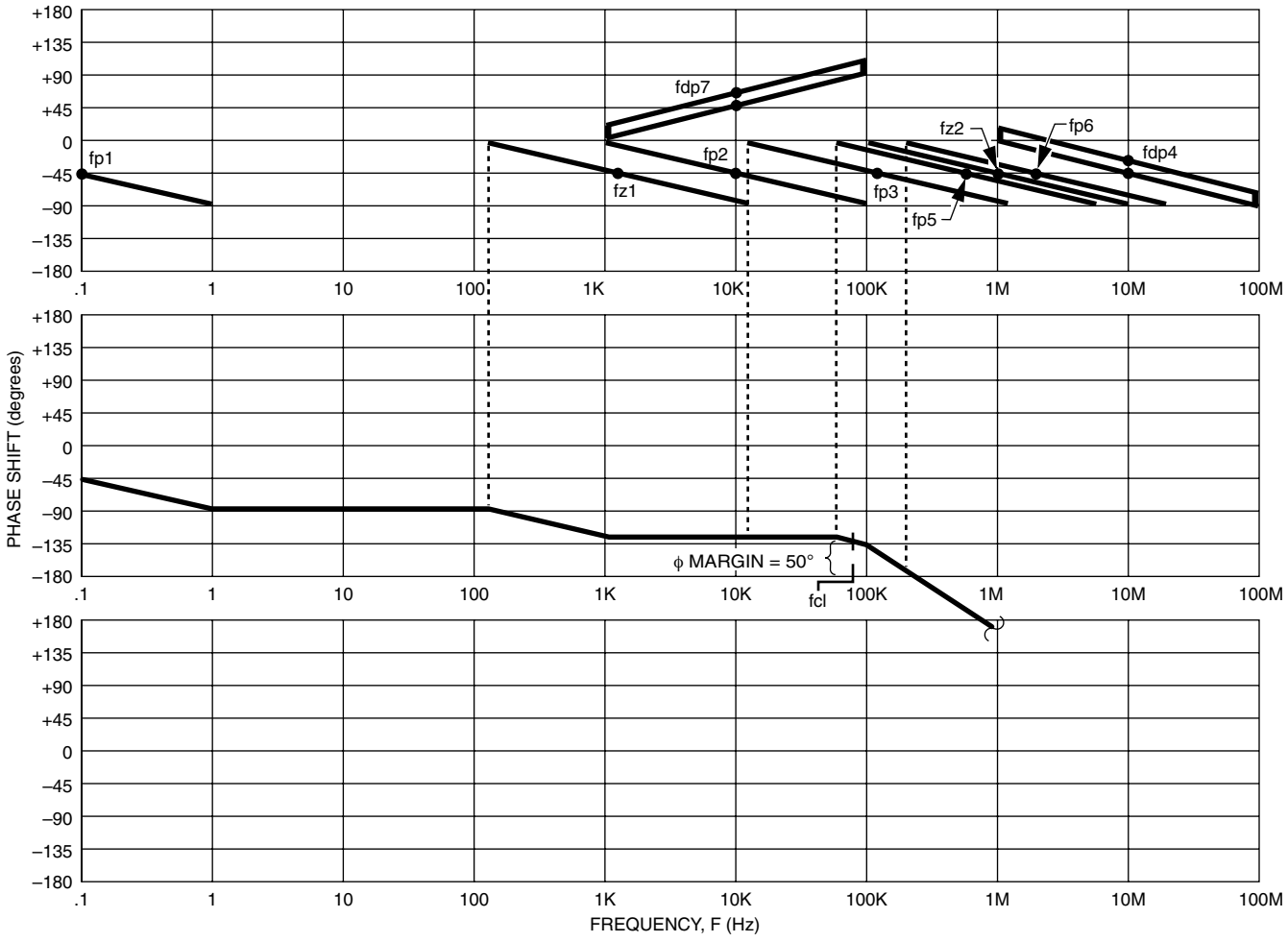

FIGURE 31. COMPOSITE AMPLIFIER OPEN LOOP PHASE PLOT FOR STABILITY

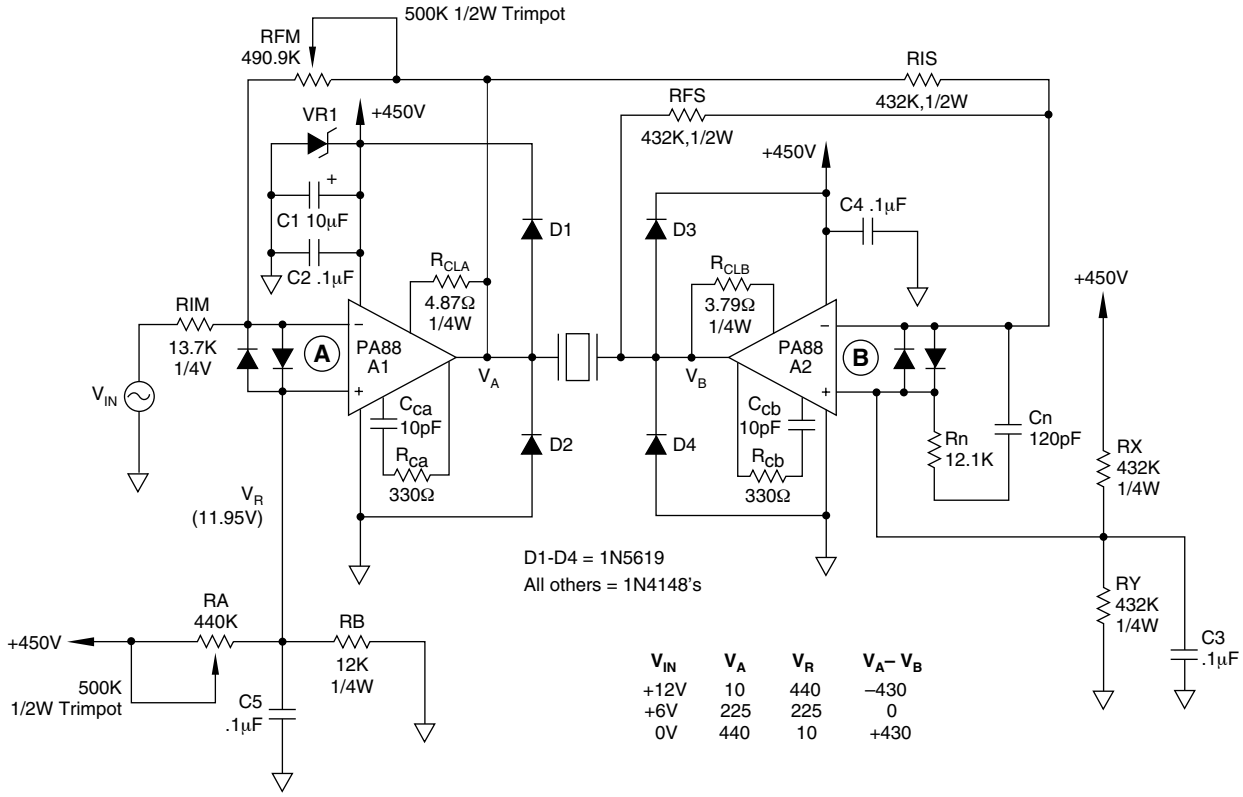

FIGURE 33. 860Vpp PIEZO DRIVE
(SINGLE SUPPLY BRIDGE)

The resistor divider of RA and RB was set to yield the desired offset. These values yield V_R = 11.95V which is greater than the minimum common mode voltage specification of 10V for the PA85.

4.0 FINAL NOTE

You have now looked at several ways to drive capacitive loads using high voltage amplifiers. The techniques presented here are intended to enable you to complete your circuit designs in a short time.

If there are additional questions or concerns not covered in this application note, please feel free to contact APEX APPLICATIONS ENGINEERING through our TOLL FREE HOTLINE, 800-546-2739 (Canada & USA, outside Arizona), by direct telephone, 520-690-8600, or by using the APEX APPLICATIONS FAX, 520-888-7003.

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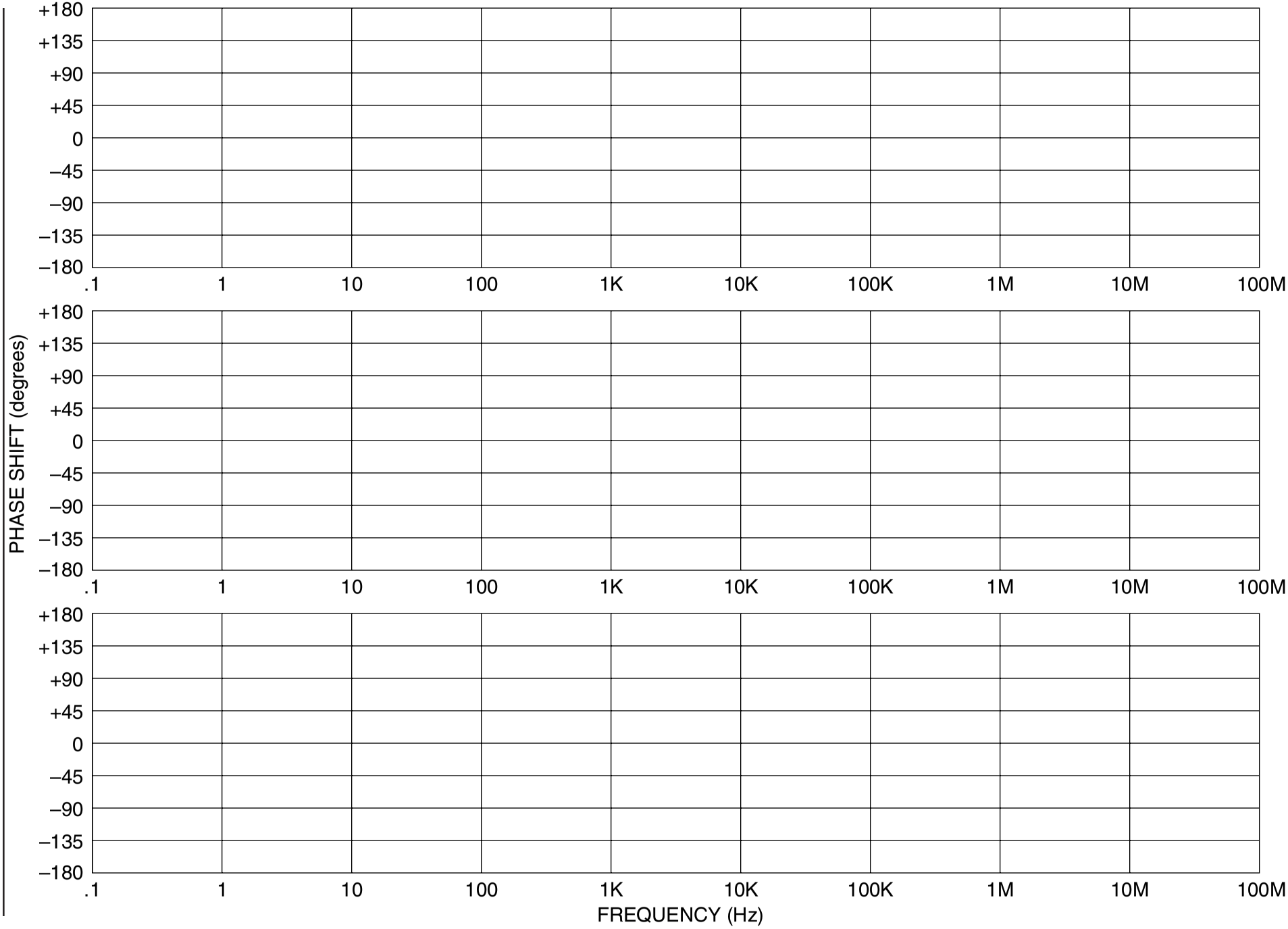
240
220
200
180
160
140
120
100
80
60
40
20
0
GAIN (dB)
.1
1
10
100
1K
10K
100K
1M
10M
100M
FREQUENCY (Hz)



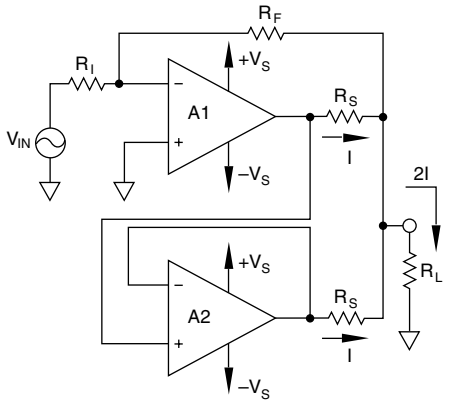
PARALLEL CONNECTION OF POWER OP AMPS

Power op amps can be paralleled to increase current, improve SOA (Safe-Operating-Area), or double thermal capability. While the basic topology seems simple, there are design details which require careful attention such as common-mode range considerations, stability, slew rate, and losses which can reduce efficiency and increase power dissipation.

1.0 BASIC PARALLEL TOPOLOGY

A1 in Figure 1 referred to as the master amplifier, can be configured in any form desired, inverting or non-inverting, and any gain desired. Feedback for A1, and only A1, will come from the overall output of the parallel connection. The output of each amplifier will have in series equal small-value resistors to improve current sharing characteristics. The slave amplifiers, A2 and up to An, are configured as unity gain non-inverting buffers driven from the output terminal of the master amplifier A1. Each slave's individual feedback is taken directly at its output terminal.

The idea of this connection is since each slave is a unity gain buffer, the slave outputs will match as closely as possible the output of the master. Yet with the master feedback being wrapped around the entire circuit, overall accuracy is maintained.



CONSIDERATIONS

- $I_{LOSS} = V_{OS}/2R_S$
- $V_{LOSS} = I_{OUT}R_S$
- SLEW RATE MISMATCH WILL GIVE LARGE I_{CIRC}

FIGURE 1. BASIC CONNECTION.

2.0 LOSSES

The output of the slaves in this configuration will not exactly match the master. Since the slaves operate at unity gain, the difference will be equal to the worst case offset of a single amplifier for two amplifiers in parallel since only the offset of the slave causes this mismatch. With more than one slave, each slave could have worst case offset in opposite directions, and in the worst case, the mismatch is twice the input offset voltage.

These offset voltages produce a drop across the current sharing resistors and a corresponding current flow. This is current that is "lost", never appearing in the load and increasing amplifier dissipation.

2.1 CURRENT SHARING RESISTOR CHOICE

Increasing values of current sharing resistors will reduce the circulating current loss. But this improvement must be weighed against direct losses through the current sharing resistors when delivering current to the load. The challenge to the designer is to find the happy medium for Rs values. As a general rule, power amplifiers will be used with Rs values of from 0.1 ohm to 1.0 ohm.

3.0 CURRENT LIMITING

Current limit of the master should be set 20% lower than the slaves if possible, and the ultimate current limit of the overall circuit will be that limit multiplied by the total number of amplifiers. The idea here is the master current limits first, and since it provides the drive for all other amplifiers, that drive is also clipped. This insures equal sharing of all stresses during current limit.

4.0 SLEW RATE CONSIDERATIONS

Assume an initial condition where the output of the circuit in Figure 1 is resting close to the negative rail. Then apply a step function to the input of the master amplifier to drive the output positive. The output will slew as fast as the amplifier's slew rate to the positive rail. With the slave being driven from the master, the slave doesn't get its input transition until the master slews, and then the slave requires additional time to slew positive.

In the interval where the master has reached positive output and the slave is trying to catch up, there is a large difference in the output voltage of the two amplifiers developing current through the two current sharing resistors. This can be a large current equivalent to the current limit of the amplifier. That's the bad news. The good news is that it is a transient current and as such may be within transient SOA limits. But this can be difficult to prove for certain.

When in doubt, the best rule of thumb is to not use the parallel connection at greater than half the rated slew rate of the amplifiers.

5.0 STABILITY CONSIDERATIONS

For detailed information on stability, refer to Application Note 19, "Stability For Power Operational Amplifiers". All discussion here is based on the stability theory contained in Application Note 19.

5.1 SLAVE STABILITY

The most obvious problem from a stability standpoint is the unity gain buffer connection of the slaves. This configuration has the least ability to tolerate poor phase margin. Poor phase margin usually occurs as a result of excessive capacitive loading. But in the case of the PA12, the unity gain buffer connection should not be used without additional compensation. Externally compensated amplifiers should normally be compensated for unity gain and may still require additional compensation. Alternatively, they may be decompensated to improve slew rate and use noise gain compensation to insure stability.

The most common way we recommend to compensate the slave is with a noise gain compensation network across the inputs to the amplifier. However, for noise gain compensation to work, there must be impedance in the feedback path. Figure 2 shows the modifications necessary to incorporate noise gain compensation.

The R_{FS} value of Figure 2 is somewhat arbitrary, but its choice will dictate the final values of Rn and Cn. As is the general case in any op amp circuit, excessive impedance for RFs is something to be avoided. A realistic range of values for RFs is from 1 KΩ to 1 MΩ with a good starting point being 10 KΩ.

Once the value of R_{FS} is pegged, noise gain compensation should usually be set to give a noise gain of 10. This corresponds to Rn being one-tenth Rf. Cn must be found analytically according to procedures outlined in Application Note 19 after considering the effects of amplifier bode plot and additional poles resulting from capacitive loading. In many cases, selecting Cn for a corner frequency of 10KHz based on the value of Rn (Xcn = Rn@10KHz) will result in a stable circuit; although, analytical methods will maximize bandwidth in comparison to this method.

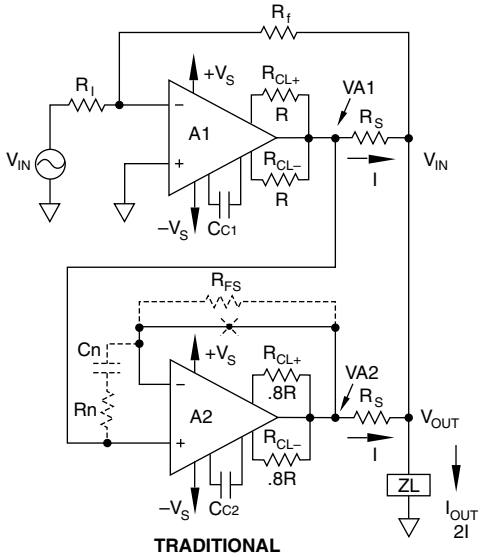


FIGURE 2. SLAVE STABILITY.

5.2 MASTER STABILITY

A1 is subject to all normal considerations for stability. If A1 is a gain of 10 or greater, its stability will be equal to that of the slave with noise gain compensation described above. At gains below 10, the optimum noise gain will be a gain of 10 to match the slaves.

6.0 COMMON MODE CONSIDERATIONS

The unity gain buffer configuration must be able to accept inputs equal to the maximum output swing of the master. This will be a problem in MOST cases. The following is a list of op amp models in which the output voltage swing exceeds the acceptable input common-mode range:

PA02 ..... (Special problems)
PA03
PA04 ..... (Boost equipped)
PA05 ..... (Boost equipped)
PA07 ..... (Special problems)
PA08
PA09 ..... (Special problems)
PA19 ..... (Special problems)
PA21, 25, 26 ..... (Usually OK)
PA41
Any PA8X

PA21, PA25, PA26 are listed only because, according to the product data sheet, it is possible to have common-mode violations in the parallel connection. However, this is only likely when lightly loaded and the PA21, PA25, PA26 behavior is so good under common mode violation conditions that it is not likely to be a problem.

Special problem amplifiers deserve special mention. The PA02 does not lend itself to parallel connection. Negative inputs which get within 6 volts of the negative supply rail can cause output polarity reversals which can be catastrophic in the parallel connection.

In the PA07, PA08, PA09, all PA8X, or anything with JFET input stages, common-mode violations can cause output reversals and common-mode range is restricted to no closer than 10 to 12 volts within the supply rails.

6.1 OVERCOMING COMMON MODE RESTRICTIONS

A method most useful with high voltage amplifiers where currents are low, is to simply use zener diodes in series with the supply line to the master amplifier as shown in Figure 3A. These drop the master supply low enough to restrict its output swing to be within the common-mode range of the slaves. Determine wattage ratings based on expected load + quiescent current flow.

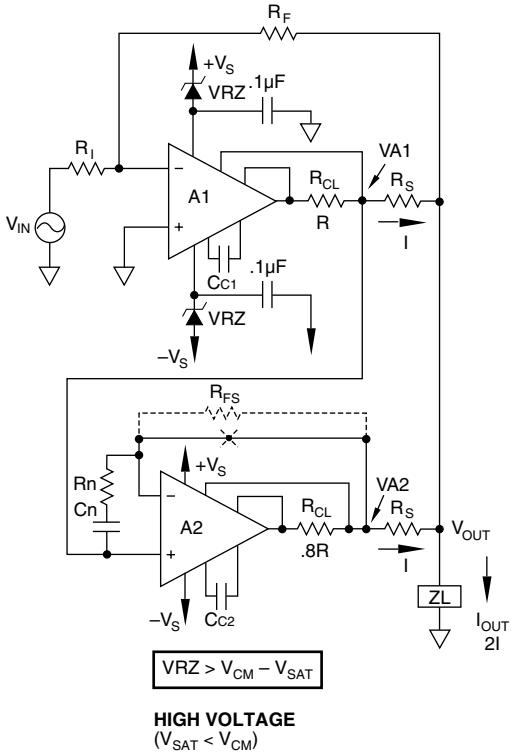


FIGURE 3A. OVERCOMING COMMON MODE RESTRICTIONS.

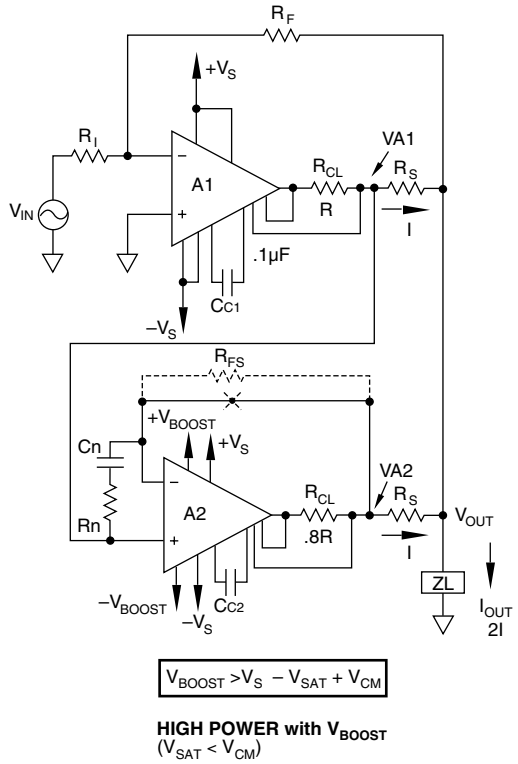


FIGURE 3B. OVERCOMING COMMON MODE RESTRICTIONS.

The PA04 and PA05 present another opportunity to overcome common-mode limitations by taking advantage of their boost pins. Originally incorporated to improve output voltage swing, we effectively increase common-mode range by increasing front-end supply voltages. A boost of at least 5 volts will be adequate to overcome this limitation. Figure 3B elaborates on this connection.

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Other methods include operating slaves on slightly higher voltages than the master. This is what is accomplished with the zeners described previously, but is not easily applied to high current power amplifiers unless they have boost voltage provisions. In such cases the zeners can be included in series with the Vboost pins of the master amplifier.

It may seem possible to attenuate the output of the master and set the slaves up with corresponding gain, but it will be found that unless very strict matching requirements of the associated resistors are met, extremely large circulating currents will flow.

7.0 BRIDGE CIRCUITS

The master-slave combination once realized and taken as a whole, comprises one effective op amp. Treated this way, incorporation into a bridge circuit is simply a matter of using an inverting unity gain configuration on the slave side of the bridge (note that the slave of the parallel combination and the slave side of a bridge are two different things). Bridge techniques are discussed in detail in Application Note 20, “Bridge Operation”.

8.0 SINGLE SUPPLY

There are no unique considerations concerning single supply except those described in Application Note 21, “Single Supply Operation”. Again, as in the bridge, treat the parallel combination as a single op amp.

APPLICATION NOTE 28

POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

1.0 AVOID PREDICTABLE FAILURES

This brief application note is intended to guide you through successful prototyping and final construction of power op amp circuits by using proper component location and interconnection techniques.

Proper analog construction of power op amps is just as critical as choosing the proper power op amp, heatsink, or schematic design. For reliable success, you should treat all power op amps as high frequency devices. Even though you may have designed a circuit to operate at 400Hz, the amplifier will, in general, have a bandwidth capability out to 4MHz or so and will be happy to oscillate at that frequency if not constructed properly.

In addition to this application note, be sure to read "General Operating Considerations" in the Apex handbook for details on stability, supplies, heatsinking, mounting, current limit, SOA, and specifications interpretation.

2.0 PROPER MECHANICAL MOUNTING

Refer to Figure 1. This side view of the amplifier mounted to a heatsink shows optimum mounting to allow for wiring ease of the peripheral components associated with the power op amp. Notice the necessity of teflon sleeving to insulate the amplifier leads from the heatsink; the use of a mating socket for ease of solderable component connections; and the use of an Apex thermal washer (or thermal grease) as the only approved interface between the amplifier and the heatsink.

You also want to be sure the recommended mounting torque of 4-7in-lbs (.45-.79 N-m) for the 8-pin TO-3 package and 8-10in-lbs (.90-1.13 N-m) for the Power Dip, JEDEC MO-127, package is used. This torque needs to be applied in small increments alternating between the two mounting bolts, similar to tightening the lug nuts on a car tire.

2.1 8-PIN TO-3 MOUNTING

Since the 8-pin TO-3 package is more sensitive to improper mounting torque, here is a rule of thumb for those who do not have ready access to a torque screwdriver:

i) After an Apex thermal washer or grease is applied and the teflon sleeving installed on the leads, assemble the power op amp onto the heatsink and press it firmly into the mating socket until it is firmly seated and there is no gap in the assembly.

ii) Insert the two mounting bolts through the mounting holes in the flange of the amplifier and tighten them "finger-nail" tight. Literally use your fingernail as a screwdriver. This ensures no overtorque and gives a starting point so that the nut fits snugly against the mating socket.

iii) After using "finger-nail" tightening, one complete revolution on the head of each mounting bolt is 4-7in-lbs. Apply this torque one quarter of a turn at a time, alternating between the two mounting bolts, until one complete revolution is reached.

3.0 PROPER ANALOG CONSTRUCTION

Figure 2 illustrates a typical inverting power op amp circuit which will be used to discuss proper component locations and wiring. Other power op amp circuits will use similar techniques.

Refer to Figure 3. This Figure shows the proper routing of connections and component locations for the circuit of Figure 2.

The mating socket will be facing towards you to allow for "unlimited" height so a "circuit ball" or "bird's nest" of components can be soldered directly to the mating socket. This will result in an analog construction equivalent to a properly designed printed circuit board.

Note the location of all components associated with the power op amp circuit shown in Figure 2 are directly at the power op amp's mating socket. A single point ground is illustrated by physical connection of the power supply ground, input signal ground, and output load ground.

For the single point ground wire running from the power supply to the power op amp, strip back the wire's insulation about 2 or 3 inches and tin it with solder. This wire can then be bent or "bussed" wherever it needs to go to pick up all ground points for the power op amp and its associated components.

Stand components on end, "cordwood style", or leave them hanging in mid-air, using the leads of the components themselves as interconnection wires.

DO NOT RUN WIRES FROM EACH PIN OF THE POWER OP AMP OVER TO A PIECE OF VECTOR BOARD, PERF BOARD , OR PRINTED CIRCUIT BOARD WHERE THE POWER OP AMP'S ASSOCIATED COMPONENTS ARE LOCATED—THIS WILL BECOME AN OSCILLATORY, ANALOG DISASTER!

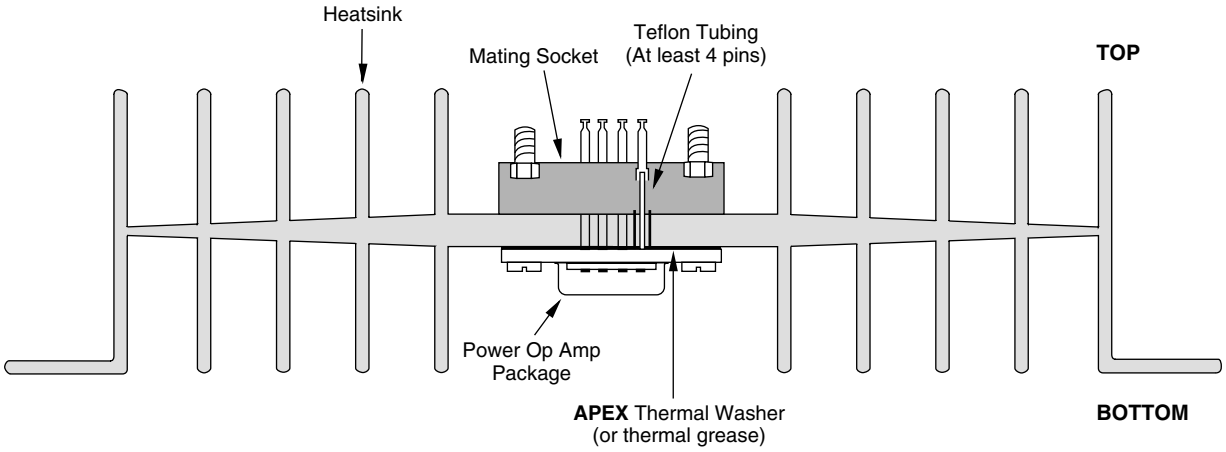

FIGURE 1. SIDE VIEW.

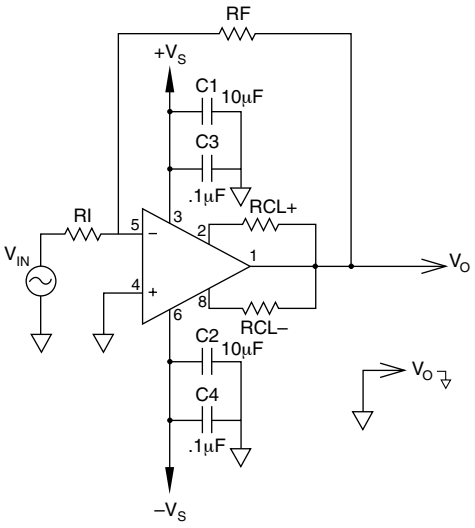

FIGURE 2. SCHEMATIC.

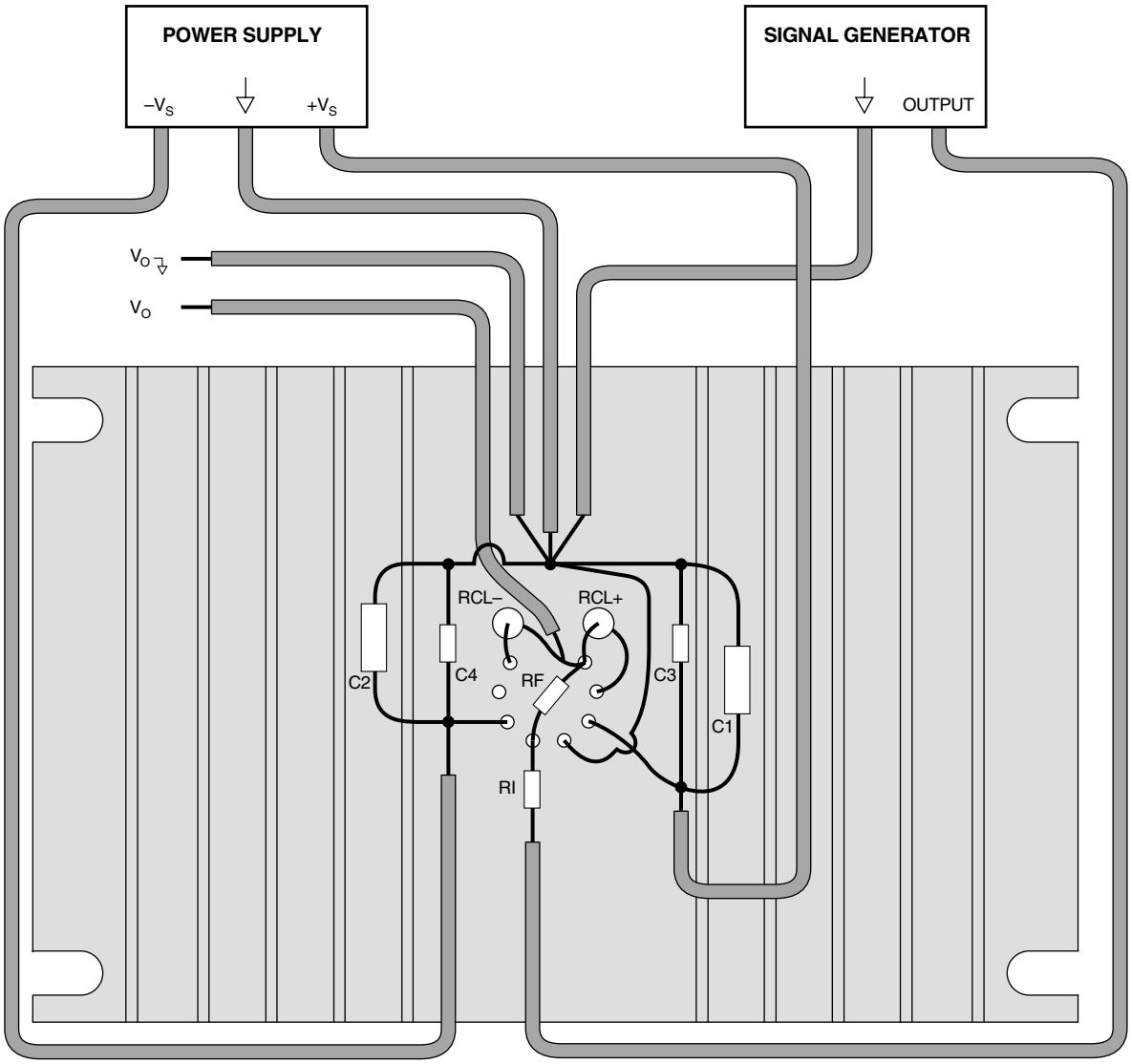

FIGURE 3. TOP VIEW. BOTTOM VIEW OF AMPLIFIER.

APPLICATION NOTE 30

PULSE WIDTH MODULATION AMPLIFIER

INTRODUCTION

This note is divided into three sections. The first section provides general information on Pulse Width Modulation amplifiers and examines a typical block diagram. The second section on designing with PWM amplifiers is NOT intended for optional reading. The family of PWM amplifiers are not all equal in protection features and some of the design errors which would cause a linear amplifier to oscillate will destroy some of the less protected PWM amplifiers. The final section examines some ways to use PWM amplifiers.

PWM circuits are taking the same general course of development traveled by op amps and many other electronic functions. Concepts were brought to life using discrete components and were followed by modules, hybrids and then monolithics. The first hybrids on the scene in PWM technology are the SA01, SA50 and SA51 from Apex. The SA01 and SA50 contain all the functions needed to implement a wide variety of control circuits. The SA01 features three levels of protection circuits and the SA50 and SA51 feature the small TO-3 package. The SA51 will accept digital inputs as opposed to analog inputs of the other two models.

THE WHY AND HOW OF PWMs

As power levels increase the task of designing variable drives increases dramatically. While the array of linear components available with sufficient voltage and current ratings for high power drives is impressive, a project can become unmanageable when calculation of internal power dissipation reveals the extent of cooling hardware required. A 20A output stage often requires multiple 20A semiconductors mounted on massive heatsinks, usually employs noisy fans and sometimes liquid cooling is mandated.

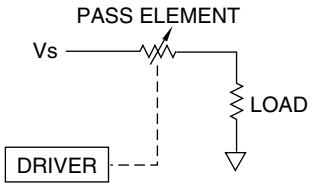

FIGURE 1. LINEAR POWER DELIVERY.

Figure 1 illustrates the linear approach to delivering power to the load. When maximum output is commanded, the driver reduces resistance of the pass element to a minimum. At this output level losses in the linear circuit are relatively low. When zero output is commanded the pass element approaches infinity and losses approach zero. The disadvantage of the linear circuit appears at the midrange output levels and is often at its worst when 50% output is delivered. At this level, resistance of the pass element is equal to the load resistance which means heat generated in the amplifier is equal to the power delivered to the load! We have just found the linear circuit to have a maximum efficiency of 50% when driving resistive loads to midrange power levels. When loads appear reactive this efficiency drops even further.

Figure 2 illustrates the most basic pwm operation. The PWM control block converts an analog input level into a variable duty cycle switch drive signal. As higher outputs are commanded, the switch is held ON longer portions of the period. The switch is usually both ON and OFF once during each cycle of the switching frequency but many designs are capable of holding a 100% ON duty cycle. In this case, losses are simply a factor of the ON resistance of the switch plus the inductor resistance. As less output is commanded the duty cycle or percent of ON time is reduced. Losses include heat generated in the flyback diode. At most practical supply voltages this diode loss is still small because the diode conducts only a very small portion of the time and this voltage drop is a small fraction of the supply voltage.

The job of the inductor is storing energy during the ON portion of the cycle for filtering. In this manner the load sees very little of the switching frequency but responds to frequencies significantly below the switching frequency. A rule of thumb is to expect a usable bandwidth one decade below the switching frequency. Inductive loads often provide adequate filtering without dedicated filters.

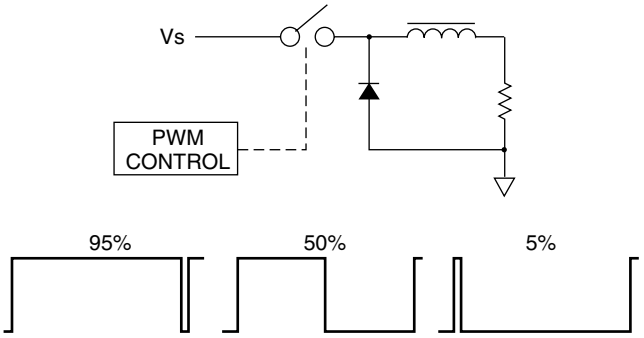

FIGURE 2. PWM POWER DELIVERY.

With the PWM circuit, the direct (unfiltered) amplifier output is either near the supply voltage or near zero. Continuously varying filtered output levels are achieved by changing only the duty cycle. This results in efficiency being quite constant as output power varies compared to the linear circuit. Note that efficiency claims on the hybrid PWM amplifier data sheet do not include filter losses. Typical efficiency of filtered PWM circuits range from 80 to 95%.

Almost all power amplifiers (low duty cycle sonar amplifiers are a notable exception) must be designed to withstand worst case internal power dissipation for considerable lengths of time compared to the thermal time constants of the heat sinking hardware. This forces the design to be capable of cooling itself under worst case conditions. Conditions to be reckoned with include highest supply voltage, lowest load impedance, maximum ambient temperature and, lowest efficiency output level. In the case of reactive loads, maximum voltage-to-current phase angle (lowest power factor) must also be addressed.

Consider a circuit delivering a peak power of 1KW. A 90% efficient PWM circuit generates 100W of waste heat when running full output and around 50W delivering half power. The theoretically perfect linear circuit will generate 500W of waste heat while delivering 500W. Table 1 shows three possible approaches to this type design. In all three cases it is assumed ambient temperature is 30°C and maximum case temperature is 85°C. It is also assumed power ratings of the TO-3 devices is 125W each. Heatsinks for linear designs require multiple sections mounted such that heat removed from one section does not flow to other sections. The linear approaches require five times the heatsink rating of the PWM approach. The bad news with the hybrid linear design is that the heat is concentrated in such a small area that this design is right on the edge of requiring liquid cooling. With its high package count the discrete linear approach will likely have more than five times the heatsink size and weight of the PWM.

	Discrete Linear	Hybrid Linear	Hybrid PWM
Waste heat	500W	500W	100W
Pkg count	16 x TO-3	2 x PA03	1 x SA01
Heat sink	0.11°C/W	0.11°C/W	0.55°C/W

TABLE 1. CONTRASTING DISCRETE LINEAR, HYBRID LINEAR AND HYBRID PWM 1KW DESIGNS

The simple form of PWM circuit examined thus far is very similar to a number of switching power supply circuits. If the control block is optimized for producing a wide output range rather than a fixed output

level, the power supply becomes an amplifier. Carrying this one step further results in the PWM circuit employing four switches configured as an H-bridge providing bipolar load current from a single supply. This does mandate that both load terminals are driven and zero drive results in 50% of supply voltage on both load terminals. See Figures 3 and 4 for the basic bridge operation and typical waveforms.

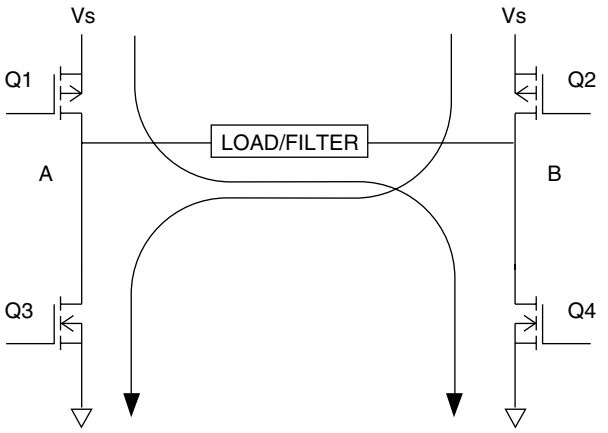

FIGURE 3. BIPOLAR OUTPUT OF THE BRIDGE.

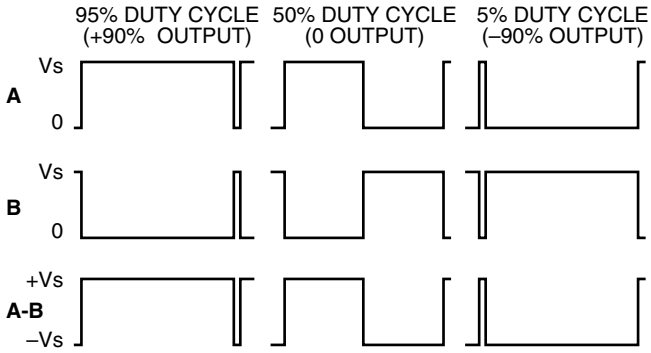

FIGURE 4. H-BRIDGE WAVEFORMS.

The H-bridge switches work in pairs to reverse polarity of the drive even though only one polarity supply is used. Notice how the levels of the A-B waveform are different even though shape is identical to the A waveform. Q1 and Q4 conduct during one portion of each cycle and Q2 and Q3 are on during the remainder of the cycle. Changing duty cycle through 50% (zero output current) is a continuous function meaning there is no inherent cause of crossover distortion as exists in a linear circuit where different transistors conduct depending on current polarity.

Figure 5 shows a block diagram of the SA01. The hybrid construction of the SA01 allows monitoring temperature on the top surface of each power die rather than case or heatsink monitoring, the best that could be achieved with a discrete PWM implementation. This technique includes thermal resistance variables in the measurement and reduces response time orders of magnitude to enhance reliability. The thermal limit is set for approximately 165°C. Activation will cause the PWM controller to immediately turn off all switches in the H-bridge. A latch circuit will keep the SA01 shut down until power is cycled.

The first of two current limits in the PWM block is the high side current limit which activates only upon output shorts to ground (assuming the programmable current has been properly configured.) This circuit has a variable response time based on the current magnitude in +Vs line. With a fault current of 35A it will require several cycles of the switching frequency to activate the circuit. As higher currents are sensed the response time decreases. Once a fault has been sensed the amplifier will remain latched off until power is cycled.

The second current limit circuit in the block diagram is programmable and activates upon a load fault or a short to the power supply. An external resistor senses current flowing between ground and the low side of the H-bridge. The sensed voltage is fed to the SHDN/

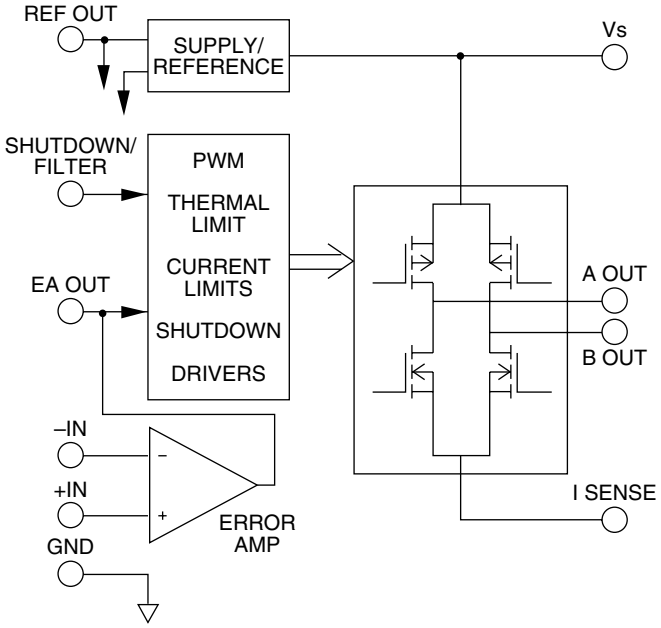

FIGURE 5. SA01 BLOCK DIAGRAM.

FILTER pin. When this voltage exceeds 200mV, all switches in the H-bridge are shut off for the remainder of the switching cycle. Because the sense voltage will have considerable spike content, the hybrid includes an internal filter stage. A second external stage of R-C filtering allows larger peak currents for any given value of current sense resistor. The resistor in this filter is also used as a voltage divider to shut the amplifier down on command of a logic level input voltage.

The supply/reference block provides operating voltages for the PWM controller and the error amplifier plus a reference quality 7.5V which can be used to bias input signals to the error amplifier. This reference voltage is also used to provide accuracy for several functions in the PWM block.

The error amplifier is used to integrate the difference between command signals and feekback signals. Its output voltage will go to the exact voltage required by the PWM block to generate the proper duty cycle corresponding to the desired output. The first job of the error amplifier is responding to input signal changes, but it also compensates other variables inside the feedback loop. Any variation in supply voltage will require an adjustment of duty cycle to maintain a constant output. On resistance of the H-bridge, resistance of the filter inductor and sometimes load resistance temperature variations are compensated. Systems such as speed controls may place mechanical factors such as conveyer belt load weight inside the loop where the error amplifier compensates the variations.

The PWM circuit converts the error amplifier output into a variable duty cycle drive signal which includes 0% and 100%. A dead time (all FETs turned OFF) is inserted between each change of polarity at the output. This precludes “shoot through” current spikes caused by both FETs in the same leg of the H conducting at the same time. If these spikes were allowed to exist they would cause high stress and possibly destruction of both amplifier and power supply components.

Refer to figures 6 & 7 for the following discussion of the PWM control block. The oscillator portion of the PWM controller consists of two comparators, two switched current sources charging the timing capacitor and a flip-flop. When voltage on the timing capacitor reaches 7.5V, the upper comparator resets the flip-flop which opens the upper current source and connects the lower one. When the timing capacitor voltage reaches 2.5V, the lower comparator sets the flip-flop to start the next cycle.

Comparators A and B set up the duty cycle based on the voltage relationship of the input voltage and the very linear triangle. For initial examination of operation imagine the 500Ω resistors are shorted. When the input voltage is midrange, there are equal portions of the triangle wave above and below the input, thus a 50% duty cycle is generated at each comparator. When the input voltage moves half way between midrange and the 7.5V peak of the triangle, 1/4 of the triangle is above the input and 3/4 is below the input generating a 75% duty

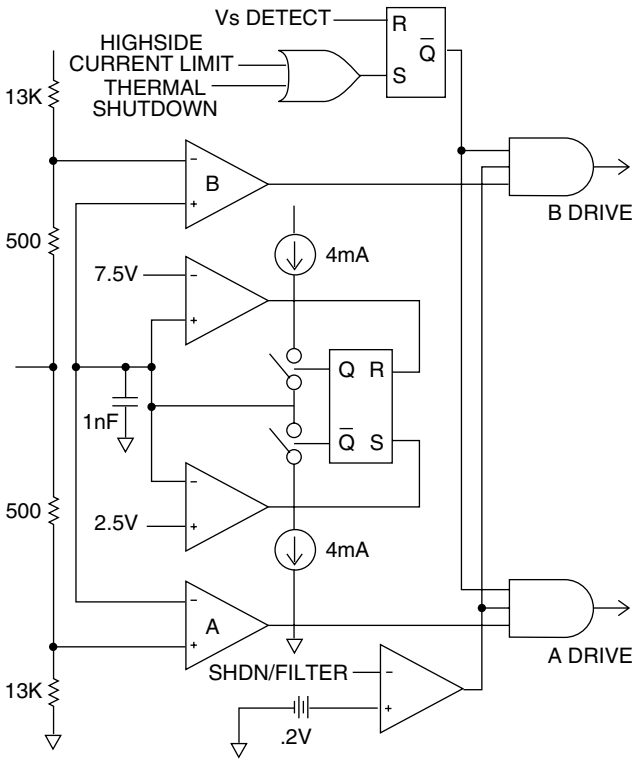

FIGURE 6. PWM CONTROL BLOCK.

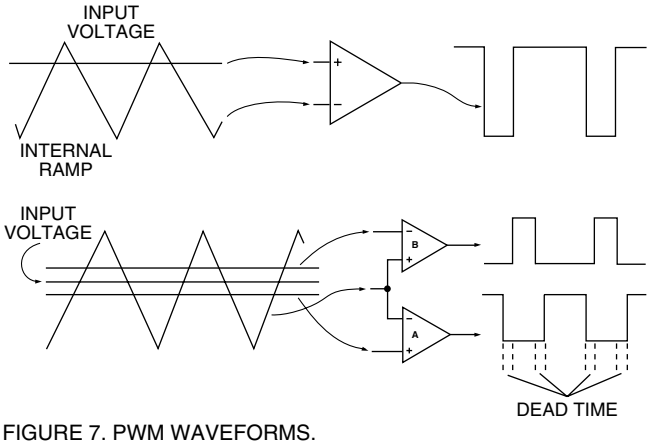

FIGURE 7. PWM WAVEFORMS.

cycle at the A comparator. The B comparator looks at the input and triangle voltages in the opposite polarity, so it generates a 25% duty cycle. Note the circuit is arranged such that a positive going input voltage results in a larger percent on time for the A driver.

With the 500Ω resistors actually in the circuit the input voltage seen directly at the comparators is modified slightly, which modifies the duty cycle proportionally. The A comparator sees a voltage a little more negative than the actual input. The basic function of positive going input creating a longer A duty cycle means this negative offset produces a slightly shorter duty cycle. In the same manner the B duty cycle is also shortened to produce a dead band where all switches are off. Voltage drops across the individual 500Ω resistors change as the input signal varies, but as one drop decreases, the other increases so total dead time is constant.

It is important to note that the input voltage depicted here is a straight line. While the input voltage obviously varies, this reflects the concept that useful bandwidth of the PWM amplifier is significantly less than the switching frequency. If the slew rate of the input voltage were allowed to approach that of the triangle wave, dead time would changed significantly. This can result in shoot through and amplifier shut down.

The output waveform during dead time is primarily a function of load impedance. Current flow is interrupted by the dead time and the load or filter inductance will discharge its flyback energy at this time. While generally not shown in the block diagrams, each power switch has a diode to conduct the flyback current.

The outputs of this block labeled A Drive and B Drive do not directly represent high and low states of the two amplifier output pins. When the A Drive line is high it turns on the switch between the A output and the power supply and also the switch between the B output and ground. When the A Drive is low, both these switches are off. B Drive controls the other two switches in the bridge. The and gates generating both A and B drives can be disabled by either of two lines. The first of these lines represents activation of the thermal shutdown or the high side current limit. The second line is the comparison of the SHDN/FILTER input and a 0.2V reference.

DESIGNING WITH PWMs

PWM amplifiers are high level switching devices whose voltage and current slew rates often surpass those found in either digital or analog circuits. Even though signal bandwidth may not top 1KHz, adopting the viewpoint of an RF designer can be very wise. Here are a few useful things to keep in mind:

Wire inductance ≅ 20nH per inch
Inductor voltage = dI/dt * L
Capacitor current = dV/dt * C
A good square wave = very large harmonic content

POWER SUPPLY BYPASS

It is difficult to over emphasize this aspect of the PWM design. Most of us are familiar with the good design practice of including a supply bypass capacitor at every IC in a low level logic design. If this in not done, the high switching rates cause problems. Inadequate bypass causes ripple and spikes on the supply line which make circuits inoperative and can even destroy components. Careful attention to location, size, ESR and ripple current capacity can result in a good design.

Power supply bypassing is a wideband job requiring at least two components for satisfactory operation of the amplifier. Use at least 10μF per ampere of load current to bypass the lower frequencies. Some applications appear to require many times this amount of capacitance. Capacitors with lower ESR ratings may ease the burden of finding space for such large devices. Locate this capacitor within a few inches of the amplifier. The high frequency bypass is absolutely critical! Think of frequencies in the 1 to 10Mhz range. Remember that many capacitors appear inductive in this range. Use **ceramic** capacitor(s) totaling 1μF to 10μF. Connect these capacitors **directly** between the supply and ground pins of the amplifier. To illustrate the importance of this consider a design having 3" between the supply pin and the ground plane terminated capacitor: The supply pin had spikes equal to the supply voltage! When this happens signal integrity is in question and peak voltages applied to components may be twice expected values. Connect the capacitor right at the amplifier pin and don't forget that both leads of the capacitor must be counted when figuring distance from the pin.

The function of bypass capacitors is to satisfy AC current demands of the amplifier which is isolated from the power supply by the very same line that connects them. The degree of isolation increases with current magnitude, frequency and distance. When this isolation prevents current flow to the power supply, it must come from the bypass capacitors. Attempting to calculate capacitor currents is a questionable investment but ignoring them is no solution. Keep the requirement in mind when selecting components and follow up with temperature measurements on the prototype. Run the system at maximum frequency and power until temperatures stabilize. During this process, keep in mind that under-rated capacitors can explode.

HOW MUCH INDUCTANCE?

PWM amplifiers driving resistive loads with no filtering are unable to modulate the output voltage, they can only switch polarity. Loads with small amounts of inductance may over heat with high ripple current even with a 50/50 duty cycle (zero output) drive. Other types of loads may suffer performance degradation if ripple currents exceed 1% or even 0.1% of their full scale current. Once a design limit on peak-to-peak ripple current has been set, calculate minimum total inductance.

It is proportional to supply voltage and inversely proportional to I_{P-P} and switching frequency:

$$L = Vs/(2*F*I)$$

where Vs is the supply voltage and F is the switching frequency.

As an example, this means the SA01 (switching at 42Khz) on 100V needs 300μH to keep ripple current down to 4Ap-p.

GROUND CONCERNS

Remember all the high frequency currents discussed under the bypass heading? You're right, all that stuff must go through ground to return to the supply. This means a ground plane is the only way to go. It provides good cross sectional area keeping resistance low plus the aspect ratio minimizes both skin effect and inductance. Even with a good ground plane, all local ground connections should be made as close to the PWM ground pin as possible.

IS THE SCOPE TELLING THE TRUTH?

Could be, but touching the probe tip to the ground clip may reveal otherwise. If the scope shows a waveform with this "grounded" input, or all high impedance nodes appear to have spikes which they should not, there are at least three possible sources of error.

The amplifier local ground may be quite different from the local ground seen by the scope input amplifiers and their common mode rejection is less than perfect. First, disconnect all other signal cables from the scope to remove interaction with any other local grounds. If a battery operated scope is available give it a try. If not, install a ground breaker on the scope power cord.

Use only shielded probes and do not use any extenders, grabbers, or clips which do not have nearly complete shielding. Capacitive coupling into high impedance nodes works best when voltage slew rate is high and these switching amplifiers have plenty to get in trouble.

That 3" to 6" ground lead may have to go. It is forming an inductive pickup loop and the PWM is moving lots of high frequency current. If luck holds, the scope accessory kit will yield an RF adapter capable of providing a ground lead less than 1/4" long. If not, consider buying one or making your own from a length of spring wire.

INTERNAL POWER DISSIPATION

PWM amplifiers share most thermal principles with their linear counterparts.

Quiescent current and supply voltage determine standby power.
Additional heat is generated by driving the load.
The heatsink must dissipate both the above.
The case temperature range must not be exceeded.
Load related power elevates power transistor junctions above case temperature.
Maximum junction temperatures must be observed.
Lower temperatures (case and junction) increase reliability.

There are two major differences in the thermal aspects of linear power amplifiers and PWM amplifiers. First, power in the PWM amplifier due to loading can be calculated without knowing the output voltage or the supply voltage. The second difference is more subtle but affects the very reason a PWM amplifier is used: Efficiency drops rapidly as junction temperature increases. This means heatsinking the PWM is more than a reliability issue. Thermal design of the PWM amplifier has a first order affect on circuit performance.

First order calculation of power due to loading involves the output current and the total ON resistance of the amplifier. The high speed waveforms present at the output pins do indicate second order calculations could be made but this document will concentrate only on the basic elements of power dissipation.

Total On resistance includes impedance of the H-bridge power switches plus resistance of the metal interconnects. Consult the amplifier data sheet to find the contribution of each element. If interconnect resistance is not specified, consider it to be insignificant. Consider interconnect resistance to be constant over temperature. Because FET ON resistance is a function of temperature, choose a maximum junction temperature consistent with your design standards (not to exceed the data sheet absolute maximum). Find FET ON resistance(s) at your maximum junction temperature. $I^2 * R$ now yields power due to loading. This is a single calculation on lower current amplifiers using all N-channel FETs, but requires another calculation if P-channel FETs are used and a third if interconnect resistance is broken out separately. Sum the above calculations with standby power to obtain total heat loading on the heatsink. If the amplifier has a separate low voltage supply pin, don't forget to include it in the total power calculation.

With total internal power dissipation now known, it is time to determine the heatsink requirement. Again, consistent with your design standards, choose a maximum case temperature. Do not exceed the product operating temperature range listed on the last line of the specifications table. $R_{\theta CS}$ is the thermal resistance of the package to heatsink interface.

$$R_{\theta SA} \leq \frac{T_C \text{ max} - T_A \text{ max}}{\text{Total Power}} - R_{\theta CS}$$

The last item to check is the junction temperature. Multiply power in a single FET by the thermal resistance of the amplifier and add to the maximum case temperature. In the case of the SA01, use the P-channel power level and realize the N-channel devices will run cooler. An alternative to finding the specific junction temperature is to find the appropriate fraction of total power and then use the power derating graph to make sure junctions do not exceed 150°C.

As an example consider an SA01 delivering up to 10A from a supply of 70V in a maximum ambient of 35°C. Design rules allow case and junction temperatures up to data sheet maximums.

Standby power = 70V * 90mA = 6.3W
N-channel power = $10A^2$ * .145Ω = 14.5W
P-channel power = $10A^2$ * .26Ω = 26W
Interconnect power = $10A^2$ * .05Ω = 5W
Total power = 51.8W
Maximum case rise = 85°C - 35°C = 50°C
Allow .02°C/W for $R_{\theta CS}$
Heatsink maximum rating = 50°C/51.8W - .02°C/W = .95°C/W
Junction temperature = 85°C + 26W * 1°C/W = 111°C

This example would actually run cooler than the above example would seem to indicate because junction tempertures are lower than the assumed starting point and FET ON resistance is lower. An iteration of the above based on an assumed maximum junction of 110°C would yield a heatsink rating of 1.1°C/W and result in maximum junction temperatures of 106°C. This will still have a small safety margin because the N-channel junctions run cooler than the P-channel junctions.

TYPICAL APPLICATIONS

The design steps of the PWM speed control employing a tachometer feedback shown in Figure 8 are as follows: The 7.5V reference output is used to bias the non-inverting input of the error amplifier to the middle of its 2V to 8V common mode voltage range. The gain adjust potentiometer corrects initial inaccuracies stemming from error amplifier voltage offset, tolerance of the 3.83KΩ bias resistor in the inverting input and possibly even for offsets in the input signal. The 470Ω

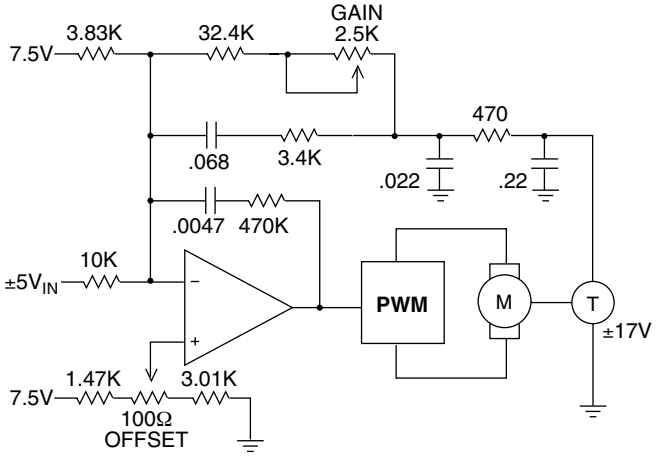

FIGURE 8. PWM SPEED CONTROL.

resistor and the two associated capacitors form a low pass filter to attenuate components of the switching frequency which may be coupled to the tachometer through the motor. The gain adjust potentiometer compensates tachometer variables of accuracy and internal resistance plus tolerances of other resistors in the feed back path. The 10KΩ input resistor sets overall gain to 3.4. The 3.83KΩ resistor was selected to pull the inverting input of the error amplifier up to 5V when both the input voltage and tachometer output voltage are zero. The two R-C networks were selected to provide circuit stability while maximizing system response time. Specific values will depend on both motor parameters and mechanical load characteristics.

While one of the simplest forms of position sensing is shown in Figure 9, options such as optical encoders, LVDT sensors and variable capacitance transducers are also viable. Again, error amplifier inputs are biased to 5V. While 20KΩ input and feedback resistors would have set proper gain and biasing for the inverting input, they would have allowed common mode violations at the error amplifier. This could happen if the system was at one position extreme while a very quick command came in to travel to the opposite extreme. The three 30KΩ resistors prevent common mode problems by increasing impedance from summing junction to the two 10V signal levels at the output and at the input while adding an impedance to ground.

Figure 10 shows a differential input, voltage controlled output circuit resembling the familiar differential op amp configuration. Signal gain is $2*R_F/R_I$. Again, two pull-up resistors are used to bias error amplifier inputs within the common mode range. Select this value to get 5V bias when both inputs are zero and both outputs are 1/2 the supply voltage (50/50 duty cycle.) At zero drive to the load, this differential stage is rejecting 1/2 the supply voltage present on both outputs. This means resistor ratio matching becomes critical. It should also be noted that even though the signal gain is 20, the gain of offset errors is 50 because the effective input resistance is the parallel combination of the signal input resistor and the pull-up resistor.

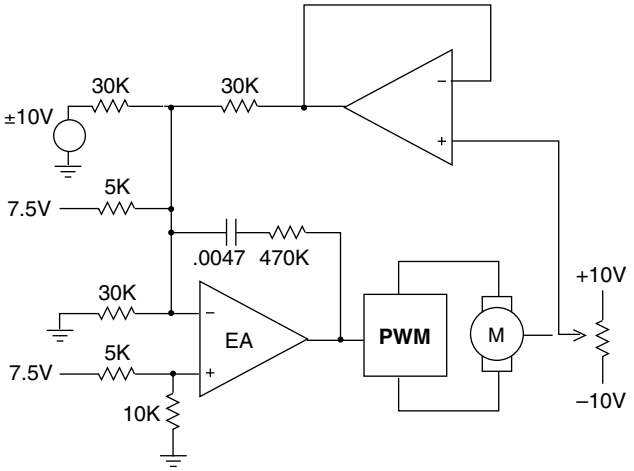

FIGURE 9. PWM POSITION CONTROL.

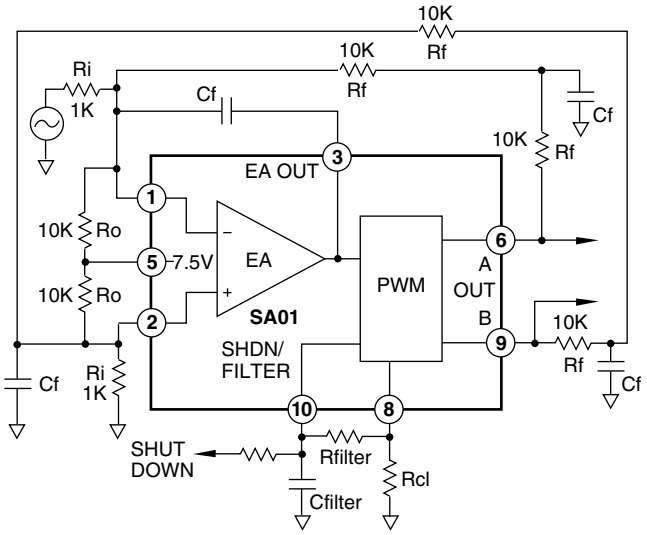

FIGURE 10. VOLTAGE FEEDBACK.

CONCLUSION

The switching amplifier provides solutions to high power drives which could otherwise require in inordinate amount of heat sinking hardware. The arrival of the hybrid PWM speeds the design process and in the case of the SA01 greatly enhances fault tolerance by offering protection circuits simply not possible in a discrete implementation. These features can make an electronic motion control solution feasible where a hydraulic solution may have previously been the only practical alternative.

APPLICATION NOTE 31

POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

HISTORY

The performance and shape of operational amplifiers has changed considerably since the vacuum tube units were produced by George Philbrick, and others, over three decades ago. Discrete transistor-circuit op amps were the main catalog item for companies like Burr-Brown Research Corp. and Analog Devices. The monolithic age of high-production-volume op amps began with the uA709 from Fairchild. Modern op amps have taken on many signal processing challenges. The Apex family has been specialized for high power and high voltage. Whatever the specialty or construction technique, the underlying theory remains the same.

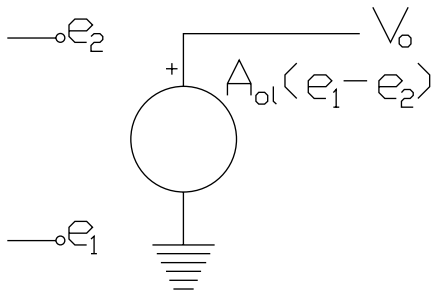

FIGURE 1. ELEMENTARY MODEL OF AN OPERATIONAL AMPLIFIER.

IDEAL MODEL

An ideal operational amplifier (modeled in Figure 1) is a voltage controlled voltage source. The input sense pins have infinite impedance to ground and to each other. The output source has a zero output impedance and the transfer constant (Open-loop Gain, A_{ol}) approaches infinity. This unit, simply placed in a system, would be of little use in a linear mode without the benefits of closed loop control in the form of negative feedback.

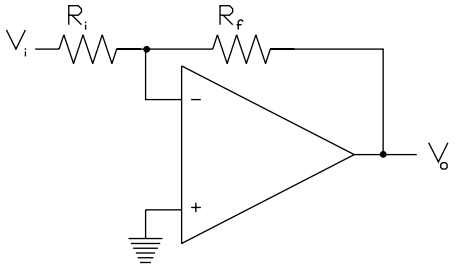

FIGURE 2. BASIC INVERTING CONFIGURATION.

FEEDBACK CONTROL

Consider the circuit in Figure 2. For this first example, the op amp is placed in an inverting configuration with input resistor R_i and feedback resistor R_f. Since the op amp input impedance is infinite, all current flowing through R_i must flow through R_f. If one writes the equations for current flow from V_i to V_o and solves for the V_i to V_o ratio the result is:

$$\frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

Where: A_{ol} approaches infinity.

The operational amplifier has now been converted into a linear circuit element with significant possible extensions.

It is important to notice that the inverting input of the op amp (junction of R_i and R_f) is maintained very near to the potential of the non-inverting input. This point is a "summing junction" and is called a virtual ground. The op amp output is adjusting to maintain this relationship. This fact gives rise to two significant extensions. The input impedance is constant at the value of R_i and it is possible to have multiple inputs which are summed at the output. Each input may have a different gain associated with it as shown in Figure 3.

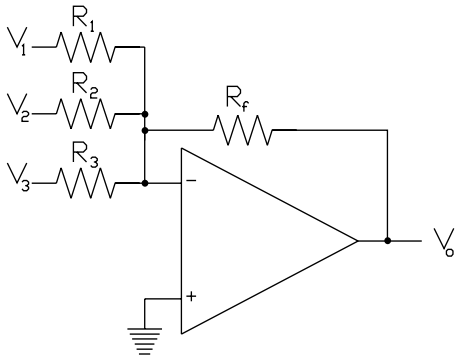

FIGURE 3. SUMMING AMPLIFIER CONNECTION.

The output of this configuration is given by the expression:

$$V_o = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

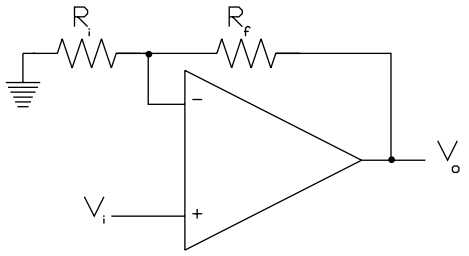

FIGURE 4. NON-INVERTING CONFIGURATION.

Our discussion up to here has ignored the non-inverting input. Write the current summation equations for the circuit in Figure 4 and solve for V_o in terms of V_i as above. With A_{ol} approaching infinity, the following relationship results.

$$V_o = V_i \left(1 + \frac{R_f}{R_i} \right)$$

This circuit has the features that the output signal is not inverted as it is amplified, the input impedance approaches infinity, and the gain can not be less than unity.

By combining the inverting and non-inverting circuits it is possible to make a full, weighted sum and difference system element as shown in Figure 5.

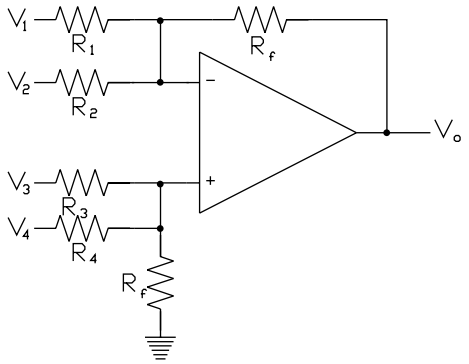

FIGURE 5. SUM AND DIFFERENCE AMPLIFIER.

Through the use of super-position the sum and difference amplifier can be analyzed. The accuracy of this relationship depends on the matching accuracy of the two resistors labeled R_f. The complete transfer function is given by:

$$V_o = R_f \left(-\frac{V_1}{R_1} - \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_4}{R_4} \right)$$

NON-IDEAL OP AMPS

All of the discussion to this point has assumed an ideal device. With real world op amps there are deviations from the ideal, or errors. The magnitude of some of the possible errors for an op amp are listed in the specification sheet for that device. A description of the circuits used to measure these parameters can be found in the section titled "Parameter Definitions & Test Methods".

When the magnitude of the error, as seen at the output, is a direct function of the closed loop gain that error magnitude is specified referred to the input (RTI). The maximum error to be expected at the output is the error value times the non-inverting gain of the amplifier. The most common of these errors is initial voltage offset.

Recall that the op amp works because the negative feedback brings the inverting input to equal the non-inverting input. When connected as a non-inverting amplifier both inputs will be at a potential equal to the input signal. Since this input is common to both inputs it is called the "Common Mode Voltage". In an ideal amplifier the common mode signal would be subtracted out and not appear at the output. Due to limitations imposed by the real world circuits there is an error signal at the output which is a function of the common mode voltage. A limit exists on the range of the common mode voltage that the op amp can withstand.

POWER SUPPLY SYMMETRY

To this point we have not considered the power supply configuration. When op amps are furnished symmetric power supplies common mode voltage limits are easy to meet. It is generally possible to operate from a single supply if the common mode voltage limits are honored. For further extensions on single supply operation Application Note 21 should be studied.

AC CONSIDERATIONS

All of the relationships discussed above can be extended to the AC domain by replacing resistance with impedance and allowing for the finite frequency response of the op amp. If a plot is made of open loop gain vs frequency it would look similar to Figure 6. This graphic display is used to describe the op amp's open loop performance as a function of frequency and to predict stability.

The two change of slope points in the response curve are caused by the existence of poles in the transfer function of the op amp. Most op amps have Bode plots very similar to that shown in Figure 6. The slope of the trace between 10 Hz and 1 MHz is -20 dB per frequency decade. Extensive discussions of stability are presented in Application Note 19 and others. In the opening discussion we assumed the op amp gain to approach infinity. The difference between the open loop gain of the op amp and the closed loop gain, set by the feed-back network, is referred to as excess loop gain. As the excess loop gain decreases

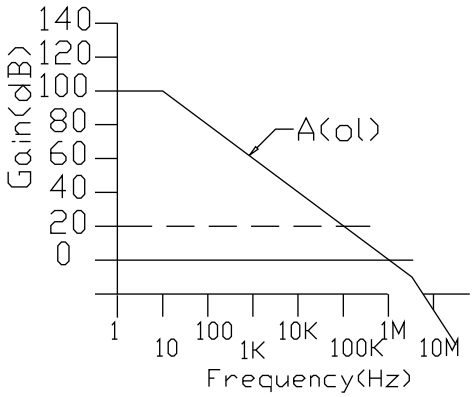

FIGURE 6. TYPICAL BODE PLOT.

the op amp circuit deviates more from the ideal. Consider the op amp of Figure 6 if it were used in a closed loop gain configuration of 20 dB (X10) as shown by the dashed line. At low frequencies the excess loop gain is 80 dB. As the frequency is increased the excess loop gain decreases until it reaches zero dB at 100 KHz. The performance of the circuit would be very near ideal at low frequencies and deviate more from ideal as the frequency approached 100 KHz. If the closed loop gain was increased to 40dB(X100). The non-ideal response would become apparent one frequency decade earlier.

CONCLUSION

Some of the basic features of operational amplifier circuits have been discussed here. The concept of negative feedback and the graphical representation of the Bode plot are the most common tools used in op amp circuit design. The application notes that follow present techniques for solving many of the problems which arise in the use of op amps.

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APPLICATION NOTE 32

1.0 INTRODUCTION

Pulse width modulation (PWM) amplifiers require low pass filtering of the output to demodulate the PWM carrier. Some applications also utilize the filter as a way to achieve an impedance transformation which draws less power supply current than is delivered to the load. These filters can be as simple as a single inductor, to multiple LC nodes depending on the application. In some applications the load will have enough inductance to act as its own filter. Deciding on the type and size of a filter can be time consuming since the calculations can be tedious and often give component values that are not easily obtainable. This application note is an effort to reduce filter calculation time. Using the Apex Power Design tool, available at www.apexmicrotech.com. will further reduce time. Power Design.exe is a self-extracting Excel97 spreadsheet and will be used extensively in this application note.

2.0 FILTER TYPES

PWM filters are normally a low pass configuration. These exhibit low attenuation to the frequency spectrum from 0 Hertz to the frequency of cutoff (F_C). This low attenuation region is called the pass band. Beyond the F_C, attenuation increases at a rate determined by the filter type and the number of poles (order). Figure 1 indicates the general response of the low pass filter.

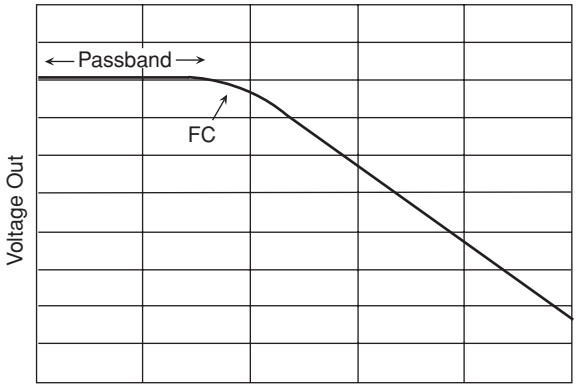

FIGURE 1. LOW PASS FILTER RESPONSE

Many different types of low pass filters exist. Each has favorable and unfavorable traits and the selection usually is a compromise of performance in one area to achieve desired performance in another area. Some characterizations are: pass band flatness, rate of attenuation, and phase shift versus frequency. Common filters include Butterworth, Chebyshev, and Bessel.

The Butterworth filter has a flat response in the pass band and good roll off beyond the cutoff frequency. Component variations do not greatly affect the performance. It is considered a good general filter that is often used and therefore will only be considered here.

3.0 INITIAL CONSIDERATIONS

If you are unfamiliar with Apex PWM amplifiers or with locked anti-phase modulation, please refer to Application Note 30. This should convince you that using unfiltered PWM outputs is useless for some loads (applies only full supply voltage) and can often be destructive to the load or the amplifier. Filter design requires trading off many variables. Here are some things to consider:

1. This filter design technique assumes amplifier output impedance is low compared to the load impedance and that the combined impedance of the load plus matching network is constant over frequency. The demand for circuit efficiency will insure the impedance relationship requirement is met. Beware that changing load element values, without corresponding matching network value changes, will alter the filter response curve. With some loads, such as solenoids or valves that tend to change inductance with position, the textbook response curve is nearly impossible to achieve. In these cases, try designing for the highest impedance, and then check performance driving the lower impedance.
2. As shown in Figure 2, a full bridge PWM amplifier driving a first order (single pole) filter with F_C set at 1/10, the switching frequency will be required to deliver approximately 15% of the peak output current as peak ripple current. The ripple is at the switching frequency; measured when the modulation level is 50%; and assumes peak output current equals Vs/R_L. Figure 2 also indicates that changing to a second or higher order filter will drop this to almost 10%. A second and even more effective way to reduce this ripple current is to widen the ratio between signal and switching frequencies. As switching frequencies of Apex PWM amplifiers range from 22.5KHz to 500KHz, this technique has obvious limits

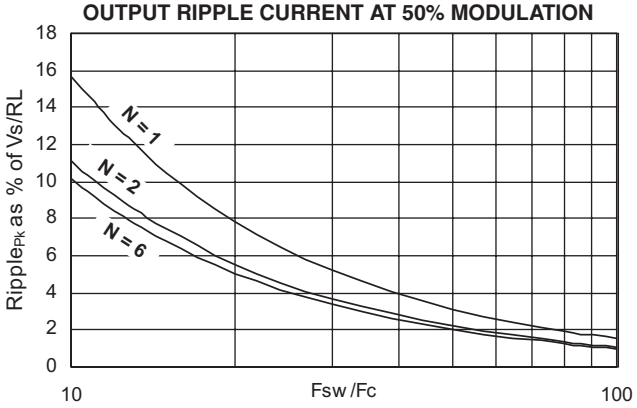

FIGURE 2. OUTPUT RIPPLE CURRENT VARIES WITH ORDER AND RATIO OF SWITCHING TO SIGNAL FREQUENCY

2.1 This ripple current flows through the first inductor of the filter, meaning high frequency core loss is of concern. With first order filters driving resistive loads, it also flows through the load. With higher order filters, most of the ripple current flows in the first filter capacitor, affecting the ripple capacity rating of these components.

2.2 In applications where full modulation is expected (output current is expected to approach V_S/R_L), the workload imposed on the amplifier by delivering the ripple current is of minor concern. While 15% (or less as shown in Figure 2) of maximum output may seem more than minor, Figure 3 shows this ripple current decreases as modulation percentage moves away from 50% (a graph of zero to 50% would produce a mirror image curve). In other words, heatsink size is not increased 15% because maximum DC output and maximum ripple output never occur at the same time. The heatsink will be sized to handle the much larger output current. The ripple current curve of Figure 3 is also valid for half bridge circuits, but the Vout curve would need to be re-scaled from 0.5 at 50% modulation to 1 at 100%.

2.3 For applications spending a major portion of the time near the 50% modulation level, the ripple current will be quite noticeable in terms of lowered efficiency (power supply

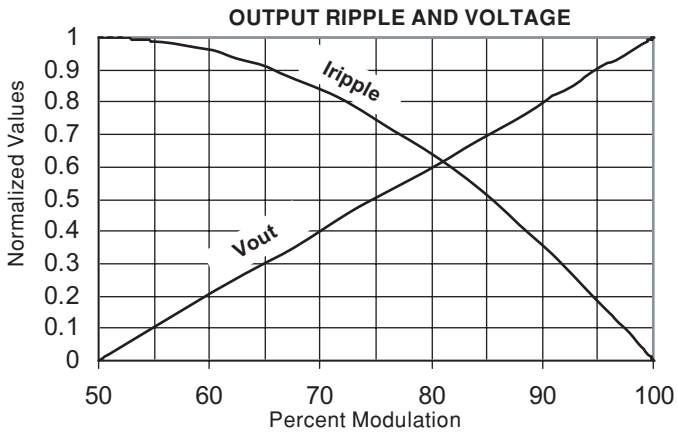

FIGURE 3. RIPPLE CURRENT AND OUTPUT VOLTAGE IN THE FULL BRIDGE

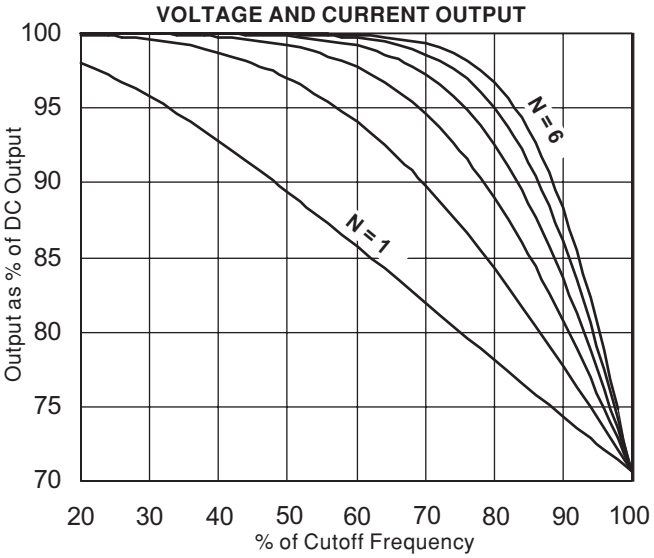

FIGURE 4. REDUCED V & I AS FSIGNAL APPROACHES Fc

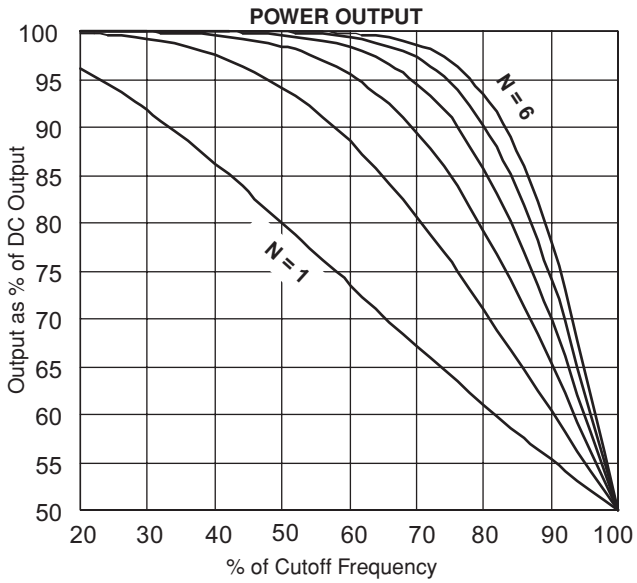

FIGURE 5. REDUCED POWER AS FSIGNAL APPROACHES FC

loading and heatsink temperature). These circuits include full bridges spending most of their time delivering small signals compared to peak output capability; full bridges whose peak output voltage is considerably less than supply voltage; and half bridges spending most of their time delivering half the supply voltage.

3. Filter attenuation at 100% of cutoff frequency is 3db, that is, a factor of 0.707 for voltage output (and consequentially, current) and 0.5 for power output. Refer to Figures 4 and 5 for more data on attenuation as signal frequency approaches cutoff frequency. Designing the cutoff frequency at least twice the actual maximum signal frequency is a very common technique to obtain a flatter response in the portion of the pass band actually used.
4. With supply voltage and desired maximum ripple voltage at the load held constant, a larger ratio between signal frequency and switching frequency will lower the number of filter poles required. This will lower cost, weight and size. For example, starting with a 10:1 ratio requiring a 4 pole filter; changing to 21.4:1 brings N down to 3; and changing to 100:1 yields N=2.
5. In the design of servo loops or any other application where feedback is taken at the filter output or beyond, phase shift of the filter is critical to stability of the overall loop. With properly terminated filters, phase shift at the cutoff frequency will be 45° per pole and the shift will decrease in a linear fashion at lower frequencies. Power Design will calculate voltage and current phase shift at the load for all cases, but first and second order filters are likely to be the maximum acceptable. In fact, many designs use no dedicated filter components, but instead rely on load inductance and resistance to form a first order filter. The important point to check is how this inductance reacts to square waves of the switching frequency.
6. When using second and higher order filters, impedance presented to the PWM amplifier will dip below the load impedance as signal frequency approaches F_C. Figure 6 shows this in reciprocal form. Putting some numbers to go with the worst point: N=6, F_C=1KHz, F_{SIGNAL}=900Hz, I_{LOAD}=10A, amplifier output=12.3A. This "extra" current flows in the output devices of the PWM amplifier increasing internal power, increasing ON resistance, increasing junction temperatures and reducing efficiency. This effect should be considered also with regard to amplifier and power supply current ratings and design of current limit circuits. We will see what looks almost like a duplicate of this graph when discussing filter component stress levels.

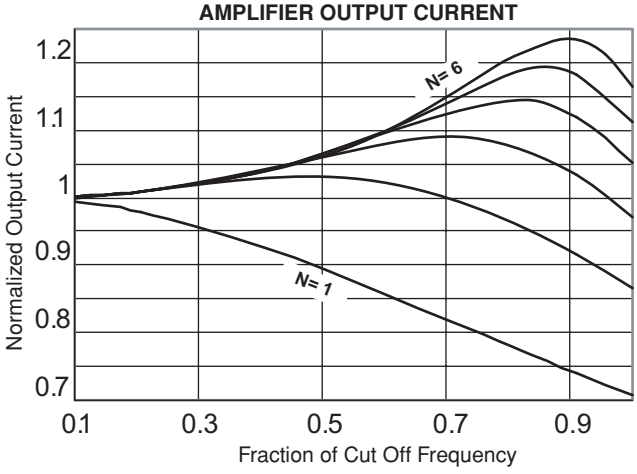

FIGURE 6. AMPLIFIER OUTPUT CURRENT CAN BE MORE THAN EXPECTED

Figure 7 shows efficiency data for a perfect component filter (no parasitics) designed for an SA03 running maximum output voltage into a 10Ω load while mounted on a 0.1°C/W heatsink. At 10% of F_C, about 3.3% is lost in the amplifier and the filter is having very little affect on efficiency. As signal frequency increases, three effects combine to bring high frequency efficiency down further. First,

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quiescent power remains constant even though the output signal is rolled off. Secondly, the peaking output current demanded by second and higher order filters increases internal PWM losses. The last item is the positive non-linear temperature coefficient of the ON resistance of the PWM, which increased about 1% in this example. The point here is that filter choices can double efficiency loss even before allowing for filter component loss. Importance of this data varies with the spectral content of the signal being amplified. Consider an audio application versus a fixed 400Hz inverter application.

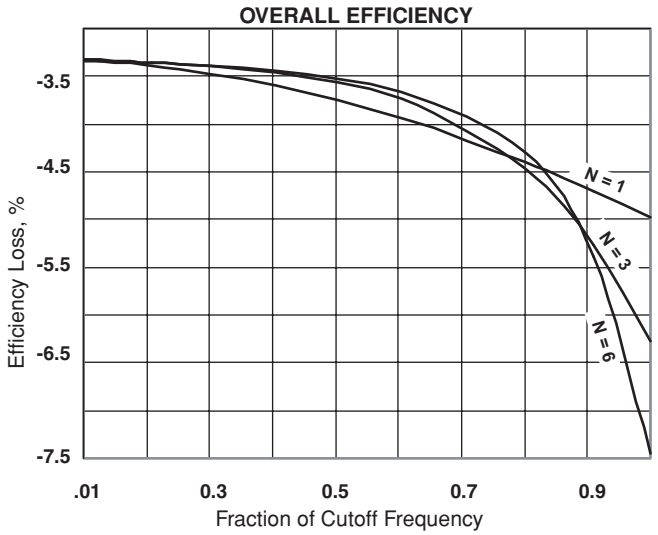

FIGURE 7. EVEN A THEORETICAL FILTER CAUSES REAL POWER LOSS

Desired attenuation of the PWM square wave output must be known to establish the order of the filter. While standard filter equations assume sine wave inputs, the PWM applies square waves at the switching frequency. Artificially increasing the bridge supply voltage by 25% approximates a correction factor for this. A non-integer value of this requirement is given in the following equation:

$$N = \frac{\frac{A}{10}}{2 * LOG\left[\frac{F_X}{F_C}\right]}$$

Where:

A (in db) = 20 log (bridge supply voltage * 1.25/load peak ripple voltage)

F_X = frequency of the desired attenuation (usually the switching frequency)

F_C = filter cutoff frequency

N is rounded up to the next integer

Note that ripple voltage on the load is a differential specification. With a full bridge circuit, it is not the voltage seen at either load terminal with respect to ground.

4.0 FILTER TABLES

Filter analysis begins by developing general mathematical equations to describe the filters. Each filter equation can be reduced to a set of coefficients.

Filter coefficient tables are usually in a normalized form. Normalized coefficients are calculated at a frequency of 1 radian per second and an impedance of 1 ohm. This is done for convenience so the designer does not have to calculate coefficients for every case. The normalized coefficients require the designer only to scale the frequencies and impedances to fit the particular requirement.

The filters most designers are familiar with are the symmetrical load type. These assume equal terminations on both ends of the filter. These configurations will generally not work here because the output impedance of the amplifier bridge is usually low and the actual load usually will be much higher. Apex PWM amplifiers have room temperature output impedances from less than 0.1 ohm to about 1 ohm and are mostly resistive. The filter tables here assume a very low source impedance and a higher impedance load.

The coefficient table also assumes zero loss components; therefore, real components will compromise results.

Filter orders up to 6 are given which is more than what is usually needed. Beyond order 5 or 6, the point of diminishing returns begins as losses in the filter components, parasitics of the physical layout, and undesired coupling eat up all the theoretical advantages of additional poles.

The single-ended filter configuration is shown in Figure 8. A first order filter would use only L1, a second order adds C1, a third order adds L2, and so on. The coefficients of Table 1 are used directly to find values for these filters. This configuration must be used with half bridge circuits and can be used with full bridge circuits by substituting the second PWM output for all the ground connections. This substitution is very rarely done because it places the high speed square waves of the PWM output on both load terminals and all the cabling between the amplifier and load. With rise and fall times usually in the tens of nanoseconds, and amplitude nearly equal to supply voltage, this is an extreme RFI problem

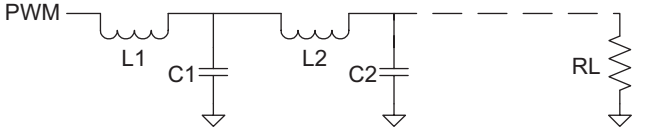

FIGURE 8. FOURTH ORDER, SINGLE-ENDED FILTER CONFIGURATION

ORDER	L1	C1	L2	C2	L3	C3
1	1					
2	1.4142	.7071				
3	1.5	1.3333	.5			
4	1.5307	1.5772	1.0824	.3827		
5	1.5451	1.6944	1.382	.8944	.309	
6	1.5529	1.7593	1.5529	1.2016	.7579	.2588

$$L = \frac{COEF * R_L}{2 * \pi * F} \qquad C = \frac{COEF}{2 * \pi * F * R_L}$$

L in Henries
C in Farads
R_L in Ohms

TABLE 1. FILTER COEFFICIENTS

5.0 FULL BRIDGE FILTER TOPOLOGIES

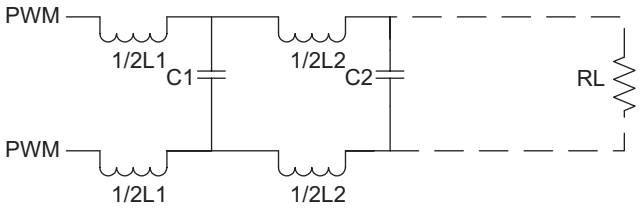

FIGURE 9. BASIC SPLIT INDUCTOR TOPOLOGY FOR THE FULL BRIDGE

With full bridge circuits, an additional filter requirement is introduced in that common mode voltage applied to both load terminals usually needs to be minimized. The technique to achieve low common mode voltage is to simply split the inductor values in half, applying half to each PWM output as shown in Figure 9.

If one could acquire a perfect PWM amplifier (equal rise and fall times, no dead time plus an exact out of phase condition), this filter would output common mode voltage proportional to inductor mismatch only. With real PWM amplifiers, the output will contain large amounts of high frequency harmonics. Each application is different, but peak-to-peak noise amplitude may approach the supply voltage. The spectral content of this noise extends well above the switching frequency. A pair of small capacitors added from the output side of each half of L1 to ground, as shown in Figure 10, will remedy this

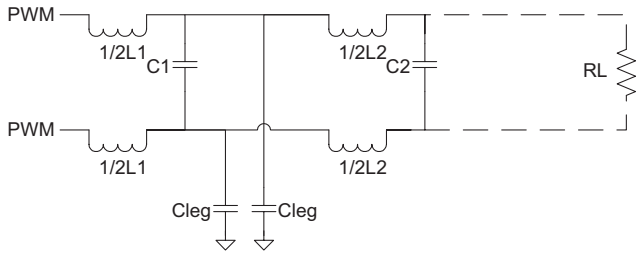

FIGURE 10. GROUND LEG CAPACITORS FILTER HIGH FREQUENCY COMMON MODE NOISE

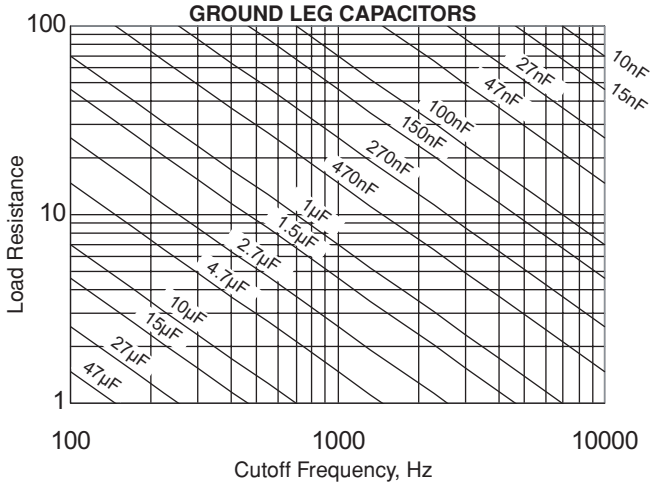

FIGURE 11. GROUND LEG CAPACITORS FOR COMMON MODE FILTERING

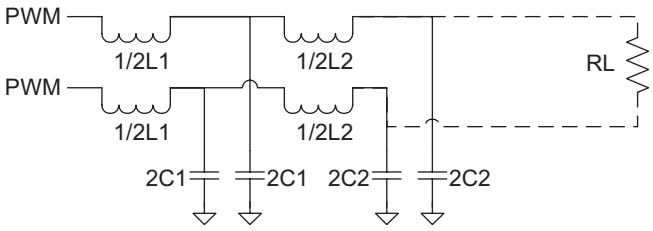

FIGURE 12. DUAL CAPACITOR TOPOLOGY MAY ALLOW UNIPOLAR CAPACITORS

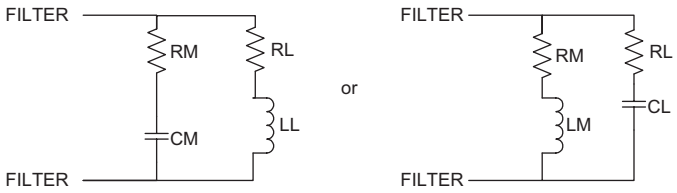

FIGURE 13. CONJUGATE MATCHING NETWORKS

problem. It is not necessary (and sometimes it is counterproductive) to use more than this one pair of leg capacitors. Placing these small capacitors on the load side of L2 or L3 is not as effective as the placement shown.

Value selection for these ground leg capacitors is less critical than for the main filter capacitors. It has been determined empirically that setting the impedance value of these capacitors at the cutoff frequency, to between 10 to 30 times the value of the load resistance will provide reasonable common mode filtering. The addition of these capacitors will typically produce no more than 0.05db peaking, nor more than 0.2db change at the cutoff frequency in any order filter. From the technical point of view, the two Clegs are in series, and this is in parallel with C1. This means that on all but first order filters, C1 could be reduced by half the value of Cleg to eliminate even these small errors. Figure 11 shows the results of the following equation where the impedance ratio was set to 23:1:

$$C = \frac{1}{145 * FC * RL}$$

From a practical point of view, the lower left quadrant of this graph is textbook material only when using second and higher order filters. C1, C2, and C3 must be capable of bipolar operation and will be an order of magnitude or more larger than the leg capacitors. While the bipolar capacitors exhibit very low ESL and ESR to provide good roll off in the high frequency spectrum, this leads to very large and expensive banks of capacitors.

We previously noted that the two ground leg capacitors form an equivalent capacitor one half the value of the two individual devices. Carrying this thought a little further, we arrive at the common topology shown in Figure 12 where only unipolar capacitors are used, and where very good common mode filtering is inherent.

Do not assume this dual capacitor topology is a panacea for all high current, low frequency filters. The total amount of capacitance increases fourfold over the single capacitor topology. Additionally, the high frequency performance of these large unipolar capacitors tends to fall off more rapidly than bipolar varieties (ESL and ESR rise faster). As the two capacitors are in series, the equivalent ESL and ESR are TWICE the individual values rather than half. If maximum high frequency attenuation is required, large high quality bipolar capacitors are a must.

The dual capacitor topology using unipolar capacitors always works with second order filters and may work with higher order filters. Be sure to read section 6.0 FILTER COMPONENTS, where we will find it is very common for higher order filters to apply negative voltage to these capacitors.

6.0 REACTIVE LOADS

One more time: to achieve these filter responses a constant and purely resistive load termination is required. If a reactive load can be modeled as resistance in series with either capacitance or inductance, a simple conjugate match network can be used as shown in Figure 13. The resistor in the network will equal the resistor of the load model. As the network is in parallel with the load, all signals in the pass band will be applied to the network and power dissipation must be checked. Realize that combined impedance of the network plus load is constant and that changing frequency shifts the power between the network and the load. This means a 100W capacitive load drive will require a 100W matching network if DC signals are allowed.

The Power Design frequency sweep capability will prove quite useful in determining power dissipation and in possibly choosing a non-perfect network trading off lower power dissipation for some distortion of the ideal filter response curve. Figure 14 illustrates one response example where the ideal match network resistor was doubled to reduce power dissipation. It is perfectly acceptable to omit the network as long as the resulting attenuation curve is also acceptable.

7.0 FILTER COMPONENTS

Filters used in high power switching circuits often are the largest physical part of the circuit. Expect the filter to occupy more space than the rest of the circuitry. Expect currents and voltages to be greater than the output signal.

Filter components should be low loss, high current, high frequency devices. Check current ratings carefully as different manufacturers can use different rating methods. Make sure the inductors chosen

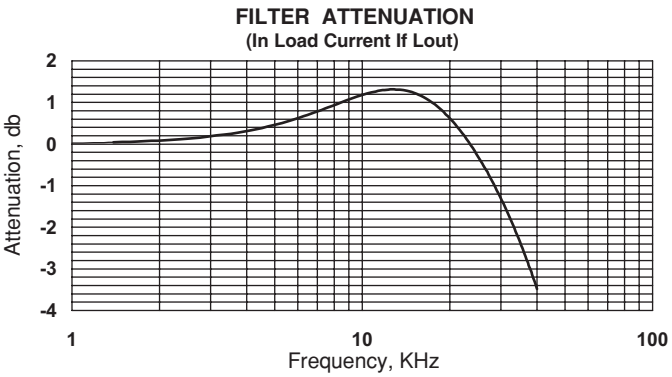

FIGURE 14. TRADING MATCH NETWORK POWER FOR SOME PEAKING OF THE FILTER

have the required inductance at the maximum rated current and at the square wave switching frequency (many inductors are rated only with sine waves applied). We have seen laminated steel core inductors destroy circuits even when cutoff frequency was only 100 Hz! Successful applications usually implement powdered iron, ferrite, or air cores.

Polyester, polycarbonate, polypropylene, and chip ceramic capacitors are often used in the best PWM filters. Tantalum (preferred if voltages and temperatures allow) or electrolytic capacitors may be required in low frequency filters. The capacitors should have low loss at the switching frequency and well beyond (to at least the tenth harmonic).

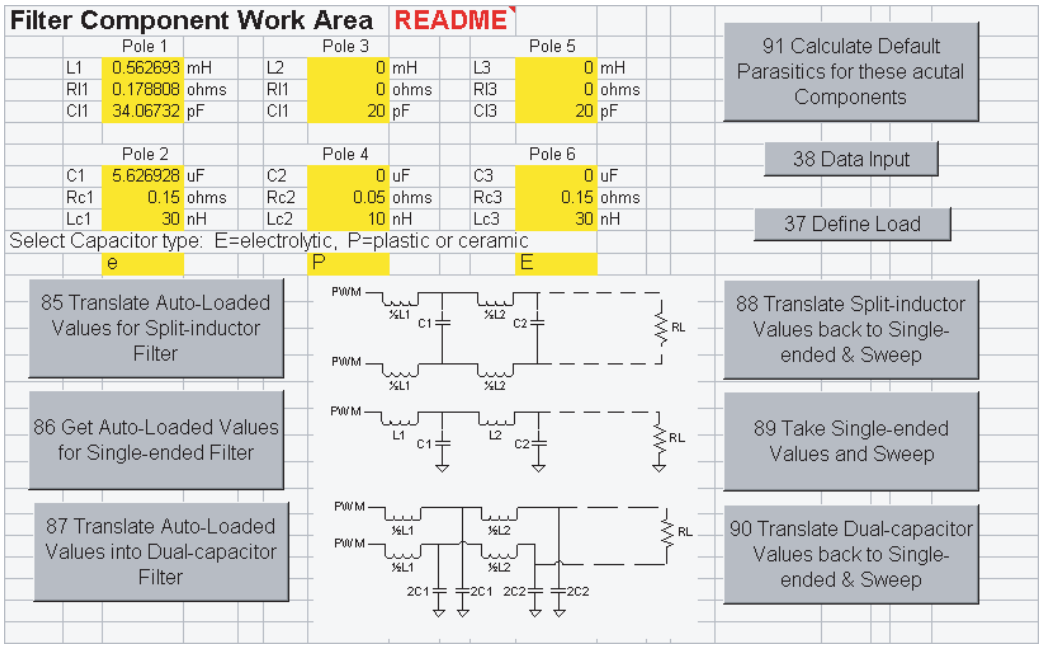

FIGURE 15. TRANSLATING VALUES FOR THE THREE TOPOLOGIES AND DEFAULT PARASITIC CALCULATION

While there is absolutely no substitute for finding real parasitic values for filter components, Power Design provides a default parasitic calculator for first pass design efforts, as shown in Figure 15. Parasitics vary WILDLY form part to part. The default calculator is ONLY intended to get somewhere in the pall park. These defaults are reasonable for parts suitable for switching applications. Your real parts could be better, but could easily be much worse.

Consult manufacture's data sheets or measure the parts to get accurate data.

Components loaded into this sheet by the PWM Filters sheet are for single-ended filters (to minimize spreadsheet size and sweep execution time). Use buttons 85-87 to put physical component values here for the type of filter you intend to build. Values to design single-ended filters will not be changed. For split-inductor designs, L will be divided by 2. For dual-capacitor designs, L will be divided by 2, plus C will be doubled.

Enter actual parasitics or calculate default values with button 91.

Use buttons 88-90 to re-load into the filter/load area and run the sweep. Values for Single-ended designs are not changed. For split-inductor designs, L and the parasitic R will be doubled plus parasitic C will be divided by 2. For dual-capacitor designs, inductors will be treated the same as for split-inductor designs and C will divided by 2, plus parasitic R & L will be doubled. Please note that even when using similar quality capacitors, the Q of a dual capacitor equivalent of a single capacitor is likely to be four times lower.

The folly of ignoring parasitics is illustrated by the data in Table 2. A second order filter was designed to provide 100.9db attenuation at the switching frequency. Using default parasitics, attenuation is listed for the three filter topologies using electrolytic and plastic capacitors.

TOPOLOGY	ELECTROLYTIC	PLASTIC
Split-inductor	68.1db	81.8db
Single-ended	68.6db	82.4db
Dual-capacitor	62.4db	75.3db

TABLE 2. COMPARING FILTER TOPOLOGY AND CAPACITOR TYPES.

There are two conclusions to draw from this data: first, plastic capacitors have a definite advantage over electrolytic types. Secondly, the dual-capacitor topology is inferior to the other two. In a related issue, do not fall into the trap of thinking that adding a small high frequency capacitor in parallel with a much larger one having poor ESR and ESL will regain the ideal attenuation. Adding a plastic or ceramic capacitor equal to 1/10 the value of the large electrolytic brings attenuation up to only 81.1db for the split-inductor topology, still almost 20db short of ideal.

7.1 FILTER COMPONENT STRESS LEVELS

Multi-pole filters are a combination of one or more series resonant circuits and they do develop currents and voltages above the input and output levels as the signal frequency approaches the cutoff frequency. The highest stress levels will be born by L1 and C1. Higher order filters produce higher amplification levels. The last two components of the filter do not see stress levels above the signal level. Figure 16 illustrates these stress levels for L1, L2, C1, and C2 for all filter orders up to 6. Voltages and currents are normalized to the DC or very low frequency output signal amplitude and are based on ideal components.

Data on current can be used directly for any filter topology for both inductors and capacitors. If a split inductor topology is used, the inductor voltage data must be divided by two. Voltage data can be used directly for capacitors not connected to ground. Ground terminated capacitors have a DC bias equal to 1/2 the supply voltage which must be added to half the peak voltage calculated from the graphs. To find peak capacitor voltages the equation is:

$V_{PEAK} = Vs/2 + Vout_{PEAK}/2 * \text{graph reading}$

Do this calculation for BOTH the positive and negative peak output voltages. Note that if output voltage is nearly equal to supply voltage, and the filter order is three or more, the most negative going peak for C1 will be negative with respect to ground. The same is true for C2 with fifth and sixth order filters. This means even a ground-terminated capacitor can have BIPOLAR voltages applied. From a practical point of view, this situation implies the use of unipolar capacitors limits filter order to two.

As an example, consider filter options for an SA06, which is to deliver ±470V to a 332Ω resistive load at 1KHz. Current will be 1.414A peak or 1A RMS. Power will be 665W peak or 332Wrms. A supply of 480V will provide plenty of headroom for internal losses and maximum linear duty cycle limitations. The worst case for voltage and current extremes will be a sixth order filter.

L1 peak current = 1.414A * ~1.23 = 1.75A
L1 peak voltage = 470V * ~1.82 = 850V
C1 RMS ripple current = 1A * ~1.82 = 1.82A
C1 peak voltage (differential) = 470V * ~1.17 = 548V
C1 + peak voltage (grounded) = 240V + 274V = 514V
C1- peak voltage (grounded) = 240V - 274V = -34V Must be bipolar

The same math with graph values from the other four graphs will yield stress levels for L2 and C2.

We can now make some general statements about filter design. Higher order filters can increase component ratings by as much as 82%. The two most costly increases are first, the ripple current on C1 and then the voltage rating of L1. While lowering filter order helps this situation, an even better way to minimize component requirements is to design the cutoff frequency as a multiple of the maximum input signal frequency. Turning this around, limiting input signal to one half or less of the cutoff frequency, limits these stress level increases to about 6% for sixth order filters and even less for more moderate (and practical) orders. Figures 17 and 18 show the Power Design answers for L1 and C1 stress levels of this example modified for a cutoff frequency of 2KHz rather than 1KHz. An additional benefit of this change is a 2:1 reduction in the values of filter components. The performance cost of this change at the switching frequency is a reduction of attenuation equal to 6db for each order (@ N=4, -108db drops to -84db).

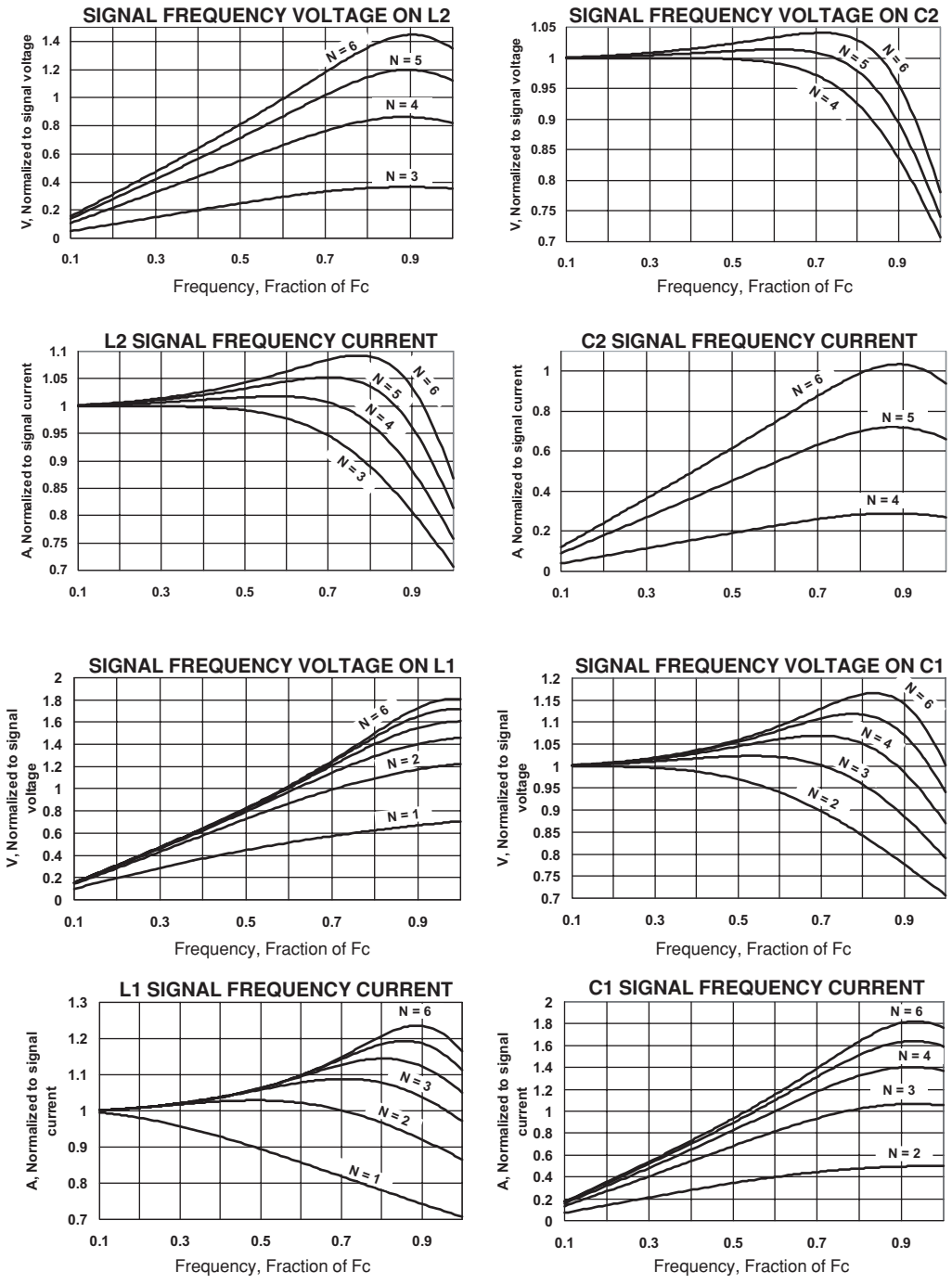

FIGURE 16. FILTER COMPONENT STRESS LEVELS

8.0 SAFETY CONCERNS

A word of CAUTION. These graphs were generated with perfect components giving the best possible circuit Q, compared to real components having losses and therefore generating lower peaks. On the opposite side, these graphs reflect perfectly terminated filters; and normal component tolerances destroy this perfection. Do NOT power up filters unless your are sure they are properly terminated. Use Power Design to **CHECK COMPONENT TOLERANCES.**

These graphs also assume sine wave inputs (the only waveform Power Design deals with). Figure 19 is a Spice simulation of this original example showing L1 and C1 stresses when the input signal is a 900Hz, 470V square wave. L1 voltage = ±582V and is for 1/2 the total inductance. L1 current peaks at ±2.14A. C1 current peaks at ±3.18A. C1 is grounded and has voltage peaks of 587V and -107V. The output is a very good looking sine wave instead of a square, and peak amplitudes have risen from 470V to 527V, from 1.414A to 1.59A and from 665W to 838W.

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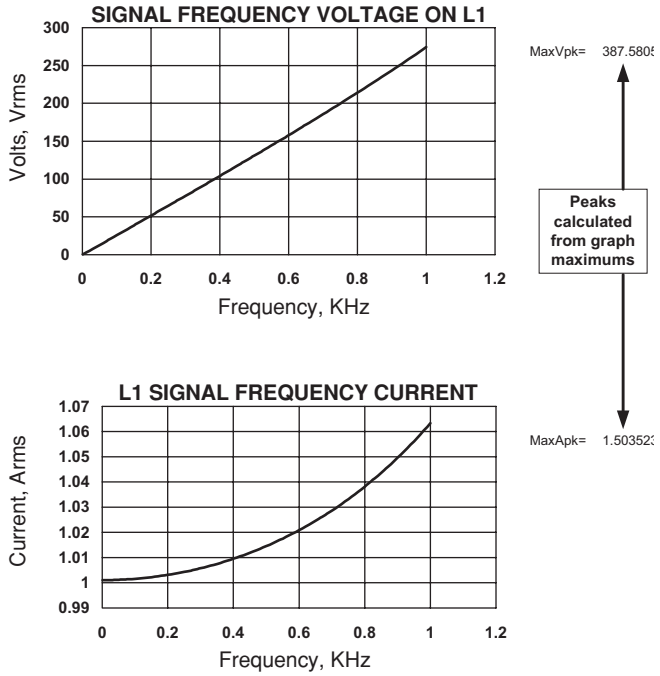

FIGURE 17. DOUBLING Fc LOWERS L1 STRESS LEVELS

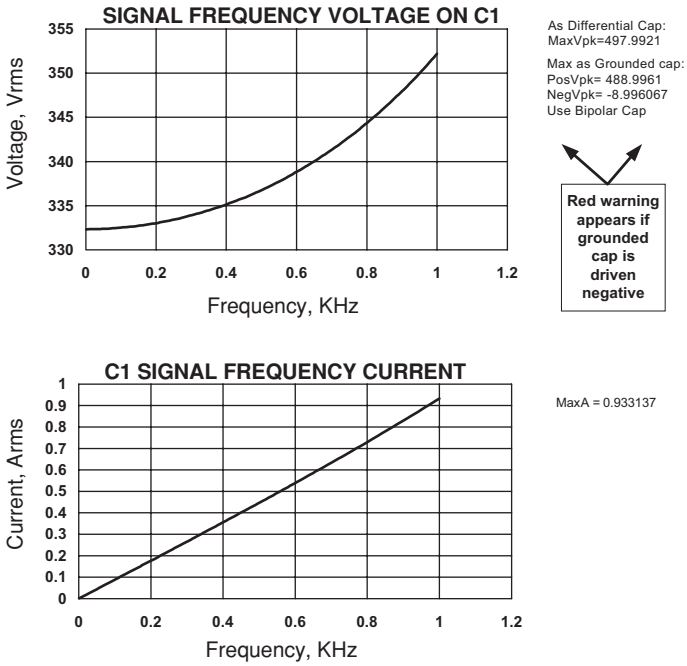

FIGURE 18. DOUBLING Fc LOWERS C1 STRESS LEVELS

9.0 EXAMPLES

Example 1 The voice coil of a shaker table has 7Ω resistance and 100uH inductance. The desired drive level is 50V peak from 10Hz to 2KHz. Starting with the Power Design, Part Selection sheet, SA60, PA93, PA04, and SA01 are the first choices in order of cost. SA60 was rejected because it has no current limit. In the Power sheet, it takes only about a minute to find that the PA93 cannot handle the internal power dissipation (about 140W). Switching to PA04 reveals the circuit is possible, but would require a 0.2°C/W heatsink to keep junction temperatures to 150°C and has efficiency in the 50% area. This temperature may not be acceptable from a reliability point of view and leaves poor choices for the heatsink. Choice one is the Apex HS11 with liquid cooling; read this as costing nearly as much as the amplifier before calling a plumber. Choice two involves a custom heatsink.

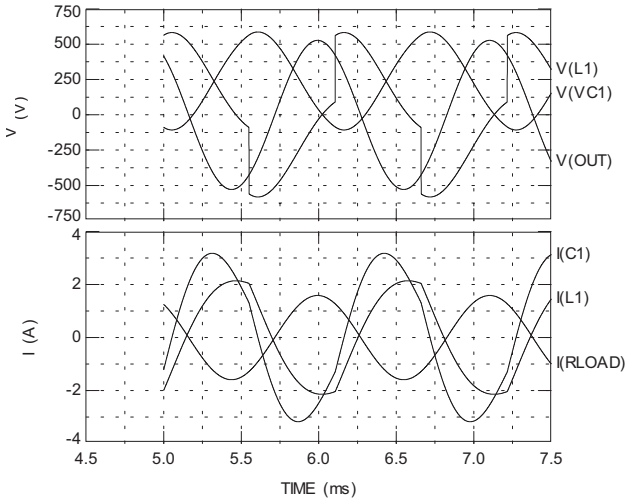

FIGURE 19. SQUARE WAVES THROUGH A 6 POLE FILTER COME OUT AS LARGER SINE WAVES

The SA01 PWM amplifier is the most cost effective choice and will run much cooler. With PWM amplifiers, a power supply voltage substantially higher than peak output voltage is not a killer in terms of internal power dissipation. This allows an 80V unregulated supply, saving a lot in terms of efficiency, cost and design time over a regulated supply required by a linear solution. The SA01 circuit will follow the voltage control example given in Application Note 30 PWM BASICS. It was determined that 150mV peak ripple at the 42KHz switching frequency would be acceptable. In order to maximize pass band flatness and avoid the numerous pitfalls of driving signals right up to the cutoff frequency, Fc will be designed for 4KHz. Figure 20 shows this data loaded into the PWM Filters sheet of Power Design.

Figure 21 gives all the component choices for the third order filter. If a single ended filter was desired, components under that heading would be used. If a dual capacitor topology is desired, use components from the dual cap column. To form the most common topology, the split inductor, this example will use inductors from the differential column and capacitors from the single-ended column. Leg capacitors will be 0.27uF per Figure 11. The 2.28Ap-p ripple will be the maximum ripple in L1 at the switching frequency. The 0.57A is used to calculate power loss in the amplifier.

The inductors will be custom wound. L1s are 47 turns of #12 on a Micrometals T184-18 torriodal core. L2s are 39 turns of #12 on a T130-18 core. The single ended capacitor is metallized polypropylene and the leg capacitors are X7R ceramic. The matching network capacitor is a pair of 1uF, X7R ceramics in parallel. Figure 22 shows the delivered power to be about 2% low at the lowest frequencies. This is primarily from copper loss in the inductors and suggests a simple gain adjustment be included in the circuit. At first glance the power roll-off at 2KHz looks a bit large. However a linear sweep analysis of a perfect drive to the voice coil reveals the coil inductance itself is responsible for over half this droop.

With your own copy of Power Design, you will use the PWM Power sheet to find the SA01 delivers full power while averaging an internal loss of under 15W. When mounted on the Apex HS16 without a fan, the SA01 will have a case temperature rise of only 19°C and junctions only 3°warmer. Adding in filter loss (including the matching network) as shown in Figure 23, still yields efficiency better than 92% over most of the frequency band.

Example 2 This example illustrates the transformer-like action of a PWM system. The requirement is to drive a 2Ω thermo-electric cooler at ±10V, using an existing single 48V supply. Any linear solution will draw 5A or 240W from the supply and will need to dissipate 190W. SA60 is the least expensive PWM amplifier having analog input capability. A 10Hz bandwidth will be plenty and ripple voltage should be kept below 100mV across the cooler. It is also desirable to keep the common mode ripple as low as possible, so a dual capacitor filter will be considered. A first pass with the PWM Filter sheet loaded with switching frequency=45KHz and cutoff frequency=100Hz, called for inductors of 2.25mH and capacitors of 1125uF. The large capacitance

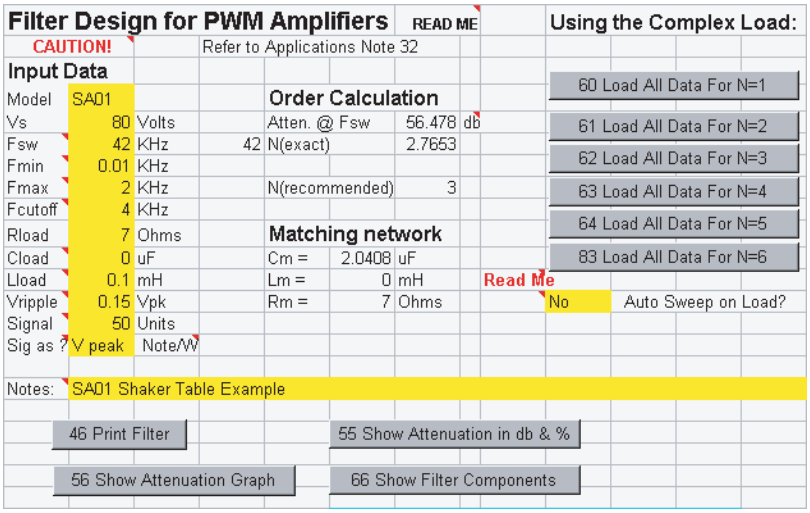

FIGURE 20. SETTING UP THE PWM DESIGN FOR ANALYSIS

Shading indicates values for Split Inductor topology				
		Dual Cap Filter		Single-ended Filter
N = 3	L1 =	0.2089	mH	0.4178 mH
	C =	15.157	uF	7.5786 uF
	L2 =	0.0696	mH	0.1393 mH
	P-P Iripple =	2.2796	Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.5699		

FIGURE 21. THIRD ORDER DATA ONLY FROM THE COMPONENTS SCREEN

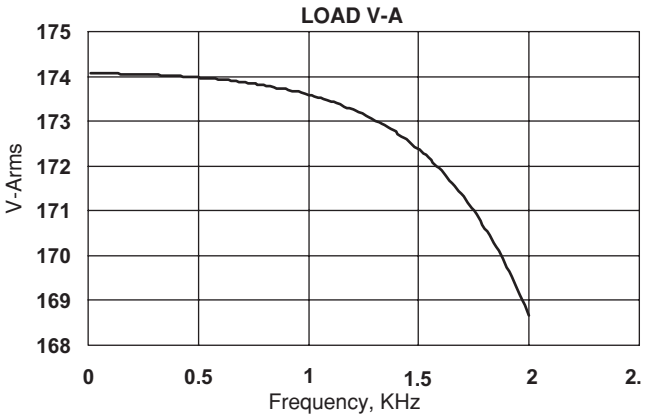

FIGURE 22. POWER DELIVERY TO THE SHAKER TABLE

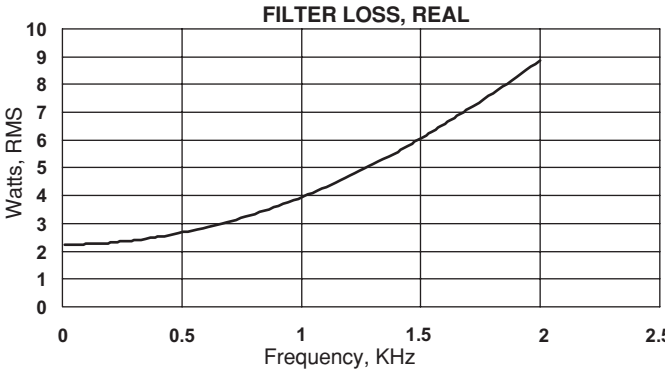

FIGURE 23. POWER LOSS IN THE FILTER AND MATCHING NETWORK

values suggest electrolytic types which generally offer lower performance in the high frequency spectrum. A second pass at the design set cutoff frequency at 1KHz, yielding the data in Figure 24.

In checking available metallized polypropylene capacitors, it was discovered that a single-ended capacitor would cost less than a third that of the pair of dual value capacitors. The final filter shown in Figure 25 is a hybrid where the table for leg capacitors is ignored and the three capacitors form the equivalent of a 55uF single capacitor and provide excellent common mode attenuation.

Figure 26 illustrates finding default parasitics and loading equivalent components to run the frequency sweep on. In the Filter Component Work Area, enter values by hand and then use button 91 to calculate the parasitics. Note the 0.1Ω and 23nH values calculated for the 10µF capacitors. The equivalent single-ended capacitor has half the capacitance and twice the resistance and twice the inductance. Translate back to single-ended with button 88 and return to the Define Load area when the sweep is complete. Now enter the equivalent values for the pair of 10µF capacitors as shown in Figure 27, and run the sweep.

Now for the real beauty of this circuit: when delivering the full 5A (50W), the SA60 mounted on an Apex HS03 1.7°C/W heatsink (needs a mounting hole drilled), has an internal dissipation of only about 15W! Throwing in filter loss also, the supply is working to the tune of only about 70W, or about 1.5A.

Shading indicates values for Split Inductor topology				
		Dual Cap Filter		Single-ended Filter
N = 2	L =	0.2251	mH	0.4502 mH
	C =	112.54	uF	56.269 uF
	P-P Iripple =	1.1848	Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.2962		

FIGURE 24. CHANGING Fc TO 1KHz YIELDS MORE REASONABLE COMPONENT VALUES

Example 3 This circuit drives a magnetic bearing requiring up to 12A DC plus up to 3A peak AC up to 300Hz. Bearing coil inductance is 5mH and resistance is 2Ω. Using the Power sheet reveals the AC drive will require 29Vpk, which brings total peak voltage up to 54V. As the PWM circuit will be inside a larger loop based on a position sensor, low phase shift is much more important than amplitude accuracy. The SA03 will handle this job using a current output circuit based on its data sheet typical application. Maximum 22.5KHz ripple voltage at the bearing is 1V peak. Knowing that filters shift phase the least amount in the lowest portion of the bandpass, it was decided to set the cutoff frequency to 3KHz. A split inductor topology will be used with N=3. This data was loaded into Power Design yielding 80uH for the L1s, 35uF for the capacitor, 27uH for the L2s, and 1250uF for the capacitor in the matching network. Leg capacitors will be 1uF. Figure 28 shows the initial current control results.

In checking the graph on load current, it agrees by saying current at 300Hz is down to about 20% of DC levels. The ideal filter keeps output voltage constant in the pass band. In this case the large inductance of the load called for an R-C matching network, which draws most of the current at 300Hz.

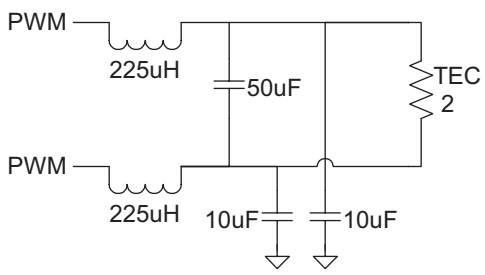

FIGURE 25. A CROSS BETWEEN SPLIT INDUCTOR AND DUAL CAPACITOR TOPOLOGIES

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Filter Component Work Area				README					
	Pole 1			Pole 3			Pole 5		
	L1	0.225	mH	L2	0	mH	L3	0	mH
	Rl1	0.0775	ohms	Rl1	0	ohms	Rl3	0	ohms
	Cl1	25.625	pF	Cl1	20	pF	Cl3	20	pF
	Pole 2			Pole 4			Pole 6		
	C1	50	uF	C2	10	uF	C3	0	uF
	Rc1	0.134949	ohms	Rc2	0.1	ohms	Rc3	0.15	ohms
	Lc1	32.08661	nH	Lc2	23	nH	Lc3	30	nH
Select Capacitor type: E=electrolytic, P=plastic or ceramic									
		p			P			E	

FIGURE 26. FINDING DEFAULT PARASITICS FOR A HYBRID FILTER TOPOLOGY

Pole 1			Pole 3		
L1	0.45	mH	L2	0	mH
Rl1	0.155	ohms	Rl1	0	ohms
Cl1	12.8125	pF	Cl1	5	pF
Pole 2			Pole 4		
C1	50	uF	C2	5	uF
Rc1	0.134949	ohms	Rc2	0.1	ohms
Lc1	32.08661	nH	Lc2	23	nH

FIGURE 27. MANUAL ENTRY OF COMPONENT EQUIVALENTS FOR A HYBRID FILTER TOPOLOGY

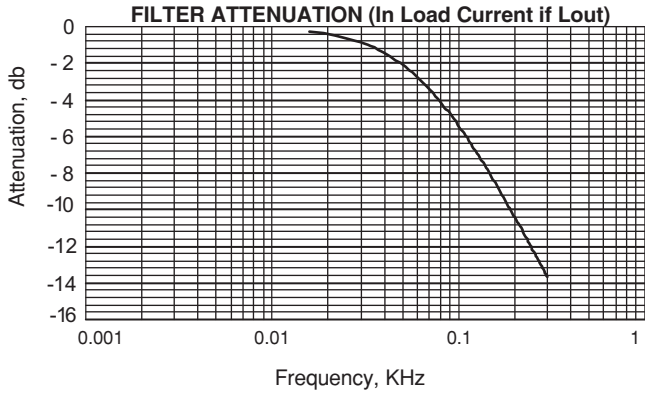

FIGURE 28. THIS IS IDEAL RESPONSE?

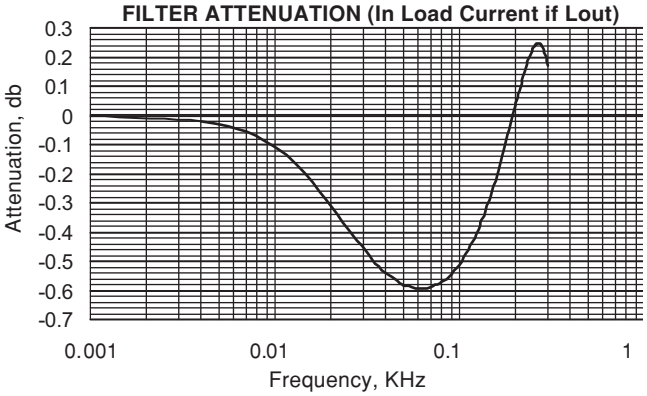

FIGURE 29. DB RESPONSE OF THE MODIFIED MATCHING NETWORK

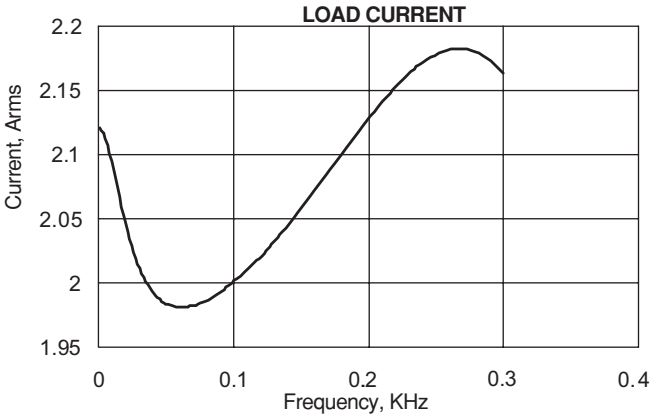

FIGURE 30. CURRENT OUTPUT WITH THE MODIFIED MATCHING NETWORK

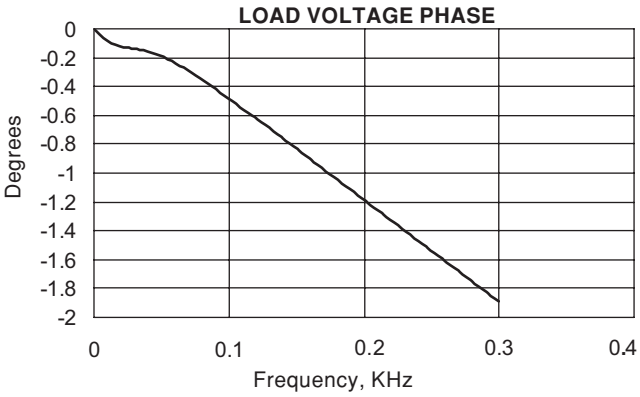

FIGURE 31. OUTPUT VOLTAGE PHASE WITH THE MODIFIED MATCHING NETWORK

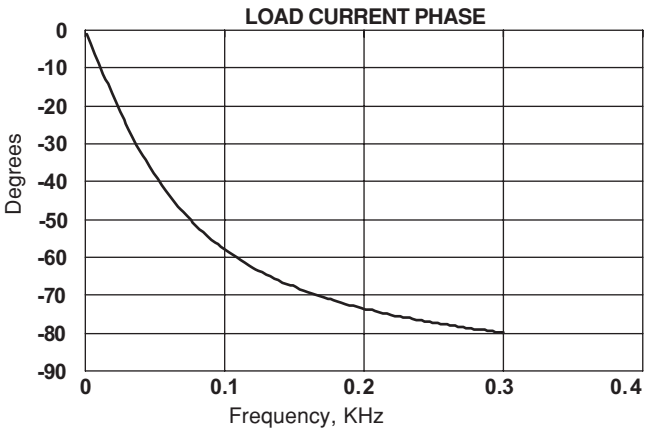

FIGURE 32. CURRENT OUTPUT PHASE WITH THE MODIFIED MATCHING NETWORK

We found earlier that removing a matching network causes voltage peaking at the filter output; this is exactly what we need to keep current constant due to the bearing inductance. Total removal causes about an 8db peaking (a gain of about 2.5), but a few iterations later, 470uF and 13? was found to produce the results shown in Figures 29-34.

To estimate internal power dissipation for the SA03, a new sweep was run with amplitude set to the RMS sum of 12A DC and 3Apk AC (~12.2Apk). Putting the 1.48°C/W minimum rating from this sweep into the Heatsinks sheet brings up the HS06 rated at .96°C/W. This will result in a case temperature a little over 60° and junctions a little over 70° at maximum drive.

10.0 FINAL CONSIDERATIONS

DO NOT DRIVE THESE FILTERS WITHOUT PROPER LOADING.

If you were taught to never have a load on a power circuit the first time you turn it on, be aware that the resonant circuits of these filters can generate voltages many times larger than the input voltage.

Poor circuit layout cannot be remedied by good filtering. PWM circuits, by their nature, have high frequency, and high power transients, that are difficult to eliminate from the desired output signal. Use ground planes and shielding as much as possible, but do not use these as a high current path. Use wide traces on circuit boards for power supply and output signals and heavy gauge wire for interconnects. Use star grounding techniques with the PWM amplifier ground pin as the center. A very small amount of inductance can cause large transients where high currents switch quickly. A rule of thumb is to expect 20nH per inch of conductor. Assume all output current changes its path through the PWM output switches each cycle of the switching frequency in 20 to 50ns. Space circuit board traces and wiring away from sensitive circuits to avoid extraneous noise pickup. Use bypass capacitors liberally.

The response curves for prefect components imply that the attenuation increases continuously with increasing frequency. With real components and real interconnects this is simply not the case. If you have a design claiming 150db attenuation, check it again.

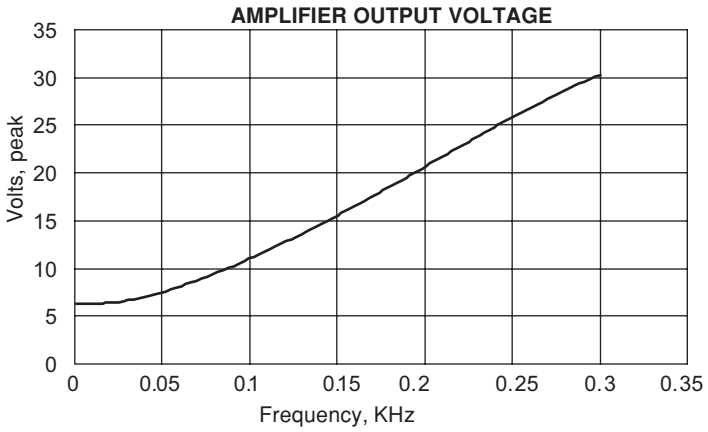

FIGURE 33. AMPLIFIER OUTPUT VOLTAGE WITH THE MODIFIED MATCHING NETWORK

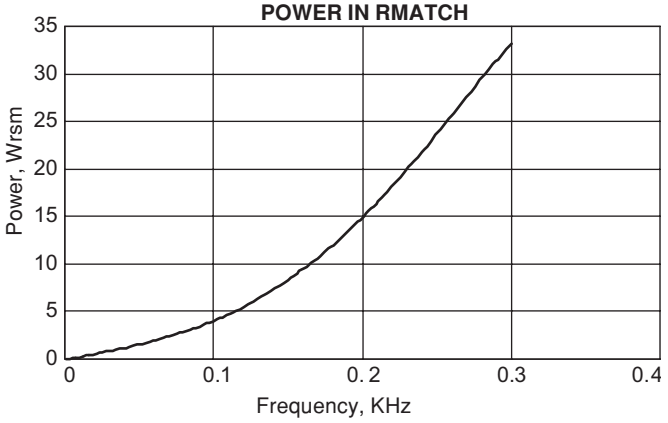

FIGURE 34. POWER DISSIPATION IN THE MODIFIED MATCHING NETWORK

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APPLICATION NOTE 33

PULSE WIDTH MODULATION AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

PWM AMPLIFIER INTRODUCTION

The recent availability of high-voltage and high-current PWM amplifiers in hybrid packages has attracted the interest of many designers who traditionally use linear amplifiers. The advantage of PWM amplifiers is obvious: efficiency of 70 to 97%. High efficiency translates to lower internal power loss, smaller heat sinks, and reduced overall physical size.

To make it easier to design with these amplifiers, a simple and versatile generic PWM Spice model lets you check out PWM waveforms without the fear of blowing up the amplifiers or getting shocked by high voltages. The methodology behind generating such a model applies not only to hybrid PWM amplifiers, but also to monolithic and discrete PWM amplifiers. The inputs to the model come from the PWM amplifier's data sheet, and you can run the model on any commercial Spice program.

Even though a PWM amplifier offers analog signals in and analog signals out, its circuit functionality is entirely different from a linear amplifier's. A PWM amplifier modulates a pulse train in the time domain and uses LC filtering to extract the analog-signal output. You can use PWM amplifiers to emulate linear constant- voltage amplifiers or linear constant-current amplifiers, both at much higher levels of efficiency.

If you're unfamiliar with how a PWM amplifier works, you're not alone. Just like op amps, PWM amplifiers come in many sizes and flavors, some with fancy bells and whistles. Fortunately, the amplifiers all operate under the same principle.

A PWM amplifier converts an analog signal into a pulse train of variable duty cycle. The analog input controls the duty cycle of the output pulse train, which switches on and off once during each cycle. When a high output is necessary, the pulse train switches on most of the time and vice versa.

Figure 1a shows a basic PWM amplifier. Vin is the analog input of 1 to 8V dc. AOUT is a pulse train, and BOUT is its inverse. The PWM oscillator determines the frequency of the pulse train, and some PWM amplifiers allow you to put in your own PWM oscillator. As Vin changes from its minimum to its maximum value, the duty cycle of AOUT changes from 0 to 100%, and the duty cycle of BOUT changes from 100 to 0%. The difference voltage of AOUT–BOUT has the same pulse train as AOUT but with double the amplitude of 2xVs p-p (Figure 1b).

If you connect a dc brush-type motor across AOUT and BOUT, you can control the motor speed with Vin. When you set Vin in the middle of its range, for 50% duty cycle at AOUT and BOUT, the motor stands still. With Vin at its maximum, the motor turns at maximum rpm; with Vin at its minimum, the motor reverses direction of rotation and turns at maximum rpm again. You can directly connect AOUT and BOUT to a motor because the winding inductance of the motor turns the pulsed voltage into a rippled dc current whose magnitude controls the motor speed and whose polarity controls the clockwise or counterclockwise direction of the motor. As Figure 1a indicates, most other applications need LC filters to filter out the PWM pulse train to ensure that an analog signal appears at the load.

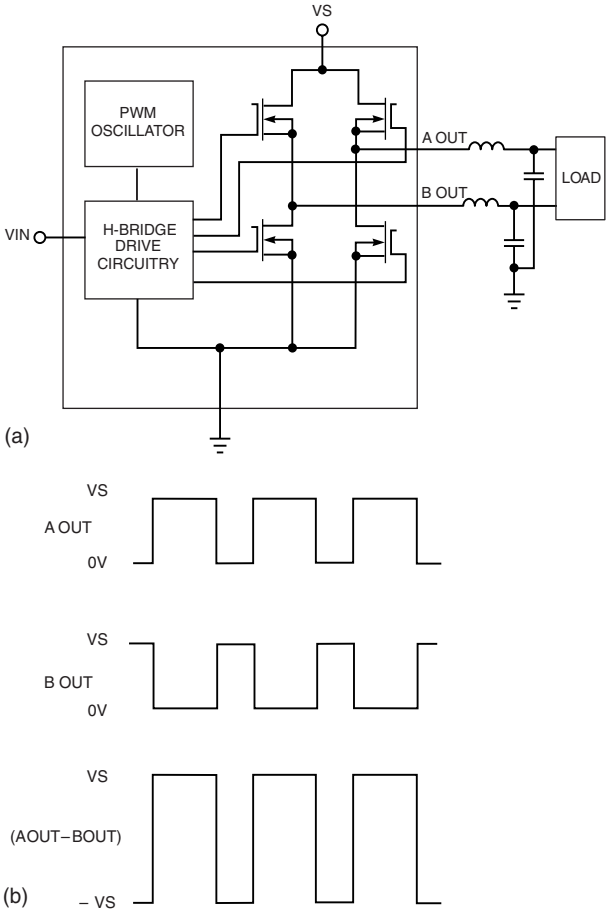

FIGURE 1. A PWM amplifier (a) converts an analog signal into a pulse train of variable duty cycle (b). AOUT and BOUT can directly drive a dc motor, but most other loads require additional LC filtering.

USE A GENERIC SPICE MODEL

Figure 2 shows the generic Spice subcircuit model of a PWM amplifier. V1 is a ramp of fixed frequency. E1 serves as a comparator that converts the PWM ramp as it crosses Vin into a variable-duty-cycle pulse train (**Figure 3**). S5, V5, S6, and V6 limit the amplitude of the pulse train to ±5V. S1/R1, S2/R2, S3/R3, and S4/R4 represent the four MOSFET drivers for which R1, R2, R3, and R4 are the respective

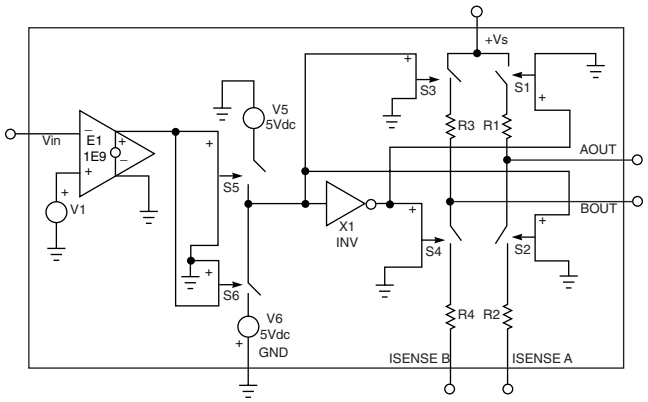

FIGURE 2. A generic Spice model of a PWM amplifier includes a fixed-frequency ramp (V1), a comparator (E1), an inverter (X1), and MOSFET drivers (S1 to S4) and their respective on-resistances(R1 to R4).

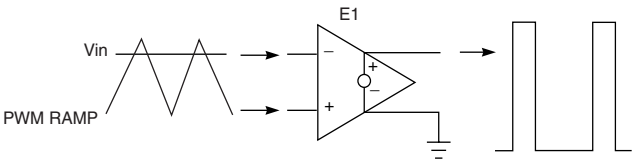

FIGURE 3. In the PWM amplifier model, E1 serves as a comparator that converts the PWM ramp as it crosses Vin into a variable duty cycle pulse train.

on-resistances. The four MOSFETs always turn on and off in diagonal sets,that is, when S1 and S4 are on, S2 and S3 are off and vice versa. The inverter X1 provides the diagonal switching control. ISENSE A and ISENSE B are current-sensing terminals, usually available at two output pins for current-feedback control circuitry. For open-loop operation or for voltage-feedback control, just connect ISENSE A and ISENSE B to ground.

When an external load connects between AOUT and BOUT, current flows from Vs to ground through one of two routes: Vs to S1/R1, to an externally connected load between AOUT and BOUT, to S4/R4, and then to ground or Vs to S3/R3, to the external load, to S2/R2, and finally to ground. The voltage across the load actually doubles the Vs voltage. For example, when Vs=100V, the voltage across the load is 200V p-p. This voltage-doubling feature is another advantage PWM amplifiers offer for high-voltage applications. To double voltage using linear amplifiers you must use two linear amplifiers in a bridge-mode configuration.

DESIGN EXAMPLE: CONSTANT–CURRENT AMPLIFIER

You commonly use constant-current amplifiers for applications such as motor-torque control and battery chargers. You can use the model and the specifications of a commercial PWM amplifier—in this case, the Apex SA50—to design a constant-current amplifier (also called a voltage-to-current converter). You start out with the following specifications from the SA50 data sheet:

Analog input voltage/output duty cycles:
Vin=4V; AOUT=0% and BOUT=100%
Vin=6V; AOUT=50% and BOUT=50%
Vin=8V; AOUT=100% and BOUT=0%
switching frequency: 45 kHz.
MOSFET on-resistance: 0.5Ω total or 0.25Ω each

The analog input voltage range of 4 to 8V dc and the switching frequency of 45 kHz determine the waveform of the PWM ramp (Figure 4), which V1 in Figure 2 produces. You can describe this waveform as a constant-voltage source in any commercial Spice program, such as Intusoft's Model ICAP/4Rx V8.8.1. You enter V1's parameters as

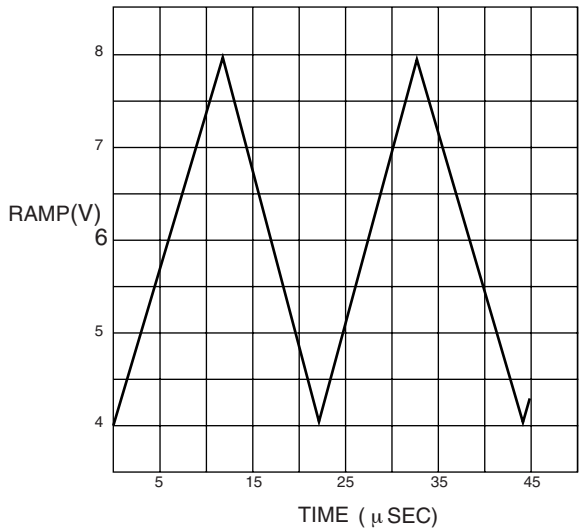

FIGURE 4. The analog input-voltage range and the switching frequency (in this case, 4 to 8V and 45kHz, respectively) determine the waveform of the PWM ramp.

manual-driven inputs, and this Spice program automatically generates the following statement for V1: V1 12 0 PULSE 4 8 0 11.1E-6 11.1E-6 1E-12 22.2E-6, where "12 0" designates the two nodes for V1.

The MOSFET on-resistance of 0.25V determines the values of R1, R2, R3, and R4. The addition of Rq=600V and Vcc=12V model the SA50 amplifier's quiescent current and the low-voltage power supply necessary to power the H-bridge drive circuitry.

Figure 5 shows the complete Spice subcircuit for the SA50. This basic SA50 can drive a bidirectional motor for which Vin controls the motor speed and direction of rotation. You can add LC filters that let you drive other loads. Even when driving a motor, LC filters next to the amplifier module are useful for EMI and EMC purposes. Without filters,

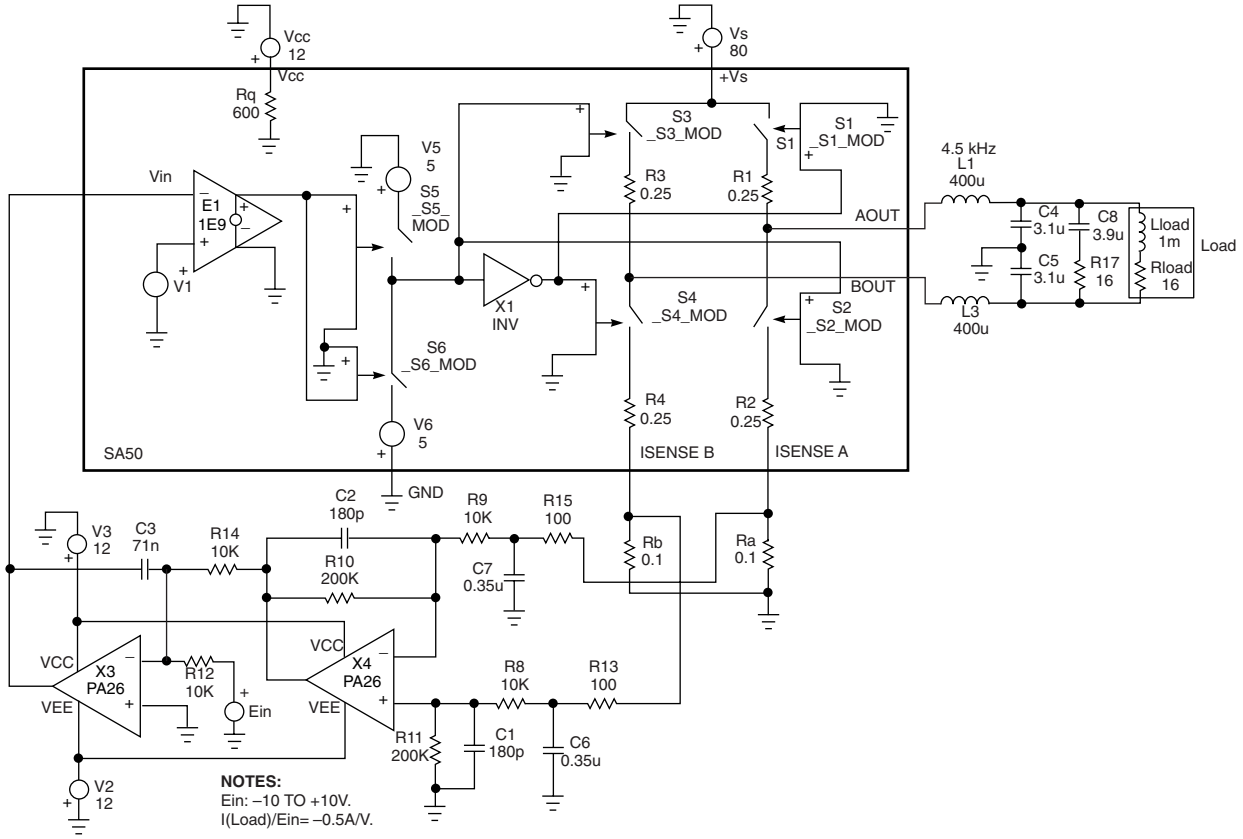

FIGURE 5. Combining the generic Spice model with the specifications for the SA50 PWM amplifier, you can use the model to simulate a voltage-controlled, constant-current amplifier.

the long cables to the motor carry high-voltage switching pulses and act as antennas. Because the waveform across AOUT and BOUT is a pulse train of variable duty cycle and because Vin, the analog input signal, controls the pulse train's duty cycle or pulse width, you must first filter the PWM pulse train to extract the analog output signal.

In Figure 5, the load comprises Rload and Lload. L1, C4, L3, and C5 form a low pass filter with a cut off frequency (Fc) of 4.5 kHz to filter out the SA50 amplifier's 45-kHz PWM pulse train. A rule of thumb is to set the LC filter's corner frequency one decade below the PWM frequency. Of course, you can push the corner frequency higher by using multiple-pole LC filters. The equations to calculate filter LC values are as follows:

$$L1 = L3 = \frac{1.4142 \cdot Rload}{2\pi \cdot Fc} \cdot 0.5, \quad (1)$$

and

$$C4 = C5 = \frac{0.7071}{2\pi \cdot Fc \cdot Rload} \cdot 2. \quad (2)$$

Because of the filter's differential configuration, these equations include a x0.5 factor for L1 and L3 and a x2 factor for C4 and C5. In this example, Rload=16Ω, and Fc=4.5 kHz, so L1=L3=400 μH, and C4=C5=3.1 μF. Because the load for this example is inductive, adding the matching network of R17 and C8 creates a combined load of 16Ω. The equations for R17 and C8 are as follows:

$$R17 = Rload, \quad (3)$$

$$C8 = \frac{Lload}{Rload^2}. \quad (4)$$

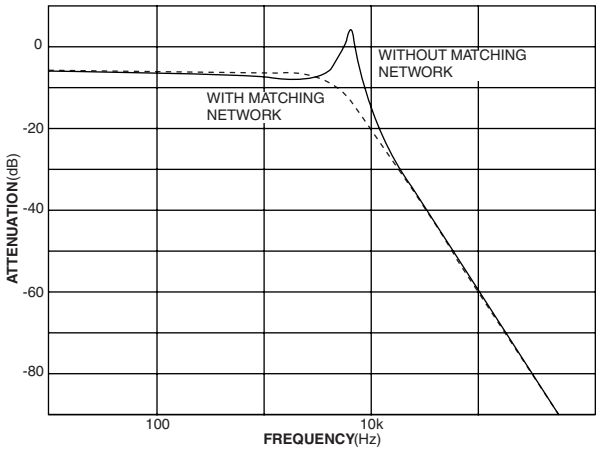

FIGURE 6. The LC filter's frequency response differs with and without the matching network.

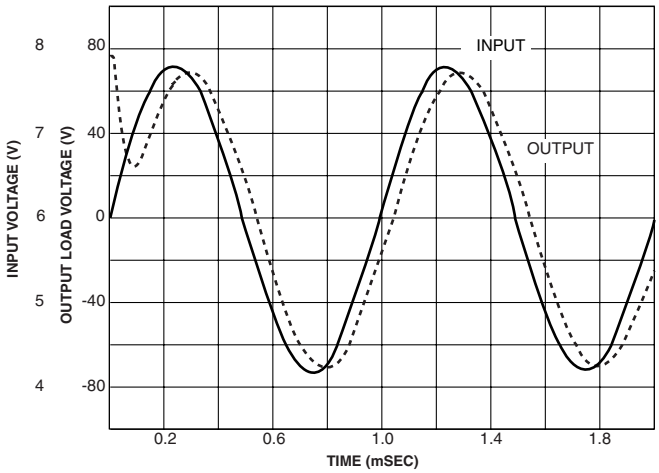

FIGURE 7. Ignoring the feedback circuitry of X3 abd X4, a 1-kHz, 3.5V p-p sine wave with offset at Vin produces a 120V p-p sine wave across the load.

In this example, Lload=1 mH, and Rload=16Ω, so C8=3.9 μF, and R17=16Ω. Similarly , if you have a capacitive load, you can use a LC matching network to make the combined load resistive, for which

$$L = Cload \cdot Rload^2. \quad (5)$$

Figure 6 shows the frequency response of the filter with and without the matching network. Ignoring the feedback circuitry of X3 and X4, a 1kHz 3.5V p-p sine wave with 6Vdc offset at Vin produces a 120V p-p sine wave across the load (**Figure 7**) .

To complete the design of a constant-current amplifier , you must have some means of sensing the load current and provide feedback control in case of a load change. Ra and Rb are the two current-sensing resistors. Op amp X4 and its associated components serve two purposes: first, as a difference amplifier with a gain of 20 that converts the current difference between Ra and Rb into a voltage output of – 0.5A/V and, second, as a lowpass filter comprising C1, C2, C6, and C7 that filters the ripple currents in Ra and Rb with a corner frequency of 4.5 kHz. The design equations are as follows:

$$GAIN = -\frac{R9}{R10 \cdot Ra} \ A/V, \quad (6)$$

$$C6 = C7 = \frac{1}{2\pi \cdot R13 \cdot Fc}, \quad (7)$$

$$C1 = C2 = \frac{1}{2\pi \cdot R10 \cdot Fc}. \quad (8)$$

To minimize power losses, you should choose Ra and Rb values of 0.01 to 0.1Ω. In this example, Fc=4.5 kHz, R8=R9=10 kΩ. To minimize loading effects, these resistors must be much greater than R13=R15=100Ω. Substituting these values into Equation 7 and Equation 8, C6=C7=0.35 μF, and C1=C2=180 pF. Choosing R10=200 kΩ, Equation 6 yields a gain of –0.5 A/V.

X3 is an integrator that compares the error voltage from X4 with the input voltage Ein and provides the correct input voltage for the SA50 amplifier to close the feedback loop. The design equations for the integrator are as follows:

$$R12 = R14, \quad (9)$$

$$C3 = \frac{1}{2\pi \cdot (0.05Fc) \cdot R12}. \quad (10)$$

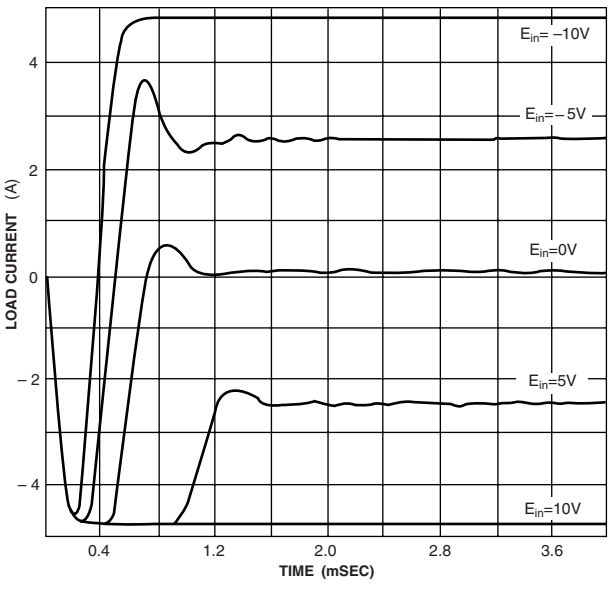

FIGURE 8. Spice-simulation runs indicate the load-current waveforms of the constant-current amplifier for various values of Ein.

```
*#save V(1) V(25) @R4[i] @R4[p] V(3) @R1[i] @R1[p] V(5)
*#save V(29) @R3[i] @R3[p] V(7) V(19) @R2[i] @R2[p] V(9)
*#save @Vs[i] @Vs[p] V(10) @S4[i] @S4[p] V(11) @S2[i] @S2[p]
*#save @S3[i] @S3[p] @S1[i] @S1[p] V(12) @V1[i] @V1[p] V(13)
*#save V(18) @E1[i] @E1[p] @V5[i] @V5[p] V(8) @S6[i] @S6[p]
*#save @V6[i] @V6[p] V(17) @Rload[i] @Rload[p] @Lload[i] @Rb[i] @Rb[p]
*#save @Ra[i] @Ra[p] V(16) V(14) V(20) V(21) @R8[i] @R8[p]
*#save @R9[i] @R9[p] @R10[i] @R10[p] @R11[i] @R11[p] @V3[i] @V3[p]
*#save @C1[i] @C2[i] V(24) V(18) V(26) @R12[i] @R12[p] @VEin[i]
*#save @VEin[p] @C3[i] @R14[i] @R14[p] @S5[i] @S5[p] V(15) V(30)
*#save V(2) @L1[i] @L3[i] @C4[i] @C5[i] @R13[i] @R13[p] @C6[i]
*#save @R15[i] @R15[p] @C7[i] V(23) V(29) V(6) V(4) V(21)
*#save V(22) @V2[i] @V2[p] V(27) @Vcc[i] @Vcc[p] @Rq[i] @Rq[p]
*#save V(28) @R17[i] @R17[p] @C8[i] @Rload[i]
*#VIEW  TRAN Y1
*#alias Y1 @Rload[i]
.TRAN 22.2E-9 4000E-6 0 22.2E-8 UIC
.PRINT  TRAN Y1
R4 1 25 0.25
R1 3 23 0.25
R3 5 29 0.25
R2 7 19 0.25
Vs 9 0 DC=80
S4 29 1 10 0 _S4_mod
.MODEL _S4_mod SW VT=2.5 RON=1E-9 ROFF=1E9
S2 23 7 11 0 _S2_mod
.MODEL _S2_mod SW VT=2.5 RON=1E-9 ROFF=1E9
S3 9 5 11 0 _S3_mod
.MODEL _S3_mod SW VT=2.5 RON=1E-9 ROFF=1E9
S1 3 9 10 0 _S1_mod
.MODEL _S1_mod SW VT=2.5 RON=1E-9 ROFF=1E9
X1 11 10 INV { }
.SUBCKT INV 1  2
*          in out
B1 3 0 V= ~V(1)
RD 3 2 1
CD 2 0 .87NF
.ENDS
V1 12 0 PULSE 4 8 0 11.1E-6 11.1E-6 1E-12 22.2E-6
E1 13 0 12 18 1E9
*#save  @E1[i] @E1[p]
L1 23 4 400u
V5 15 0 DC=5
S6 11 8 0 13 _S6_mod
.MODEL _S6_mod SW VT=2.5 RON=1E-9 ROFF=1E9
V6 0 8 DC=5
Rload 17 6 16
V2 0 22 DC=12
Lload 4 17 1m
Rb 25 0 0.1
Ra 19 0 0.1
X4 16 14 20 21 22 PA21 { }
.SUBCKT PA21 1 2 3 4 5
* PINOUT ORDER +IN -IN OUT +V -V
Q1 10 1 8 QI1
Q2 11 2 9 QI2
R3 12 8 7.39E+03
R4 12 9 7.39E+03
I2 12 5 3.61E-05
C1 12 5 2.73E-12
R5 12 5 1.11E+06
R1 4 10 8.85E+03
R2 4 11 8.85E+03
C2 10 11 9.00E-12
I1 4 5 3.70E-02
G1 6 15 11 10 1.13E-04
G2 6 15 12 15 6.36E-09
R6 6 15 1.00E+05
D1 6 15 DD
D2 15 6 DD
C3 6 7 3.00E-11
G3 15 7 15 6 8.85E+00
R7 7 15 1E3
D3 7 16 DD
V1 18 16 1.60E+00
D4 17 7 DD
V2 17 19 1.60E+00
RE1 15 0 0.001
E2 18 0 4 0 1
E3 19 0 5 0 1
R8 7 20 50
C4 20 15 3.08E-09
Q3 19 20 21 QOP
Q4 18 20 22 QON
Q5 4 23 29 QON
Q6 5 24 30 QOP
Q7 25 27 31 QLN
Q8 26 28 31 QLP
R11 21 23 1.70E-01
RCLP 29 31 1.70E-01
RCLN 30 31 1.70E-01
R13 22 24 1.70E-01
D5 23 25 DL
D6 26 24 DL
R9 27 29 1E3
R10 28 30 1E3
I3 18 23 7.92E-03
I4 24 19 7.92E-03
R15 31 3 5.42E-01
RSN 3 34 1
CSN 34 5 0.1E-6
.MODEL DD D(CJO=0.1PF IS=1E-17)
.MODEL DL D(CJO=3PF IS=1E-13)
.MODEL QI1 NPN (BF=6.55E+02 IS=8E-16)
.MODEL QI2 NPN (BF=4.24E+02 IS=8.46E-16)
.MODEL QOP PNP (BF=4.64E+02 IS=1E-14)
.MODEL QON NPN (BF=4.64E+02 IS=1E-14)
.MODEL QLN NPN (BF=100 IS=1E-14)
.MODEL QLP PNP (BF=100 IS=1E-14)
.ENDS
R8 16 30 10K
R9 14 2 10K
R10 14 20 200K
R11 16 0 200K
Vcc 27 0 DC=12
V3 21 0 DC=12
C1 16 0 180p
C2 14 20 180p
Rq 27 0 600
X3 0 24 18 21 22 PA21 { }
R12 24 26 10K
VEin 26 0 DC=10
C3 18 24 71n
S5 15 11 13 0 _S5_mod
.MODEL _S5_mod SW VT=2.5 RON=1E-9 ROFF=1E9
L3 29 6 400u
R14 24 20 10K
C4 4 0 3.1u
C5 0 6 3.1u
R17 28 6 16
R13 30 25 100
C6 30 0 0.35u
C8 4 28 3.9u
R15 2 19 100
C7 2 0 0.35u
.END
```

LISTING 1. SA50 CONSTANT -CURRENT- AMPLIFIER SPICE CIRCUIT

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You can complete the design by choosing R12=R14=10 kΩ and C3=71 nF (**Figure 6**).

You can now run the Spice program. The load current waveforms (**Figure 8**) are as expected. Note that there is a small error between the Spice output and the expected value.

For example, with Ein=10V, the expected output current should be –5A, but Figure 8 shows –4.8A. This difference is because of the loss resulting from the 0.25Ω MOSFET's on-resistance. If you set the on-resistance to zero, you get exactly –5A. Listing 1 is the complete Spice circuit description for the constant-current amplifier.

CONSTANT–VOLTAGE AMPLIFIER

In applications such as audio-speaker drivers, motor-speed control, and power inverters, you need a constant voltage amplifier. You can use the Apex SA02 to design a high efficiency, high-power PWM audio-speaker driver. The SA02 data sheet lists the following specifications:

Analog input voltage/output duty cycles:
Vin=1.25V; AOUT=0%, BOUT=100%
Vin=2.50V; AOUT=50%, BOUT=50%
Vin=3.75V; AOUT=100%, BOUT=0%
switching frequency: 250-kHz
MOSFET on-resistance: 0.42Ω total or 0.21Ω each.

The LC filter design is similar to that of the constant-current amplifier except the LC filter requires no matching network because of the 8Ω resistive load (**Figure 9a**). The SA02 amplifier's PWM frequency is 250 kHz, so the design sets the LC filter's corner frequency to 25 kHz. The design of the difference amplifier (X4) is somewhat different, however. This constant-voltage amplifier configuration senses the output voltage, not the output current. The voltage at AOUT and BOUT is much higher than the voltage across the current-sensing resistors in the previous example. Instead of boosting the gain, resistor dividers lower the sense voltage to levels that a small signal amplifier can handle. The integrator's (X3) time constant is faster to provide the frequency response necessary for audio applications. The SA02 audio-speaker driver has a –10V/V voltage gain and a 10-kHz power bandwidth. Figure 9b shows the circuit's input and output waveforms. Note that it takes about 50 μsec for the output's sinewave to stabilize.

The SA02 has many bells and whistles, such as thermal sensing and external-logic shutdown, that the generic model does not implement. A design engineer can easily analyze these independent features with a paper and pencil. However, this simple yet versatile model makes it easy to model the main PWM function when manual analysis of this feed-back-control circuit becomes unmanageable.

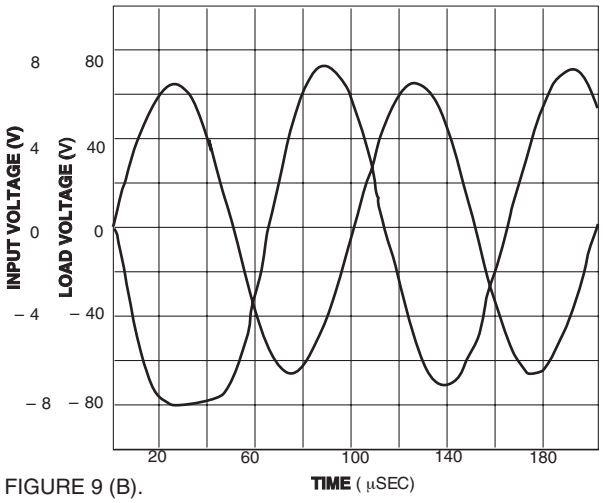


FIGURE 9 (B).

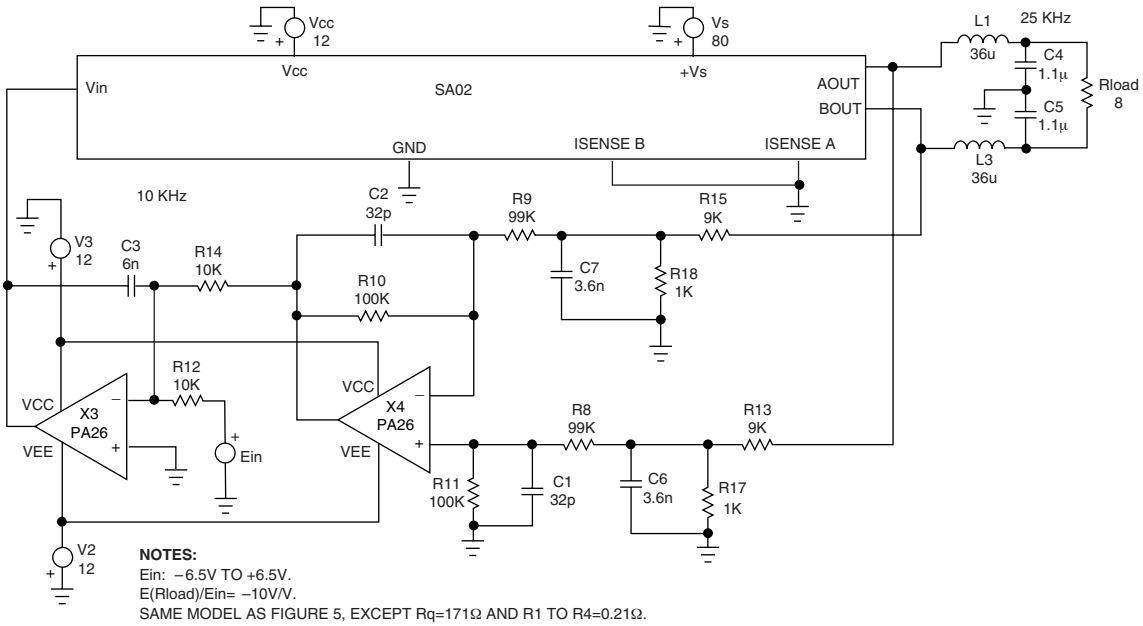


FIGURE 9 (A). A similar model using specifications from the SA02 amplifier is part of a constant-voltage feedback amplifier (a). The output sine wave takes about 50 μsec to stabilize (b).

APPLICATION NOTE 34

PULSE WIDTH MODULATION AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

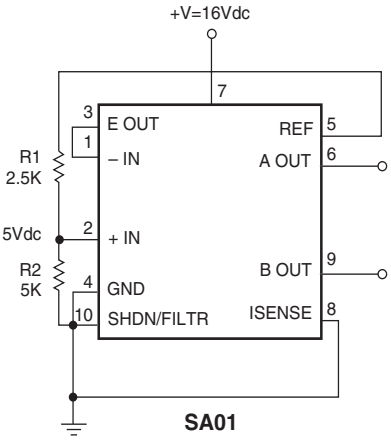
INTRODUCTION

Hybrid PWM amplifiers are widely used in applications such as motion control, offline drivers, capacitor discharge welder controller, and audio speaker drivers. When you first build an engineering prototype to check out your application circuit, it may not work the first time. So, you do the trouble shooting. One common question is, "is my PWM amplifier still working?" Well, maybe. You can always pull it out from your circuit board, ship to Apex and request for a retest in Apex' ATE tester. But, you may have to wait for days or weeks to get an answer back. Chances are you need the answer right then. Well, you can do it yourself and it is surprisingly simple. While they are not shown on these diagrams, be sure to bypass all supplies with ceramic capacitors (1μF recommended) with short leads. You don't need a 100V, 30A power supply to test, for example, an Apex SA03, which is rated at 100V and 30A. All you need is a 15V, 100mA power supply and an oscilloscope. Why? Because Apex had already tested every SA03 for its 100V, 30A capability, and all other guaranteed parameters before shipping to you. If the PWM is subsequently damaged in your application, the probability is remote that a 100V PWM amplifier will become an 80V amplifier, or its 30A current capability will be reduced. More likely, it is damaged to the point of not functioning at all.

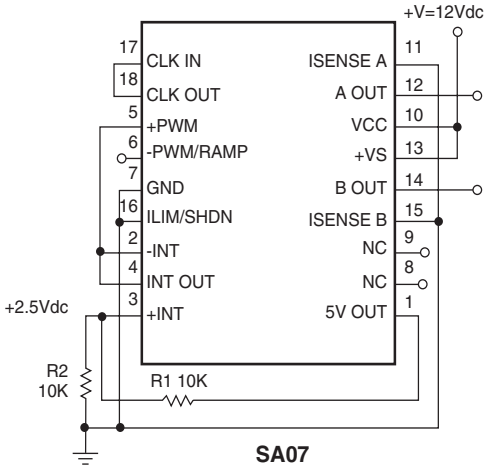
FUNCTIONALITY TEST CIRCUITS

The purpose of this application note is to prescribe a very simple circuit (Figure 1A and 1B) for each Apex PWM model to test for functionality. The circuit is not intended to test for parametric shifts.

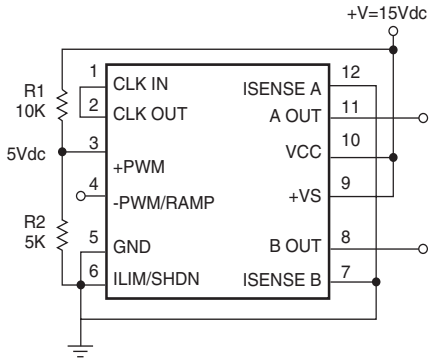
FIGURE 1A. FUNCTIONALITY TEST CIRCUITS FOR DIFFERENT APEX PWM AMPLIFIER MODELS.



SA01



SA07



SA03, SA04, SA06, SA08, SA12

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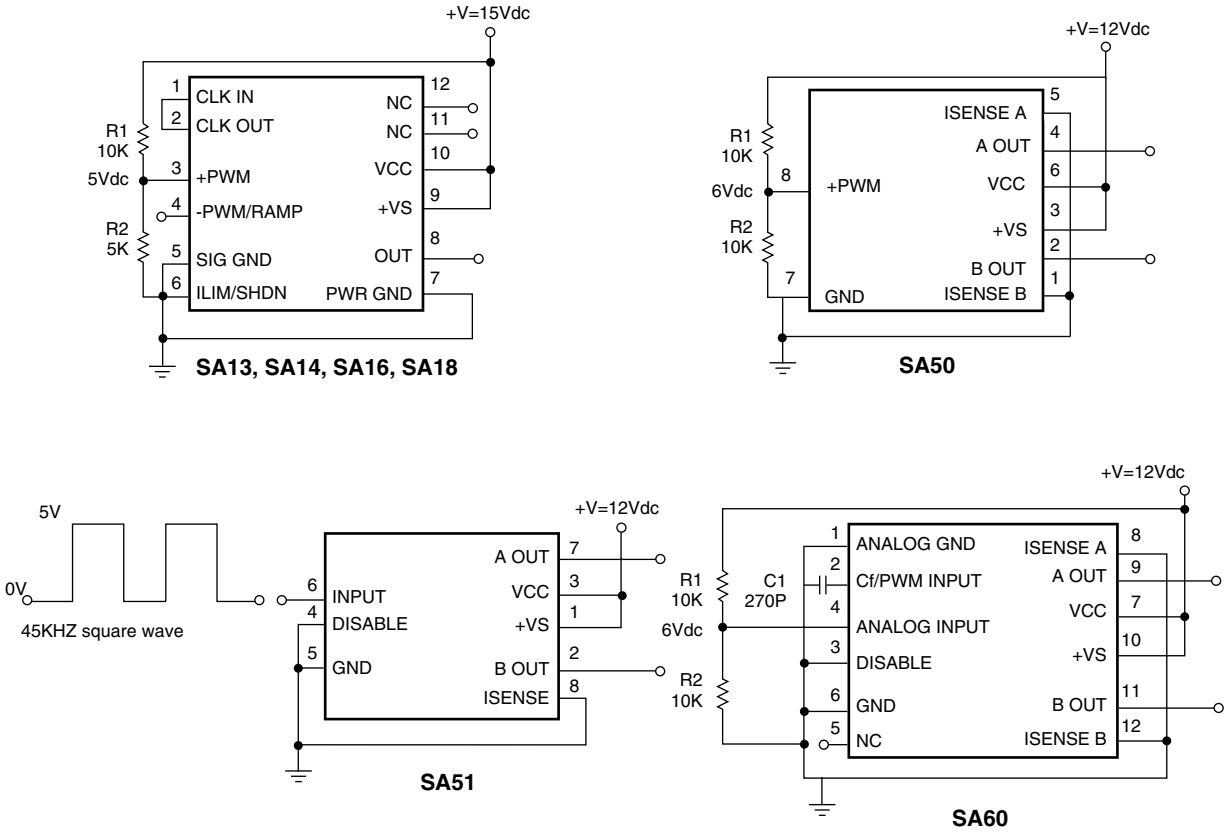
FIGURE 1B. FUNCTIONALITY TEST CIRCUITS FOR DIFFERENT APEX PWM AMPLIFIER MODELS.



LOOK FOR OUTPUT WAVEFORMS

Use an oscilloscope to look at the waveforms at AOUT and BOUT. You should see two square waves as shown in Figure 2; one is inverted, or 180 degrees out of phase, from the other. For half bridge models, the SA13, SA14, SA16 and SA18, you have only one output and will see only one square wave.

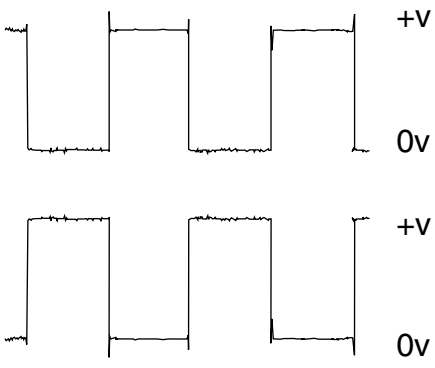


FIGURE 2. OUTPUT WAVEFORMS AT AOUT (TOP) AND BOUT (BOTTOM).

The square wave's amplitude should be the same as your power supply voltage, and its frequency is as follows:

SA01 - 42 KHz	SA13 - 22.5 KHz
SA03 - 22.5 KHz	SA14 - 22.5 KHz
SA04 - 22.5 KHz	SA16 - 22.5 KHz
SA06 - 22.5 KHz	SA18 - 22.5 KHz
SA07 - 500 KHz	SA50 - 45 KHz
SA08 - 22.5 KHz	SA51 - 45 KHz
SA12 - 200 KHz	SA60 - 45 KHz

If you do see two square wave outputs, or one square wave for a half bridge PWM amplifier, your amplifier is alive and well. Otherwise you will see at least one of the following symptoms, which implies your PWM amplifier is dead and needs to be replaced.

1. A high impedance DC voltage at AOUT or BOUT or both. That DC voltage can be near 0V or near +Vs. Or,
2. The output is not a square wave, but a ramp. Or,
3. High current drain, greater than 100mA, from your power supply.

APPLICATION NOTE 35

PULSE WIDTH MODULATION AMPLIFIER

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INTRODUCTION

High power PWM amplifiers are now available in the 200V to 500V range with current ratings in the 10A to 20A range. Such PWM can be used to build transformerless AC/DC power supplies whose output DC voltage is linearly proportional to an input control signal. It operates just like linear amplifier's whose gain is set by resistor values. Such amplifier's efficiency is much higher, usually in the 90% range, because of PWM technique.

Why transformerless? In applications such as driving magnetic bearings, electric power in the order of kilowatts is required. A transformer at such power ratings is heavy and expensive. It is very desirable to do it without the transformer. In portable equipment that one has to carry from one place to another, the elimination of a heavy duty transformer makes it a lot lighter to carry around.

Other applications that require the combined functions of AC/DC conversion plus amplification include DC motion control and powering high current linear amplifiers. In controlling brush type DC motors, one needs an AC/DC power supply plus an amplifier to control the voltage across the motor or the current through the motor. This AC/DC power supply does the job of both. You obtain the power from your 115 Vac wall socket and control the motion of your DC motor directly. Another application is in the testing of high current devices such as micro-processors, memory chips and logic circuits with programmable V-I (voltage and current) sources that are built into most automatic test equipment. At first thought, you can use this transformer-less AC/DC power supply as a programmable V-I source, as shown in Figure 1a. In practicality, this power supply uses PWM switching technique and the switching noises are usually too high and not acceptable for such applications. To work around this problem, you can use this programmable AC/DC power supply to drive a linear amplifier like the Apex PA03 which in turn drives the real load, as shown in Figure 1b. A linear amplifier with power supply rejection in the 60 dB to 100 dB range will suppress the switching noises from this programmable AC/DC power supply. Key advantage of such an arrangement is to keep the internal power dissipation of the PA03 at its minimum. The PA03 is capable of delivering 30A of output current continuously. With a constant voltage at Vcc and the same load current, PA03's power dissipation increases as the load voltage drops. This programmable AC/DC allows PA03's Vcc to drop or to increase in proportion to the load voltage, and thus keeps the PA03's internal power dissipation at a constant level. Because this AC/DC uses PWM technique with efficiency in the 90% range, its internal power dissipation is minimal as compared to that of the PA03.

To design a complete transformer-less AC/DC power supply, we will first start out with a paper and pencil design, then use Spice simulation to verify the paper design and finally build a prototype to verify the Spice simulation.

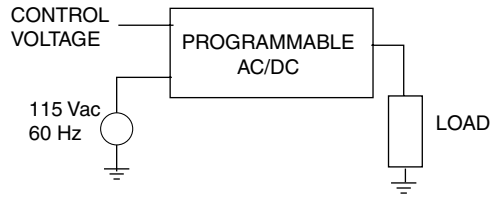


FIGURE 1A. USE A PROGRAMMABLE AC/DC POWER SUPPLY AS A V/I SOURCE FOR ATE. SWITCHING NOISE IS USUALLY TOO HIGH TO BE ACCEPTABLE FOR SUCH APPLICATIONS.

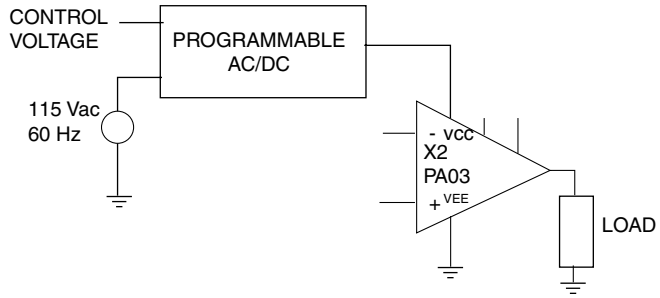


FIGURE 1B. A LINEAR AMPLIFIER LIKE THE PA03 WITH POWER SUPPLY REJECTION IN THE 60 DB RANGE SUPPRESSES NOISE FROM THE PROGRAMMABLE AC/DC SUPPLY.

FUNCTIONAL DIAGRAM

A block diagram to illustrate the functionality of a transformer-less AC/DC power supply is shown in Figure 2. Power is taken from 115 Vac wall outlet and goes through a diode rectifier, D1, which converts the input sinewave into a half wave rectified output. L1 and C1 is a filter that attenuates the harmonics of the half wave sine wave and extracts its DC component out to supply the high voltage PWM amplifier. The output of the PWM amplifier is a pulse train whose duty cycle is controlled by its input voltage through a resistor divider made up of R1, R2 and R3. L2 and C2 is another filter that attenuates the harmonics of the PWM pulse train and extracts its DC components out as a programmable high voltage and high current DC source. Thus this AC/DC power supply's output DC voltage is linearly proportional to the PWM amplifier's input control voltage.

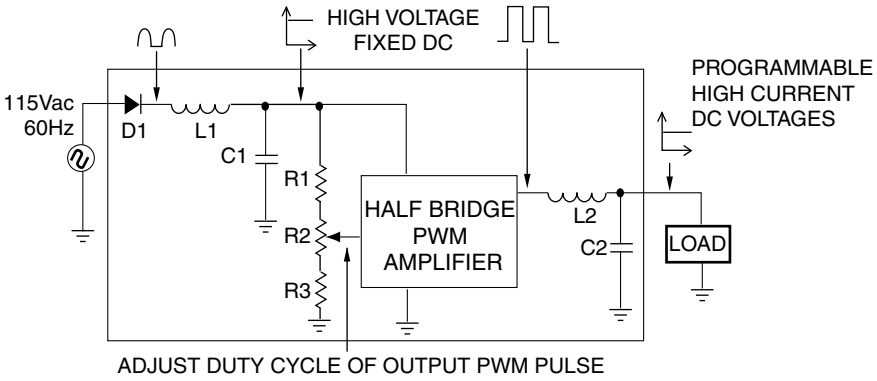


FIGURE 2. TRANSFORMERLESS AC TO DC CONVERTER FUNCTIONAL DIAGRAM

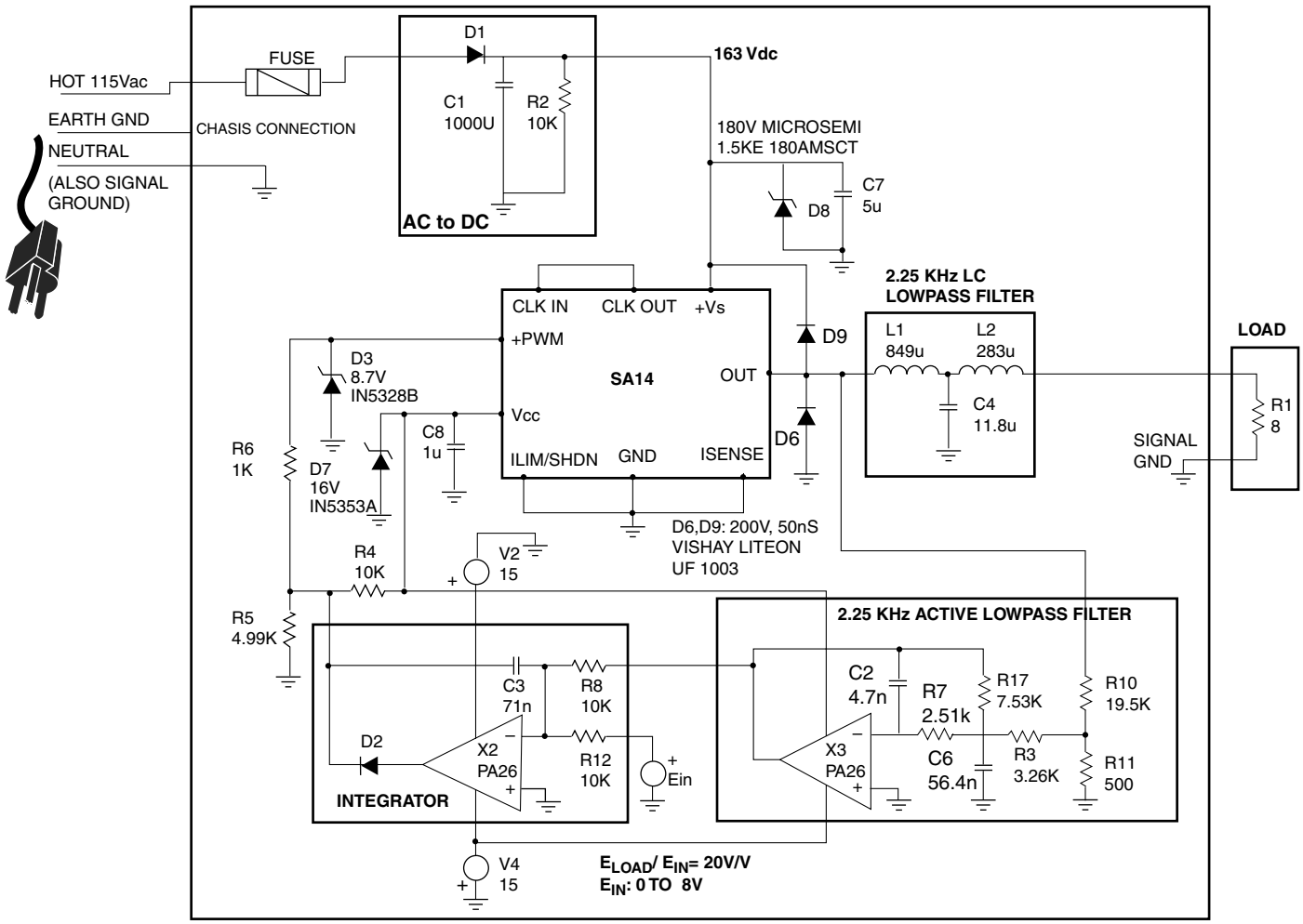


FIGURE 3. DETAILED TRANSFORMERLESS AC TO DC CIRCUIT DIAGRAM.

COMPLETE CIRCUIT DESIGN EXAMPLE

The functional diagram in Figure 2 has no feedback or voltage regulation. Thus, the output DC voltage will not be very stable and will change with external environment such as load change, temperature, +Vs ripple, ... etc. In a real world circuit, feedback control is necessary to compensate for such environmental changes. Figure 3 is a complete circuit made up of the following blocks:

AC-TO-DC.

D1 is a diode rectifier whose reverse voltage must be at least 326V (= 2 x 115V x 1.4142). C1 is a smoothing capacitor whose value affects the output ripple. The larger, the better but also more expensive and bulky. We will arbitrarily start out with C1 = 1000 uF because it is available with voltage rating of 200 V, in electrolytic type, and at reasonable price. Analytical calculation of output ripple versus C1 is very complex because of the PWM waveform. It is not practical if not impossible. We will later use Spice to see the output ripple reduction with increased C1. R2 is a bleeder resistor whose value determines how fast it will discharge the capacitor C1 after power is turned off. R2's wattage must be equal or greater than (163*163/R2). With R2 = 10K, it must be 2.66W or larger.

SA14.

Apex SA14 is the PWM amplifier of choice because of its 200 V, 20 A rating. The 115 Vac will provide a peak voltage of 163 V (= 115*1.4142) so the PWM amplifier must have a voltage rating of at least 163 V. In some foreign countries where the ac power source is 230 Vrms, choose the Apex SA16 or SA08 whose voltage rating is 500 V.

2.25 KHZ LC LOWPASS FILTER.

L1, L2 and C4 form a 3-pole lowpass filter with Butterwoth (maximum flatness) frequency response for the 8 ohm load. The corner frequency is set at 2.25 KHz, one decade below SA14's 22.5 KHz PWM frequency. As the load changes, the filter's corner frequency will not change but its peaking, or Q factor will change. To achieve even lower ripple and noise, use higher pole filters. The design of LC filters can be found in reference 1 and reference 3.

2.25 KHZ ACTIVE LOWPASS FILTER.

This filter block and the next integrator block form voltage feedback control for the AC/DC power supply. Active filter is used here because this is the small signal processing path, not the power transmission path. Active filter is smaller and cheaper. The design of active filters can be found in reference 2. The SA14 is an inverted PWM amplifier, that is, as SA14's input increases, the duty cycle of its output decreases. We choose the multiple feedback active filter configuration because of its polarity inversion to reverse SA14's polarity.

You can verify if your feedback loop has the correct polarity by using the following check:

Start out with SA14's +PWM input and arbitrarily assume that it is increasing. SA14's output will decease because it is an inverted PWM amplifier. Op amp X3's output will then increase because SA14's output drives the (-) input of X3. Op amp X2's output will decrease again because X3's output drives the (-) input of X2. Since X2's output drives SA14's +PWM input, the former decreases while the latter was arbitrarily assumed increasing. They go in opposite directions and that is negative feedback. If they go in the same direction, it becomes positive feedback and your circuit won't work.

INTEGRATOR

This integrator completes the voltage feedback loop when the filtered output of SA14 is compared with an external voltage Ein. In this example, the transfer function is given by Eload/Ein = 20 V/V where Ein ranges from 0V to 8V.

PROTECTION COMPONENTS.

Each and every functional block described above is necessary for the functionality of the AC/DC power supply. The following protection components are highly recommended to protect the SA14 from accidental blow out. It is a cheap insurance.

D6 AND D9

Fast recovery diodes used to protect the SA14 from inductive kickbacks. Model UF1003 from Vishay Liteon is chosen because of its 50 nsec reverse recovery time and 200V reverse diode break down voltage. You need at least 163V and the diodes should be 200 nsec or faster.

D3 AND D7

These are zener diodes to prevent over-voltage at various inputs. D3 prevents the +PWM input from going above 8.7V and from going below -0.65V. D7 prevents the Vcc input from going above 16V and from going below 0.65V.

D8

This is a transzorb (transient absorber) to prevent over-voltage at the +Vs terminal, and it also absorbs energy from high voltage spikes. Model 1.5KE180AMSCT from Microsemi is chosen because of its 180 V rating, which must be above the 163 V needed to operate the SA14 and must be equal or below SA14's rated voltage of 200 V.

C7 AND C8

These are power supply bypass capacitors and must be located as close to the Vcc pin and +Vs pin as possible. In no case should these capacitors be more than 2 inches away from their respective pins. Use low ESR capacitors such as ceramic.

D2, R4, R5 AND R6

These components prevent the SA14 from going into tri-state condition upon powering on. R4 and R5 set SA14's +PWM input at the mid range of 5V which puts SA14's output at 50% duty cycle immediately upon powering on. D2 prevents op amp X2 from sinking current which should never happen under normal operation. R6 prevents D3 and the +PWM input from over-current.

FUSE

Remember to include a 20A slow blow fuse in series with V1, your 115 Vac input power source.

SPICE SIMULATION RESULTS

The Spice model of SA14 is given in Figure 4 and is discussed in great detail in Reference 1. The SA14 is a half bridge PWM amplifier so one side of the H-bridge, or two of the four output Mosfet's, is removed from the full bridge PWM amplifiers discussed in Reference 1. In Figure 3, CLK IN, CLK OUT and ILIM/SHDN are the bells and whistles of the SA14 and are not modeled in Spice. Protection components discussed in the above

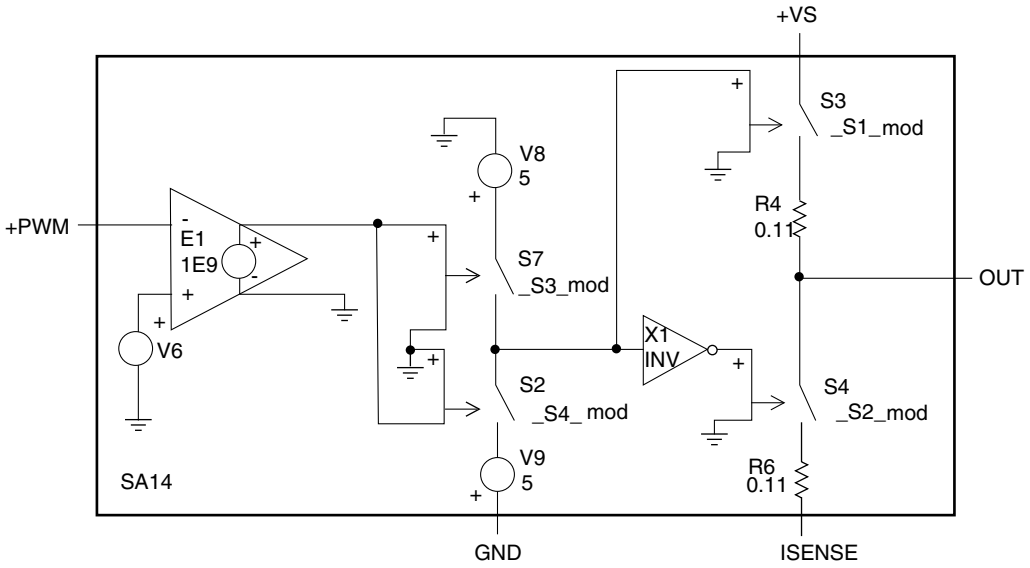


FIGURE 4. SA14 HALF BRIDGE PWM AMPLIFIER SPICE MODEL.

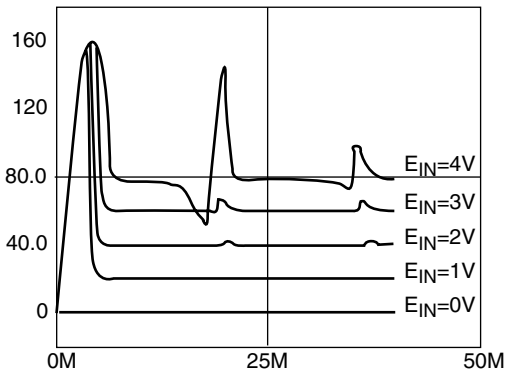


FIGURE 5A. SMOOTHING CAPACITOR C1=1000 μF

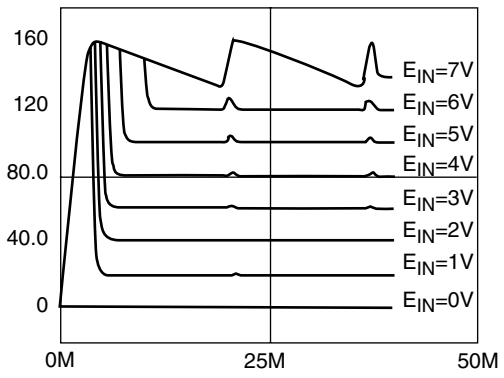


FIGURE 5B. SMOOTHING CAPACITOR C1=10,000 μF

FIGURE 5A AND B. TRANSIENT RESPONSE OF LOAD CURRENT.

paragraph are also excluded from Spice simulation because they do not affect normal circuit functionality. PA26's Spice model , which is the same as that of PA21, can be downloaded from the Apex Website (www.apexmicrotech.com). The rest of the circuit components are standard components available from most Spice libraries.

Figure 5a shows the transient response of the load current with different values of Ein. Note that the ripple increases as Ein, also the load voltage, increases. At 40V load voltage, the ripple is around 2 to 3 Vpp. If you need lower ripple, use a bigger smoothing capacitor. Figure 5b shows significantly lower ripples when the smoothing capacitor is increased to 10,000 uF.

MEASUREMENT RESULTS

In the actual prototype circuit, we tried to find components that are as close to the calculated values as practical. Sometimes calculated components are not available from our engineering stock and substitutes are used. Component deviations from the calculated values given in Figure 3 are listed below:

L1 = 820 uH
L2 = 200 uH
C3 = 82 nF
C4 = 10 uF
C6 = 57 nF.

Actual oscilloscope waveforms are shown in Figure 6a. The three load waveforms, from bottom to top, are respectively with inputs at 1 Vdc, 2 Vdc and 3 Vdc. There are two groups of ripple in each waveform. The ripple marked (A) is caused by the 60 Hz, 115 Vac power source, and can be lowered by increasing the capacitance for C1. Figure 6b shows the improved 60 Hz ripple by paralleling another 10,000 uF with C1 of 1000 uF. The improvement is especially noticeable with Ein = 3 Vdc. The high frequency ripple marked (B) in Figure 6a is caused by insufficient attenuation of the 22.5 KHz PWM pulse train by the three pole LC filter made up of L1, L2 and C4 in Figure 3. You can lower ripple (B) by increasing the number of poles for the LC filter. Figure 6c is the same as Figure 6a except R1 becomes open circuit. Note that high frequency ripples are noticeably higher because the LC filter no longer has a balanced load and its frequency response is no longer maximally flat. But, the 60 Hz ripple disappears because it is proportional to the load current.

This AC/DC power supply was designed with a gain of 20V/V. With Ein = 1 Vdc, Eout should be 20 Vdc and this is what Figure 6a shows in its bottom waveform. In the top waveform where Ein = 3 Vdc, Eout should be 60 Vdc while Figure 6a shows about 58 Vdc. The error is caused by the winding resistances of the inductors L1 and L2; and the error is higher at high output voltage and high current levels. You can eliminate this error by moving the voltage feedback point from the output of SA14 to the load, positive terminal of R1 (Figure 3). You will get better load voltage accuracy but at the expense of very restricted load variation. For example, if R1 becomes an open circuit, the LC filter will resonate near the corner frequency of 2.25 KHz. With voltage feedback taken at the positive terminal of R1, the whole feedback circuit will become unstable. On the other hand, if voltage feedback is taken from SA14's output, the load R1 and its associated LC filter do not affect loop stability.

HALF BRIDGE OR FULL BRIDGE

If you replace the half bridge rectifier in the AC to DC block of Figure 3 by a full bridge rectifier as shown in Figure 7, you will get significantly lower 60 Hz ripple with the same smoothing capacitor C1. Figure 8 shows the equivalent transient response as that of Figure 5a except with a full bridge rectifier.

The main disadvantage with the full bridge rectifier is the circuits signal ground being at 57.5 Vrms (=115 Vac/2) above the power cord's neutral line which is connected in your building's circuit breaker box to the protective earth ground. When using an oscilloscope to probe test points, you cannot connect the scope probe's ground clip, which is internally connected to the power cord's neutral wire, to this circuit's signal ground. You will get false readings because they are referenced to the wrong ground reference. Instead, use both channels of your oscilloscope and select "channel A minus channel B". Connect channel B to this circuit's signal ground and use channel A to do the probing. Connect the probes ground clip to power cord's neutral line.

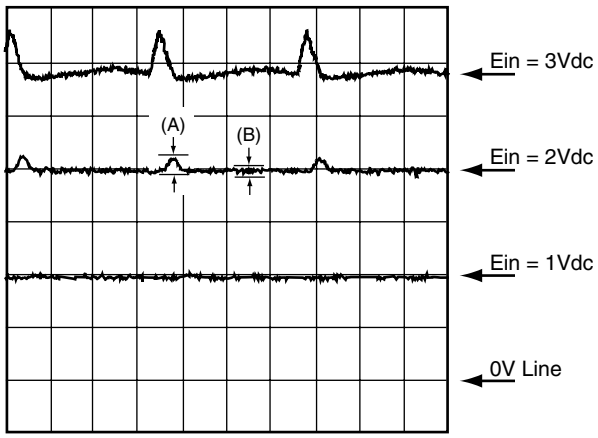


FIGURE 6A. MEASURED LOAD WAVEFORM. X SCALE: 5MS PER DIVISION; Y SCALE 10V PER DIVISION.

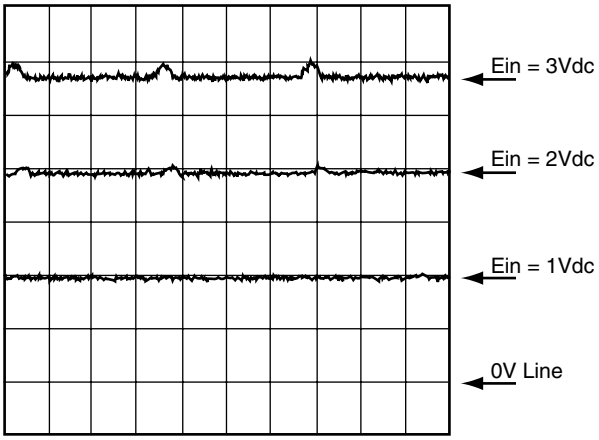


FIGURE 6B. ADDING A 10,000 μF IN PARALLEL WITH C1 LOWERS OUTPUT RIPPLE, ESPECIALLY AT HIGH CURRENT LEVELS.

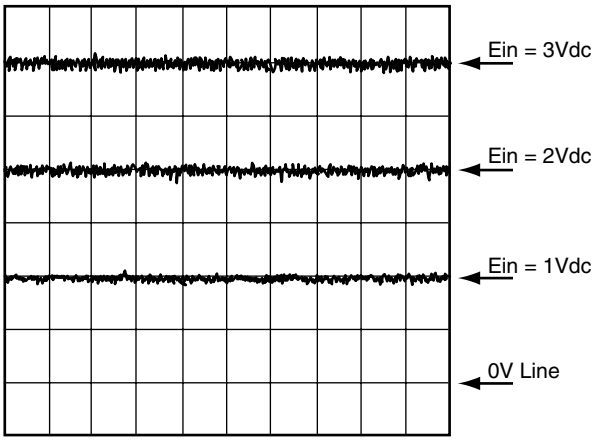


FIGURE 6C. WORKS WITH A WIDE RANGE OF LOADS. WITH R1 OPEN, HIGH FREQUENCY RIPPLE IS HIGHER BECAUSE OUTPUT LC FILTER IS UN-TERMINATED.

SAFETY WARNING

The voltage in this AC/DC power supply can kill! It should only be worked on by a skilled person who is aware of the hazard involved. Insulated clip test leads should be used for hands off measurements while troubleshooting. After the power cord has been disconnected, it is advisable to wait at least 2 minutes to let high voltage capacitors discharge over their bleeders. Do not work alone unless another person capable of rendering first aid and resuscitation is present.

Because this power supply uses no transformer, it also has no isolation between the 115 Vac power line and its internal circuitry. It is mandatory to use a 3-prong wall plug and cannot be used in applications where government or company regulation does require transformer isolation from power line. The hot (115 Vac) wire and the neutral wire must be wired correctly in both the wall plug and the wall receptacle. Use a receptacle circuit tester to check for faults such as reverse polarity, open ground, open hot, open neutral, hot/ground reversed, hot on neutral. If this power supply is housed in a metallic chassis, connect the chassis to the wall plug's protective earth ground.

Most other AC/DC power supplies use transformers and have 3 output terminals as +V, –V and Ground; you can connect either +V to Ground or –V to Ground. The Ground terminal is internally connected to its chassis and to the power cord's protective earth ground. Not on this transformerless power supply with no isolation. You cannot connect either one of the two output terminals to earth ground except, in the half bridge circuit, you can connect –V (marked as Signal Gnd in Figure 3) to the earth ground.

REFERENCES:

1. Y. J Wong, Spice Model Makes It Easy To Design With PWM Amplifiers, EDN, August 17, 1998
2. Y. J. Wong and W.E. Ott, Function Circuits, Design and Applications, McGraw-Hill Book Company, New York, 1976
3. Application Note 32, PWM Low Pass Filtering, Apex Microtechnology Corporation, Tucson, Arizona, 1998

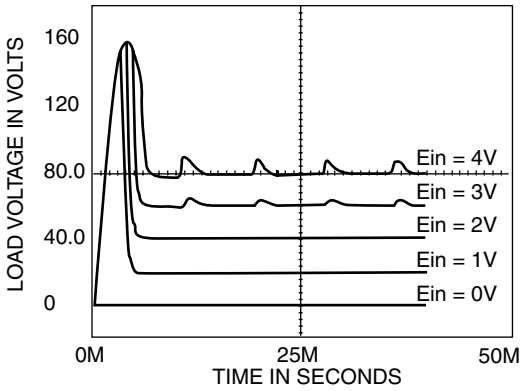


FIGURE 8. TRANSIENT RESPONSE OF LOAD CURRENT WITH FULL WAVE RECTIFIER, C1=1000 μF.

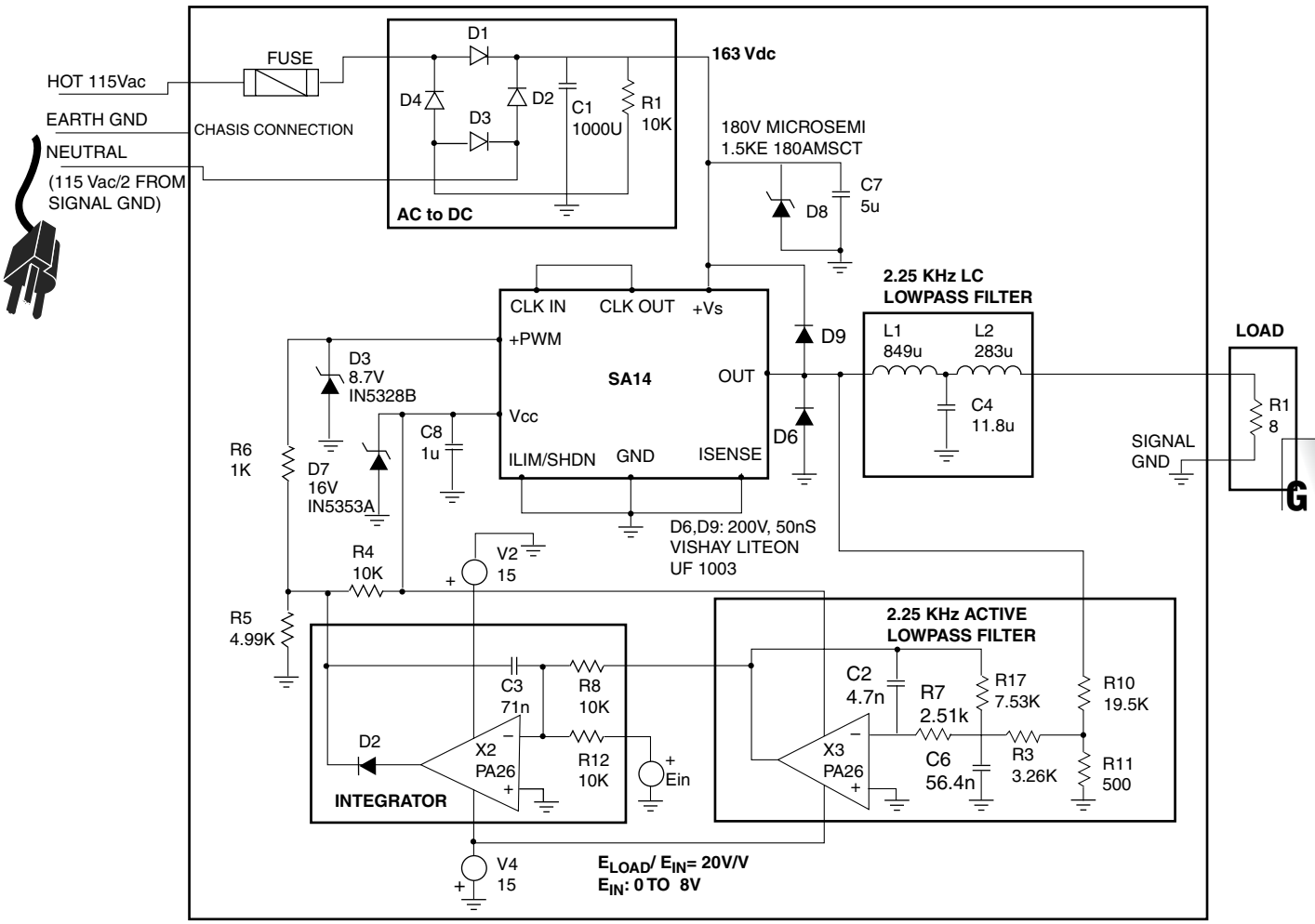
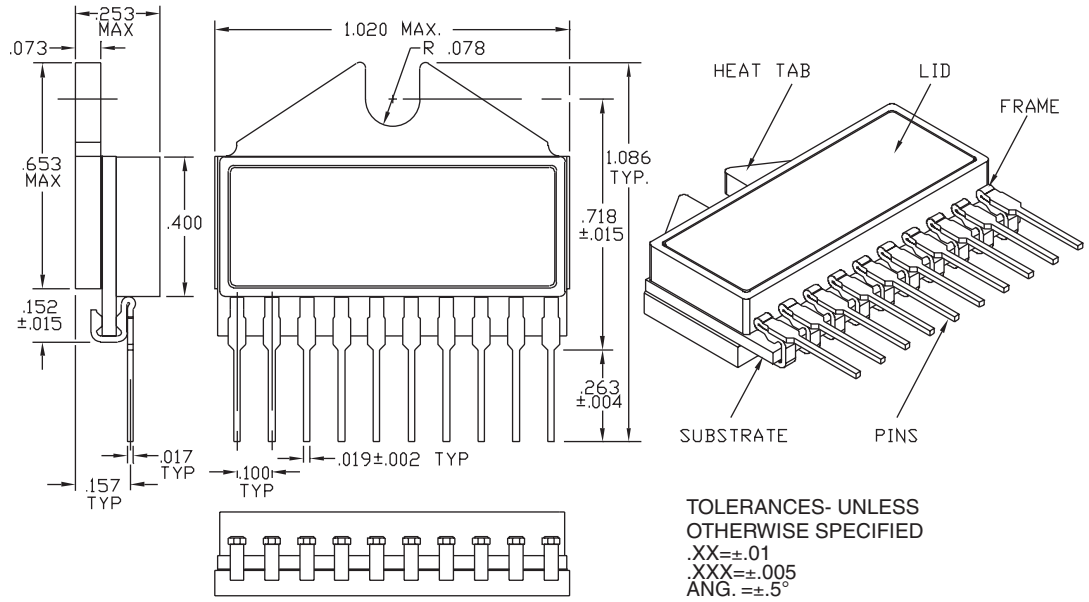


FIGURE 7. FULL BRIDGE RECTIFIER LOWERS OUTPUT RIPPLE BUT SIGNAL GROUND IS AT 57.5 Vrms FROM POWER CORD NEUTRAL WIRE.

APPLICATION NOTE 36

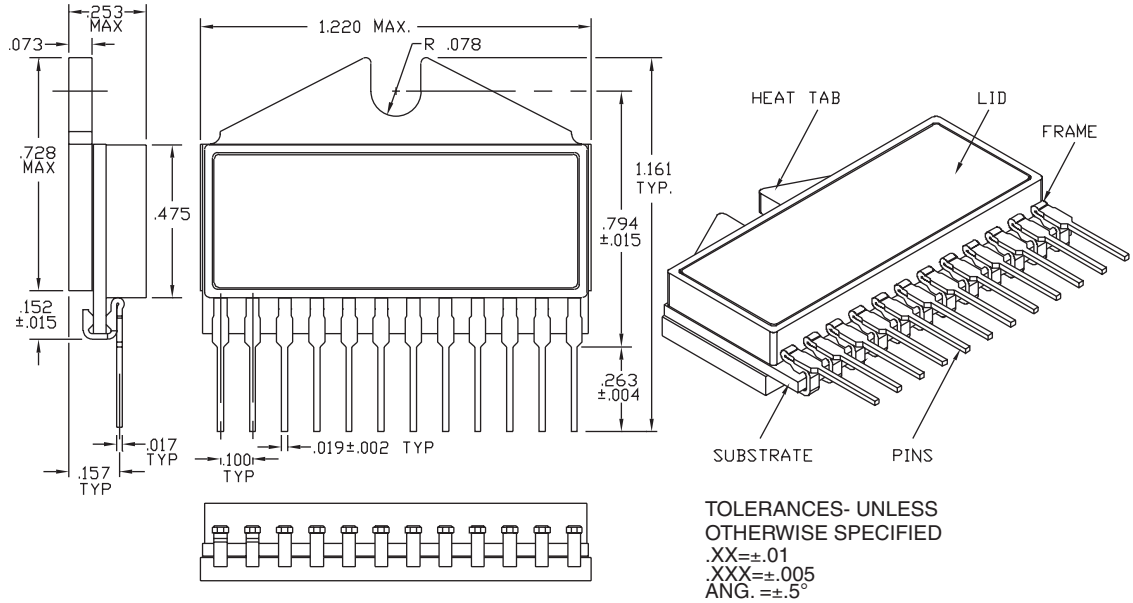
MECHANICAL SUGGESTIONS FOR POWERSIP SURFACE MOUNT PACKAGES

Apex Power SIP package is a single in-line package. Five different packages enter this SIP (Single In-line Package) Category.



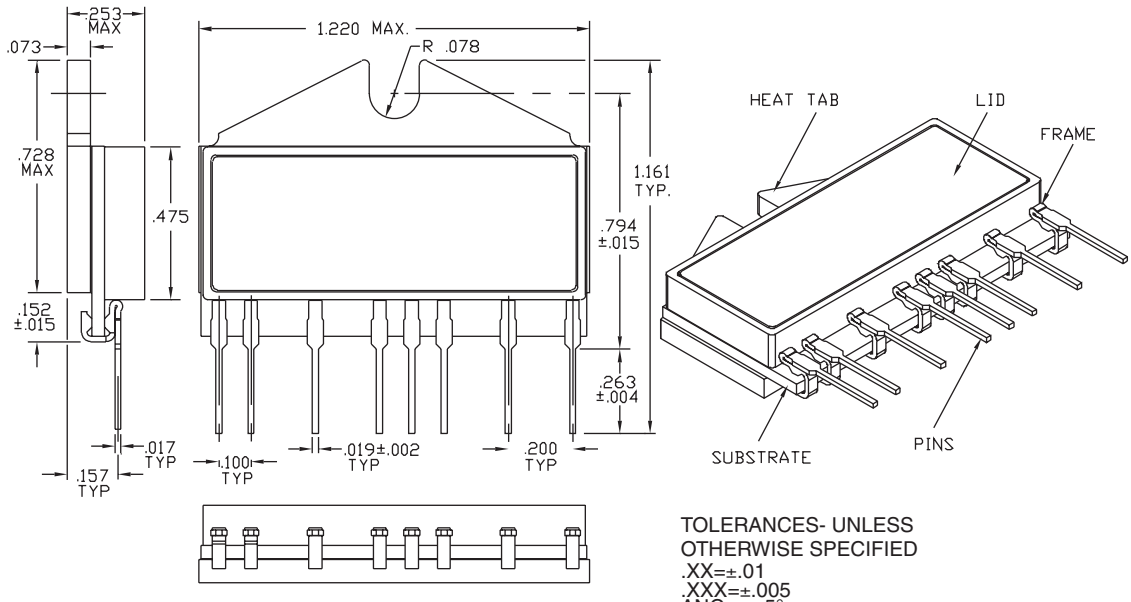
TOLERANCES- UNLESS OTHERWISE SPECIFIED
.XX=±.01
.XXX=±.005
ANG. =±.5°

SIP02



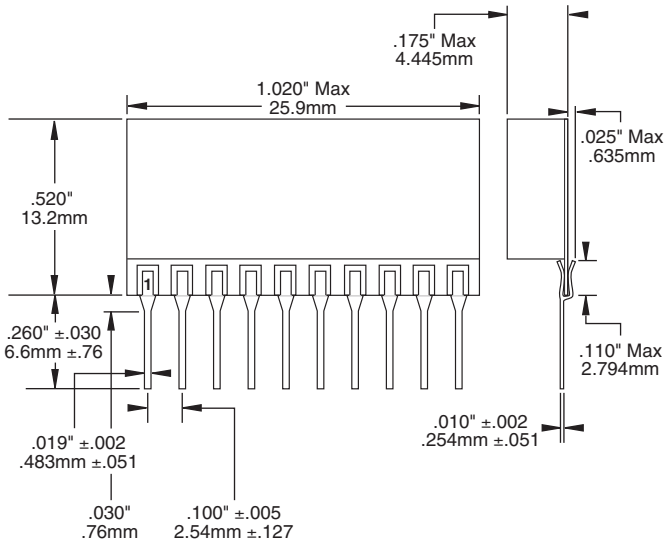
TOLERANCES- UNLESS OTHERWISE SPECIFIED
.XX=±.01
.XXX=±.005
ANG. =±.5°

SIP03

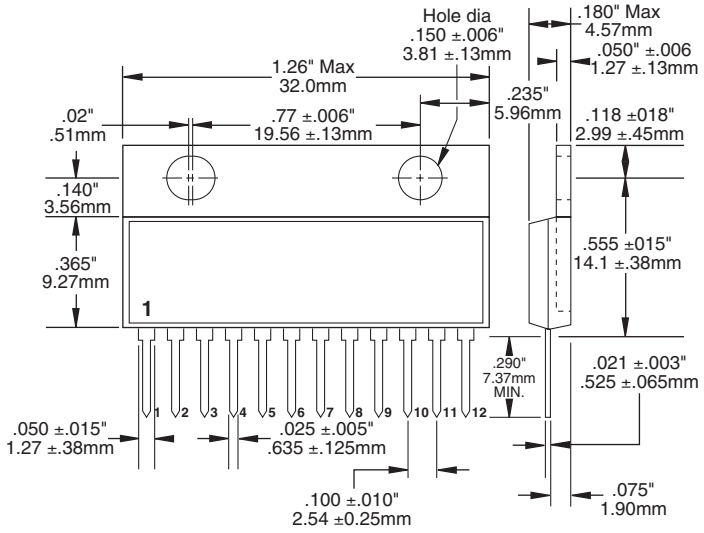


SIP04

TOLERANCES- UNLESS
OTHERWISE SPECIFIED
.XX=±.01
.XXX=±.005
ANG. =±.5°



SIP10

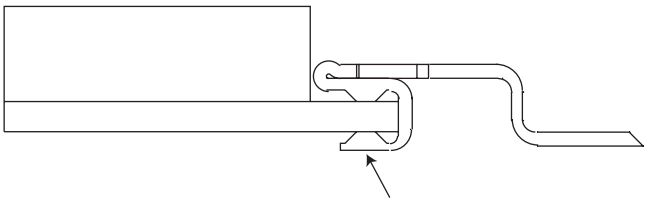


SIP12

G

All surface mount use of the SIP will require bending the leads. At this time Apex does not support bent leads options for SIP04 and SIP10.

SIP10 does not have any heat sink attached to the back of the substrate therefore limiting head dissipation. Mechanically, the absence of the heat sink would not allow to have it surface mount on its back. There is a potential short circuit between the leads.



Potential short circuit between leads

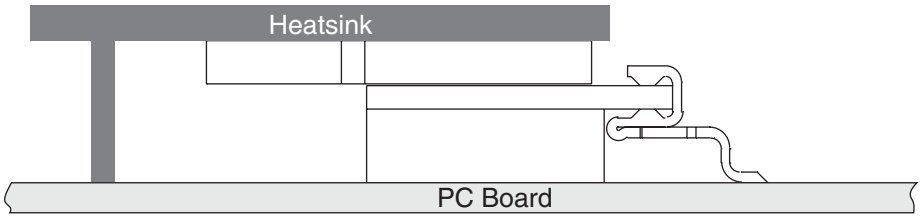
FIGURE 1.

SIP BENT LEAD CONFIGURATIONS BY PACKAGE

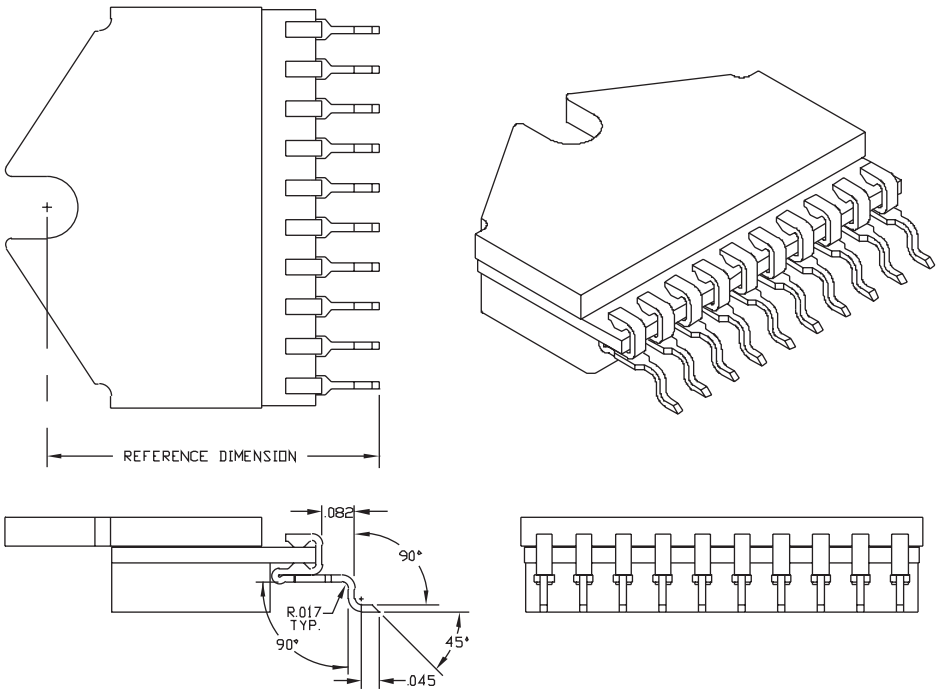
Model	Configuration
SIP02, SIP03	PAxx/LF001 or SAxx/LF001 PAxx/LF004 or SAxx/LF004
SIP12	PAxx/LF003 or SAxx/LF003

Note: No devices are kept in stock with bent leads. Please consult factory for availability.

SIP02, SIP03: DIFFERENT BENDING AND MOUNTING OPTIONS



CAUTION The heat sink has to be mechanically attached to the same PC board as the device, close to the device if possible. Not doing so may result in catastrophic failure.



NOTES:

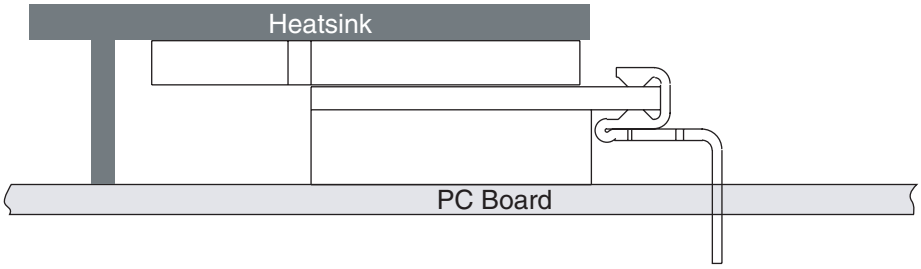
1. THIS LEAD FORM CAN BE APPLIED TO SIP02 AND SIP03 PACKAGES.
2. THE REFERENCE DIMENSION FOR EACH SIP PACKAGE IS AS FOLLOWS:

SIP02	SIP03
0.84	0.92

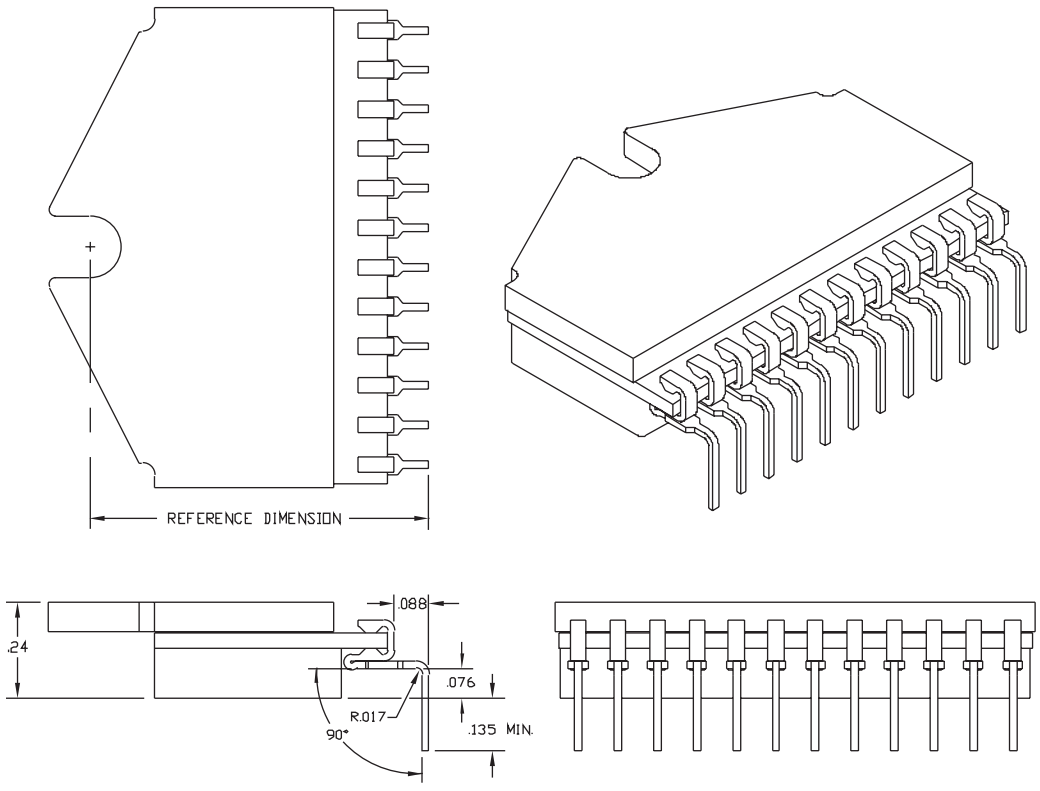
3. REFER TO SIP02 AND SIP03 OUTLINE DRAWINGS FOR OTHER PACKAGE DIMENSIONS.

LF001

SIP02, SIP03: DIFFERENT BENDING AND MOUNTING OPTIONS CONTINUED



CAUTION The heat sink has to be mechanically attached to the same PC board as the device, close to the device if possible. Not doing so may result in catastrophic failure.



NOTES:

1. THIS LEAD FORM CAN BE APPLIED TO SIP02 AND SIP03 PACKAGES.
2. THE REFERENCE DIMENSION FOR EACH SIP PACKAGE IS AS FOLLOWS:

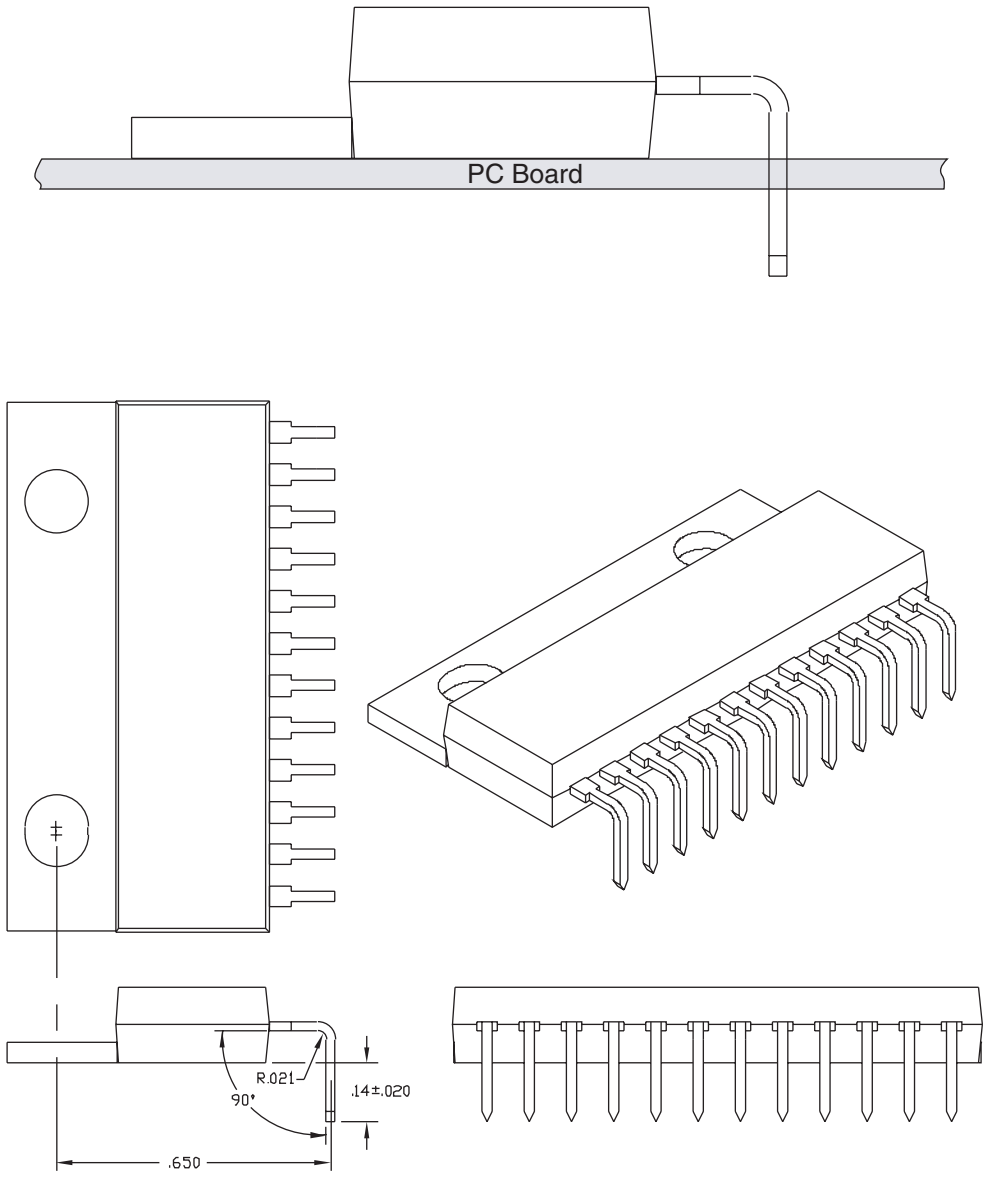
SIP02	SIP03
0.78	0.86

3. REFER TO SIP02 AND SIP03 OUTLINE DRAWINGS FOR OTHER PACKAGE DIMENSIONS.

LF004

G

SIP12: DIFFERENT BENDING AND MOUNTING OPTIONS



NOTES:

1. THIS LEAD FORM CAN BE APPLIED TO THE SIP12 PACKAGE.
2. REFER TO THE SIP12 OUTLINE DRAWING FOR OTHER PACKAGE DIMENSIONS.

LF003

APPLICATION NOTE 37

USING THE POWER DESIGN TOOL

1.0 INTRODUCTION

With the massive amounts of literature on the subject of power dissipation, one may question why any more time should be devoted to such a basic subject. Assume for a moment you have your favorite text book(s) in front of you. Your mission is to look up formulas to find heat both in the load and the driving amplifier. The chances are high that you will find yourself in several chapters before you find Ohm's Law (OK, forget that one), impedance, phase shift and power factor for reactive load elements and finally power dissipation in the amplifier. By now you probably have 10 to 20 formulas with at least three devoted to the amplifier.

Of the three amplifier related equations (typically DC, current-to-voltage phase angles less than 40°, and phase angles greater than 40°), only one may be required. Even the power amplifier data sheet is likely to present two separate thermal ratings for below or above 60Hz. With the proper equations selected and worked out in the right order, you have a wattage rating to apply to the next group of equations needed to select a heatsink. The sad part is that hours have passed.

By the way, did your research turn up a procedure for plotting load lines? This is especially important for bipolar transistor output amplifiers having second breakdown limitations which can be destructive even though a properly selected heatsink keeps the amplifier cool. On top of all this, text covering amplifier power dissipation presents classic circuits where one amplifier using dual symmetric supplies drives a load with respect to ground. This still leaves you on your own when it comes to bridge circuits, single supplies, highly reactive loads at very low frequencies or parallel amplifiers. Calculating power dissipation is anything but a basic subject.

If intuition or experience tells you it would be a major benefit to have one piece of software that remembers all the equations, can select the right ones and can apply them in the right order, then Apex's Power Design is a tool you need. It is a Spice alternative dedicated to the analysis of power dissipation and local loop stability of the most common power amplifier circuits. While written with hybrid power operational amplifiers in mind, it can be used with just about any power amplifier from multiple KW discrete monsters down to the monolithic world.

2.0 FASTER WAY TO MORE ACCURATE ANSWERS

The traditional power dissipation equations for amplifiers do not appear in any cell of Power Design. Calculations start by finding peak and RMS values of current, voltage and power (both apparent and true) in the load. For frequencies less than 60Hz, stress levels are picked off the load line plot. This procedure catches some stress levels that can slip by the traditional equations. The DC equation yields peak power levels, but assumes zero current-to-voltage phase shift. Both AC equations account for increased heating in the amplifier due to the phase shift, but yield only RMS power levels. Consider a 5Hz, 60° load where the frequency is too low to use RMS power, but the peak power is substantially more than identical currents and voltages in a purely resistive application.

Power Design next calculates power delivered to the amplifier from the power supplies. For frequencies at or above 60Hz, true power in the load is subtracted from delivered power to yield internal power dissipation. The key element here is knowing what signal amplitude corresponds to worst case power dissipation. A polynomial approximating worst case signal amplitude is used to eliminate the step function found when switching between the pair of traditional equations at the 40° mark.

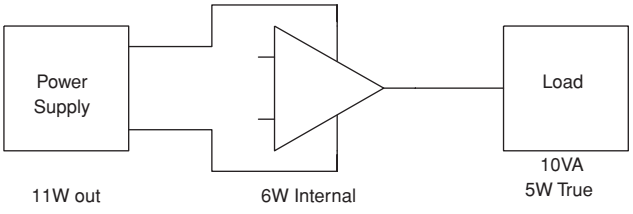


FIGURE 1. A SIMPLE VIEW OF WORK AND HEAT

3.0 THE CLASSIC AMPLIFIER

Figure 2 illustrates the most common power amplifier configuration and the one that relates directly to the traditional power dissipation equations. It is also the starting point for Power Design which will compute power levels for DC and sine wave signals.

All data entry cells in Power Design are yellow on the monitor (shaded in black and white as in Figure 3 shown on next page).

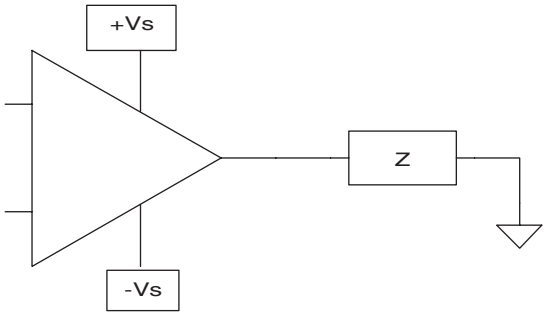


FIGURE 2. THE CLASSIC DUAL SYMMETRIC SUPPLY OP AMP DRIVING A GROUNDED LOAD

The data shown here will be used in the following example. In the top left, a pull-down entry of amplifier model reads an internal database containing enough specifications to flag operation outside the amplifier's capability and to calculate a heatsink rating. The data base contains all amplifiers manufactured by Apex and comments in the cells with red triangles tell users how to enter other data. This feature makes Power Design valuable to a very wide spectrum of engineers designing one ton rack mount systems down to monolithic users. Model data has no effect on calculation of load parameters. Going down, enter the supply voltage that will be assumed to be the magnitude of both positive and negative supplies. The next two cells specify minimum and maximum frequencies for the output signal. .001KHz will work fine for most DC applications. Next is magnitude of the output signal followed by a pull down entry labeled "Sig as ?". This is where those magnitude units are defined as volts, amps or watts with choices of peak, peak-to-peak or RMS. Yes, it's that easy to find what is needed to drive a 3.2 ohm speaker to 150W!

If your load can be modeled by one of the four simple diagrams keep going down, entering component values. Each load is computed independently so the previous entries other than the 15 ohms and 0.3mH of our current R-L load make no difference. If you have both an L and a C in your load and the resonant frequency is shown as lying between your min/max range, check the READ ME to see if you have a peak or a dip as far as internal power is concerned. If your load is more complicated, you will use the "Define" command button. More on this later. Just below the data entry cells, note the number of watts labeled "Piq". This is the standby power of the amplifier you entered as the Model when running on dual supplies of the value you specified. For hybrid op amps this will be the total quiescent current of the amplifier. For discrete designs, quiescent current would normally be set to the quiescent current of only the output transistors because the driver stages are not normally on the same heatsink as the output transistors.

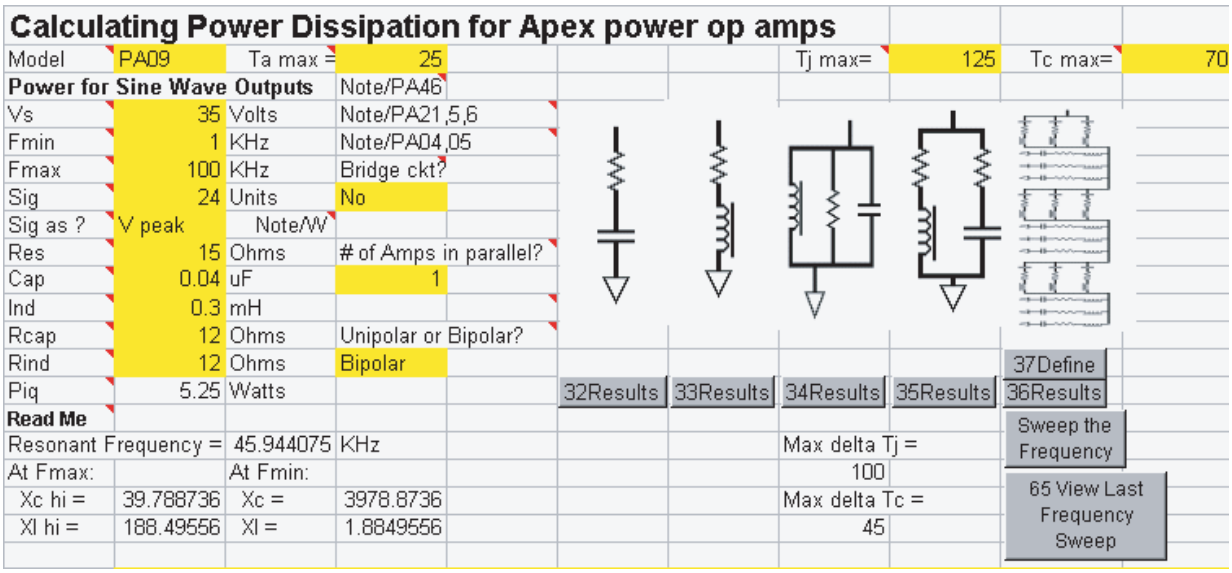


FIGURE 3. POWER DESIGN DATA INPUT SCREEN

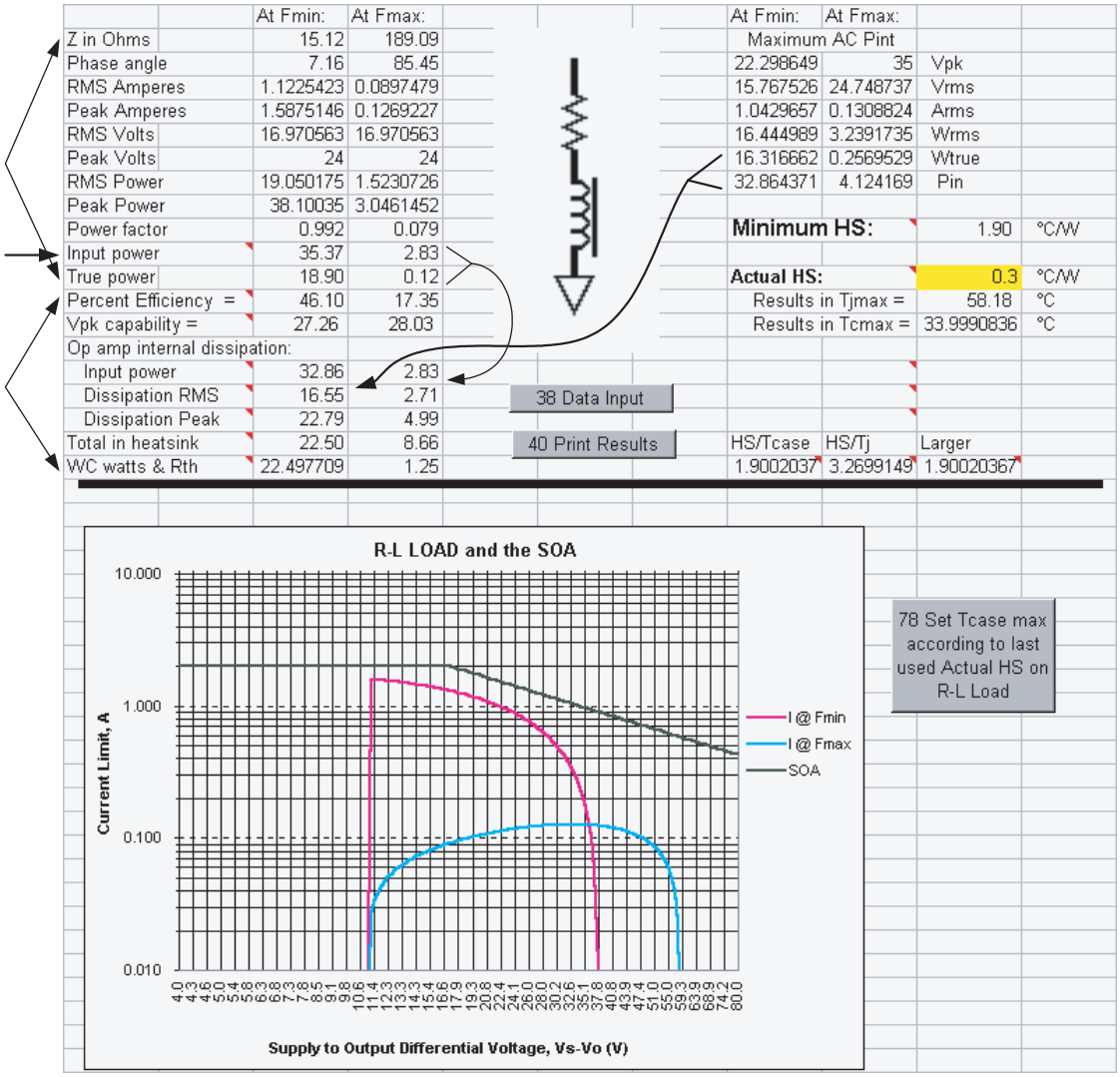


FIGURE 4. ALL THE POWER DATA

Selecting an Apex Heatsink See ACCESSORIES INFORMATION data sheet for specifications

Thermal Resistance	Package	Velocity Calculator:				Units of Measure:
1.96 °C/W	TO-3	15	CFM	2	Inch Width	English
	Update heatsink List	4	Inch Dia	3	Inch Length	
READ ME		171.8873	Ft/min	360	Ft/min	
		0.873198	M/sec	1.8288	M/sec	

Notes:

Beware: Flow rates change as you enter Thermal Resistance, but may be **wrong** until the Command Button is used!

Model	Fluid	Thermal resistance, free air, °C/W	Your rating requires FPM or GPM flow	Package(s) accepted	Style	Length, inches **or cm**	Width, inches **or cm**	Heigth, inches **or cm**	Weight, ounces **or grams**	Singles Price USD Domestic
HS02	Air	4.5	298.0982	TO-3	Cup	1.81	1.81	1.5	1.89	$16.85
HS03	Air	1.7	0	TO-3		3	4.75	1.25	5.6	$38.45
HS04	Air	0.95	0	TO-3		3	4.75	3	12	$74.85
HS05	Air	0.85	0	TO-3		5.5	4.75	2.63	18.3	$58.60
HS11	Air	0.68	0	TO-3,MO127		6	8	2	44.8	$214.80
HS11	H2O	0.68	0	TO-3,MO127		6	8	2	44.8	$214.80
HS13	Air	1.48	0	TO-3		5.5	4.81	1.312	13.9	$53.95
HS14	Air	2	100	TO-3		3	4.81	1.312	7.6	$33.95

FIGURE 5. HEATSINK SELECTION AND AIR VELOCITY CALCULATIONS

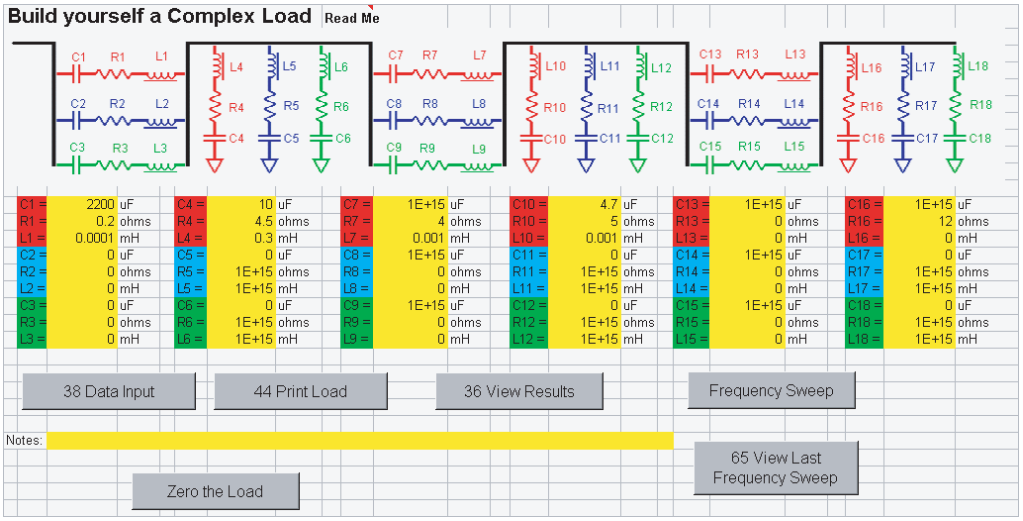


FIGURE 6. THE COMPLEX LOAD

Referring again to Figure 3, to the right of the signal magnitude entry cell is the pull-down bridge question cell. Make sure this cell contains "No". Below this is the cell specifying the number of amplifiers connected parallel. Make sure this cell contains "1". Below this, we need to specify "Bipolar" output current. From here, go up to enter the maximum ambient temperature your application will encounter. This is the starting point for the heatsink. To the right, enter the maximum junction temperature you wish to allow for the power transistors. 150° is acceptable for many commercial applications but in one respect transistors are just like cars: the hotter your run them, the shorter the life. Using lower temperatures should be considered when down time would be very costly. The last entry cell on this screen is that of maximum case temperature. In addition to life concerns, case temperature affects DC accuracy of the power op amp (check voltage offset and bias current drift) and often has significant affect on current limit values. In this example, a tight DC error budget mandates a maximum case temperature of 70°C.

To see power calculations use the "Results" button under the appropriate load diagram. The entire power data output is shown in Figure 4. Load lines based on voltage output from 90° to 270°. With purely resistive loads this produces one-quarter cycle of current output. With purely reactive loads one-half cycle of current is displayed. In this case the amplifier seems to be loafing at high frequency and is comfortably within SOA at low frequency.

The left side of both curves seems to indicate current drops to zero abruptly. This is not the electrical case, but is a function of Excel plotting routines. Note that at low frequency the load is mainly resistive (only ~7°) and the curve shows maximum current at minimum voltage stress across the conducting transistor (at the peak of the output voltage wave form). It drops to zero current (right end of the curve) at a stress voltage of just a little more than supply voltage or just a little after zero crossing of the output voltage. At high frequency, the load is mainly inductive (~85°) and peak current appears at a stress voltage approaching the supply voltage (near zero crossing of the output voltage). Current does not drop to zero until stress voltage is considerably more than supply voltage or until well after zero crossing of the output voltage. This explains why current drops better than 12:1 from low to high frequency but RMS internal dissipation drops only about 6:1 and peak drops less than 5:1.

This SOA graph is dynamic in that the constant power portion of the curve is drawn to meet the maximum case and junction temperatures you specified earlier. Data sheet graphs usually show one curve for a case temperature of 25°C plus others for elevated temperatures. All these curves assume maximum junction temperature as published in the product data sheet (up to 200°C on some bipolar transistors) but this is not in the best interest of long-term reliability. Power Design draws only one constant power line according to the case and junction temperatures you specify. If you assign an actual heatsink more generous than the minimum for the application, the constant power curve will be artificially low until you use the "Set Tcase max according to last used Actual HS on..." button.

For details on the load, refer to upper left block of numbers. Just about all the electrical information you could want is detailed. Mixed in here is a line showing power delivered to the amplifier by the power supply (except for quiescent current). "Percent Efficiency =" is based on watts drawn from the supply (including quiescent) and VA delivered to the load. It does not include power factor of the load. "Vpk Capability" is supply voltage minus an estimate of the saturation voltage of the power amplifier at the peak load current.

Turn your attention to the upper right hand corner where the first line of numbers indicate the peak output voltage producing the maximum internal power dissipation. Below this are results of power calculations at these worst case signal levels. The bottom two are the most important:, true watts in the load and power delivered to the amplifier. At low frequency signals, peak internal power dissipation is at about 22.3Vpk, less than the maximum signal amplitude specified earlier. The Power Design assumes real signal amplitude does vary and the amplifier must be able to survive the lower signal level.

The 32.86W is then used on the left (long arrow) as well as the 16.31 true watts that is subtracted from input power to yield "Dissipation RMS" of 16.55W. "Dissipation Peak" is higher than the RMS value but is

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ignored because minimum frequency is well above 60Hz in this case. "Total in the heatsink" at low frequency is the addition of the 16.55W RMS and 5.25W calculated for quiescent earlier.

The same calculations are repeated for maximum frequency. In this case the very high phase angle demands the amplifier swing all the way to the supply rail (35V) to experience worst case internal heating. As our maximum signal amplitude is less, the input power (short arrow) and true load power are used from the user specified signal amplitude. Again, RMS and quiescent powers are added to find the heatsink total at maximum frequency (peak values are ignored). The last line picks the higher power level of the two frequencies and displays the DC thermal resistance if the frequency is below 60Hz or the AC thermal resistance.

To the right with bold face heading we find the minimum heatsink rating for this application. Your job is to find or design a heatsink and enter its actual thermal rating. Entering the 1.7°C/W rating causes display of case and junction temperatures for the amplifier. A little below this area are the actual calculations which include thermal interface resistance between the amplifier and the heatsink. Separate calculations are made to insure both case and junction limitations are met. In this example, case temperature is the limiting factor. If the heatsink had been sized according to junction temperature only, the case would have been running about 97°, outside the guaranteed performance range for drift with the commercial part.

In this general area you may also find up to three warning flags. The most common warning is for excessive temperatures. The other two warnings will pop up if your application is demanding more voltage or current output than the amplifier is specified to deliver. The voltage calculation takes into consideration the supply voltage and the output saturation characteristics of the amplifier.

If you're asking what's so magic about 1.7°C/W, refer to Figure 5 where an Apex heatsink can be selected. To use this sheet, simply enter the desired heatsink rating and package type, then click on the command button. Even though our example used the HS03 without a fan, note that an HS02 inside a 2"x3" duct fed with a 15CFM fan would be more than adequate to produce the required thermal rating.

4.0 USING THE COMPLEX LOAD

Using the load shown in Figure 6 requires complex numbers which most Excel users do not automatically activate. You will probably need to use Tools, Add-Ins and Analysis ToolPak. Unless you have known good data already entered, use the "Zero the Load" button to place extremely high impedance components in all the vertical strings with a ground connection and extremely low impedance components in the horizontal strings.

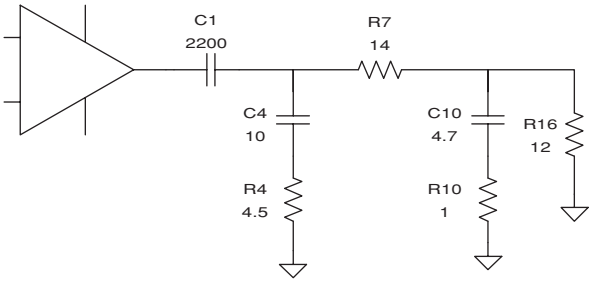


FIGURE 7. A SAMPLE COMPLEX LOAD (PARASITICS NOT SHOWN)

Refer to the sample load diagram in Figure 7 to illustrate data entry. Let's start on the left at the amplifier connection. Use any one of the three strings for the capacitor. Note that we are also entering values for ESR and ESL for the capacitor. These may be found on the data sheet or measured with an impedance analyzer. R1 is used to model ESR of the 2200uF capacitor and L1 to model ESL. It is important to open the other two unused strings in parallel with our component model. The easiest way to achieve this is entering zero capacitance in each string. Our second group of components could again use any of the three strings with a ground termination. The resistor is actually a coil and parasitic inductance is also entered. Proceed through groups of components until finished.

After entering your load data, the "View Results" button will show performance at the minimum and maximum frequencies. To see what's happening in between, press the "Frequency Sweep" button. Figure 8 illustrates typical results of a sweep. This specific load shows the need to analyze carefully in the low KHz area.

Setting the min/max frequencies to 2/4KHz and re-running the sweep as shown in Figure 9 will allow a more precise determination of the peak values for current output and internal power dissipation. Notice that peaks and dips do NOT coincide exactly. In this case set Fmin to 2.54KHz and Fmax to 2.84KHz and click "View Results" to see maximums in numerical form and select the heatsink rating.

5.0 NORMAL BRIDGE CIRCUITS ARE EASY

The master/slave approach shown in Figure 10 is an easy way to implement a bridge circuit. The master maybe be configured any way desired. The job of the slave is to invert the master's output such that the load is driven equally but opposite at its two terminals. The schematic suggests calculating internal power dissipation might be tricky, but not so when using Power Design. Enter signal amplitude applied to the total load, enter the total load components, enter "Yes" for the bridge question and all the modeling is taken care of automatically. Load impedance shown will be the total value, currents are for load and each amplifier. Voltages, wattages and heatsink ratings are for a single amplifier and are flagged as such.

6.0 SINGLE OR NON-SYMMETRIC SUPPLY BRIDGES REQUIRE A TRICK

The circuit shown in Figure 11 is often used to achieve bi-directional drive on a single supply or to double voltage swing capability when a single higher voltage amplifier is not cost effective or does not exist. To easily accommodate ground referenced small signal driver circuits, a small negative supply is often used to overcome common mode voltage restrictions.

Note that zero drive to the load requires both amplifier outputs to be equal to that of the voltage divider (two equal resistors). This forces the center of the load to be constant and at 50% of a true single supply or centered between the two supply voltages. If one algebraically subtracted the correct voltage from both the positive and negative supply pins of the amplifiers and the lower divider termination, you would end up with operation identical to the symmetric supply bridge of Figure 10.

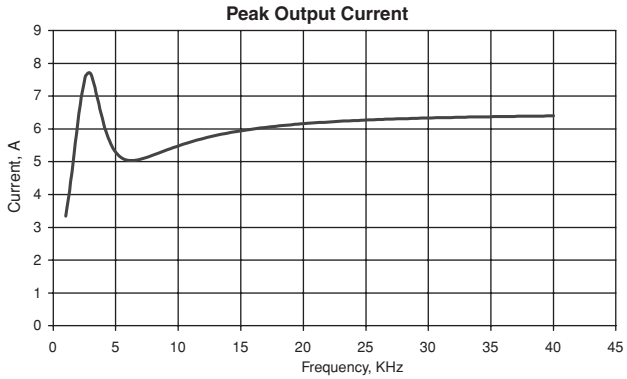
For Power Design to analyze this circuit, enter a supply voltage equal to half the single supply or half the sum of the absolute values of both supplies. For 110V single supply, enter 55V. If an opposite polarity supply of 10V is added, enter 60V.

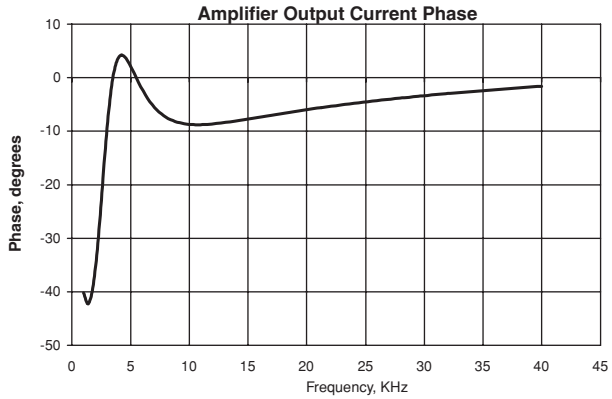
7.0 BIAS LEVELS ON AC ONLY LOADS

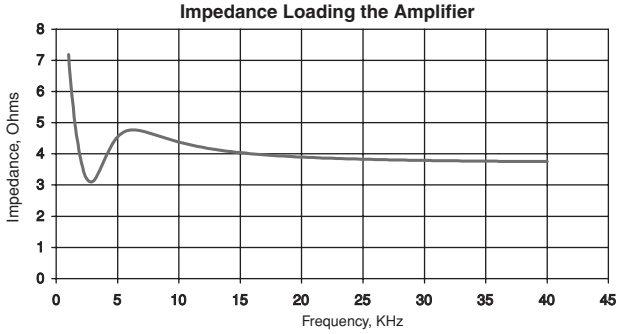
There are two bias voltages to determine with AC only loads; one affects internal power dissipation, the other does not. Refer to Figure 12, noting that neither bias level affects output current. The DC blocking property of the load capacitance means current demand is a function of only the load impedance and the applied AC signal. DC bias levels can be ignored, even if they result from the load being terminated at one of the amplifier power supplies or a separate supply. While constant load bias has no affect on internal power dissipation, output bias directly affects voltage across the conducting transistor and therefore power levels. Power Design always assumes output bias is zero meaning equal power dissipation in both transistors.

Given a requirement to drive a capacitive load at 7.07VAC riding on 100VDC, the least expensive op amp solution would be a 100V reference supply and a low voltage op amp. The catch is that this reference supply must sink and source current. If using an output filter capacitor 10 to 100 times the value of the Cload is acceptable, this type solution is likely to be lower cost overall. Remember that if these two capacitance values are constant, the resulting drive voltage errors due to the non-zero impedance of the reference supply can be compensated by increasing the drive signal.

Refer to TABLE 1 for a way to approximate power levels given the following assumption: +120V and -10V will be used to accommodate voltage saturation on the high side and common mode voltage on the low side. Calculate voltage stresses on each transistor from mid point of the sine wave to each supply. In this case, 20V to the positive supply and 110V to the negative supply. Run two calculations using







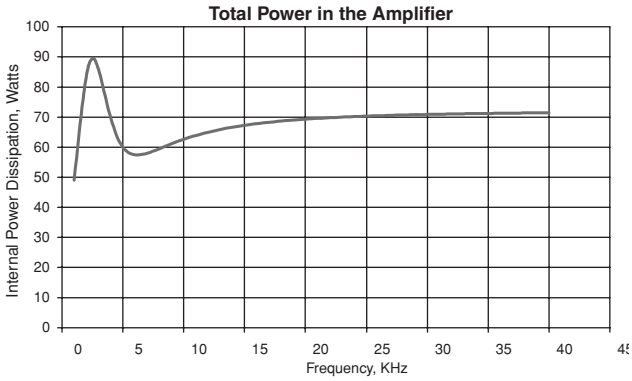
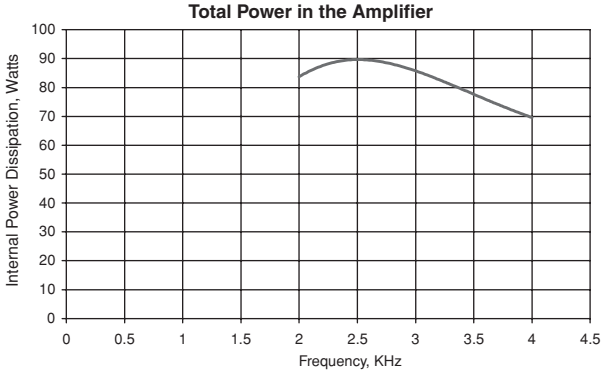


FIGURE 8. GRAPHS RESULTING FROM A FREQUENCY SWEEP



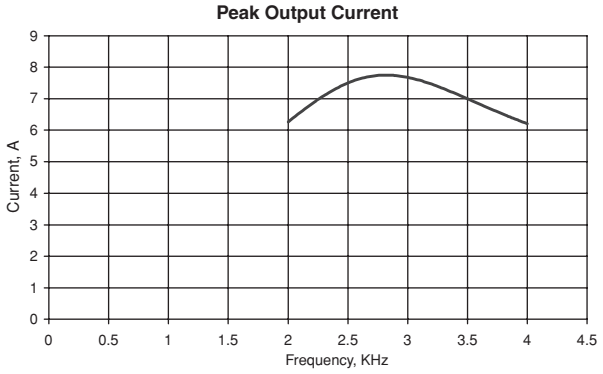


FIGURE 9. ZEROING IN ON THE PEAK VALUES OF A COMPLEX LOAD

each of these values. Select an arbitrarily large initial heatsink value. The numbers in TABLE 1 are a result of a PA88 driving 15 ohms and 0.04uF at 40kHz with Ta=25°, Tc max=70 and the actual heatsink 1.7°C/W. Subtract case temperatures from junction temperatures to find temerature rise. The 110V data tells us the hardest working transistor is 35.5° above case temperature. The 20V data tells us the other transistor is only 6.2° above case temperature. Now set supply voltage to 65V (the average of 110 and 20) to find a minimum heatsink rating of 10.3 °C/W is required. Enter an actual heatsink rating, such as 4.5°C/W corresponding to an Apex HS02 with no fan. To find a case temperature of 44.8°C add to this the previously calculated temperature rises. To find the output transistors junction temperatures of 80.3° and 51°C. Iterate the last step if this is too hot.

Vs	Tj	Tc	Delta	Heatsink
110	73.2	38.2	35.5	6.1
20	33.5	27.3	6.2	

TABLE 1. MULTIPLE PASS METHOD OF DETERMINING TEMPERATURE WITH DC BIAS ON A CLOAD

8.0 TECHNIQUES FOR PARALLEL OPERATION

Calculation methods for parallel operation of power amplifiers is simple; however, getting two or more power amplifiers to cooperate rather than kill each other is often quite another matter. Power Design assumes all the precautions of Apex Applications Note 26 PARALLEL CONNNECTION or some other authoritative reference have been followed. Potentially destructive currents between amplifiers are NOT modeled. Causes of these currents include voltage offset, common mode errors and violations, phase shift, and current limit sequence errors. If you have overcome all these, refer to Figure 13 for the most common approach to parallel operation along with a way to think about an equivalent load for the single amplifier.

To use Power Design for parallel operation, enter the number of amplifiers in parallel in the yellow cell below the bridge question. Total values are then calculated for the load results area and scaled by the number of amplifiers for the SOA graph and amplifier internal power dissipation results. The heatsink rating will then need to be applied to each amplifier.

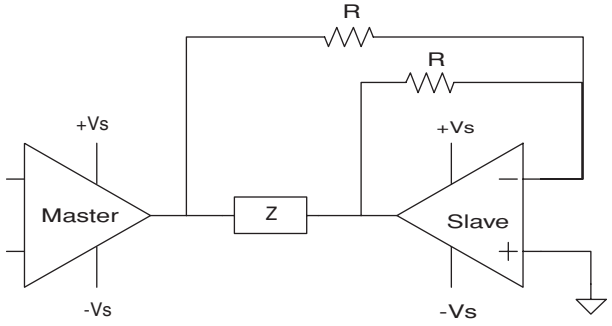


FIGURE 10. THE MOST COMMON METHOD USED TO IMPLEMENT A BRIDGE CIRCUIT

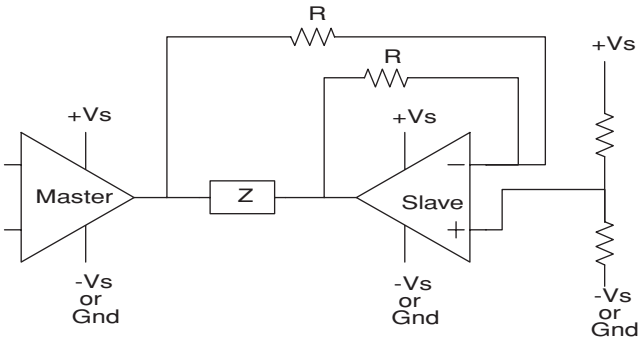


FIGURE 11. THE CLASSIC NON-SYMMETRIC BRIDGE CIRCUIT

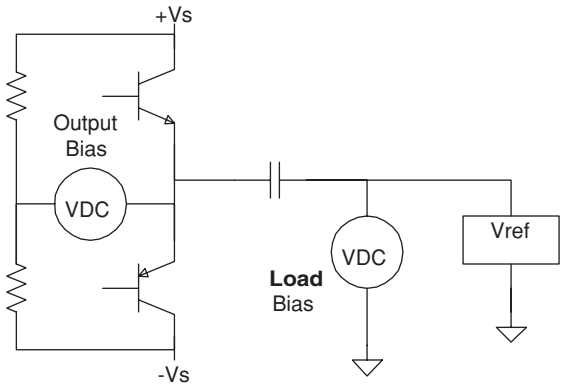


FIGURE 12. BIAS LEVELS FOR AC ONLY LOADS

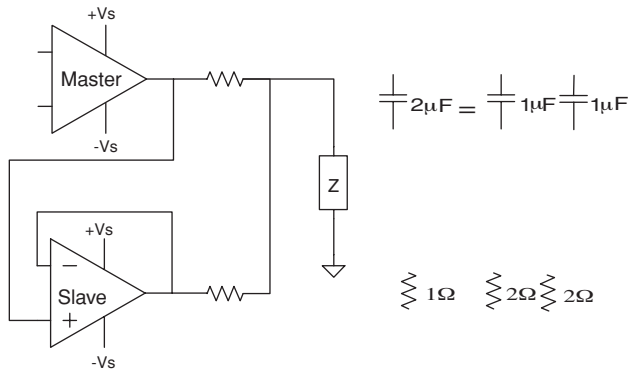


FIGURE 13. A COMMON PARALLEL CIRCUIT AND CIRCUIT ALGEBRA TO MODEL A SINGLE AMPLIFIER'S LOAD CURRENT

9.0 UNIPOLAR OUTPUT CURRENT

Programmable Power Supplies (PPS), Thermo-Electric Coolers (TEC) and heaters are often configured for current of only one polarity. This means only one output transistor is doing the work and therefore the DC thermal resistance specification of the amplifier must be used even if the signal frequency is quite high. Most op amp data sheets footnote the AC rating as applying if current alternates between the two output transistors are at a rate greater than 60Hz. The mechanism yielding an improved AC rating is simply a larger square area of the package materials used to conduct heat when two transistors are active.

All the previous examples assumed output current was bipolar. In cell D13 (under the parallel question), you can enter “Unipolar” to force all heatsink calculations to be based on DC thermal resistance and change the quiescent power calculation to reflect the supply voltage you entered as being a true single supply, plus change the supply problem flag.

A word of caution is in order here. Many loads will demand bipolar current even though the voltage is uni-polar. The easiest to visualize is the capacitive load: current flow is determined only by rate of change and direction of change. Both positive and negative direction changes can be achieved without changing polarity. A good rule of thumb is to not use this feature if the phase angle for your load is greater than 10°.

If your application uses a low voltage supply opposite a high voltage supply which is doing all the work, enter the high voltage supply ignoring the low one. This will result in an error in quiescent power by a factor of Iq*Vs low (usually negligible).

Returning to our classic example with the PA09, reducing the maximum frequency to 1.2KHz and setting cell D13 to “Uni-polar” results in data shown in Figure 14. The frequency change keeps us within the 10° limit. Note that neither peak nor RMS power dissipation has changed but total in the heatsink has come down 2.63W. This change is due to total supply voltage being reduced by 35V. Thermal resistance used has jumped from 1.25°C/W (AC rating) to 1.6 (DC rating). Just as before, the limitation of this application is case temperature rather than junction temperature. It is interesting to note that the same heatsink now produces a case temperature about 5° lower but the increased thermal resistance produces junction temperature only 1° lower.

10.0 A LITTLE ‘WHAT IF?” GAME

You have a PA12A rated at +/-50V, 15A, 125°C case, 200°C junction. It can drive to within 5V of the rail at 5A and to within 6V at 15A. How much power can be delivered when mounted on a 0.5°C/W heatsink?

The first correct answer is: “that depends”. Start with a sine wave driving a 225 ohm pure resistor which will be voltage limited. We need no help on this one; 45V peak output will drive .2Apk or 9W peak or 4.5W RMS. Yes, a ridiculous job for the PA12A but it shows the importance of impedance matching. Set up the PA12A as above, set the signal to 44Vpk and define the load as 4.4 ohms (0mH). This would be 10Apk, 440W peak and 220W RMS. Can it be done? Still “depends”. If you have a frequency below 60Hz, no; if not, we are just barely over the limit. Assume we must operate below 60Hz. What can we do? Lower the peak output voltage and the supply voltage by equal amounts until the TOO HOT flag goes away. Did you arrive at something like 120W RMS and 240W peak?

Change the rules just a bit; stay below 60Hz, but you may vary the load resistor to achieve maximum output power. High power demands high efficiency which means saturation voltage loss (a relatively constant value) must be small compared to output voltage. This means maximum supplies and signal level should be used. Now enter increasing values of load resistance until the TOO HOT flag goes away. Did you get something like 7.35 ohms, 132W RMS and 263W peak?

This time I have looked up the specs on a high quality woofer: 8 ohms nominal impedance, 5.9 ohms resistive, 0.93mH inductance, 40Hz to 4KHz usable frequency range. The amplifier is too hot at maximum supply and signal levels, so bring them both down. How does 122W RMS at 40Hz but only 30W at 4KHz sound?

One last item: The circuit will use -5V and +95V, resistive load at DC. You tell me the rest of the story.

Uni-polar Current	At Fmin:	At Fmax:		At Fmin:	At Fmax:		
Z in Ohms	15.12	15.17		Maximum AC Pint			
Phase angle	7.16	8.58		22.298649	22.377096	Vpk	
RMS Amperes	1.1225423	1.1187227		15.767526	15.822997	Vrms	
Peak Amperes	1.5875146	1.5821128		1.0429657	1.0430736	Arms	
RMS Volts	16.970563	16.970563		16.444989	16.50455	Wrms	
Peak Volts	24	24		16.316662	16.320037	Wtrue	
RMS Power	19.050175	18.985354		32.864371	32.86777	Pin	
Peak Power	38.10035	37.970708					
Power factor	0.992	0.989		**Minimum HS:**		2.25	°C/W
Input power	35.37	35.25					
True power	18.90	18.77		**Actual HS:**		1.7	°C/W
Percent Efficiency =	50.14	50.12		Results in Tjmax =		88.23	°C
Vpk capability =	27.26	27.26		Results in Tcmax =		59.5109188	°C
Op amp internal dissipation:							
Input power	32.86	32.87					
Dissipation RMS	16.55	16.55	38 Data Input				
Dissipation Peak	22.79	23.24					
Total in heatsink	19.17	19.17	40 Print Results	HS/Tcase	HS/Tj	Larger	
WC watts & Rth	19.172733	1.6		2.2470833	3.6179691	2.24708327	

FIGURE 14. OUR CLASSIC EXAMPLE TURNED INTO A UNI-POLAR CURRENT OUTPUT AMPLIFIER

11.0 CONCLUSION

The Apex Power Design Tool automates examination of sine wave power levels of both the load and the power amplifier. Gone is the need to remember or look up multiple formulas or even decide which ones to use. With almost instant plotting of load lines with plenty of resolution, the tendency to scrimp on this part of power design is eliminated. With frequency sweep capability, sweet points or hot spots of complex loads can be quickly located. While aimed at and containing a database of power amplifiers from Apex Microtechnology, this tool is usable for just about any power amplifier application. It is available free of charge at www.apexmicrotech.com.

Please remember that answers to perfect calculations are only as accurate as the input data and assumptions they are based on. Do not let the bad news of poor assumptions ruin your day. Here are some things to consider: How good is the power supply regulation? Does load impedance change with temperature, current, voltage or mechanical loading? How well were all the parasitic values nailed down? What is the phase margin of the circuit? What is the reduction in airflow due to backpressure?

There is still no excuse to skip measurement of operating temperatures on your equipment under worst case operating conditions. With Power Design, these measurements are more likely to say “Job well done!” than “Oops”.

PS. About 303W (SOA graph will be fine when case temp is set to 77.5°C).

Other Application Notes in this “Power Design Tool” series are: Application Note 38: Loop Stability With Reactive Loads Application Note 39: Filters & Power Dissipation for PWMs

APPLICATION NOTE 38

USING THE POWER DESIGN TOOL

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

One definition of an oscillator: A circuit with gain and a total phase shift of 360*. Usually 180° comes from the ideal amplifier being inverting. The remaining shift comes from feedback elements and the non-ideal portion of the amplifier.

A second definition of an oscillator: A circuit the power amplifier designer has nightmares about.

If you are looking for a l o n g and b o r i n g Application Note with lots of formulas you no longer remember how to deal with, this is not the document for you. This article works in conjunction with the Apex Power Design CAD tool to remember and apply correctly all the rules and formulas, thus allowing concentration on the big picture. As a toddler, you probably had toys that gave you the "feel" that square pegs do not fit in round holes. The objective here is to give you a "feel" for what curve to bend in which direction allowing you to slay the evil dragon of power amplifiers, the oscillator.

WHY THE DRAGON APPEARS

By far and away, the most common cause of oscillation is lack of adequate supply bypassing! This is often true even of circuits having hundreds or even thousands of microfarads of bypass. It is all too easy to forget details such as:

1. The amplifier has gain into the MHz range even when used at DC.
2. In the MHz range, some capacitors have significant inductive reactance.
3. Even a straight piece of wire has inductance.
4. Resistance of PC traces and even wire makes a difference in power circuits.

Bypassing supplies for a power amplifier is such a broadband job that it often requires multiple sets of components and demands proper placement of each set. For the high frequency spectrum (this includes the frequency where the amplifier runs out of gain) the use of small value ceramic capacitors placed right at the pins of the amplifier is required. In the range of the signal frequency, capacitors will be larger in value and physical size so they will be further from the supply pins of the amplifier. Relying on the output capacitors of the power supply may be acceptable, but not if they are multiple feet from the amplifier.

The second most common cause of oscillation is the elusive ground loop. Refer to Figure 1 for an over-simplified picture of the problem. Load currents flowing through the parasitic impedances in the line back to the supply, develop voltages which are inserted as positive feedback. To break the loop, designate one physical point as the center of a star ground. Make sure every connection to ground has its own path to the center of the star. Do not forget the low side of the bypass capacitors. The best news about this problem is that the frequency of oscillation usually points to the cause by being right at the unity gain frequency of the amplifier.

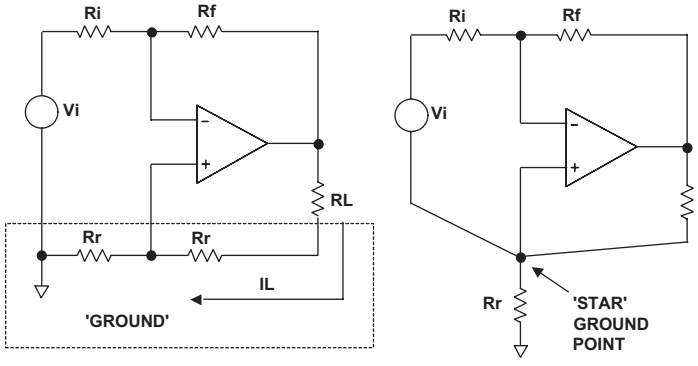


FIGURE 1. GROUND LOOPS AND THEIR SOLUTIONS SIMPLIFIED

The least common cause of oscillation is related to design of the output stage of the amplifier itself and also raises a flag to identify itself. If the oscillation is above the unity gain frequency of the overall amplifier (below 0db on the bode plot), we have a local feedback problem in the output stage. First, check supply bypass. Then try a snubber network (series R-C connected from the output to ground) in the range of 1 to 10 ohms and 0.1 to 1uF.

What about exceeding the capacitive load specification that appears on most op amp data sheets? This refers to Cload with the amplifier connected in a unity gain configuration. We will examine means to circumvent this limitation.

THE GROUND RULES DEFINING THE PLAYING FIELD

With the above out of the way, we can attack the real subject of this article-taming oscillations caused by the non-ideal characteristics of the amplifier and feedback elements. A few more definitions are in order:

Closed loop response is the relationship between the input and output signals of the total amplifier (including feedback). We will be looking at both the gain and the phase of this response.

Open loop response is the relationship between the input and output signals of the amplifier without feedback. This response does not go away when we close the loop. It is still the input to output pin relationship and it does affect closed loop response.

Loop gain is the difference between the open and closed loop gains. This is the magic of op amps allowing overall circuit function to be primarily a function of feedback elements. It allows an op amp to be a general purpose building block. More loop gain means the circuit will be more faithful to the ideal closed loop response.

Beta is the fraction of the output signal fed back to the negative input of the op amp. We refer more often to the reciprocal which is closely related to inverting signal gain. It is imperative to note that stability analysis is treated as a non-inverting circuit, just as when calculating the effects of voltage offset on the output signal. This means gain, or 1/beta can never go below one or 0db.

Intersection rate is the slope difference between the open and closed loop roll-off at the point where they cross.

Closure frequency is the frequency where open loop gain is 0db. Above this frequency the circuit can not meet the definition of an oscillator.

Phase margin is the difference between the 360°of the oscillator definition and the phase shift of the total circuit at closure frequency. In practical circuits, it is recommended that all frequencies below closure be examined as well. Note also that by using negative feedback to close the loop we have the first 180° of phase shift needed to oscillate simply from the inverting function of the op amp. The phase plots you will see do not reflect the inversion, only the change over frequency. This further means that on all the phase plots to follow, phase margin will be the difference between the curve and 180°.

Phase margin is the buffer zone between the power amplifier and the power oscillator. 45° is desirable, more is better, never accept less than 30.

Straight line approximation is the technique used to plot most of the response curves to follow. While real performance would be represented by smooth curves, the straight segments make it much easier to pinpoint corner frequencies. The penalty in terms of phase accuracy is +/-6°.

SNAP SHOT OF A CLASSIC AMPLIFIER POWER DESIGN MECHANICS

The data entry screen of the Cload sheet is shown in Figure 2. Yellow cells are for data entry and their labels correspond to component labels of the schematic. Entering actual, extremely high or zero values can model the most common stabilization techniques. Comment cells will instruct you how to enter data for

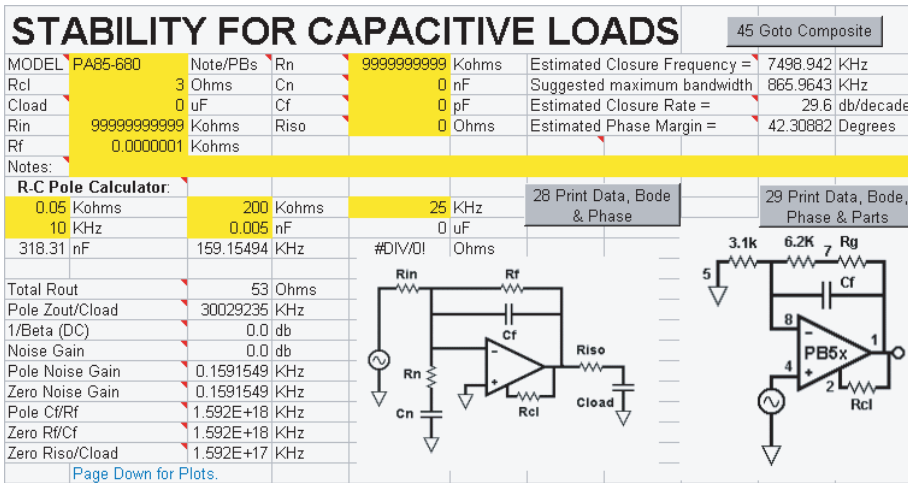


FIGURE 2. DATA ENTRY FOR CLOAD ANALYSIS

Notice the first smooth curves in the Phase Shift Graph.The right most curve plots the closed loop phase shift of the complete circuit. For example, phase shift at 40KHz is about 7°. For those times when phase shift at lower frequencies is of interest, factors of 10, 100 and 1000 scale the other three curves. Phase shift at 400Hz would be about 0.007°.

In the upper right corner of Figure 2, are some answers that illustrate what this whole exercise is about. The most important answer is phase margin where we like to see 45*. Closure (intersection) rate is a key indicator of health, where 20 is the desired number. The number is usually a multiple of 20 but as you see here, when the intersection and a corner frequency are nearly coincident, it may fall in between. The suggested maximum bandwidth is the frequency where loop gain is down to 20db. This is very much a judgement call and will be application dependent. Remember the basic op amp theory where various internal errors are reduced by the loop gain when the circuit is closed. For example, open loop output impedance (affecting gain accuracy) of 10 ohms would be a killer with a 1A output. If the circuit has 40db of loop gain, this error drops from 10V to 0.1V. Demanding this 40db would reduce the suggested maximum bandwidth by a decade.

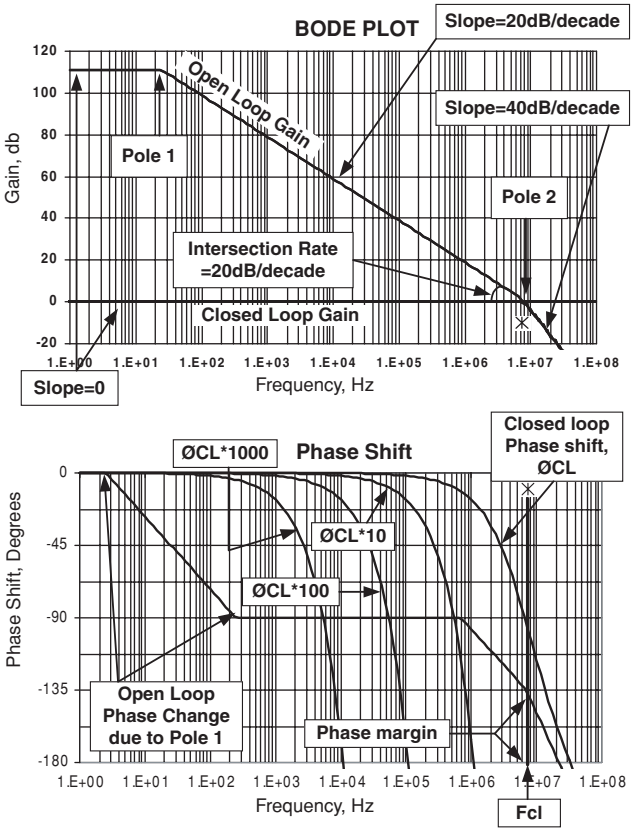


FIGURE 3. UNITY GAIN STABLE AMPLIFIER CURVES

your own operational amplifier, but Apex hopes you will use the pull down to select one of theirs from the built-in data base. The first thing Power Design should be able to do is duplicate the small signal response (or bode plot) and the open loop phase response of the given amplifier.

For amplifier models featuring external compensation, Power Design uses a three digit suffix to specify compensation capacitor values detailed on the product data sheet. The Rcl entry allows entry of the current limit setting used with most power amplifiers. Enter the remaining circuit values according to your application. Setting up the PA85 (compensated for unity gain) as a unity gain buffer (Rin=very high, Rf=very low) will produce the graphs shown in Figure 3. Open loop response should duplicate what is shown in the data sheet, or measured values of your own amplifier.

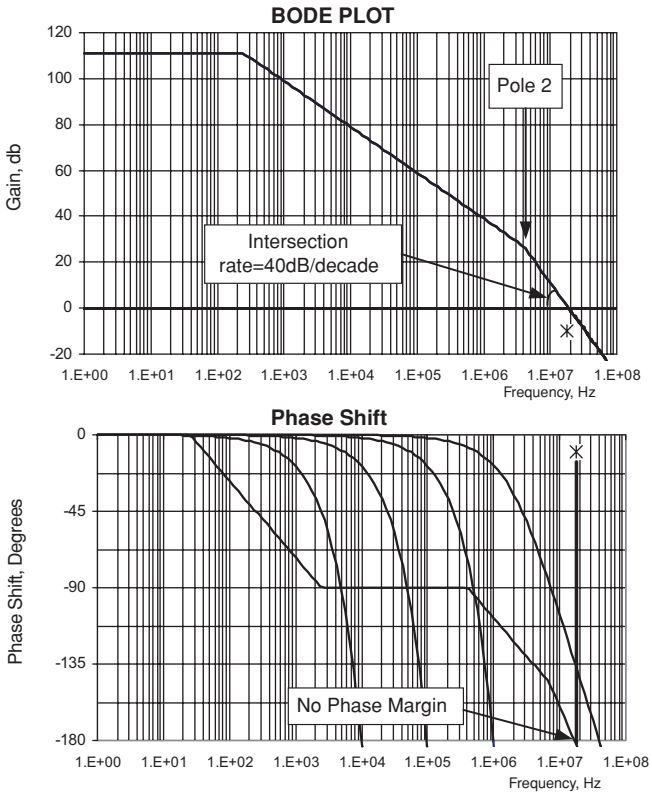


FIGURE 4. ATTEMPTING TO USE AN AMPLIFIER BELOW SPECIFIED MINIMUM GAIN

The unity gain stable op amp will have its first pole at a low frequency and the second pole will not appear until open loop gain has crossed 0db. The horizontal line at 0db indicates closed loop unity gain operation. Notice that pole 1 of the open loop response is at roughly 25Hz, that phase started moving a decade before this and within 2 decades has moved 90*. We find the second pole at about 7MHz and again phase starts moving a decade before. While the third pole does not show on the bode plot, a corner in the phase plot around 7MHz tells us pole 3 is near 70MHz. The main point of

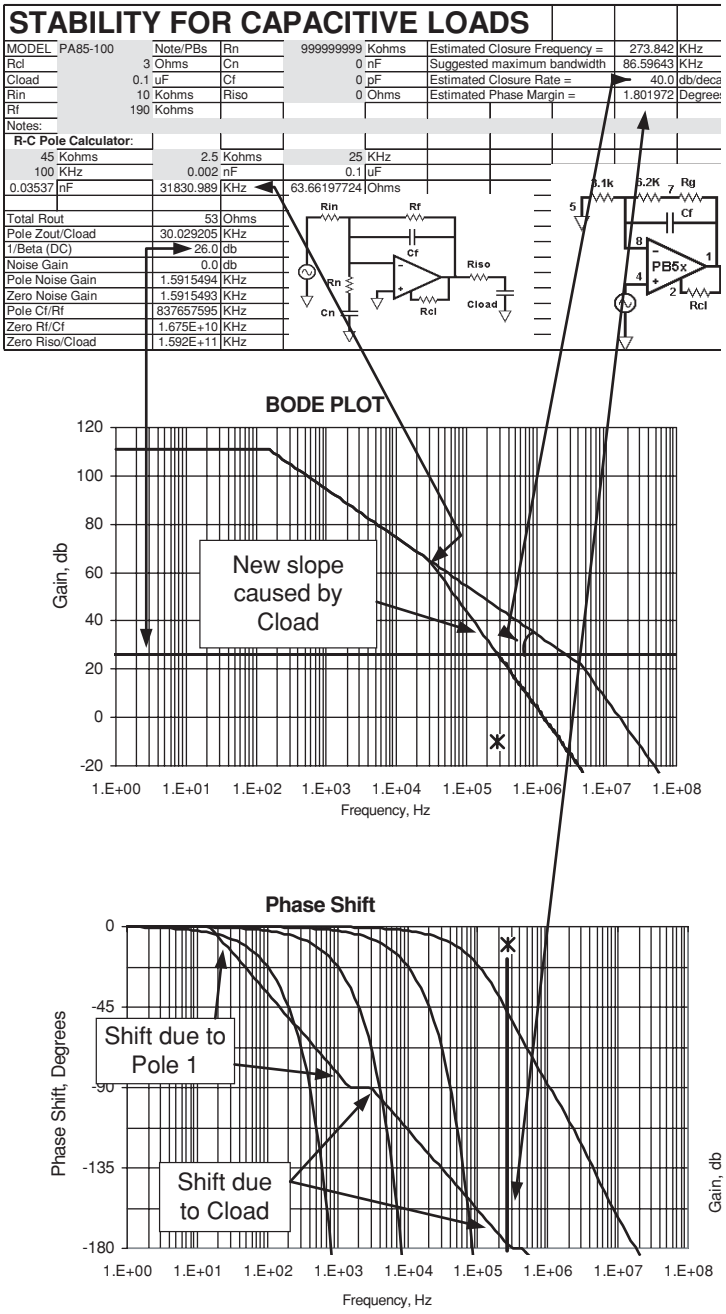


FIGURE 5. MODELING A LARGE CAPACITIVE LOAD

interest for stability concerns is at Fcl where intersection rate is 20db per decade and open loop phase is about 135°. This means the phase margin is about 45°.

The R-C Pole Calculator is a convenience item having no effect on any of the results. However, it does make it easy to translate graphic data to component values. Below this are listed many of the operating points of the circuit. As experience is gained using this tool, you will start using some of these numbers directly to eliminate paging down to the graphs.

In contrast, Figure 4 shows the same amplifier compensated for a gain of 100, but still configured for unity gain. Pole 1 has moved up in frequency giving us a greater gain-bandwidth product, but notice that pole 2 is now well above 0db and the intersection rate is 40db per decade. Our phase margin has disappeared. This example is a little radical, but it does show the dangers of improper compensation. There are also some op amps having a minimum gain specification which would fit this same general picture if used below the minimum gain spec.

In the following examples, we will first attempt to obtain an intersection rate of 20db per decade (a very good sign but not a guarantee) by visualizing line segments and then checking out the actual phase graph.

LARGE CAPACITIVE LOADS CAUSE PROBLEMS

Open loop output impedance of an amplifier forms a pole with a capacitive load, which is modeled as an additional pole in the small signal response as shown in Figure 5. This is our same amplifier (compensation recommended for gain=20), attempting to drive a heavy Cload with an inverting gain of 19. Note that this pole introduced with the addition of an external component is causing the same 90° shift of phase; 45° taking place below the pole frequency and the other half above. Any time the combination of Zout (sum of the amplifier output impedance and any other resistance inside the loop) and Cload is large enough to place this pole below closure frequency. The intersection rate will no longer be 20db per decade and stability will be in question.

It is now time to start the process of visualizing potential solutions. We know good intersection rate is a key. Sometimes we can change amplifier compensation to move the open loop response, but usually not enough to cure this problem. One thing we might do is increase the closed loop gain to 66db. Entering Rin=.1 results in the data shown in Figure 6 where the stability problem now looks fine with a phase margin of ~45*. There are several problems associated with this solution. The most obvious is that we have changed the closed loop transfer function which now requires other system changes to compensate. Next, DC errors due to voltage offset and drift are up by a factor of 100! Also notice that if we demand the recommended 20db of loop gain, circuit bandwidth is only ~2.7KHz, about a factor of 30 reduction. This solution is rarely acceptable.

USING AN ISOLATION RESISTOR

Go back to Figure 5 and imagine we have the power to grab the segment modeling the effect of our Cload, just above the intersection point (about 200KHz & 30db) and bend it back to a minus 20db/decade slope. This would result in a new intersection rate of 20db/decade. This is exactly what an isolation resistor does

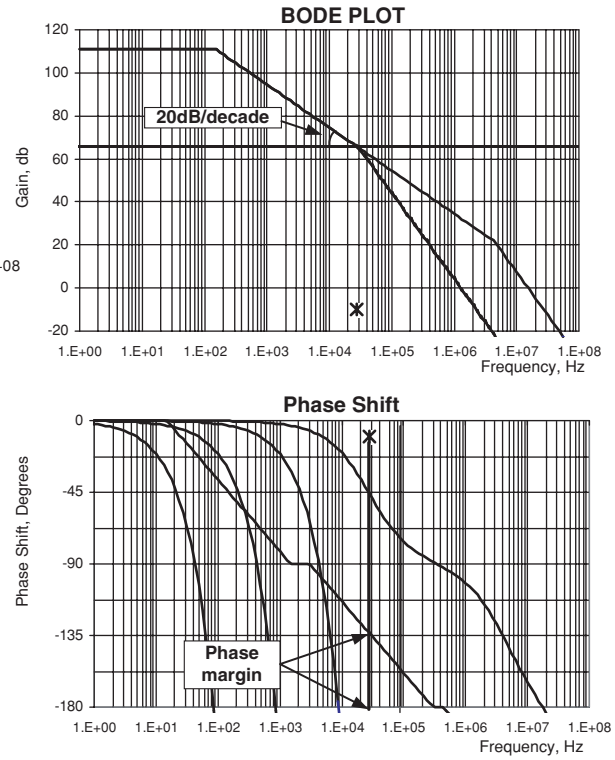


FIGURE 6. INCREASED GAIN YIELDS ACCEPTABLE PHASE MARGIN

for us! The R-C Pole calculator is pre-loaded with the Cload value and prescribes 8 ohms when we enter the corner frequency of 200KHz. Figure 7 shows the results of entering 8.2 ohms as Riso.

What about larger values of Riso? They will produce stable circuits but there are two things you need to know. Riso is outside the feedback loop where voltage drops and phase shifts are not corrected by loop gain. The curve labeled "Signal at Cload" shows roll off of the signal at the actual load. Check Figure 8 to see the effect of increasing Riso to 40 ohms. The load is now rolled off at 40KHz cutting usable bandwidth to about half that of the 8.2 ohm solution. The suggested maximum bandwidth cell does not take this into account. Also, phase shift outside the loop is not reported by Power Design.

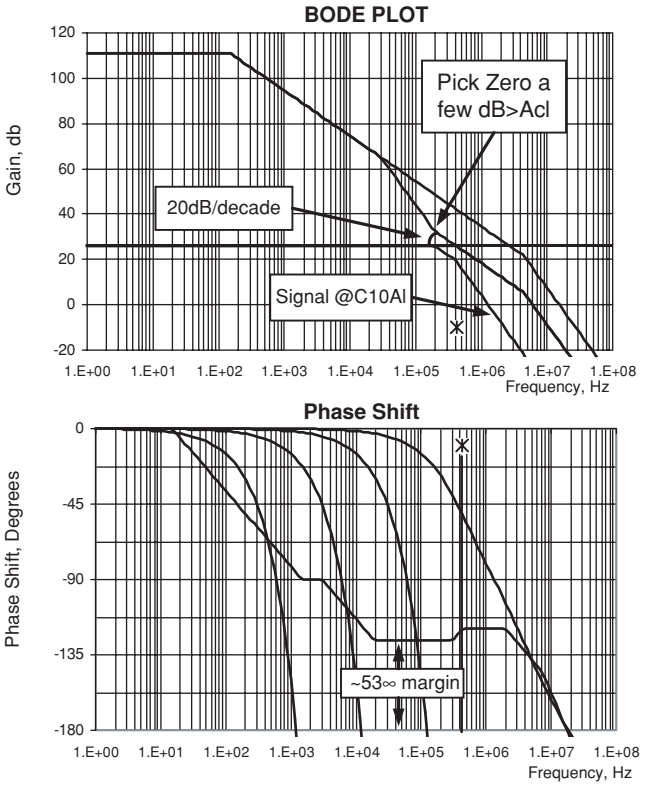


FIGURE 7. AN ISOLATION RESISTOR IS OFTEN THE BEST STABILIZATION METHOD

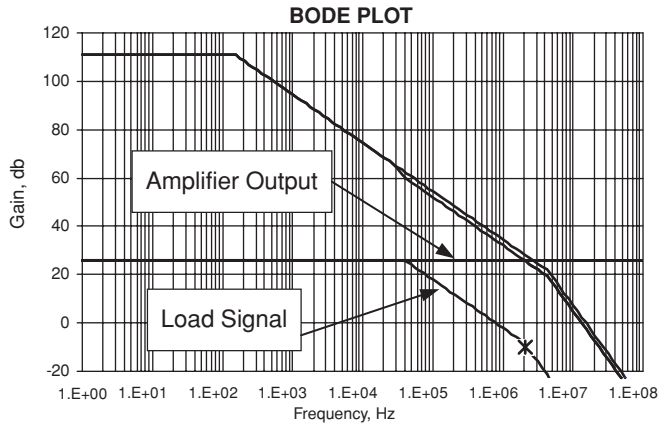


FIGURE 8. THE BANDWIDTH PENALTY IMPOSED BY LARGE ISOLATION RESISTORS

Do not let these drawbacks to the isolation resistor technique scare you off. It is the easest to visualize from the graph; generally not bothered by parasitics; works equally well for inverting and non-inverting circuits; and it is very tolerant of variations in Cload. This circuit remains stable even if the load capacitance increases

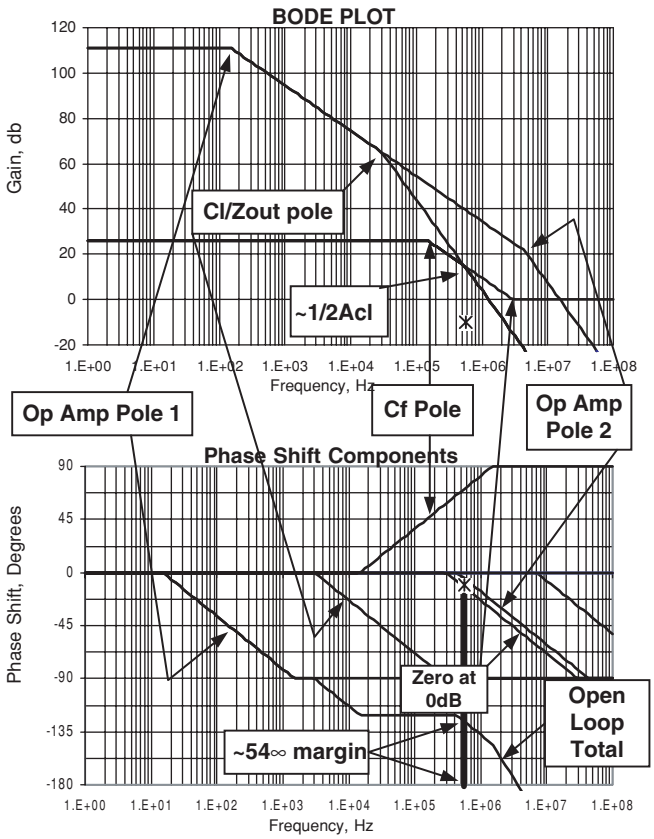


FIGURE 9. A CORRECTLY SIZED ROLL OFF CAPACITOR ACHIEVES STABILITY

MODEL	PA85-100	Note/PBs	Rn	9999999999	Kohms
Rcl	3	Ohms	Cn	0	nF
Cload	0.005	uF	Cf	0	pF
Rin	10	Kohms	Riso	0	Ohms
Rf	190	Kohms			
Notes:					
R-C Pole Calculator:					
1	Kohms	2.5	Kohms	25	KHz
20	KHz	0.002	nF	0.005	uF
7.95775	nF	31830.989	KHz	1273.239545	Ohms

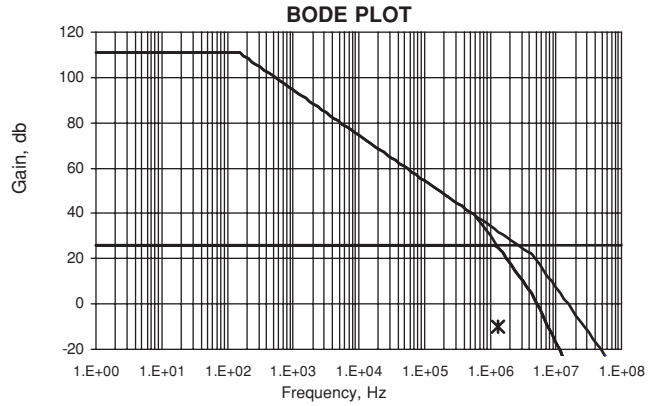


FIGURE 10. A NEW PROBLEM TO CONQUER

several orders of magnitude. This is true because the singular value of Cload forms both a pole with the amplifier output impedance and a zero with Riso. These tend to cancel each other as they move up and down the frequency spectrum together with changes in Cload. Obviously, huge values of capacitance reduce bandwidth.

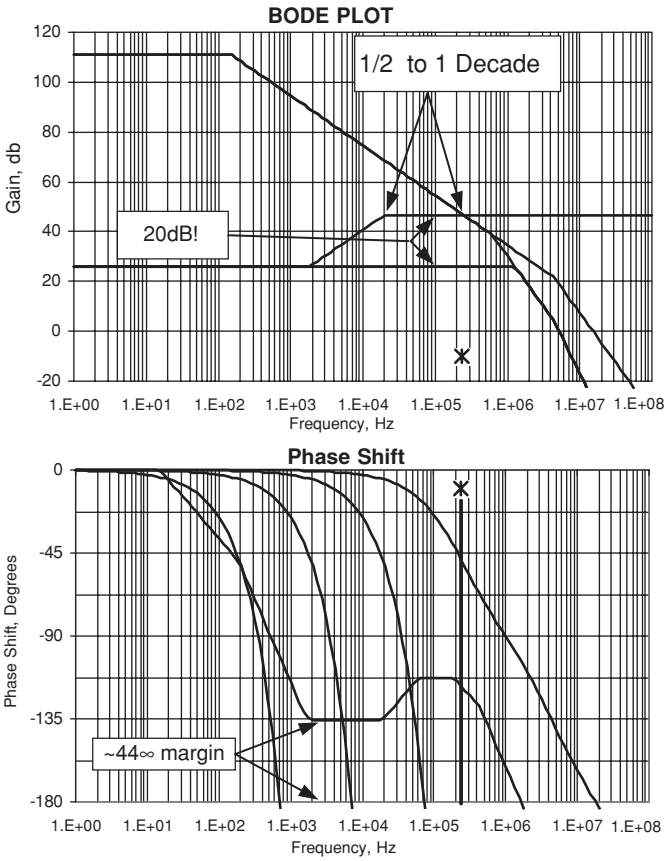


FIGURE 11. THE NOISE GAIN COMPENSATION NETWORK DOING ITS THING

THE ROLL OFF CAPACITOR

We know a capacitor across the feedback resistor will attenuate high frequency gain or roll off the circuit, changing slope of the closed loop gain from zero to -20db/decade. If we position the pole of this roll off correctly, it will cross the open loop gain curve producing an intersection rate of 20db/decade giving a good shot at stability. We also know that 1/beta is the critical factor in stability analysis; it must be thought of as non-inverting; and non-inverting gain (or 1/beta) can never go below 0db. This means the desired segment of 1/beta will have a -20db/decade slope, starting at 26db and stopping at 0db. Here's where the vision or feel of things comes in. Look again at the graph of Figure 5, our problem statement. Picture (maybe with the help of a straight edge) a line segment with a -20db/decade slope crossing the open loop gain curve at half the closed loop gain (13db in this case). At what frequency will this segment cross the closed loop gain (26db)? With a little practice, your vision will yield about 150KHz and the R-C Pole Calculator will tell you 5.6pF across the 190K ohms is the place to be. See Figure 9 for the results.

We now have a paper circuit with ~54° phase margin, the desired gain, acceptable DC accuracy and a recommended bandwidth of 86KHz. The reason for the phrase "paper circuit" has to do with parasitic capacitance, which can vary wildly with quality of the physical layout. If the actual layout were to add 5pF to the feedback capacitor, we would loose almost 20° of our phase margin. In addition to careful layout, consider using lower values for the input and feedback resistors. Cutting the resistors in half will double the value of Cf, making errors due to parasitics less destructive.

Was this magic? No, just Power Design automation of Apex Application Note 25 on Driving Capacitive Loads. Refer to this and Application Note 19 on Stability for Power Operational Amplifiers for theory and formulas. You will learn that the closed loop phase shift curves we have been looking at are the sum of effects of all the poles and zeros in the circuit. The bottom curve of Figure 9 shows graphically most of the individual phase shift components. Individual phase shift relating to pole 1 is hidden under the total curve. The only positive going curve is the result of the pole of the roll off capacitor. Note the zero associated with Cf (-45° at 3MHz) when 1/beta reaches 0db. Do not fall into the trap of thinking that if a small capacitor is good, a bigger one must be better. This capacitor will certainly roll off signal amplitude below 0db, but it does not take 1/beta below 0db. A larger capacitor would produce a flat high frequency 1/beta at 0db, a high intersection rate and oscillation.

The roll off capacitor technique is very effective when closed loop gain is 20db or more. With a slope of 20db/decade on this segment, the frequency spacing of the pole and zero are directly related to closed loop gain. As gain decreases the pole and zero become closer together and cancel each other.

THE NOISE GAIN COMPENSATION NETWORK

The last technique requires two components and requires the non-inverting input to be hard grounded. The hardware is a series connected R-C from the summing junction to ground. The Power Design schematic has them labeled Rn and Cn. With this network grounded, it does not change gain of the signal path. At high frequencies, where you would think of Cn as appearing as a short, the noise of this circuit will increase because it has two input resistors in parallel making the net gain higher. The real objective, however, is to increase 1/beta or to reduce the fraction of the output signal fed back to the inverting input.

Please: Visualize, "feel" and refer to Figure 10 with a modified problem statement. The capacitive load is only 5nF this time, but this is enough to yield a phase margin of ~8°. Step one is to imagine a new horizontal line located 20db above the original closed loop gain. Note the frequency where the new line crosses the open loop gain curve. Step two is dividing by something between 3 and 10. For now, let's pick 10 and hope your answer is somewhere in the area of 20KHz. ***This will be the pole location of the noise gain network.***

The 20db elevation of the new line segment is important; too little does not help enough, too much gets to be just as bad. Select the value of Rn such that when paralleled with Rin, the non-inverting gain goes up by a factor of 10. An approximation is simply Rin/10, which has already been entered in the R-C Pole Calculator. Power Design tells us this approximation yields 20.4db. Entering the desired pole frequency of 20KHz yields 8nF. We will use 8.2nF and proceed to Figure 11.

Noise gain compensation works best when the pole formed by output impedance and capacitive load is not more than 20db above the closed loop gain.

A COMBO DEAL IS NOT ALWAYS FAST FOOD

We found that a minimum closed loop gain of 20db is desirable for the roll off capacitor to do a good job. Also, for the noise gain compensation to produce good results, we want no more than 20db between closed loop gain and the pole produced by output impedance and the load capacitor. There are a fair number of applications requiring a signal gain of -1, which is a 1/beta of only 6db. See Figure 12 as our next problem statement. This circuit is an ideal candidate for a combination of both roll off capacitor and noise gain techniques.

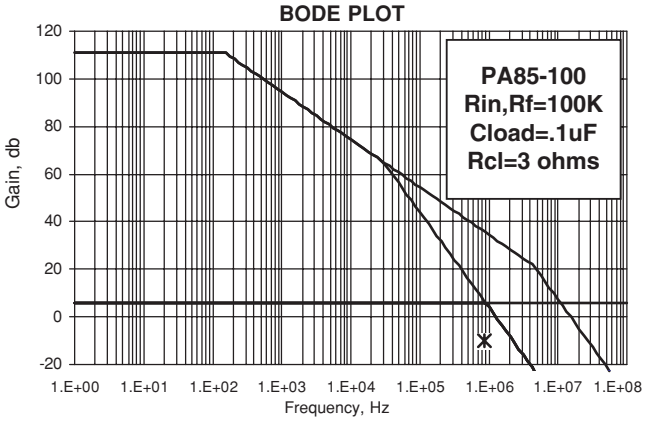


FIGURE 12. LOW GAIN AMPLIFIERS PRESENT THE BIGGEST CHALLENGE

As a first step, select Rn for a 20db increase of 1/beta or non-inverting gain (5K was used in this example). For a trial, enter 1000nF for Cn and refer to Figure 13 showing our new 1/beta. Divide the frequency where 1/beta crosses open loop gain (~250KH) by 2 and set the Cf pole accordingly. Set the noise gain pole two decades lower yet. The R-C Pole Calculator makes it easy to select 12pF for Cf and 27nF for Cn. Figure 14 shows the results.

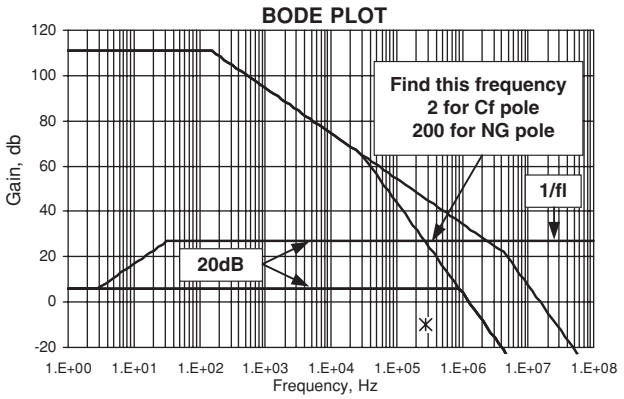


FIGURE 13. SETTING UP THE INITIAL NOISE GAIN CURVE

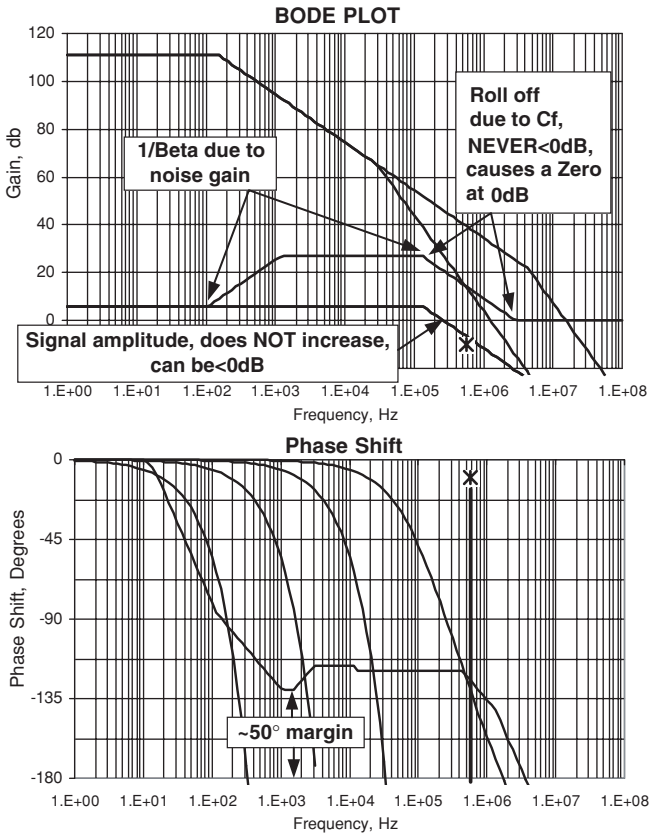


FIGURE 14. COMBINING NOISE GAIN WITH A ROLL OFF CAPACITOR

COMPARING THE METHODS

Your Daddy probably avoided using the isolation resistor technique because of the dreaded voltage drop outside the loop. But being of the enlightened age, you will look at the roll off error shown in Figure 15 and realize this error applies to any feedback capacitor inside the loop as well! This means that when pole frequencies are equal, gain errors introduced by either an isolation resistor or a feedback capacitor are identical.

We also need to look at the phase shift issue. The lower graph of Figure 15 shows the phase shift occurring outside the loop; an error to be added to the closed loop phase shift to find total phase shift applied to the actual load. Comparing the closed loop phase shift of Figure 7 (the isolation resistor solution) to that of Figure 9 (the feedback capacitor solution) reveals much better phase performance when the isolation resistor is used. The key to this difference is that adding the feedback capacitor introduces both a positive and a negative component to open loop phase shift while adding an isolation resistor introduces only a positive component. This difference can be seen directly in the Phase Components graphs. For an indirect indicator, notice that open loop phase beyond the closure frequency falls off more rapidly with the Cf solution than with the Riso solution. Table 1 shows gain errors and total phase shift errors for the two circuits at the suggested maximum bandwidth and several points below. With the pole frequency of the isolation resistor solution a little higher than the pole of the feedback capacitor solution, both gain and phase performance of the isolation resistor solution is superior.

	865KHz	43KHz	22KHz	8.6KHz	860HZ
Cf Gain	12.8%	4%	1.1%	0.17%	0.002%
Riso Gain	8.7%	2.4%	0.62%	0.1%	0.001%
Cf Phase	40°	21°	11°	4.3°	0.43°
Riso Phase	37°	19°	9.5°	3.9°	0.39°

TABLE 1. TOTAL GAIN AND PHASE ERRORS FOR Cf AND RISO SOLUTIONS

WORKING WITH COMPOSITE AMPLIFIERS

Stability headaches seem to escalate exponentially with the number of amplifiers in the loop, so most designers tend to avoid them. However, the composite is often worth the extra trouble when large power levels and high DC accuracy are both required. The techniques to achieve stability with the composite are basically the same as we already covered; stabilize the power stage first, then repeat the job for the total circuit.

Figure 16 is the data entry screen for the second half of this work. The first half is represented by the Pwr symbol (accomplished as above), and those numerical results become input data for this half. The schematic is showing that the closed loop response of the power stage is in series with the host amplifier, or is being added to the open loop response of the host amplifier. Stability analysis for the composite performs exactly that addition and a typical result and the classic problem with the composite is shown in Figure 17.

The OP07 host amplifier has a well behaved open loop gain curve with its second pole near 0db gain. If the small signal amplifier you wish to use is not included in the built-in data base, Power Design comments tell how to enter data extracted from a data sheet. The model of the composite open loop gain features the poles of both the host amplifier and the closed loop power stage response. The pole at ~25KHz (due to the roll off capacitor in the power stage) causes an intersection rate of 40db/decade for any closed loop gain between 25db and 45db. Lower gains would yield 60db/decade because closure frequency in the power stage places pole just over 80KHz. It is quite possible to see this type stability problem even when not driving a capacitive load..

Power Design provides two techniques to stabilize the composite circuit. If an isolation resistor was used, it is modeled in the power stage only and its effects are included in the closed loop response data fed into the composite problem statement. You may use the roll off capacitor, the noise gain network or both as shown in Figure 18. The same basics on component selection apply here, but you may find a little more tweaking of component values is required. Final values for the solution shown are Rn=3.4K, Cn=15nF and Cf=47pF which yield a phase margin of 52°.

DOES INDUCTANCE ALWAYS BRING STABILITY PROBLEMS?

The answer is no. You can drive inductance all day long in the voltage mode without waking the dragon. The problem is current mode drive where inductive V-to-I phase shift is inside the loop, courtesy of the current sense element. Figure 19 illustrates a combination of typical topologies on the data entry screen. We will address the numbered boxes later.

The most simple real topology is realized by applying the input signal to the non-inverting input and not using Rin. The power op amp drives the load in phase with the input signal to whatever amplitude is required to obtain voltage across Rs equal to the input signal. Adding Rin (grounded) to the circuit causes the voltage across Rs to be greater than the input signal.

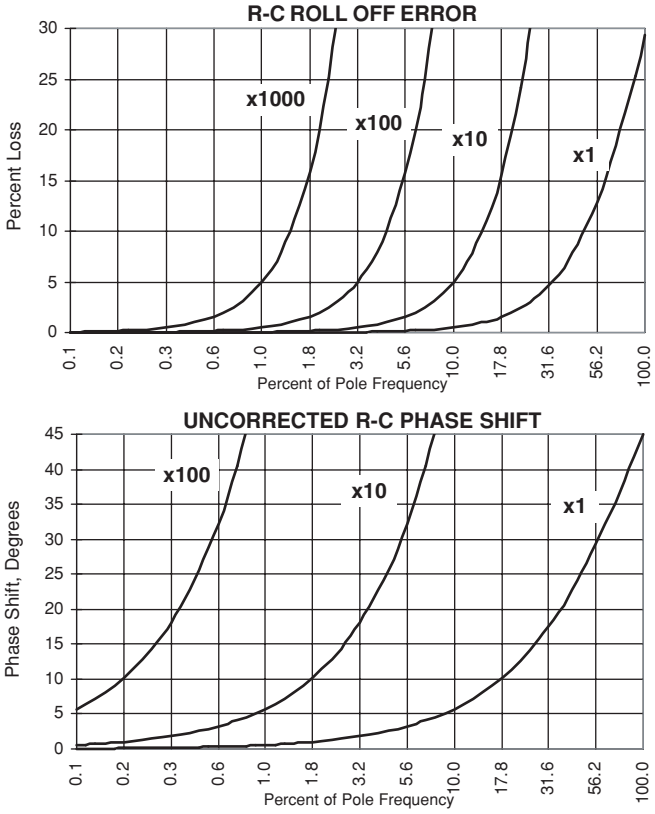


FIGURE 15. R-C ROLL OFF AMPLITUDE ERROR AND UNCORRECTED PHASE SHIFT

Composite Circuits

MODEL	OP07	READ ME				Estimated Closure Frequency =		86.59643	KHz
Aol =	135	db	Pole 1 =	0.1	Hz	Suggested maximum bandwidth		27.3842	KHz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz	Estimated Closure Rate =		40.0	db/decade
Rin	21	Kohms	Rn	9999999999	Kohms	Estimated Phase Margin =		13.41074	Degrees
Rf	340	Kohms	Cn	0	nF				
Cf	0	pF	Using Look-Up data						
Notes:									
R-C Pole Calculator:									
9	Kohms	90	Kohms						
200	KHz	0.43	nF						
0.08842	nF	4.1125308	KHz						
1/Beta (DC)		24.7	db						
Noise Gain		0.0	db						
Pole Noise Gain		0.1591549	KHz						
Zero Noise Gain		0.1591549	KHz						
Pole Cf/Rf		4.681E+09	KHz						
Zero Rf/Cf		8.047E+10	KHz						

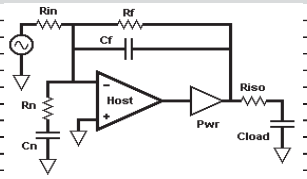


FIGURE 16. ENTERING HOST AMPLIFIER FOR THE COMPOSITE CIRCUIT

To achieve an inverting circuit, ground the non-inverting pin and apply the signal to Rin. The op amp will drive the load out of phase at an amplitude large enough to develop a voltage on Rs equal to Rf/Rin. This inverting setup has dual advantages over the non-inverting circuit. Voltage on the sense resistor can be larger or smaller than the input signal, plus there is no common mode voltage on the amplifier.

Notice that in both circuits the load impedance is inside the feedback loop, meaning closed loop gain is partially a function of load impedance. This is exactly what we want for current control; load impedance goes up; gain goes up; output voltage goes up; and current remains constant. Refer to Figure 20 for a picture of the problem with "the gain goes up". Open loop gain is falling at 20db/deacade and closed loop gain is rising at 20db/decade to produce an intersection rate of 40db/decade; an event of which we've grown suspicious.

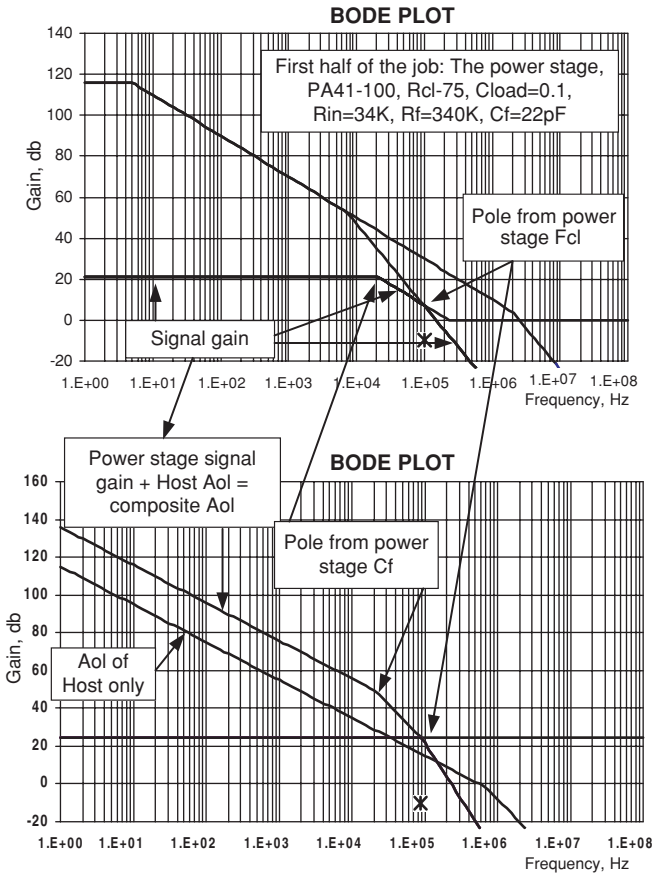


FIGURE 17. A POWER STAGE RESPONSE INCORPORATED INTO A COMPOSITE AMPLIFIER

When it comes to adding all the phase shift elements to find open loop phase shift (and phase margin), notice that the first pole in the open loop response of the op amp is nearly coincident with a zero in the closed loop. This causes open loop phase to drop like a rock to 180°(zero phase margin) at 100Hz. The key to stabilizing this circuit will be to lower the frequency of the closed loop pole (currently at the intersection point) by using a second feedback path consisting of Cf and Rd.

This R-C network will introduce a second feedback path doing practically nothing at low frequencies but providing dominant voltage feedback at higher frequencies, without the additional V-to-I phase shift of the inductor. Figure 21 shows a typical solution where the flat portion of this feedback path is usually positioned at least 20db above DC gain or 20db below the intersection of open loop gain and the inductive feedback path. If there is a conflict between these to goals, start with the higher db level. The corner frequency of the R-C network is usually about 3/4 of a decade below the intersection of the two feedback paths.

The circuit function of our example is an inverting amplifier with an input signal of ±10V and a transfer function of 0.167A/V. At peak currents of 1.67A, power dissipation in the sense resistor seemed acceptable and values of Rin and Rf were convenient. Please note that these same component values could model a non-inverting amplifier with a transfer function of 1A/V.

Refer to Figure 19 again to see that Power Design calculates two values for Rd and then a value for Cf. To use these features:

1. Enter large values for both Cf and Rd.
2. Enter the larger recommendation for Rd.
3. If phase margin is well over 45°, raise Rd, if less, lower Rd.
4. When satisfied with phase margin, enter recommendation for Cf.

In this example, values of 82K ohms and 120nF were used.

As transfer functions and Q ratings of inductors change, the curves Power Design draws for you will vary a lot. As in this example, some will fall into place with suggested values; some will require playing

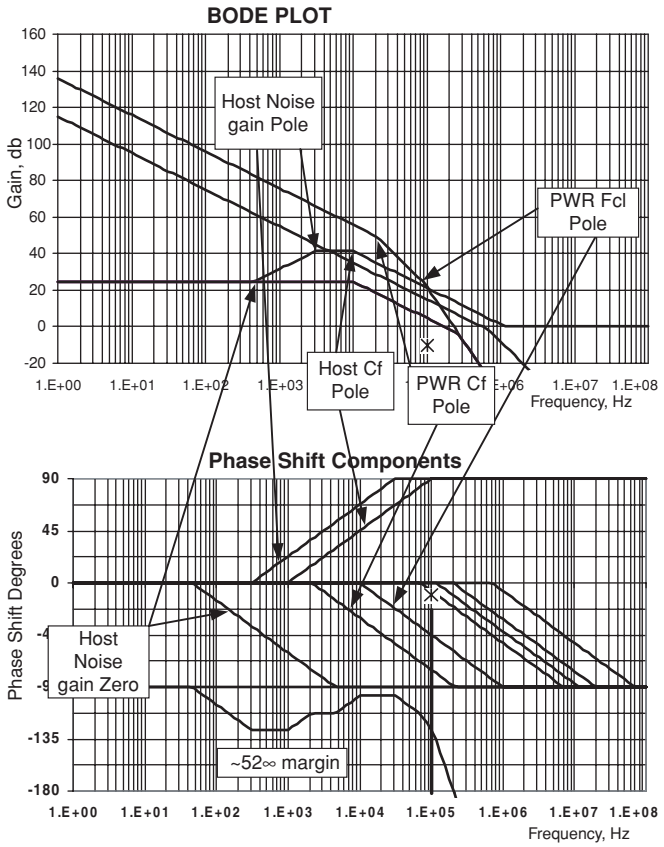


FIGURE 18. THE FINISHED COMPOSITE AMPLIFIER

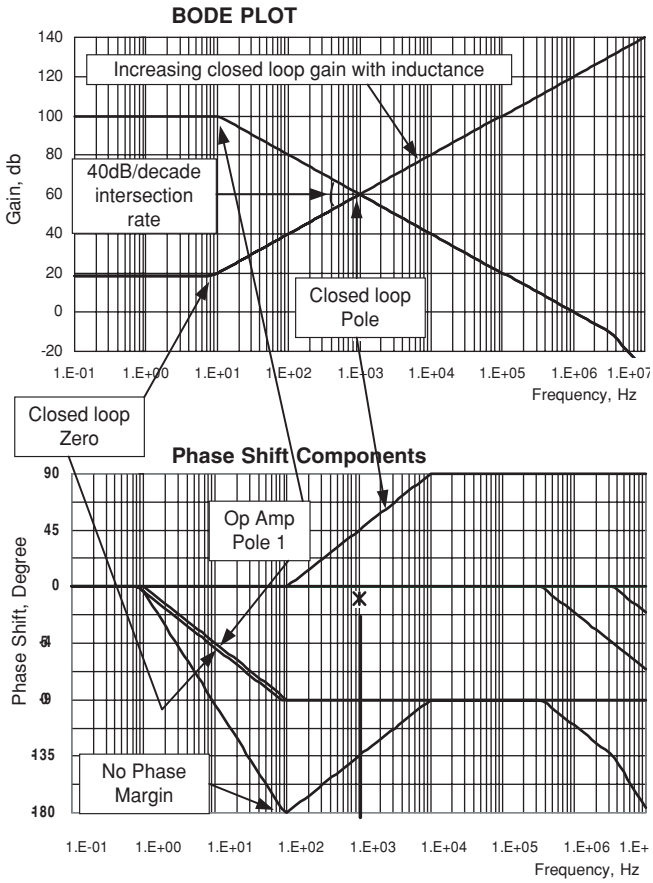


FIGURE 20. GAIN AND PHASE PROBLEMS CAUSED BY INDUCTANCE IN THE FEEDBACK LOOP

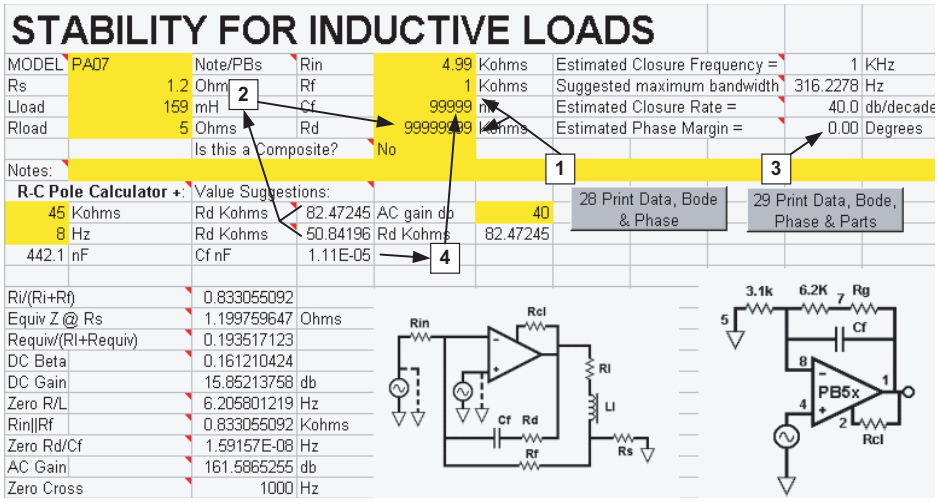


FIGURE 19. STEPS TO STABILITY FOR CURRENT CONTROL WITH INDUCTIVE LOADS

with the value of Rd; and a few may require no network at all. When viewed as a single issue, stability for these amplifiers is simple. However, you will often find yourself fighting for bandwidth. The good news is that re-running the stability analysis for a dozen sets of gain and sense resistors is an easy task. As a general rule, large sense resistors and low gain settings will maximize bandwidth.

THEORY IS GREAT--------BUT

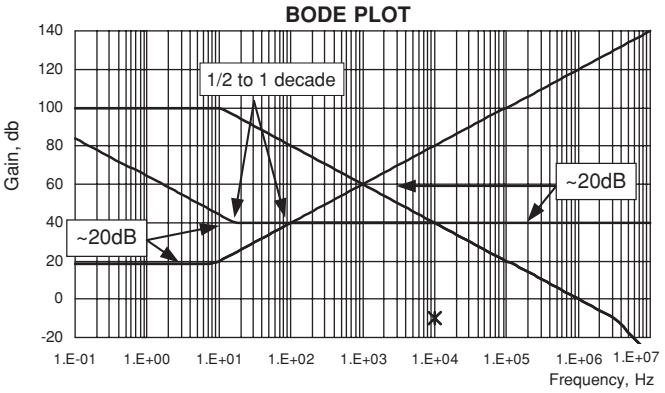
We have mentioned parasitics and layout concerns a couple of times. Please pull from your memory the old phrase, "too broad a subject to cover....". True, so we will get right to Figure 22 and say the job is positively not finished until the hardware is tested. Use all components as close to production version as possible; power supplies, cable harnesses, signal sources, loads and any thing else you can think of.

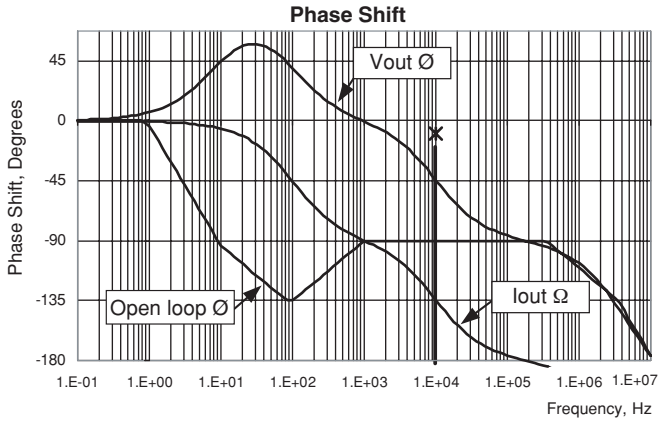
Watch the 1KHz output signal for over/under shoot while setting the very low frequency signal to exercise the amplifier output (plus the supplies, cables and the load) over the entire dynamic range. Then estimate phase margin of the system using the graph. A little time spent here now may keep you off the production line in six months.

CONCLUSION

The next time you happen to be involved in a nightlong argument about whether stability is a science or a black art, just smile. You won't have to say anything, just keep smiling. It would be good though, if you have your laptop along loaded with Power Design. When you think the smiling is about to get you smacked, tell the crowd both arguments are correct; arithmetic is the science portion, but expecting anyone to remember all the rules and formulas is the black art. With almost instant calculations and graphic data presentation, arithmetic is a snap and a lot of the rules can remain hidden. Power Design's built-in documentation presents the most important procedures and rules at the command of your mouse. The entire process becomes so easy, tasks like checking worst case component tolerances become bearable.

You'll be the hit of the party.





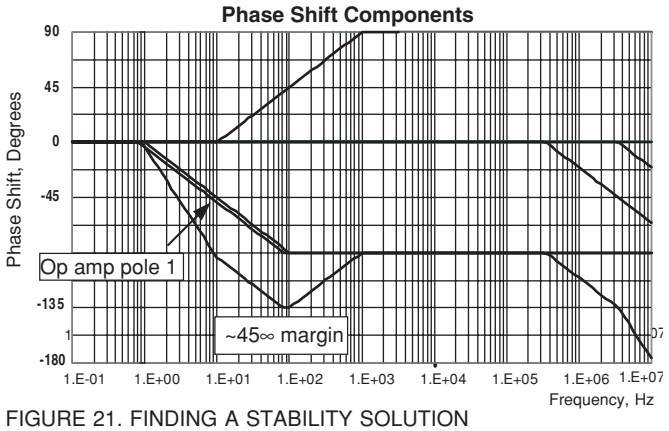
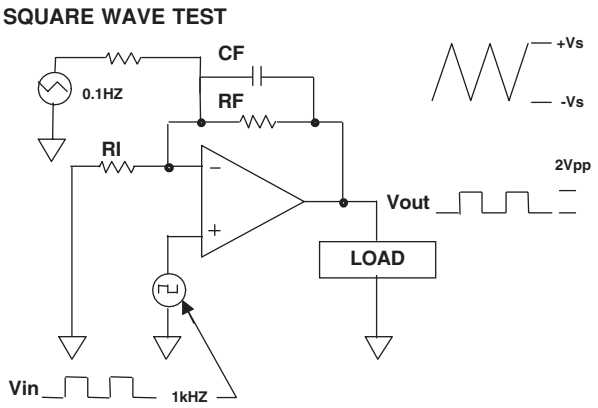


FIGURE 21. FINDING A STABILITY SOLUTION



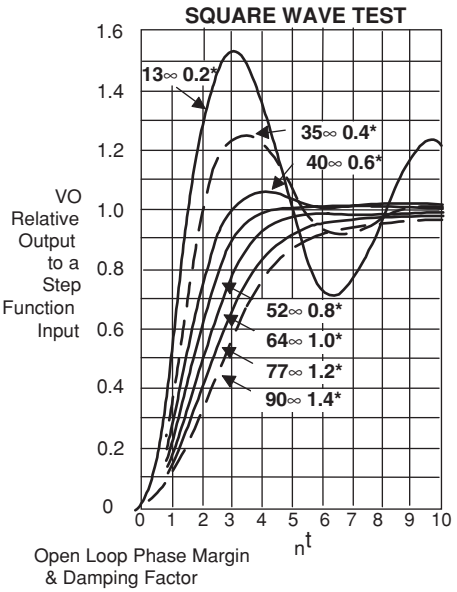


FIGURE 22. TESTING THE ENTIRE SYSTEM HARDWARE FOR PHASE MARGIN

APPLICATION NOTE 39

USING THE POWER DESIGN TOOL

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

Those of us who have ventured into high power linear circuits with their massive and sometimes liquid cooled heatsinks have a tendency to go ga-ga over the efficiency potentials of the Pulse Width Modulation (PWM) amplifiers. This is OK. But these little switching miracles do bring a new set of challenges to the table.

The PWM amplifier with no filtering is NOT capable of amplitude modulation. It can only change times and maybe polarity. We get lucky once in a while and get a load which will do the filtering for us. Much more often we must design the filter, a job many of us do not place at the top of our list of most cherished activities. In addition to this, the methods required to calculate internal power dissipation and the heatsink size are quite different than those used in the linear world.

The Power Design CAD tool automates Butterworth filter equations found in Apex Applications Note 32 and expands on this base by graphing response with real world components. It then goes on to automate internal power dissipation equations, plus draw a wide variety of graphs on amplifier performance over frequency. As the overall process is usually iterative, the benefit of computer analysis is indispensable.

SOME PWM BASICS

PWM circuits achieve high efficiency compared to their linear counterparts in much the same manner as switching power supplies do versus linear supplies. If the control block is optimized for producing a wide output range rather than a fixed output level, the power supply becomes an amplifier. Figure 1 illustrates a typical PWM amplifier output stage employing four switches configured as an H-bridge providing bipolar output from a single supply. This does mandate that both load terminals are driven and zero drive results in 50% of supply voltage on both load terminals.

The H-bridge switches work in pairs to reverse polarity of the drive, even though only one polarity supply is used. Figure 2 shows waveforms of locked anti-phase modulation where S1 and S4 are

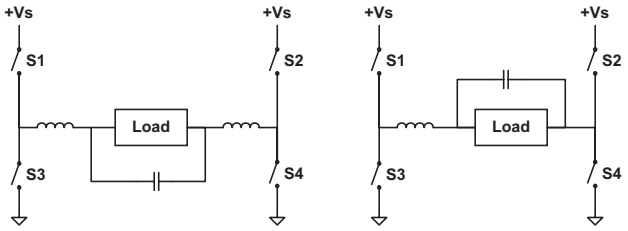


FIGURE 1. H-BRIDGE OUTPUTS WITH DIFFERENTIAL AND SINGLE-ENDED FILTERING

on during one portion of each cycle, and S2 and S3 are on during the remainder of the cycle.

To help understand the conversion of the time modulated data to analog levels, visualize each waveform segment of Figure 2 run through a low pass filter whose cutoff frequency is at least 10 times lower than the switching frequency. The A and B voltages of the 50% duty cycle waveforms will both be equal to 50% of the supply voltage. With both terminals of the load connected to the same voltage, the load sees 0V across itself. The A-B waveform represents this differential connection of the load, and the filtered voltage of this waveform equals zero. To examine the 95% duty cycle waveforms, lets assume a supply voltage of 100V. The filtered A value will be 95V, B will be 5V, and the load will see 90V; the same as the filtered value of the A-B waveform.

Note that if S1 and S3 were to turn on simultaneously, there is nothing to limit current. Self-destruction would be only microseconds away. The fact that these transistors turn on faster than they turn off,

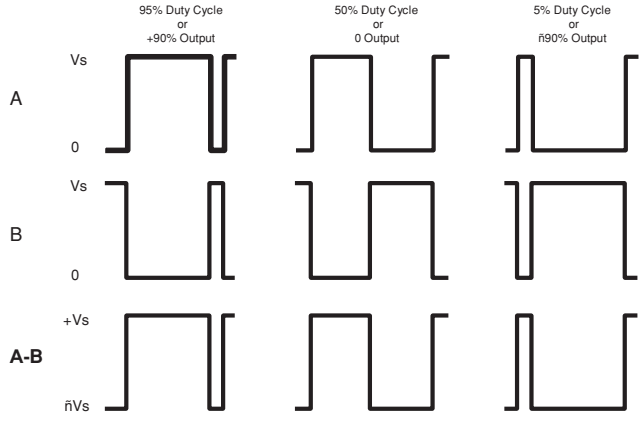


FIGURE 2. H-BRIDGE WAVEFORMS

means a “dead time” needs to be programmed into the controller if doing your own design. When you buy the amplifier from Apex, this is all inside the package.

Changing duty cycle through 50% is a continuous function, meaning there is no inherent discontinuity as exists in sign magnitude modulation. This is analogous to the much improved distortion levels of class AB linear stages versus class C linear stages where zero current crossing brings a discontinuity or dead spot usually referred to as crossover distortion.

National created their FAST and DAMN FAST buffers, but they can’t hold a candle to these guys. In fact, that’s the problem with switchers- -they move voltages and currents around so fast it’s difficult to keep the noise down. From the linear or analog world we borrow the equation relating slew rate to power bandwidth. If your PWM amplifier switches 50V in 25ns, the slew rate is 2000V/us. With a peak voltage of 50V, this equates to over 6MHz. With 5 or 10 amps flowing, those transitions contain RF energy similar to a moderate radio transmitter. Spending a few minutes thinking like an RF designer may be worthwhile.

Refer to Figure 3 for a pictorial of the filter’s job. The relatively flat portion of the curve is the pass band of the filter. The signal frequency of the power drive to the load must fit under this area.

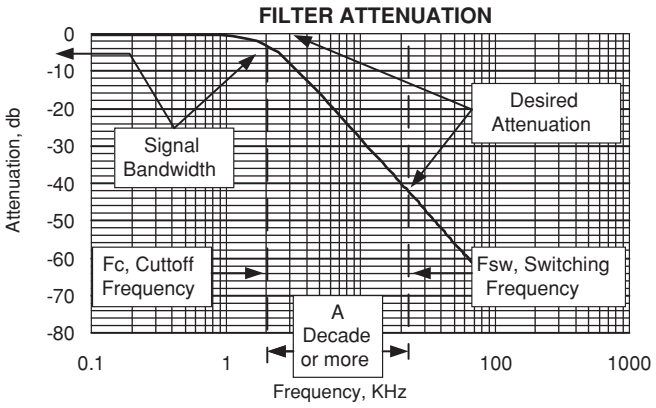


FIGURE 3. PWM FREQUENCY RELATIONSHIPS

Desired attenuation in this area is 0db and the corner frequency is Fc, the cutoff frequency. We then go down the filter slope to the switching frequency, Fsw. Allowing one decade between these two

frequencies is a good starting point. In this case, the graph tells us the worst case peak ripple voltage at the switching frequency will be a little under 1% of the supply voltage.

Figure 4 illustrates how a zero output voltage corresponds to a 50% duty cycle and produces maximum ripple current. As expected, there is a linear relationship between increased output voltage and increased duty cycle. Not quite as obvious is the curve that indicates the ripple current is reduced all the way to zero if we push modulation all the way to steady state.

The need to squeeze the last ounce of bandwidth from our designs, along with the physics limitations on switching frequencies, makes it desirable to minimize the distance between signal and switching frequency. Pure theory says adding more poles can increase filter slope. This is true to a point. We would probably question an eight-pole filter in the small signal world. Do you really need that? Can you find high enough quality components to make it work? Can you afford it in terms of size and cost?

In the PWM world these questions are not only valid but are many orders of magnitude more important because power levels have gone from mW to KW! Rule of thumb: Allow at least a decade between switching and signal frequencies.

RIPPLE CURRENT AND DUTY CYCLE VS. OUTPUT VOLTAGE

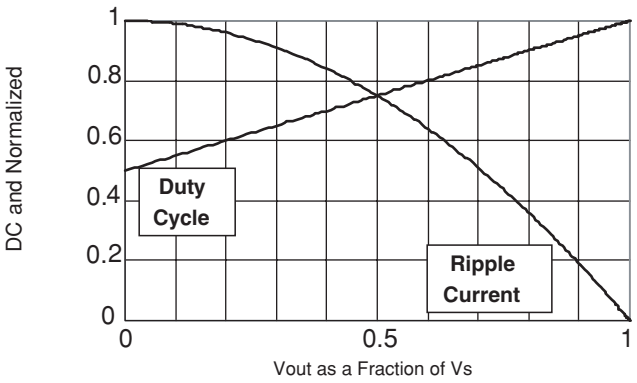


FIGURE 4. DUTY CYCLE AND RIPPLE CURRENT VARIATIONS WITHOUT OUTPUT VOLTAGE

THE POWER DESIGN APPROACH TO SUCCESSFUL PWM AMPLIFICATION

The usual process is:

1. Select an amplifier model (possibly with the Part Selector sheet).
2. Load circuit data into the PWM Filters sheet.
3. Auto load components into the Filter/load model and sweep the frequency.
4. Tune components and parasitics plus check load variations and fault conditions.
5. Set sweep frequency band from Fmax to at least 10 times Fsw to check high frequency attenuation.
6. Use the graphs to select the heatsink.

The Power Design, PWM Filters sheet data entry screen for step 2 is shown in Figure 5. The pull down Model cell reads the built-in database containing specifications on supply voltage, maximum switching frequency, current levels, and internal resistance. Alternatively, comments in the database area provide instructions to enter data for your own design.

Switching frequency, Fsw, is required because some models are programmable, most can be run lower than the maximum and many can be driven with digital signals. Immediately to the right of this data entry cell is the maximum for the model selected. Enter minimum frequency to be amplified as Fmin. Use .001 for DC. Consider using .001 even if the application is a substantially higher fixed frequency, as this may simulate a "lost" input signal condition and some circuits will present their lowest impedance at DC. Enter the maximum frequency to be amplified in Fmax. Fmin and Fmax set the frequency end points of the sweep that will be run later. Fcutoff is the cutoff frequency of the filter and will be the -3db response point. The next three cells describe three series connected elements forming the load. Vripple is the maximum peak voltage on the load at the switching frequency, your way to specify the attenuation of the filter at Fsw. The bottom two cells specify the magnitude and unit of measure for the output signal.

The Order Calculation section first converts your maximum ripple and power supply ratings into db attenuation. Then by examining the switching and cutoff frequencies, it calculates the order, or number of poles needed. The integer recommendation is rounded up. The matching network that is calculated will cause reactive loads to appear resistive to the output of the filter. Figure 6 shows the actual filter components for filter orders up to N=6, plus expected ripple current at the switching frequency. Figure 7 shows the ideal response graphed and an area where attenuation at specific frequencies can be checked in detail.

"Ideal" is a great word. Just as we use the concept to describe theoretical performance of the linear op amp, it will work equally well here. To achieve the performance shown in this graph, output impedance of the amplifier must be zero; the filter must contain perfect components; be terminated with the load described; and the specified matching network must be in place. If these conditions are not true, **ALL BETS ARE OFF.**

A quick look at PWM amplifier data sheets will tell us actual output impedance can cause small errors if left unchecked. Use your knowledge of op amp theory and Figure 8 to see how closed loop output impedance of the PWM amplifier is extremely low just as with a closed loop op amp. On the left circuit we know output impedance is reduced by the loop gain. As long as the op amp in the

Filter Design for PWM Amplifiers READ ME — Using the Complex Load:

CAUTION! Refer to Applications Note 32

Input Data

Model	SA03			**Order Calculation**		
Vs	90	Volts		Atten. @ Fsw	41.023	db
Fsw	22.5	KHz	22.5	N(exact)	1.9513	
Fmin	0.001	KHz				
Fmax	2	KHz		N(recommended)	2	
Fcutoff	2	KHz				
Rload	10	Ohms		**Matching network**		
Cload	0	uF		Cm =	0	uF
Lload	0	mH		Lm =	0	mH
Vripple	1	Vpk		Rm =	10	Ohms
Signal	85	Units				
Sig as ?	V peak	Note/W				

60 Load All Data For N=1
61 Load All Data For N=2
62 Load All Data For N=3
63 Load All Data For N=4
64 Load All Data For N=5
83 Load All Data For N=6

Read Me
Yes Auto Sweep on Load?
Recommended Cleg = 0.3448 uF

Notes:

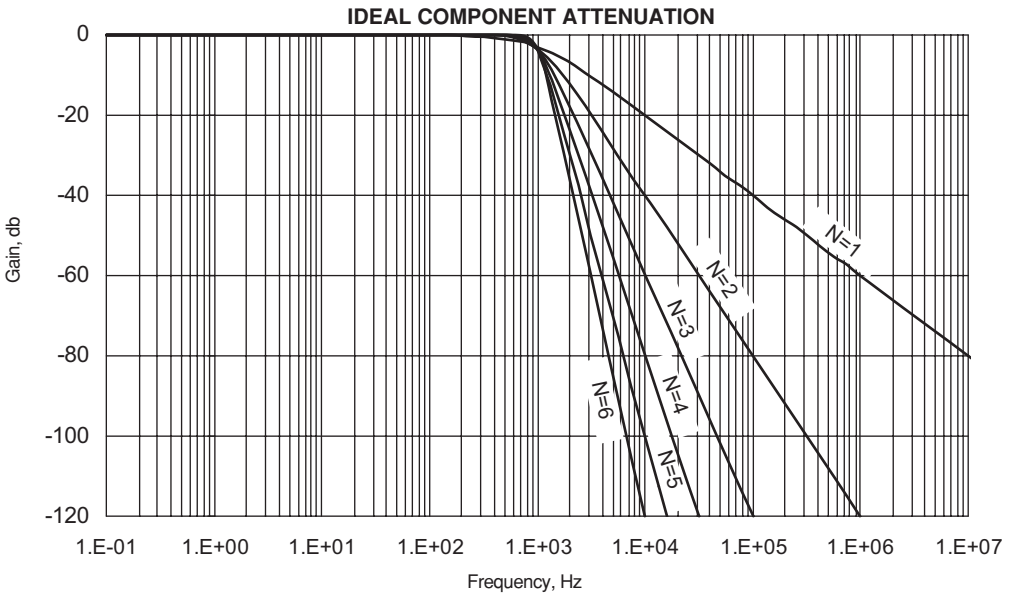
46 Print Filter
55 Show Attenuation in db & %
56 Show Attenuation Graph
66 Show Filter Components

FIGURE 5. PWM FILTER DESIGN DATA ENTRY SCREEN

Component Calculations Shading indicates values for Split Inductor topology

		Dual Cap Filter	Single-ended Filter
N = 1	L =	0.3979 mH	0.7958 mH
	P-P Iripple =	2.5133 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.6283	
N = 2	L =	0.5627 mH	1.1254 mH
	C =	11.254 uF	5.6269 uF
	P-P Iripple =	1.7772 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4443	
N = 3	L1 =	0.5968 mH	1.1937 mH
	C =	21.22 uF	10.61 uF
	L2 =	0.1989 mH	0.3979 mH
	P-P Iripple =	1.6755 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4189	
N = 4	L1 =	0.609 mH	1.2181 mH
	C1 =	25.102 uF	12.551 uF
	L2 =	0.4307 mH	0.8613 mH
	C2 =	6.0909 uF	3.0454 uF
	P-P Iripple =	1.6419 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4105	
N = 5	L1 =	0.6148 mH	1.2296 mH
	C1 =	26.967 uF	13.484 uF
	L2 =	0.5499 mH	1.0998 mH
	C2 =	14.235 uF	7.1174 uF
	L3 =	0.1229 mH	0.2459 mH
	P-P Iripple =	1.6266 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4067	
N = 6	L1 =	0.6179 mH	1.2358 mH
	C1 =	28 uF	14 uF
	L2 =	0.6179 mH	1.2358 mH
	C2 =	19.124 uF	9.562 uF
	L3 =	0.3016 mH	0.6031 mH
	C3 =	4.1189 uF	2.0595 uF
	P-P Iripple =	1.6184 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4046	

FIGURE 6. COMPONENT VALUES FOR DIFFERENTIAL AND SINGLE ENDED FILTERS



Attenuation in db							Percent attenuation						
500	-9.7E-01	-2.6E-01	-6.7E-02	-1.7E-02	-4.2E-03	-1.1E-03	5.0E+02	10.55728	2.98575	0.772212	0.194742	0.048792	0.012205
750	-1.9E+00	-1.2E+00	-7.1E-01	-4.1E-01	-2.4E-01	-1.4E-01	7.5E+02	20	12.84245	7.863584	4.658634	2.702074	1.547157
22500	-2.7E+01	-5.4E+01	-8.1E+01	-1.1E+02	-1.4E+02	-1.6E+02	2.3E+04	95.55994	99.80247	99.99122	99.99961	99.99998	100
225000	-4.7E+01	-9.4E+01	-1.4E+02	-1.9E+02	-2.4E+02	-2.8E+02	2.3E+05	99.55556	99.99802	99.99999	100	100	100
Hertz	N=1	N=2	N=3	N=4	N=5	N=6	Hertz	N=1	N=2	N=3	N=4	N=5	N=6

FIGURE 7. THE IDEAL ATTENUATION GRAPH AND PRECISE CHECKING OF POINTS OF INTEREST

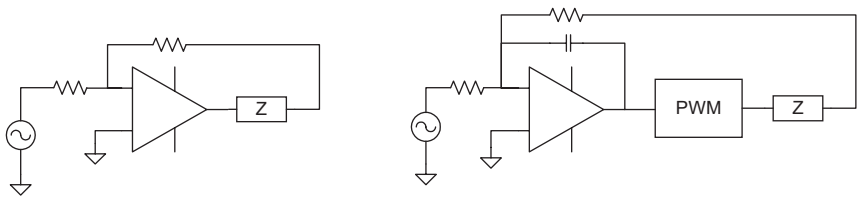


FIGURE 8. A PURE INTEGRATOR IS THE KEY TO ACCURACY

right circuit has no direct DC feedback, and the PWM block with its output impedance (typically ranging from 0.1Ω to 1Ω) is inside the feedback loop, closed loop output impedance will be reduced in the same fashion. With PWM amplifiers being relatively slow compared to op amps, it is easy to obtain high loop gains over the power signal bandwidth to achieve negligible errors in driving the filter. In actual PWM systems, the feed back loop is often much more complex than shown here.

Trying to approach the second "ideal" condition means most of the work still lies ahead in finding components which work as advertised in the MHz range and whose losses won't radically change the pretty graphs. An electrolytic capacitor may perform very well at 60Hz, but rather poorly at 6MHz. If temperatures allow, switching to tantalum should result in a noticeable high frequency improvement. Moving to switching rated plastic capacitors or ceramic capacitors is usually an even better choice.

Not many of us would attempt using laminated steel core inductors here, but please note that not all "high frequency" coils are created equal. Air core inductors get away from the magnetic saturation problem and they have fewer tendencies to become dummy loads at high frequency. The down side will be more turns of wire and more copper losses. When adding a magnetic core, make sure the material can handle the high frequency components of the square wave (manufacturers often rate frequency capability for only sine waves) at the switching frequency and can accommodate the flux density of the peak currents to be delivered.

Pressing one of the "Load All Data" buttons on the PWM Filter sheet transfers your application to the PWM Power sheet. Starting on the left of Figure 9 we find single-ended components for up to a sixth order filter have been entered. Next we find the matching network. On the far right you will find the simple three-element load specified on the PWM Filters sheet plus space to model a more complex load. Parasitics for the filter components have all been zeroed.

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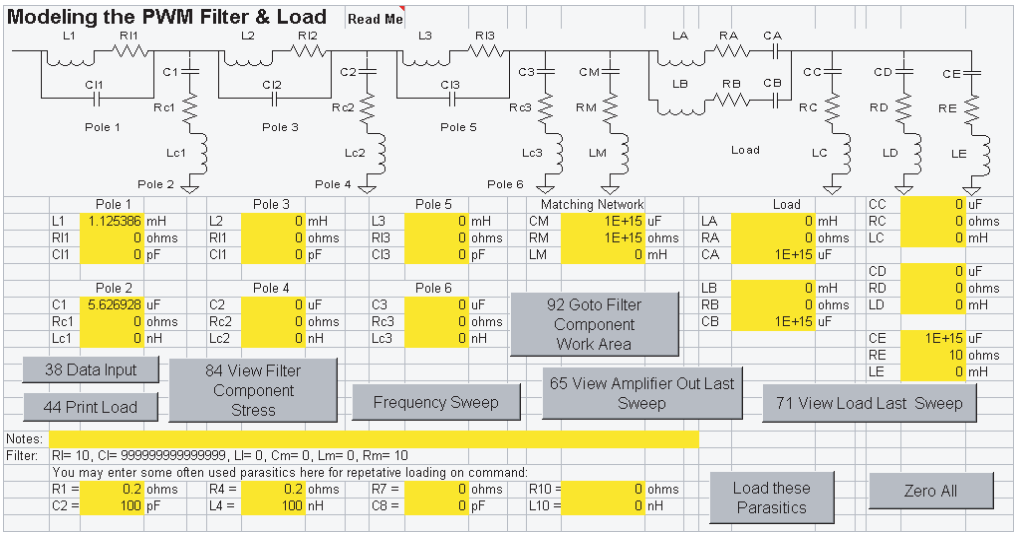


FIGURE 9. LOADING APPLICATION DATA FROM THE FILTER SHEET TO THE POWER SHEET

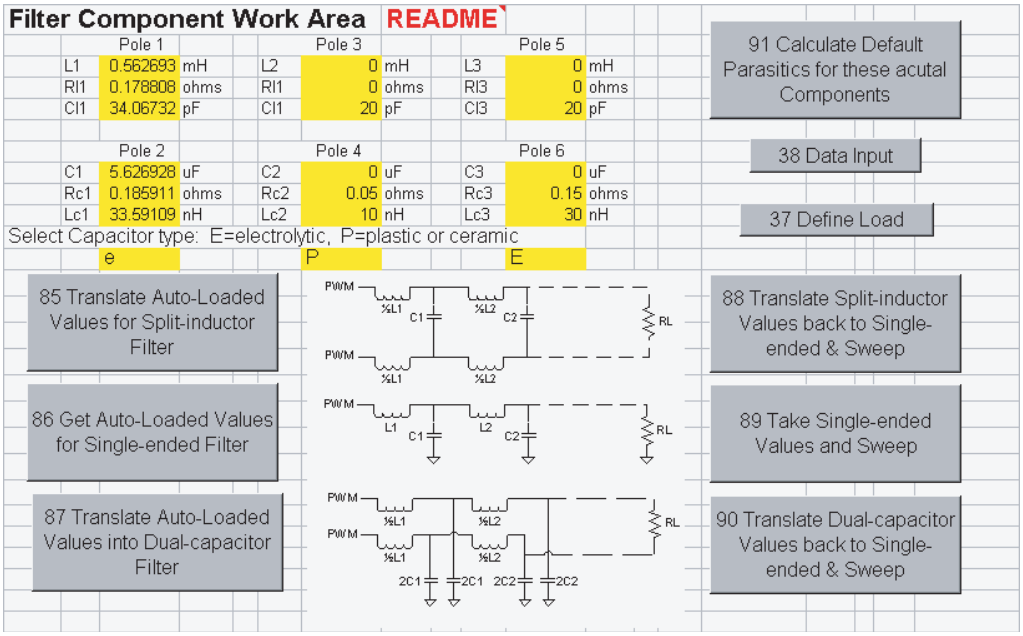


FIGURE 10. TRANSLATION BETWEEN FILTER TOPOLOGIES AND DEFAULT PARASITIC CALCULATION

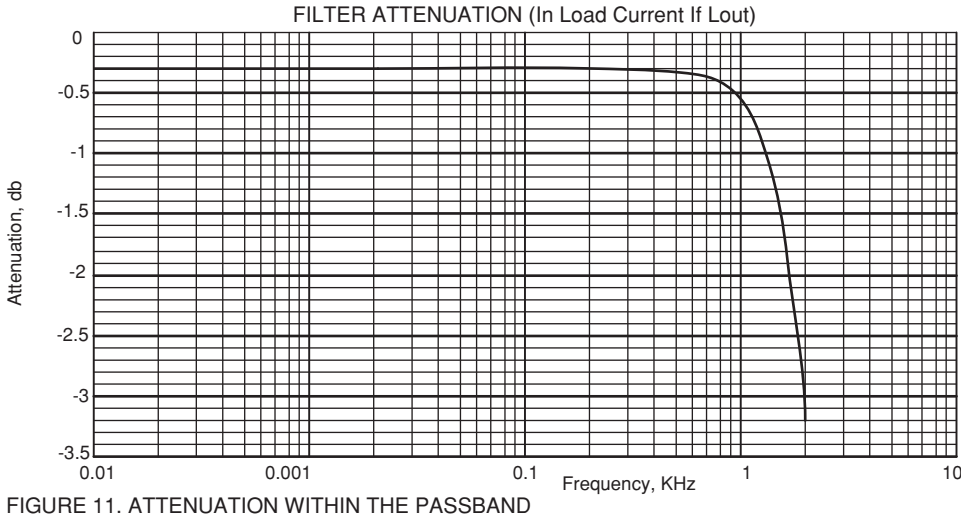


FIGURE 11. ATTENUATION WITHIN THE PASSBAND

The sweep function handles only single ended filters, but Figure 10 shows the area where these component values can be translated into values for either split-inductor or dual-capacitor designs. While there is absolutely no substitute for finding real parasitic values for filter components, button 91 provides a default parasitic calculator for first pass design efforts. Notice the cells where capacitor type can be selected individually for all three capacitors. Parasitics vary WILDLY form part to part. The default calculator is ONLY intended to get somewhere in the ballpark. These defaults are reasonable for parts suitable for switching applications. Your real parts could be better, but could easily be much worse. Consult manufacture's data sheets or measure the parts to get accurate data for subsequent analysis. Values of purchased components and their real parasitics should be entered directly into the yellow cells and then be translated with button 88, 89, or 90.

This picture is part of the result of loading our sample application from the PWM Filter sheet (no auto sweep); going to the Filter Component Work Area with button 92; translating component values for a split-inductor design with button 85; and calculating default parasitics with button 91. Button 88 will translate prime component values and the parasitics back to single-ended equivalents and then run the frequency sweep to calculate critical voltages, currents, powers and phase angles over the frequency range we specified. 100 frequency points will be examined. If this takes less than 10 seconds, you should be proud of your computer. If it takes more than a minute ------. Frequency sweep requires Analysis ToolPak. If you see cells with #NAME? or a runtime error, try TOOLS, ADD-INS, Analysis ToolPak and then do the sweep.

Figure 11 shows attenuation of signal frequencies is close to the ideal except the entire curve is about 0.3db lower than expected. This drop is due to inductor resistance. We learned earlier that the extremely fast transition times of the PWM amplifiers means high frequency content is powerful well into the megahertz range. To check performance in this range; go to the data input screen; enter the cutoff

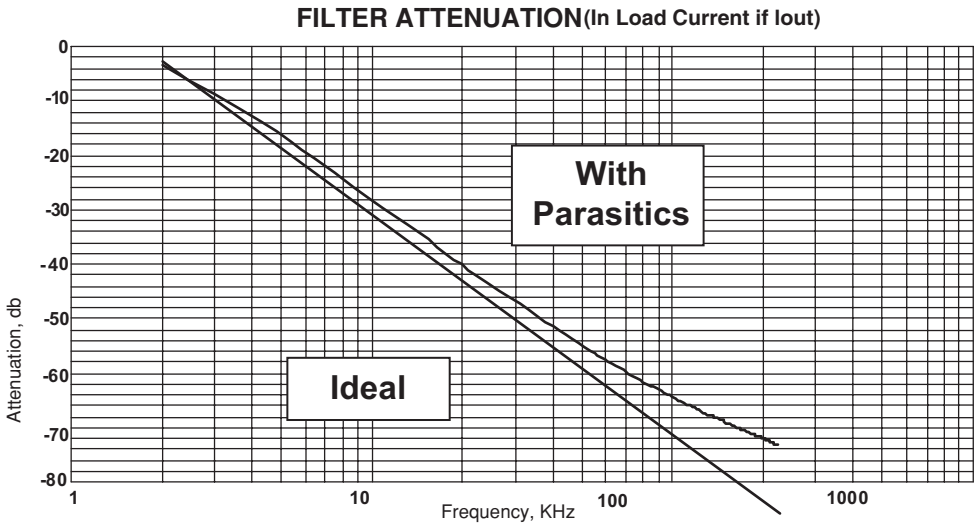


FIGURE 12. SMALL PARASITICS CAUSE A LARGE DEPARTURE FROM THE "IDEAL" PICTURE AT HIGHER FREQUENCIES

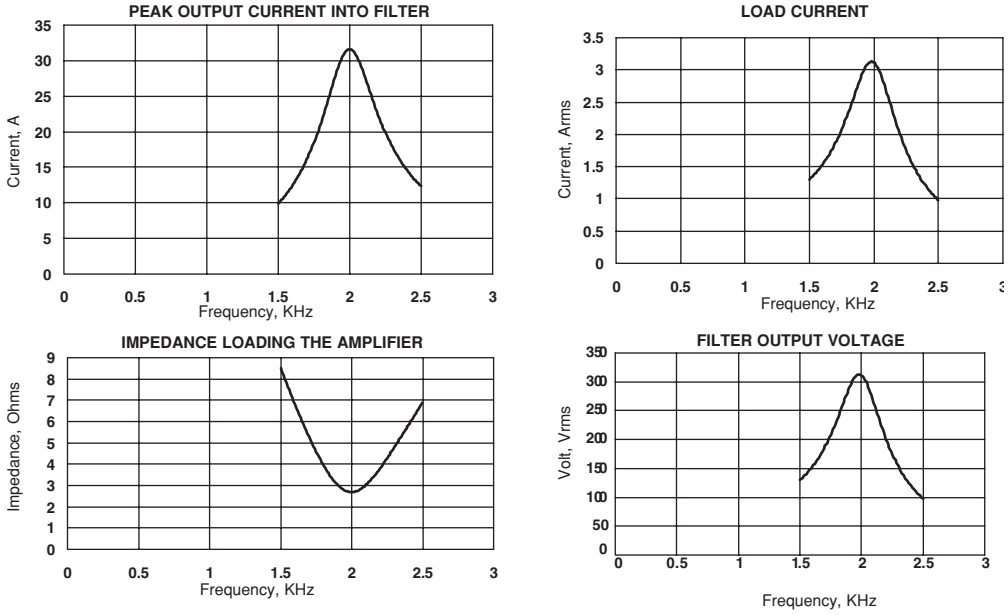
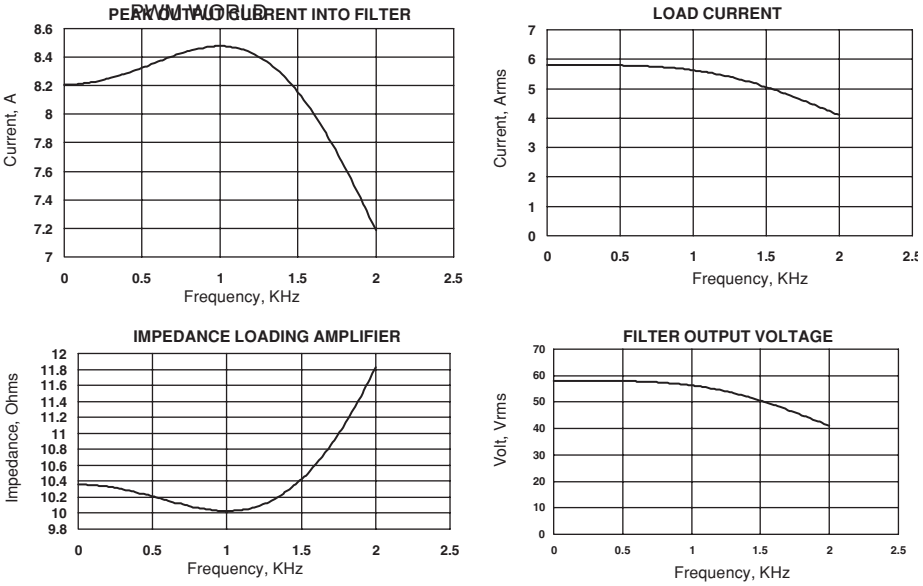


FIGURE 13. A GOOD PROCEDURE FROM THE LINEAR WORLD MAY BE DANGEROUS IN THE PWM WORLD



frequency as Fmin; and at least the tenth harmonic of the switching frequency as Fmax; and rerun the sweep. The graph in Figure 12 tells us spike content at the filter output is far from ideal. An ideal second order filter for this example has about 82db attenuation at 225KHz, but parasitics reduce this figure to about 73db, or roughly a factor of 3 less attenuation with electrolytic capacitors in this dual-capacitor design. Is this OK? Or should we spend more time looking for better filter components? Or should we consider one of the other two topologies which will perform better at high frequencies?

So, you're an old hand with linear power circuits. You fire up the prototype with a light load to make sure everything is working before connecting the real load.

While this procedure is commendable for linear drives and may work fine for a PWM drive, watch out for tuned circuits in the filter/match network/load. Replacing a designed 10 ohm/1mH load with a 100 ohm purely resistive load (matching network removed), produces the graphs of Figure 13. At the 2KHz cutoff frequency, impedance presented to the amplifier drops to ~2.7 ohms, peak current tops 30A, load voltage is ~313V and load current is 3.1A. 970W delivered to the light 100 ohm load!

Be careful! Deadly voltages easily generated.

The second order filter driven at the designed cutoff frequency, with no load, is a series resonant circuit which presents a theoretical zero impedance to the amplifier and develops a theoretical infinite voltage at its center. Higher order filters generally produce lower amplitude peaks at lower frequencies relative to the cutoff frequency.

The very nature of PWM amplifiers demands reactive elements be driven. Inductance is mandatory and capacitance is very common, meaning resonance will exist. A properly designed and terminated filter will yield a response close to the text

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book curve. The trick is to design the circuit to accommodate load variations and possibly certain fault conditions such that these conditions will not place undue stress on components or produce extreme high voltage hazards.

Figure 14 shows the well behaved performance of this example modified for a 10Ω purely resistive load. At DC, impedance loading the amplifier is the sum of the load and the parasitic 0.36 ohms of the filter inductor(s). The amplifier sees about a 3% impedance dip at mid-band and drives a corresponding peak output current. This is normal and Power Design will search for these peaks and dips when calculating heatsink requirements.

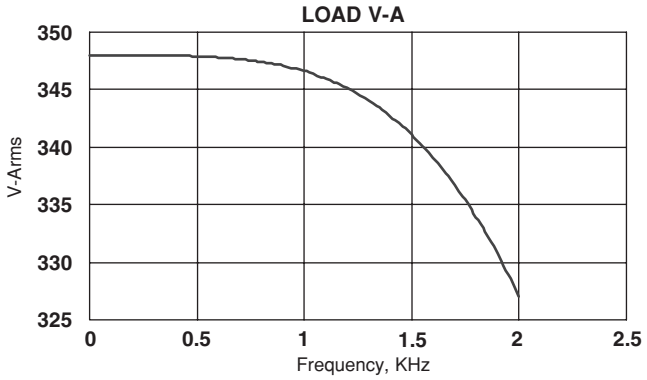

FIGURE 15. DOUBLING Fc YIELDS INCREASED OUTPUT POWER

While this operation is proper, is it what you wanted? The cutoff frequency of the filter is where the load voltage is down 3db. Does -3db equal .707 or .5? Both, .707 applies to the voltage and the current ratio but .5 is correct for the power ratio. In this example output power drops form 337W at DC to 172W at 2KHz. Many times half power at maximum frequency is not acceptable. This is why some designers routinely start their filter calculations using a cutoff frequency twice the required maximum signal frequency of the application.

Doubling the design cutoff frequency of the filter enables the circuit to deliver a lot more power at the desired 2KHz as shown in Figure 15. This is still a 2 pole filter and power loss is only about 6% at 2KHz. As an added benefit, inductors for a 4KHz filter are half the value of those for a 2KHz filter and likely will have substantially lower parasitic resistance.

Yes, you could double again to achieve an even flatter pass band. No, there is no free lunch. Every time you move cutoff frequency up, you allow more switching frequency power in the load. Yes, you can add more poles to the filter. Analyze as many combinations as you wish, it won't take long. The question becomes one of cost in terms of money, extra loss in the filter, size and weight.

Speaking of properly terminated filters, we need to look closely at the matching network. While the conjugate matching network performs almost like magic in terms of forcing the attenuation graph to approach text book shape, there is a cost involved. This cost is slight when the load is mostly resistive, but the power dissipated in this network approaches power delivered to the load as the load approaches pure reactance.

The graphs of Figure 16 are for an application driving a 1uF piezo stack with 12 ohms series resistance, to 75V peak from 1KHz to 20KHz. The second order filter cutoff frequency was designed for 40KHz providing a quite flat response. The V-A output falls at low frequency because the load impedance is increasing. To keep filter termination impedance flat, the matching network impedance moves in the opposite direction, giving rise to large power levels in the matching network resistor, especially at low frequencies. As this power is not delivered to the load, efficiency is far from the desired level.

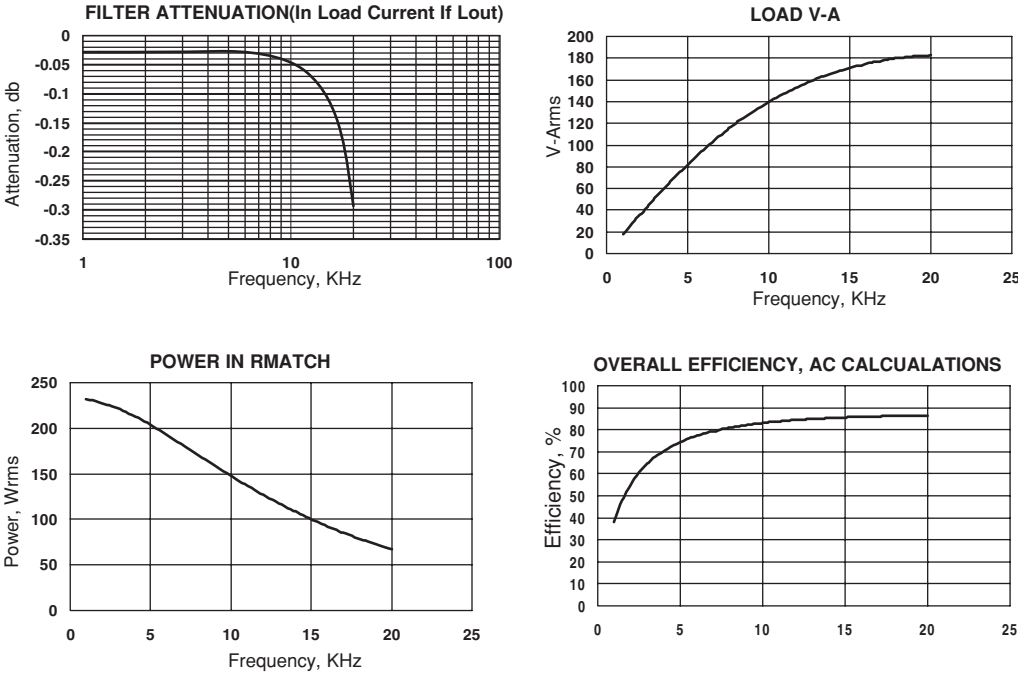

FIGURE 16. PERFORMANCE OF THE PROPERLY TERMINATED FILTER

Upon seeing this power loss, some designers immediately want to see what happens if they simply remove the matching network. With no matching network we cannot lose this power, but this leaves the filter with an improper termination. This would result in a unwanted resonant circuit causing almost 4db peaking as shown in Figure 17. In terms of V-A in the load near the upper end of the band, power goes from ~180 to over 450V-A. If you wish to see more on this subject, use the Filter Hazard on the Power Design Examples sheet. Comments explain each situation and a macro sets up and runs the analysis.

Here lies part of the beauty of the Power Design tool; investigating possible compromise circuits is a snap. See Figure 18 for results of doubling the resistor value in

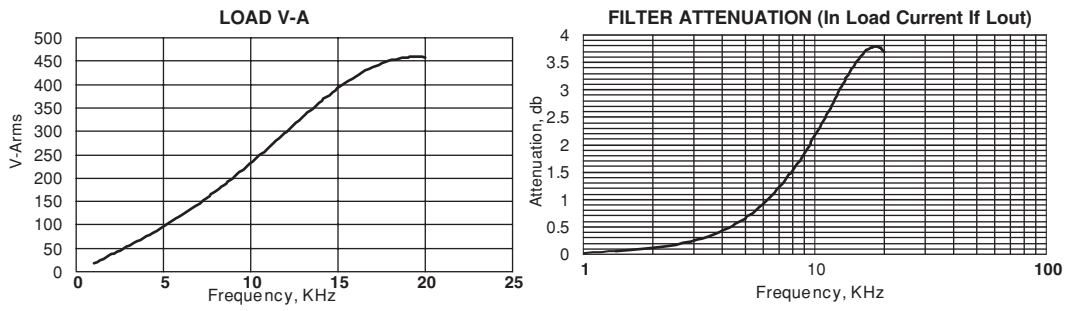

FIGURE 17. THE BAD NEWS IF THE MATCHING NETWORK IS OMITTED

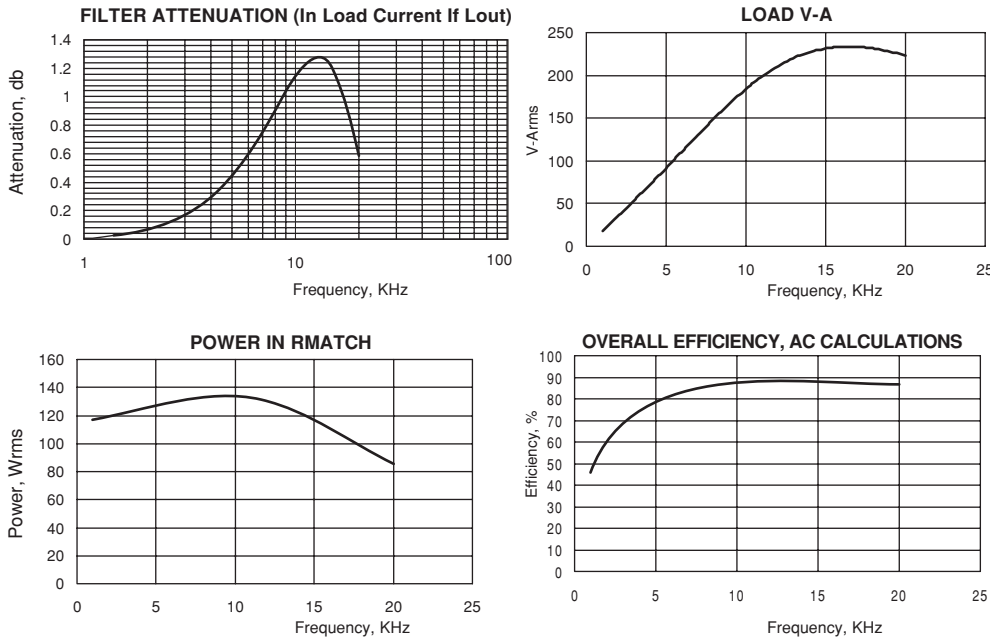

FIGURE 18. RESULTS OF A MODIFIED MATCHING NETWORK

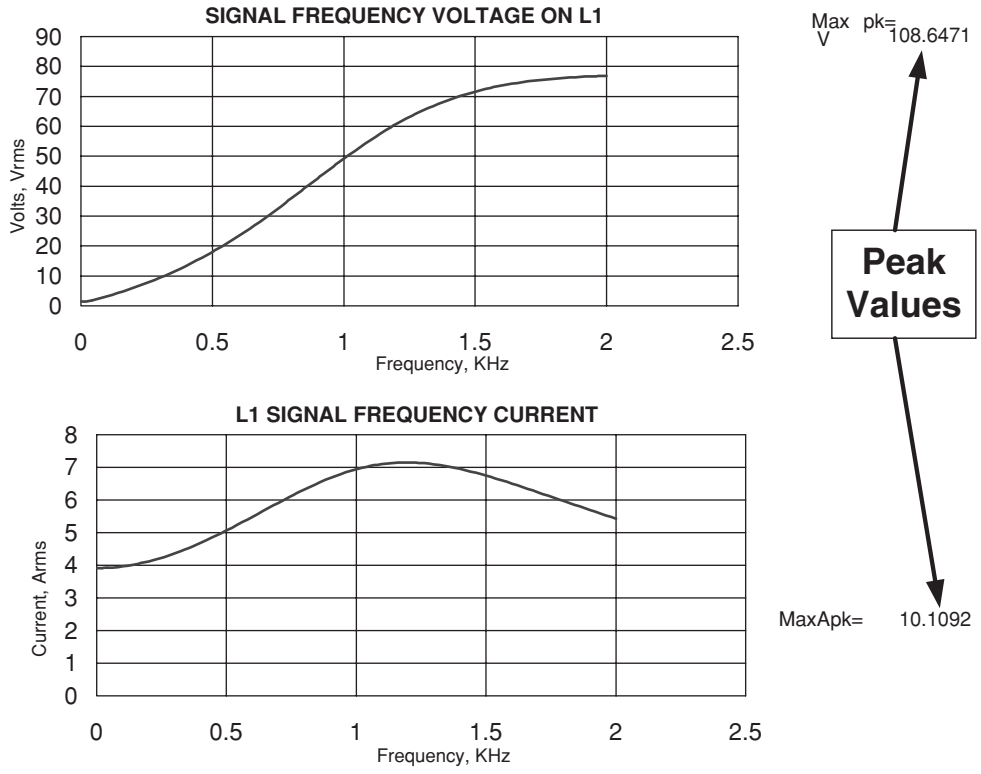

FIGURE 19. STRESS LEVELS ON L1

the matching network which may provide a workable compromise. Peaking at the load is down substantially from not using any network and wasted power is down substantially from using the ideal network.

DETERMINING FILTER COMPONENT STRESS LEVELS

This section uses the original coil driver example, with the second order filter designed for cutoff frequency=2KHz; load resistance=10Ω; and load inductance=1mH. However, we are assuming the load has gotten hot and the resistance has gone up to 15Ω. This change affects all the performance graphs covered so far and they should be checked. Power Design calculates voltage and current stress levels on L1 and L2, plus C1 and C2 for all designs. Resonance of these filters can produce voltages and currents larger than the load levels. Button 84 will place the first graph on the screen, then scroll up and to the right to view other graphs. The currents shown in Figure 19 can be used directly for all filter topologies. If L1 is actually two inductors, half the voltage shown will be across each individual inductor. Note that our circuit example only has a 90V supply; the drive signal is only 85Vpk; the load resistance is 15Ω; but L1 has current peaks of 10.1A and voltage peaks of 108V.

In Figure 20, we find that in addition to the switching frequency current, C1 has 3A flowing at 1.6KHz. Three peak voltages are given; 96Vpk for a differential capacitor; a positive peak of 93V for a grounded capacitor; and a negative peak of -3V. Any time the negative peak is below ground, the warning to use bipolar capacitors also appears.

PHASE ANGLES AT THE LOAD

These filters are notorious for introducing large phase shifts. This is usually not a problem when feedback is taken directly at the output of the PWM amplifier. In applications such a servo loops, feedback is taken after the filter and any phase shift introduced here affects system phase margin. Figure 21 shows both voltage and current phase in the load for this example.

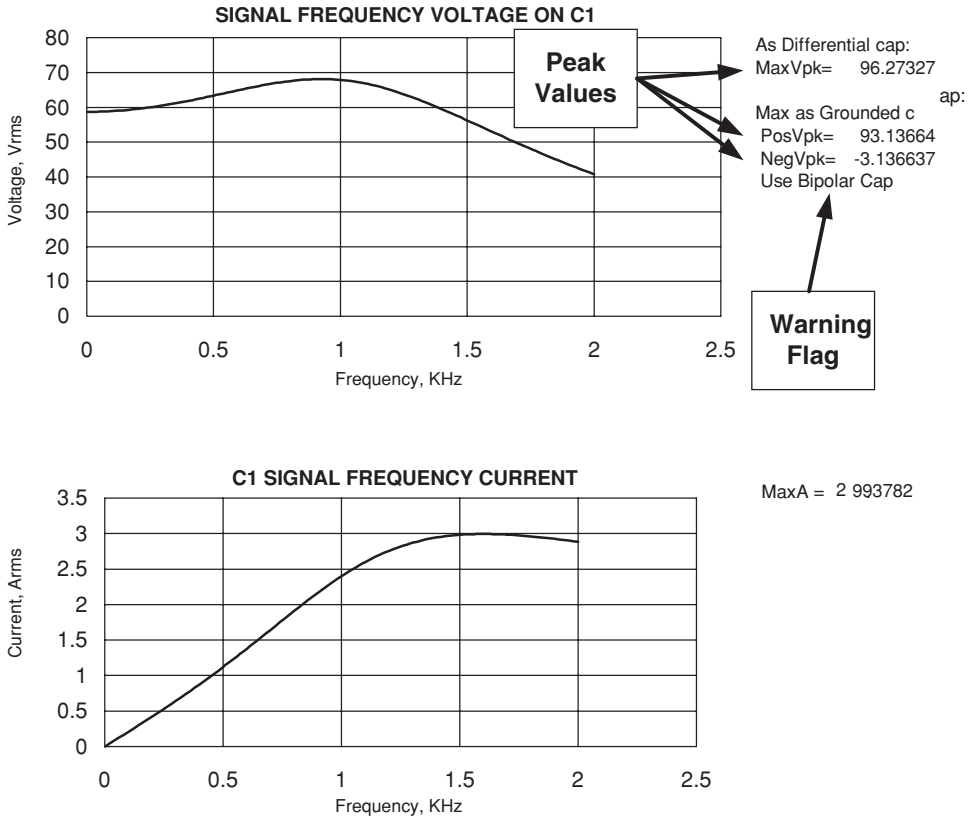

FIGURE 20. STRESS LEVELS ON C1

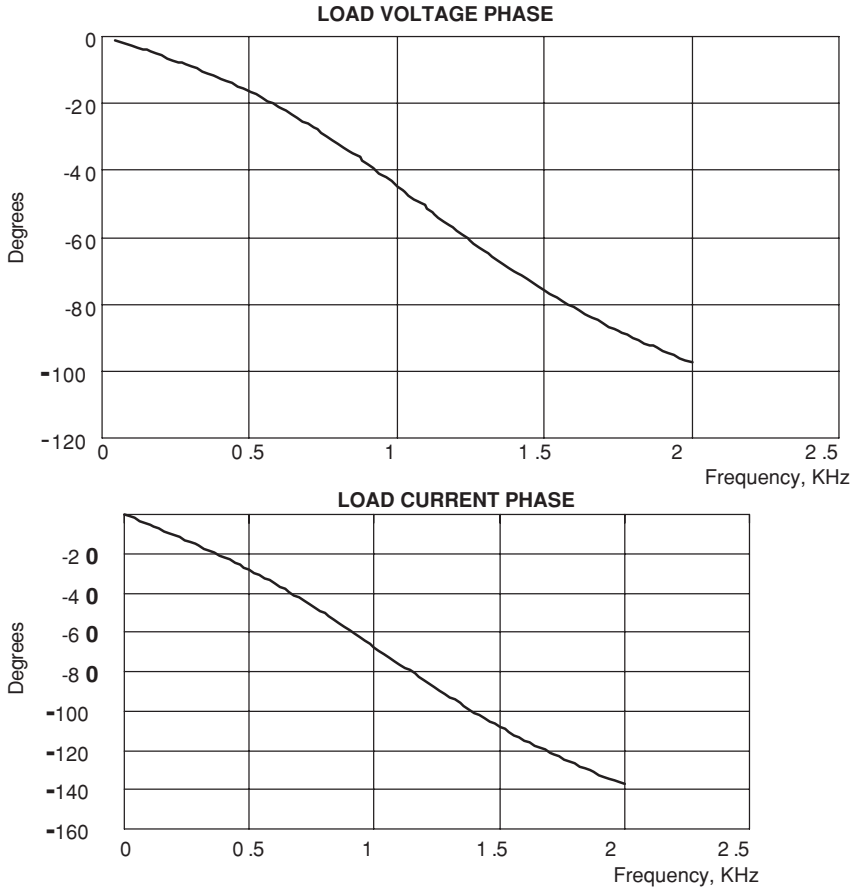

FIGURE 21. VOLTAGE AND CURRENT PHASE IN THE LOAD

This phase shift is reduced as the ratio between Fmax and Fcutoff frequencies widens, and is lower with lower order filters.

CALCULATING INTERNAL POWER DISSIPATION FOR PWM AMPLIFIERS

Heatsink selection for most PWM amplifiers is more complex than for a linear amplifier because FET ON resistance (and hence voltage drop, internal power and dissipation) increases roughly 2:1 as junction temperature goes from 25°C to 150°C. PWMs have the same concern over temperature vs. life expectancy as linears, but changes of circuit performance over temperature are much more pronounced than with linear amplifiers.

For a first order estimation of power dissipation in the PWM, simply multiply the output current (a given application requirement) and the voltage drop at that current (read from a graph on the product data sheet). This points out the PWM advantage over linear power delivery; supply voltage is not part of the equation. With a first order approximation, the voltage drop divided by supply voltage yields efficiency (quiescent current of both Vcc and Vs will reduce this a little). Unfortunately, first order approximation is not good enough unless you have the luxury of using overkill amplifiers and massive heatsinks.

Looking a little deeper, there are two points of confusion. First, the voltage graph offers multiple curves based on various case temperatures. We know cooler is better for life expectancy and efficiency, but there are no rules regarding which one to choose. Something not presented in any direct way is the second problem: methods to calculate junction temperature are not given. This is a parameter every power designer should know and it is often specified by contract.

While the linear Power sheet simply provides you with a minimum heatsink rating, the PWM Power sheet gives you graphs of junction temperature, internal dissipation and efficiency. With this data, you can make intelligent tradeoffs concerning circuit operation vs. investment in the heat removal system.

Our exercises on filter design have already taken us to the PWM Power sheet. From numerous locations you can use command button 38 to see the Data Input screen as shown in Figure 22. The green input cells are normally filled in with one of the Load Data command buttons on the PWM Filter sheet. These values may be changed at will but neither the graphs nor circuit parameters in the blue cells will necessarily be valid until a Frequency Sweep has been run.

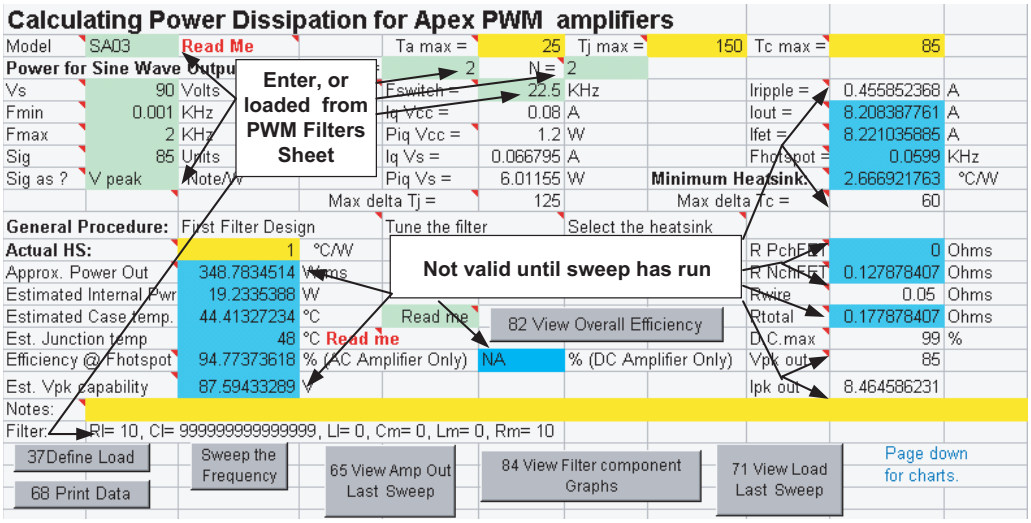

FIGURE 22. THE PWM POWER SHEET DATA INPUT SCREEN

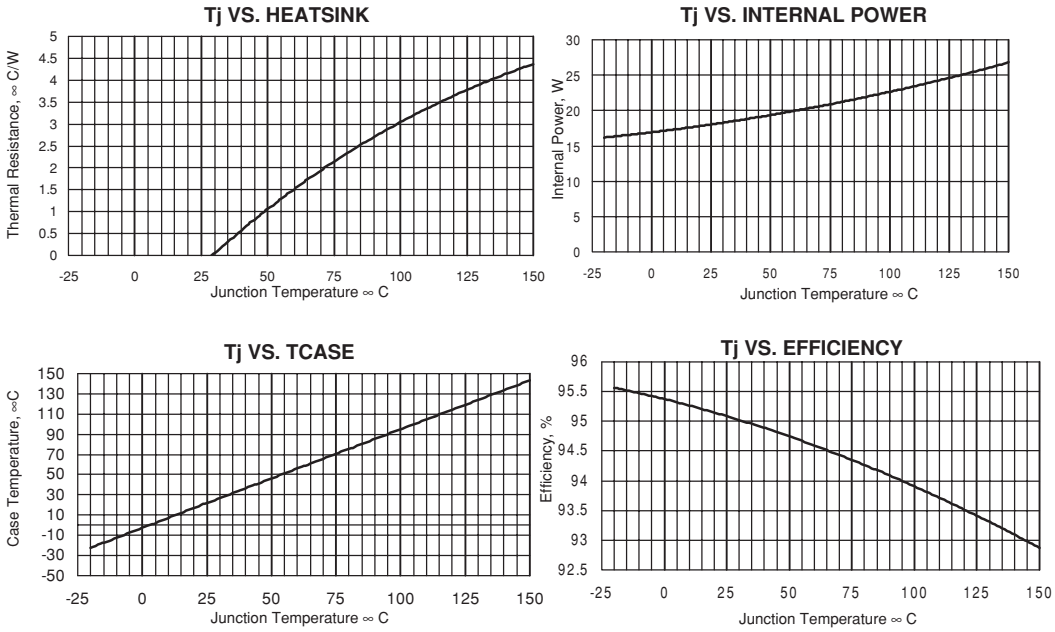

FIGURE 23. SELECTING A MAXIMUM JUNCTION TEMPERATURE IS THE KEY STEP

In the center area, find data on quiescent current and resulting power dissipation. Data for these calculations comes from application parameters and the built-in database containing information on quiescent current variations with supply and switching frequency. In the upper right, applying a sine wave at the switching frequency and using a correction factor have approximated ripple current. If the filter and load are close to those entered in the Filter sheet, this ripple approximation will be close to ripple predicted by the Filter sheet. Hotspot frequency is the frequency where load current is producing the highest junction temperature. This is not necessarily coincident with the frequency producing the highest peak current. Consider the case of a DC current of 10A rising to 11A peak at 1KHz. At 1KHz heat generation is alternating between pairs of transistors fast enough to find them running cooler than at a steady state level of 10A.

The Iout cell will report amplifier output current at signal frequencies using peak values for hotspot frequencies below 60Hz or RMS values at higher frequencies. The Ifet cell is the RMS addition of the ripple current (at the switching frequency) and the output current. If hotspot frequency is 60Hz or more, ripple current is reduced 30% because ripple decreases as duty cycle increases (there is no ripple at 100%). The Minimum Heatsink is the thermal rating which will keep both the case temperature and the junction temperature within the boundaries entered at the top of the screen.

Continuing down on the right side are On resistances of the H-bridge switches at the hotspot frequency. The P channel number will be for one FET if P channel devices are used in the amplifier. If this is the case, the N channel number will also be for one FET. When only N channel FETs are used, this number will be for two FETs. If you specify a heatsink that will not keep junction temperatures below the specified maximum, both FET resistances will be forced to 10 ohms. Rwire represents internal conductor losses in the amplifier and Rtotal adds it all up. For amplifiers using IGBTs, all resistance cells will be blank.

Most PWM amplifiers can hold their output switches in one state. To rephrase, PWM amplifiers can be driven to zero or 100% duty cycle; however, propagation delays and dead time requirements limit the linear modulation range to less than these levels. D.C.max is the maximum percentage of the power supply voltage delivered before encountering the non-linear jump to being latched in one state. Vpk out and Ipk out are from anywhere between Fmin and Fmax.

Back on the left side under Actual HS, Approx. Power Out is the power factor corrected VA output directly at the amplifier at the hotspot frequency. If you really intend to look at DC or want a peak value, multiply by two. Estimated Internal Pwr includes losses due to driving the load and the quiescent power.

Efficiency of a DC power supply would compare DC, or peak power out, to input power. Efficiency of an audio amplifier would likely compare RMS power out to input power. These two approaches to efficiency will produce different answers for the same amplifier, driving the same peak current from the same power supply. Power Design always calculates an efficiency based on the AC thought process but will give you a DC based answer only if both Fmin and Fmax are less than 0.003 (remember to Sweep before reading the answer). In both cases, the numbers appearing here do not include filter loss. Est. Vpk capability subtracts internal losses and duty cycle limitations from the supply voltage.

Not shown in Figure 22 are four data dependent red warning flags. The first warning appears if the Actual HS is too small to maintain either specified case temperature or junction temperature. If Est. Vpk capability is less than the signal voltage, the next flag will become visible. The third flag warns of output current beyond the peak rating of the amplifier. The last flag concerns application supply voltage compared to amplifier ratings.

We know many of these numbers are a moving target relative to selection of the actual heatsink rating. Refer to Figure 23 for this important step. All heatsink references assume fresh thermal grease has been properly applied or an Apex thermal washer has been used.

In the upper left graph it looks like a quite small heatsink will keep junction temperatures below the maximum of 150°C specified by almost all PWM amplifiers. However the graph below says there is little difference between junction and case temperature and we surely want to keep case temperature much lower than 150°C.

On the top right we see that internal power dissipation of the amplifier changes with junction temperature. Settling for the minimum heatsink size instead of investing in a 1°C/W heatsink (easy to do without a fan) will increase internal power almost 8W or nearly 40%. Below we see this same effect expressed in terms of efficiency. At first, moving only a few percentage points may not seem like much, but remember these points are relative to a quite large power level. Enter 100 as the Actual HS if you plan to not use a heatsink. More likely, a rating will come from the Heatsink sheet of Power Design, a manufacturer's data sheet, or your own design efforts.

The efficiency graphs above refer to performance only at the hotspot frequency and do not include filter losses. Figure 24 however, includes losses in the filter and matching network and provides frequency data. The curve is based on the AC thought pattern discussed earlier, input power compared to RMS power delivered. If there is a glitch at 60Hz, it is due to the instant change (mathematically) from peak power heating effect to RMS power heating effect. Fig. 24. Including filter losses in the big picture.

CONCLUSION

The Power Design tool is even more important to the PWM designer than the linear designer. PWMs are not as widely understood and worse yet, literature is not as widely available. The comments and automated examples built into this spreadsheet serve well as a text on the subject. PWMs also tend to require more iteration to approach an optimum design and are more frequency sensitive than linears. Again, tackling all this with computer aided design is the only way to go and the tasks of filtering and heatsinking are better handled by Power Design than by many Spice machines.

Not to harp on it, but do not let all this quick and easy data lead you into the trap of accepting theory with a smile while sticking your head in the sand when it comes to the hardware world and parasitics. And one more time: Without case temperature measurements, your design effort is NOT complete!

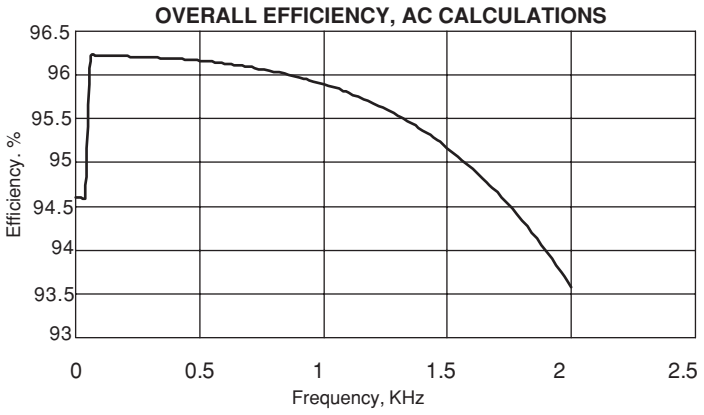

FIGURE 24. INCLUDING FILLER LOSSES IN THE BIG PICTURE