



Designed to Help You Boost Your Analog Design Power

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PWM Amplifiers \propto Power Op Amps

Power Integrated Circuits with Technical Support

Since 1981, Apex has been designing and manufacturing hybrid (chip and wire) power amplifiers. Careful attention to process development and control has made Apex the world leader in hybrid power. The products consistently perform per the data sheet. The product line now boasts the highest current, the highest voltage and highest wattage hybrids to be found anywhere in the industry.

The expertise in handling large power levels electrically and thermally has been adapted to high reliability DC-DC converters. Unique construction techniques make these converters especially impervious to demanding environmental conditions. The Apex design philosophy provides converters with no de-rating over their entire operating temperature range.

Pulse Width Modulation (PWM) amplifiers share the same reliability as their linear counterparts but utilize switching technology to greatly extend the delivered power range while keeping wasted heat in the same area as the linears.



The present Apex facility is 55,000 sq. ft. on ten acres zoned such that we can double our size. Current sales are about \$14M and we can do \$25M in this building. Almost half the area and third the cost of the building are clean room related. This class 100,000 clean room keeps the ICs clean.

Apex extends an invitation to you all to visit us and take a tour of our home to see first hand how we design and manufacture the world's best power integrated circuits.



- Total Quality Management
- Certified Mil-Std-1772 in 1989
- Certified ISO9001 in 1994

Sigma Plus has led to consistent increases in quality and performance for Apex and our customers. *Sigma Plus*, our Total Quality Management program, continues to produce measurable quality improvements, a culture based on teamwork, and increased value for our customers.

In alignment with *Sigma Plus*, we have instituted training and development in the fundamentals of our business, further supporting Apex teams with the tools they need to perform at high productivity and quality levels. With a firm foundation of *Sigma Plus* quality tools that solve the “how” of continuous improvement, team members are now learning the “why” with Open Book Management. As a result, Apex teams are gaining greater understanding of their personal impact on organizational systems and how they can directly improve organizational performance. By giving team members a stake in the outcome, they gain personal satisfaction and ownership of the products and services they provide to you, our customers.

We will continue to improve our systems and processes to exceed our customers' expectations. Feedback systems that identify internal and external customers' needs and expectations keep Team Apex focused on customer value. Team members have increased their job skills and have become functionally cross-trained to quickly adapt to changes that anticipate customer needs.

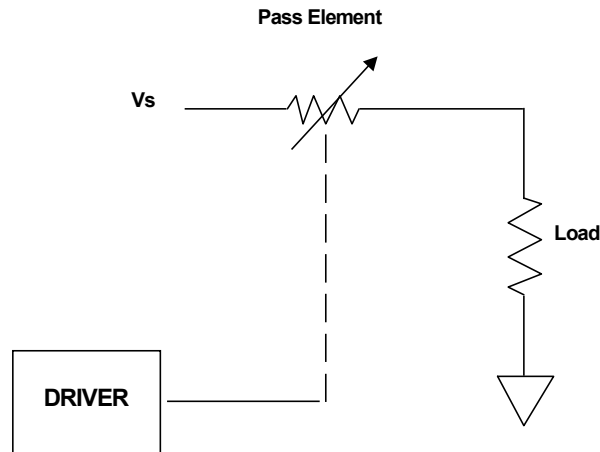
PWM

Pulse Width Modulation

- More Work
- Less Waste

As delivered power levels approach 200W, sometimes before then, heatsinking issues become a royal pain. PWM is a way to ease this pain.

LINEAR POWER DELIVERY

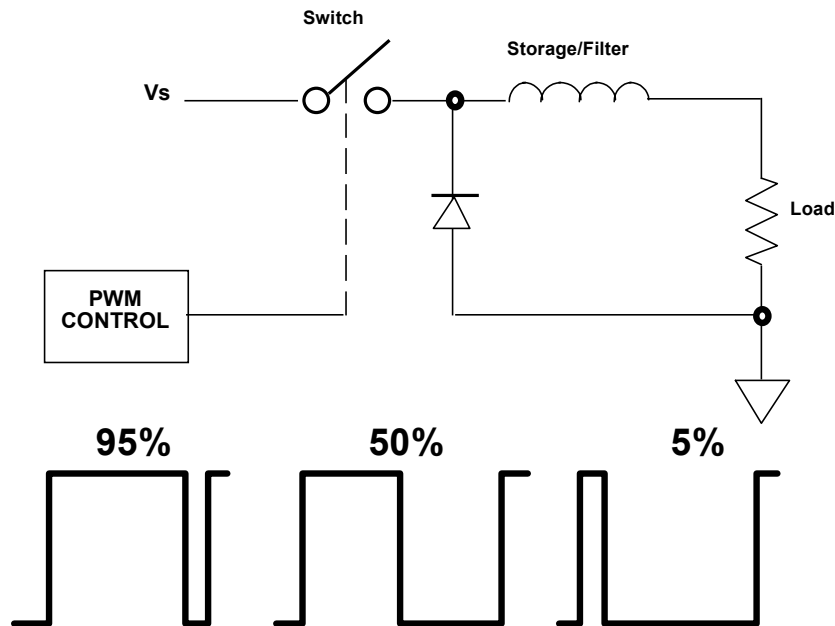


As power levels increase the task of designing variable drives increases dramatically. While the array of linear components available with sufficient voltage and current ratings for high power drives is impressive, a project can become unmanageable when calculation of internal power dissipation reveals the extent of cooling hardware required. Often the 20A drive requires multiple 20A semiconductors mounted on massive heatsinks, usually employs noisy fans and sometimes liquid cooling is mandated.

This slide illustrates the linear approach to delivering power to the load. When maximum output is commanded, the driver reduces resistance of the pass element to a minimum. At this output level, losses in the linear circuit are relatively low. When zero output is commanded the pass element approaches infinity and losses approach zero. The disadvantage of the linear circuit appears at the midrange output levels and is often at its worst when 50% output is delivered. At this level, resistance of the pass element is equal to the load resistance which means heat generated in the amplifier is equal to the power delivered to the load! We have just found the linear circuit to have a maximum efficiency of 50% when driving resistive loads to mid-range power levels. When loads appear reactive, this efficiency drops even further.

Ref. AN30

PWM POWER DELIVERY



These figures illustrate the most basic PWM operation. The PWM control block converts an analog input level into a variable duty cycle switch drive signal. If high output is commanded, the switch is held on most of the period. The switch is usually both on and off once during each cycle of the switching frequency, but many designs are capable of holding a 100% on duty cycle. In this case, losses are simply a factor of the on resistance of the switch plus the inductor resistance. As less output is commanded, the duty cycle or percent of on time is reduced. Note that losses now include heat generated in the flyback diode. At most practical supply voltages this diode loss is still small because the diode conducts only a portion of the time and voltage drop is a small fraction of the supply voltage.

The job of the inductor is both storing energy during the off portion of the cycle and of filtering. Inductors make their living by demanding continuous current flow; they become the energy source during the off time. In this manner the load sees very little of the switching frequency, but responds to frequencies significantly below the switching frequency. When the load itself appears inductive, it is often capable of performing the filtering itself.

With the PWM circuit, the direct (unfiltered) amplifier output is either near the supply voltage or near zero. Continuously varying filtered output levels are achieved by changing only the duty cycle. This results in efficiency being quite constant as output power varies compared to the linear circuit. Typical efficiency of PWM circuits range from 80 to 95%.

Ref. AN30

CONTRASTING DISCRETE LINEAR, HYBRID LINEAR AND HYBRID PWM 1KW DESIGNS

	Discrete Linear	Hybrid Linear	Hybrid PWM
Wasted Heat	500W	500W	100W
\$/Year ¹	\$438	\$438	\$88
Package Count ²	8 x TO-3	2 x PA03	1 x SA01
Heatsink	0.11°C/W	0.11°C/W	.55°C/W

Almost all power amplifiers (low duty cycle sonar amplifiers are a notable exception) must be designed to withstand worst case internal power dissipation for considerable lengths of time compared to the thermal time constants of the heat sinking hardware. This forces the design to be capable of cooling itself under worst case conditions. Conditions to be reckoned with include highest supply voltage, lowest load impedance, maximum ambient temperature, and lowest efficiency output level, and in the case of reactive loads, maximum voltage to current phase angle.

Consider a circuit delivering a peak power of 1KW. A 90% efficient PWM circuit generates 100W of wasted heat when running full output, and around 50W driving half power. The theoretically perfect linear circuit will generate 500W of wasted heat while delivering 500W. Table 1 shows three possible approaches to this type design. In all three cases it is assumed ambient temperature is +30°C and maximum case temperature is +85°C. It also assumes power ratings of the TO-3 devices to be 125W each. Heatsinks for linear designs require multiple sections mounted such that heat removed from one section does not flow to other sections.

Ref. AN30

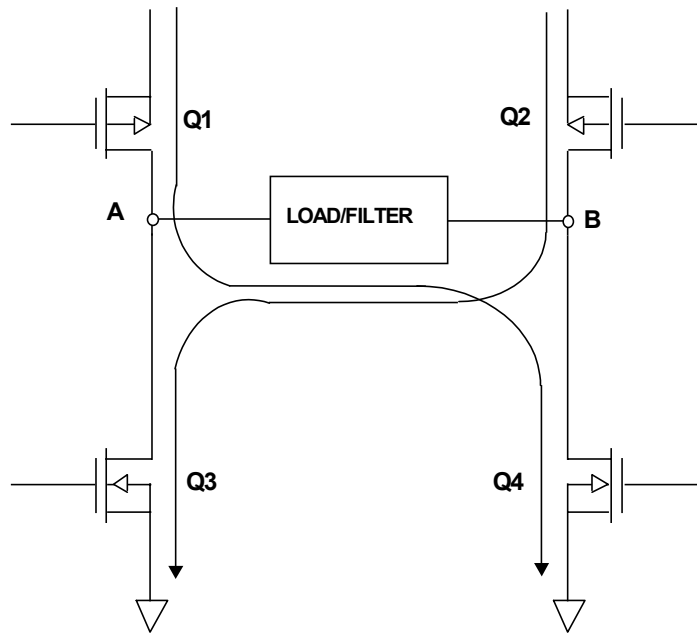
¹ Continuous operation at a cost of \$.10/KWH. If equipment is located in a controlled environment total cost will be considerably higher.

² Package count must be doubled for the discrete design if bipolar output is required.

Benefits Resulting From PWM Efficiency

- Operating cost savings
- Capital cost savings
- Reduced heatsinking 5:1
- Smaller, lighter finished product

H-BRIDGE PROVIDING BIPOLAR OUTPUT FROM A SINGLE SUPPLY



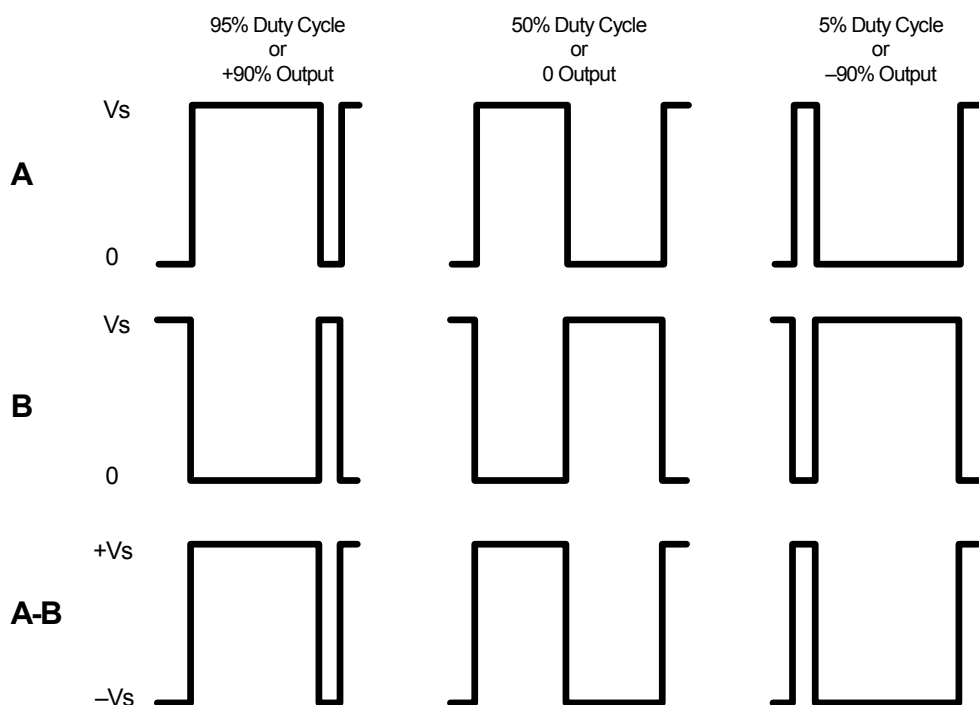
The simple form of a PWM circuit examined thus far is very similar to a number of switching power supply circuits. If the control block is optimized for producing a wide output range rather than a fixed output level, the power supply becomes an amplifier. Carrying this one step further results in the PWM circuit employing four switches configured as an H-bridge providing bipolar output from a single supply. This does mandate that both load terminals are driven and zero drive results in 50% of supply voltage on both load terminals.

The H-bridge switches work in pairs to reverse polarity of the drive even though only one polarity supply is used. Q1 and Q4 conduct during one portion of each cycle and Q2 and Q3 are on during the remainder of the cycle.

Note that if Q1 and Q3 turned on simultaneously, there is nothing to limit current. Self-destruction would be only microseconds away. The fact that these transistors turn on faster than they turn off means a “dead time” needs to be programmed into the controller.

Ref. AN30,AN39

H-BRIDGE WAVEFORMS



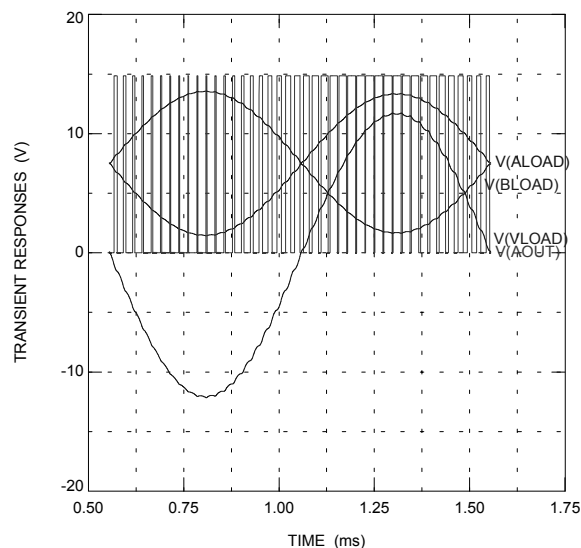
To help understand the conversion of the time modulated data to analog levels, visualize each waveform segment of Figure 2 run through a low pass filter whose cutoff frequency is at least 10 times lower than the switching frequency. The A and B voltages of the 50% duty cycle waveforms will both be equal to 50% of the supply voltage. With both terminals of the load connected to the same voltage, the load sees 0V across itself. The A-B waveform represents this differential connection of the load, and the filtered voltage of this waveform equals zero.

To examine the 95% duty cycle waveforms, let's assume a supply voltage of 100V. The filtered A value will be 95V, B will be 5V, and the load will see 90V; the same as the filtered value of the A-B waveform. When the duty cycle shifts to 5%, the filtered A value will be 5V, B will be 95V, and the load will see -90V, again matching the filtered value of the A-B waveform.

Changing duty cycle through 50% is a continuous function, meaning there is no inherent discontinuity as exists in sign magnitude modulation. This is analogous to the much improved distortion levels of class AB linear stages versus class C linear stages where zero current crossing brings a discontinuity or dead spot usually referred to as crossover distortion.

Ref. AN30,AN39

PWM + Filter Action



This picture shows the B output, switching at 42KHz, modulated at a 1KHz rate, along with the two filtered outputs and voltage as seen by the load.

As the B output spends most of its time in the low state, its filtered counterpart is swinging low. At the same time the A output (not shown, but out of phase with B) is mostly high and results in the filter A voltage swinging high.

With the load looking at the two filtered outputs differentially, it swings plus and minus. Note the 42KHz ripple in the filtered waveforms. While this can be reduced somewhat with more filtering, there is an obvious limit to how close the modulating frequency can get to the switching frequency.

Ref. AN30.AN39

Only Need ½ a PWM Amp?

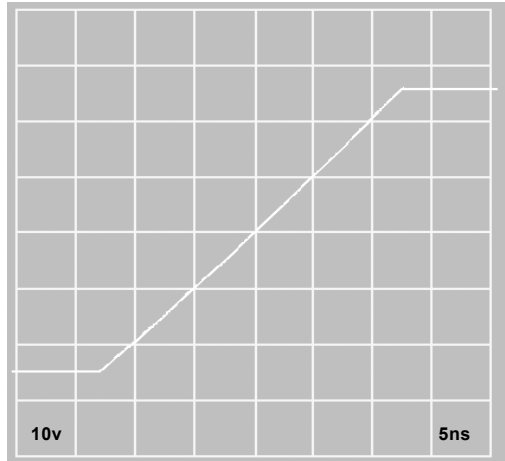
- Unipolar, usually grounded loads
- PPS, TEC, 3Ø motor
- Heater, uni-directional speed control
- Active loads, CD weld charger
- Saves ~½ internal losses
- Saves ~25% on cost

While all Apex PWM amplifiers can be configured in the half-bridge mode, three models are built that way to save you money. These models are ideal for applications requiring only unipolar drive. This means the load is usually grounded. Three amplifiers driving a three phase motor, and active load circuits are exceptions to this rule.

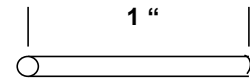
Since load current flows through only one MOSFET at a time rather than two, efficiency is increased. By leaving out some of the internal components, a cost savings is realized.

H-Bridge Waveforms

TEK-NO-WIZ



$$PBW = \frac{SR}{6.238 \cdot V_p}$$



~20nH

$$V = \frac{L \cdot di}{dt}$$

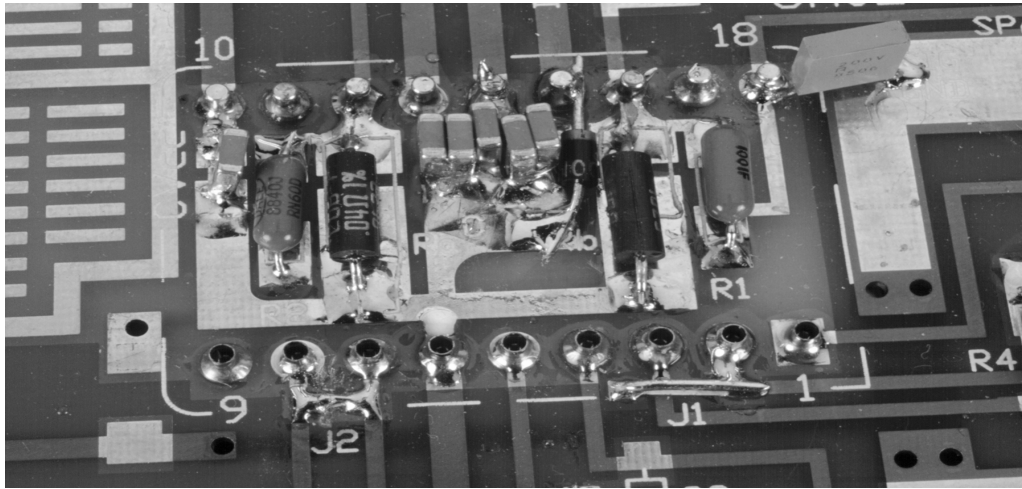
National had their FAST and DAMN FAST buffers, but they can't hold a candle to these guys. In fact, that's the problem with switchers- they move voltages and currents around so fast it's difficult to keep the noise down. Here are a few items you may not have had a chance to use lately.

From the analog world we borrow the equation relating slew rate to power bandwidth. If your PWM amplifier switches 50V in 25ns, the slew rate is 2000V/us. With peak voltage of 50V, this is over 6MHz. With 5 or 10 amps flowing, those transitions contain RF energy similar to a moderate radio transmitter. Spending a few minutes thinking like an RF designer may be worthwhile.

Currents are also changing very rapidly in these circuits. The picture above is of voltage, but keep in mind this voltage is on one end of an inductor where a power MOSFET just interrupted current flow. Look at the positive going transition: the lower MOSFET was conducting and the inductor is driving the voltage positive, above the positive supply, to maintain the previous current flow. The path will be through the body diode of the upper MOSFET, into the supply bypass capacitor. If current changes 5A in the same 25ns, two 1 inch capacitor leads will develop an 8V spike. On high speed PWMs this spike will cause the controller to freak out, rendering the circuit useless.

Ref. AN30, POWER SUPPLY BYPASS

Layout Sensitive? You Bet Your ...



Apex has an Eval Kit for every PWM model

Evaluation Kits for PWM amplifier prototyping are a must. A bad layout will produce ample frustration and can cause dead amplifiers!

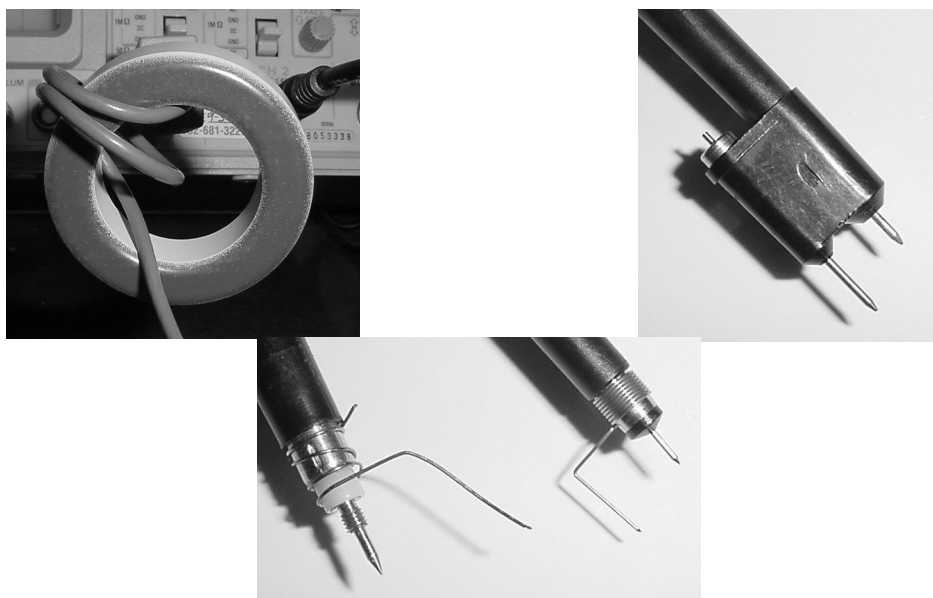
At a minimum, each kit provides a PC board, a way to get the amplifier plugged in, a moderate sized heatsink, and enough hardware to get it all put together. Several models also provide chip capacitors for low inductance bypass of the supplies.

In this example, the amplifier is on the opposite side of the board. Note the chip capacitors DIRECTLY between supply and ground pins of the amplifier. The two large black resistors are the current sense resistors which need to be a non-inductive type.

Separate high current traces from low level traces as much as possible. Include ground plane under low level traces, but NOT under high current traces. Specify at least 2 ounce copper for the PC board. Make the ground pin of the amplifier be the center of the star ground system.

Ref. AN30

Can you believe your scope?



Does every low level scope observation yield the same spike-laden waveform? Here are a few causes and helpful hints.

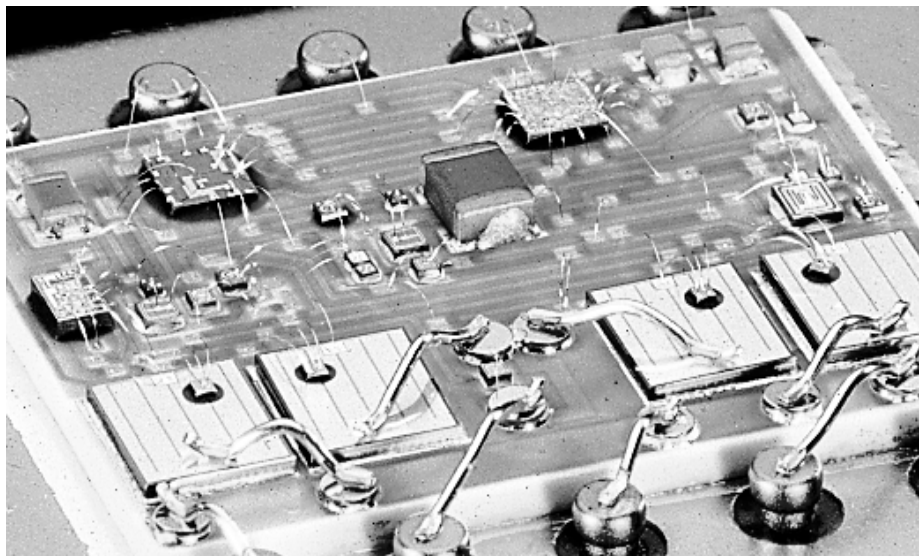
The typical 3" to 6" ground clip on the probe has to go because it is forming an inductive pickup loop. If luck holds, the scope accessory kit will yield an RF adaptor capable of providing a ground lead about $\frac{1}{4}$ " long. If not, consider buying one or making your own by winding a length of spring wire (check for piano wire at your local hardware store) on a shaft slightly smaller than the probe tip (a set of drill bits would be handy).

The ground at the amplifier contains high levels of high frequency signal relative to the ground at the scope and common mode rejection of the scope is limited. Disconnect all other signal cables from the scope. Use a battery operated scope or a ground breaker on the power cord. Use a high frequency toroid to construct a low pass common mode filter for the probe as shown.

Fast slewing signals can easily be coupled to high impedance or unshielded probes. Use only probes with nearly complete shielding. Forget the grabber clips, extenders or any single conductor connections to the scope.

Ref. AN30

SA01

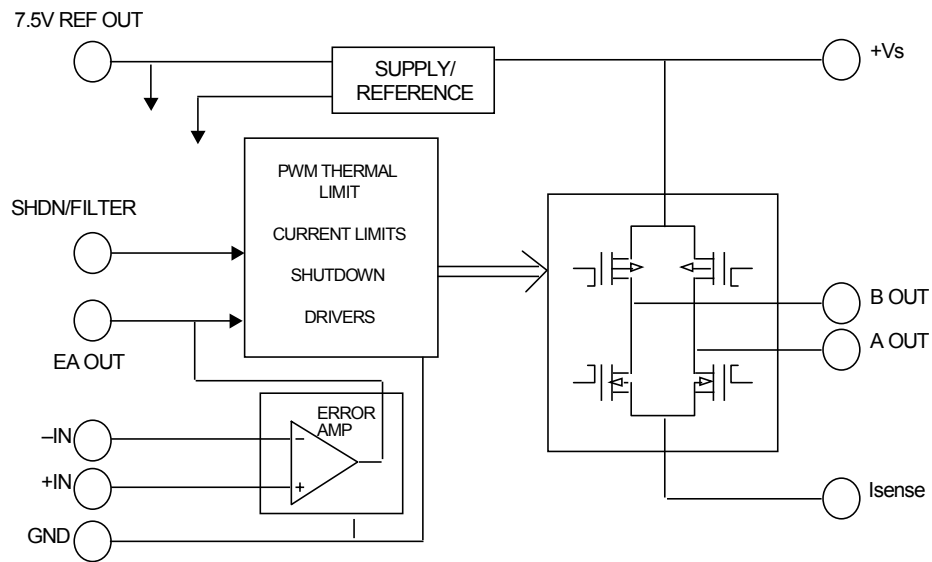


The four huge transistors are the FETs of the H-bridge.

Not quite as obvious, is a unique advantage of hybrid construction which discrete designs can only dream of. Mounted right on top of each FET is a temperature sensor, exactly where the heat is generated.

Ref. AN30

SA01 BLOCK DIAGRAM

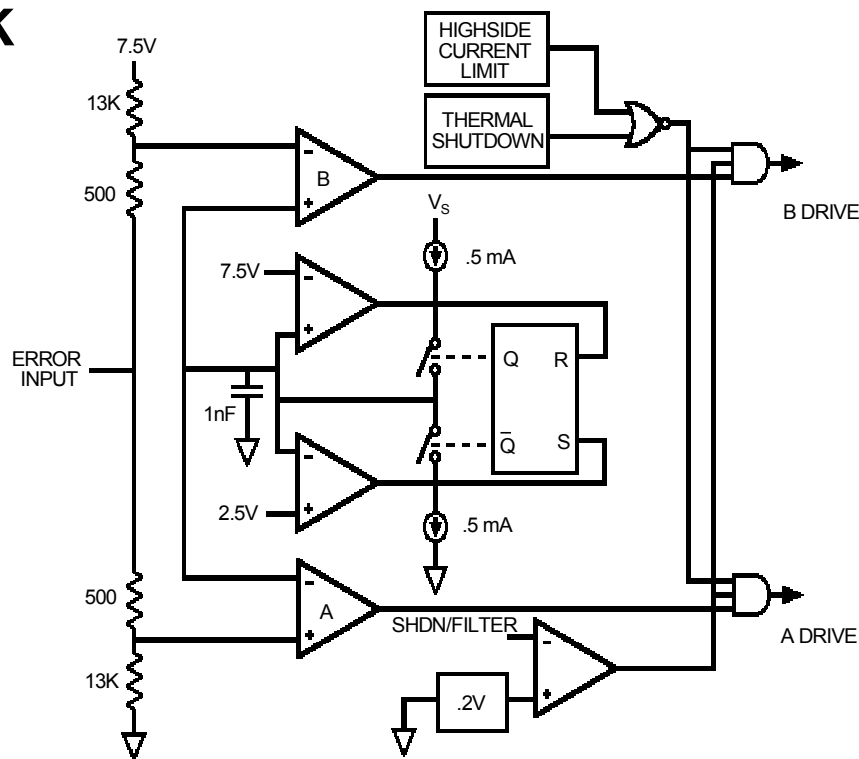


As EA goes more positive, high state of A OUT increases and high state of B OUT decreases.

PWM circuits are taking the same general course of development traveled by op amps and many other electronic functions. Concepts were brought to life using discrete components and were followed by modules, hybrids and then monolithics. The first hybrid on the scene in PWM technology is the SA01 from Apex. The amplifier contains all the functions needed to implement a wide variety of control circuits.

Ref. AN30

PWM BLOCK

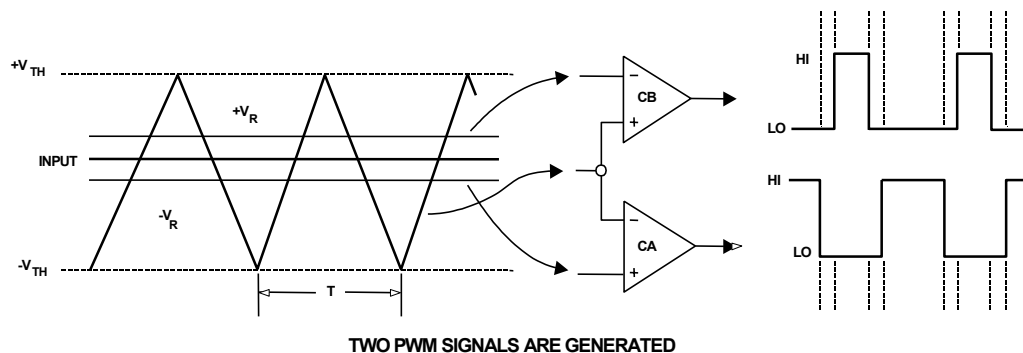
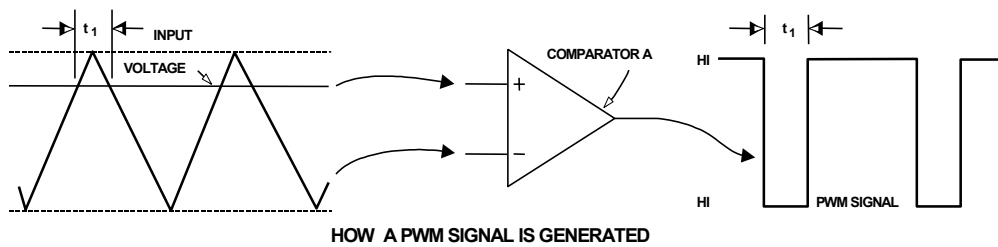


The oscillator portion of the PWM controller consists of two comparators, two switched current sources charging the timing capacitor and a flip-flop. When voltage on the timing capacitor reaches 7.5V, the upper comparator resets the flip-flop which opens the upper current source and connects the lower one. When the timing capacitor voltage reaches 2.5V, the lower comparator sets the flip-flop to start the next cycle.

Comparators A and B modulate the driver output duty cycle based on the voltage relationship of the PWM input voltage and the very linear triangle. For initial examination of operation, imagine the 500Ω resistors are shorted. When the input voltage is midrange, there are equal portions of the triangle wave above and below the input, thus a 50% duty cycle is generated at each comparator output. When the input voltage moves half way between midrange and the 7.5V peak of the triangle, 1/4 of the waveform is above the input and 3/4 is below the input generating a 75% duty cycle at the A comparator. With the inputs of the B comparator looking at the input and triangle voltages in the opposite polarity, it generates a 25% duty cycle. Note the circuit is arranged such that a positive going input voltage results in a larger percent on time for the A driver.

Ref. AN30

PWM WAVEFORMS

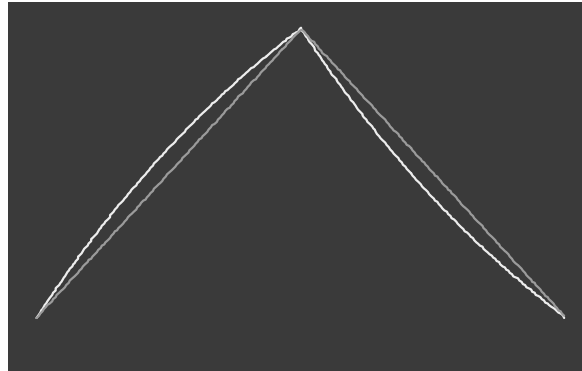
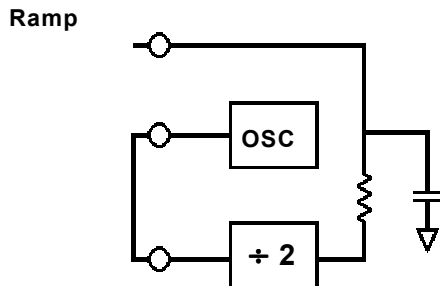


With the 500Ω resistors actually in the circuit, the input voltage seen directly at the comparators is modified slightly, which modifies the duty cycle in a similar way. The A comparator sees a voltage a little more negative than the actual input. The basic function of positive going input creating a longer A duty cycle means this negative offset produces a slightly shorter duty cycle. In the same manner, the B duty cycle is also shortened to produce a dead band where all switches are off. Voltage drops across the two 500Ω resistors change as the input signal varies, but as one drop decreases, the other increases so total dead band time is relatively constant.

The and gates generating both A and B outputs can be disabled by either of two lines. The first of these lines represents activation of the thermal shutdown or the high side current limit. The second line is the comparison of the SHDN/FILTER input and a 0.2V reference. This configuration makes operation of both functions asynchronous and also allows operation to resume anywhere in the cycle when those lines return to their normal state.

Ref. AN30

Alternate Ramp Generator



The switched current source method of ramp generation is elegant in that the slopes are very linear and the end points are set with reference quality voltages. The circuit above is much less expensive and has less non-linearity than one would expect at first glance.

When used to generate duty cycle information, the total time above and below the input signal level is what counts- not the non-linearity of one individual slope. Another way to look at it is that the upward slope has a non-linearity, the downward slope has another and the sum of both determine total non-linearity. It turns out there is a good amount of cancellation between the two such that the non-linearity of the sum is less than 1%.

We will discover other open loop errors are far greater; therefore, PWM amplifiers are almost never run open loop. Once the loop is closed, all of these errors are reduced to insignificant levels.

The alternate ramp generator also allows digital drive circuits to override the ramp waveform if desired.

Basic PWM Transfer Function

$$V_o = \frac{V_{mid}-V_{in}}{V_{pk}} * V_s - I_o * R_{on}$$

V_o = output voltage

V_{mid} = ramp midpoint

V_{in} = input voltage

V_{pk} = 1/2 ramp V_{p-p}

V_s = supply voltage

I_o = output current

R_{on} = total on resistance

- Poor load regulation
- No line regulation
- Temperature sensitive
- Close the loop!

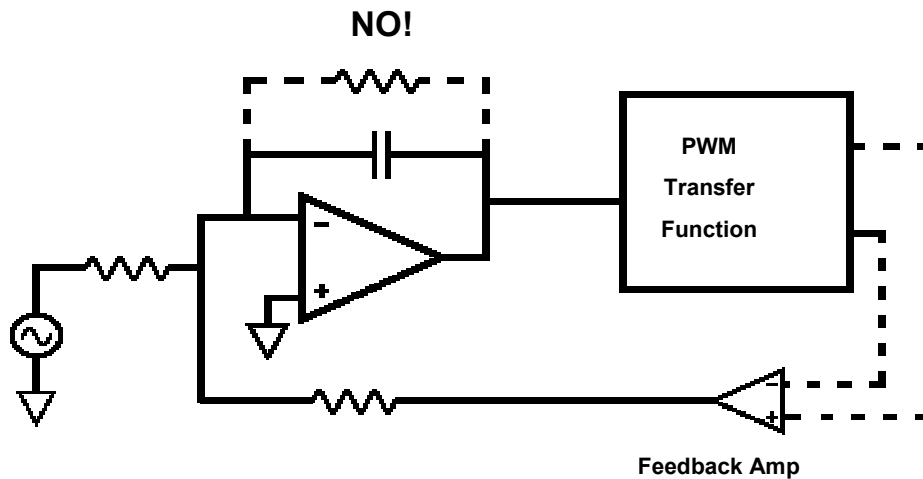
The PWM controller output is duty cycle information only, It is proportional to the input signal level with respect to the end points of the ramp. The power MOSFETs convert this to power pulses and the filter integrates the area under the pulses to provide an analog output. Given a fixed duty cycle, the amplitude of the pulses, and hence the analog output level, is controlled by the power supply voltage and the MOSFET losses.

Those of us accustomed to working with power op amps take power supply rejection for granted; at least at low frequencies, so supply voltage changing a few percent is of no concern. In a similar fashion, we tend to not worry about op amp output impedance because it is reduced by the loop gain of the amplifier. Notice the assumption that nobody runs an op amp open loop; at least when looking for an analog output.

OK, we have learned that open loop performance of a PWM is very different than an op amp: its open loop gain is not $\cong 100\text{db}$, it is the ratio between the peak ramp voltage and the supply voltage and its supply rejection is not 60 to 100db, it is zero db. Accuracy and open loop operation of a PWM amplifier do NOT go together.

Closing this loop can be done locally in the voltage mode and with most models in the current mode. The alternative is closing the loop with system components. This often involves mechanical components, velocity or position sensors and a computer.

Pure Integrator: Key to Accuracy



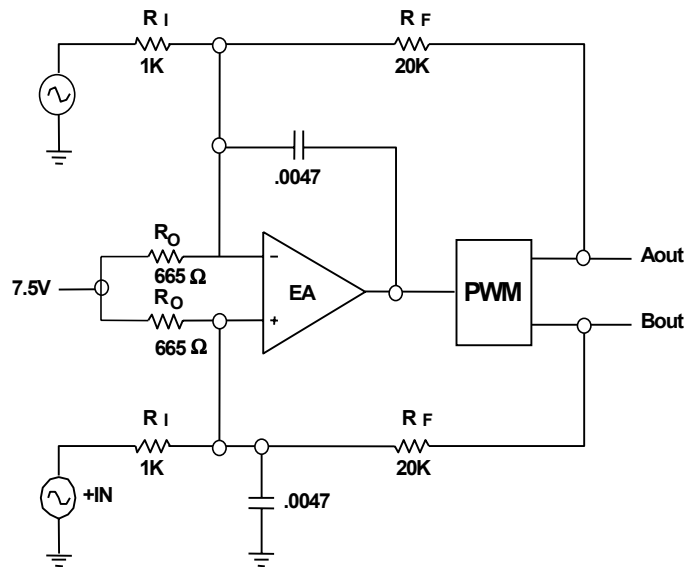
Lets go back to some basic op amp theory for a moment: The open loop gain (the voltage ratio of the output pin to difference of the input pins) of an op amp is extremely high (100db is 100K:1). This means the input pin voltage above is approaching zero. If there is no DC feedback and no current in or out of the input pin, then current through the two resistors must be equal. The PWM output is accurately scaled to the input signal.

The beauty of this analysis is the lack of discussion about the output level of the integrator. As long as all the circuit scaling insures we do not saturate any stage, the integrator takes care of all the variables: supply changes, ramp non-linearity, MOSFET losses, and changes in load impedance.

Sometimes it is a temptation to add resistive feedback. If this is done, DC feedback current lowers accuracy. To find this current we must know the output voltage of the integrator. Start with the PWM output and go backward through the transfer function. The worst case is when the output is near the supply voltage which demands the integrator output be near one of the ramp peaks. The resulting DC feedback current is now causing a mismatch between the input signal and the feedback amplifier currents. Not only is there a gain error and usually a significant offset error, but supply variations and ramp inaccuracies creep in.

Ref. AN39

PWM VOLTAGE CONTROL

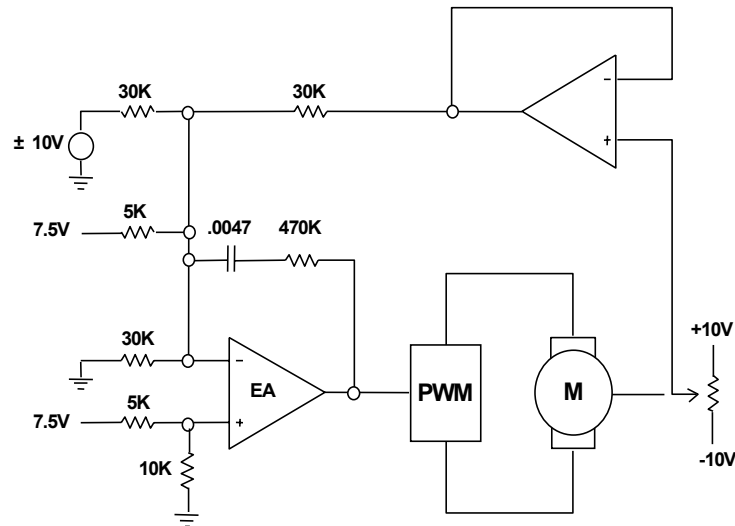


This is a differential input, voltage controlled output circuit resembling the familiar differential op amp configuration. Signal gain is simply R_F/R_I . Two pull-up resistors are used to bias error amplifier inputs within the common mode range. Select this value to get 5V bias when both inputs are zero, and both outputs are 1/2 the supply voltage (50/50 duty cycle.) At zero drive to the load, this differential stage is rejecting 1/2 the supply voltage present on both outputs. This means resistor ratio matching becomes critical. It should also be noted that even though the signal gain is 20, the gain of offset errors is 50 because the effective input resistance is the parallel combination of the signal input resistor and the pullup resistor.

While the specific load is not indicated here, it must be remembered that the SA01 output needs to be filtered. In fact, if the load were purely resistive, this circuit will NOT work! The load would receive full power one direction the first half cycle and full power of the opposite polarity the next. Many common loads such as motors and magnetic bearings will provide adequate filtering on their own. If this is not the case, filtering must be added.

Ref. AN30

PWM MOTION CONTROL



While one of the simplest forms of position sensing is shown here, options such as optical encoders, LVDT sensors, tachometers and variable capacitance transducers are all viable ways to sense speed or position. Again, error amplifier inputs are biased to 5V. While 20Kohm input and feedback resistors would have set proper gain and static biasing for the inverting input, they would have allowed common mode violations. This could happen if the system was at one position extreme while a very quick command came in to travel to the opposite extreme. The three 30Kohm resistors prevent common mode problems by increasing impedance from the summing junction to the two 10V signal levels (at the output and at the input) while adding an impedance to ground to form an equivalent 10Kohm impedance to match the 10Kohm leg on the non-inverting input.

The 0.0047 μ F and 470Kohm values shown here are ballpark values only. In closing the loop in this manner, the inertia of the motor, gear train and load, plus the responses of other electronic components of the application, all enter into the stability/response considerations.

Ref. AN30

Compare: PWM & Linear Amps

V or I input	OK	OK
V or I output	OK	OK
Supplies	Single	Single/Dual
Max Power	Several KW	Fractional KW
Efficiency	High	Low
Noise	High	Low
Speed	Low	High

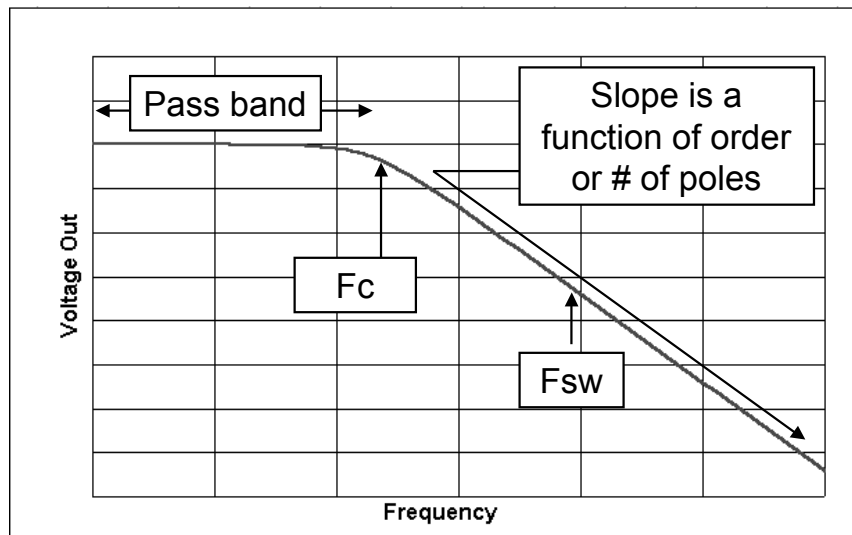
Think about the two previous pages a moment.

They are both basically op amp circuits where the driving op amp has a specialized output stage labeled PWM. In fact there are many applications where linear and PWM solutions would both work. The keys to the decision may be on the last two lines above: IF THE APPLICATION DOES NOT REQUIRE LOW NOISE AND HIGH SPEED, PWM AMPLIFIERS CAN PROVIDE A SOLUTION.

The next item to consider is cost. On a cost per watt capability basis, PWM amplifiers are generally less expensive than linears. With PWM capability starting at 200W, they are not the most likely candidates for a 5W job. At a few hundred watts, PWM amplifiers are very attractive. In between these levels, you may want to think more about the options because both linear and PWM amplifiers will likely work.

Ref. AN30

Low Pass Filter Response

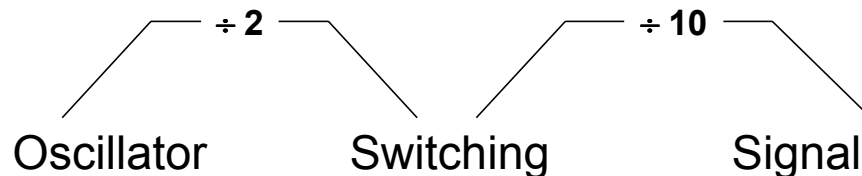


PWM filters are normally low pass configuration. These exhibit low attenuation to the frequency spectrum from 0 Hertz to the frequency of cutoff (F_c). This low attenuation region is called the pass band. Beyond the F_c , attenuation increases at a rate determined by the filter type and the numbers of poles (order).

As we speak of the “frequency” of a PWM signal it is very important to realize what area of this response curve is being referred to. In the pass band area, signals are slow and can be thought of as analog. The switching frequency will be well beyond F_c , can be thought of as the carrier frequency containing time modulated digital information. A reasonable analogy for the filter function might be the audio CD technology where high speed DACs translate digital data to analog output, where the D-to-A conversion rate corresponds to switching frequency. Going even further out in frequency, where the high speed transitions of the PWM amplifiers generate spikes, it is best to think of RF energy.

Ref. AN32,AN39

PWM Frequency Relationships



The alternate ramp generator illustrated the relationship between oscillator and switching frequencies. Some PWM data sheets (such as the SA01) do not mention oscillator frequency because there is no divide by two circuit.

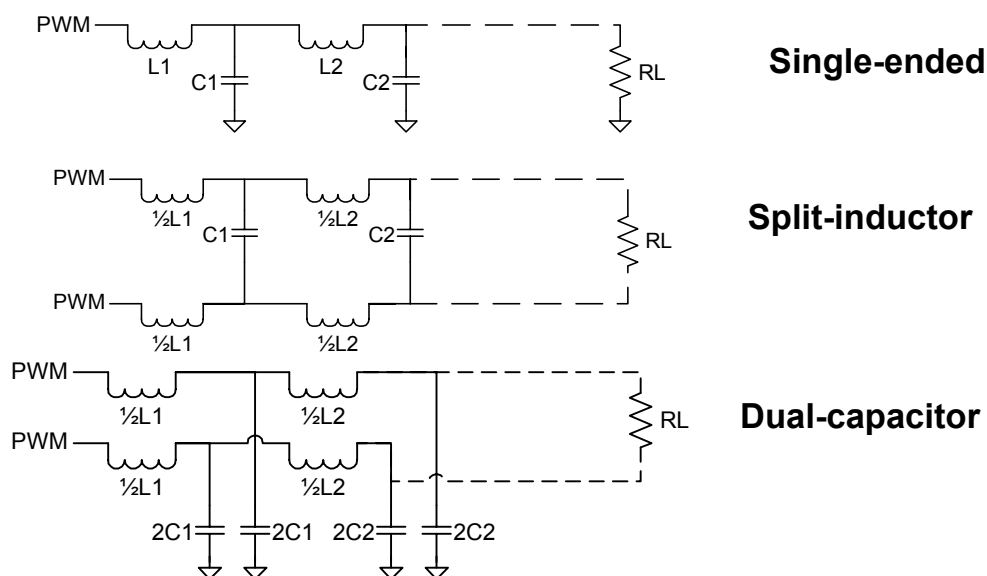
Signal frequency is that of the power drive to the load, power bandwidth. Between the load and the PWM amplifier is the low pass filter (or at least the model of one if the load is also the filter). On the input side of the filter we have the switching frequency. We then go down the slope to a point where the attenuation is adequate. The frequency band we cover while going down the slope is required spacing between the switching and signal frequencies.

Pure theory says filter slope can be increased simply by adding more poles. This is true to a point. We would probably question an eight pole filter in the small signal world. Do you really need that? Can you find high enough quality components to make it work? Can you afford it in terms of size and cost?

In the PWM world these questions are not only valid but are many orders of magnitude more important because power levels have gone from mW to KW! Rule of thumb: Allow a decade between switching and signal frequencies.

Ref. AN32,AN39

Basic Filter Topologies



No matter what topology is used, a first order filter would use only $L1$, a second order adds $C1$, a third order adds $L2$, and so on. Each pole of the filter adds 20db/decade to the slope or roll-off of the filter.

The single-ended filter configuration is the simplest; must be used with half bridge circuits; and can be used with full bridge circuits by substituting the second PWM output for all the ground connections. This substitution is very rarely done because it places the high speed square waves of the PWM output on both load terminals and all the cabling between the amplifier and load. With rise and fall times usually in the tens of nanoseconds, and amplitude nearly equal to supply voltage, this is an extreme RFI problem.

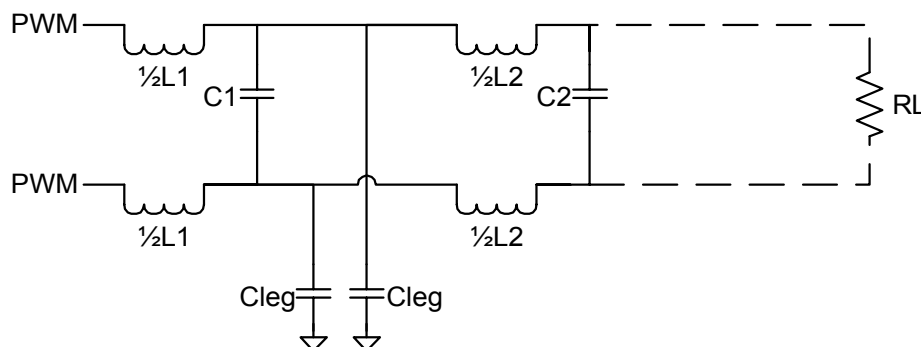
With full bridge circuits, an additional filter requirement is introduced in that common mode voltage applied to both load terminals usually needs to be minimized. The technique to achieve low common mode voltage is to simply split the inductor values in half, applying half to each PWM output as shown in the split-inductor topology.

Capacitors of the split-inductor topology must be capable of bipolar operation and will be very large when the filter is designed for both high current and low signal frequency. While the bipolar capacitors exhibit very low ESL and ESR to provide good roll off in the high frequency spectrum, this leads to very large and expensive banks of capacitors. The dual-capacitor topology can provide a cost savings, at the expense of high frequency performance, by substituting a pair of electrolytic (or possibly tantalum) capacitors of twice the size. To convince yourself this a valid substitution, forget the ground connection and think of two series connected capacitors in place of one. This substitution usually allows the use of unipolar capacitors.

If one could acquire a perfect PWM amplifier (equal rise and fall times, no dead time plus an exact out of phase condition) and perfectly matched inductors, current through each of the dual capacitors would be equal and phased such that no current would flow into the ground node. Even with these imperfections, the ground node current will be a small percentage of the capacitor current.

Ref. AN32

The Most Common Filter

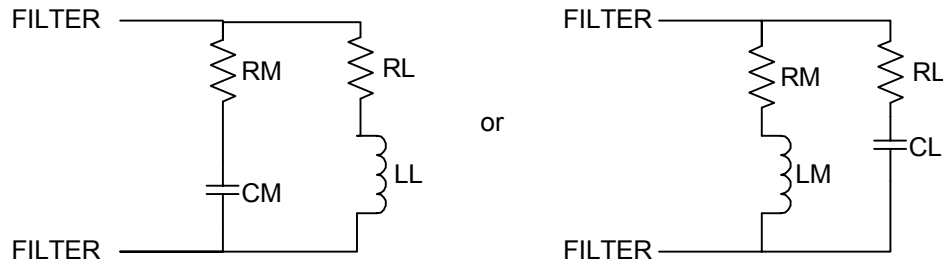


If we apply our previously mentioned fantasy of perfect components to the split inductor filter topology, common mode voltage on the load terminals will be zero. With real PWM amplifiers, the output will contain large amounts of high frequency harmonics. Each application is different, but peak-to-peak noise amplitude may approach the supply voltage. The spectral content of this noise extends well above the switching frequency. A pair of small capacitors added from the output side of each half of $L1$ to ground will remedy this problem. It is not necessary (and sometimes it is counterproductive) to use more than this one pair of leg capacitors. Placing these small capacitors on the load side of $L2$ or $L3$ is not as effective as the placement shown.

Value selection for these ground leg capacitors is less critical than for the main filter capacitors. It has been determined empirically that setting the impedance value of these capacitors at the cutoff frequency, to between 10 to 30 times the value of the load resistance will provide reasonable common mode filtering. The addition of these capacitors will typically produce no more than 0.05db peaking, nor more than 0.2db change at the cutoff frequency in any order filter. From the technical point of view, the two $Clegs$ are in series, and this is in parallel with $C1$. This means that on all but first order filters, $C1$ could be reduced by half the value of $Cleg$ to eliminate even these small errors.

Ref. AN32

Reactive Loads



To achieve even close to these ideal filter responses a constant and purely resistive load termination is required. If a reactive load can be modeled as resistance in series with either capacitance or inductance, a simple conjugate match network can be used to achieve proper termination. The resistor in the network will equal the resistor of the load model. As the network is in parallel with the load, all signals in the pass band will be applied to the network and power dissipation must be checked. Realize that combined impedance of the network plus load is constant and that changing frequency shifts the power between the network and the load. This means a 100W capacitive load drive will require a 100W matching network if DC signals are allowed.

Ref. AN32

Power Design.xls

Filter Design for PWM Amplifiers				READ ME	Using the Complex Load:	
CAUTION!		Refer to Applications Note 32				
Input Data						
Model	SA03	Order Calculation			60 Load All Data For N=1	
Vs	90 Volts	Atten. @ Fsw	41.023 db		61 Load All Data For N=2	
Fsw	22.5 KHz	22.5 N(exact)	1.9513		62 Load All Data For N=3	
Fmin	0.001 KHz				63 Load All Data For N=4	
Fmax	2 KHz	N(recommended)	2		64 Load All Data For N=5	
Fcutoff	2 KHz				83 Load All Data For N=6	
Rload	10 Ohms	Matching network				
Cload	0 uF	Cm =	0 uF			
Lload	0 mH	Lm =	0 mH	Read Me		
Vripple	1 Vpk	Rm =	10 Ohms	Yes	Auto Sweep on Load?	
Signal	85 Units					
Sig as ?	V peak Note/W				Recommended Cleg = 0.3448 uF	
Notes:						
46 Print Filter		55 Show Attenuation in db & %				
56 Show Attenuation Graph		66 Show Filter Components				

So maybe filter design is not at the top of your list of most cherished jobs. Application Notes 32, Part 3 and the Power Design spreadsheet can help. Enter data describing the amplifier circuit, the load and desired attenuation. Placing the cursor in cells with red triangles will display notes of explanation. The order Calculation section converts your maximum ripple spec into db attenuation and by examining the switching and signal frequencies, it calculates the order, or number of poles needed. The matching networks calculated will cause reactive loads to appear resistive to the output of the filter, Finally, a capacitor value is recommended for the leg capacitors for a dual-inductor.

power_design.exe is a free download from www.apexmicrotech.com. When executed, Power Design.xls will be extracted, ready to be run with Excel97.

Ref. AN39

Ideal Components

Component Calculations				Shading indicates values for Split Inductor topology			
Dual Cap Filter		Single-ended Filter		Dual Cap Filter		Single-ended Filter	
N = 1	L = 0.3979 mH		0.7958 mH	N = 2	L = 0.5627 mH		1.1254 mH
	P-P Ripple = 2.5133 Amps out of the amplifier				C = 11.254 uF		5.6269 uF
	Avg. I _{out} for thermal calculations = 0.6283				P-P Ripple = 1.7772 Amps out of the amplifier		
					Avg. I _{out} for thermal calculations = 0.4443		
N = 3	L1 = 0.5968 mH		1.1937 mH	N = 4	L1 = 0.609 mH		1.2181 mH
	C = 21.22 uF		10.61 uF		C1 = 25.102 uF		12.551 uF
	L2 = 0.1989 mH		0.3979 mH		L2 = 0.4307 mH		0.8613 mH
	P-P Ripple = 1.6755 Amps out of the amplifier				C2 = 6.0909 uF		3.0454 uF
	Avg. I _{out} for thermal calculations = 0.4189				P-P Ripple = 1.6419 Amps out of the amplifier		
					Avg. I _{out} for thermal calculations = 0.4105		
N = 5	L1 = 0.6148 mH		1.2296 mH	N = 6	L1 = 0.6179 mH		1.2358 mH
	C1 = 26.967 uF		13.484 uF		C1 = 28 uF		14 uF
	L2 = 0.5499 mH		1.0998 mH		L2 = 0.6179 mH		1.2358 mH
	C2 = 14.235 uF		7.1174 uF		C2 = 19.124 uF		9.562 uF
	L3 = 0.1229 mH		0.2459 mH		L3 = 0.3016 mH		0.6031 mH
	P-P Ripple = 1.6266 Amps out of the amplifier				C3 = 4.1189 uF		2.0595 uF
	Avg. I _{out} for thermal calculations = 0.4067				P-P Ripple = 1.6184 Amps out of the amplifier		
					Avg. I _{out} for thermal calculations = 0.4046		
56 Show Attenuation Graph				38 Data Input			

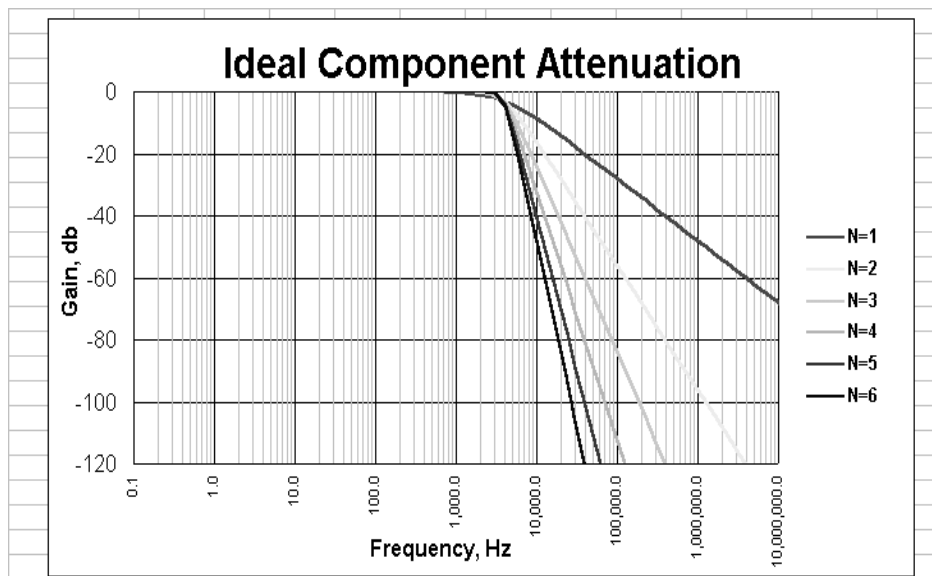
Application Note 32 will provide filter coefficient tables and formulas if you insist on calculating component values the hard way.

Values for dual-capacitor and single-ended filters are found under the appropriate columns, for orders up to six. Six is generally higher than is practical because of cost and diminishing returns due to component parasitics and stray coupling. To build a split-inductor filter, use values in the shaded areas from both columns.

P-P ripple calculations refer to current in L1 at the switching frequency when a 50% duty cycle is present. The *Avg. I_{out} for thermal calculations*, is the average current through one PWM switch and can be used for determining junction temperature.

Ref. AN32,AN39

What a Wonderful Word!



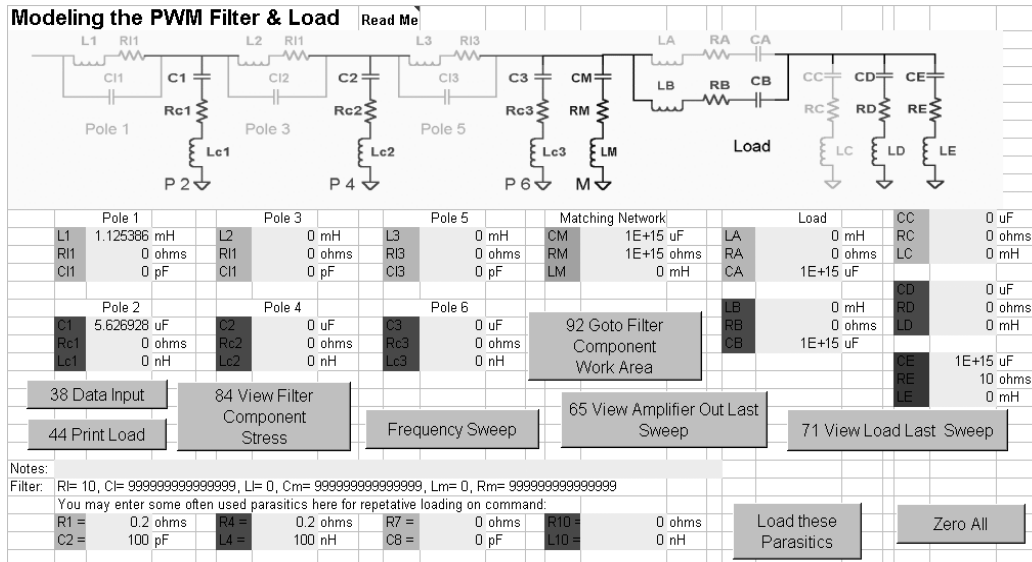
“Ideal” is a great word. In this case it means most of the work still lies ahead in finding components which work acceptably in the MHz range and whose losses won’t kill you at high current levels.

For capacitors, this often means parallel bipolar devices to obtain high value and high frequency performance. You will probably want ceramic for the smallest values and plastic for the higher values. For the largest capacitance values tantalum, or electrolytic types, can often be used in the dual-capacitor topology with some loss of high frequency attenuation.

Finding suitable inductors is also challenging. Air core inductors get away from the magnetic saturation problem and they have less tendency to become dummy loads at high frequency. The down side will be more turns of wire and more copper losses. When adding a magnetic core make sure the material can handle the high frequency components of the square wave at the switching frequency and can accommodate the flux density of the peak currents to be delivered to the load. Ferrite and powdered iron cores hold the most promise; avoid laminated steel cores.

Ref. AN32,AN39

The Filter & Load Model



Pressing one of the “Load All Data” buttons on the PWM Filter sheet transfers your application to the PWM Power sheet. Ideal component values are loaded automatically for all six pole elements, the matching network and on the far right, the load we specified earlier. Extra components in the load modeling area provide more flexibility. As the math (and execution time) would be a significantly larger burden for any other topology, Power Design only analyzes single-ended filters.

Note that the horizontal load model components are “zeroed” with no resistance, no inductance, but an extremely large capacitance. Unused components in the vertical orientation require zero capacitance or extremely large values of resistance or inductance.

The Frequency Sweep button will calculate critical voltages, currents and powers over the frequency range we specified. 100 frequency points will be examined. If this takes less than 10 seconds, you should be proud of your computer. If it takes more than a minute

The Goto Filter Component Work Area button will be used to translate component values between the three topologies and for first pass design work, to estimate parasitic values.

Ref. AN32,AN39

Translate & Estimate Parasitics

Filter Component Work Area				README			
Pole 1				Pole 3			
L1	0.562693 mH	L2	0 mH	L3	0 mH	91 Calculate Default Parasitics for these acutal Components	
RI1	0.178808 ohms	RI1	0 ohms	RI3	0 ohms		
CI1	34.06732 pF	CI1	20 pF	CI3	20 pF		
Pole 2				Pole 4			
C1	5.626928 uF	C2	0 uF	C3	0 uF	38 Data Input	
Rc1	0.087514 ohms	Rc2	0.05 ohms	Rc3	0.15 ohms		
Lc1	19.75353 nH	Lc2	10 nH	Lc3	30 nH		
Pole 5				Pole 6			
Select Capacitor type: E=electrolytic, P=plastic or ceramic				37 Define Load			
P				P			
85 Translate Auto-Loaded Values for Split-inductor Filter							
86 Get Auto-Loaded Values for Single-ended Filter							
87 Translate Auto-Loaded Values into Dual-capacitor Filter							
				88 Translate Split-inductor Values back to Single-ended & Sweep			
				89 Take Single-ended Values and Sweep			
				90 Translate Dual-capacitor Values back to Single-ended & Sweep			

Buttons 85-87 will get or translate the Auto-loaded single-ended component values to values for the topology or your choice.

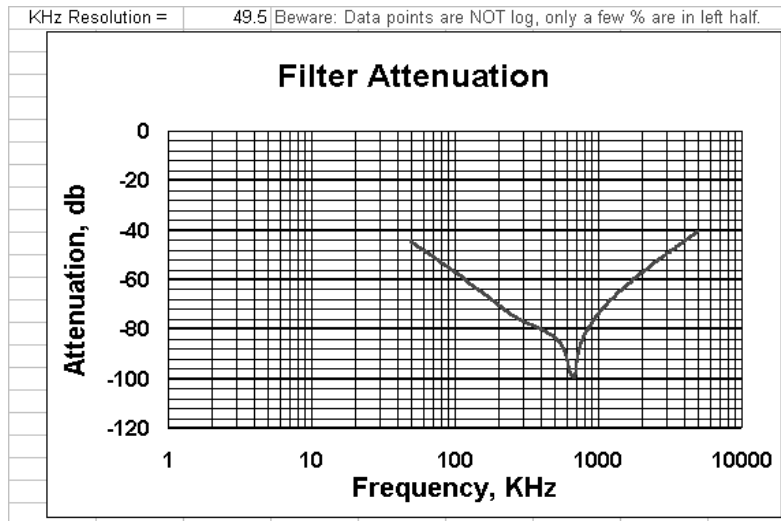
While there is absolutely no substitute for finding real parasitic values for filter components, button 91 provides a default parasitic calculator for first pass design efforts. Notice the cells where capacitor type can be selected individually for all three capacitors. Parasitics vary WILDLY from part to part. The default calculator is ONLY intended to get somewhere in the ballpark. These defaults are reasonable for parts suitable for switching applications. Your real parts could be better, but could easily be much worse. Consult manufacturer's data sheets or measure the parts to get accurate data for subsequent analysis. Values of purchased components and their real parasitics should be entered directly into the yellow cells and then be translated with button 88, 89, or 90.

During the translation back to single-ended values, if dual inductors are being used, the inductance and resistance will be doubled, and the capacitance will be divided by two. If dual capacitors are being used, capacitance will be divided by 2, plus the resistance and inductance will be doubled.

Frequency sweep will run automatically upon translation, and requires Analysis ToolPak. If you see cells with #NAME? or a runtime error, try TOOLS, ADD-INS, Analysis ToolPak and then do the sweep.

Ref. AN32,AN39

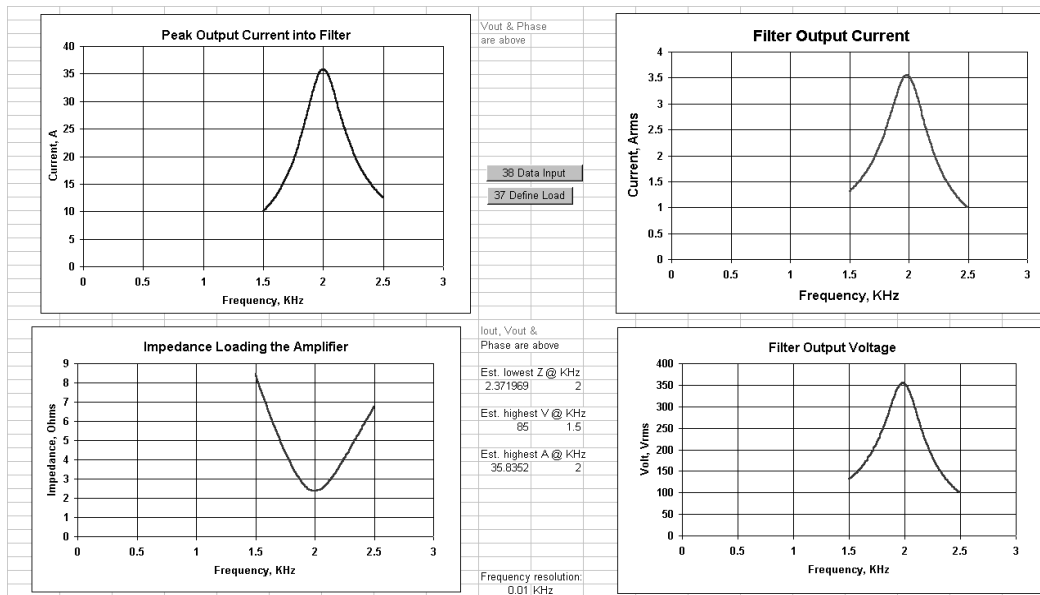
The Penalty of Real Parts



Attenuation is about as expected up to 200KHz, but then the parasitics come into play. We learned earlier that the extremely fast transition times of the PWM amplifiers means high frequency content is powerful well into the megahertz range. This graph is telling us spike content at the filter output is far from ideal. Is this OK? Or should we spend more on better filter components?

Ref. AN32,AN39

Light Test Load- -Oops!



So, you're an old hand with linear power circuits; you fire up the prototype with a light load to make sure everything is working before connecting the real load.

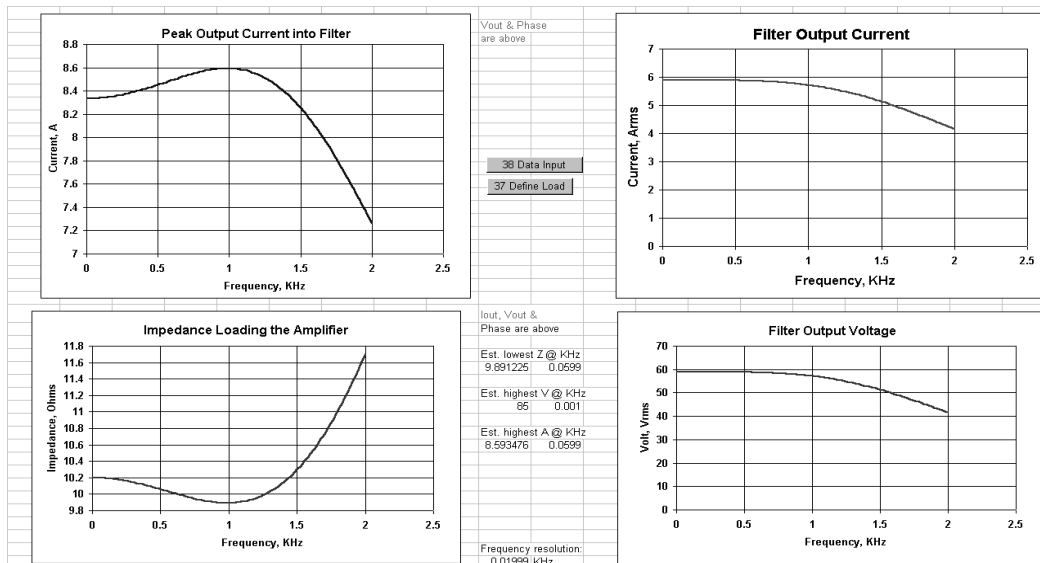
While this procedure is commendable for linear drives and *may* work fine for a PWM drive, watch out for tuned circuits in the filter/match network/load. Replacing the designed 10 ohm load with 100 ohms produces the graphs above. At 2KHz impedance drops to ~2.5 ohms, peak current tops 35A, load voltage is ~355V and load current is 3.5A. 1200W delivered to the *light* 100 ohm load!

Be careful- -deadly voltages easily generated.

The second order filter driven at the designed cutoff frequency, with no load, is a series resonant circuit which presents a theoretical zero impedance to the amplifier and develops a theoretical infinite voltage at its center.

Ref. AN39

Right Load gets Right Results



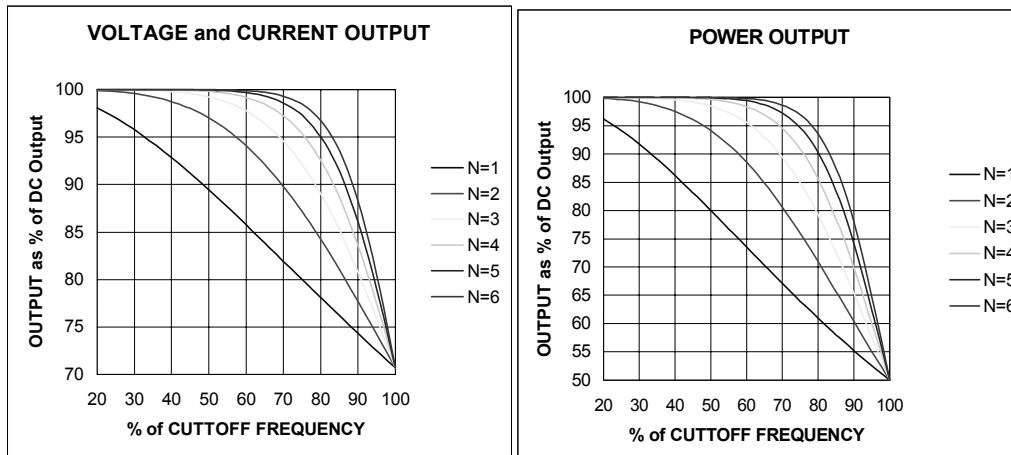
With proper termination of the filter we get a little mid-band peaking amplifier output current but the catastrophic potential of bad filter termination has gone away.

This filter design technique assumes amplifier output impedance is low compared to the load impedance and that the combined impedance of the load plus matching network is constant over frequency. The demand for circuit efficiency will insure the impedance relationship requirement is met. Beware that changing load element values, without corresponding matching network value changes, will alter the filter response curve. With some loads, such as solenoids or valves that tend to change inductance with position, the textbook response curve is nearly impossible to achieve. In these cases, try designing for the highest impedance, and then check performance driving the lower impedance.

While this operation is *proper*, is it what you wanted? The cutoff frequency of the filter is where the load voltage is down 3db. does -3db equal .707 or .5? Both, .707 is the voltage or current ratio and .5 is the power ratio. Many times the half power at maximum frequency is not acceptable.

Ref. AN32,AN39

Passband Attenuation

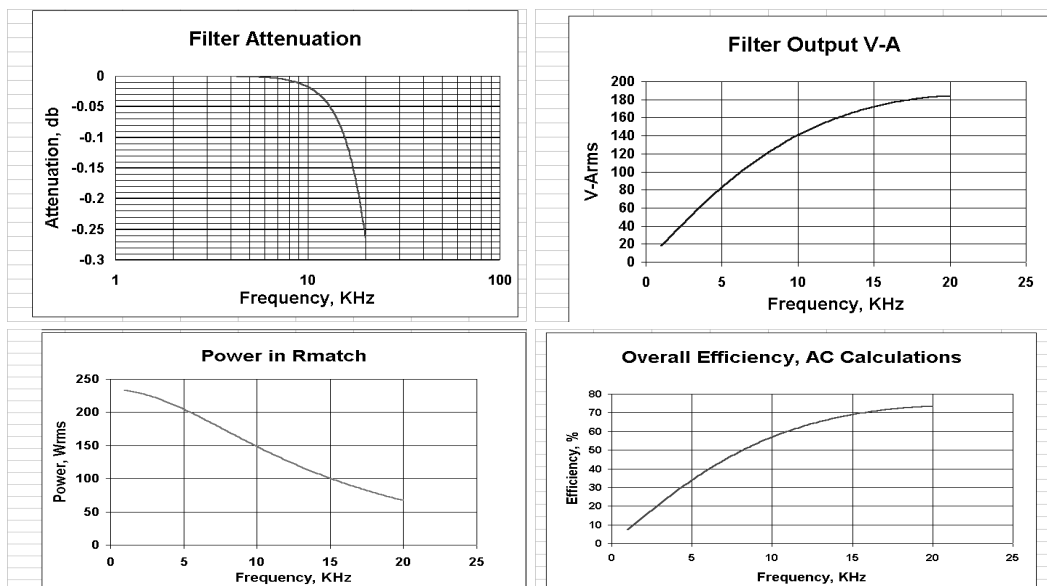


Designing the cutoff frequency at twice the actual maximum signal frequency is a very common technique to obtain a flatter response in the portion of the pass band actually used. You can see that in cases where amplitude flatness is critical, higher order filters and a wider ratio between actual signal frequency and F_c both help.

Yes, you could double again to achieve an even flatter pass band. No, there is no free lunch. Every time you move cutoff frequency up, you allow more switching frequency power in the load. Yes, you can add more poles to the filter. The question becomes one of cost in terms of money, extra loss in the filter, size and weight.

Ref. AN32

Power in the Matching Network

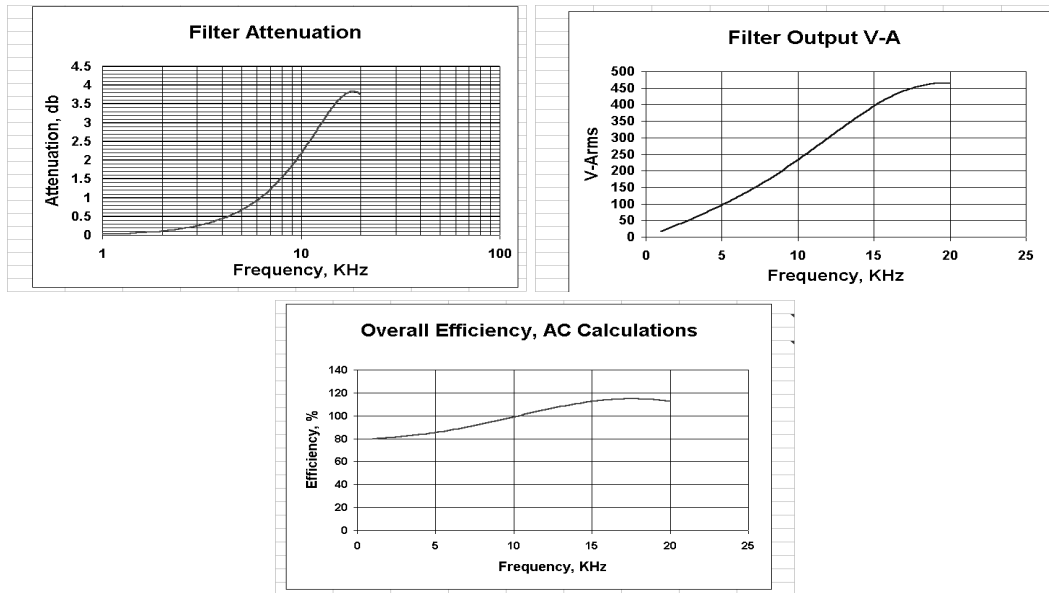


While the conjugate matching network performs almost like magic in terms of forcing the attenuation graph to near text book shape, there is a cost involved. This cost is slight when the load is mostly resistive but power dissipated in this network approaches power delivered to the load as the load approaches pure reactance.

These graphs are for an application driving a 1uF piezo stack with 12 ohms series resistance, to 75V peak from 1KHz to 20KHz. The filter cutoff frequency was designed for 40KHz providing quite flat response. The V-A output falls at low frequency because the load impedance is increasing. To keep filter termination impedance flat, the matching network impedance moves in the opposite direction giving rise to large power levels in the matching network resistor. As this power is not delivered to the load, efficiency is far from the desired level.

Ref. AN32,AN39

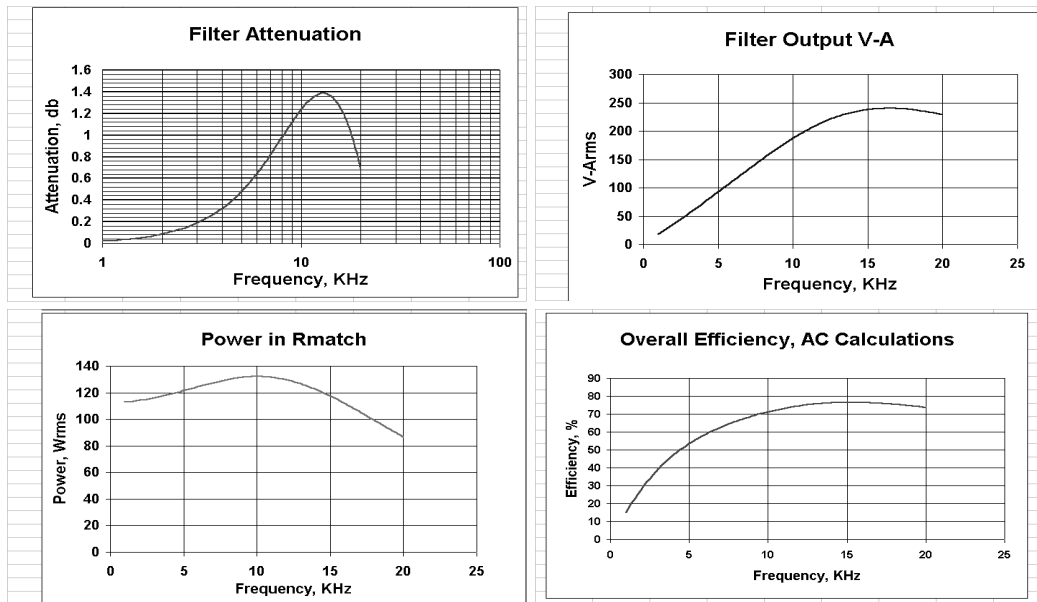
Without a Matching Network



With no matching network we cannot lose any power there, but this leaves the filter with an improper termination. The result is a resonant circuit causing almost 4db peaking. In terms of V-A in the load near the upper end of the band, power goes from ~180 to over 450V-A. The efficiency graph looks like a patent should be applied for. The reason for this is recirculating currents in our newly formed resonant circuit.

Ref. AN32,AN39

Modified Matching Network

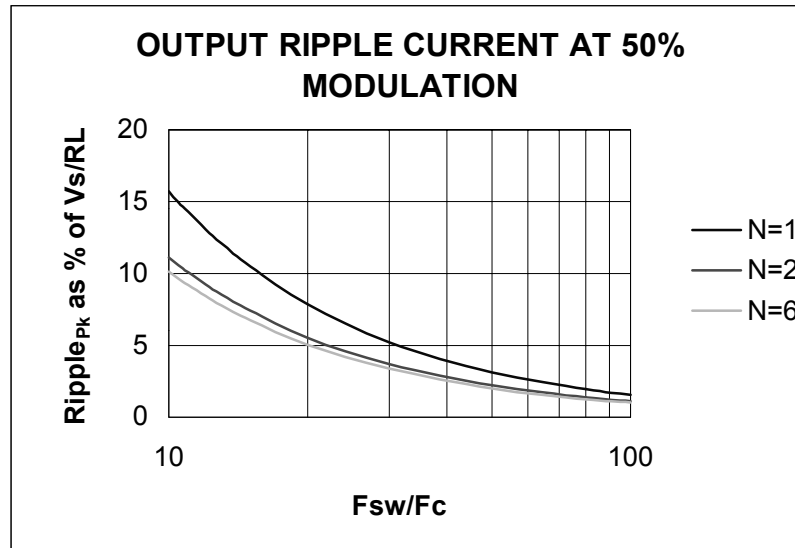


Here lies part of the beauty of the Power Design spreadsheet; it took more time to prepare this slide than it did to discover that doubling the resistor value in the matching network may provide a workable compromise.

Peaking at the load is down substantially from not using any network and wasted power is down substantially from using the ideal network.

Ref. AN32,AN39

Minimum Inductance



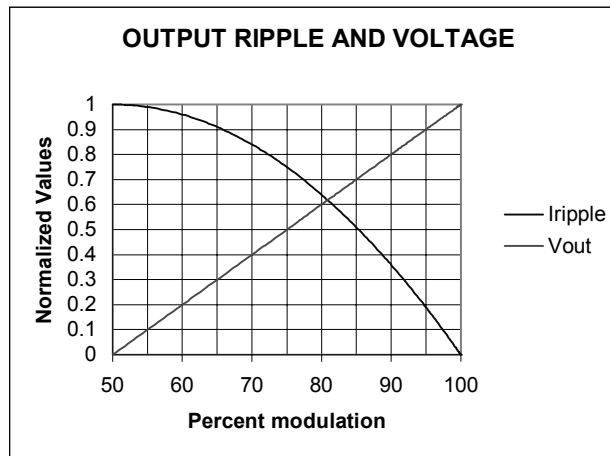
Application Note 30 admonishes us to make sure the PWM amplifier is driving enough inductance to keep ripple current at the switching frequency to a reasonable level. When designing filters according to Application Note 32, this concern becomes part of the filter design.

A full bridge PWM amplifier driving a first order (single pole) filter with F_c set at $1/10$, the switching frequency will be required to deliver approximately 15% of the peak output current as peak ripple current. The ripple is at the switching frequency; measured when the modulation level is 50%; and assumes peak output current equals V_s/RL . Changing to a second or higher order filter will drop this to almost 10%. A second and even more effective way to reduce this ripple current is to widen the ratio between signal and switching frequencies. As switching frequencies of Apex PWM amplifiers range from 22.5KHz to 500KHz, this technique has obvious limits.

This ripple current flows through the first inductor of the filter, meaning high frequency core loss is of concern. With first order filters driving resistive loads, it also flows through the load. With higher order filters, most of the ripple current flows in the first filter capacitor, affecting the ripple capacity rating of these components.

Ref. AN32

Ripple Varies with Modulation

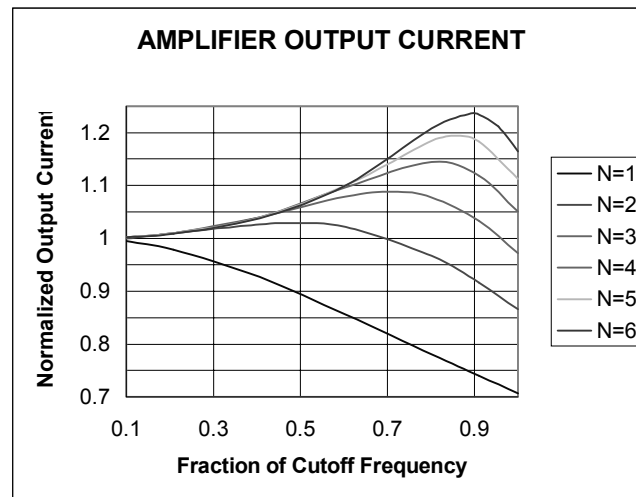


In applications where full modulation is expected (output current is expected to approach V_s/RI), the workload imposed on the amplifier by delivering the ripple current is of minor concern. While 15% (or less as) of maximum output may seem more than minor, this ripple current decreases as modulation percentage moves away from 50% (a graph of zero to 50% would produce a mirror image curve). In other words, heatsink size is not increased 15% because maximum DC output and maximum ripple output never occur at the same time. The heatsink will be sized to handle the much larger output current. The ripple current curve is also valid for half bridge circuits, but the V_{out} curve would need to be re-scaled from 0.5 at 50% modulation to 1 at 100%.

For applications spending a major portion of the time near the 50% modulation level, the ripple current will be quite noticeable in terms of lowered efficiency (power supply loading and heatsink temperature). These circuits include full bridges spending most of their time delivering small signals compared to peak output capability; full bridges whose peak output voltage is considerably less than supply voltage; and half bridges spending most of their time delivering half the supply voltage.

Ref. AN32

Load current≠Amplifier Current

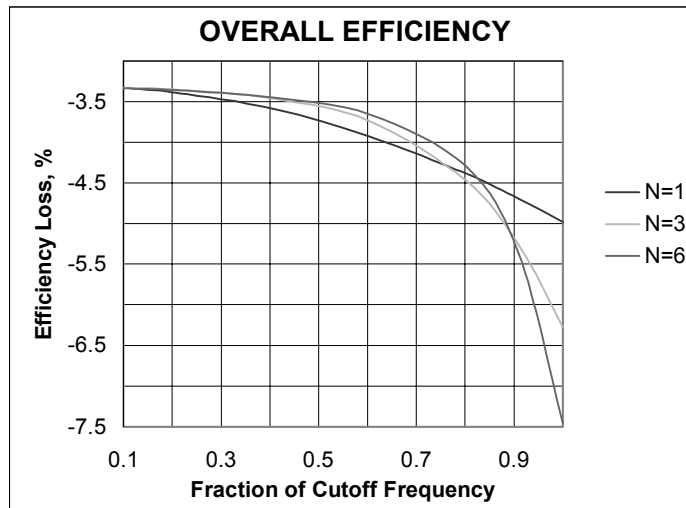


When using second and higher order filters, impedance presented to the PWM amplifier will dip below the load impedance as signal frequency approaches F_c . The graph above shows this in reciprocal form. Putting some numbers to go with the worst point: $N=6$, $F_c=1\text{KHz}$, $F_{\text{signal}}=900\text{Hz}$, $I_{\text{load}}=10\text{A}$, amplifier output=12.3A. This “extra” current flows in the output devices of the PWM amplifier increasing internal power, increasing ON resistance, increasing junction temperatures and reducing efficiency. This effect should be considered also with regard to amplifier and power supply current ratings and design of current limit circuits. We will see what looks almost like a duplicate of this graph when discussing filter component stress levels.

Again, this graph shows the advantages of lower order filters and wider ratios between actual signal frequency and F_c .

Ref. AN32,AN39

Speed & Order vs Efficiency

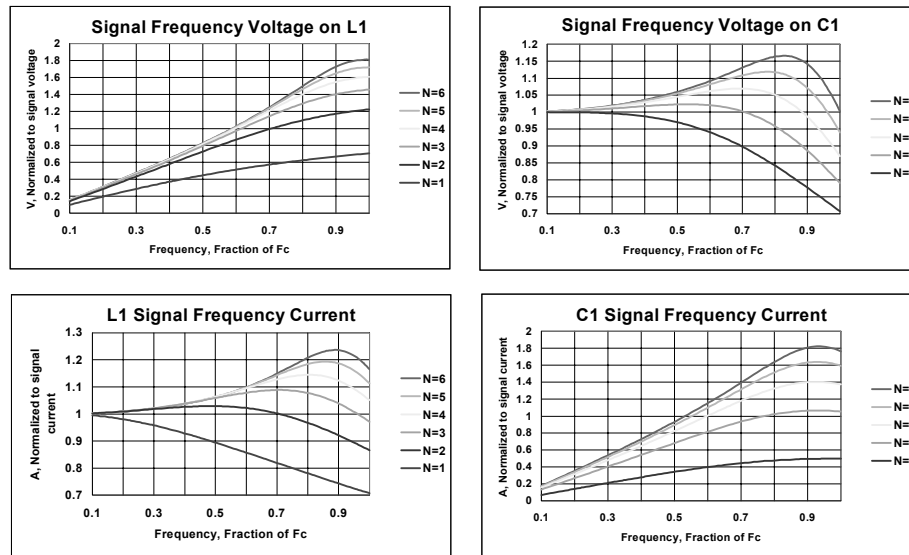


This is efficiency data for a perfect component filter (no parasitics) designed for an SA03 running maximum output voltage into a 10Ω load while mounted on a 0.1°C/W heatsink. At 10% of F_c , about 3.3% is lost in the amplifier and the filter is having very little affect on efficiency. As signal frequency increases, three effects combine to bring high frequency efficiency down further. First, quiescent power remains constant even though the output signal is rolled off. Secondly, the peaking output current demanded by second and higher order filters increases internal PWM losses. The last item is the positive non-linear temperature coefficient of the ON resistance of the PWM, which increased about 1% in this example.

The point here is that filter choices can double efficiency loss even before allowing for filter component loss. Importance of this data varies with the spectral content of the signal being amplified. Consider an audio application versus a fixed 400Hz inverter application.

Ref. AN32

V & I Ratings for L & C



Multi-pole filters are a combination of one or more series resonant circuits and they do develop currents and voltages above the input and output levels as the signal frequency approaches the cutoff frequency. The highest stress levels will be born by L1 and C1. Higher order filters produce higher amplification levels. The last two components of the filter do not see stress levels above the signal level. In these graphs, voltages and currents are normalized to the DC or very low frequency output signal amplitude and are based on ideal components.

Data on current can be used directly for any filter topology for both inductors and capacitors. If a split inductor topology is used, the inductor voltage data must be divided by two. Voltage data can be used directly for capacitors not connected to ground. Ground terminated capacitors have a DC bias equal to $\frac{1}{2}$ the supply voltage which must be added to half the peak voltage calculated from the graphs. Do this calculation for BOTH the positive and negative peak output voltages. Note that if output voltage is nearly equal to supply voltage, and the filter order is three or more, the most negative going peak for C1 will be negative with respect to ground. The same is true for C2 with fifth and sixth order filters. This means even a ground-terminated capacitor can have BIPOLAR voltages applied. From a practical point of view, this situation implies the use of unipolar capacitors limits filter order to two.

As an example, consider filter options for an SA06, which is to deliver $\pm 470V$ to a 332Ω resistive load at 1KHz. Current will be 1.414A peak or 1A RMS. Power will be 665W peak or 332Wrms. A supply of 480V will provide plenty of headroom for internal losses and maximum linear duty cycle limitations. The worst case for voltage and current extremes will be a sixth order filter.

$$L1 \text{ peak current} = 1.414A * \sim 1.23 = 1.75A$$

$$L1 \text{ peak voltage} = 470V * \sim 1.82 = 850V \quad 425V \text{ each if dual}$$

$$C1 \text{ RMS ripple current} = 1A * \sim 1.82 = 1.82A$$

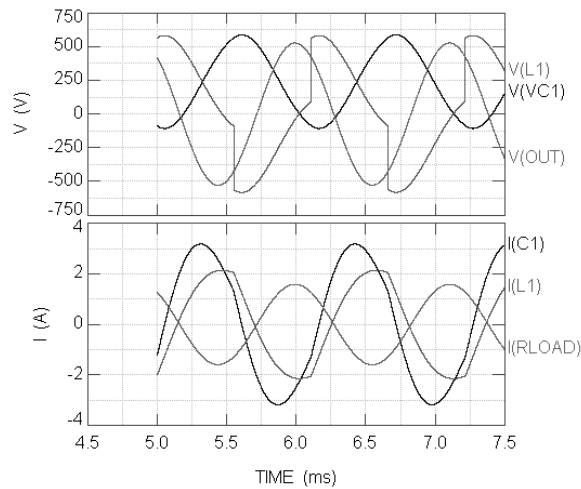
$$C1 \text{ peak voltage (differential)} = 470V * \sim 1.17 = 548V$$

$$C1 + \text{ peak voltage (grounded)} = 240V + 274V = 514V$$

$$C1 - \text{ peak voltage (grounded)} = 240V - 274V = -34V \quad \text{Must be bipolar}$$

These stress levels are normal, even though the output ratings of the circuit are only 470V peak and 1Arms and the filter is properly designed and terminated. Before we go to the next slide, note that the input signal for this circuit is a sine wave. Ref. AN32

Square In-Sine Out, And....



File: C:\TsWin32\Circuits\BARE DIFFERENTIAL FILTER.OUT REV: 5

This is a Spice simulation of the previous example showing L1 and C1 stresses when the input signal is a 900Hz, 470V square wave instead of a sine. The modeled filter topology was a dual capacitor design.

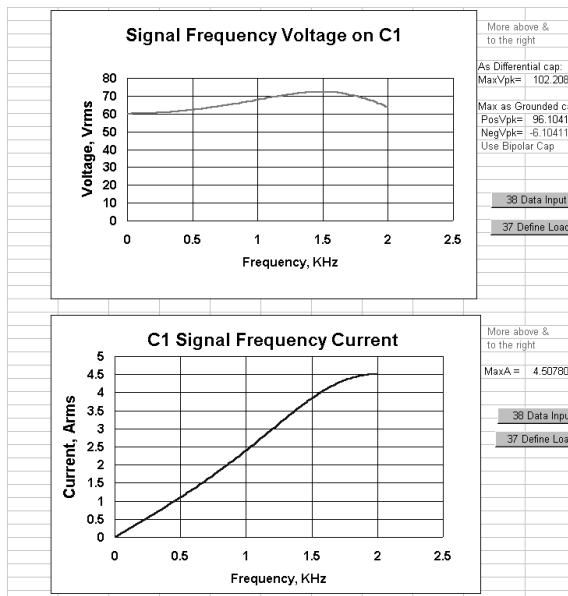
L1 voltage = $\pm 582\text{V}$ and is for $\frac{1}{2}$ the total inductance (a single-ended design would place $\pm 1164\text{V}$ across the inductor). L1 current peaks at $\pm 2.14\text{A}$. C1 current peaks at $\pm 3.18\text{A}$. C1 is grounded and has voltage peaks of 587V and -107V . Watch out with that electrolytic capacitor! The output is a very good looking sine wave instead of a square, and peak output amplitudes have risen from 470V to 527V , from 1.414A to 1.59A and from 665W to 838W .

Points to consider:

1. Other than this slide, all input signals have been sine waves.
2. Input waveforms other than sine, can produce stress levels even higher than Power Design predicts.
3. As signals approach F_c , filters REALLY like to output sine waves.
4. If you really do need constant frequency sine waves with peak amplitude higher than the supply voltage, this is a possible circuit.

Ref. AN32

Component Stress/Warning Flags



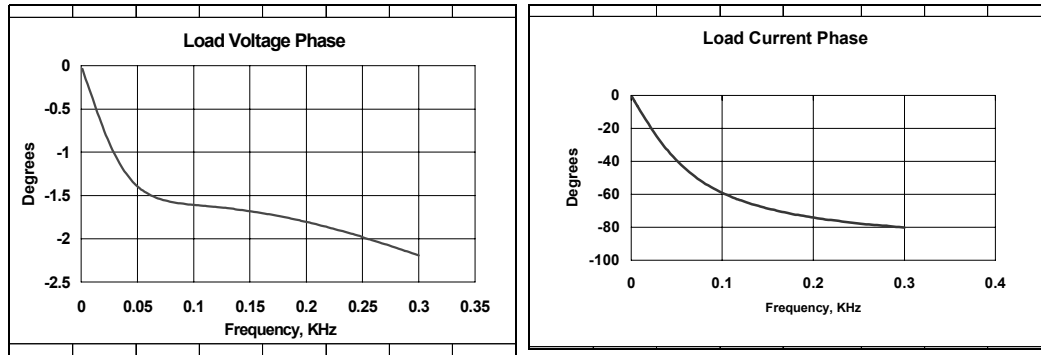
Power Design calculates voltage and current stress levels on L1 and L2, plus C1 and C2 for all designs. Resonance of these filters can produce voltages and currents larger than the load levels. Button 84 will place the first graph on the screen, then scroll up and to the right to view other graphs. The currents shown here can be used directly for all filter topologies. If L1 is actually two inductors, half the voltage shown will be across each individual inductor.

This circuit example only has a 90V supply; the drive signal is only 85Vpk; the load resistance has risen to 15Ω even though the filter design was for a 10Ω load. We might initially expect the 85Vpk signal and the 15Ω to limit inductor current to about 5.7A, but L1 has current peaks of 10.1A and voltage peaks of 108V. These peak values are pointed out on the right.

For capacitors, peak voltage is calculated for both differential and grounded capacitors. If a ground capacitor would experience a negative voltage, The red flag pops up.

Ref. AN32

Filters in Servo Loops



These filters are notorious for introducing large phase shifts. This is usually not a problem when feedback is taken directly at the output of the PWM amplifier. In applications such as servo loops, feedback is taken after the filter and any phase shift introduced here affects system phase margin. Power Design calculates both voltage and current phase in the load.

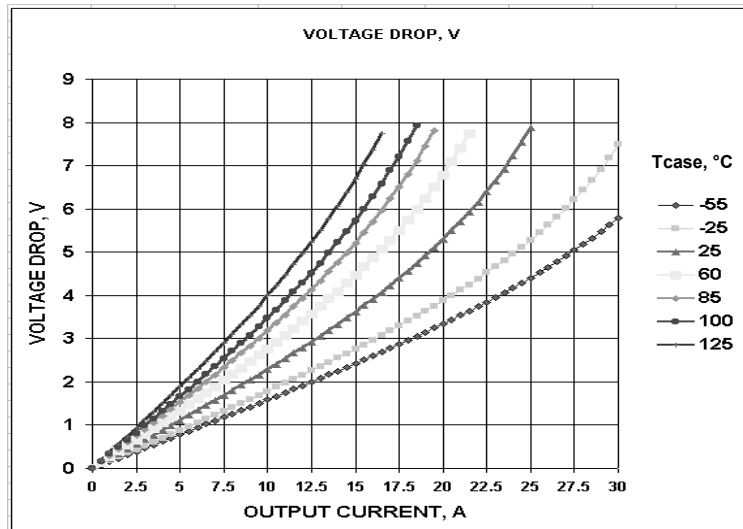
Voltage phase shift through a properly designed and terminated filter will be 45° per pole at F_c . This phase shift is reduced as the ratio between F_{max} and F_{cutoff} frequencies widens.

These graphs are from a 5mH, 2Ω magnetic bearing application featuring current output, third order filter with a cutoff frequency of 3KHz, and a modified matching network.

Ref. AN32

Keep it Cool!

$$R_{on} = f(t_j)$$



The “on” resistance of a power MOSFET increases a little over two times as junction temperature rises from +25°C to +150°C. This means a larger heatsink increases both output capability and efficiency. If there’s good news to this story it’s the non-linearity of the curve: The first few degrees we lower temperatures buys the most. Here’s a way to approach the problem.

First order power dissipation in the PWM is a function of the output current and the voltage drop at that current. This is the PWM advantage over linear power delivery; supply voltage is not part of the equation. Start with the 60°C curve (interpolate if required). Find your current (PEAK if below 60Hz, otherwise RMS) and read the voltage drop. The product is power dissipation. The voltage drop divided by supply voltage approximates efficiency (quiescent current of both Vcc and Vs will reduce this a little). The heatsink rating is 60°C minus ambient temperature, divided by power.

Are these numbers all affordable? Remember that a bigger heatsink actually reduces the watts to be dissipated (unlike linear systems).

Ref. AN32,AN39

PWM Power Dissipation

Calculating Power Dissipation for Apex PWM amplifiers									
Model	SA03	Read Me	Ta max =	25	Tj max =	150	Tc max =	85	
Power for Sine Wave Outputs			Fc(KHz) =	4	N =	2			
Vs	90 Volts		Fswitch =	22.5 KHz			Irripple =	0.932806782 A	
Fmin	0.001 KHz		Iq Vcc =	0.08 A			Iout =	8.500476297 A	
Fmax	2 KHz		Piq Vcc =	1.2 W			Ifet =	8.551504299 A	
Sig	85 Units		Iq Vs =	0.066795 A			Fhotspot =	0.0599 KHz	
Sig as ?	V peak	Note/W	Piq Vs =	6.01155 W			Minimum Heatsink:	2.54225414 °C/W	
			Max delta Tj =	125			Max delta Tc =	60	
General Procedure:		First Filter Design	Tune the filter		Select the heatsink				
Actual HS:		1 °C/W					R PchFET	0 Ohms	
Approx. Power Out	361.2499818	Wrms					R NchFET	0.12956009 Ohms	
Estimated Internal Pwr	20.3424608	W					Rwire	0.05 Ohms	
Estimated Case temp.	46.0680827	°C					Rtotal	0.17956009 Ohms	
Est. Junction temp	50 °C	Read me					D.C.max	99 %	
Efficiency @ Fhotspot	94.66906088	% (AC Amplifier Only)	NA				% (DC Amplifier Only)		
Est. Vpk capability	87.52934768	V					Vpk out	8.747223943	
Notes:									
Filter:	Rl= 10, Cl= 99999999999999, Ll= 0, Cm= 99999999999999, Lm= 0, Rm= 99999999999999								
37 Define Load		Sweep the Frequency		65 View Amp Out Last Sweep		84 View Filter component Graphs		71 View Load Last Sweep	Page down for charts.
68 Print Data									

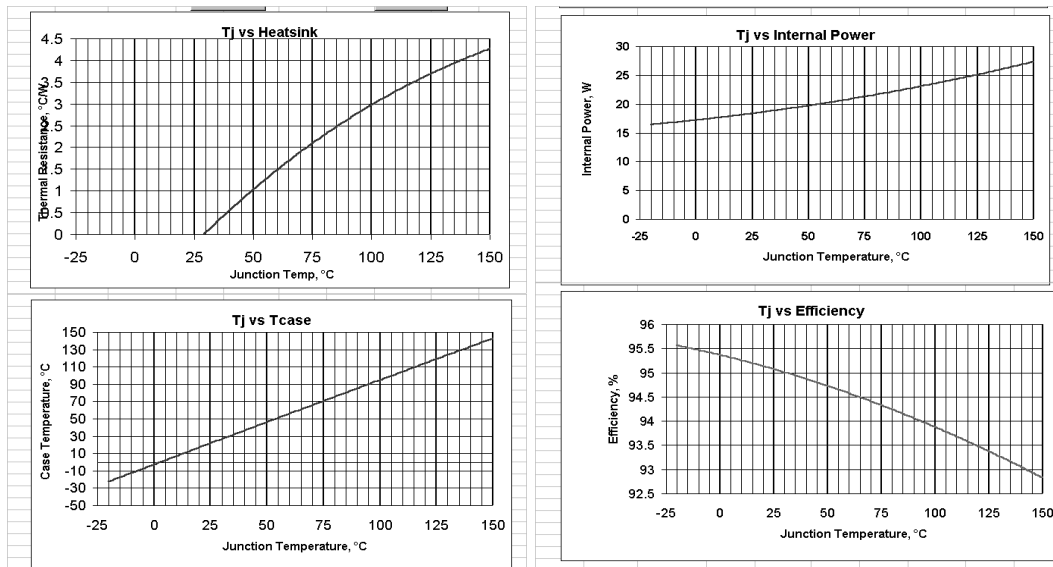
Did someone complain about lack of detail on the previous page? Here they are, and the inputs were transferred from the PWM Filter sheet. If you change a green cell value, blue cell answers will not be valid until you run a frequency sweep.

If you get errors when you do this at home, check the READ MEs. You need the Analysis Toolpak add-in. Now you can see in the upper half, quiescent powers calculated, plus output current, FET current, hotspot frequency and best of all, minimum heatsink.

A little lower, notice I have already input an acceptable heatsink value and operating points have been calculated. Please read the comments. The Power Output assumes a properly terminated, zero loss filter, and a power factor of 1 in the load. Use button 82 to see efficiency including filter losses. If you enter too small a heatsink, most of these answers will be forced to ridiculously large numbers and a red TOO HOT warning will appear.

Ref. AN39

Find a Heatsink Rating







In the upper left graph it looks like a quite small heatsink will keep junction temperatures below maximum. However the graph below says there is little difference between junction and case temperatures and we surely want to keep case temperature a lot lower than 150°C.

On the top right we see that internal power dissipation of the amplifier changes with junction temperature - - or with the size of the heatsink. Below we see this same effect expressed in terms of efficiency. This is a relatively low power PWM application. With higher power applications the percentage point change shown on this graph will increase.

Ref. AN39

Find a Heatsink

Selecting an Apex Heatsink											See ACCESSORIES INFORMATION data sheet for specifications	
Thermal Resistance		Package		Velocity Calculator:						Units of Measure:		
2.3 °C/W		MO127		100 CFM						9.5 Inch Width		
				10 Inch Dia						12 Inch Length		
READ ME		Update heatsink List		183.3465 Ft/min						126.32 Ft/min		
				0.931412 M/sec						0.6417 M/sec		
Notes:												
Beware: Flow rates change as you enter Thermal Resistance, but may be wrong until the Command Button is used!												
Model	Fluid	Thermal resistance, free air, °C/W	Your rating requires FPM or GPM flow	Package(s) accepted	Style	Length, inches or cm	Width, inches or cm	Height, inches or cm	Weight, ounces or grams	Singles Price USD Domestic		
HS06	Air	0.96		0 MO127		4.5	6.25	2	19.8	\$42.25		
HS11	Air	0.68		0 TO-3,MO127		6	8	2	44.8	\$214.80		
HS11	H2O	0.68		0 TO-3,MO127		6	8	2	44.8	\$214.80		
HS18	Air	1		0 MO127		5.5	4.612	1.5	14.1	\$80.95		

Believe me, heatsinking is NOT the easiest science in our universe.

Let's start with "the" heatsink rating. The HS03 is rated at 1.7°C/W in free air. True, when power dissipation is about 45W, but check the actual curve at 10W and you'll find a rating more like 2.3°C/W. On top of that, "free air" means no obstructions to air flow and the flat mounting surface must be in the vertical plane. Demands for higher performance in smaller packages can be at odds with optimum heatsinking. Poor installation choices can easily reduce effectiveness 50%.

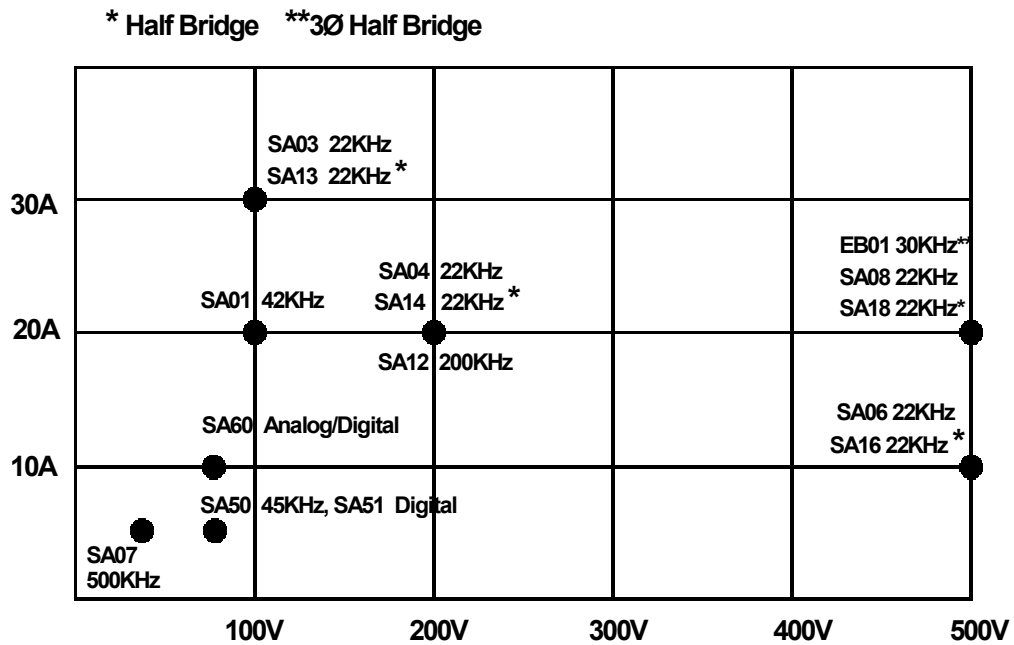
Moving on to this selector software. Air velocity curves from the heatsink data sheet (when available) have been approximated with polynomial expressions. While these errors are minor compared to the previous paragraph, it would be good to allow 10% for velocity ratings over 150 feet per minute and 20% below that.

Adding a fan to your design enables you to use smaller heatsinks. Please remember: Most fans are rated in cubic delivery and this rating varies with working pressure. A 5 inch diameter fan delivering 100 CFM produces over 700 FPM right at the fan. If this air is flowing through a 19 x 24 inch rack, theoretical velocity is down to 32 FPM, will vary with location and goes lower as the rack is sealed tighter.

The bottom line: Without case temperature measurements, your design effort is NOT complete!

Ref. AN39

PWM AMPLIFIERS

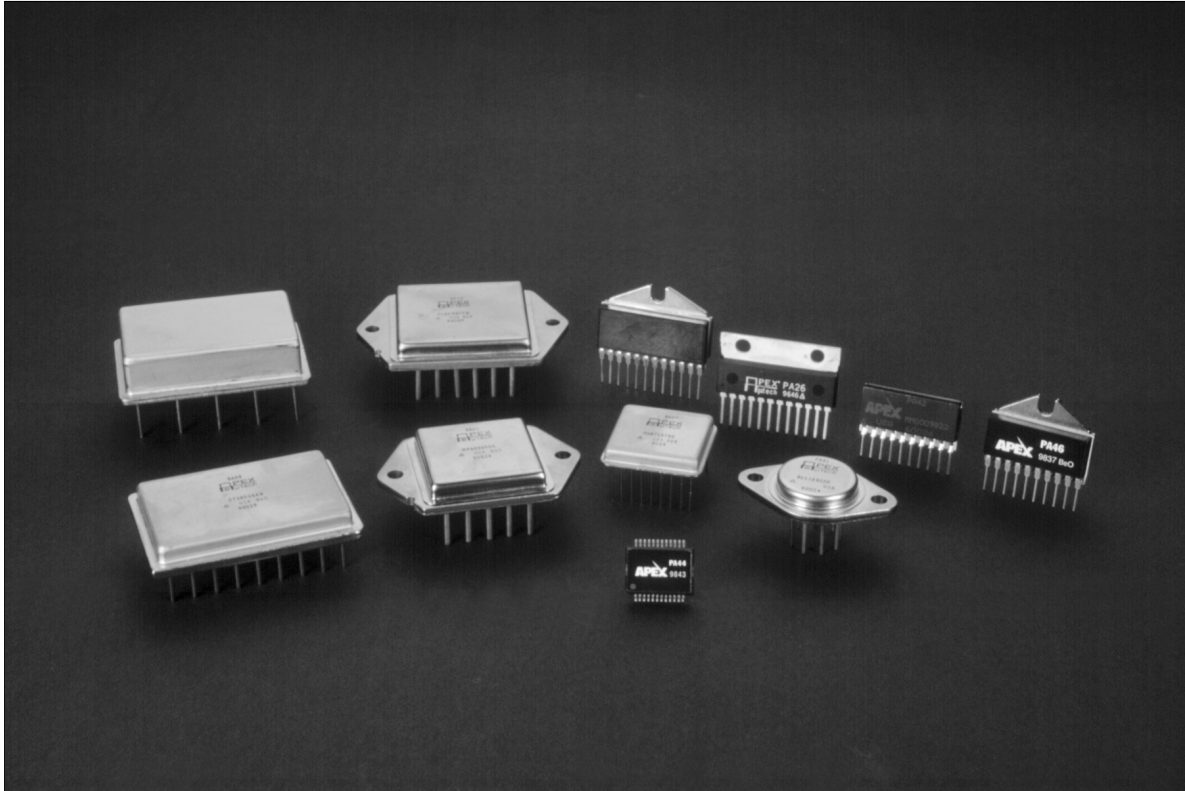


Data as of December 2000.

APEX'S WORLD OF POWER OP AMPS



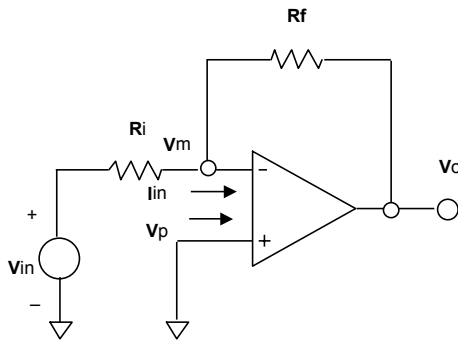
APEX is the industry leader in monolithic and hybrid high current and high voltage power amplifiers. With more than 70 different models, we provide solutions for designs requiring output current greater than 1A or total supply voltages above 100V. When considering the cost versus performance trade-offs between using a power op amp versus discrete circuits, you must figure in design time, troubleshooting, procurement as well as production costs, not to mention labor, as well as the reliability factors. More often than not, you will find *it does not pay to be discrete!*



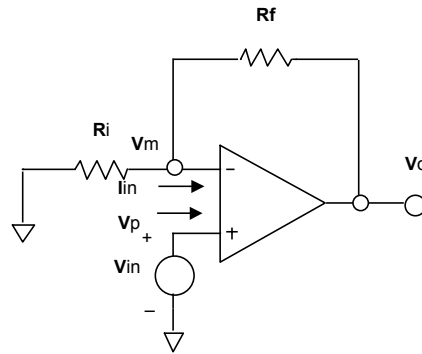
Apex offers a wide variety of packaging solutions to meet your needs. The 8-pin TO-3 is cost effective and easy to heatsink. The 10 and 12 pin Power Dips share the same rugged construction features but offer larger area for increased power handling capability. The power SIPS are easy on real estate and their flat back mates to a wide variety of heatsink options. The surface mount packages promise the ultimate in circuit density. All models featuring monolithic construction are also offered in chip form.

Ref. Packages data sheet

LINEAR OPERATION BASICS



$$\begin{aligned} V_m &= V_p = 0 \\ I_{in} &= 0 \\ \frac{V_{in}}{R_i} + \frac{V_o}{R_f} &= 0 \\ V_o &= -V_{in} \frac{R_f}{R_i} \end{aligned}$$



$$\begin{aligned} V_m &= V_p = V_{in} \\ I_{in} &= 0 \\ \frac{V_o - V_{in}}{R_f} + \frac{0 - V_{in}}{R_i} &= 0 \\ V_o &= V_{in} \left(1 + \frac{R_f}{R_i} \right) \end{aligned}$$

Before we discuss non-linear operation, we will cover some of the basics of linear operation for that mythical creature, the "ideal op amp". The three most important characteristics of an ideal op amp are:

1. Infinite input impedance
2. Zero output impedance
3. Infinite open loop gain

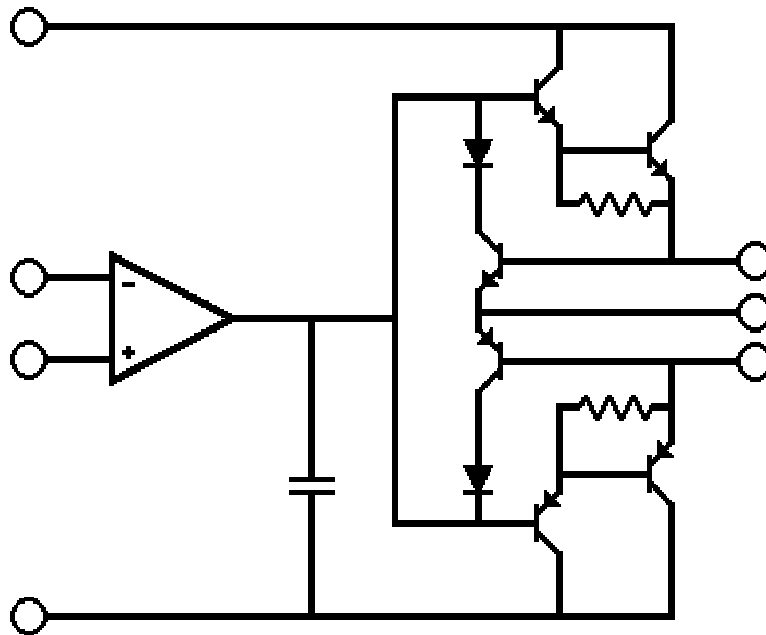
Let's review the inverting configuration in light of these three basic characteristics. #1 dictates that the input current into the op amp is 0. #3 implies that any voltage appearing between the input terminals will result in infinite output voltage. The resistive divider action of R_f and R_i causes a portion of the output voltage to be fed back to the inverting input. It is this **NEGATIVE FEEDBACK** action coupled with #3, open loop gain, that keeps the voltage between the two inputs at zero.

In the inverting configuration, this results in a "virtual ground" node. The concept of a virtual ground, coupled with the zero input current flow, allows the "closed loop gain" or transfer function of the circuit to be easily calculated. Current flow in R_i is equal to V_{in}/R_i . The same current is forced to flow through R_f , giving an output voltage of $-I_{in}R_f$.

In the non-inverting amplifier, the infinite open loop gain of the amplifier, coupled with negative feedback, force the inverting terminal to be equal to the non-inverting terminal. This sets up a voltage across R_i which develops a current that also flows through R_f . Therefore, the total output voltage is $s V_{in}/R_{in}$ current times the series combination of R_f and R_i .

Ref. AN 31

Class C Output Stages

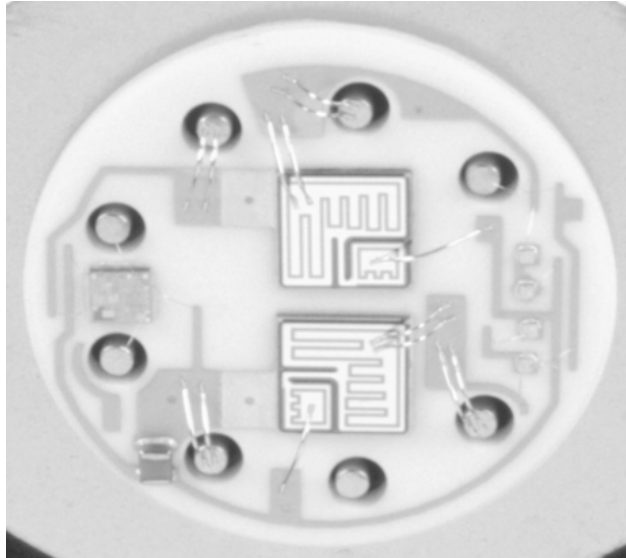


Class “C” output stages tie the bases or gates of the power devices together. Omitting the usual bias network between these bases reduces cost with the penalty of increased crossover distortion.

Assuming a resistive load and the drive stage voltage in the range of $\pm 0.6V$. There is no output current because the power devices need about a V_{be} to turn on. There is a dead band of about 1.2V which the driver must cross over before output current can change polarity. For MOSFET outputs this dead band is usually somewhere between 4 to 6V.

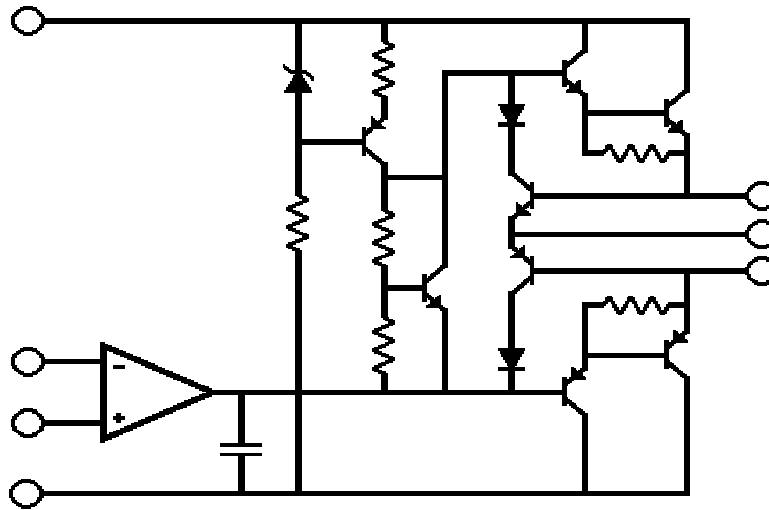
The good news is that because the output does not move, there is no feedback to the driver. It is running open loop during dead band transition and slews across as fast as it can. This means at low frequencies this distortion is quite low. Class “C” outputs are generally not recommended above 1KHz but this varies with tolerance of distortion.

PA51



With a minimum transistor count and no resistors, the class “C” amplifiers enjoy a roomy layout. The power transistors are soldered to silver thick film conductors. Small signal devices are epoxied and wire bonded to gold thick film conductors. Wire bonds are 1 mil and 5 mil diameter. The white ceramic substrate is beryllium oxide (BeO) which spreads the heat over a wide area before it travels through the steel header. The substrate is also solder attached.

Simple Class AB Outputs

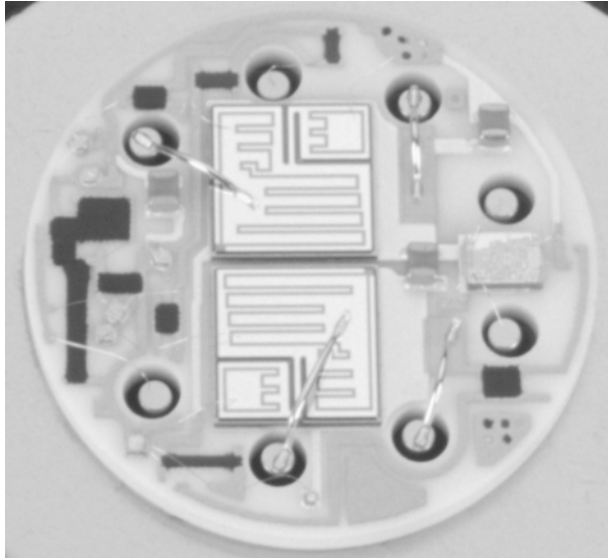


The class “AB” output keeps some current flowing in the output transistors at all times to minimize crossover distortion. This area is still the largest contributor to total harmonic distortion but the “dead” band is gone.

The circuit is known as a V_{be} or V_{gs} multiplier. Think of this transistor as a non-inverting op amp with the V_{be} (V_{gs}) as an input and two about equal input and feedback resistors. If the multiplier transistor and the output transistors are tightly thermally coupled, distortion can be kept low and the possibility of thermal runaway is eliminated. This is one area where the hybrid really shines over a discrete circuit because these transistors are physically and thermally close to each. Many Apex amplifiers also use thermistors to compensate for tracking differences due to the transistors being different types. Imagine the tracking differences when the multiplier and power transistors are in separate packages.

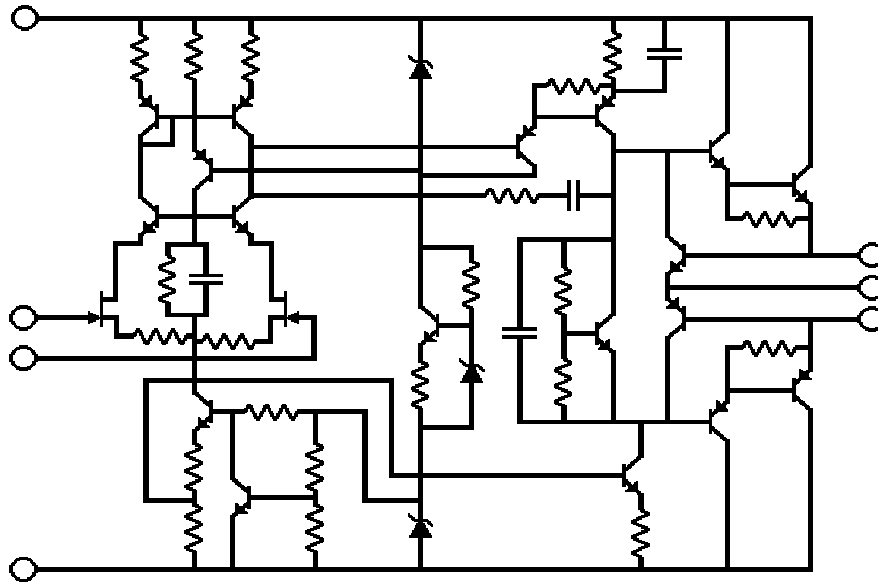
We refer to this as a simple amplifier because of the monolithic driver stage which may incorporate 50 to 100 transistors on a single chip.

PA12



The black areas are thick film resistors which are very cost effective because many resistors can be screened on a single pass and they require no wire bonding. Their intimate contact with the substrate makes them run cool. Wire size here jumps to 10 mils. On higher current products we also use 15 and 20 mil wire.

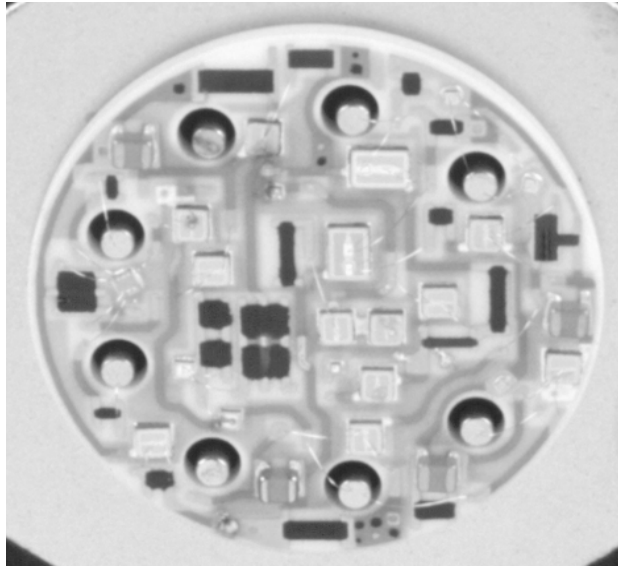
Complex Amplifier



Here is the most difficult and costly way to build a power op amp. Monolithic driver candidates are often lacking in performance above $\pm 15\text{V}$ and above $\pm 40\text{V}$ the picture is down right discouraging.

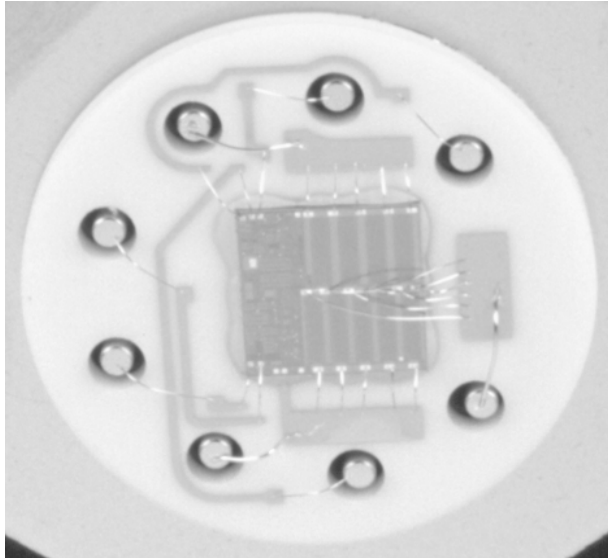
Being able to select each individual transistor for optimum overall performance of the power op amp results in DC accuracy under 1mV , speeds to $1000\text{V}/\mu\text{s}$ or total supply voltages to 1200V .

PA85



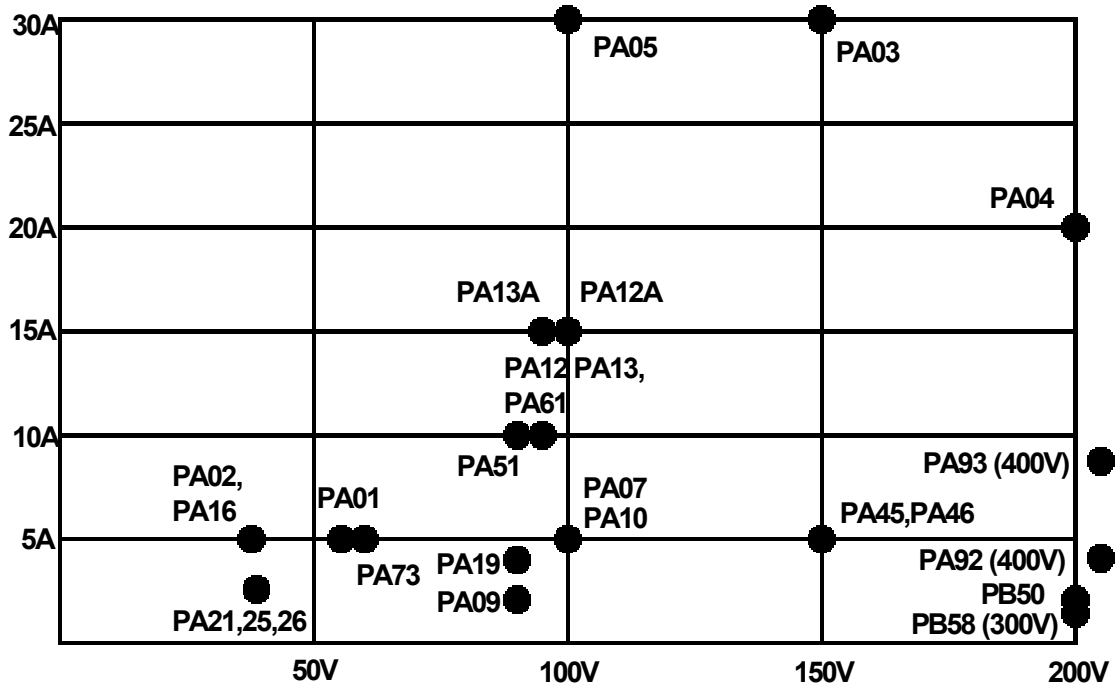
Real estate is at quite a premium with the complex designs. The only new thing added here is the blue glass layer covering most of the conductor traces. It has a two fold purpose: It is a bonding aid and an electrical insulator. This model happens to be a 450 volt part.

PA45



This photo represents the latest technology advance in power op amps. Having only one chip enhances reliability and lowers cost plus enables smaller packages all at the same time. This amplifier is a 150 volt, 5 amp model.

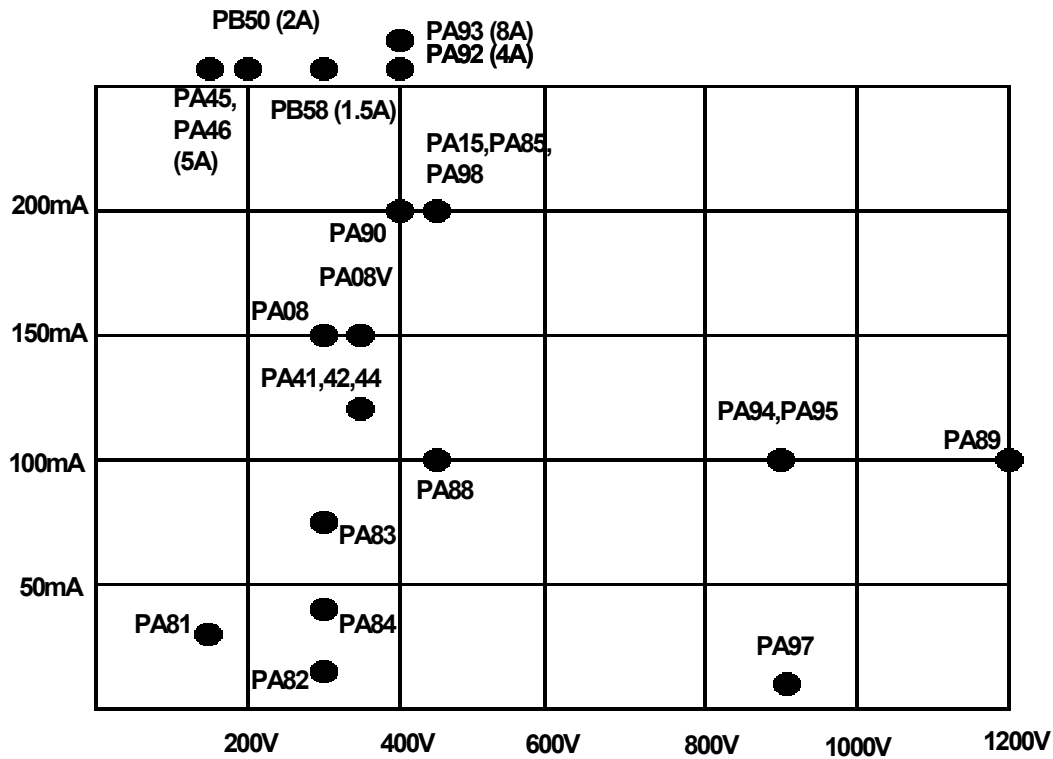
High Current Amplifiers



From the plastic packaged PA26 for USD\$4.95 @1K to the PA03 for USD\$525 @1, Apex covers a very wide spectrum of multiple ampere models. Typical power response ranges from 13KHz to 3.5MHz.

Data as of December 2000.

High Voltage Amplifiers



You are looking at the widest selection of high voltage op amps anywhere. From the surface mount PA44 for USD\$36.20 to the PA89 for USD\$525. Typical power response ranges from 5KHz to 500KHz.

Data as of December 2000.

Apex Model Conventions

- PAxx Power Op Amp
 - No suffix Standard model
 - “A” suffix Improved performance via grade out
 - “M” suffix Military screened model
 - No design differences
- PBxx Power Booster
- SAxx Switching Amplifier (PWM)
- EBxx Triple Half Bridge Power Stage

The PA power op amps are indeed operational amplifiers following all the rules for these basic building blocks where in a properly designed circuit performance is controlled by feedback rather than op amp parameters.

The “A” suffix indicates electrical grade out for improved DC accuracy and sometimes voltage capability, temperature range or speed.

The “M” suffix indicates a part with identical design to the standard but with military screening added. Various models are offered as non-compliant (Apex verified), /883 (government verified) or SMD (government verified and controls the drawing).

The PB power boosters are a unique cost effective solution providing a programmable gain from 3 to 25 at voltages up to $\pm 150V$ and up to 2A. They are usually configured as the power stage of a composite amplifier which then acts like a power op amp. With the front end of the composite being a low cost typically $\pm 15V$ op amp, speed and accuracy are easily tailored to need of the application.

PWM amplifiers come to the rescue when internal power dissipation gets out of hand with linear devices.

Model Selection: Step 1

Part Selection				Read Me																					
Most positive peak output				63 Volts																					
Most negative peak output				-63 Volts																					
Output current				5.5 Amps																					
Frequency				1.2 KHz																					
DUAL																									
Model	Vss Min	Vss Max	Iout Continuous Max A	Vdrop (Saturation V)	Common Mode V	Power Bandwidth KHz	Type	Iq mA Max	Int. Power W Max	Pkg Style	Singles Price USD Domestic	Voltage Offset mV max	Vos Drift uV/°C Max	Eval Kit Sold Separately	Amplifier Type	Current Limit	Thermal Shut-down	Thermal Washer	Socket	Cage Jack					
SA60	0.1	80	10	4.3		25.0	12	140	SIP03	\$ 134.95				EK06	PWM Full	None	No	TW13	MS06						
PA93	80	400	8	10.8	15	126.3	14	125	SIP03	\$ 202.05		10	50	EK16	Op Amp	Adjust	No	TW13	MS06						
PA04	30	200	20	6.9	8	64.4	90	200	MO-127	\$ 252.00		10	50	EK04	Op Amp	Adjust	No	TW05	MS05	MS04					
PA04+Vb	30	200	20	4.6	8	64.4	90	200	MO-127	\$ 252.00		10	50	EK04	Op Amp	Adjust	No	TW05	MS05	MS04					
SA01	16	100	20	2.4		4.2	78	185	PD10	\$ 375.00		10		EK01	PWM Full	Adjust	Yes	TW10	MS04	MS04					
SA12	16	200	15	3.9		20.0	200	250	MO-127	\$ 481.50				EK17	PWM Full	Adjust	Yes	TW05	MS05	MS04					
SA03	16	100	30	1.5		2.3	73	300	MO-127	\$ 517.50				EK03	PWM Full	Adjust	Yes	TW05	MS05	MS04					
SA04	16	200	20	2.1		2.3	73	300	MO-127	\$ 517.50				EK03	PWM Full	Adjust	Yes	TW05	MS05	MS04					
PA03	30	150	30	4.6	10	20.2	300	500	MO-127	\$ 525.00		2	30	EK09	Op Amp	Fixed	Yes	TW05	MS05	MS04					
SA06	16	500	10	9.1		2.3	112	300	MO-127	\$ 628.50				EK05	PWM Full	Adjust	Yes	TW05	MS05	MS04					
SA08	16	500	20	2.9		2.3	90		MO-127	\$ 634.20				EK15	PWM Full	Adjust	Yes	TW05	MS05	MS04					
PA45	30	150	5	10.5	10	68.2	50	85	TO-3	\$ 44.80		10	50	EK09	Op Amp	Adjust	No	TW03	MS03	MS02					
PA46	30	150	5	10.5	10	68.2	50	75	SIP02	\$ 44.80		10	50	EK12	Op Amp	Adjust	No	TW13	MS06						

Amplifier requirements have been entered into the yellow cells and the command button used to calculate suitability and sort by cost. For each parameter, the suitability ratio is 1 if the product meets (or exceeds) the requirements or is equal to requirement/capability. The sum of the ratios is used to sort the list.

In this example we see both switching and linear solutions meeting all the application requirements spanning more than a 4.5:1 price range. Vss min and max are data sheet specifications while +Vs and -Vs are estimations of supply requirements for this specific application (accounts for Vdrop or Saturation Voltage at the application output current). Note the blank cells where parameters do not apply to PWM amplifiers.

Here we find the SA60 is the “best” choice. However, the selection process knows nothing about noise tolerance of the application, space and weight limitations for heatsink and filter inductors, duty cycle of the output signal, accuracy requirements, military screening needs or - - - -. This is a good tool, but we still need an engineer to complete the job.

Even though Dilbert would have a fit, we may even find that talking to marketing would be a good idea. Note the last two lines where the output current spec is shaded because the amplifiers do not meet the application requirements. This indicates we may be able to reduce cost 3:1 if the output current specification could be reduced only 10%!

ELECTRICAL LIMITATIONS

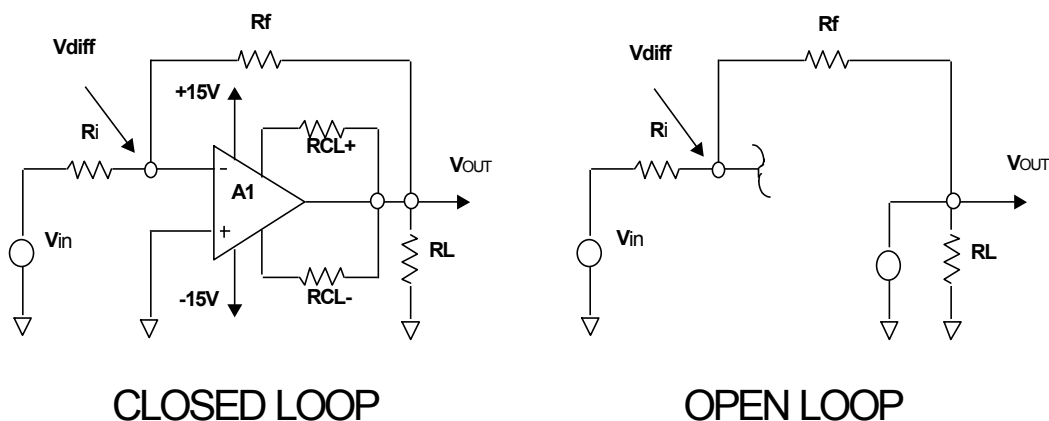
EFFECTS ON THE AMPLIFIER

- Slew Rate Limiting
- Output Saturation
- Current Limiting
- Shut Down
- Common Mode Requirements

Power amplifiers and small signal op amps share many limitations. Understanding the limitations of a standard op amp will help you design more accurate, reliable circuitry. It helps to have a good understanding of what happens to an amplifier when it operates outside of its linear region. Most of these electrical limitations can be traced to this common denominator.

NON-LINEAR OPERATION

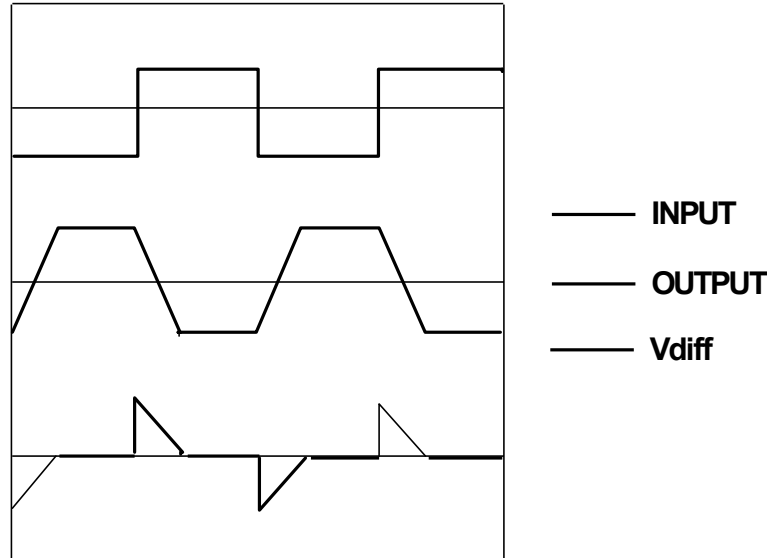
OPEN LOOP MODEL



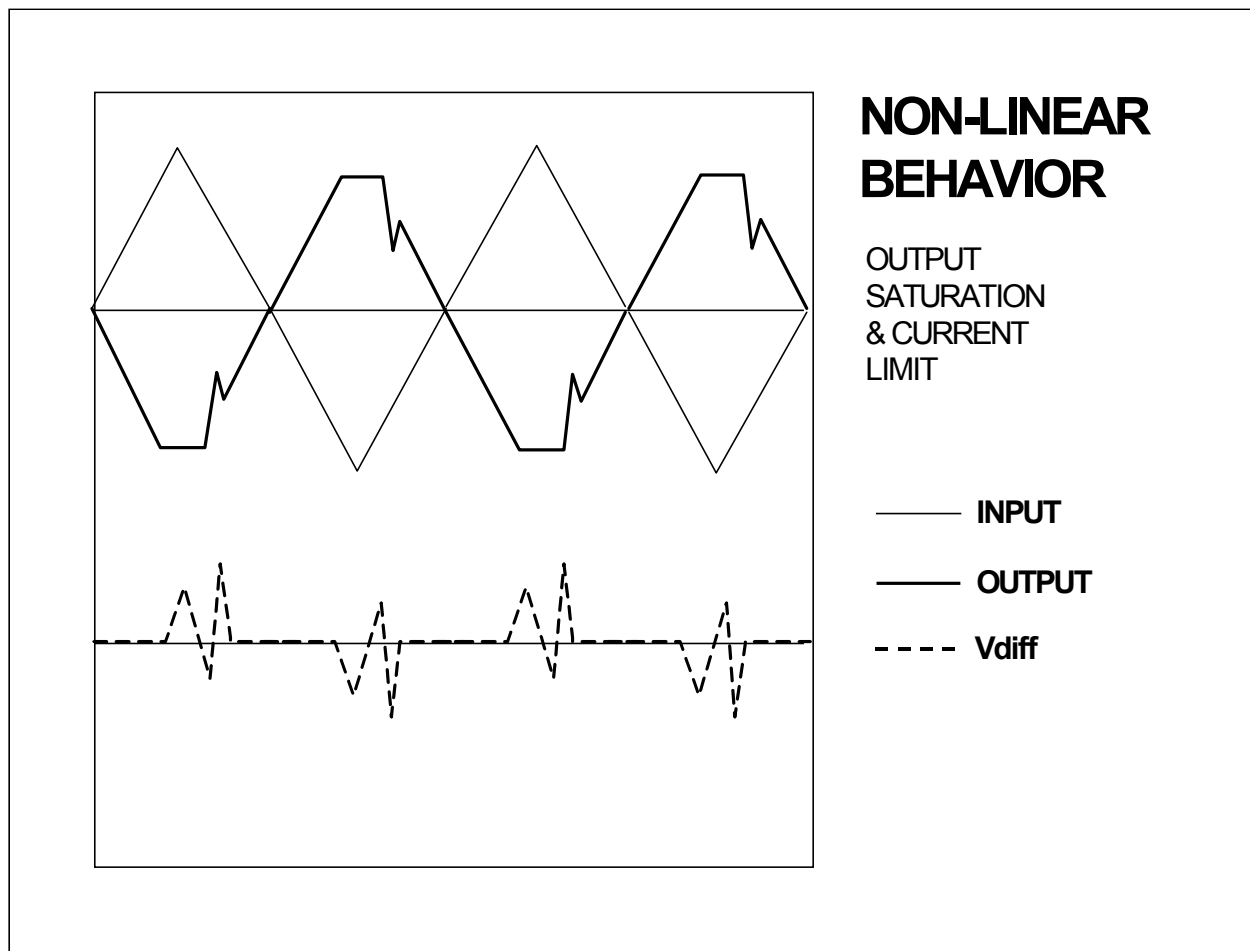
When an amplifier is operated in a closed loop it exhibits linear behavior. A violation of any of the limitations mentioned earlier will effectively open the loop. Once the loop is opened, V_{in} and V_{out} appear as two independent voltage sources. R_f and R_i function as a simple voltage divider between the two resistors. This voltage appears as a differential input voltage. In cases where the output stage is in a high impedance state, such as power off or thermal shutdown, V_{out} goes away and V_{in} is divided down by the series combination of R_{in} , R_f and R_{load} .

NON-LINEAR BEHAVIOR

SLEW RATE LIMIT

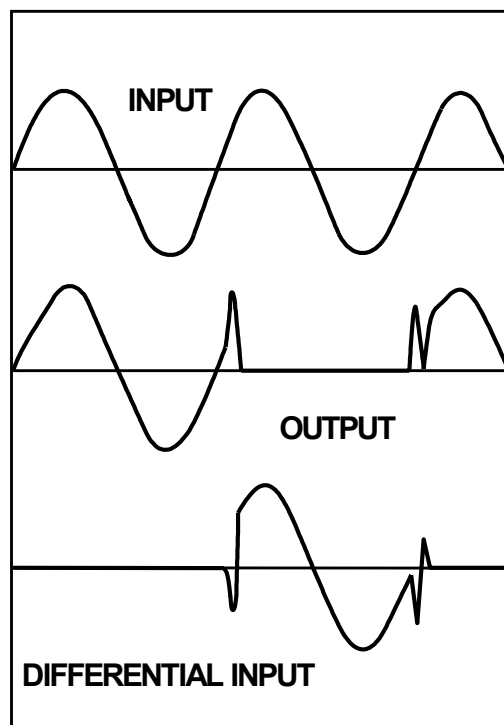


The effect of operating the amplifier in the slew limited region can be seen most dramatically by applying a step voltage to the input. Since the output of the amplifier cannot keep up with an infinite dV/dt , it goes into slew limited mode and begins changing its output voltage. At the point the amplifier goes into slew limit, we can use our "disappearing op amp" model to visualize what happens at the inverting input node of A1. In the example above, at $t=0+$, the input voltage has changed from +10 volts to -10 volts, but the output voltage has not yet changed from -10 volts. Therefore, -10 volts will be on both sides of the divider comprised of R_F and R_I . Since there is no voltage difference, the full -10 volts will appear as V_{DIFF} . As the output tries to "catch up", the right side of the divider will be changing linearly to +10 volts, therefore the differential voltage will drop linearly until the output catches up with the input. When the output catches up, the loop is closed and the differential voltage is zero.



Output saturation and current limit exhibit similar behavior — clipping on the amplifier output. This clipping produces differential input voltages.

Any type of clipping can result in an overdriven condition internal to the amplifier. This can lead to recovery problems ranging from simple long recovery to ringing during recovery.



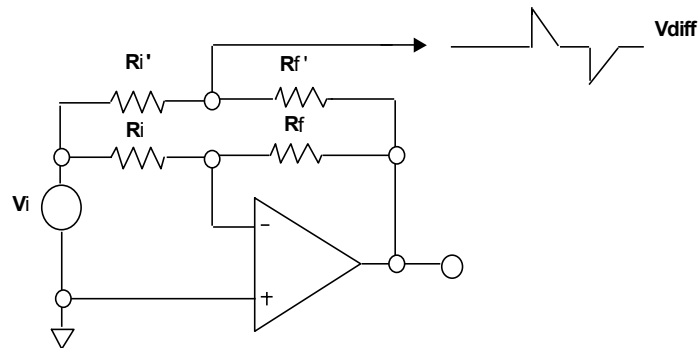
NON-LINEAR BEHAVIOR

THERMAL
SLEEP
MODE

The situation with sleep mode is similar to thermal shutdown. In both cases, the amplifier is disabled by some circuitry which results in the output going into a high impedance state. One additional caution is that when coming out of sleep mode, an amplifier may saturate to one of the rails before recovering.

NON-LINEAR OPERATION

DETECTING PROBLEMS



FALSE SUMMING NODE TECHNIQUE

The common denominator of all non-linear modes of operation is the appearance of differential input voltages. One method of sensing when an amplifier is in a non-linear region is to use this false summing node technique.

If $R_f'/R_i' = R_f/R_i$, then V_{diff} equals the voltage at the inverting node of the amplifier. This buffered error voltage signal can be used as an error flag possibly to drive a logical latch that could shut down the system.

ABS Maximums vs. the Spec Table

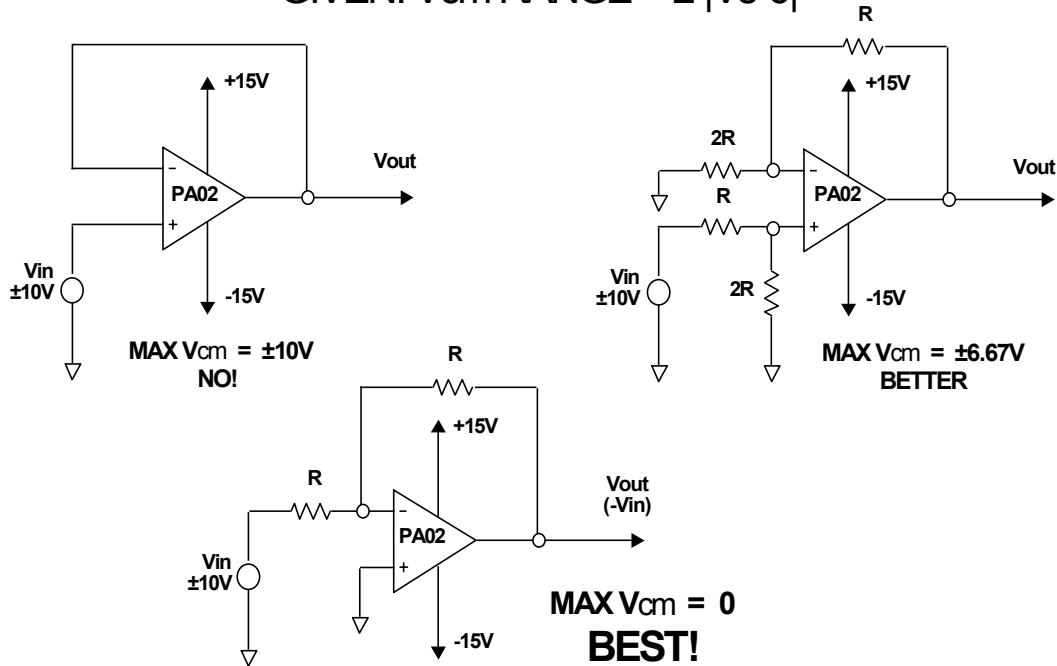
- ABSOLUTE MAXIMUM RATINGS
 - Stress levels, applied one at a time, will not cause permanent damage.
 - Does NOT guarantee op amp performance
- SPECIFICATIONS
 - Linear operation ranges
 - Vos, Ib, drift, CMRR... guaranteed performance

Beware that one stress level may bring on a second, which calls off all bets on op amp survival. Consider a commercial part where the last line of the specification table called "TEMPERATURE RANGE,case" is listed as -25/+85°C. Even though the ABS MAX temperature is 125°C, the part may latch up (very large voltage offset) at 86°C. With loads such as DC coupled inductors this may also lead to violation of the SOA.

Ref. AN1

COMMON MODE VIOLATIONS

GIVEN: $V_{cm} \text{ RANGE} = \pm |V_s - 6|$



In an inverting configuration, the op amp's non-inverting terminal is usually tied to ground, making the inverting terminal a "virtual ground." This results in zero common mode voltage: a desirable benefit. However, operating the amplifier in a non-inverting mode results in the common mode voltage being equal to the voltage at the non-inverting terminal.

The schematics above illustrate the problem. The amplifier used in this example cannot have any common mode voltage that approaches within 6 volts of either supply rail. The first example shows a unity gain follower. This is the configuration where common mode violations are most common. Note that the input voltage is equal to the common mode voltage. In our example the input voltage exceeds the common mode range.

In the second example the input signal is first attenuated and then gained back up to result in a lower common mode voltage but a unity gain non-inverting transfer function. That is:

$$V_o = V_i(2R/(2R+R))(1+R_f/R_i)$$

$$\text{where } R_f = R \text{ and } R_i = 2R$$

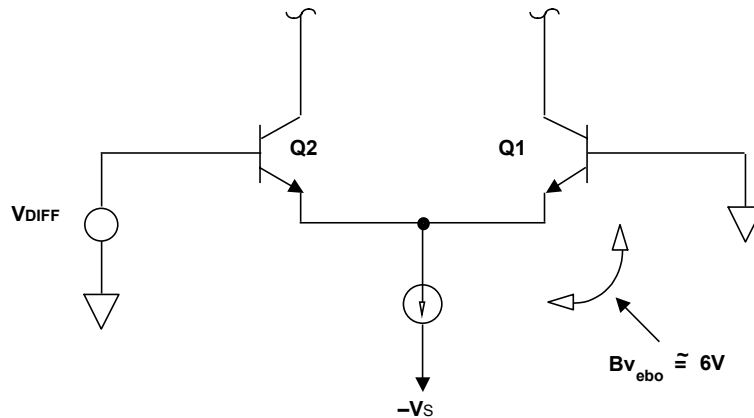
The third example shows the best approach to eliminating common mode violations: use inverting configurations. In this case the input voltage is still 10 volts, the output voltage is 10 volts, but the common mode voltage is zero, eliminating the problem. Of course this does invert the phase of the output signal.

Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

AMPLIFIER PROTECTION ELECTRICAL

- Input Transients
- Output Transients
- Over-voltage

WHY DIFFERENTIAL INPUT PROTECTION?



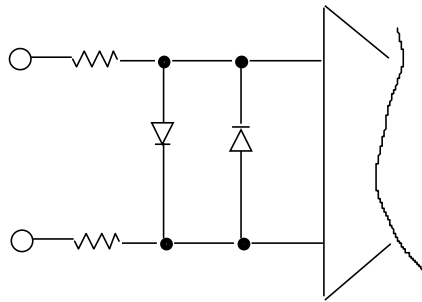
WHY DIFFERENTIAL INPUT PROTECTION?

Simple, to avoid damaging input stages due to differential overstress. Any input stage has maximum differential limits that can be exceeded any number of ways, with the most subtle occurring during non-linear operation.

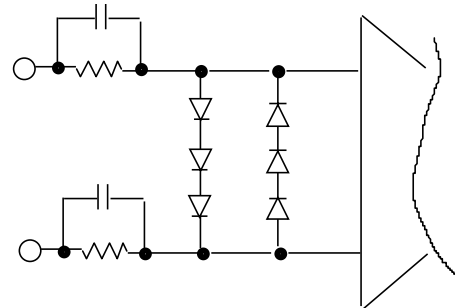
In amplifiers with bipolar inputs, such as a PA12, differential overload has the additional hazard of causing degradation without catastrophic failure. Exceeding the reverse-bias zener voltage of a base-emitter junction of a transistor used in a differential amplifier can permanently degrade the noise, offset, and drift characteristics of that junction.

INPUT PROTECTION

DIFFERENTIAL



SIMPLE



ALLOWS OVERDRIVE

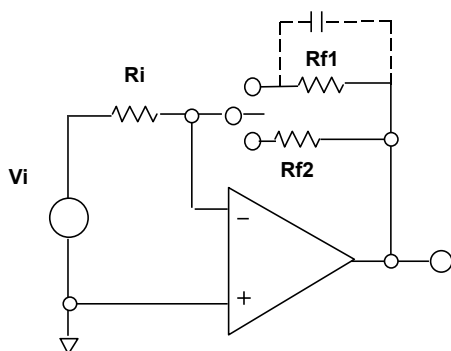
The protection scheme on the left uses parallel diodes to limit the differential voltage and uses series resistors to limit the current that flows through the diodes. The slightly more complicated scheme on the right accomplishes the same thing, but by using stacked diodes, allows a higher differential voltage to be developed. This allows a greater slew rate overdrive. The capacitors perform a similar function by allowing high frequency information to be passed directly to the input terminals.

Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

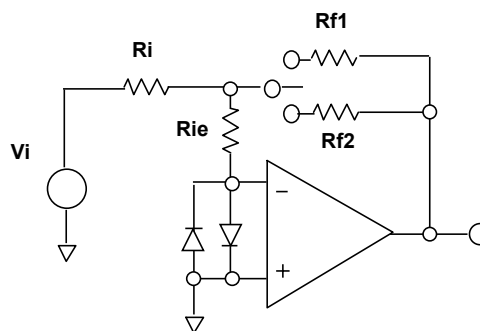
AN25 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS

GAIN SWITCHING

DON'T GET BURNED!



BAD



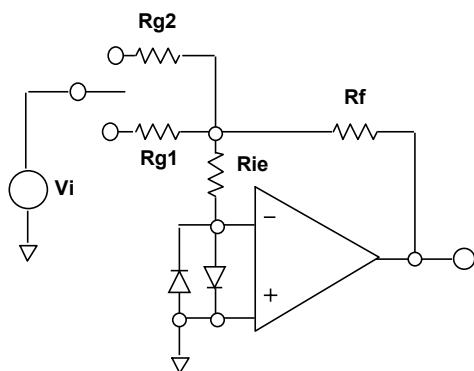
BETTER...

Often it is a requirement that the gain of an amplifier be switchable. This is very common in ATE applications. One method of doing this is shown on the left. This is a very poor way to accomplish gain switching. The problem is that the amplifier is usually much faster than the relay used to switch between the two resistors. WHEN THE RELAY OPENS, THE AMPLIFIER HAS NO FEEDBACK. Since the amplifier is now open loop, the amplifier will immediately slew toward one of the supply rails. By the time the relay closes, the amplifier will be saturated and the output voltage will appear directly at the inverting terminal of the amplifier.

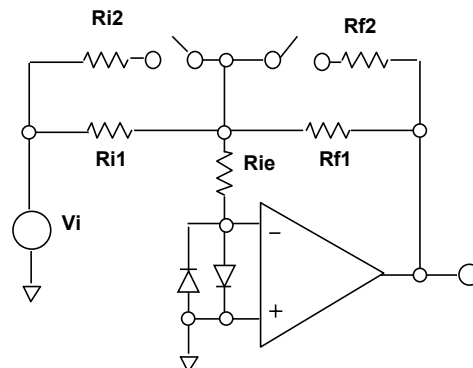
The method on the right does not solve the problem, but it does provide amplifier protection. The parallel diodes clamp the differential input voltage while R_{ie} limits the amount of current that can flow during transient conditions. The value of R_{ie} should be chosen to limit the current to approximately 15mA with one full supply voltage across the resistor.

Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

GAIN SWITCHING



GOOD



BEST

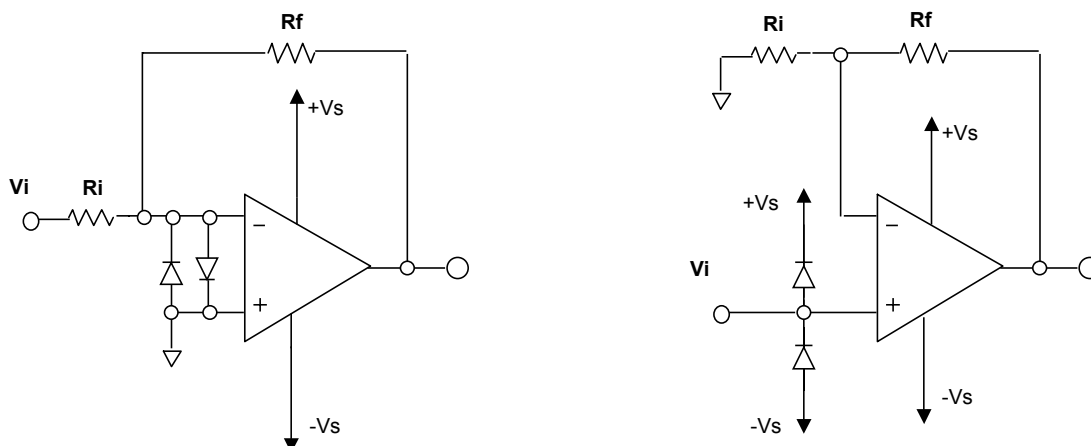
The "good" approach above represents a vast improvement over the previous technique. In this approach, gain is switched by switching the value of the input resistors rather than the feedback resistor. The major advantage to this approach is that the feedback loop is kept closed at all times. When the relay opens, the amplifier is now a unity gain follower with a zero volt input. The most voltage that will appear at the output is the offset of the amplifier. Input protection is still shown in this configuration to protect against possible switching transients.

The "best" approach above shows a configuration that prevents switching inside the feedback loop or opening up the input loop. R_{i1} and R_{f1} are in place at all times. The gain of the circuit is switched by EITHER switching in R_{i2} to parallel R_{i1} OR by switching in R_{f2} to parallel R_{f1} . This approach eliminates any transient voltages due to relay switching. At the time of contact closure, only the gain changes. Although input protection is still shown in this schematic, its only function is to protect the input in cases of non-linear operation, such as slew rate or current limit.

Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

INPUT PROTECTION

OVERVOLTAGE

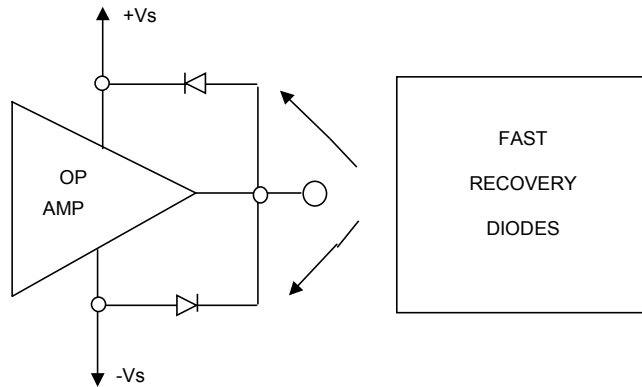


In multiple power supply systems, power supply sequencing is often a problem. If the power supplies for the "driving stage" come up before the "driven stage", the maximum input common mode specification may be violated. The diodes shown in the two circuits above serve to clamp the driven input to the amplifier supply pin so that the input cannot be raised above the supply voltage. Note, however, that if the supplies are in a high impedance state when the power supply is turned off, this approach will not protect the amplifier. Under those conditions however, the inverting amplifier configuration could be protected by running parallel diodes from the inverting node to ground. These would clamp the inverting input to ground under any circumstances. Since the inverting terminal is normally at virtual ground, these diodes would not interfere with signal in any way. However, on the non-inverting amplifier this approach will not work because the non-inverting input sustains a common mode voltage.

Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

OUTPUT PROTECTION

KICKBACK / FLYBACK



**NOTE: SUPPLIES MUST BE ABLE TO ABSORB
TRANSIENT ENERGY, i.e.: LOW IMPEDANCE**

Attempting to make a sudden change in current flow in an inductive load will cause large voltage flyback spikes. These flyback spikes appearing on the output of the op amp can destroy the output stage of the amplifier. DC motors can produce continuous trains of high voltage, high frequency kickback spikes. In addition, piezo-electric transducers not only generate mechanical energy from electrical energy but also vice versa. This means that mechanical shocks to a piezo-electric transducer can make it appear as a voltage generator. Again, this can destroy the output stage of an amplifier.

Although most power amplifiers have some kind of internal flyback protection diodes, these internal diodes **SHOULD NOT** be counted on to protect the amplifier against sustained high frequency kickback pulses. Under these conditions, high speed, fast recovery diodes should be used from the output of the op amps to the supplies to augment the internal diodes. These fast recovery diodes should be under 100 nanoseconds recovery time; and for very high frequency energy, should be under 20 nanoseconds.

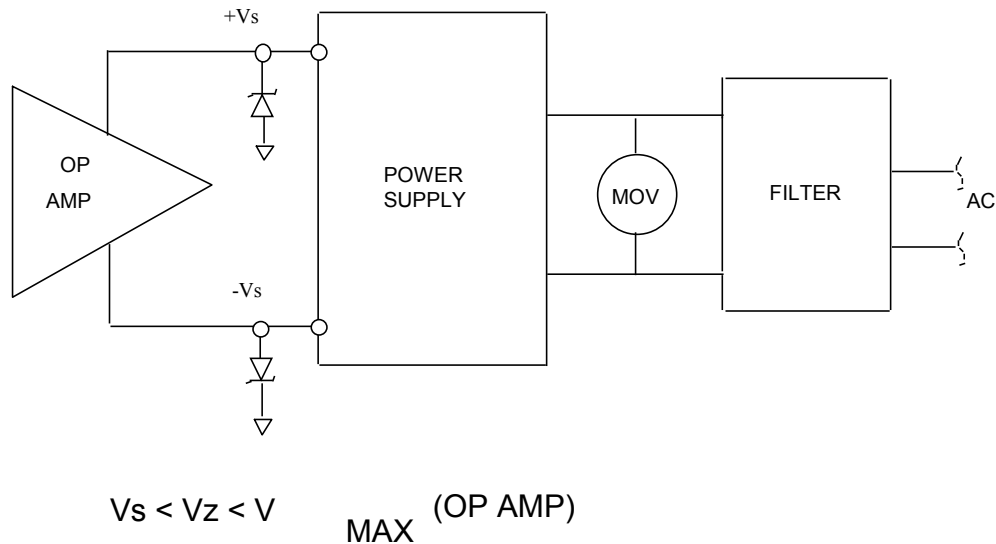
One other point to note is that the power supply must look like a true low impedance source or the flyback energy coupled back into the supply pin will merely result in a voltage spike at the supply pin of the op amp again leading to an over voltage condition and possible destruction of the amplifier.

Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

AN25 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS

AMPLIFIER PROTECTION

OVERVOLTAGE



The amplifier should not be stressed beyond its maximum supply rating voltage. This means that any condition that may lead to this voltage stress level should be protected against. Two possible sources are the high energy pulses from an inductive load coupled back through flyback diodes into a high impedance supply or AC main transients passing through a power supply to appear at the op amp supply pins. These over voltage conditions can be protected against by using zeners or transorbs direct from the amplifier supply pins to ground. The rating of these zeners should be greater than the maximum supply voltage expected, but less than the breakdown voltage of the operation amplifier. Note also that MOS's can be included across the input to the power supply to reduce transients before they reach the power supply. Low pass filtering can be done between the AC main and the power supply to cut down on as much of the high frequency energy as possible. Note that inductors using power supplies will pass all high frequency energy and capacitors used in power supply are usually large electrolytics which have a very high ESR. Because of this high ESR, high frequency energy will not be attenuated fully and therefore will pass on through the capacitor largely unscathed.

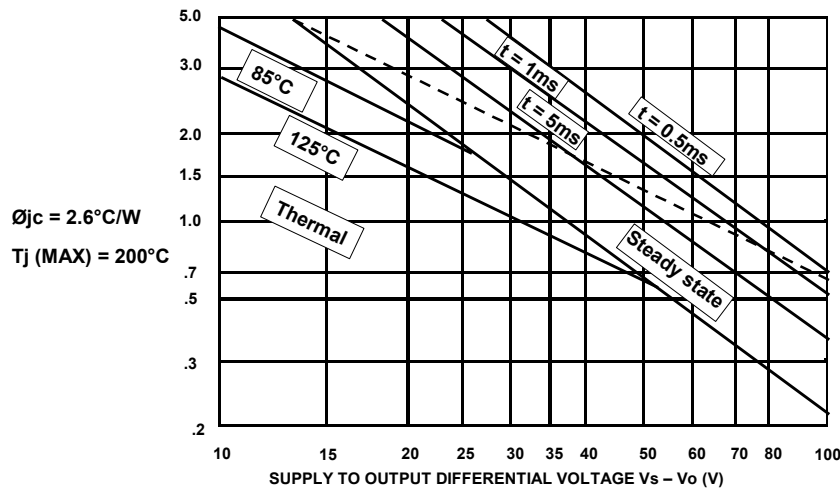
Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

AN25 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS

SAFE OPERATING AREA OUTPUT STAGE DANGER!

- Current Handling Limitations
- Thermal (Power) Limitations
 - Steady State
 - Transient/Pulse Operation
- Second Breakdown
 - Bipolar Devices
 - MOSFETs: Not Applicable

USING THE SOA CURVE



Safe operating area curves show the limitations on the power handling capability of power op amps. There are three basic limitations.

The first limitation is total current handling capability. A horizontal line or the top of the SOA curve and represents the limit imposed by conductor current handling capability die junction area and other current density constraints. The second limitation is total power handling capability or power dissipation capability of the complete amplifier. This includes both of the power die and the package the amplifier is contained in. Note that the product of output current on the vertical axis and $V_s - V_o$ on the horizontal axis is constant over this line.

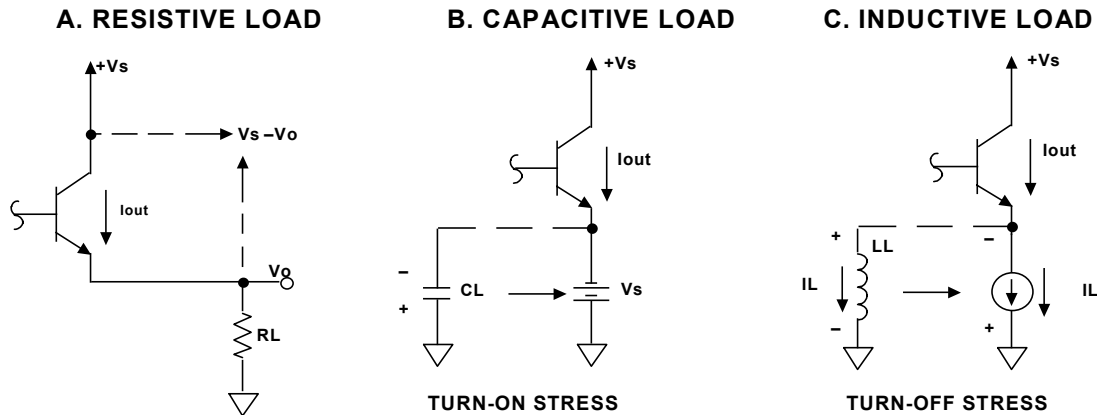
The third portion of the curve is the secondary breakdown areas. This phenomenon is limited to bipolar devices. MOSFET devices do not have this third limitation. Secondary breakdown is a combined voltage and current stress across the device.

Although the constant current boundary and the secondary breakdown boundary remain constant, the constant power/thermal line moves toward the origin as case temperature increases. This new constant power line can be determined from the de-rating curves on the data sheet. The case temperature is primarily a function of the heat sink used.

The dashed line was constructed in this manner for $T_c = 25^{\circ}\text{C}$ for an amplifier advertised as a 67W device (PA07 or PA10). In addition to the fact that very few applications exhibit $T_c = 25^{\circ}$, secondary breakdown prohibits DC operation over its entire length!

Ref. AN1 SAFE OPERATING AREA, AN22

SOA STRESS CONDITIONS



On the SOA graph, the horizontal axis, $V_s - V_o$ does not define a supply voltage or total supply voltage or the output voltage. IT DEFINES THE VOLTAGE STRESS ACROSS THE CONDUCTING DEVICE. Thus $V_s - V_o$ is the difference from the supply to the output across the transistor that is conducting current to the load. The vertical axis is simply the current being delivered to the load.

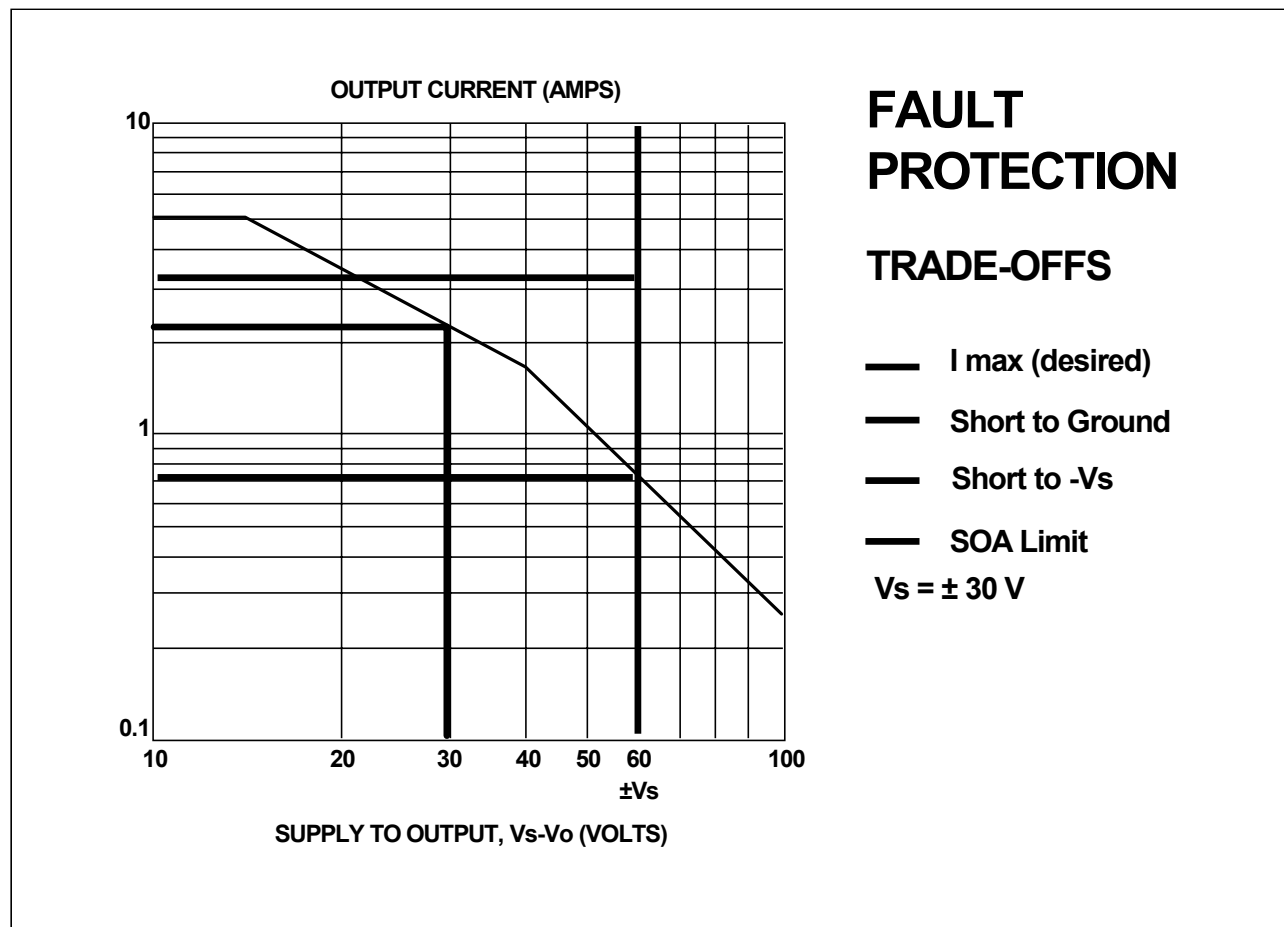
For resistive loads maximum power dissipation in the amplifier occurs when the output is 1/2 the supply voltage. This is because when the output is at 0 volts, no current flows from the amplifier whereas at maximum load current very little voltage is across the conducting transistor since the output voltage is near the supply voltage.

For reactive loads this is not the case. Voltage/current phase differences can result in higher than anticipated powers being dissipated in the amplifier.

An example of an excessive stress condition created by a capacitive load is shown in Figure B. In this case the capacitive load has been charged to $-V_s$. Now the amplifier is given a "go positive" signal. Immediately the amplifier will deliver its maximum rated output current into the capacitor which can be modeled at $t = 0$ as a voltage source. This leads to a stress across the conducting device of $I_{max} \times \text{total supply voltage}(2V_s)$.

Figure C shows a similar condition for an inductive load. For this situation we imagine the output is near the positive supply and current through the conductor has built up to some value I_L . Now the amplifier is given a "go negative" signal which causes the output voltage to swing to down near the negative supply. However the inductor at time $t = 0$ can be modeled as a current source still drawing I_L . This leads to the same situation as before, that is total supply voltage across a device conducting high current.

Ref. AN1 SAFE OPERATING AREA, AN22



Current limit can be used to protect the amplifier against fault conditions. If, for instance, it is desired to protect the amplifier against a short-to-ground fault condition the V_s-V_o number on the horizontal axis is equal to V_s since V_o is zero. Following this value up to the power dissipation limit and then across to the output current gives the value of current limit necessary to protect the amplifier at that case temperature. Note that better heat sinking allows higher values of current limit.

For more aggressive fault protection it may be desired to protect the amplifier against short to either supply. This requires a significant lowering of current limit. For this type of protection, add the magnitudes of the two supplies used, find that value on the V_s-V_o axis, follow up to the SOA limit for the case temperature anticipated, then follow across to find the correct value of current limit.

It is often the case that requirements for fault protection and maximum output current may conflict at times. Under these conditions there are only four options. The first is simply to go the an amplifier with a higher power rating. The second is to trim some of the requirements for fault protection. The third is to reduce the requirement for maximum output current. The fourth option is a special type of current limit called “foldover” or “foldback.” This is available on some amplifiers such as the PA10 and PA12.

Ref. AN1 SAFE OPERATING AREA, AN22

Current Limit Definition

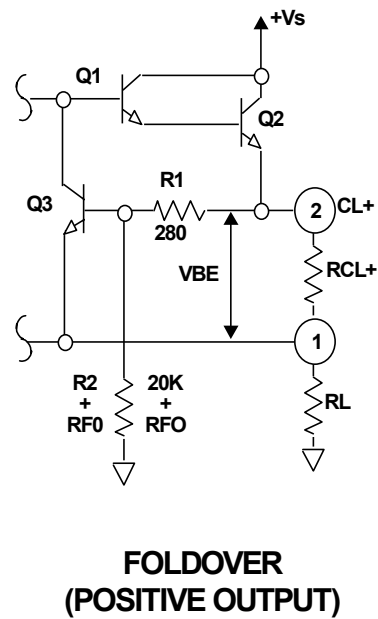
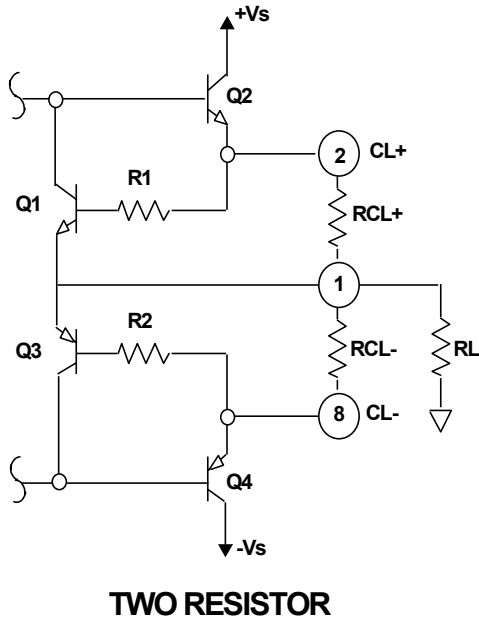
A way to force output voltage where ever needed to maintain constant output current.

- **A non-linear mode of operation**
- **$V_{out} = f(I_{limit} \text{ and } Z_{load})$**
- **I_{limit} is only one term of the power equation**

Current limit circuits do what their name implies but they are not magic cures for all load fault conditions. The non-linear operation (the op amp is unable to satisfy input signal/feedback demands) means monitoring the inputs for the presence of a differential voltage will signal this mode of operation.

Usually the current limit mode will reduce the output voltage but this is not always true. To determine circuit survival the worst case voltage stress across the conducting transistor must be determined.

CURRENT LIMIT TWO RESISTOR AND FOLDOVER

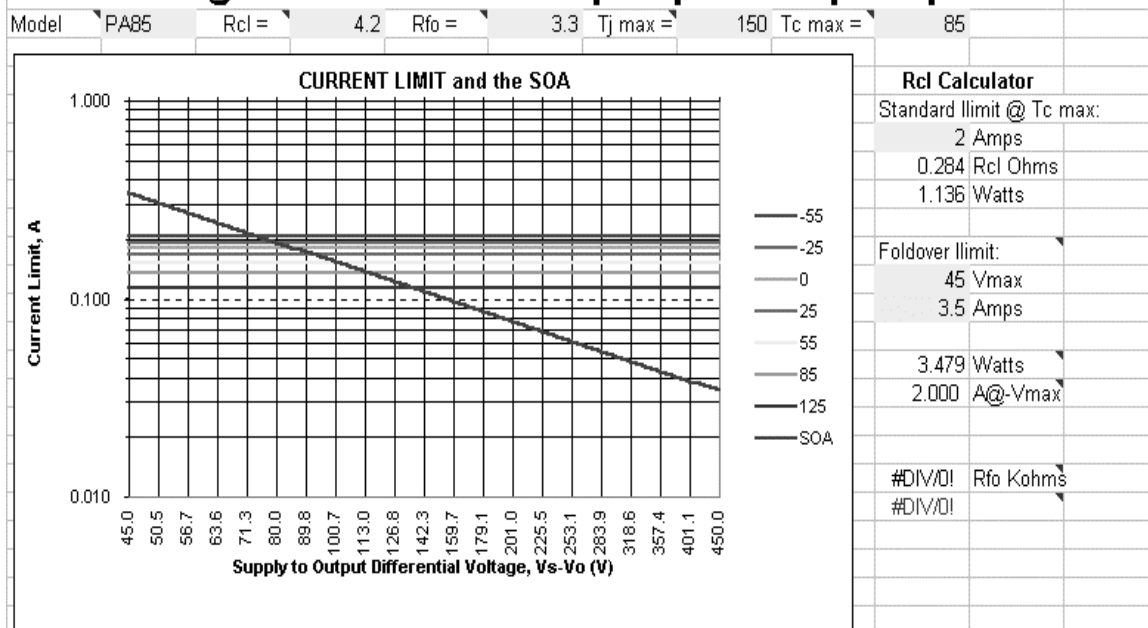


The current limit is the first line of defense against SOA violations. Several different types of current limits are used. The first and most common type of current limit is the two resistor scheme shown above. In this scheme the current limit resistors perform a dual function. The first and primary function is to provide current limit but a secondary function is to provide local degeneration for the emitter followers in the output stage. In this scheme load current flowing from positive supply through Q2 and CL+ to the load will develop a voltage drop across RCL+. When this voltage drop reaches the base emitter turn on voltage of Q1 which is approximately .65 volts Q1 will turn on robbing base current drive through Q2.

The second type of current limit is called foldover or foldback current limit. It's available on the Apex PA04, PA05, PA10 and PA12. The circuit above shows only the positive half of a foldover current limit scheme. This type of current limit scheme works identically to the type just discussed for output voltages near zero. However, for high output voltages the dividing action of R1 and R2 requires that the voltage drop across RCL be slightly higher than before in order to turn on Q3. When energy is stored or produced in the load (reactive loads, motors, short to supply, active load circuits, et al) there will be times Q2 is conducting but output voltage is negative. In this case the divider action lower the current limit.

Ref. AN1 CURRENT LIMIT, AN9

Calculating current limit for Apex power op amps



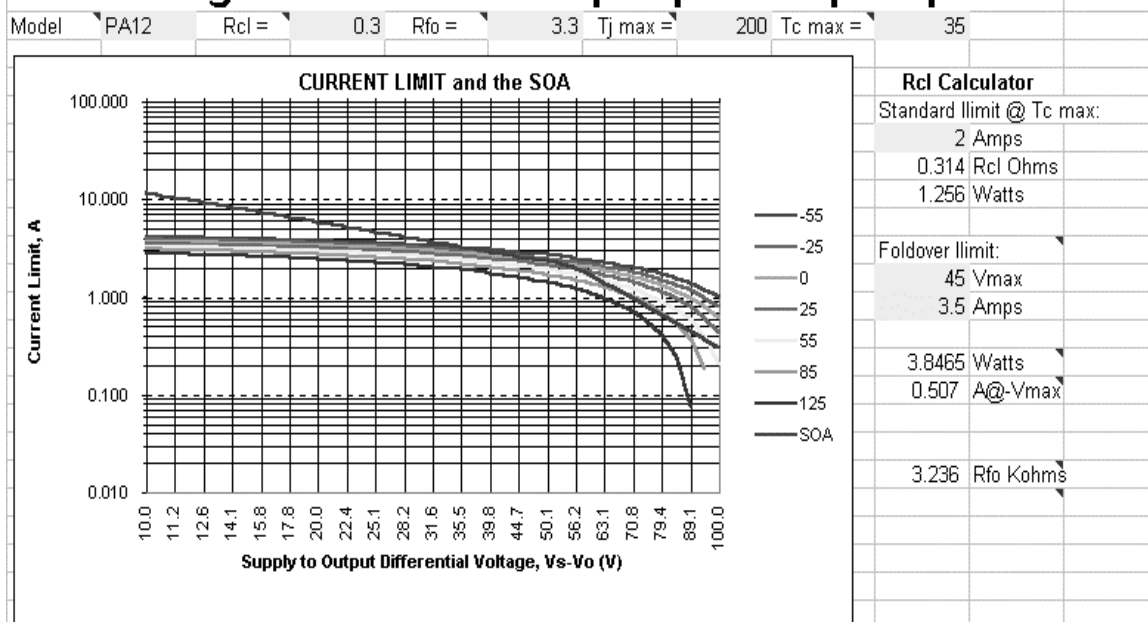
The Ilimit sheet of Power Design.xls really shows the temperature variation. It's a good thing most of us don't have to cover -55° to 125°C. Not all op amps have this slope, but the spreadsheet knows the details of each model. Also enter your limit on junction temperature.

In the upper right, enter your maximum case temperature for the design then drop down and enter the desired current limit at high temperature to see the required resistor. Enter this as Rcl to see the graph. Note that the steady-state SOA curve has been adjusted to your max case and junction temperatures.

When analyzing an existing circuit, simply enter Rcl to see the graph. If the model you are using does not feature foldover current limit, don't worry about Rfo, any entry has no effect.

Ref. AN9

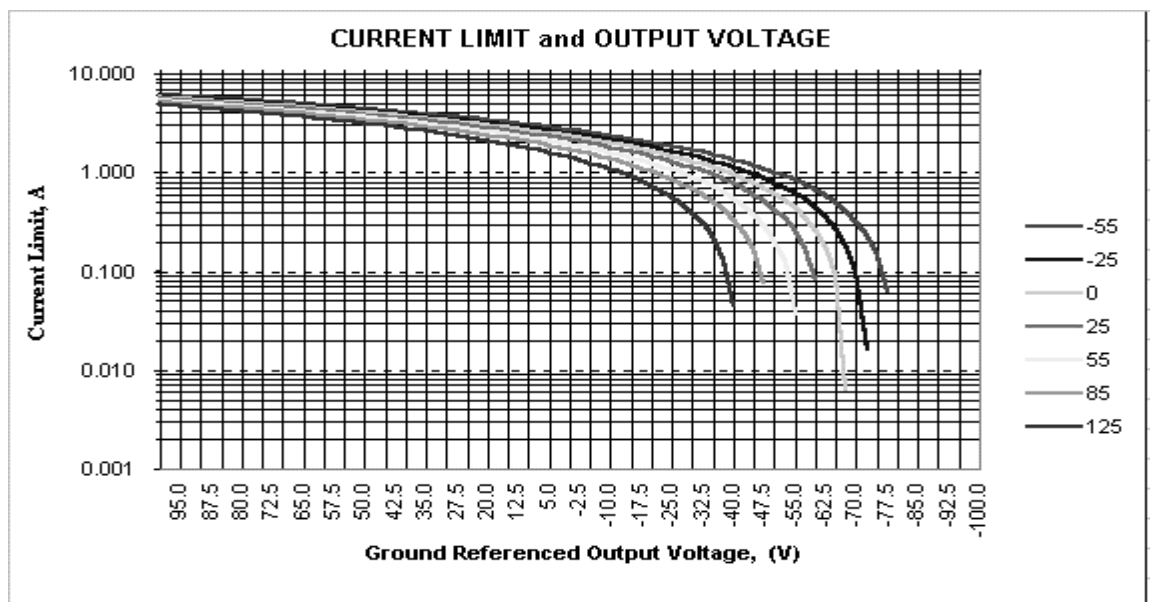
Calculating current limit for Apex power op amps



Models featuring foldover current limit may be used in the fixed limit mode by entering ~100Mohms for Rfo. To use foldover enter the desired current limit at 0V output in the RCL calculator and then the desired current limit and voltage when swinging a signal below. If it is possible to meet this slope requirement, a value will be displayed for Rfo. Enter the two resistor values at the top to see the graph. Note that a new Rcl wattage for foldover operation has been calculated.

This graph assumes dual supplies of maximum rating and charts voltage across the conducting transistor. In this graph, the 50V label corresponds to 0V output; the 10V label to 40V output.

Ref. AN9



Foldover current limit takes a fraction of the dynamic output voltage (relative to ground where the foldover resistor is connected) and combines it with the static V_{be} reference voltage setting current limit. While we often speak of THE current limit, there are actually two, one for the power transistor connected to the positive supply pin and another for the negative side.

The left half of this graph (labeled positive output) shows current limit when the output voltage and the power supply conducting the current are both on the same side of ground. This must be the case when the load is purely resistive and referenced to ground.

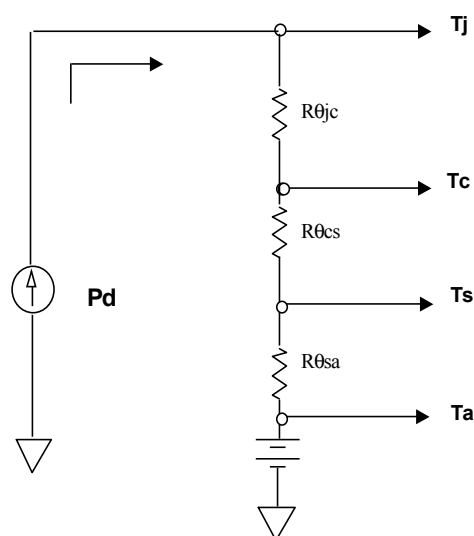
The right half of this graph (labeled negative output) shows current limit when the output voltage and the power supply conducting the current are on opposite sides of ground. This may be the case with reactive or EMF producing loads or if the load is referred to something other than ground.

The dynamic modification of current limit affects BOTH current limits. While one limit is increasing, the other is decreasing. This is a function of output voltage ONLY. If the decreasing side is allowed to reach zero, the amplifier may latch up. This means this graph should be checked for current limit crossing zero anywhere between plus and minus the maximum output voltage of the circuit.

With the graph extending to the full supply voltage spec in each direction, it can be used for any circuit from symmetric supplies to true single supply.

Ref. AN9

THERMO-ELECTRIC MODEL



$$T_j = P_d (R_{\theta jc} + R_{\theta cs} + R_{\theta sa}) + T_a$$

The thermo-electric model translates power terms into their electrical equivalent. In this model, power is modeled as current, temperature is modeled as voltage, and thermal resistance is modeled as electrical resistance.

The real "name of the game" for power amplifiers is to keep T_j as low as possible. As you can see from the model, there are two approaches to doing this. The first is to reduce the current, ie; the power dissipation. The second is to reduce the thermal resistance.

Reducing power dissipation can be accomplished by reducing the supply voltage to no more than what is required to obtain the voltage swing desired. This reduces the $V_s - V_o$ quantity to as low a value as possible.

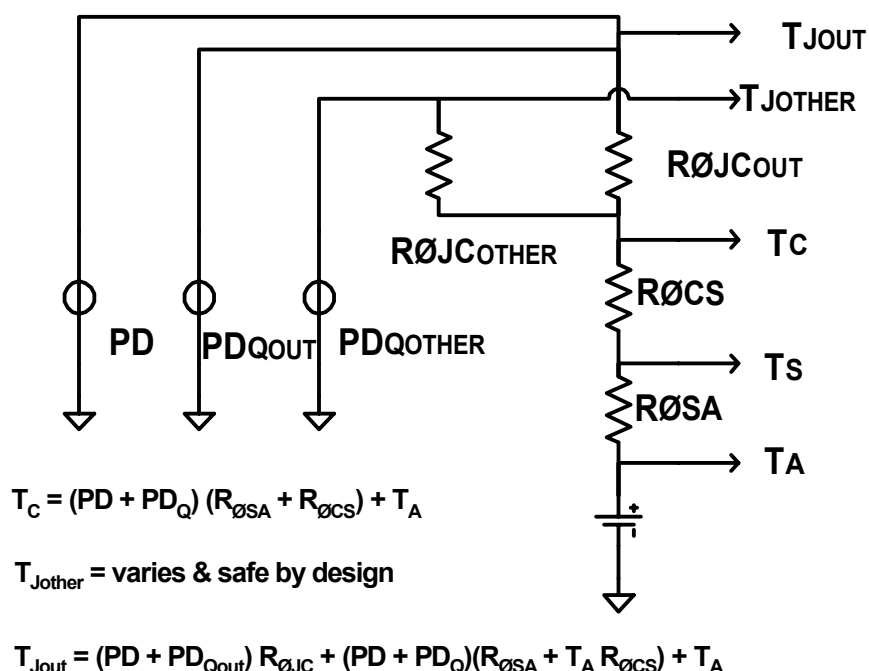
The thermal resistance problem should be attacked on all three fronts. R_{jc} , the thermal path resistance from the semiconductor junction to the case of the amplifier, is characteristic of the amplifier itself. The way to obtain maximum reliability and cool junction temperatures is to buy an amplifier with as low a R_{jc} as affordable.

R_{cs} is the thermal resistance from the case to a heat sink. This resistance is minimized by good mounting techniques such as using thermally conductive grease or an approved thermal washer, properly torqueing the package, and by not using insulation washers.

The last piece of the thermal budget is R_{sa} , the thermal resistance of the heat sink to ambient air. This is a very crucial piece of the puzzle and should not be skimmed on. A quick glance at an SOA curve that shows the difference between the power limitations of an amplifier with a 25° C case and an 85° C case shows the benefit of using the maximum heat sink allowable.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

THERMO-ELECTRIC MODEL



In this model, quiescent power has been split according to the actual transistors generating the heat. PD_{Qout} is only the quiescent current flowing in the output transistors. When appropriate, this specification will appear in the amplifier data sheet. Multiply this output stage quiescent current times the total supply to find worst case PD_{Qout} .

$$PD_{Qout} = I_{Qout} (+V_S + |-V_S|)$$

PD_{Qother} is the current flowing in all the other components and could be found by subtracting PD_{Qout} from PD_Q .

Note that the data sheet junction-to-case thermal resistance speculations refer to only the output transistors. Thermal resistances and power dissipations of other components vary wildly. Design rules applied by Apex for all these components insure they will be reliable when operating within maximum supply voltage, maximum input voltage and maximum "Meets full range specifications" case temperature.

No matter which model you use, there are three thermal resistances contributing directly to hot junctions. The thermal resistance should be attacked on all three fronts:

- 1) Buy an amplifier with the lowest possible $R_{\theta JC}$.
- 2) Use good mounting practices.
- 3) Use the largest practical heatsink.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

HEATSINK SELECTION

GIVEN: PA02 POWER OP AMP

$$P_d = 14 \text{ Watts}$$

$$T_a = 35^\circ \text{ C}$$

$$R_{jc} = 2.6^\circ \text{ C/W}$$

$$R_{cs} = .2^\circ \text{ C/W}$$

FIND: APEX HEATSINK TO KEEP $T_j = 100^\circ \text{ C}$

$$T_j = P_d (R_{jc} + R_{cs} + R_{sa}) + T_a$$

$$100^\circ \text{ C} = 14\text{W}(2.6^\circ \text{ C/W} + .2^\circ \text{ C/W} + R_{sa}) + 35^\circ \text{ C}$$

$$R_{sa} = 1.8^\circ \text{ C/W}$$

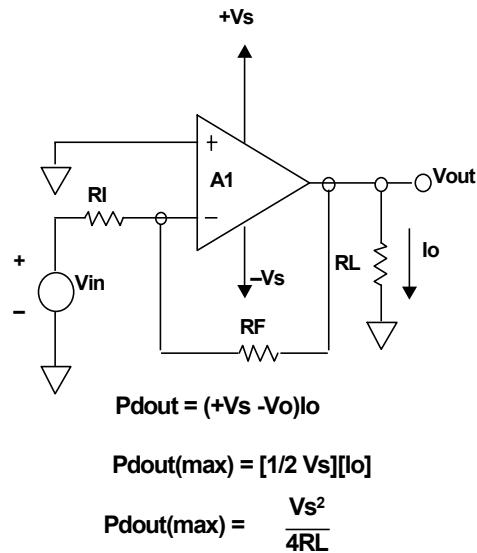
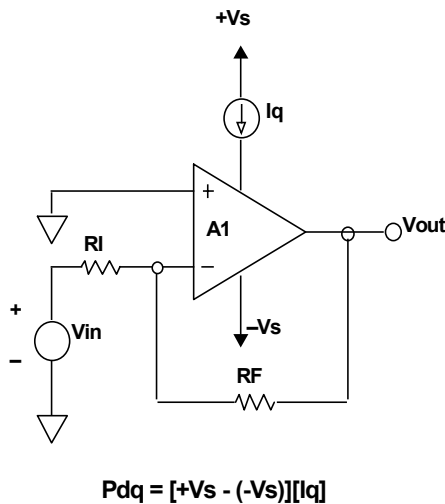
SELECT APEX HS03: $R_{sa} = 1.7^\circ \text{ C/W}$

This calculation illustrates the heat sink selection procedure using the thermal electric model discussed. First we calculate the power dissipation within the amplifier under worst case conditions. In this example, that number came out to 14 watts. Next we pick a desired value of T_j . In this example, we picked a very conservative value of 100° C . This value of T_j will result in a very large mean time to failure, spelling reliability for this application. Consulting the data sheet for the PA02, we find that the maximum DC thermal resistance from junction to case is $2.6^\circ \text{ C per watt}$. Next, we consult the APEX Data Book to determine that the typical case to heatsink resistance is between $.1$ and $.2^\circ \text{ C per watt}$, when thermal grease is used. Solving the given formula for the unknown, R_{sa} , we find that the required thermal resistance is less than or equal to $1.8^\circ \text{ C per watt}$. This can easily be achieved by using the Apex HSO3 Heatsink which has an RSA of $1.7^\circ \text{ C per watt}$.

If a system has forced air or a liquid cooling system available, physical size of the heatsink can be decreased. Heatsink data sheets often graph thermal resistance vs. air velocity. Fan data sheets usually speak of volume moved. At the very least a conversion is needed which takes in account the square area of the air path as it passes the heatsink.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

POWER OP AMP “DC POWER DISSIPATION”



$$P_{dtotal} = P_{dq} + P_{dout}$$

When calculating power dissipation in an amplifier, you MUST NOT FORGET THAT POWER DISSIPATION IN THE AMPLIFIER IS NOT EQUAL TO POWER DISSIPATION IN THE LOAD. That is, most of the time. One exception is when the output voltage is half of the supply voltage and the load is resistive. In this particular case the power dissipations are equal.

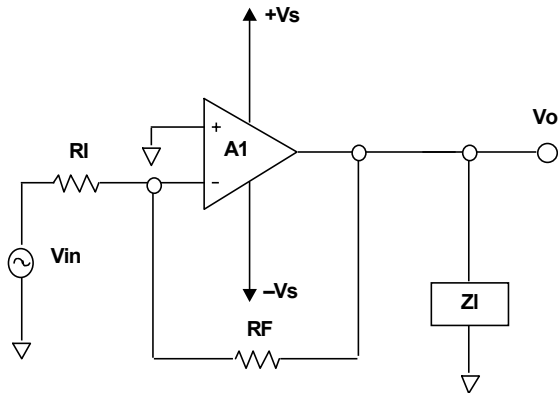
Calculating power dissipation in an amplifier under DC conditions with a resistive load is very simple.

The first portion of power dissipation is due to the quiescent power that the amplifier dissipates simply by sitting there with +Vs and -Vs applied. Multiplying total supply voltage by quiescent current gives the value of this power dissipation.

The maximum power dissipation in the amplifier under DC conditions with a resistive load is when the output voltage is 1/2 of the supply voltage. Therefore, whatever current is delivered to the load at 1/2 supply voltage multiplied by 1/2 supply voltage gives maximum power dissipation in the amplifier. The total dissipation is the sum of these two.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

POWER OP AMP “AC POWER DISSIPATION”



$$Z_L = |Z_L|$$

$$P_{dout(max)} = \frac{2V_s^2}{\pi^2 Z_L \cos \theta}, \theta < 40^\circ$$

$$P_{dout(max)} = \frac{V_s^2}{2Z_L} \left[\frac{4}{\pi} - \cos \theta \right], \theta > 40^\circ$$

$$P_{total} = P_{dout(max)} + P_{dq}$$

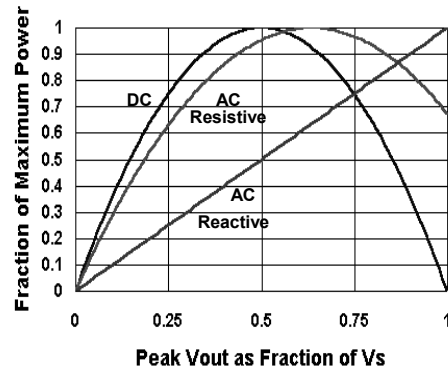
With an AC output and/or reactive loads, output power dissipation calculations can get a bit stickier. Several simplifying assumptions keep the problem reasonable for analysis. The actual internal dissipation can be determined analytically or through thermal or electrical bench measurements. Both Application Note 22 and Application Note 1 General Operating Considerations give details on measuring AC power dissipation.

Worst case AC power dissipation formulae are given above for any reactive load range. With these worst case formulae one can calculate worst case power dissipation in the output stage for AC drive conditions and reactive loads. For most power op amps output stage power dissipation is the dominant component of total power dissipation so adding worst case AC output power dissipation with DC quiescent power dissipation and using AC $R_{\theta jc}$ thermal impedance for junction to case, will be sufficient for heatsink calculations.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

More is not Always More

- DC W.C.=50% of V_s
- R AC W.C.=63.7% of V_s
- Z AC W.C.>63.7% of V_s



Cranking the volume or the output up to maximum is not necessarily the worst case internal power dissipation for a linear output stage. We saw earlier that under DC and resistive load conditions, 50% of supply voltage was worst case.

As we progress to AC signals but the load remains resistive, worst case is when peak output is 63% of supply voltage. As we start adding reactive elements to the load the 63% figure starts increasing.

Is this chart saying reactive loads are the least demanding on the linear output stage?

No Way!

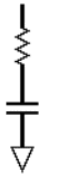


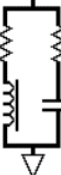
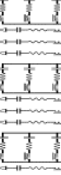
There are hidden scale changes in this chart. Assume the power scale is in actual watts and supply voltage is 1V. A resistor of 0.25Ω will generate the DC curve and maximum output power is 4W. Note that the heatsink calculation will use DC thermal resistance which is larger than AC thermal resistance. A resistor of 0.2027Ω will generate the AC resistive curve with a maximum output power of $\approx 2.47W$. A reactance of 0.637Ω will generate the AC reactive curve with a maximum output VA of only 0.785W.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

Power Dissipation-the Easy Way

Power Design.xls

Calculating Power Dissipation for Apex power op amps							
Model	PA12A	Ta max =	25	Tj max=	150	Tc max=	125
Power for Sine Wave Outputs		Note/PA46					
Vs	50 Volts	Note/PA21,5,6					
Fmin	0.005 KHz	Note/PA04,05					
Fmax	0.9 KHz	Bridge ckt?					
Sig	45 Units	No					
Sig as ?	V peak	Note/W					
Res	12.5 Ohms	# of Amps in parallel?					
Cap	1E+11 uF	1					
Ind	689 mH						
Rcap	0 Ohms	Unipolar or Bipolar?					
Rind	0 Ohms	Bipolar					
Piq	2.5 Watts						
Read Me							
Resonant Frequency =	6.06E-07 KHz						
At Fmax:		At Fmin:					
Xc hi =	1.77E-09	Xc =	3.18E-07				
Xl hi =	3896.203	Xl =	21.64557				
Notes:		Power Trial					

32Results

33Results

34Results

35Results

37Define

36Results

Sweep the Frequency

85 View Last Frequency Sweep

If your application can be modeled as a sine wave of any frequency, this sheet will tell you a lot. Entering a model pulls up a sizable portion of the data sheet for calculation and flag raising. Enter the three temperatures: ambient from the application, case per data sheet max or lower, and junction per contract or philosophy on reliability. If you need DC response, anything below 60Hz is OK. Define your output signal in terms of volts, amps or watts. If your load can be modeled by one of the first four diagrams, enter the values below. If you need diagram 5, use the Define Load command button.

Be sure to check these three cells!

If the Bridge circuit cell is "Yes", the signal and load values specified will be treated as total but internal power will be for a single op amp.

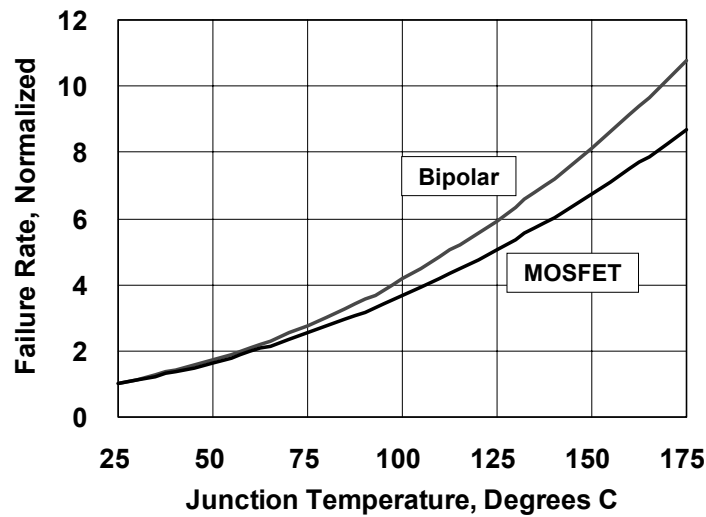
Internal power will be divided by the # of parallel amplifiers.

"Unipolar" forces only one power supply and the use of DC thermal resistance.

A few useful pieces of information show up on this screen along with a red flag if your specified supply voltage is out of bounds. For more answers use the command button below the desired load diagram.

Ref. AN37

What is Tjmax?



While this author would be the first to agree MIL-HDBK-217 has a few quirks and is very often misused, it does have the curves sloping in the right direction. Electronics is similar to your car, toaster- -almost anything: Run it too hot and it dies an early death. Apex suggests a maximum of 150°C for normal commercial applications. If the equipment is remotely located or down time is extremely expensive a lower temperature is appropriate.

This graph represents the temperature acceleration factors from revision F, Notice 2.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

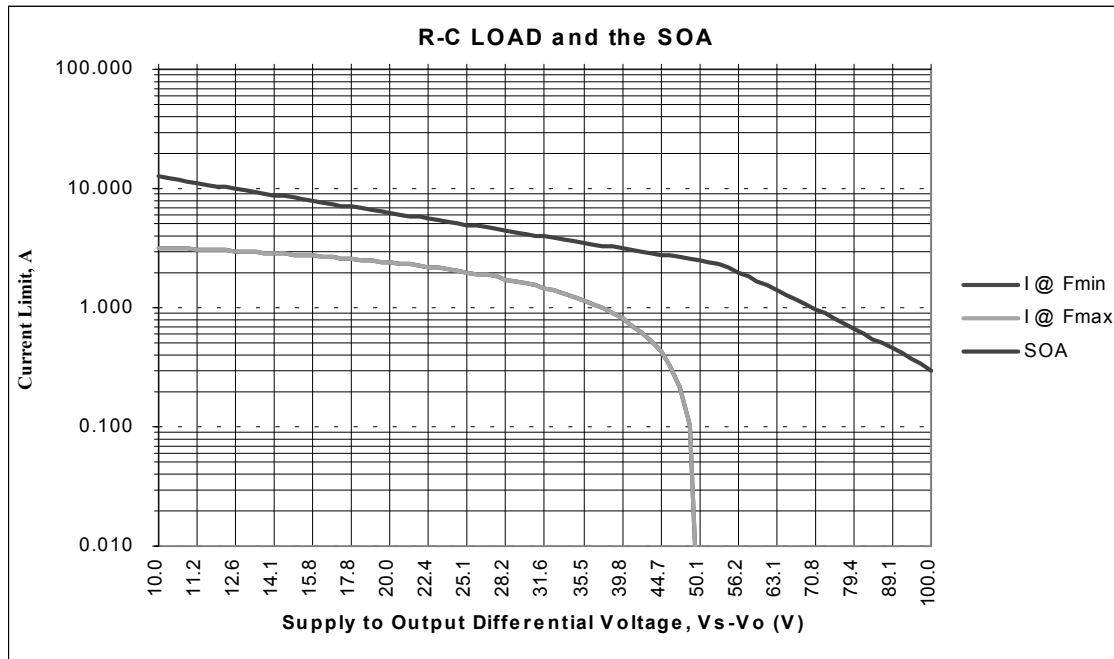
	At Fmin:	At Fmax:			At Fmin:	At Fmax:		
Z in Ohms	15915.50	21.87			Maximum AC Pint			
Phase angle	-89.95	-46.70			39.6	37.8	Vpk	
RMS Amperes	0.0012218	0.8891318			28.001429	26.728636	Vrms	
Peak Amperes	0.0017279	1.2574223			0.0017594	1.2221521	Arms	
RMS Volts	19.445436	19.445436			0.0492652	32.66646	Wrms	
Peak Volts	27.5	27.5			4.643E-05	22.404837	Wtrue	
RMS Power	0.0237583	17.289557			0.0633588	44.012142	Pin	
Peak Power	0.0475166	34.579113						
Power factor	0.001	0.686			Minimum HS:		2.61	°C/W
Input power	0.04	32.02						
True power	0.00	11.86			Actual HS:		10	°C/W
Percent Efficiency =	1.16	50.82			Results in Tjmax =		268.77	°C
Vpk capability =	35.00	34.87			Results in Tcmax =		248.82695	°C
Op amp internal dissipation:								
Input power	0.04	32.02			TOO *@&!# HOT!!!!			
Dissipation RMS	0.04	20.16						
Dissipation Peak	0.08	37.14						
Total in heatsink	2.08	22.16						
WC watts & Rth	22.161084	0.9			2.6074487	4.6405182	2.6074487	

If you're in a hurry, go to the right side just above the yellow box to find the smallest heatsink usable. Enter data sheet rating for selected heatsink to see maximum case and junction temperatures.

Since the low frequency load is so light we'll look at the high frequency numbers only. Below impedance & angle are the operating points of the load; amps, volts, watts and power factor. Next we find power being drawn from the supplies due to driving the load and true power dissipated by the load. This leads to efficiency (at your specified signal level). If the peak output capability based on the supply and output current is more than a few volts above required output, lowering supplies will reduce internal dissipation.

In the upper right, the worst case amplitude for your load is estimated (this amplitude varies with phase angle). Op amp RMS dissipation is calculated by subtracting true power from input power at worst case amplitude or your maximum level. Peak op amp dissipation is taken from the graph below. "Total in heatsink" uses peak if the frequency is below 60Hz (else RMS), then adds quiescent power. The last line picks worst case frequency and gives you power and thermal resistance for heatsink sizing. The three cells in the lower right are heatsink needed to keep the case cool, to keep the junctions cool without regard to the case, and the smaller of the two.

Ref. AN37



Remember transistor load lines from school? This is it and there should be no major surprises. At least none that we can't explain or fix.

The lack of an F_{min} curve in this example is because our load is completely off scale with peak current of only 1.7mA.

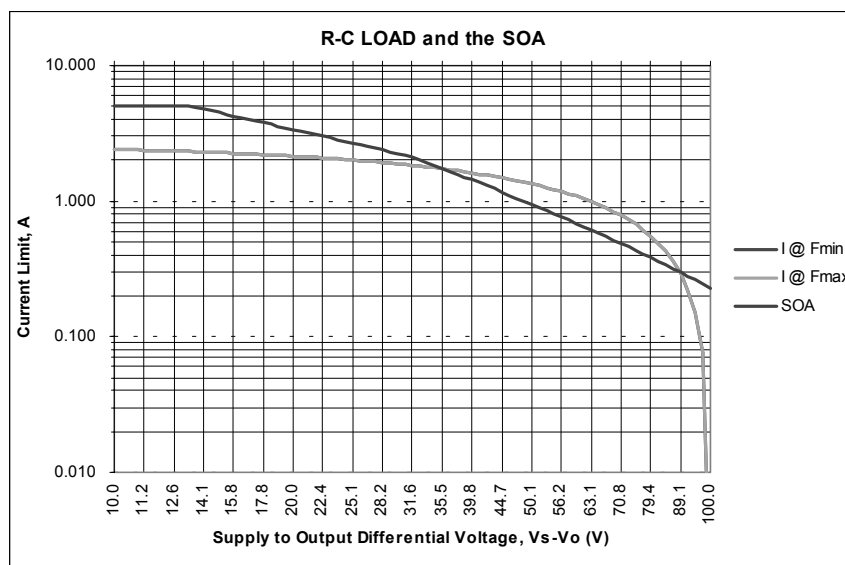
If one of the load lines peaks over the SOA curve remember we are looking at $\frac{1}{2}$ of a sine wave while the heatsink may have been sized on RMS values. If it looks like you have a lot of wasted power handling capability, go back and enter maximum case and junction temperatures calculated for the actual heatsink to be used.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING, AN22

Resistive Load Line Calculations

PA07
100Vs
37.3Ω
1.34A @ 50V
67W max

But.....



So, you've checked the maximum power dissipation at $\frac{1}{2}$ the single supply voltage and all is well (discounting the fact this example requires an infinite heatsink). The job is not over! At frequencies below 60Hz you do not to cross the second breakdown curve at all. At higher frequencies, keeping the duty cycle of these excursions down to 5% will keep you out of trouble.

When using dual symmetric supplies and pure resistive loads, all Apex power op amps are immune to this problem. For all other cases use Power Design.xls to plot sine wave load lines for you. This graph is from the power sheet but a trick had to be pulled to get a plot where output voltage is over 50% of the total supply voltage. In the Vs cell enter 100 volts and use the *Unipolar or Bipolar* input cell to specify Unipolar output current. This causes Power Design to calculate quiescent current on a single 100V supply and to use DC thermal resistance because only one transistor is doing all the work.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING, AN22

Typical Load Line Calculation

PA12

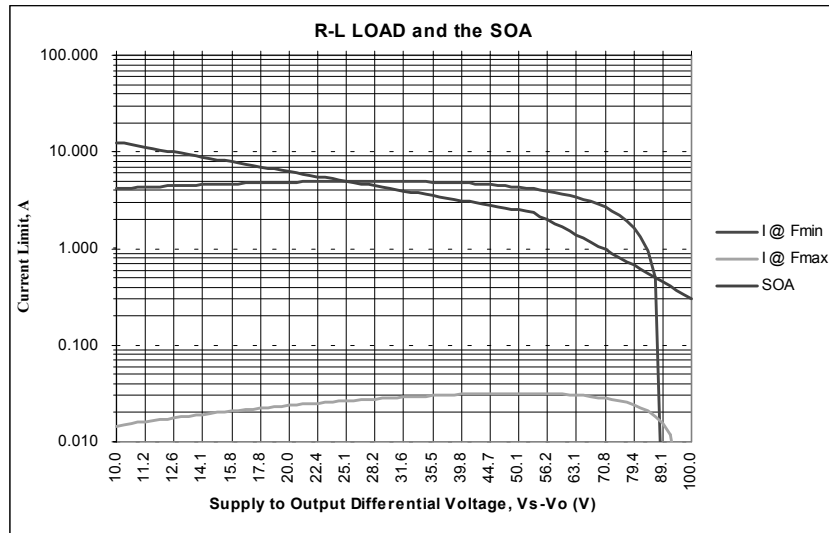
$\pm 50V_s$

45Vpk@ 5A

$9\Omega @ 60^\circ$

112VA \rightarrow Load

But.....



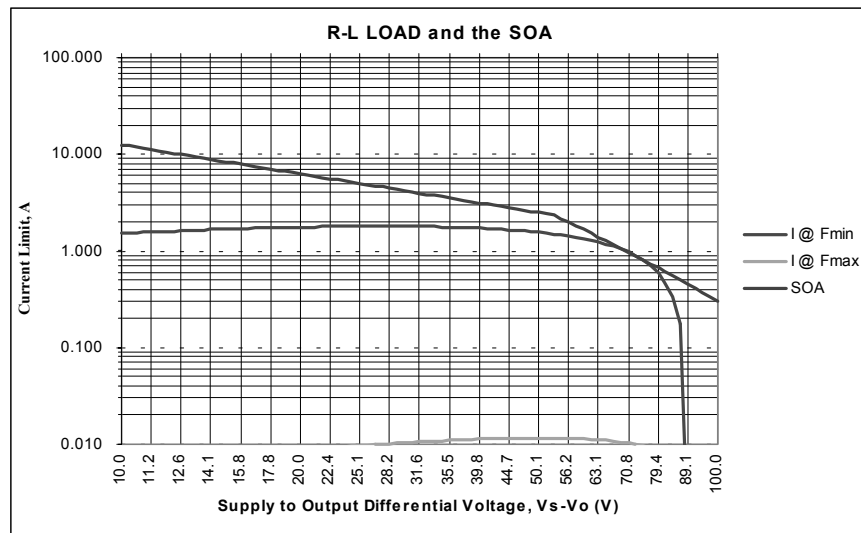
Can a 125W, 10A device drive this 5A load? It's a large coil (250mH and 4.5Ω) and the frequency is only 5Hz. If efficiency were only 50%, delivering this 112VA to the load should be OK, shouldn't it? No. And no.

Phase shift is the killer here. You can see right away the load line exceeds the second breakdown curve. Look at current at the 56.2V stress level; its almost 4A (3.93 actually) giving peak dissipation of about 220W. Indeed, the data above this graph says the number is 223.5W (including I_q). We are in big trouble even though a 9Ω pure resistive load would have been fine with dissipation of only 72W and no hint of second breakdown problems.

It is time to look for a bigger amplifier or negotiate the load specifications.

Typical Load Line Calculation

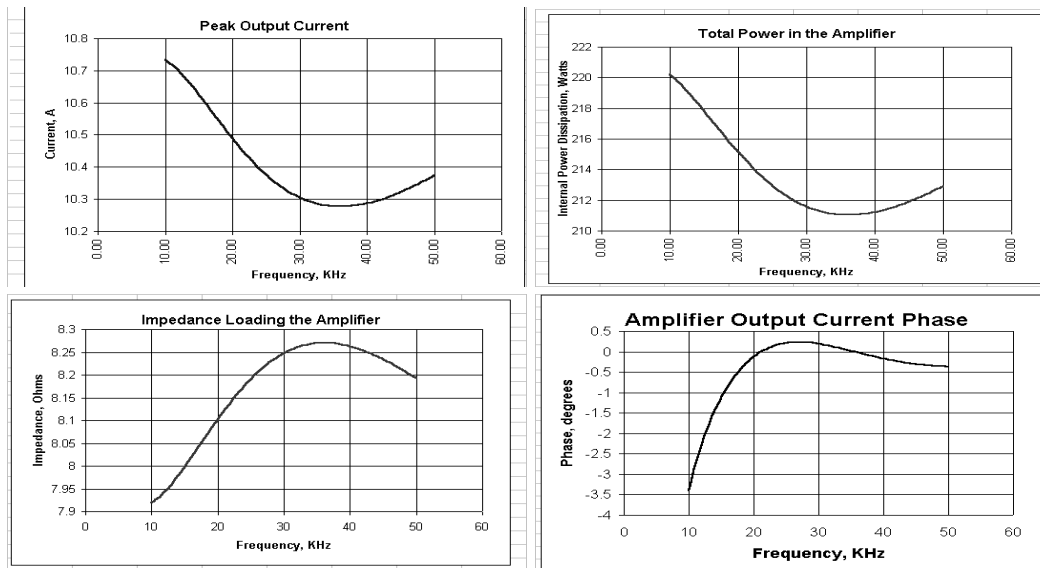
PA12
±50Vs
45Vpk@ 1.8A
25Ω @ 60°
40VA→Load



Reducing the load requirements all the way to 25Ω produces a load line not in violation of the second breakdown curve and power dissipation in the amplifier is down to a manageable 82W.

The probability of negotiating load specs this far is rather dim. Its time to look at a bigger amplifier such as the PA05.

Multiple Reactive Elements



Any time an application has more than one reactive element, peak values of voltage, current, phase shift and power dissipation may not be at the minimum or maximum frequencies. It would be a good idea to run a frequency sweep to locate worst case operating points.

These graphs model operation of a tuned piezo load and the transmission line. In this case we find worst case power dissipation in the amplifier is at minimum frequency. Don't get caught by surprise with a complex load producing a power peak instead of a dip.

Frequency sweep requires Analysis ToolPak. If you see cells with #NAME? or a runtime error, try TOOLS, ADD-INS, Analysis ToolPak and then sweep.

Ref. AN37

Thermal Capacity can be a Big Friend

- For pulse mode operation
- When pulses > 8ms
- Ap Note 11 Thermal Techniques
- Thermal response \cong to R-C response

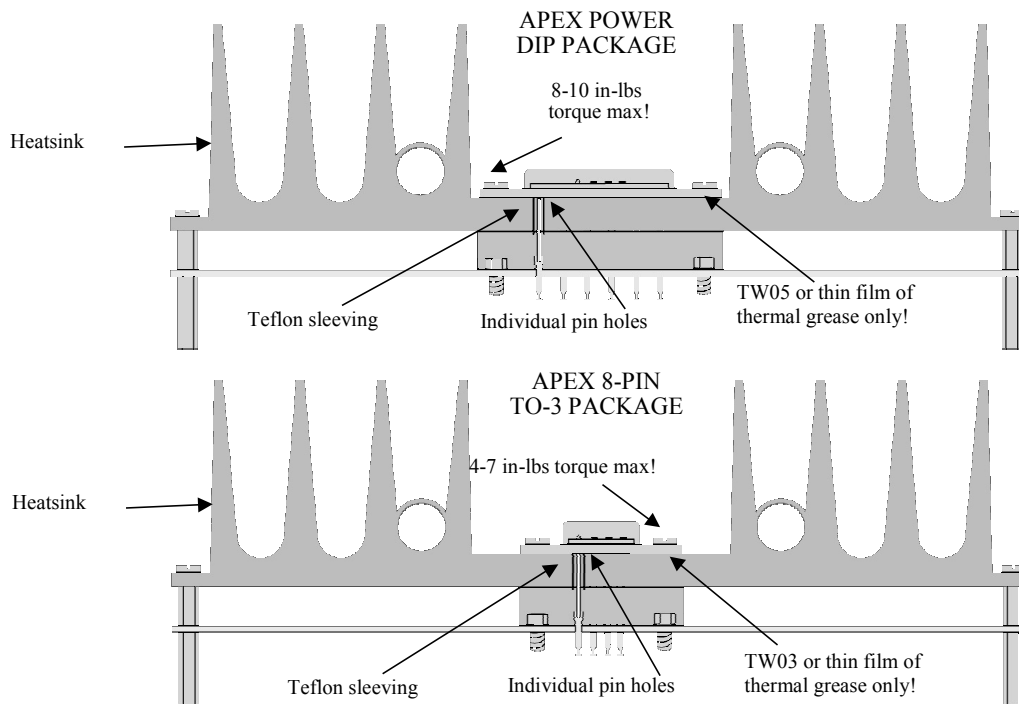
$$\Delta V = V_s * (1 - e^{-t / RC})$$

$$\Delta \text{temp} = W * \theta_{hs} * (1 - e^{-t / \text{TAU}})$$

If the drive signal is pulse mode, internal power between pulses is zero and individual pulses are less than 8ms, size the heatsink by dividing the pulse power by the duty cycle and adding the quiescent power.

For other pulse mode operations Application Note 11, Thermal Techniques, is the reference. It will explain how to calculate thermal capacity, thermal time constants and plot the charge/discharge curve. It also lists some common unit conversions and constants.

MOUNTING CONSIDERATIONS



Key areas to check for proper mounting techniques:

- 1) Heatsink flatness.
- 2) Individual heatsink thru-holes for each pin.
- 3) Thermal interface between case and heatsink.
- 4) Mounting torque.
- 5) Sleeving on pins—thickness of heatsink.

A detailed discussion of these areas follows.

Ref. AN1 AMPLIFIER MOUNTING AND MECHANICAL CONSIDERATIONS

MOUNTING CONSIDERATIONS

Heatsink surface smoothness is important to avoiding substrate cracking. While flatness in terms of total indicator runout (TIR) of 4 MIL/in. is adequate, and 1 MIL/in. preferred, any indentations, bumps or ridges, that protrude more than 0.5 mil can be a problem.

Once a proper heatsink selection is made it is essential to properly mount the amplifier. First, if you are drilling your own heatsink, drill individual holes for each pin and deburr. Since the power die are located inside the pin area, and this primary heat path is the shortest one, there must be plenty of heatsink mass in the center of the pin area. Drilling or cutting a single hole large enough for all the pins to go through can result in amplifier destruction.

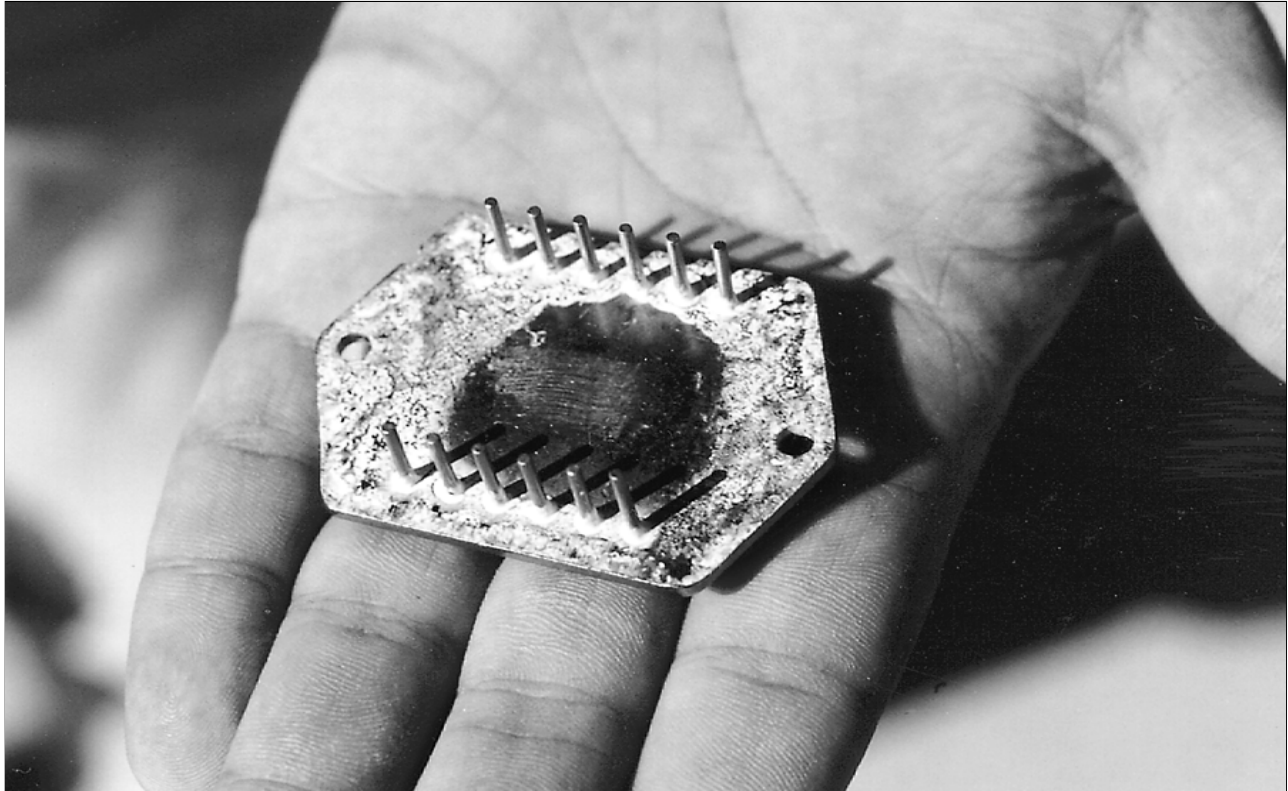
Next, the amplifier must have some media between it and the heatsink to insure maximum heat transfer. Thermally conductive grease is the oldest method to improve heat transfer, and continues to be among the best methods to reliably mount APEX power amplifiers and provide heat transfer along with avoiding problems with cracking the internal ceramic substrate.

Many customers prefer to avoid grease however. Thermally conductive washers must be approached with caution when used with APEX amplifiers. They must simultaneously provide the following attributes: 1. Good thermal conductivity. 2. Non-compressible. 3. As thin as possible and never over 5 mils thick. Power Devices Thermstrates easily meet these requirements and are available in the 8 pin TO-3 configuration. Power Devices Isostrates are thermally conductive washers suitable for those rare applications where electrical isolation is required (keep in mind that most APEX amplifiers have electrically isolated cases). APEX stocks and sells an assortment of these thermal washers for TO-3, Power DIP and Power SIP packages. Use of any other make/model of thermal washers voids any amplifier warranty.

Although not especially an issue during engineering bench testing, when mounting significant quantities of amplifiers in a production environment, use of a torque wrench is important. Proper torque ensures proper thermal conductivity without running the risk of cracking substrates..

Proper torque is defined as 4-7 in-lb for 8-pin TO-3 and Power SIP packages, and 8-10 in-lb for Power DIP packages. For packages with two mounting holes, this torque should be applied in 2 in-lb increments alternating between the two mounting bolts similar to when tightening lug nuts on a car tire.

Unless you can guarantee by mechanical design that shorts between pins and heatsinks are impossible, then it is wise to sleeve at least two amplifier pins. This will insure adequate alignment to prevent any possible shorting. Use 18 ga. tubing on TO-3 and 16 ga. tubing on power dip packages. Teflon covers all needs but other materials may work if they meet the mechanical, thermal and electrical breakdown requirements.



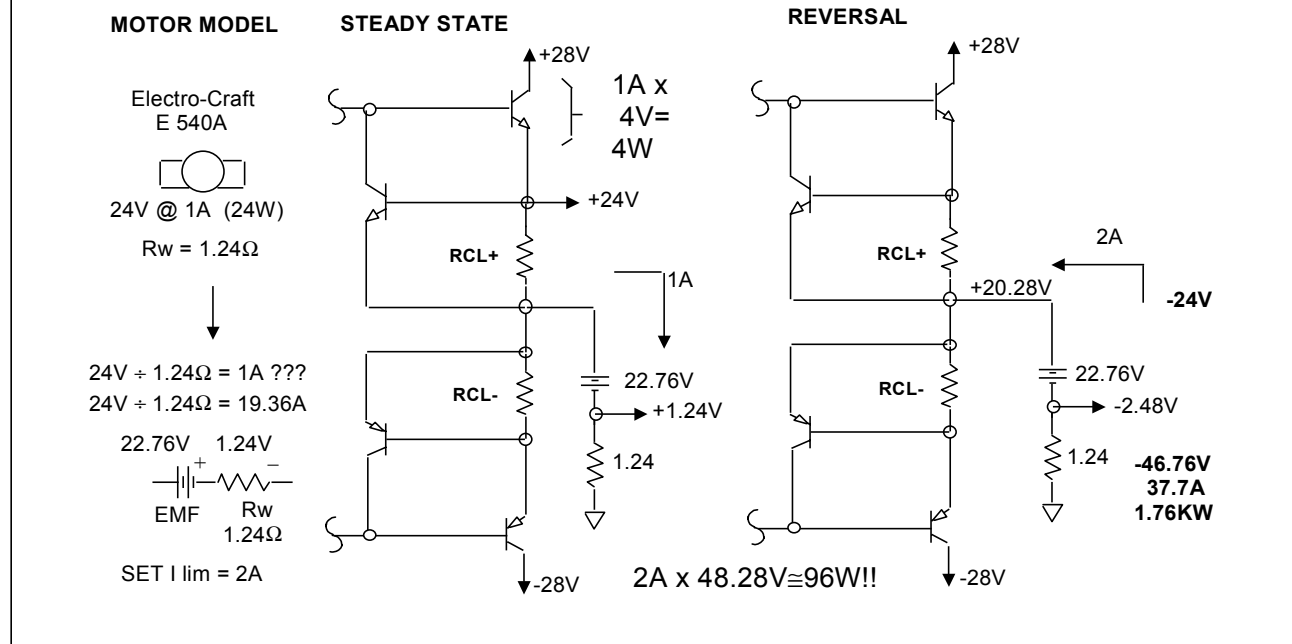
Properly applied grease results in good thermal performance. The operator variable shown above leaves the central area (where the heat is developed) with a high thermal path which led to amplifier destruction. Another variable to watch for is separation of the liquid from the solids in the grease. Too high a percentage of either can result in amplifier destruction due to thermal or mechanical stress. Buying thermal grease in a can or jar rather than a tube allows stirring to avoid the separation problem.

This slide also introduces the Apex failure analysis service. If you have a an elusive problem, call us. We'll attempt to solve it over the phone. Its always good to have a schematic handy you can fax. If appropriate, we'll give you an RMA (return material authorization) to start a failure analysis. We will:

1. Perform an external visual examination.
2. Test the part to all room temperature electrical specifications.
3. Delid and perform an internal visual.
4. Trouble shoot the circuit.

Many times the physical evidence helps pinpoint the problem. The location and nature of damage usually yields a suggestion on how to eliminate the problem.

MOTOR REVERSAL IS THE MOST DEMANDING LOAD CONDITION



A DC motor driven at 24V with 1A steady state current flow and a winding resistance specified at 1.24Ω can be modeled as a resistor in series with an EMF. In this example since the 1A drops 1.24V across the 1.24Ω , the remaining 22.76V is back EMF.

Under steady state conditions the motor voltage of 24V subtracted from the supply voltage of 28V leaves a 4V drop across the conducting transistor and a power dissipation of 4W.

When the amplifier is told to reverse the motor, the output of the amplifier attempts to go to -24V. If it could do so this -24V would add to the EMF of 22.76V to give -46.76V across the 1.24Ω resistor, resulting in a current flow of 37.71A. No way! Current limit is set at 2A.

When the current limit value of 2A flows across the winding resistance it drops 2.48V. The positive 22.76V of EMF is added to this negative 2.48V to give an output voltage of 20.28V. The difference between the output and the negative supply is now $28 - (-20.28)$ or 48.28V. That stress voltage on the conducting transistor means that the internal dissipation in the amplifier immediately after reversal is 48.28 volts * 2 amps or 96.56 watts!

This shows that a simple reversal can increase instantaneous power dissipation in the amplifier by over an order of magnitude. Judicious setting of current limiting and slowing the electrical response time will optimize reliability and mechanical response time.

Ref. AN24

Single Supply Operation

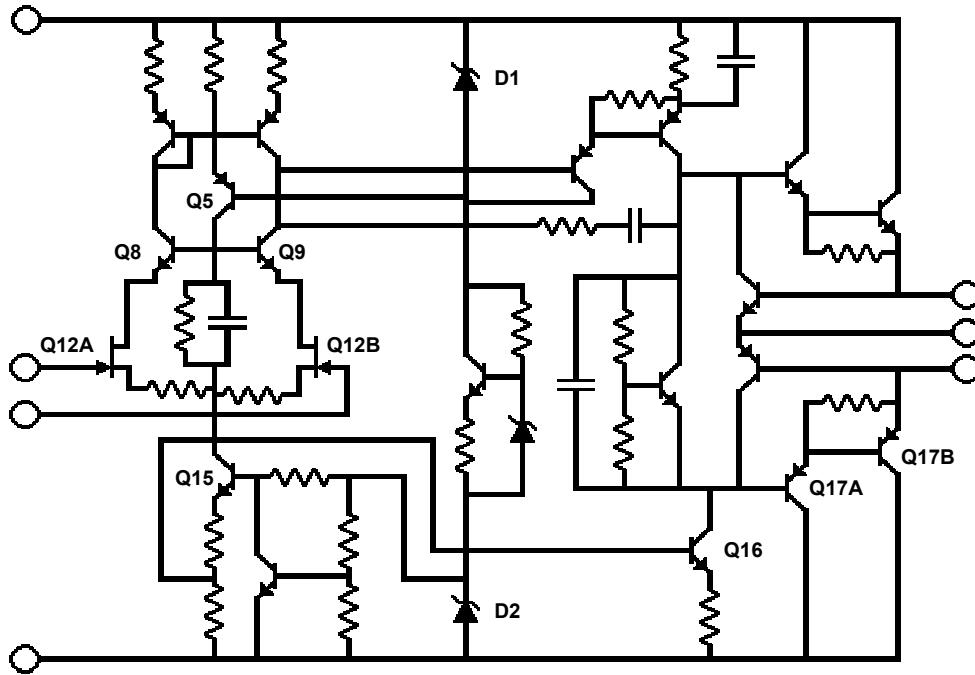
Advantages

Limitations

Special Considerations

The basic operational amplifier has no ground pin. It assumes ground is the mid-point of the voltages applied to the +Vs and -Vs pins. If voltages on the input pins deviate from the assumed ground, it labels this deviation as common mode voltage. If this common mode voltage is within the op amp's range and we don't ask the output to go out of range, the op amp is happy.

Head Room Required



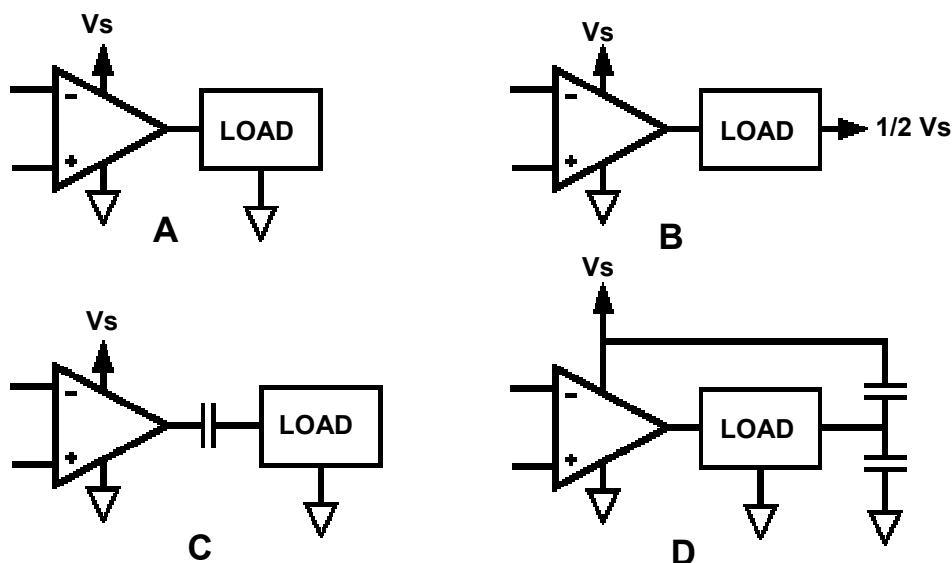
Notice that as the input pins approach the negative rail, the voltage across Q15 decreases. Minimum operating voltages for Q12 and Q15 along with the zener voltage place a limit on how close common mode voltage can get to the negative rail.

With inputs going positive Q5, Q8, Q9 and D1 place a similar limit on how close common mode voltage can get to the positive rail.

On the output side look at a fraction of the D2 zener voltage plus Q16 operating requirements and the V_{be} of Q17 as all contributing to a limit of how close the output can approach the negative rail. This is the output voltage swing spec of the op amp. While this spec moves with output current, it never gets to zero even if current does. This means getting to zero output on a true single supply power op amp circuit is NOT going to happen.

While the actual voltages vary a lot, these type limitations are typical of all linear power amplifier output stages and most input stages. The Apex PA21, PA25 and PA26 family is an exception on the input side; common mode input goes below the negative supply rail making them ideal for some moderate power single supply applications.

Basic Single Supply Circuits



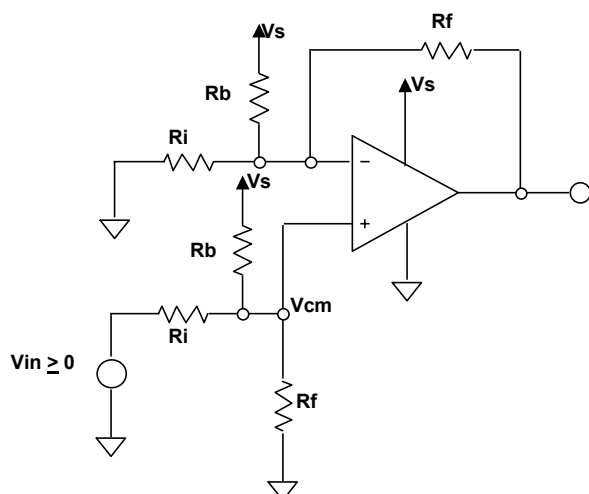
Circuit A is only suitable for unipolar and non-zero inclusive drives. These type applications might include Programmable Power Supply (PPS), heater controls and unidirectional speed controls.

Circuit B is practical only when the power supply has a mid-point capable of bi-directional current flow such as a stack of batteries. Even this can be a problem due to battery impedance being in series with the load.

Circuit C is reasonably common in the audio world. Circuit D is sometimes used to reduce turn-on pops but must be matched to input signal circuits to be of much use.

Ref. AN21

SINGLE SUPPLY NON-INVERTING CONFIGURATION



$$V_o = \frac{R_f}{R_i}$$

For $V_{in} = 0$

$$V_{cm} = \frac{V_s (R_i // R_f)}{R_b + (R_i // R_f)}$$

$$V_{cm\Delta} = \frac{V_{in} (R_b // R_f)}{R_i + (R_b // R_f)}$$

For $V_{in} > 0$

$$V_{cm} = V_{cm} @ V_{in} = 0 + V_{cm\Delta}$$

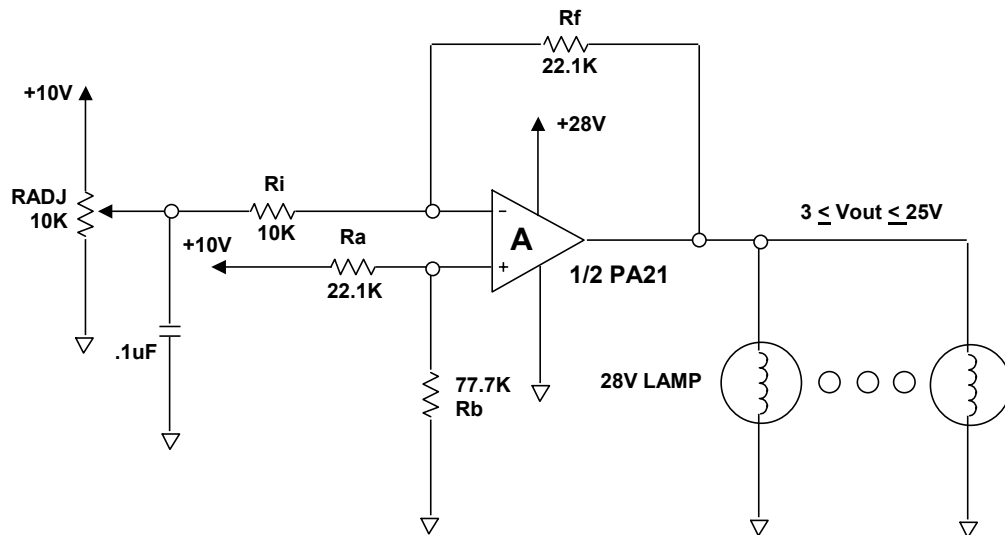
This configuration can easiest be viewed as a differential amplifier with an offset voltage summed in on both + and - input nodes. With this arrangement of resistors the transfer function is: $V_{out} = R_f/R_i V_{in}$.

R_b acts as a summation resistor to force the common mode voltage on the power op amp input to be within the common mode voltage specification. When $V_{in} = 0$, $V_{cm} = f(V_s, R_i, R_f \text{ \& } R_b)$. As V_{in} becomes greater than zero, one can easily calculate the change in common mode voltage using superposition. $V_{cm\Delta} = f(V_{in}, R_b, R_i \text{ \& } R_f)$. Adding these two functions produces V_{cm} for $V_{in} > 0$. Always check V_{cm} for entire range of V_{in} to guarantee common mode range compliance and thereby linear operation of the power op amp.

Inverting operation is actually easier. Simply move the signal source to the -side and ground the +side R_i . V_{cm} is set up in the same manner as above but there is no $V_{cm\Delta}$ to worry about at all. Since R_i and R_f will both go to ground, they could be replaced with a single resistor. For best accuracy keep two individual resistors; your are likely to get better ratios and tracking from +side to -side. Speaking of accuracy, model any current mismatch through the two R_b resistors as flowing through R_f producing an output error. Realize also that most current through R_b flows through the signal source producing an input error if the signal source is not zero impedance.

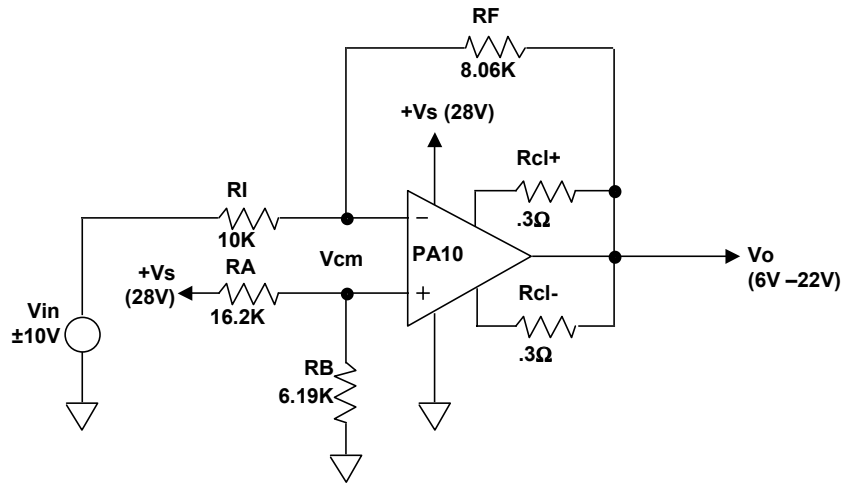
Ref. AN21

AIRCRAFT LIGHT DIMMER CONTROL



Accurate brightness control is provided in this aircraft panel light control circuit. A bank of several parallel connected lamps is driven by the PA21 which operates in a closed loop with a command voltage from a low power 10-turn pot. Offset is summed into the noninverting input of the PA21 to allow a zero to 10V input command on the inverting input to be translated into a 3 to 25V output voltage across the lamps. The 3V allowance for saturation voltage on the output of the PA21 assures an accurate low impedance output at 2.5 amps. The advantage of two power op amps in one package provided by the PA21 allows the design engineer to control two independent dimmer channels from one TO-3 power op amp package. The open loop gain of the PA21, along with its power supply rejection, force a constant commanded voltage across the lamps and thus a constant brilliance regardless of power supply line fluctuations, typical in an aircraft from 16 to 32 volts.

SINGLE SUPPLY— INVERTING



GIVEN: $V_s = 28V$
 $V_{in} = \pm 10V$
 $V_o = 6V \rightarrow 22V$

STEP 3: Offset: Set $V_{in} = 0$, $V_o = 14V$

$$V_o = -V_{in} \frac{R_f}{R_i} + \left\{ \frac{V_s R_B}{R_A + R_B} \right\} \left\{ 1 + \frac{R_f}{R_i} \right\}$$

FIND: Scaling resistor values

$$14V = 0 + \frac{R_f}{R_i} \left\{ \frac{28 R_B}{R_A + R_B} \right\} \left\{ 1 + \frac{R_f}{R_i} \right\}$$

SOLUTION:

$$\frac{R_B}{R_A + R_B} = .278 \rightarrow R_A = 2.6 R_B$$

STEP 1:

$$\text{Gain} = \frac{R_f}{R_i} \quad \text{Offset} = \left\{ \frac{V_s R_B}{R_A + R_B} \right\} \left\{ 1 + \frac{R_f}{R_i} \right\}$$

STEP 2:

$$\text{Gain} = \frac{V_o \text{ p-p}}{V_{in} \text{ p-p}} = \frac{16V}{20V} = .8$$

$$\frac{R_f}{R_i} = .8 \quad \text{Choose } R_i = 10K \rightarrow R_f = 8.06K$$

STEP 4: For minimum offset set

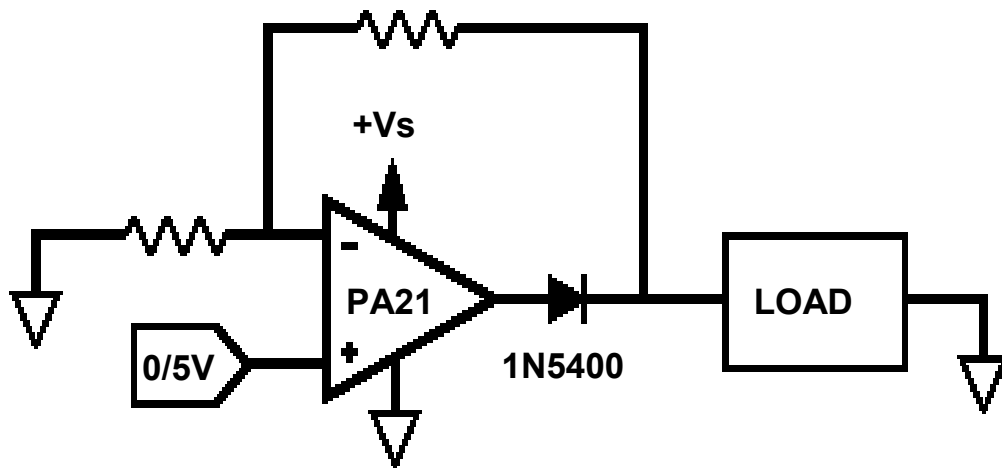
$$R_A || R_B = R_i || R_f$$

Choose $R_A = 16.2K$, $R_B = 6.19K$

STEP 5: Check for common mode:

$$V_{cm} = \frac{28 R_B}{2.6 R_B + R_B} = 7.78V (> 6V \rightarrow \text{OK})$$

Ideal Single Supply Amplifier





The PA21 series amplifiers feature a common mode voltage range from 0.3V below the negative supply rail (ground in this case) to within 2V of the positive rail. These amplifiers also swing to about 0.5V of the rail with very light loads making the diode level shifter above quite practical as long as the load is resistive. With the diode inside the feedback loop it contributes essentially no errors at the load.

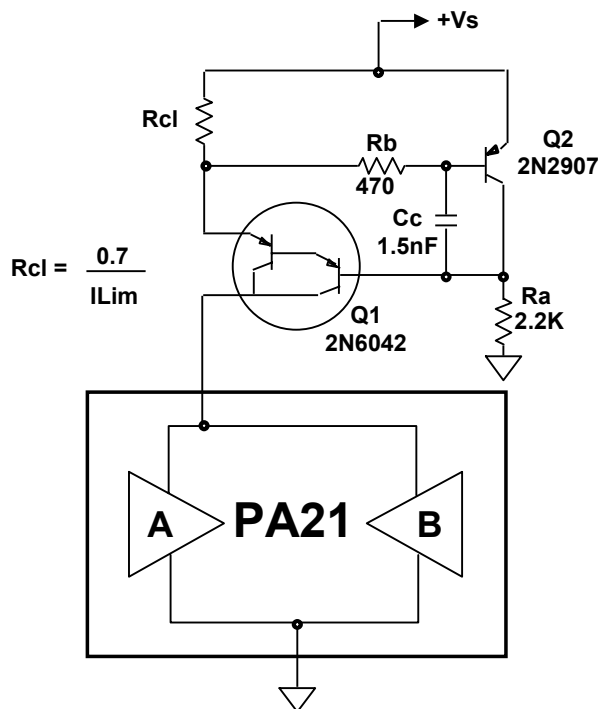
The non-inverting circuit shown is the most common but grounding the +input and using the -input in the normal summing junction fashion will work just as well.

Ref. PA21 DATA SHEET

PROTECTION ALTERNATIVES

CURRENT LIMITING PA21, PA25, PA26

NOTE:  → INVERTING GAIN
 → NO MOTORS



This handy circuit can be used with the PA21 series amplifiers in a single supply application to provide external current limit with minimum components.

By lowering the PA21 current limit one can keep the operating conditions of the PA21 within its SOA.

Q1 is the series pass element providing voltage to the PA21. During current limit we will limit the current to the load by reducing the supply rail. Ra provides a constant biasing current to the base of Q1. When the current through Q1 is sufficient enough to develop a .7V drop across Rcl Q2 turns on and starts to turn off Q1 until current into the PA21 drops below $I_{lim} = .7V/R_{cl}$. Rb and Cc insure the stability of the current limit circuit.

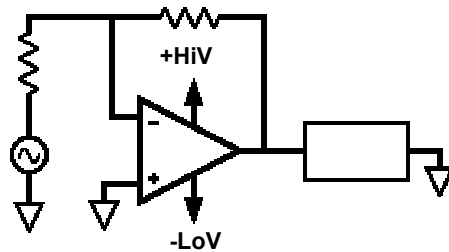
To avoid common mode violations on the input to op amp A and op amp B, as the supply rail is lowered during current limit, it is important to configure both op amp A and op amp B in an inverting gain configuration.

The maximum additional drop through the current limit circuit is 1.7V at up to 3A. This will reduce the maximum output voltage swing available from the PA21.

In a split supply application the negative current limit circuit would replace Q1 with a 2N6045 and Q2 with a 2N2222.

Asymmetrical Supplies

- More common than true single supply
- Less accuracy hassles



There's something very appealing about a circuit with only two gain setting resistors. Many times there is already a low voltage supply in the system just waiting to be used. This supply need only provide quiescent current of the op amp unless the op amp swings negative or in the case of reactive loads where current and voltage are not in phase.

There is nothing magic about having a high positive supply and a low negative supply. As long as the lower voltage supply satisfies the common mode voltage requirement it makes no difference if you turn things over using high negative and low positive. If you are allowed to reverse the load terminals, this could work to significant advantage. Say that the small signal portion of the system runs on +12V or +15V and you need to buy a high power supply to drive the load anyway. If you set up a negative high power rail, the existing low power supply will work fine.

STABILITY AND COMPENSATION

- Ground Loops
- Supply Loops
- Local Internal Loops
- Coupling: Internal and External
- Aol Loop Stability

ELIMINATE COUPLING INTERNAL AND EXTERNAL

- Ground the Case
- Reduce Impedances
- Eliminate Ib Compensation Resistor on +IN
- Don't Run Output Traces Near Input Traces
- Run Iout Traces Adjacent to Iout Return Traces

1. Grounding the case forms a Faraday shield around the internal circuitry of the power amplifier which prevents unwanted coupling from external noise sources.

2. Reducing impedances keeps node impedances low to prevent pick-up of stray noise signals which have sufficient energy only to drive high impedance nodes.

3. Elimination of the Ib compensation resistor on the +input will prevent a high impedance node on the +input which can act as an antenna, receiving unwanted noise or positive feedback, which would result in oscillations. This famous Ib compensation resistor is the one from the +input to ground when running an amplifier in an inverting gain. The purpose of this resistor is to reduce input offset voltage errors due to bias current drops across the equivalent impedance as seen by the inverting and non-inverting input nodes. Modern op amps feature compensated input stages and benefit very little from this technique.

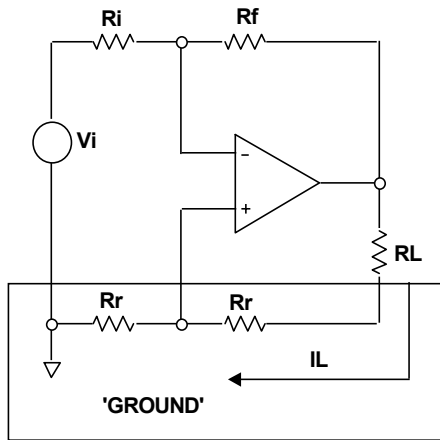
Calculate your DC errors without the resistor. Some op amps have input bias current cancellation negating the effect of this resistor. Some op amps have such low input bias currents that the error is insignificant when compared with the initial input offset voltage. Leave this +input bias resistor out and ground the +input if possible. If the resistor is required, bypass it with a .1 μ F capacitor to ground.

4. Don't route input traces near output traces. This will eliminate positive feedback through capacitive coupling of the output back to the input.

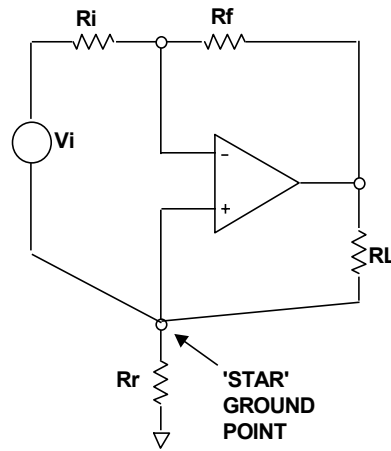
5. Run Iout traces adjacent to Iout return traces. If a printed circuit board has both a high current output trace and a return trace for that high current, then these traces should be routed adjacent to each other (on top of each other on a multi-layer printed circuit board) so they form an equivalent twisted pair by virtue of their layout. This will help cancel EMI generated from outside from feeding back into the amplifier circuit.

Ref. AN1 STABILITY, AN19

GROUND LOOPS



PROBLEM



SOLUTION

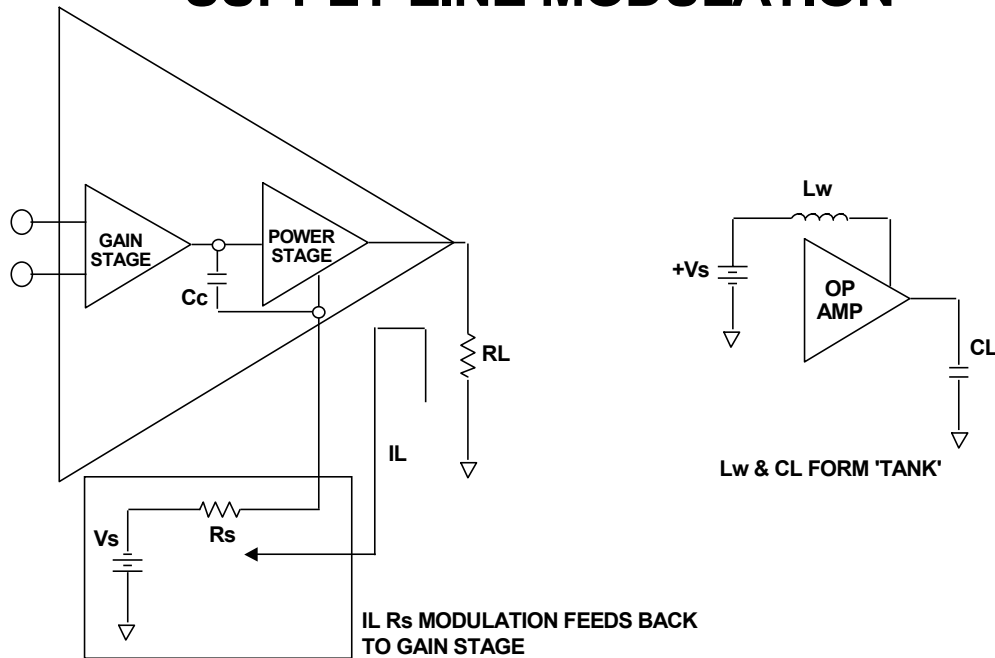
$$f(\text{osc}) = \sim f(\text{unity})$$

Ground loops come about from load current flowing through parasitic layout resistances, causing part of the output signal to be fed back to the input stage. If the phase of the signal is in phase with the signal at the node it is fed back to, it will result in positive feedback and oscillation. Although these parasitic resistances (R_r) in the load current return line cannot be eliminated, they can be made to appear as a common mode signal to the amplifier. This is done by the use of a star ground point approach. The star point is merely a point that all grounds are referred to, it is a common point for load ground, amplifier ground, and signal ground.

The star ground point needs to be a singular mechanical feature. Run each connection to it such that current from no other part of the circuit can mingle until reaching the star point. Don't forget your star point when making circuit measurements. Moving the ground lead around may change the indication leading to false assumptions about circuit operation.

Ref. AN1 STABILITY, AN19

SUPPLY LINE MODULATION

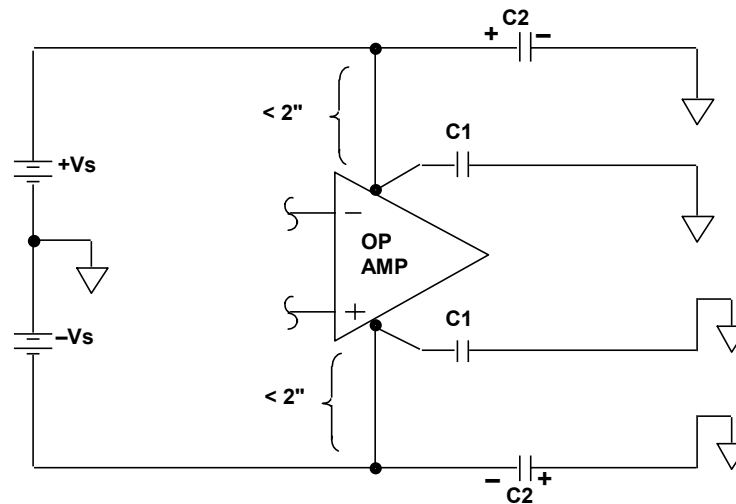


Supply loops are another source of oscillation. In one form of power supply related oscillations the load current flowing through supply source resistance and parasitic trace resistance modulates the supply voltage seen at the power supply pin of the op amp. This signal voltage is then coupled back into a gain stage via the compensation capacitor which is usually referred to one of the supply lines as an AC ground.

Another form of oscillatory circuit that can occur is due to parasitic power supply lead inductance reacting with load capacitance to form a high Q tank circuit.

Ref. AN1 STABILITY, AN19

BYPASSING SUPPLY LINES



C1 = 0.1 to 1 μ F, Ceramic

C2 = 10 μ F/Amp out (peak), Electrolytic

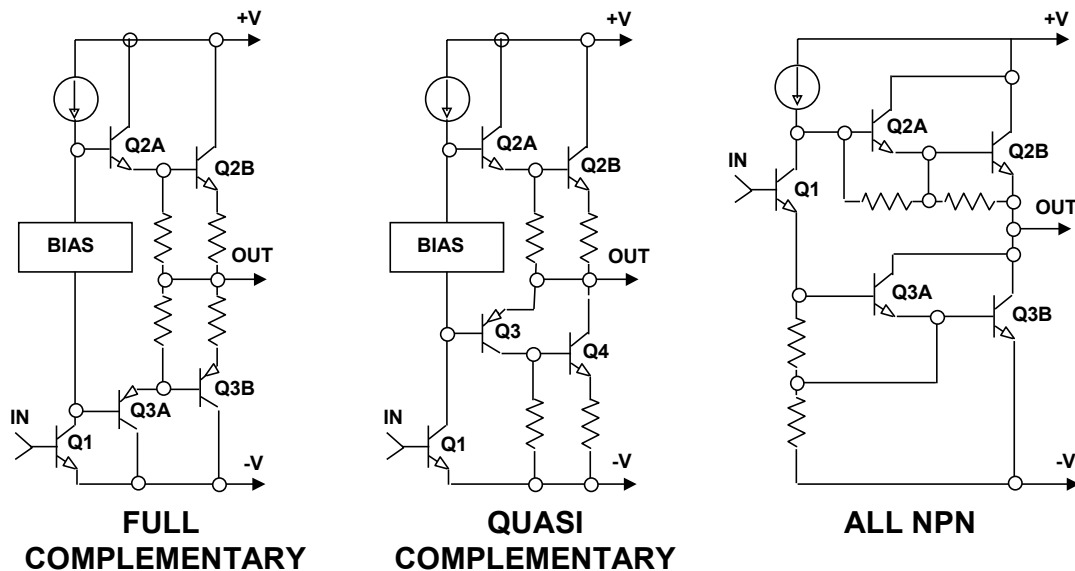
All supply line related oscillation and coupling problems can be avoided with proper bypassing.

The "must do" in all bypassing is a good high frequency capacitor right at each amplifier or socket power supply pin to ground. Not just any ground but the star point ground. This will most often be a multilayer ceramic, at least 1000pF, and as large as possible up to about 1 μ F. Above that capacitance high frequency characteristics shouldn't be taken for granted. Polyesterene, polypropylene, and mylar are possible alternatives when ceramics cannot be used for any reason. Check the manufacturer's data sheet for low ESR at least two times the unity gain bandwidth of the op amp being used.

Once high frequency bypassing is addressed, additional low frequency decoupling is advisable. In general use about 10 μ F/amp of peak output current, either electrolytic or tantalum type capacitors.

Ref. AN1 STABILITY, AN19

BIPOLAR OUTPUT STAGES



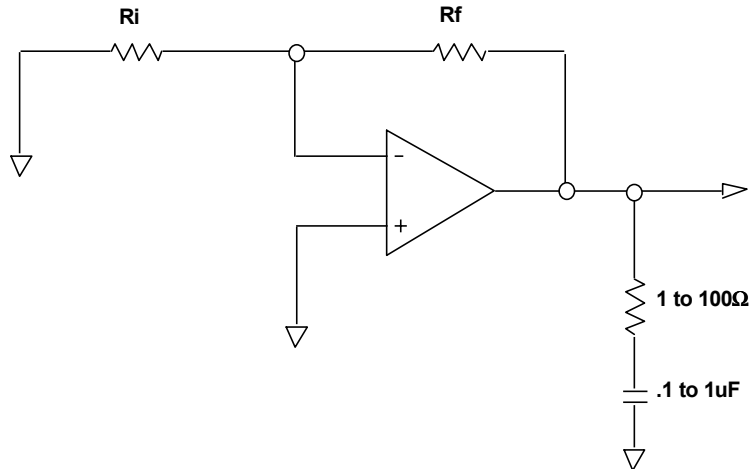
The full complementary output stage is a very easy to use stage. It exhibits symmetric output impedance and low crossover distortion. It is also easy to bias and is inherently stable under most load conditions. Q1 acts as a class A, high voltage gain, common emitter amplifier. Its collector voltage drives the output darlington. The bias circuitry provides class AB operation for the output darlington, minimizing crossover distortion. Both Q2 and Q3 are only called upon to provide impedance buffering. This is a unity voltage gain, high current gain stage. Both devices are operated as followers and thus provide very low output impedance for either sinking or sourcing current. Monolithic designers are constrained to work with NPN's for handling high currents. For this reason, the "all-NPN" output stage, followed by the "quasi-complementary" output stage were developed.

The quasi-complementary is similar to the full complementary in that Q1 again acts as a class A, common emitter, high gain amplifier and the output devices provide impedance buffering only. Q2 provides the same function as Q2 in a full complementary approach. Q3 and Q4 form a "composite PNP". The inherent problem with this approach is that there is heavy local feedback in the Q3, Q4 loop and this can lead to oscillations driving inductive loads.

The "all-NPN" output stage was an early approach to delivering power in a monolithic. During current source this stage operates much the same as the previous two. The major difference comes about during current sink. During the current sink cycle Q1 changes from a common emitter to an emitter follower. It now provides base voltage drive for Q3. Q3 is operated as a common emitter amplifier. The major disadvantage to this approach is the large changes in both output impedance and open loop gain between source and sink cycles. A problem common to both the quasi-complementary and the all NPN stage is the difficulty of biasing properly over extended temperature range.

Ref. AN1 STABILITY, AN19

FIXING OUTPUT STAGE OSCILLATIONS



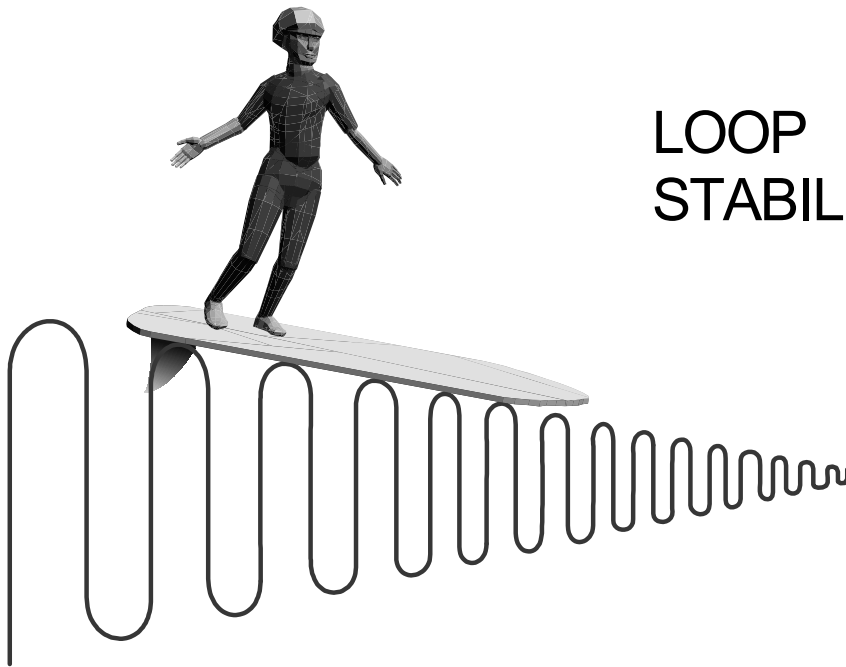
$$F(\text{osc}) > f(\text{unity})$$

Any time you encounter an oscillation above the unity gain bandwidth of the amplifier it is bound to be one of the output stage problems discussed previously. These can be fixed through the use of a simple “snubber” network from the output pin to ground. This network is comprised of a resistance of from 1 to 100 ohms in series with a .1 to 1 uF capacitor. This network passes high frequencies to ground, thus preventing it from being fed back to the input.

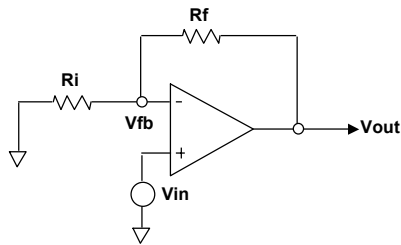
Some manufacturers who use all NPN output stages in their monolithic power amplifiers suggest the use of this type of network to reduce output stage oscillations. Other manufacturers, while having a similar problem, never suggest that this type of network is necessary for proper use. Apex either takes care of the problem internally or specifies specific values for the external network.

Ref. AN1 STABILITY, AN19

LOOP STABILITY

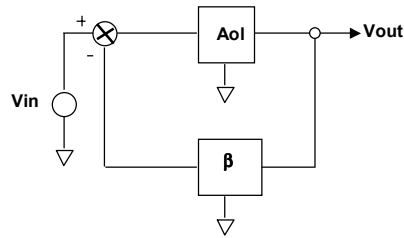


BETA (β) - FEEDBACK FACTOR



$$\beta = \frac{R_i}{R_i + R_f}$$

$$V_{fb} = \beta V_{out}$$



$$\frac{V_{out}}{V_{in}} = \frac{A_{ol}}{1 + A_{ol} \beta} = 1/\beta$$

(For $A_{ol} \beta \gg 1$)

$$V_{fb} = \frac{V_{out} R_i}{R_i + R_f}$$

$$V_{out} = V_{in} A_{ol} - A_{ol} \beta V_{out}$$

$$V_{fb} = \beta V_{out}$$

$$\frac{V_{out} + A_{ol} \beta V_{out}}{V_{in}} = A_{ol}$$

$$\beta = \frac{R_i}{R_i + R_f}$$

$$\frac{V_{out}}{V_{in}} = \frac{A_{ol}}{1 + A_{ol} \beta} = \frac{1}{\beta}$$

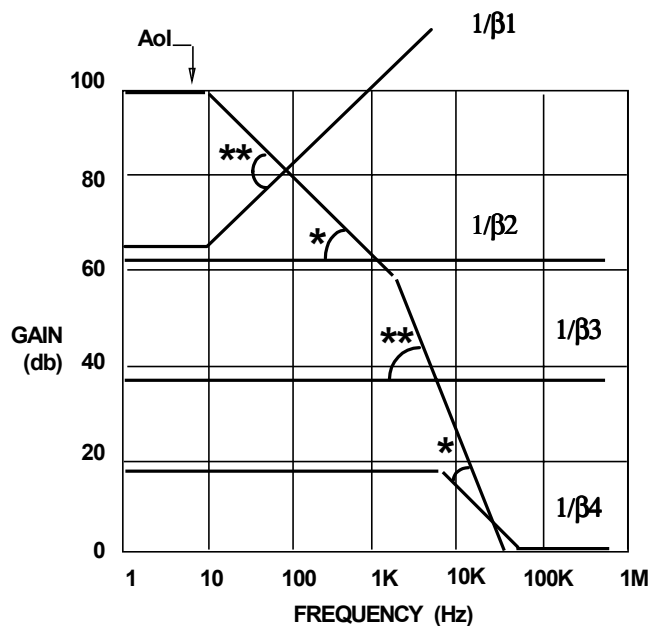
(For $A_{ol} \beta \gg 1$)

Control theory is applicable to closing the loop around a power op amp. The block diagram above in the right consists of a circle with an X, which represents a voltage differencing circuit. The rectangle with A_{ol} represents the amplifier open loop gain. The rectangle with the β represents the feedback network. The value of β is defined to be the fraction of the output voltage that is fed back to the input. Therefore, β can range from 0 (no feedback) to 1 (100% feedback).

The term $A_{ol}\beta$ that appears in the V_{out}/V_{in} equation above has been called loop gain because this can be thought of as a signal propagating around the loop that consists of the A_{ol} and β networks. If $A_{ol}\beta$ is large there is lots of feedback. If $A_{ol}\beta$ is small there is not much feedback (for a detailed discussion of this and other useful topics related to op amps refer to: Intuitive IC Op Amps, Thomas M. Frederiksen, National's Semiconductor Technology Series, R.R. Donnelley & Sons).

Ref. AN19

RATE OF CLOSURE & STABILITY



* 20 db/ decade Rate of Closure → “Stability”

** 40 db /decade Rate of Closure → “Marginal Stability”

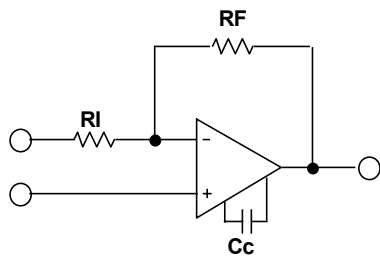
Aol is the amplifier’s open loop gain curve. $1/\beta$ is the closed loop AC small signal gain in which the amplifier is operating. The difference between the Aol curve and the $1/\beta$ curve is the loop gain. Loop gain is the amount of signal available to be used as feedback to reduce errors and non-linearities.

A first order check for stability is to ensure that when loop gain goes to zero, that is where the $1/\beta$ curve intersects the Aol curve, open loop phase shift must be less than 180 at the intersection of the $1/\beta$ curve and the Aol curve the difference in the slopes of the two curves, or RATE OF CLOSURE is less than or equal to 20 dB per decade. This is a powerful first check for stability. It is, however, not a complete check. For a complete check we will need to check the open loop phase shift of the amplifier throughout its loop gain bandwidth.

A 40 dB per decade RATE-OF-CLOSURE indicates marginal stability with a high probability of destructive oscillations in your circuit. Above examples indicate several different cases for both stable (20 dB per decade) and marginally stable (40 dB per decade) rates of closure.

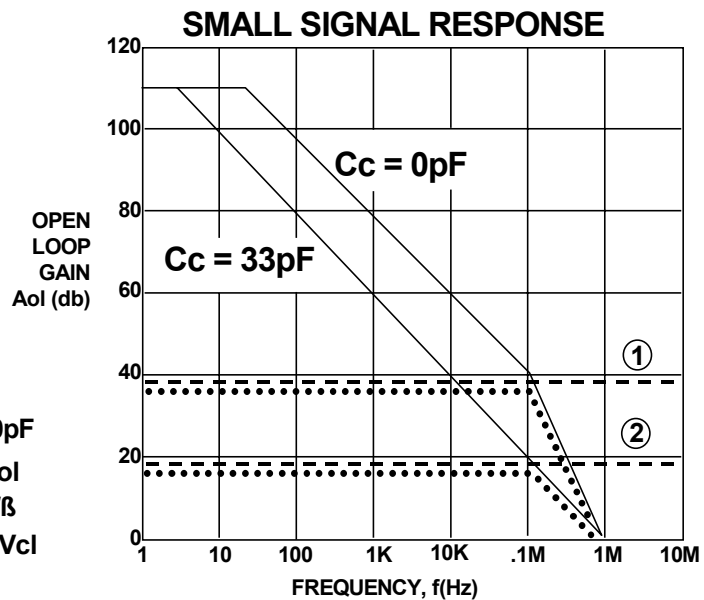
Ref. AN19

EXTERNAL PHASE COMPENSATION



- ① Stable for any C_c
- ② Unstable for $C_c = 0\text{pF}$

——— A_{ol}
 - - - - $1/\beta$
 AV_{cl}



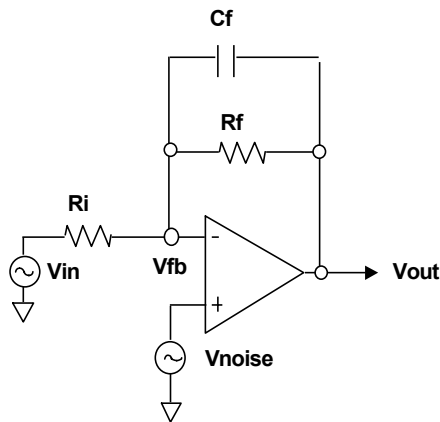
External phase compensation is often available on an op amp as a method of tailoring the op amp's performance for a given application. The lower the value of compensation capacitor used the higher the slew rate of the amplifier. This is due to fixed current sources inside the front end stages of the op amp. Since current is fixed, we see from the relationship of $I=CdV/dt$ that a lower value of capacitance will yield a faster voltage slew rate.

However, the advantage of a faster slew rate has to be weighed against AC small signal stability. In the figure above we see the A_{ol} curve for an op amp with external phase compensation. If we use no compensation capacitor, the A_{ol} curve changes from a single pole response with $C_c=33\text{pF}$ to a two pole response with $C_c=0\text{pF}$. Curve 1 illustrates that for $1/\beta$ of 40 dB the op amp is stable for any value of external compensation capacitor (20 dB/decade rate of closure for either A_{ol} curve, $C_c=33\text{pF}$ or $C_c = 0\text{pF}$).

Curve 2 illustrates that for $1/\beta$ of 20 dB and $C_c=0\text{pF}$, there is a 40 dB/decade rate of closure or marginal stability. To have stability with $C_c=0\text{pF}$ minimum gain must be set at 40dB. This requires a designer to not only look at slew rate advantages of decompensating the op amp, but also at the gain necessary for stability and the resultant small signal bandwidth.

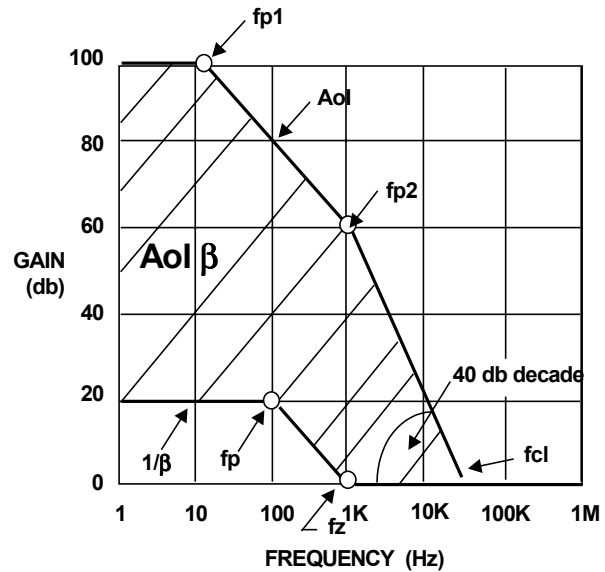
Ref. AN19

STABILITY – RATE OF CLOSURE



$$f_p = \frac{1}{2\pi R_f C_f}$$

$$f_z = \frac{R_i + R_f}{2\pi R_i R_f C_f}$$



The example above shows a typical single pole op amp configuration in the inverting gain configuration. Notice the additional Vnoise voltage source shown at the + input of the op amp. This is shown to aid in conceptually viewing the $1/\beta$ plot.

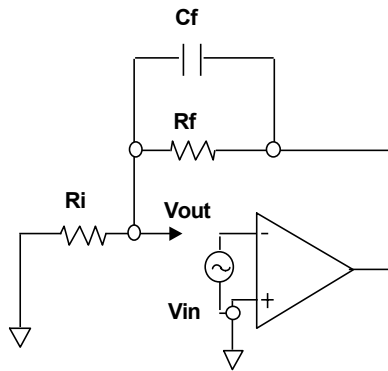
An inverting amplifier, with its + input grounded, will always have potential for a noise source to be present on the + input. Therefore, when one computes the $1/\beta$ plot, the amplifier will appear to run in a gain of $1 + R_f/R_i$ for small signal AC. The V_{out}/V_{in} relationship will still be $-R_f/R_i$.

The plot above shows the open loop poles from the amplifier's Aol curve as well as the poles and zeroes from the $1/\beta$ curve. The locations of f_p and f_z are important to note as when we look at the open loop stability check we will see that poles in the $1/\beta$ plot will become zeroes and zeroes in the $1/\beta$ plot will become poles in the open loop stability check.

Notice that at f_{cl} the RATE-OF-CLOSURE is 40 dB per decade indicating a marginal stability condition. The difference between the Aol curve and $1/\beta$ curve is labelled $Aol\beta$ which is also known as loop gain.

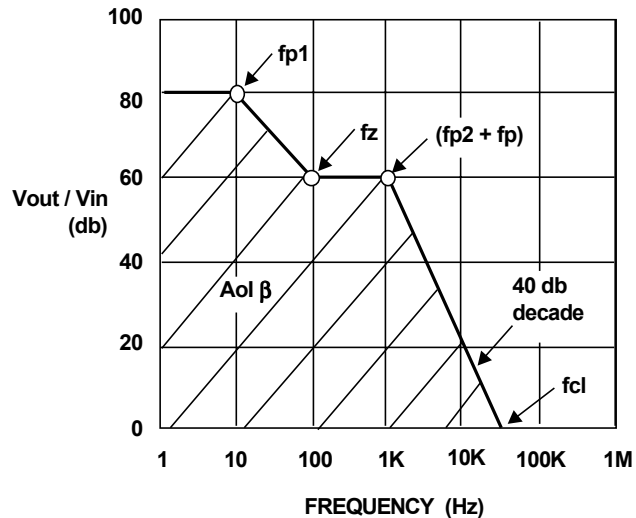
Ref. AN19

STABILITY – OPEN LOOP



$$f_z = \frac{1}{2\pi R_f C_f}$$

$$f_p = \frac{R_i + R_f}{2\pi R_i R_f C_f}$$



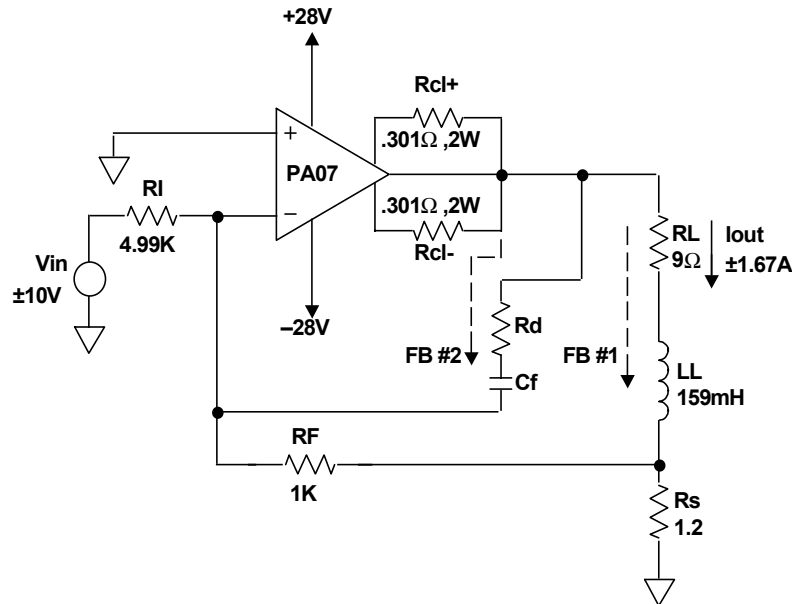
Stability checks are easily performed by breaking the feedback path around the amplifier and plotting the open loop magnitude and phase response. This open loop stability check has the first order criteria that the slope of the magnitude plot as it crosses 0 dB must be 20 dB per decade for guaranteed stability.

The 20 dB per decade is to ensure that the open loop phase does not dip to -180 degrees before the amplifier circuit runs out of loop gain. If the phase did reach -180 the output voltage would now be fed back in phase with the input voltage (-180 degrees phase shift from negative feedback plus -180 degrees phase shift from feedback network components would yield -360 degrees phase shift). This condition would continue to feed upon itself causing the amplifier circuit to break into uncontrollable oscillations.

Notice that this open loop plot is a plot of $A_{ol} \beta$. The slope of the open loop curve at f_{cl} is 40 dB per decade indicating a marginally stable circuit. As shown, the zero from the $1/\beta$ plot became a pole in the open loop plot and the pole from the $1/\beta$ plot became a zero. We will use this knowledge to plot the open loop phase plot to check for stability. This plotting of the open loop phase will provide a complete stability check for the amplifier circuit. All the information we need will be available from the $1/\beta$ curve and the A_{ol} curve.

Ref. AN19

V-I CIRCUIT & STABILITY



This V-I (Voltage to Current) topology is a floating load drive. Neither end of the load, series RL and LL, is connected to ground.

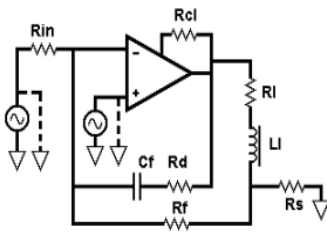
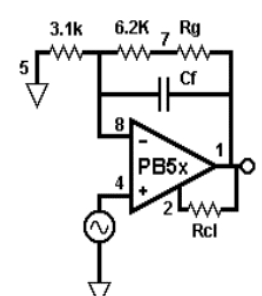
The easiest way to view the voltage feedback for load current control in this circuit is to look at the point of feedback which is the top of Rs. The voltage gain V_{Rs}/V_{in} is simply $-R_F/R_I$ which translates to $(-1K/4.99K = -.2004)$. The I_{out}/V_{in} relationship is then V_{Rs}/R_s or $I_{out} = -V_{in}(R_F/R_I)/R_s$ which for this circuit is $I_{out} = -.167V_{in}$.

We will use our knowledge of $1/\beta$, Rate of Closure, and open loop stability phase plots, to design this V-I circuit for stable operation. There are two voltage feedback paths around the amplifier, FB#1 and FB#2. We will analyze FB#1 first and then see why FB#2 is necessary for guaranteed stability.

Ref. AN19

PA07 Inductive Load Problem Entry

STABILITY FOR INDUCTIVE LOADS					
MODEL	PA07	Note/PBs	Rin	4.99 Kohms	Estimated Closure Frequency = 1 KHz
Rs		1.2 Ohms	Rf	1 Kohms	Suggested maximum bandwidth 316.2278 Hz
Load		159 mH	Cf	9999 nF	Estimated Closure Rate = 40.0 db/decade
Rload		9 Ohms	Rd	999999999 Kohms	Estimated Phase Margin = 0.41 Degrees
			Is this a Composite?	No	
Notes:					
R-C Pole Calculator +:					
82 Kohms	Rd Kohms	82.47245	AC gain db	40	28 Print Data, Bode & Phase
32 Hz	Rd Kohms	84.18197	Rd Kohms	82.47245	29 Print Data, Bode, Phase & Parts
60.654 nF	Cf nF	1.11E-06			
Ri/(Ri+Rf)		0.833055092			
Equiv Z @ Rs		1.199759647	Ohms		
Requiv/(Ri+Requiv)		0.117626267			
DC Beta		0.09798916			
DC Gain		20.17643928	db		
Zero R/L		10.20969916	Hz		
Rin Rf		0.833055092	Kohms		
Zero Rd/Cf		1.59171E-08	Hz		
AC Gain		181.5865255	db		
Zero Cross		1000	Hz		

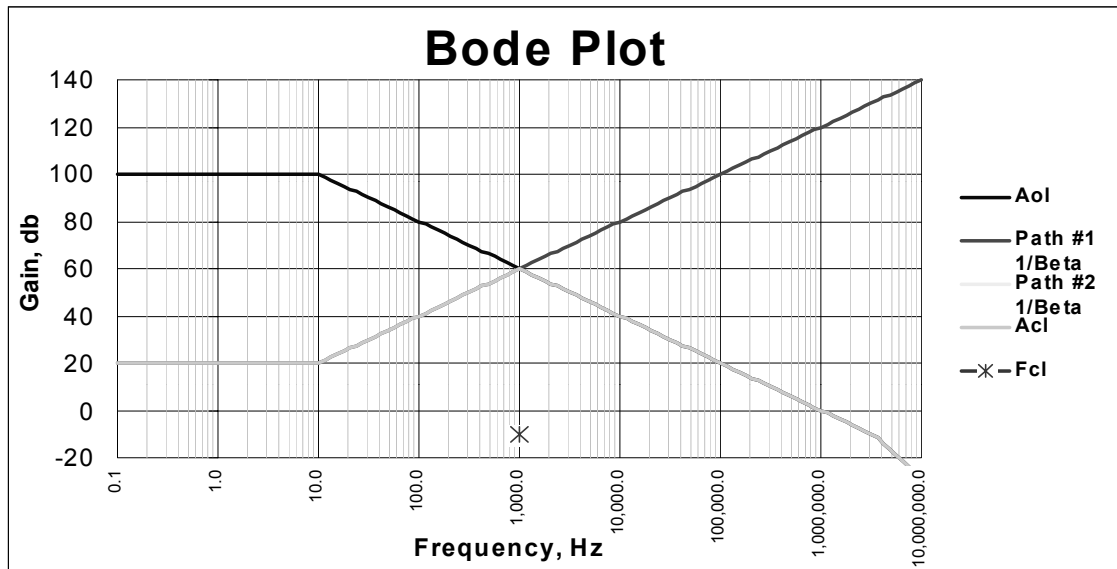



The Load sheet of Power Design.xls will handle inverting or non-inverting circuits. In this example we can enter our component values in a straight forward manner. For non-inverting circuits you probably want to enter $\cong 100M$ for Rin. To illustrate the basic problem with inductors inside the feedback loop we enter high values for the R-C stabilizing network.

Notice first on the right, rate of closure and phase margin are both not acceptable. Back to the left and down a little is a handy calculator for analyzing and selecting component values. To the right are two suggestions for the value of Rd and one for Cf. More to the right we find a yellow entry cell for setting Rd for a specific AC gain. Below this are listed several operating points of the circuit. The liberal scattering of red triangles are notes of explanation (brought up by cursor placement). Application Note 19, Stability for Power Amplifiers is the reference to consult for detailed information.

Ref. AN19,AN38

Aol & FB#1 Magnitude Plot for Stability



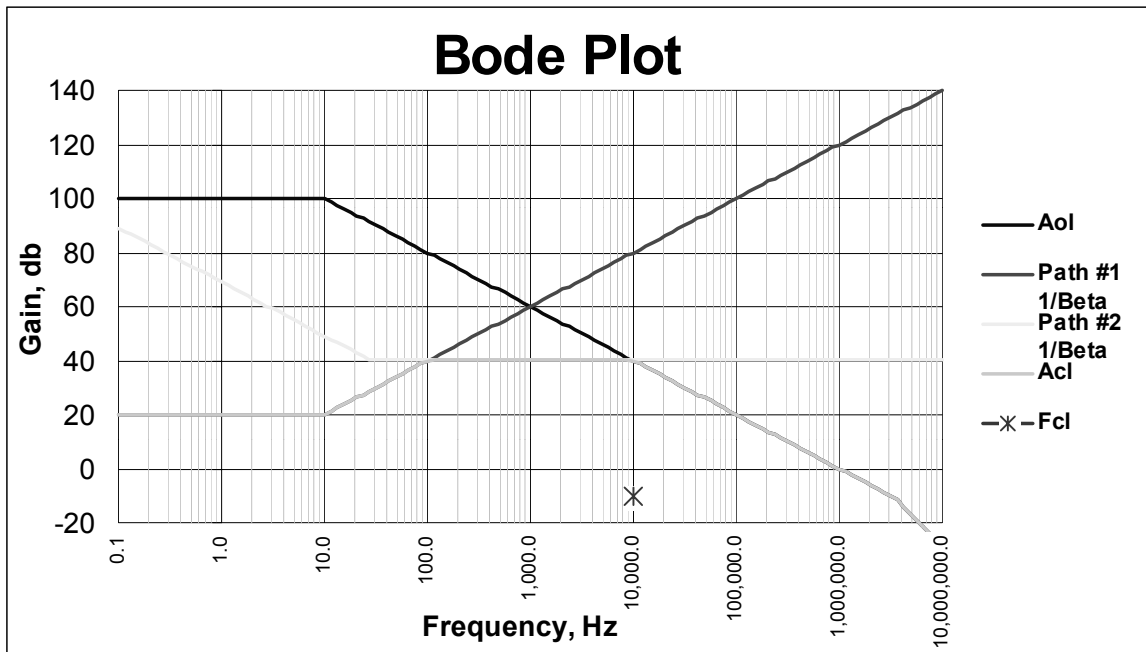
As frequency increases, impedance of the inductor increases and being inside the feedback loop it is causing closed loop gain to increase. Another way to view it: The amplifier's job is to drive constant current but as frequency goes up it needs more voltage to maintain that constant current, so voltage gain is increasing with frequency.

Open loop gain is decreasing 20db per decade and closed loop gain is increasing 20db per decade. This intersection rate of 40db per decade is the problem.

What if we could invent a circuit to make the open loop gain stop increasing? The precise function of feedback path #2! As soon as we enter this in the data entry screen, we see 20db per decade and phase margin of 45°.

Ref. AN19,AN38

Aol & FB#2 Magnitude Plot for Stability

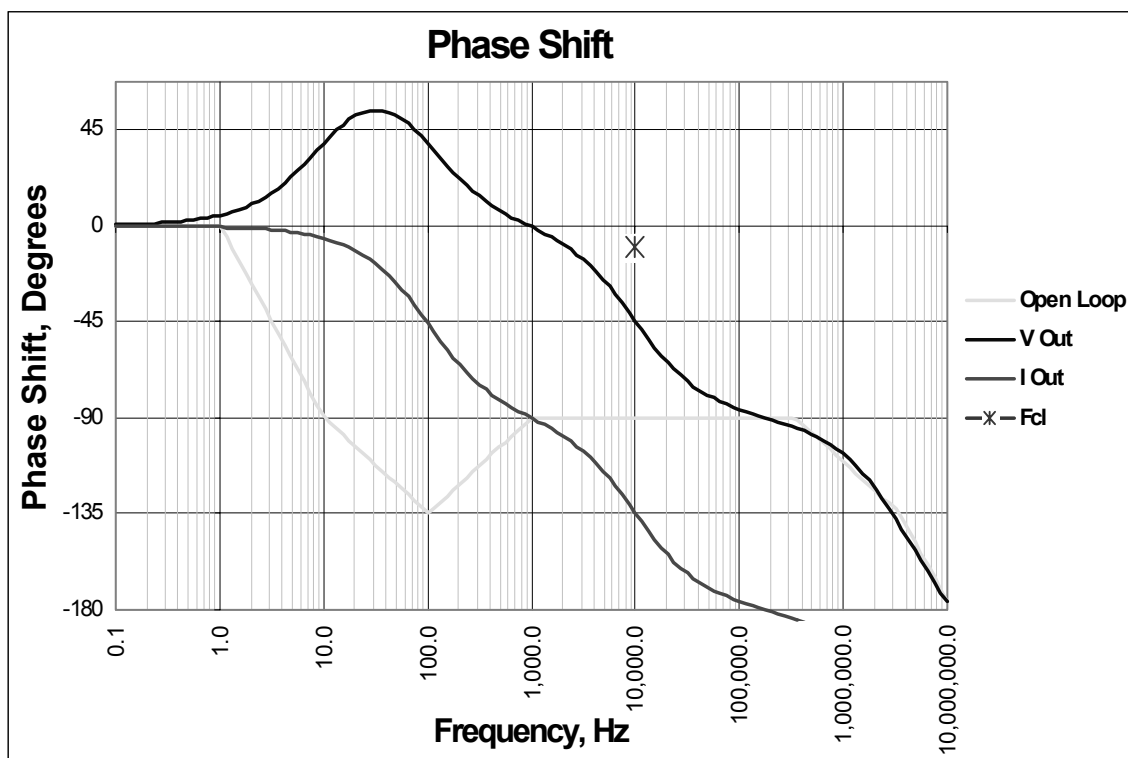


Here's a way to start:

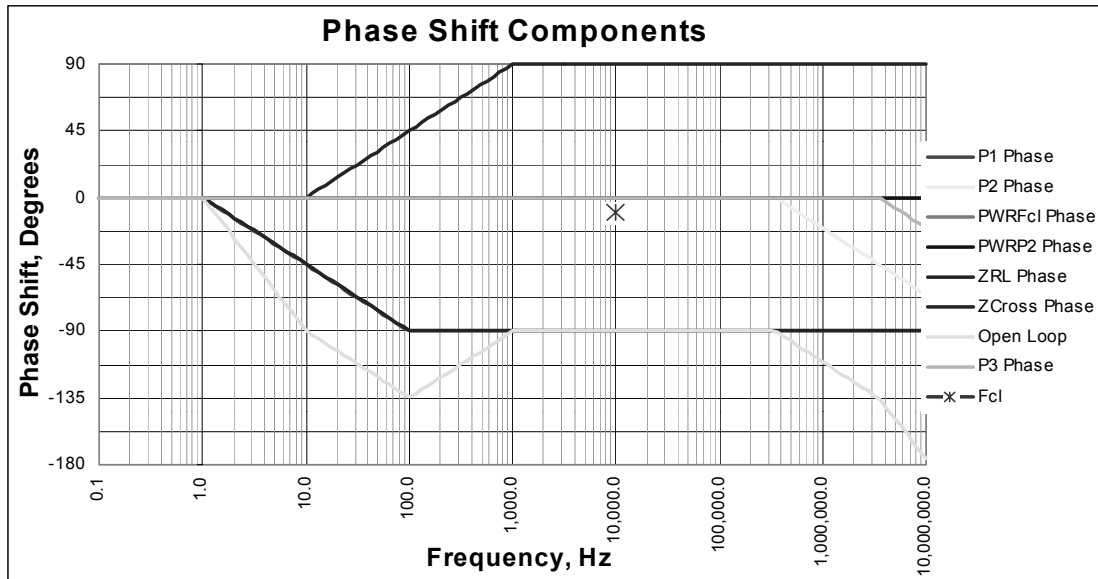
1. Select R_d for an AC gain either 20db below gain at the intersection or 20db above the DC gain of the current feedback (Path 1). These two points are the two suggested R_d values on the data entry screen. We can also read 40db from the graph and enter it as AC gain. An 82K should work well.
2. Select C_f for a corner frequency $\frac{1}{2}$ to 1 decade below the intersection frequency. Giving the calculator pad 82K and 30Hz allows it to suggest a standard value of 68nF (with a little help from you). After entering 82K for R_d , the data entry screen will suggest a capacitor based on 1 decade below the intersection frequency.
3. Play "what if" with the circuit.
4. If trying to achieve higher bandwidth, try increasing the value of R_s .

Ref. AN19,AN38

Phase Plot for Stability

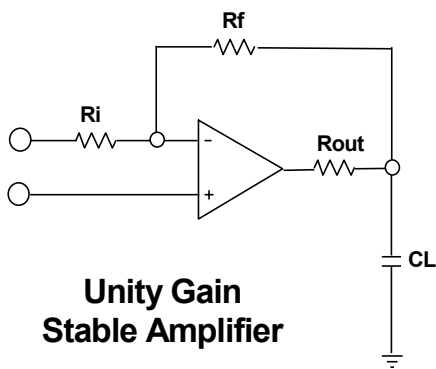


Phase Shift Components



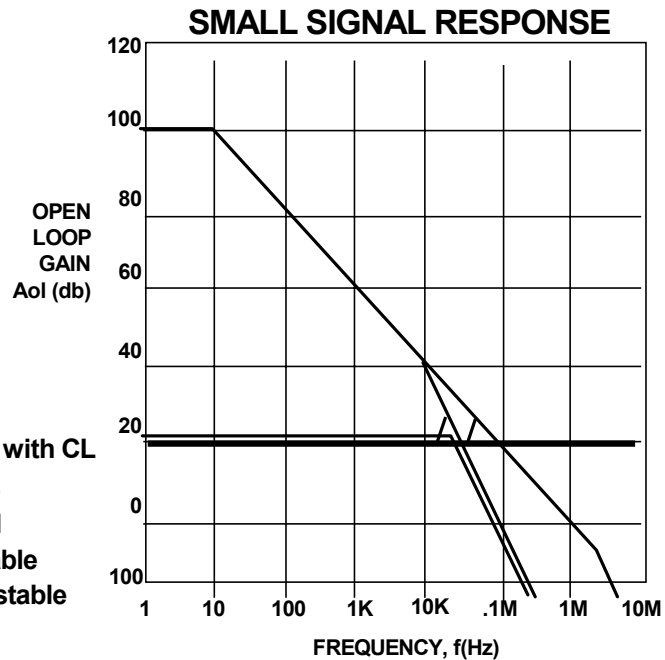
Here are all the pieces going into the previous phase plot. Again, Application Note 19 is the reference.

CAPACITIVE LOADING



Unstable
40db/decade
with CL

- Aol
- Aol with CL
- 1/β
- Acl
- Stable
- Unstable

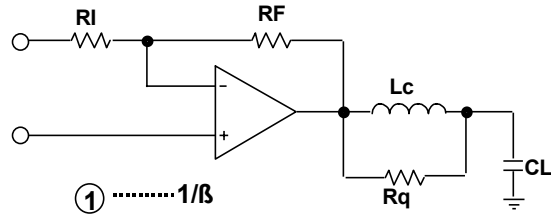
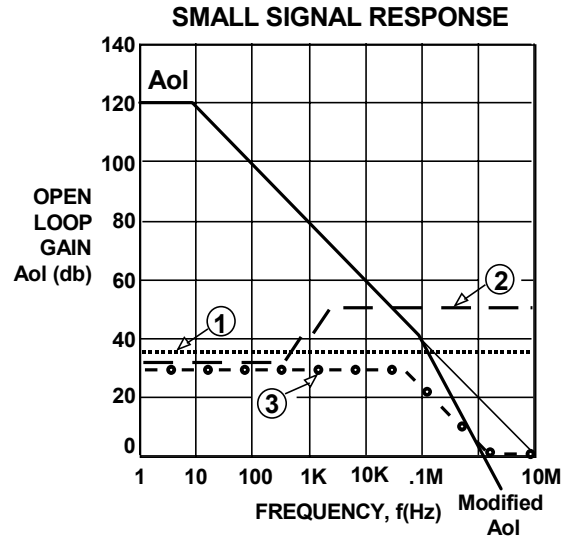
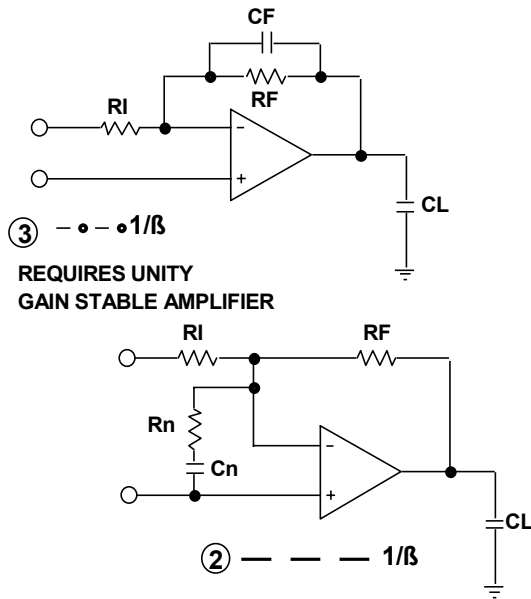


Even when using a unity gain stable amplifier, capacitive loads react with amplifier output impedance, which has the effect of introducing a second pole into the amplifier response which occurs below the unity gain crossover frequency.

If the amplifier is used at a low enough loop gain, this will result in the unstable condition shown in this graph. One simple solution is to increase the closed loop again.

Ref. AN19,AN25

CAPACITIVE LOAD COMPENSATION



If it's necessary to use low gains with capacitive loads, or in the unlikely event they are a problem at higher gain, these techniques can help solve stability problems caused by capacitive loads.

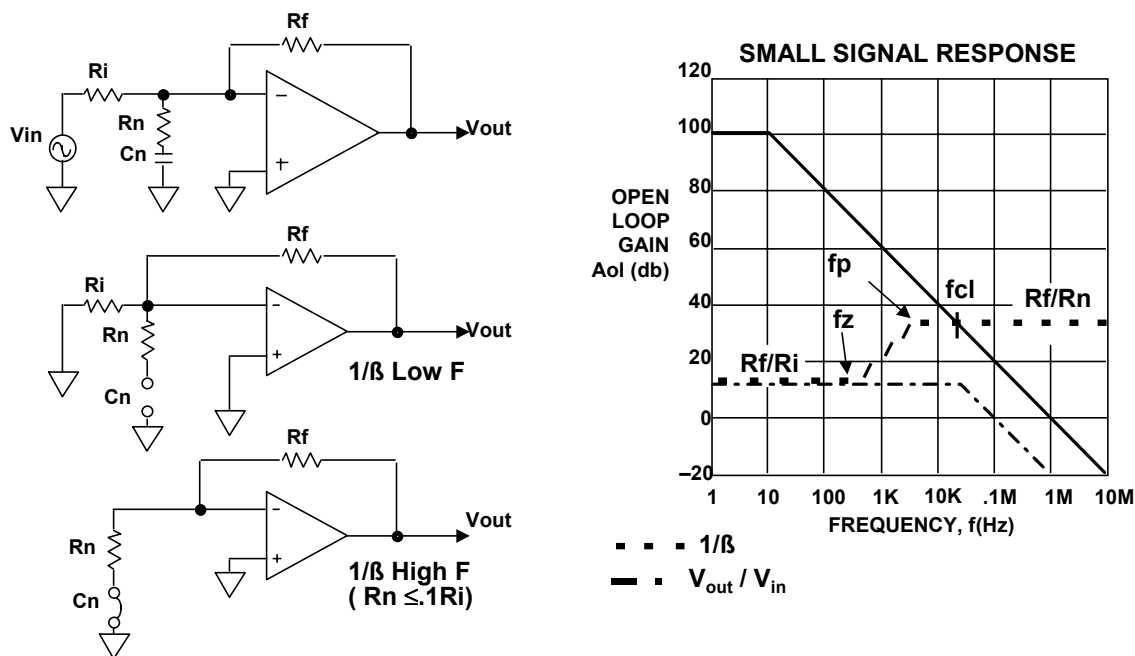
Method 1 uses a parallel inductor-resistor combination in series with amplifier output to isolate or cancel the capacitive load. Feedback should be taken directly from the amplifier's Aol output. In the graph, this has the effect of restoring the amplifier response to 20db/decade. This method has the advantage that with proper component selection, it can produce an overdamped or critically damped response to a square wave. The inductor is typically 3 to 10 μ H, and the resistor from 1 to 10 ohms; although a higher voltage, lower current amplifier like PB58 needs about 35 μ H and 20 Ω .

Method 2 uses "noise gain compensation" to enhance stability. This method will work in virtually all cases. The idea is to set the ratio of R_F/R_n for a gain high enough to insure crossing the Aol line at a stable point. The capacitor, C_n , is selected for a corner frequency one-tenth the Aol crossover.

Method 3 uses a capacitor in the feedback path to cause a phase lead in the feedback which cancels the phase lag due to capacitive loading. This technique requires careful selection of capacitor value to ensure $1/\beta$ crosses the modified Aol before unity gain, unless a unity gain stable amplifier which has a good phase margin is used.

Ref. AN19,AN25

NOISE-GAIN COMPENSATION



This plot illustrates how Noise Gain Compensation works. One way to view noise gain circuits is to treat the amplifier as a summing amplifier. There are two input signals into this inverting summing amplifier. One is V_{in} and the other is a noise source summed in via ground through the series combination of R_n and C_n . Since this is a summing amplifier, V_o/V_{in} will be unaffected if we sum zero into the R_n - C_n network. However, in the small signal AC domain, we will be changing the $1/\beta$ plot of the feedback as when C_n becomes a short and if $R_n \ll R_i$ the gain will be set by R_f/R_n . The figure above shows the equivalent circuits for AC small signal analysis at low and high frequencies.

Notice in the plot above that the V_o/V_{in} relationship is flat until the Noise Gain forces the loop gain to zero. At that point, f_{cl} , the V_o/V_{in} curve follows the A_{ol} curve since loop gain is gone to zero. Since noise gain introduces a pole and a zero in the $1/\beta$ plot, here are a few tips to keep phase under control for guaranteed stability. Keep the high frequency, flat part of the noise gain no higher in magnitude than 20dB greater than the low frequency gain. This will force f_p and f_z in the above plot to be no more than a decade apart. This will also keep the open loop phase from dipping below -135° since there is usually an additional low frequency pole due to the amplifier's A_{ol} already contributing an additional -90° degrees in the open loop phase plot. Keep f_p one-half to one decade below f_{cl} to prevent a rate of closure of 40dB per decade and prevent instability if the A_{ol} curve shifts to the left which can happen in the real world.

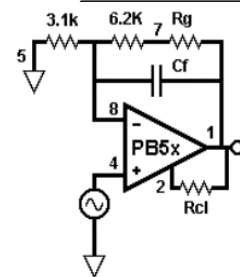
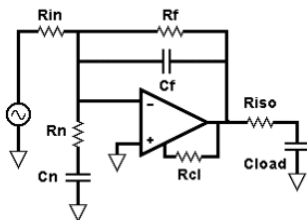
Usually one selects the high frequency gain and sets f_p . f_z can be gotten graphically from the $1/\beta$ plot. For completeness here are the formulae for noisegain poles and zeroes:

$$f_p = \frac{1}{2\pi R_n C_n} \quad f_z = \frac{R_f + R_i}{2\pi (C_n) (R_f R_i + R_f R_n + R_i R_n)}$$

Ref. AN19,AN25

PA07 with a BIG Cload

STABILITY FOR CAPACITIVE LOADS					45 Goto Composite
MODEL	PA07	Note/PBs	Rn	99999999 Kohms	Estimated Closure Frequency = 36.51741 KHz
Rcl		0.4 Ohms	Cn	0 nF	Suggested maximum bandwidth 8.659643 KHz
Cload		4 uF	Cf	0 pF	Estimated Closure Rate = 40.0 db/decade
Rin		2 Kohms	Riso	0 Ohms	Estimated Phase Margin = 25.8688 Degrees
Rf		20 Kohms			
Notes:					
R-C Pole Calculator:					
20 Kohms		0.1 Kohms		30 KHz	28 Print Data, Bode & Phase
20 KHz		10 nF		4 uF	29 Print Data, Bode, Phase & Parts
0.3979 nF		159.15494 KHz		1.326291192 Ohms	
Total Rout		2.9 Ohms			
Pole Zout/Cload		13.720253 KHz			
1/Beta (DC)		20.8 db			
Noise Gain		0.0 db			
Pole Noise Gain		15.915494 KHz			
Zero Noise Gain		15.915487 KHz			
Pole Cf/Rf		7.958E+09 KHz			
Zero Rf/Cf		8.754E+10 KHz			
Zero Riso/Cload		3.979E+09 KHz			
Page Down for Plots.					

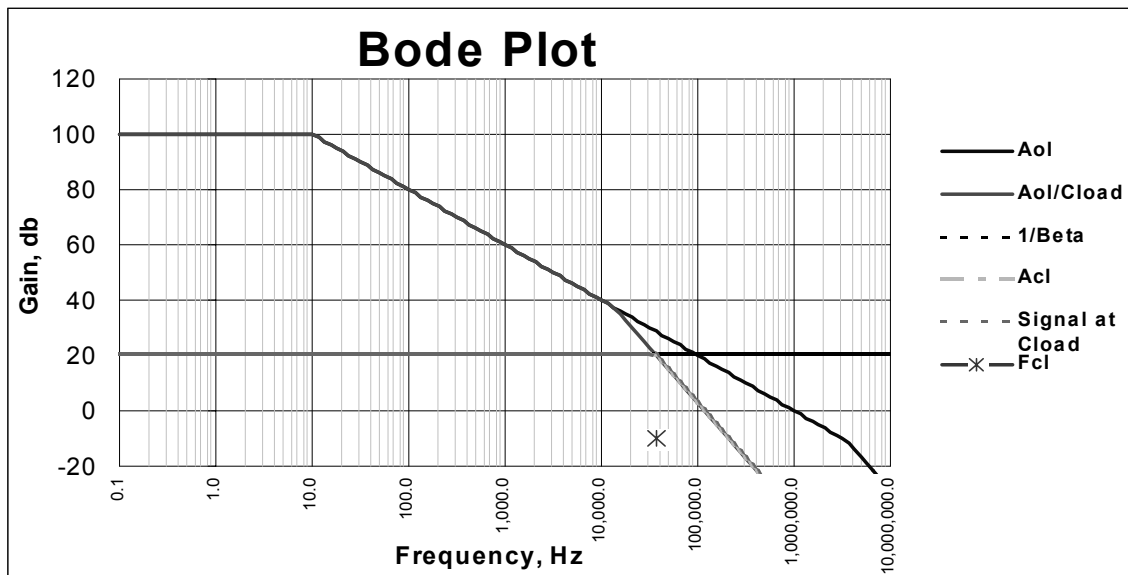


This basic circuit will demonstrate how each of the capacitive load compensation techniques can work independently to solve the large C load stability problem.

This screen sets up the problem. Enter values describing the circuit being sure to assign *open* values to components not yet in the circuit. To the right we see a 40db closure rate and less than 30° phase margin. We don't need them yet but please note the three windows of the R-C Pole Calculator . The first window tells us 398pF will yield a pole at 20KHz when paralleled with 20K. The last window tells us 1.3Ω will place the corner frequency at 30KHz when in series with 4μF.

Ref. AN38

PA07/Clod Problem



This picture is the first part of the problem. The output impedance of the PA07, plus the current limit resistor along with the big capacitive load, have added an additional pole to the open loop response of the amplifier. This degrades closure rate to 40db per decade--a warning flag. Its too bad we can't use a gain of 100 (40db) where closure rate would have been OK.

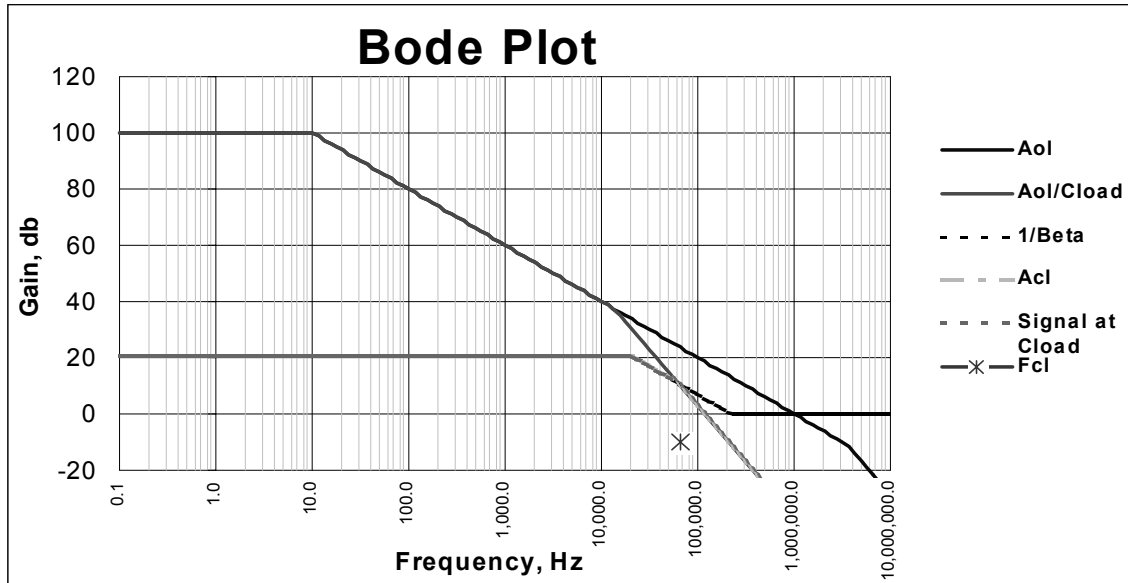
Here's the beauty of this system: Visualize or hold anything with a straight edge up to the graph in the area where we just learned a roll-off capacitor fixes these problems. Hold the edge parallel to the original open loop response curve and move it around to achieve intersection with the modified response about ½ way between 0 & 20db. Read the frequency where the straight edge crosses 20db. Remember the 20KHz in the R-C Pole Calculator? This is the origin. The spreadsheet makes it very easy to play "what if".

For noise gain compensation, visualize the upper flat portion of the curve being 20db up from the DC gain. Setting $R_n = R_{in}/9$ will put you about where it should be. On the open loop gain curve, read frequency where the imaginary line crosses. Enter one tenth this frequency and the R_n value in the R-C Pole calculator to set C_n . Again, play what if to optimize the circuit.

For Riso pick a frequency a little lower than the intersection of DC gain and the modified open loop gain. It looks like 30KHz is about as high as we should go. Use the R-C Pole Calculator, plug in values and optimize.

Ref. AN38

PA07/Clload Cf Solution



A 390pF capacitor yields 61° phase margin.

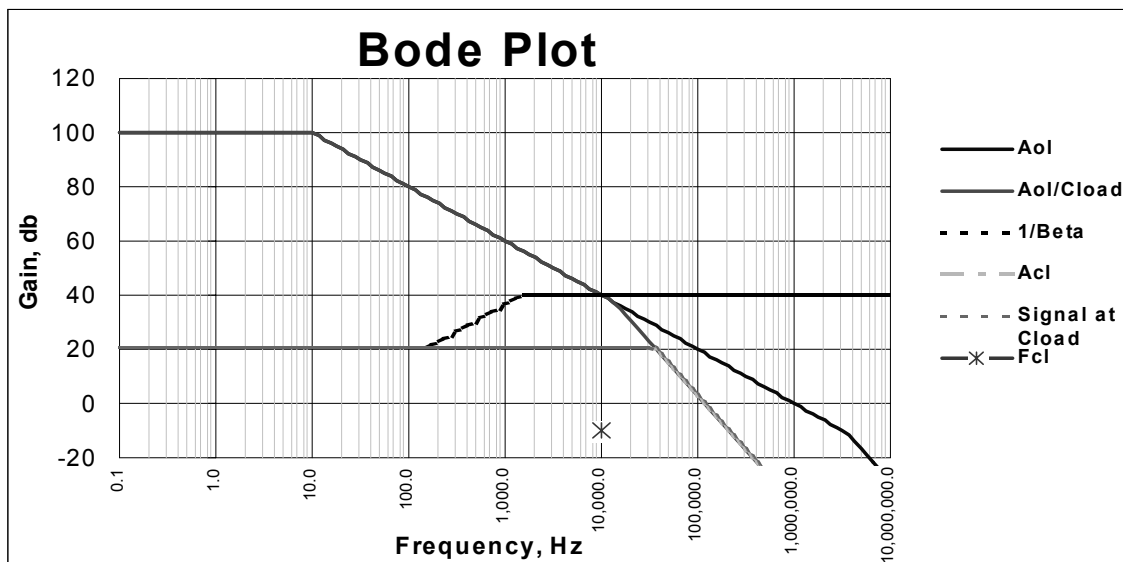
Time to use our vision again to discover a very important trap NOT to fall into.

The trap: If a little capacitor is good, a bigger one should be better.

The problem: 1/beta never goes below 0db.

Visualize a line segment for a 3.9nF capacitor starting down at 2KHz, then turning horizontal at 0db. Intersection rate is again 40db/decade and phase margin will drop to 16°!

PA07/Cload Noise Gain Solution



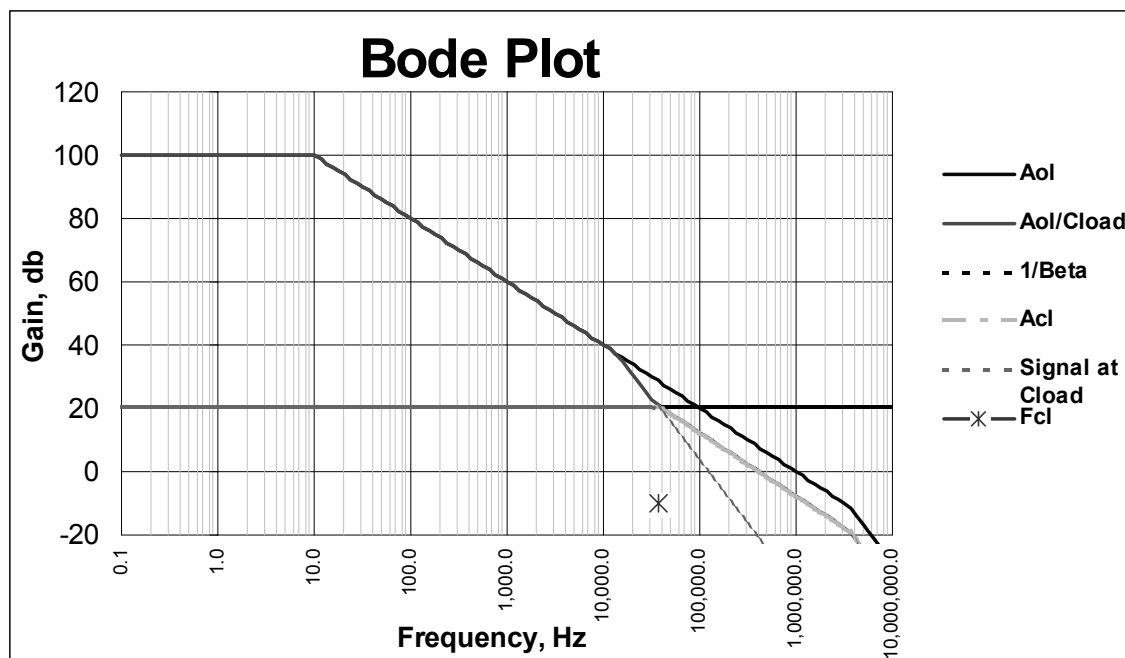
An important point one more time:

The closed loop curves here $1/\beta$ curves.

They are obviously related to signal gains but are stability analysis tools which always assume non-inverting gain. A signal gain of -1 will plot as 2 in $1/\beta$ format. The signal gain does not increase between 150Hz and 1.5KHz.

Ref. AN38

PA07/Cload Riso Solution

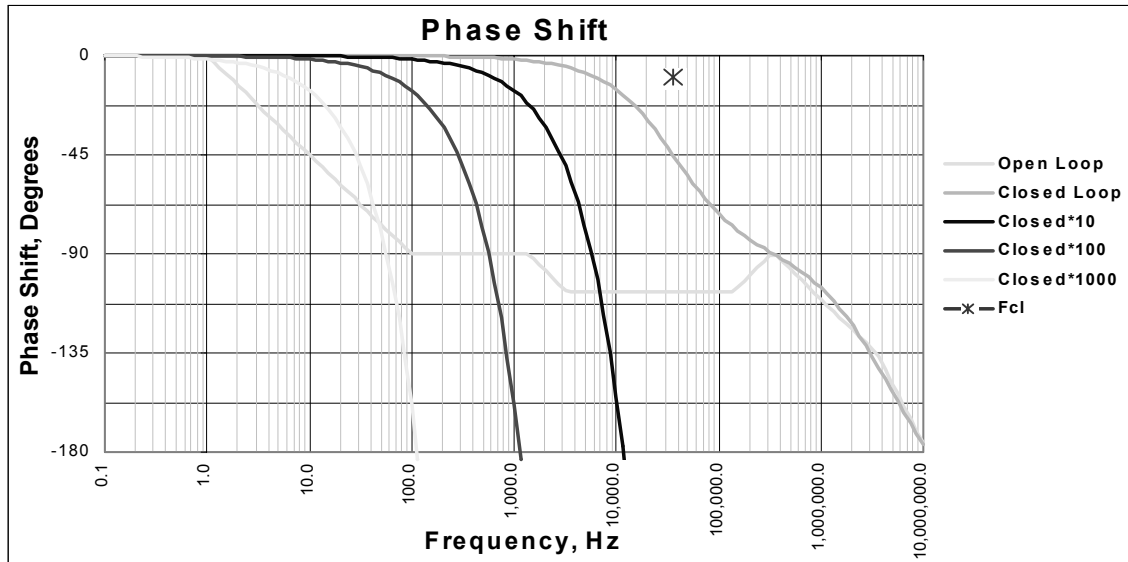


Notice the difference between the curve showing the Signal at Cload and the Acl curve. This is the voltage loss across Riso which is outside the feedback loop and therefore not corrected for amplitude loss. The picture says we really aren't losing much at usable frequencies. Let's look at another error between 10 kHz and closure frequency.

Op amp theory says output impedance is reduced by the loop gain. Our data entry screen told us Z_{out} for the PA07 was 5Ω . This graph tells us loop gain goes from 10 to zero in our band of interest. This means uncorrected output impedance goes from 0.5 to 5Ω in this band. The losses across the 1.2Ω Riso now seem even more trivial.

Ref. AN38

PA07/Cload Riso Phase

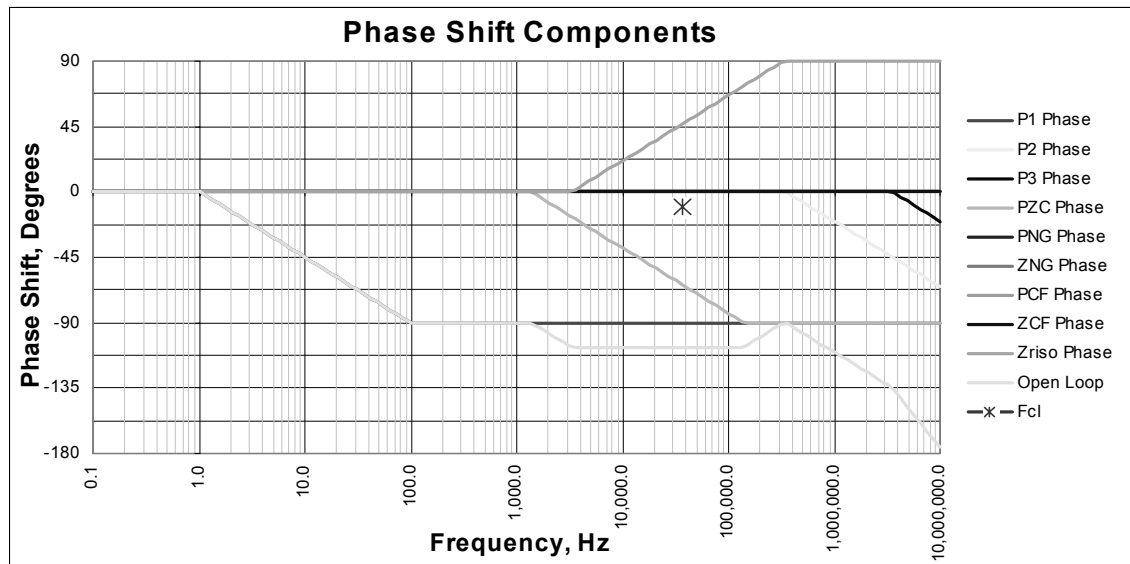


The first thing usually pulled from this graph is phase margin; 45° is good, 30° is pushing things. Here we see the open loop phase crossing Fcl (closure frequency) at 107¼° (Excel97 gives you the number if you place the cursor on the curve). Phase margin = 180° - open loop phase shift, or 72.75° in this case.

Sometimes we need to know the closed loop phase shift at a particular frequency. Suppose 1KHz is the point of interest. We can tell from the un-scaled curve this shift is not zero but resolution stinks. The curve with best resolution at 1KHz is the one scaled times 100. This curve crosses 1KHz at 158.66° for an open loop phase of about 1.6°.

Ref. AN38

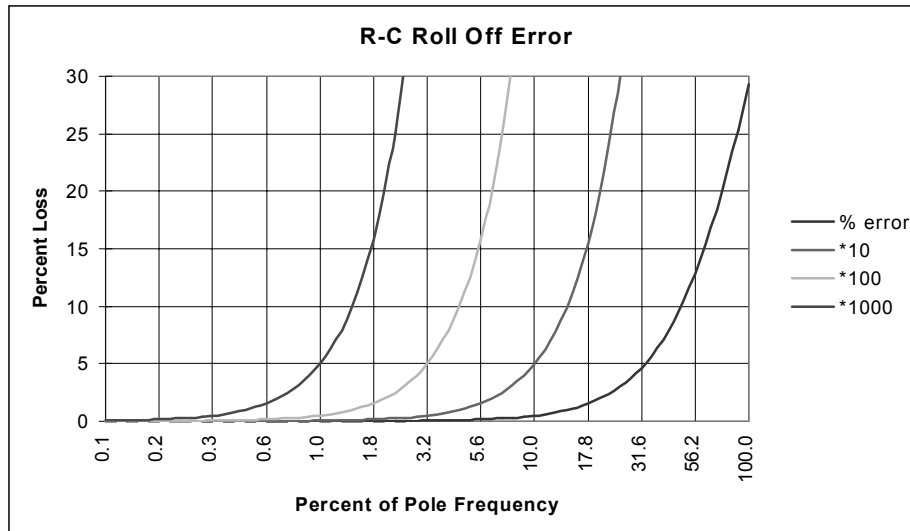
PA07/Cload Riso Phase Components



Here are all the pieces making up the total open loop phase shift. Each segment is based on component values and the plotting rules detailed in Application Notes 19 and 25. P1 Phase (first pole in the bode plot) appears to be missing. Power Design shows only one curve when two or more coincide. Notice that P1 Phase does show up roughly between 1KHz and 100KHz. Open loop Phase is simply the sum of all the segments. Some segments show only partially or not at all because they are off scale, usually because of the *open* values entered.

Ref. AN38

Errors of Straight Lines



Straight line approximation is a great way to visualize location of corner frequencies but information is lost about attenuation near the corner. In db terms, the errors are small numbers and most circuits have enough frequency margin such that we see no problems.

In more exacting circuits, this graph indicates about 30% low amplitude right at the corner frequency, a 10.6% error at half the corner frequency, 3% at one-quarter, and so on.

These errors apply to both the use of an isolation resistor and to a roll-off capacitor in the feedback loop.

Ref. AN38

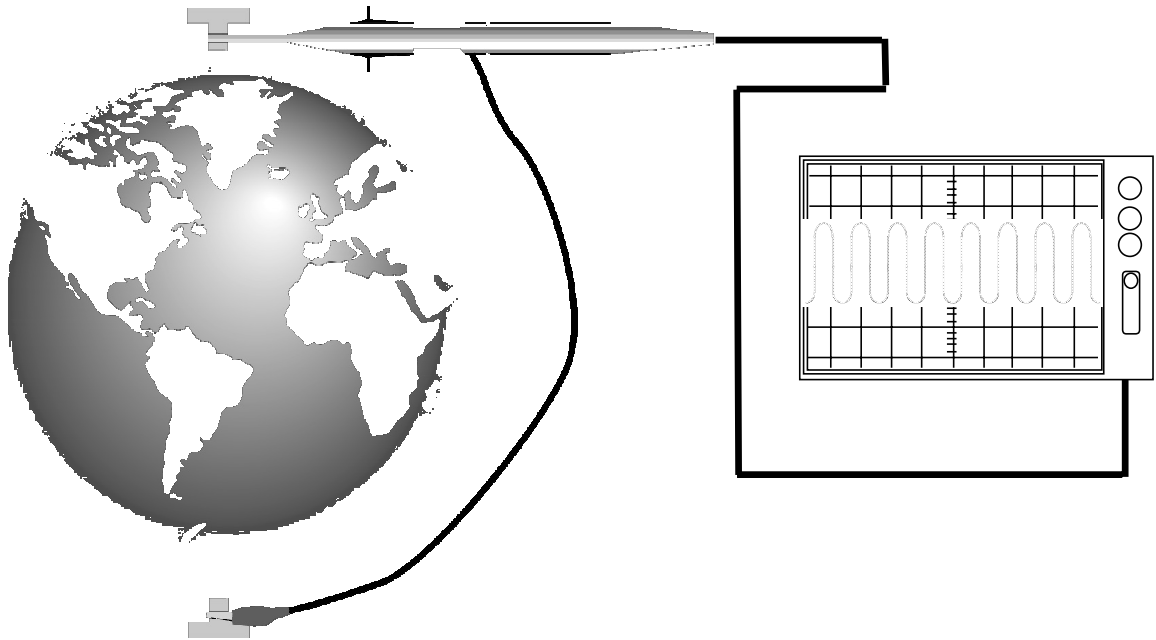
STABILITY TROUBLESHOOTING GUIDE

fosc (Oscillation Frequency)	Oscillates unloaded?			
	Oscillates with Vin = 0			
	Loop check† fixes oscillation?			
Probable Cause (In order of probability)				
CLBW ≤ fosc ≤ UGBW	N	Y	N	A,C,D,B
CLBW ≤ fosc ≤ UGBW	Y	Y	Y	K,E,F,J
CLBW ≤ fosc ≤ UGBW	-	N	Y	G
fosc ≤ CLBW	N	Y	Y	D
fosc = UGBW	Y	Y	N*	J,C
fosc << UGBW	Y	Y	N	L,C
fosc > UGBW	N	Y	N	B,A
fosc ≤ UGBW	N	N**	N	A,B,I,H

Previous sections have covered the major stability issues for more details and further explanation to use the Stability Troubleshooting Guide, refer to Application Note 1 in “General Operating Considerations” in the APEX Data Book.

Ref. AN1 STABILITY

REAL WORLD STABILITY TESTS

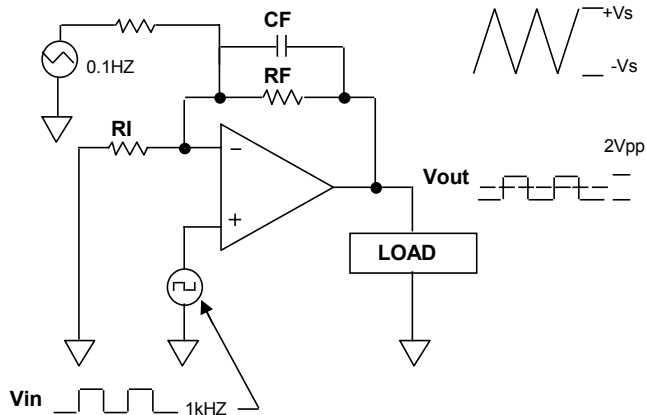


We have devoted much text to discussing and learning how to design stable circuits. Once a circuit is designed and built it is often difficult to open the feedback path in the real world and measure open loop phase margin for stability.

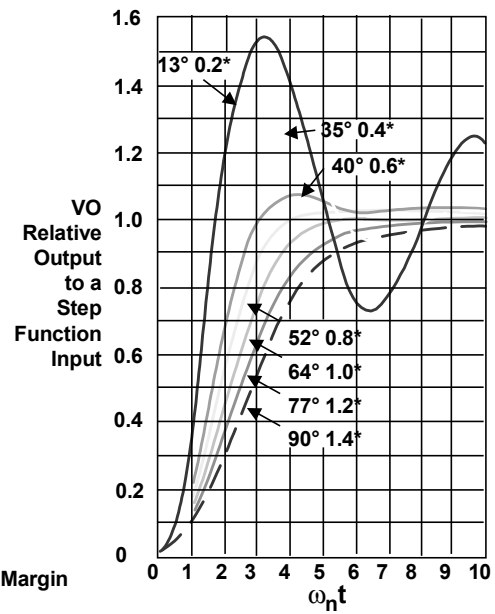
The following Real World Stability Tests offer methods to verify if predicted open loop phase margins actually make it to the real world implementation of the design. Although the curves shown for these tests are only exact for a second order system, they provide a good source of data since most power op amp circuits possess a dominant pair of poles that will be the controlling factor in system response.

When performing these tests, use actual production hardware. Supplies, harnesses, mechanical loads, fluid load and others all make a difference. The time spent here may save days of troubleshooting 6 months after the design is in production.

SQUARE WAVE TEST

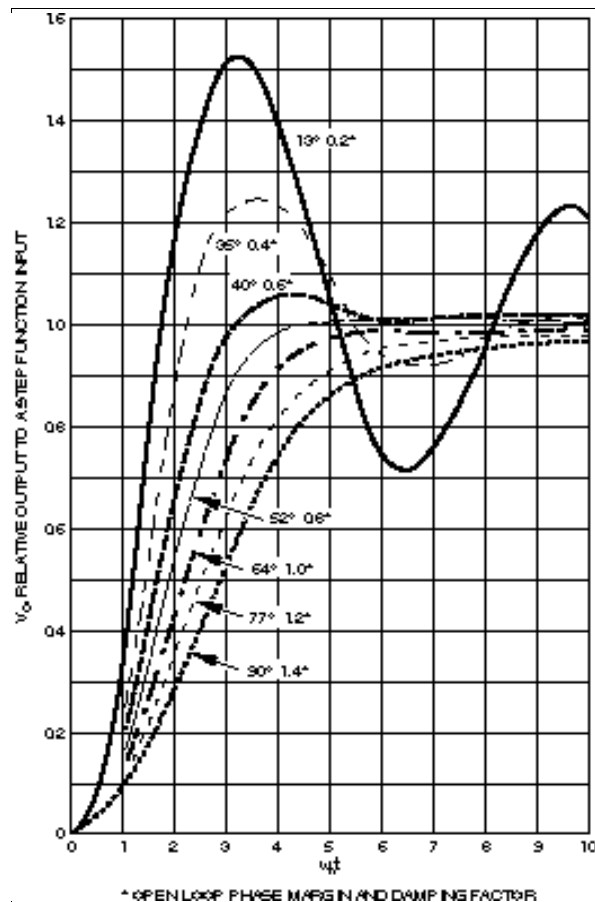


SQUARE WAVE TEST



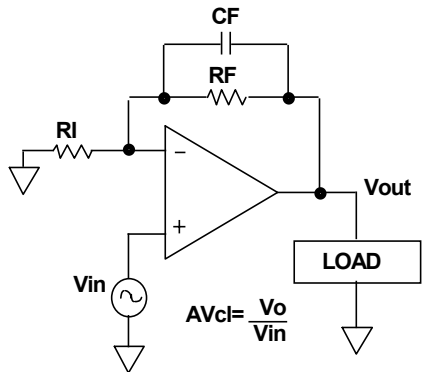
* Open Loop Phase Margin & Damping Factor

Ref. AN19

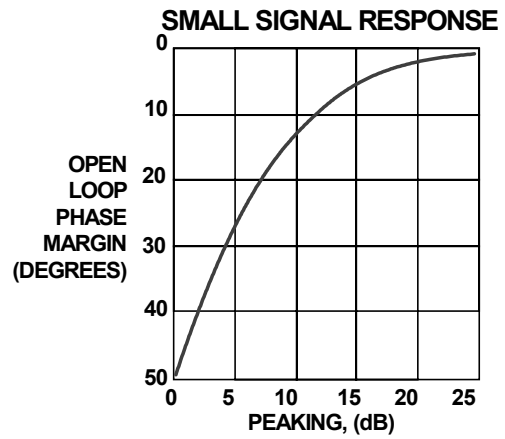


* OPEN LOOP PHASE MARGIN AND DAMPING FACTOR

AVcl PEAKING TEST



PEAKING-MEASURED CLOSED LOOP



AVcl(dB) Peaking

We are often asked to generate data resembling this test. Why not look up the graph and translate to degrees of phase margin?

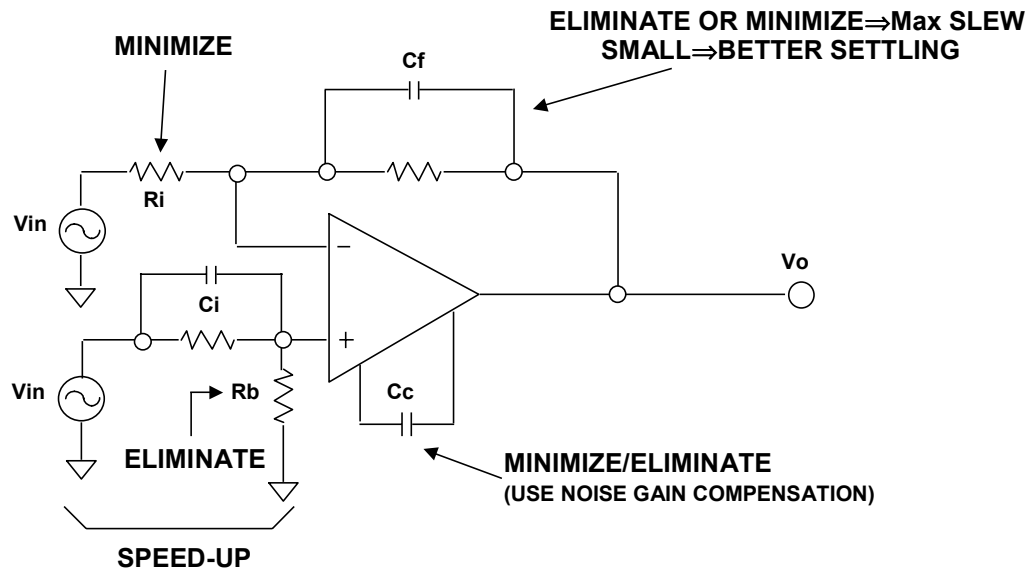
Ref. AN19

HIGH SPEED TECHNIQUES OPTIMIZING FOR SPEED

- Minimize Impedances
- Minimize Compensation Capacitance
- Minimize Integration Capacitance (C_f)
- Optimize Small Signal and Large Signal Bandwidths
- Trade-off:
 - Slew Rate
 - Settling Time

Maximum high speed performance with stability is achieved through the use of good high speed techniques and an understanding of the trade-offs involved between the various high speed requirements. For instance, small signal and large signal bandwidth requirements are not directly related and the designer must understand the trade-off between them.

Also, some high speed characteristics have conflicting requirements such as settling time and slew rate.



Ever try to buy 100K Ω coax cable? 100K Ω could simply not drive the parasitics. So, don't use that impedance trying to deliver input signals to the op amp.

C_f is a roll-off or slow down element. To achieve maximum slew rate get rid of C_f . Small values can be used to reduce overshoot and improve settling time.

The basic idea of this "Input Speed-up Network" is to provide a path for the higher frequency components of a step input to overdrive the input of the amplifier to get high slew rate. At high frequencies, the capacitor C_i is a short and the input drives the +input unattenuated. At low frequencies, such as the flat part of a step input, the resistor divider attenuates the signal to achieve the desired final gain for V_o/V_{in} .

The use of R_b to compensate bias current errors makes this pin an antenna or a low pass filter. Ground it.

Other ways to maximize high speed performance are to decrease the compensation capacitor C_c to maximize slew rate and to provide large enough drive input signal to cause at least a 1V-2V differential signal at the op amp input. If the amplifier is decompensated for slew rate, Noise Gain Compensation may be needed for stability. Most amplifier slew rates are specified using a 1V-2V input differential drive voltage into the amplifier. Adequate input signal amplitude will maximize slewing of the output.

Ref. AN17

SLEW RATE AND PBW

$$\text{S.R.} = \left[\frac{\Delta V_{\text{out}}}{\Delta t} \right]_{\text{max}} \quad [\text{V}/\mu\text{s}]$$

FOR PBW, SET:

$$\text{S.R.} = \frac{dV}{dt} (V_p \sin 2\pi f_t)_{\text{max}} \quad [\text{SINUSOIDS}]$$

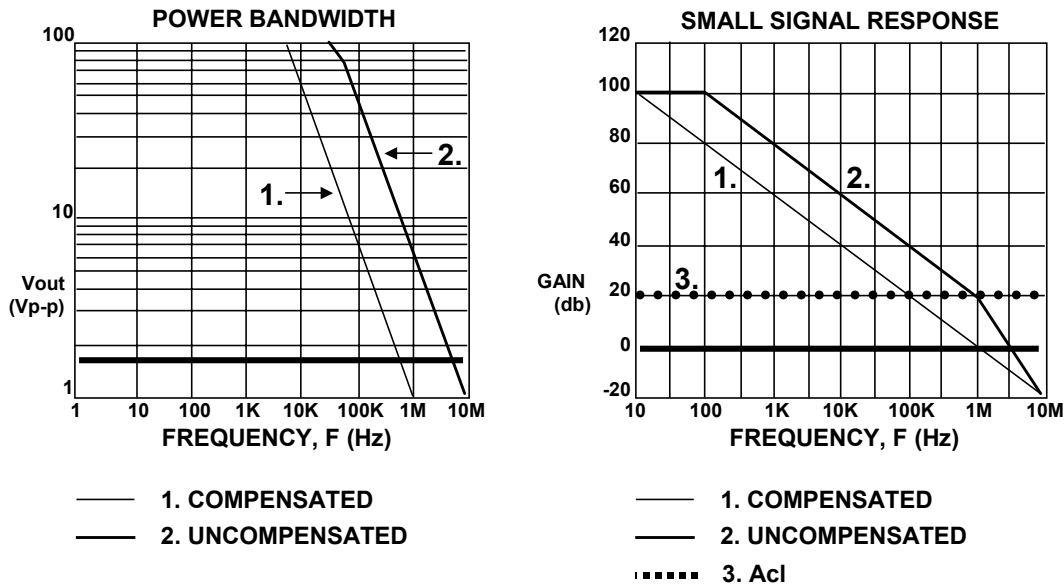
$$\text{S.R.} = 2\pi (\text{PBW}) V_p \quad [\text{SINUSOIDS}]$$

$$\text{PBW} = \frac{\text{SR}}{2\pi V_p} \qquad \text{SR} = \text{PBW} \, 2\pi \, V_p$$

Op amps have a maximum rate of change of output voltage that is directly related to the input stage current and the compensation capacitance. The maximum dV/dt of a sine wave occurs as the output passes through zero. Setting the dV/dt max of the amplifier equal to the dV/dt of a sine wave gives a relationship between slew rate and full power bandwidth. The simplicity of this relationship is often complicated by the common practice of specifying slew rates under conditions of extreme overdrive. This overdrive results in operation deep within the non-linear region with apparent slew rates up to several times higher than the slew rate derived from the full power bandwidth formula above.

Full power bandwidth is a “large signal” parameter. It is not directly related to small signal bandwidth. It’s a good idea to also check loop gain for the specific application.

OPTIMIZE PBW AND SSBW



The trade offs between small signal performance and large signal performance are often misunderstood or misinterpreted. It helps to understand the differences between the two bandwidths.

On the right are the small signal response curves of a typical high speed amplifier with both uncompensated and compensated Aol curves shown. On the left is the large signal or “full power” response curve shown for both compensated and uncompensated conditions.

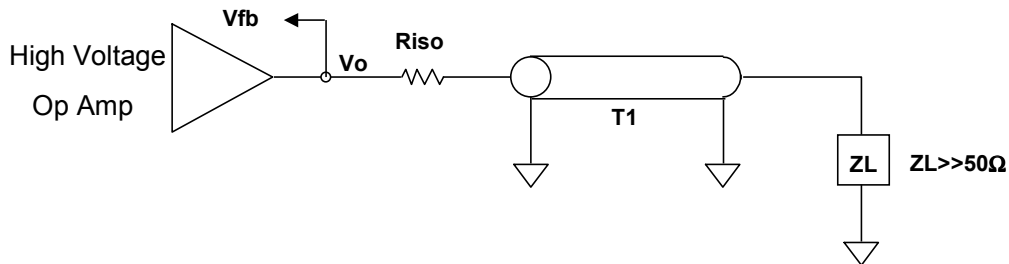
Note that the maximum useful small signal bandwidth of the amplifier is approximately 1MHz with or without compensation. The unity gain amplifier has a maximum bandwidth at unity gain of 1MHz, the uncompensated amplifier has more bandwidth but must be run at higher gains. Therefore its useful bandwidth is also limited to about 1MHz. The full power response curve may extend on up to 10MHz for low amplitude signals, however this power response is not achievable due to small signal bandwidth limits.

The best approach is to start with your maximum peak to peak output voltage requirements for sinusoids and find that peak to peak value on the Full Power Response Graph. Find the intersection of this line with the maximum output frequency required on the horizontal graph. The intersection of these two points will determine the maximum allowable compensation.

Consult the small signal response curve. For the compensation value chosen, find the minimum allowable closed loop gain. the intersection of Acl (min), with the AOL curve for that particular compensation value, gives the maximum useful small signal bandwidth.

Choosing the lowest possible compensation value combined with the lowest possible stable gain gives the maximum full power and small signal bandwidth combination. Keep in mind that larger loop gains give the best accuracy and lowest distortion.

CABLE LOADS



$$F \leq \frac{K(7.5 \times 10^6)}{L} \rightarrow T1 = CL$$

Where: L = length of cable

K = velocity factor

High voltage power op amps often drive their loads via coax and these are often not terminated in the characteristic impedance of the cable. This means the coax is primarily adding capacitive loading to the op amp unless the cable length is at least one-fortieth of wavelength at the frequency of interest.

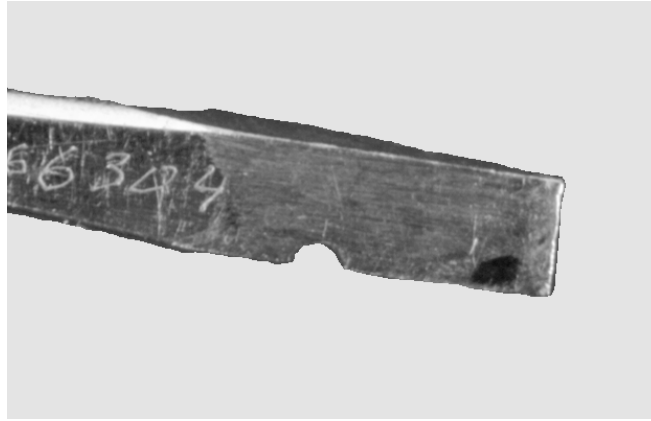
In the formula above, K is typically around .66 for common coax, the constant is simply the speed of light/40 in meters/second and L is in meters. As a benchmark, 10KHz corresponds to 1624 feet or 495 meters.

A ballpark value for the capacitive loading is 30pF/foot or 100pF/meter. As higher voltage op amps tend to have higher output impedances, they are more likely to have trouble with additional Cload and need compensation.

HIGH POWER TECHNIQUES

But, Mom...

You should've seen the other guy!



The number is part of the FBI crime lab evidence labeling program. It seems some digital jock said, "Electrons are electrons. I'll show those analog folks I can design a high power circuit just as well as they can."

The slide is right. The widow now keeps this screwdriver on the mantel in the living room.

Dead Op Amps Don't Power Much

Who, me? Read the book?

- AN1 General Operating Considerations
- AN8 Optimizing Output Power
- AN9 Current Limiting
- AN19 Power Op Amp Stability
- AN25 Driving Capacitive Loads

- Subject Index

We've heard of the male stereotype character who reads directions only as a matter of last resort. This anonymous author isn't much of a reader but after a few explosions, I broke down and opened the book- -the Apex book of course.

Better than 1/4 of the book is application notes, arranged mostly by type of application rather than amplifier model. This along with a comprehensive subject index make this book very valuable.

Here's my suggestion: Thumb through at least the Ap Notes above looking at pictures and paragraph titles. Then check out the index in the back.

Quiz for today: What is the Apex *Cage Code*?

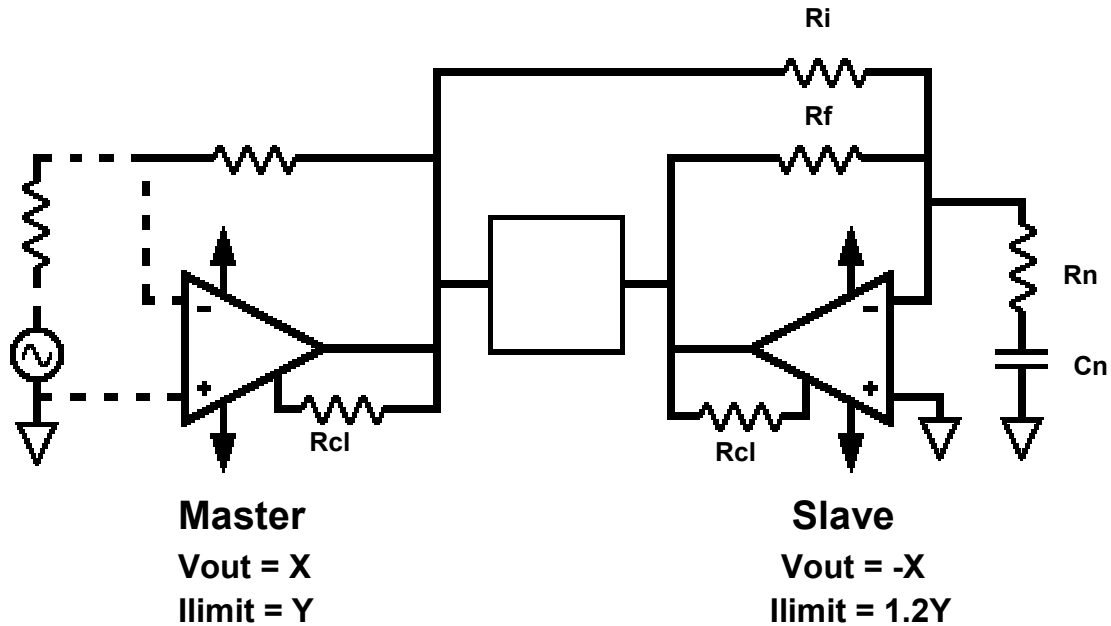
The Bridge Circuit

- Double the voltage swing
- Double the slew rate
- Double the power

- Bipolar drive on a single supply
- More efficient use of supplies

There are two basic categories of motivation to use the bridge circuit. The most common is doubling the voltage capability of the whole line of power op amps. The second category solves some limited supply availability situations.

Bridge Basics



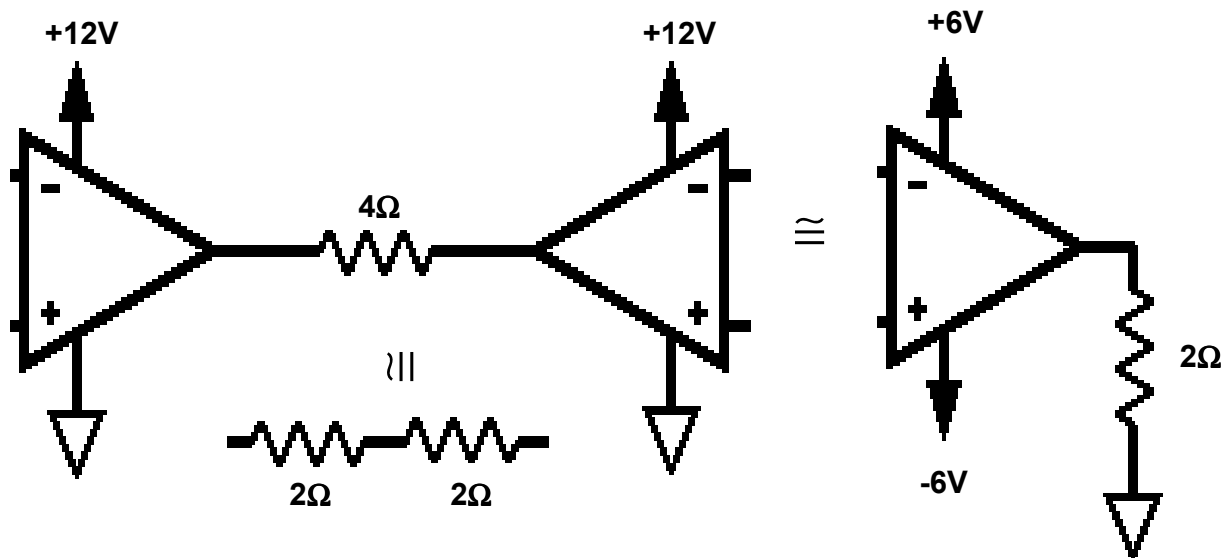
The master amplifier in the bridge may be configured in any manner suitable for a single version of the particular model. Set gain of the slave for $\frac{1}{2}$ the total required to drive the load. The slave provides the other half of the gain by inverting the output of the master and driving the opposite terminal of the load. Dual supply operation is the easiest but asymmetric or single supply versions are also common.

The R-C network is often used to fool the slave amplifier into believing it is running at the same gain as the master. This is important when using externally compensated amplifiers at other than their lowest bandwidth compensation. Set R_n for $R_{in} || R_n = R_f / \text{gain of the master}$. Set C_n for a corner frequency with R_n at least $1\frac{1}{2}$ decades below unity gain bandwidth.

Consider a shorted load. Tolerances make it impossible to set identical current limits on the master and the slave; one will go into current limit, the other will never reach the limiting level. Assume the master limits and the slave reduces its drive to the load also because it is still in a linear inverting mode. With both amplifier outputs going toward zero, power dissipations are equal and worst case is $I_{limit} * \frac{1}{2}$ total supply.

If the slave limits first, the master remains linear and capable of driving to either rail leaving a power stress on the slave of $I_{limit} * \text{total supply}$.

BRIDGE POWER CALCULATION



There are several formulae available for calculating worst case power dissipation in a power amplifier (refer to APEX catalog “General Operating Considerations” as well as previous seminar text). These formulae are based on a single power op amp using bipolar, symmetrical supplies. But what about this single supply bridge?

Instead of attempting algebraic manipulation of the formulas, try using *circuit algebra*. Knowing the master and slave drive equally but in opposite directions tells us the ohmic center of the load does not move. This leads to an equivalent two resistor load where the center voltage can be calculated. When using dual symmetric supplies the center is almost always ground and we have an equivalent circuit right away.

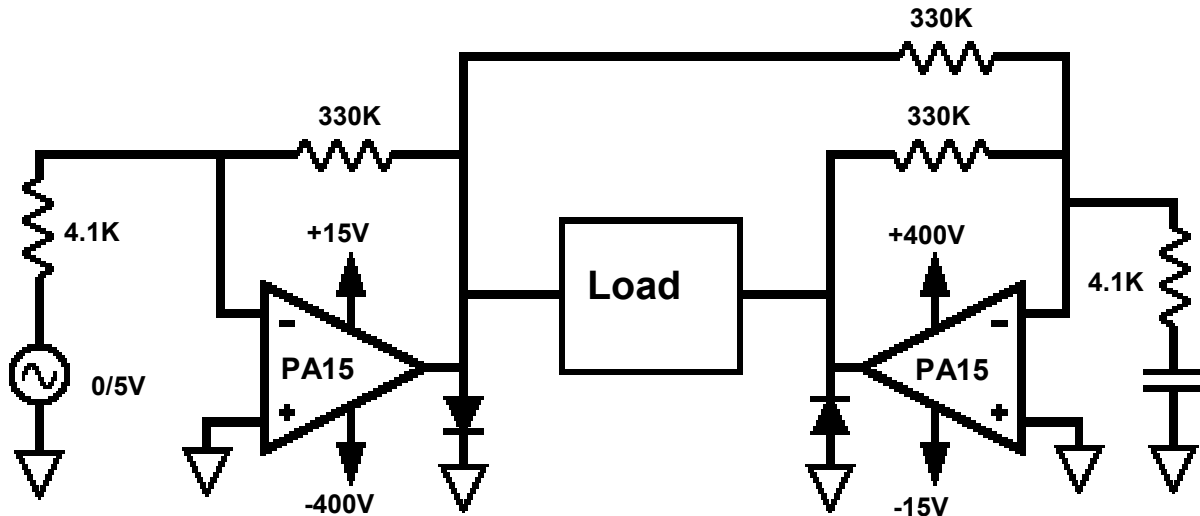
For the single supply the center of the equivalent load is almost always the mid-point of the supply. Simply lowering all voltages by the load center voltage yields the same equivalent circuit. Simply calculate power dissipation of the equivalent and don't forget to double this figure.

If you are using Power Design you will need the voltage translation portion of this exercise, but not the equivalent load. Enter the total load, total signal level and “Yes” in the bridge question yellow cell.

Ref. AN37

A Weird & Dangerous Bridge

0/800V Unipolar Output



No, this is not the most common bridge circuit. But consider that the only other choice above 450V total supply is the PA89 which is quite slow and costs about \$200 more than two PA15 amplifiers (both @ 100 quantity).

Dangerous? Any 800V circuit qualifies for this description but from the op amp point of view this one is a little more so because there are voltages in the area greater than his supply rails.

The left hand op amp swings 0 to -400V; the right hand from 0 to +400V. With the load looking at these two voltages differentially it sees 0/800V.

Consider a shorted load causing the right hand amplifier to current limit. If the left amplifier ever goes below -15V, he can destroy his partner. The diodes prevent this.

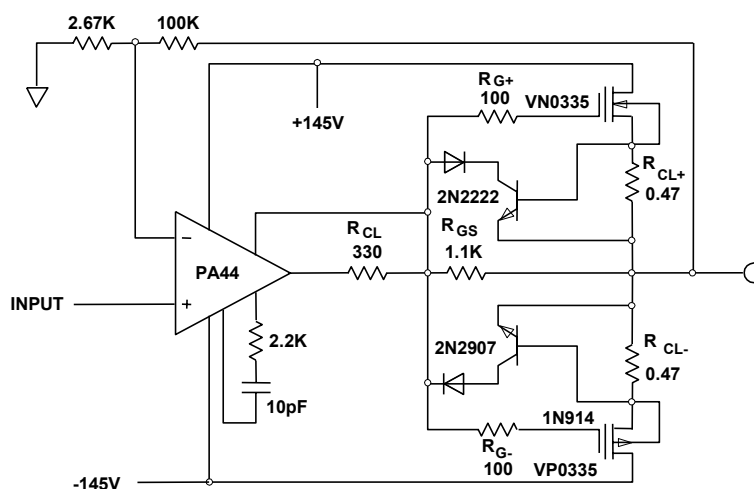
Ref. AN20 UNIPOLAR OUTPUT

Output Current Buffers

- Multiplies power & current capabilities
- Small loss of swing capability
- More prone to oscillate

Class C Current Buffer

Speed Limit Strictly Enforced



No FET bias = No chance for thermal runaway

The choice of specific MOSFETs is determined entirely by current, voltage and power dissipation requirements. There are no radical differences among the different MOSFETs regarding threshold voltages or transconductance. Note that each MOSFET must be rated to handle the total supply voltage, 300V in this case.

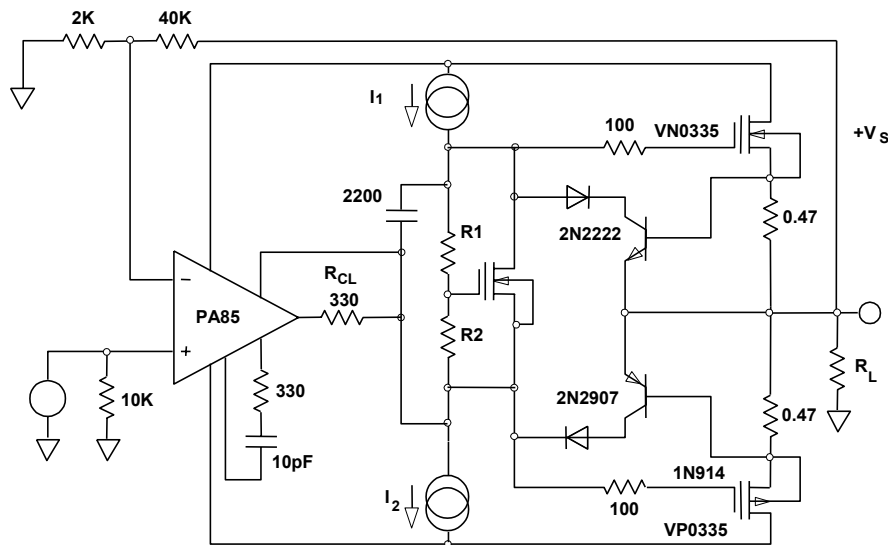
Current limits work like the circuits we covered earlier. Power dissipation requirements for the MOSFETs can also be found with methods we learned earlier, just remember the power is split between the two packages if the signal is AC only. Power Design will calculate the watts, plug in the driver amplifier, the real load and ignore the red flags.

The 330Ω current limit resistor sets the PA44 current limit to approximately 9mA. This current flowing across R_{GS} limits drive voltage on the MOSFETs to 10V. This current also lowers crossover distortion. Worst case (during output stage current limit) power dissipation in the PA44 will then be 1.3W due to output current plus 0.6W due to quiescent current totaling 1.9W. Unless you are willing to cut holes in the PC board to contact the bottom of the surface mount package with an air or liquid cooling system, this is about the limit. Typical operation will generate less than 1W in the op amp. Replacing R_{GS} with a 10 to 12V bi-directional zener will allow a cooler running op amp at the cost of increased distortion.

If more power is required than a single pair of MOSFETs can handle, additional MOSFETs may be added in parallel. Each device needs its own source resistor and gate resistor but the small signal current limit transistor and diode need not be duplicated.

Ref. *Use High-Voltage Op Amps to Drive Power MOSFETs*, by Jerry Steele and Dennis Eddlemon, *Electronic Design*, June 24, 1993.

COMPLIMENTARY MOSFET BUFFERS



The class C circuit was able use a simplified version of this slide with no attempt to establish class A/B bias in the MOSFET output stage. In that circuit with no bias, the typical MOSFET threshold of 3V means the op amp must swing 6V during the crossover transition while the final output does not move. The additional circuitry used here will lower distortion and is increasingly important as frequency goes up. Distortion improvements better than an order of magnitude have been achieved.

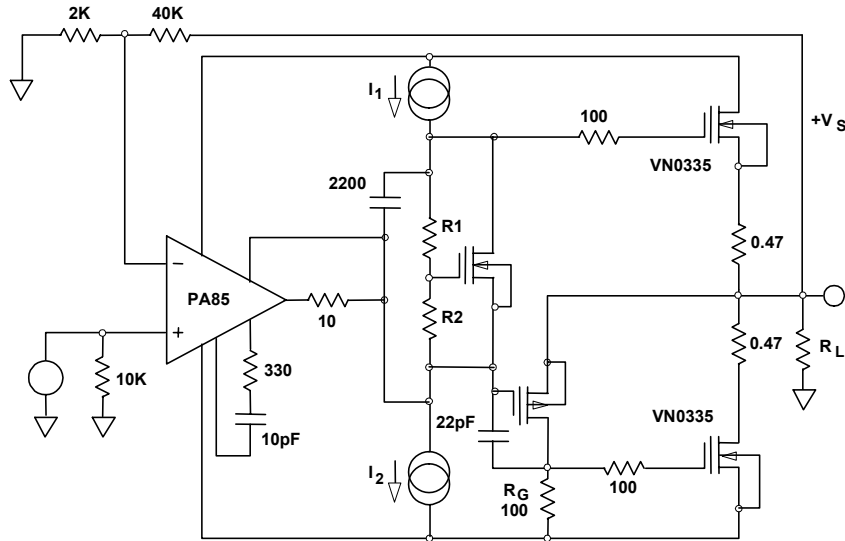
As most power MOSFET data sheets provide little data on VGS variations at low currents over temperature, it facilitates the design process to have curve tracer data over the temperature range of interest. Design the VGS multiplier empirically. Current sources of 5mA and splitting the current equally between the resistors and the MOSFET area good starting points. Decreasing current in the MOSFET will increase the multiplier TC. Typical designs requiring low distortion will be set up to obtain 2mA or less bias in the output stage. The trade offs are more distortion with low current and danger of thermal runaway on the high end. Be absolutely sure to guardband your high end temperature. The circuit shown here is capable of distortion below .05% at 50KHz and is thermally stable (flat or negative TC of current in the output stage) over the range of -25° to 85°C.

Note that any multiplier voltage at all reduces distortion. Successful designs have even reduced the multiplier circuit to just a diode connected MOSFET. Do NOT use bipolar transistors or diodes for this biasing. Their TCs do not match those of the MOSFETs.

The 100Ω gate resistors prevent local output stage oscillations. It is important they be physically close to the MOSFETs.

Ref. *Use High-Voltage Op Amps to Drive Power MOSFETs*, by Jerry Steele and Dennis Eddlemon, Electronic Design, June 24, 1993.

QUASI-COMPLIMENTARY MOSFET BUFFERS



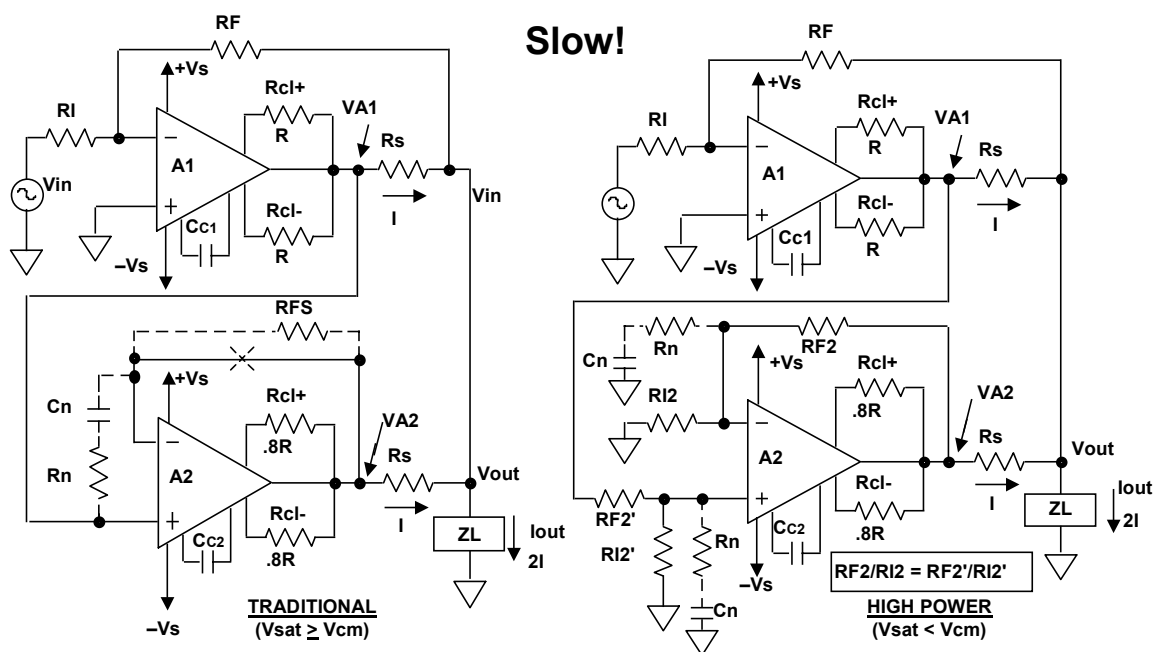
Above 300V p-channel high power MOSFETs can be difficult to find. An alternative is to use a quasi-complementary connection on the negative side. Since the required gate drive voltage of the output device appears across R_G , its value will set the maximum current through the p-channel MOSFET. Typical maximum gate drive requirements are 10V. This circuit has demonstrated a slew rate of 360V/ μ s. A second disadvantage of the quasi-complementary design is higher saturation voltage to the negative rail because two gate-source voltages are stacked between the rail and the output.

Connecting the op amp to the top side of the multiplier helps a little but both buffer design approaches can benefit from having the high voltage op amp operate on higher supply rails than the high power MOSFETs. This improves efficiency by allowing better saturation of the buffers.

Design criteria for the current sources, current limiters (not shown here) and multiplier are the same as with the complementary version. It is possible to omit one of the current sources in these circuits. However, this places an added heat burden on the high voltage op amp because the entire current of the remaining source must flow through it. When calculating this added dissipation, use the current and the total supply voltage. When both current sources are used the op amp need only make up the difference between them.

Ref. *Use High-Voltage Op Amps to Drive Power MOSFETs*, by Jerry Steele and Dennis Eddlemon, *Electronic Design*, June 24, 1993.

PARALLEL OPERATION



GENERAL COMMENTS:

Occasionally it is desired to extend the SOA of a power op amp or provide higher currents to a load than the amplifier is capable of delivering on its own. Sometimes it is more cost effective to use power op amps in parallel rather than to select a larger power op amp.

The parallel power op amp circuit will consist of a master amplifier, A1, which sets the V_{out}/V_{in} gain and slave amplifiers, A2 et al, which act as unity gain followers from the master amplifier. For simplicity we will review the case of two power op amps in parallel.

We will need to consider the following key areas when paralleling power op amps:

- 1) Input offset voltage
- 2) Slew rate
- 3) Phase compensation
- 4) Current limit resistors

If we attempt to hook the outputs of two power op amps directly together the difference in input offset voltages, divided by theoretically zero ohms (a connecting wire), will cause huge circulating currents between the amplifiers, which will lead to rapid destruction. To minimize circulating currents we will need to add ballast resistors, R_s , as shown. The worst case circulating currents now are $I_{circ} = V_{os}/2R_s$. To minimize circulating currents we want R_s to be as large as possible. However, large values of R_s will add an additional voltage drop from the power supply rails and thereby reduce output voltage swing. Large values of R_s will also result in higher power dissipations. A rule of thumb compromise is to set R_s for circulating currents of about 1% of the maximum output current from each amplifier, .01I in our example.

Ref. AN26

GENERAL COMMENTS (cont.):

Notice the particular arrangement of the master and slave amplifiers. $V_{A1} = I R_s + V_{out}$. However the point of feedback for A1 is at V_{out} causing A1 to control the gain for V_{out}/V_{in} . V_{A1} then becomes the input to A2. V_{A2} is then $V_{out} + I R_s$. But $V_{out} = V_{A1} - I R_s$. So each amplifier, A1 and A2, put out the same voltage across R_s and Z_L and currents are thereby added to force $2I$ through the load with each amplifier providing one-half of the total.

The slew rates of A1 and A2 must be selected to be the same or A1 must be compensated for a lower slew rate. If A1 slews faster than A2, large circulating currents will result since A1 could be close to $+V_s$ while A2 is still at zero output or worse near $-V_s$. C_{c1} and C_{c2} must then be selected to be the same or C_{c1} greater than C_{c2} . Even with these steps for slew rate matching it is recommended to control the slew rate of V_{in} such that the amplifiers are not commanded to slew any faster than 50% – 75% of the selected slew rates. This is because, even with identical compensation, no two amplifiers will have identical slew rates.

If it is decided to have A2 not compensated for unity gain, to utilize a higher slew rate, use Noise Gain Compensation, shown by the dashed RFS and R_n , C_n combination, to compensate the amplifier for AC small signal stability.

Current limit resistors, R_{cl+} and R_{cl-} for A2 should be 20% lower in value than current limit resistors for A1. This is to equalize SOA stresses during a fault condition. With the master amplifier, A1, going into current limit first it will lower its output voltage thereby commanding A2 to do the same for equal sharing of stresses during a current limit induced condition.

TRADITIONAL ($V_{sat} \geq V_{cm}$):

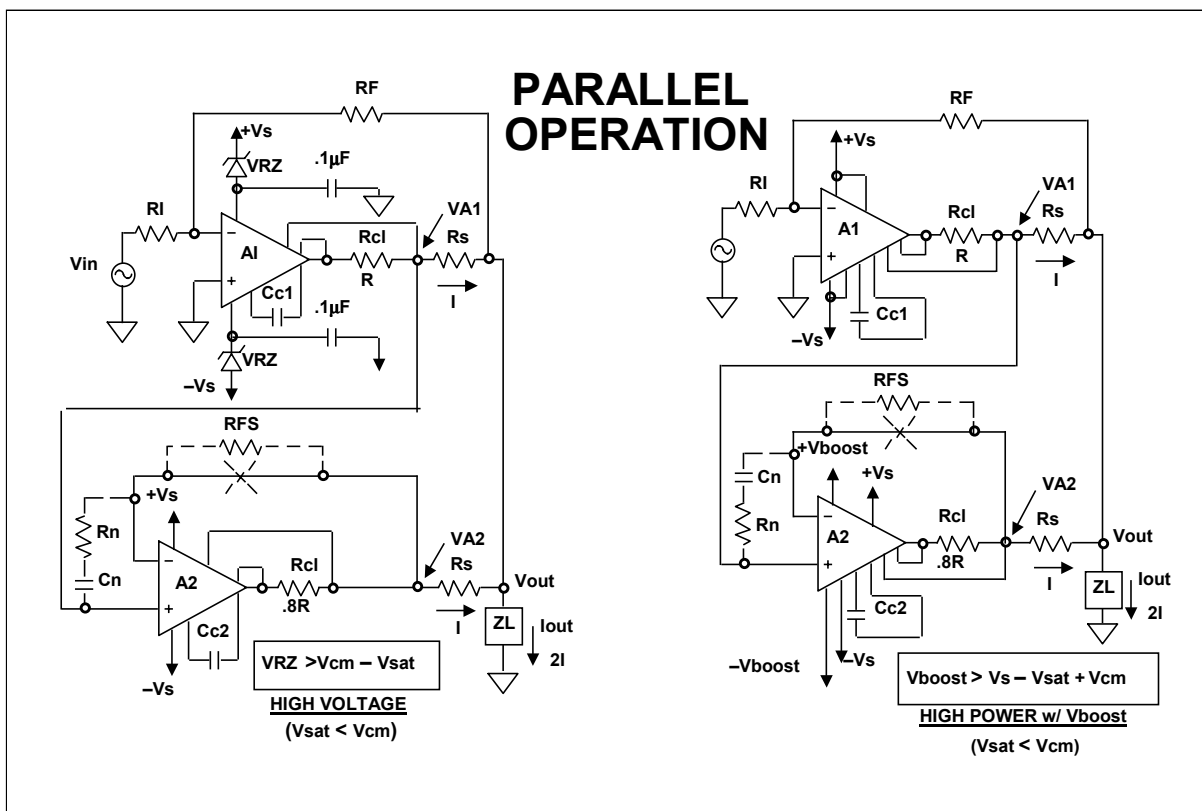
This parallel configuration is for op amps whose saturation voltage is greater than or equal to their common mode voltage ($V_{sat} \geq V_{cm}$). For example, a PA10 has a common mode voltage specification of $\pm V_s - 5$ and a saturation voltage of $\pm V_s - 5$. For the PA10 the output saturation voltage (5V) is equal to the common mode voltage (5V from either rail). We will not have any common mode voltage violation then if we drive the output of A1 into saturation as we will still be in compliance with the input common mode voltage specification for A2.

HIGH POWER ($V_{sat} < V_{cm}$):

This parallel configuration is for amplifiers whose currents are greater than 200mA and whose saturation voltage is less than their common mode voltage ($V_{sat} < V_{cm}$).

For example, a PA02 has a common mode voltage specification of $\pm V_s - 6$ and a saturation voltage of $\pm V_s - 2$. For the PA02 the output saturation voltage (2V) is less than the common mode voltage (6V from either rail). If we drive the output of A1 directly into A2 in a unity gain voltage follower configuration we will have a common mode voltage violation.

The only way around this is to use a matched resistor network where the ratio of $R_{F2}/R_{I2} = R_{F2'}/R_{I2'}$. The absolute value of each resistor is not as important as accurate ratio matching with temperature. If A1 and A2 are compensatable amplifiers and unity gain compensation is not desired, to use faster slew rates, then A1 can use noise gain compensation to guarantee AC small signal stability. R_n and C_n are our traditional Noise Gain Compensation components. $R_{n'}$ and $C_{n'}$ are essential to guarantee a flat V_{out}/V_{in} frequency response until we run out of loop gain.



All our previous “GENERAL COMMENTS” on the use of parallel power op amp circuits still apply to these configurations. Additional specific comments on each follows.

HIGH VOLTAGE ($V_{sat} < V_{cm}$):

This parallel configuration is for amplifiers whose currents are less than 200mA and whose saturation voltage is less their common mode voltage ($V_{sat} < V_{cm}$). In the APEX amplifier line this will almost always be high voltage ($\pm V_s > 75V$).

For example a PA85 has a common mode voltage of $\pm V_s - 12$ and a saturation voltage of $\pm V_s - 5.5$ at light loads. For the PA85 the output saturation voltage (5.5V) is less than the common mode voltage (12V from either rail). If we try to drive A2 as a unity gain voltage follower directly from A1 we will have a common mode voltage violation. That is, unless we lower the supply voltage of A1 by about 6.5V, which we can do easily with a zener diode in each supply line of A1. For 200mA output current plus 25mA quiescent current would require at least a 2W, 6.8V zener in each supply rail. The obvious loss with this technique is output voltage swing from the rail, now limited to V_{sat} of 5.5 Volts plus VRZ drop of 6.8 volts for a total of 12.3V, at light loads.

HIGH POWER w/Vboost($V_{sat} < V_{cm}$):

This parallel configuration is for amplifiers such as the PA04 or PA05 that are high output current and whose saturation voltage is less than their common mode voltage ($V_{sat} < V_{cm}$).

For example a PA05 has a common mode voltage of $\pm V_s - 8$ and a saturation voltage of $\pm V_s - 5.0$ at light load. If we try to drive A2 as a unity gain voltage follower directly from A1 we will have a common mode voltage violation. That is, unless we utilize the Vboost function of these power op amps on A2 to run the front end of A2 at a supply voltage which is at least 3 volts above its output voltage supply (V_s). This Vboost supply need only supply quiescent current for the device and can be generated by a switching floating regulator.

A less advantageous approach, which would reduce output voltage swing, is to utilize a zener diode in the Vboost supply of A1, similar to the “HIGH VOLTAGE($V_{sat} < V_{cm}$)” example above.

Ref. AN26

Watch the Slave Phase Shift

- PA85 Power Response Curve = 500KHz@400Vp-p
- Power Design suggests 86Khz for accuracy
- Power Design tells us phase shift is 7°@ 87KHz
- $\sin(7^\circ) = 0.122 * 200\text{Vpk} = 24.3\text{V}$
- This voltage appears across the two Rs resistors

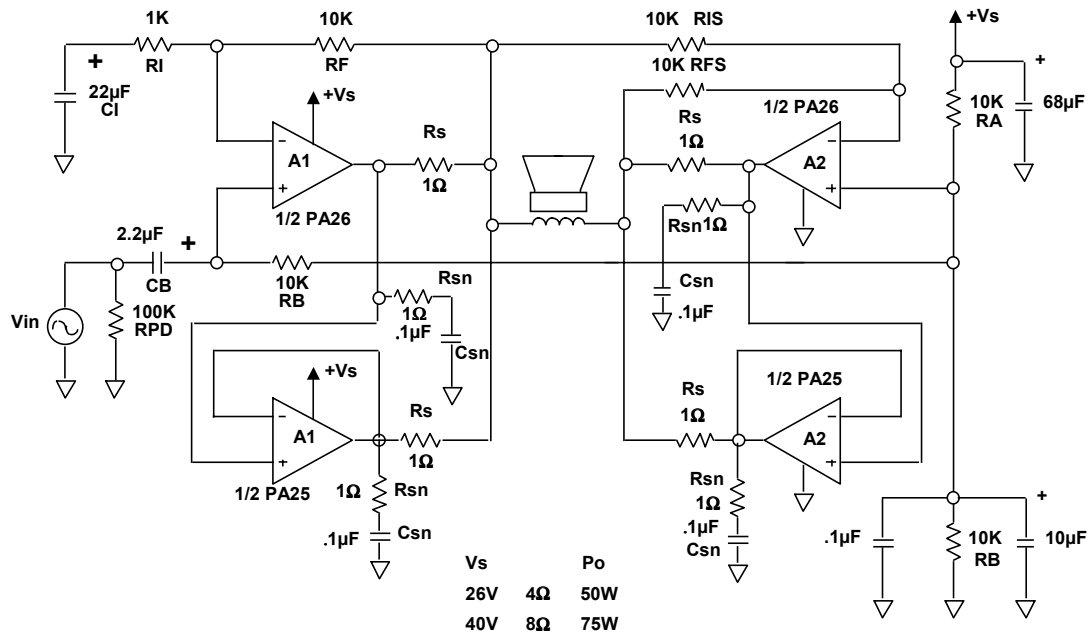
The power response graph says you can get to those points, however, you will usually need to increase the drive amplitude and you will probably just start seeing distortion. Another way to put it: these curves demand no loop gain and circuit accuracy is a function of the op amp rather than feedback components on the sloping portion of the power response curve (AC response limits rather than voltage saturation). The amplitude and distortion voltage errors of the slave appear across the two sharing resistors.

Phase phase shift grows as loop gain decreases. In the master of the parallel circuit this does no harm locally because the slave input includes the shift. However shift in the slave produces voltage applied across the sum of the two ballast resistors where circulating current becomes a concern.

The Cloud sheet of Power Design will calculate closed loop phase shift. The sine of this angle times peak voltage yields the error we are looking for.

Parallel power op amps is not a high speed technique.

SINGLE SUPPLY PARALLEL BRIDGE



This application utilizes two power op amp circuit tricks—single supply bridge mode to increase output peak-to-peak voltage and parallel power op amps to increase output current.

The PA26 is optimized for single supply operation with its wide input common mode voltage range and low saturation voltage. The parallel combination provides a dual advantage in that we can deliver higher output currents as well as reduce the output saturation voltage since each op amp need only supply one-half the total load current.

AC coupling of Vin provides level shifting of the input signal to swing symmetrically about $1/2V_s$. AC coupling through CI ensures the maximum DC offset across the load is only 20mV. RB provides a +input DC bias path for the front end of the master amplifier half of A1. Rsn and Csn networks are required on the output of each amplifier section of A1 and A2 to prevent oscillations on the output during negative swings. This is due to the type of output power stage inside the monolithic PA26. A2 is configured as a traditional inverting gain amplifier for single supply bridge mode and uses one half of itself for providing extra current as a slave amplifier in the parallel configuration.

With the PA26 at \$5US (1000) this is about 13 cents per watt. PA21 and PA25 offer hermetic packages at higher cost. Just imagine what you could do with PA03s in this circuit. Let's break the KW barrier!

Ref. AN20

Controlling Output Current

- Removes Z_{load} from the I_{out} equation
- Adds Z_{load} to the V_{out} equation

- Charge Rate control

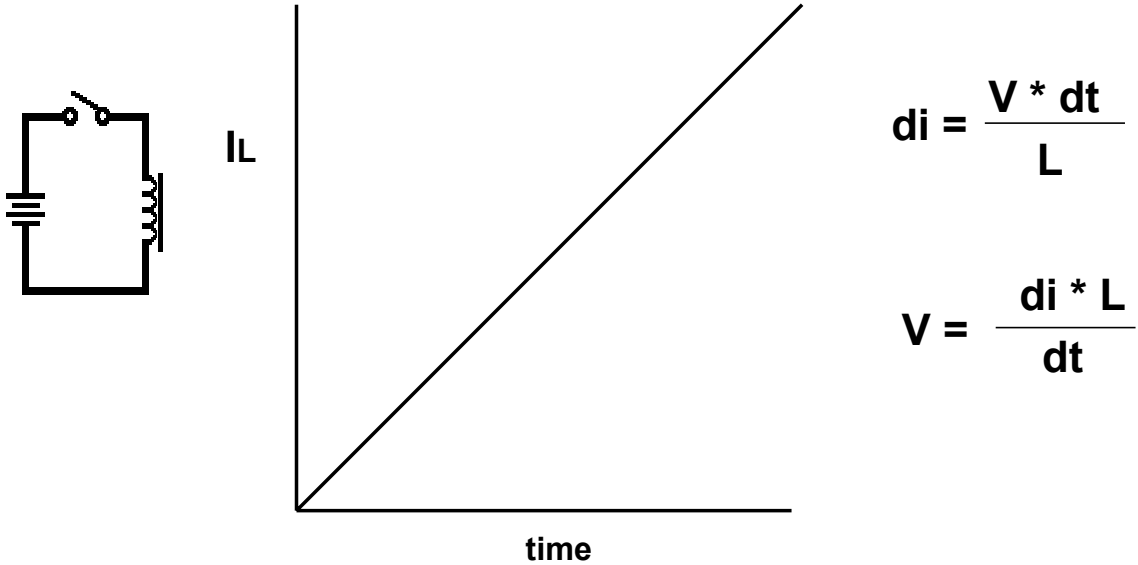
**Batteries, capacitor plate forming
power supply active loads, CD welder**

- Magnetic field intensity

**Bearings, deflection, MRI, torque, linear
or angular displacement**

Controlling current rather than voltage is much more common with power op amps than with small signal op amps. The current control world brings interesting applications plus some new techniques with their own equations and special points to watch.

1 Volt, 1 Henry, 1 second, 1 Amp



OK, so you've seen this before. It is central to current control.

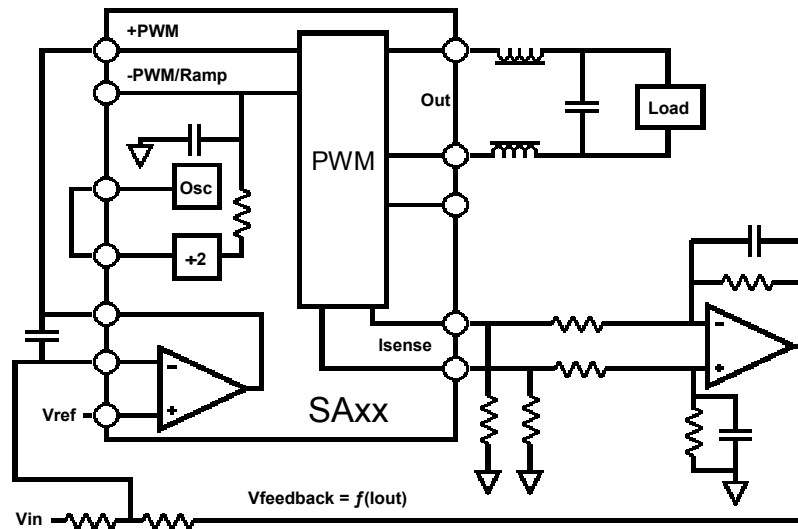
Changing current a lot, in a big inductor, in a hurry, takes lots of volts.

The corollary:

Stopping a big current, in a big inductor, in a hurry, generates lots of volts.

It may require more power than first glance says; opening a current carrying line may release all the stored energy in the form of fire.

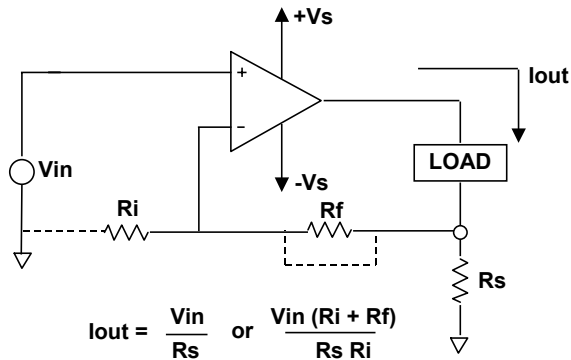
Basic PWM Current Output



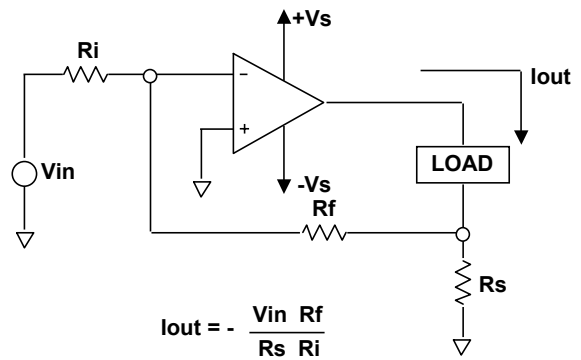
Most Apex PWM amplifiers offer two current sense pins. With the H-bridge output this means the current path changes sense pins each half cycle. Since alternating half cycles correspond to opposite directions of current flow in the load, a differential amplifier monitoring the two pins yields magnitude and direction data.

The integrator now compares the input and feedback voltages and moves its output as required to balance them. The two associated resistors allow easy magnitude scaling. Reference voltage is often used to elevate signals above ground to comply with op amp common mode voltage ranges. The reference voltage is also often used to level translation such as matching bipolar input signals to a single supply control system.

VOLTAGE-TO-CURRENT CONVERSION



**NON-INVERTING
CONFIGURATION**



**INVERTING
CONFIGURATION**

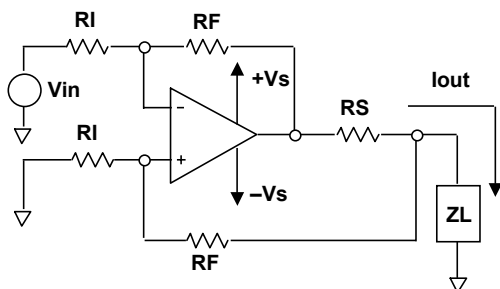
Two generic examples of voltage-to-current conversion for a floating load are shown here. The floating load circuit provides the best possible performance of any of the current output circuits with the tradeoff that the load must float.

In the basic non-inverting circuit R_i and R_f don't exist. Load current develops a proportional voltage in R_s which is fed back for comparison to applied input. As long as voltage across R_s is lower than the input voltage, the output voltage increases. In other words the op amp impresses the input voltage on the sense resistor. Adding the resistors allows increasing the transfer function. It is also common to have R_f without R_i providing an RC stabilizing network a reasonable impedance for its AC feedback signal.

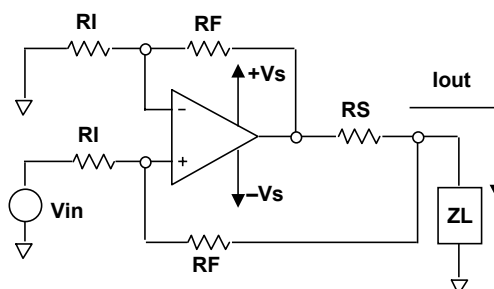
The inverting circuit works in the same manner other than polarity but does have the advantage of being able scale the transfer function up or down. This mean it is possible to have less voltage on the sense resistor than the input signal has.

Ref. AN13

VOLTAGE-TO-CURRENT CONVERSION IMPROVED HOWLAND CURRENT PUMP



$$I_{out} = -V_{in} \frac{R_F}{R_I R_S}$$



$$I_{out} = V_{in} \frac{R_F}{R_I R_S}$$

DOMINANT ERROR - MISMATCH OF R_I s AND R_F s

When a load must have one end of it ground referenced, voltage to current conversion circuits are still a possibility. The Improved Howland Current Pump provides a topology for V-I circuits driving a grounded load.

One way to view this circuit is to think of it as a differential amplifier circuit with a differential input and a differential output. V_{in} is gained up by the ratio of R_F/R_I and differentially impressed across R_S . I_{out} then is the voltage across R_S divided by R_S . Since we have a differential input as well, moving V_{in} to the opposite input reverse the relationship of I_{out} to V_{in} .

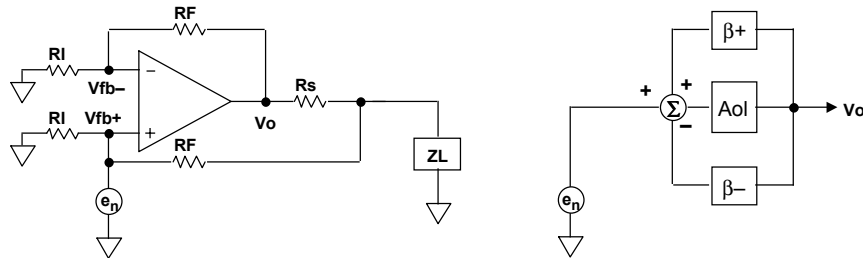
The dominant error in this topology is ratio matching of the R_F/R_I resistors. The ratio of R_F/R_I for the negative feedback path should closely match the ratio of R_F/R_I in the positive feedback path. Resistor networks with close ratio matching, where the absolute tolerance of the resistors may be as high as 10%, are required if high accuracy is desired.

The Improved Howland Current Pump offers a minimum component count ground referenced V-I circuit. In many systems accuracy of this V-I function is not critical. A typical circuit of this topology using 1% resistors may only have an overall I_{out}/V_{in} accuracy of 20% when output impedance, A_{ol} , offset voltage, and component accuracy are accounted for.

Our final consideration for the Improved Howland Current Pump will be AC stability analysis. The load itself is in the feedback path of the op amp for this circuit. Stability compensation will then be load dependent. We will look at stability in great detail in future pages.

Ref. AN13

IMPROVED HOWLAND CURRENT PUMP SMALL SIGNAL AC MODEL FOR STABILITY



$$\beta_+ = \frac{V_{fb}}{V_o}$$

$$\beta_- = \frac{R_i}{R_f + R_i}$$

$$\beta_+ = \frac{[Z_L || (R_f + R_i)] R_i}{[R_s + Z_L || (R_f + R_i)][R_f + R_i]}$$

$$\beta = \beta_- - \beta_+$$

$$V_o = A_{ol} (e_n + V_o \beta_+ - V_o \beta_-)$$

$$V_o - A_{ol} V_o \beta_+ + A_{ol} V_o \beta_- = e_n A_{ol}$$

$$\frac{V_o}{e_n} = \frac{A_{ol}}{-A_{ol} \beta_+ + A_{ol} \beta_-}$$

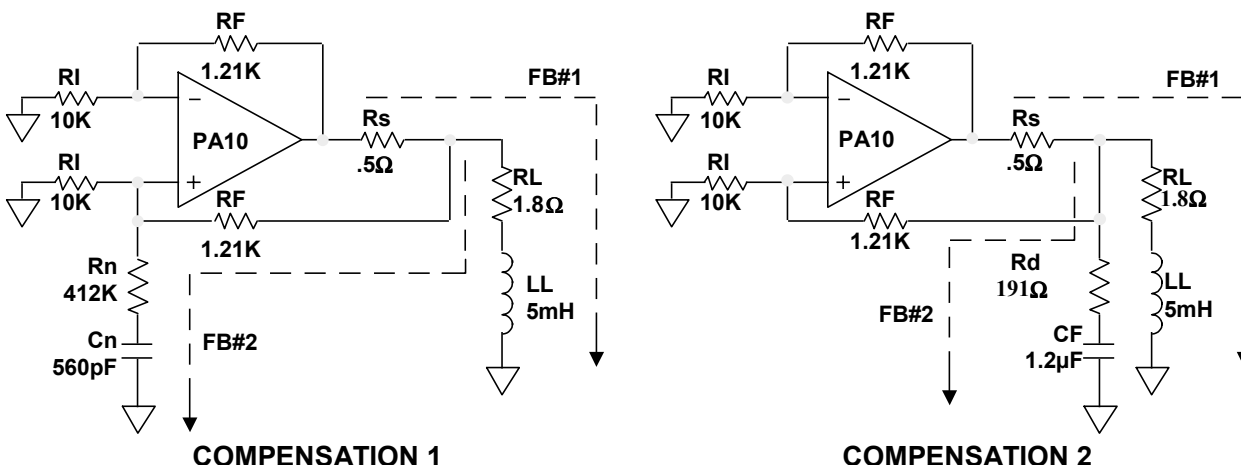
$$\frac{V_o}{e_n} = \frac{1}{\beta_- - \beta_+}$$

$$\beta = \beta_- - \beta_+$$

The figure on the left above shows a typical Improved Howland Current Pump circuit. Notice the additional e_n voltage source on the non-inverting input node of the op amp. For AC small signal stability analysis we do not know where the input signal can be injected. We choose to inject the AC input signal at the +input since this will result in the worst case stability situation. $1/\beta$ plots then will be a representation of V_o/e_n .

The figure on the right above is the equivalent control system block diagram from which we derive the powerful equation for β which will enable us to stabilize the Improved Howland Current Pump with the stability analysis techniques we have previously covered.

IMPROVED HOWLAND CURRENT PUMP AC STABILITY



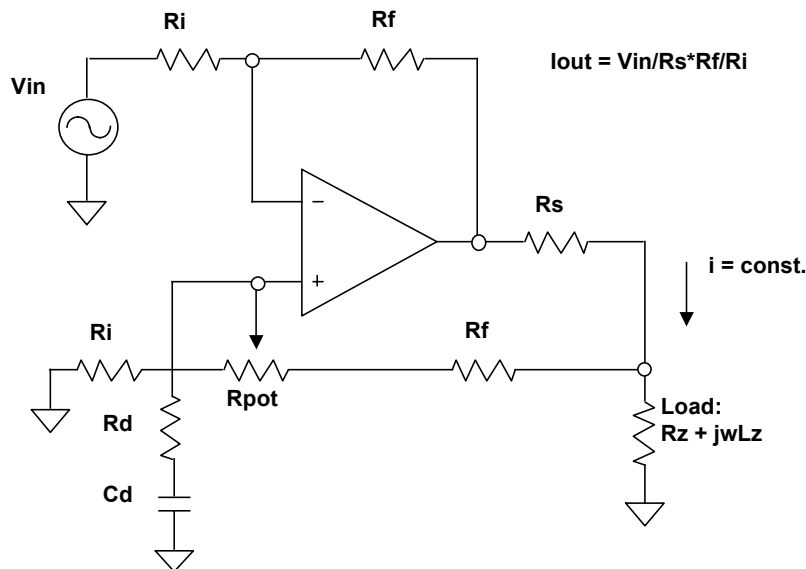
For any engineering problem there is usually more than one solution. This is true when reviewing AC stability compensation for the Improved Howland Current Pump and proposing a solution, or two!

Shown above are two compensation techniques, Compensation 1 and Compensation 2. $FB\#1$ for both compensation techniques will be the same. Similar to V—I circuits for floating loads this $\beta +$ feedback path which will cause a zero in the net $1/\beta$ plot which will result in 40dB per decade rate of closure and instability without additional compensation provided by $FB\#2$.

$FB\#2$ has the function of reducing the voltage fed back to the +input at higher frequencies and thereby forming a pole in the net $1/\beta$ plot which guarantees stability and a 20dB per decade rate of closure.

COMPENSATING THE HOWLAND CURRENT PUMP

10 STEPS TO STABILITY



Inductive loads cause stability trouble with current source applications. Because current lags voltage in an inductor, current feedback is delayed and thus decreases the phase margin of the current amplifier. Consequently, ringing or oscillation occurs. This following procedure shows a proper compensation technique for inductive loads.

After choosing R_i , select an appropriate current sense resistor R_s . The voltage available to your load is the power supply voltage minus the voltage drop across R_s . Power dissipation of R_s calculates to $P_{rs} = I_{max}^2 * R_s$. Continue to calculate the following component values: Finally, adjust R_d and C_d values to standard values and insert a trim pot between the feedback resistor and the input resistor of the positive feedback network:

$$R_{pot} = .02 * \Delta R[\%] * (R_i + R_f)^1$$

The potentiometer compensates the resistance mismatch of the R_f/R_i network. Trim for maximum output impedance of the current source by observing the minimum output current variation at different load levels and maximum output current.

¹ $\Delta R[\%]$: resistor tolerance in percent

COMPENSATING THE HOWLAND CURRENT PUMP

10 STEPS TO STABILITY

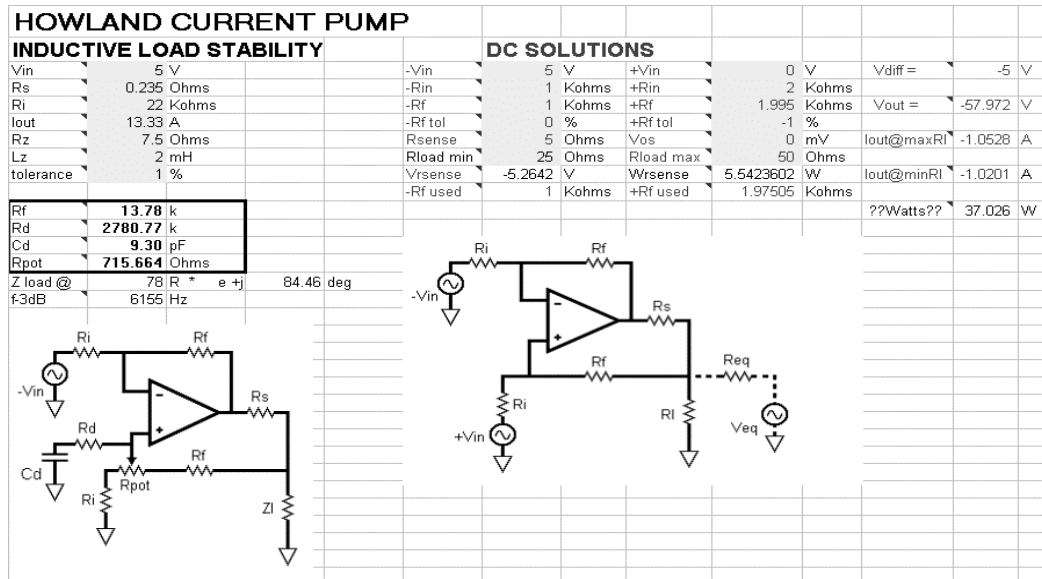
Step	Description	Symbol	Formula
1	feedback resistor	R_f	$I_{out}/V_{in} * R_i * R_s$
2	negative feedback factor	β_-	$R_i / (R_i + R_f)$
3	positive feedback (DC) factor	β_+	$R_z / (R_z + R_s) * \beta_-$
4	total feedback factor	β_{tot}	$(\beta_-) - (\beta_+)$
5	corrected total feedback limit (AC)	β_{lim}	$\beta_{tot}/10$
6	corrected positive feedback	β_{cor}	$(\beta_-) - (\beta_{lim})$
7	parallel resistance of ground leg ($R_d \parallel R_i$)	R_p	$R_f / ((\beta_{cor}^{-1}) - 1)$
8	compensation resistor	R_d	$(R_p^{-1} - R_i^{-1})^{-1}$
9	zero feedback frequency	f_z	$(R_s + R_z) / (2 * \pi * L_z)$
10	compensation capacitor	C_d	$L_z / (10 * R_d * (R_s + R_z))$

For single supply operation, two pull-up resistors are required to bias the input stage up to the minimum specified common mode voltage. They are connected from both input terminals to the positive supply and must be closely matched, too. Voltage sources represent a zero impedance (ideally) and let those pull-up resistors appear in parallel to the input resistors. A trim pot allows offset current adjustment. Apex Application Note #21 expands on single supply operation.

Note, that the current control bandwidth (f_{-3dB}) is much less than the small-signal bandwidth (f_{cl}) shown in the Bode plot. As a rule of thumb, the compensation frequency is a decade above the zero frequency f_z . Maximize current sense resistor R_s , as far as voltage swing headroom and power dissipation allow. This improves current control bandwidth. For a slope of 20dB/decade, the gain limit for high frequencies is 20dB above the DC voltage gain.

Refer to App Note #13 for details.

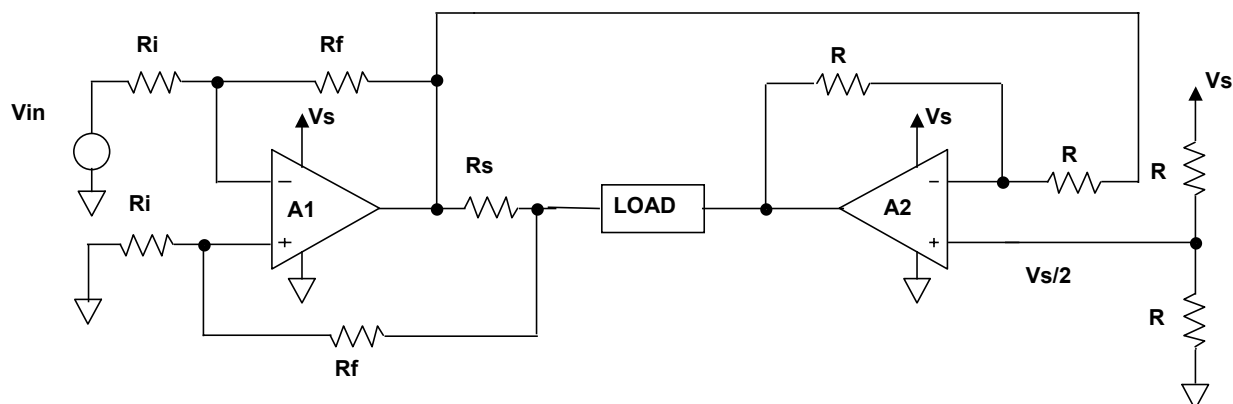
Stability for the Howland



Again, Power Design eases the design burden. Cells to describe the circuit, both for stability analysis and error budget analysis. There are many other pieces of data lying outside this slide if you like to dig around. Application Note 13, Voltage to Current Conversion is the reference.

VOLTAGE-to-CURRENT CONVERSION

SINGLE SUPPLY, BRIDGE MODE



+/-Vload LIMITED BY Vcm LIMITS OF A1

This configuration combines two previously covered techniques: single supply bridge configuration and V to I conversion using the improved Howland current pump. A2 is biased at the familiar $V_s/2$ mid-supply point. R_f and R_i must be ratioed such that during min and max output voltage swings of A1 the common mode input range of A1 is not violated. This imposes a max output voltage swing limit across the load. I_{out} through the load is given by: $I_{out} = (V_{in} \cdot R_f) / (R_s \cdot R_i)$. R_s is selected as large as possible to give as much voltage feedback as possible with acceptable power dissipation. V_{in} is set to its most positive value. V_{cm} for A1 (common mode input voltage for A1) is set to comply with data sheet specifications. Usually this will be about $V_s - 6$, which means V_{cm} must be at least 6.0 volts. R_i is selected to cause about .5 mA to flow through it when V_{in} is at its most negative voltage. This then dictates the value for R_f which is selected to complete the V_{in} to I_{out} equation given above. V_{cm} should then be rechecked for input common mode compliance at positive and negative swing out of A1. Recall that $V_{out}(A2) = V_s - V_{out}(A1)$ for the given circuit. $V_{out}(A1)$ must be at least V_{cm} to keep A1 operating in the linear region. Then $V_{load} = (V_s - V_{cm}) - V_{cm}$. In other words $V_{load} = V_{out}(A2) - V_{out}(A1)$. Therefore, the maximum output peak voltage across the load for this configuration is $V_s - (2 \cdot V_{cm})$.

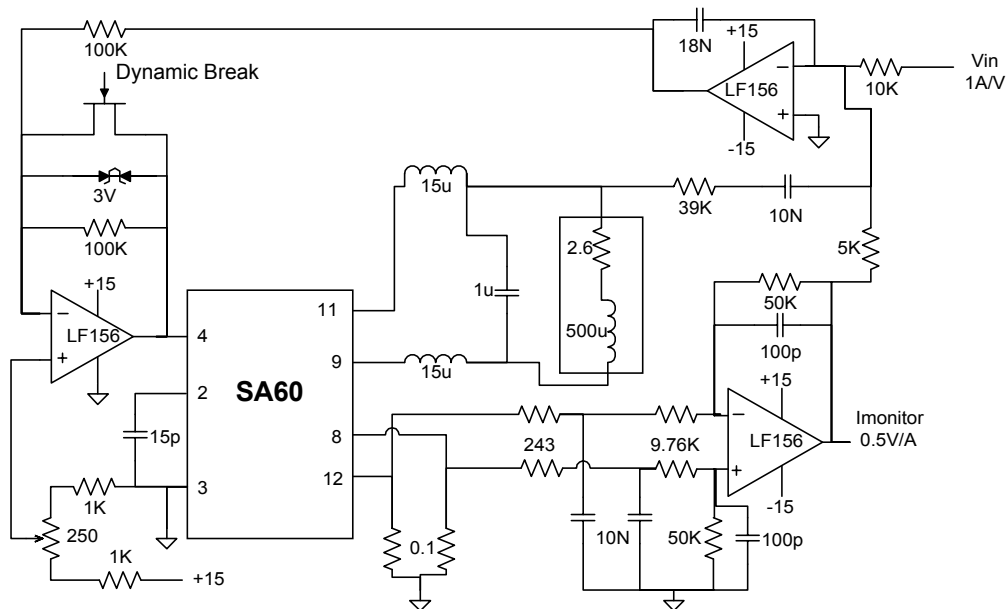
MOTION CONTROL

Position, Torque or Speed

- **Brush**
- **Micro-steppers**
- **Linear (voice coil)**
- **Multi-phase AC**
- **Galvanometers**

One of the largest applications for high power op amps is in motion control. High current high power op amps can be used for all components of motion control including speed control, position control and torque control. Their ease of use, rapid design ability and rugged hybrid construction lead to cost effective motion control systems.

Z-Axis Voice Coil Position



Slower versions of this machine used a PA12 linear op amp for Z-axis control. Even though currents were lower and motor impedance was higher, an exotic custom heat sink had to be designed to fit the small physical location of the amplifier. It was clear that this generation of the machine required higher efficiency in the drive circuit. The SA60 provides this and being programmed to switch at about 220KHz, it provides adequate bandwidth for the high speed servo loop.

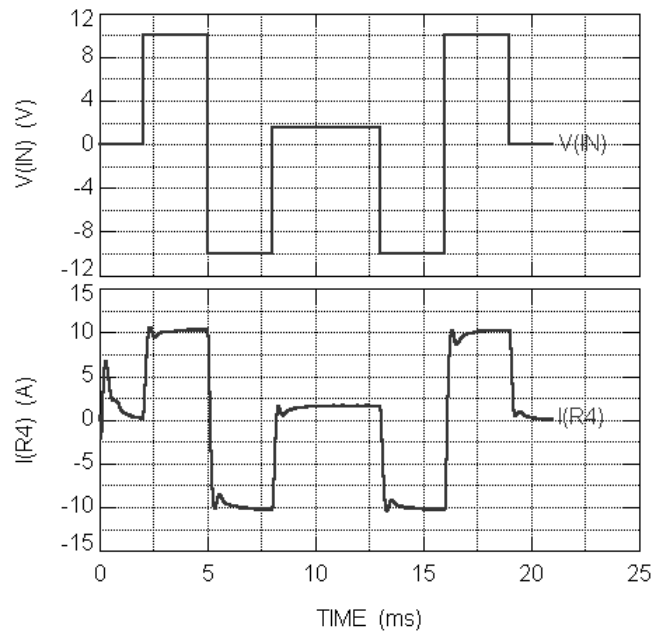
Current sense resistors of 0.1Ω develop 1V at the 10A current peaks giving very good resolution and accuracy for the differential current monitor which provides the $\frac{1}{2}V/A$ feedback signal. Both poles of the differential amplifier were placed at roughly $\frac{1}{4}$ the switching frequency. This amplifier needs to be the fastest responding block of the system.

The pure integrator now reacts to any magnitude difference between feedback and input command signals. The 18nF makes the integrator significantly slower than the current monitor. The 39K/10nF network becomes the dominate feedback path just before the V-to-I phase shift of the motor inductance brings on stability problems.

With the dynamic brake signal low, the last amplifier inverts the drive signal to the SA60 and limits drive amplitude to just greater than the peaks of the triangular ramp. When the dynamic brake is applied, this amplifier becomes a unity gain buffer for a DC level adjusted to insure the SA60 output is a low impedance, near zero voltage.

Even though the nominal motor inductance was adequate to keep ripple current in check, this inductance varied with position of the motor and a filter was used clean up the circuit.

Z-Axis Voice Coil Position



After power up settling, the first 3msec pulse accelerates the motor toward the work piece; the second 3msec pulse decelerates the motor; a constant pressure is held for 60msec (time was compressed in this plot); the last two pulses move the motor back to home position; and at $t=150\text{msec}$ the cycle is repeated.

Here is a method to calculate a heatsink for this type application. First, assume a reasonable case temperature for the amplifier. We will pick 60°C . Application Note 11 tells us the temperature of a heatsink with any reasonable mass will change very little during the period of 150msec, so knowing average power dissipation over the cycle will establish a thermal rating.

Use Power Design to find the power levels for each of the three output current levels by entering a heatsink rating of .01 and adjusting ambient temperature to obtain a 60° case temperature. Enter a minimum frequency less than 60Hz to insure power is calculated for steady state. Here are the results:

I out	Ta	Power	Tj	msec	W*msec
.01	60	11.3	61	78	881
1.5	59	12.5	61	60	750
10	52	77.3	103	12	928

Total = 2559 Divide by 150 msec = 17.1W avg.

If ambient temperature is 25°C , a 2°C/W heatsink will allow a case temperature rise of about 34° , meeting the assumed 60° operating point.

While it was not shown in the schematic, it is imperative that a heatsink mounted over-temperature shutdown circuit be installed and set for less than 90°C . The over-temp limit was found in a similar manner as the previous data, except ambient temperature was adjusted to obtain a junction temperature of 149° .

MOTOR RATINGS AND AMPLIFIER SELECTION

CAN PA21A BE USED?

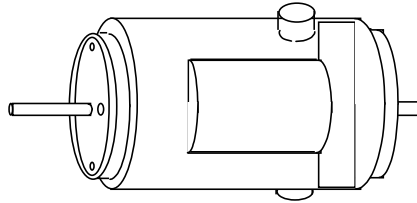
MOTOR RATINGS:

Electro-Craft E 540A

Torque Constant: 10oz/in/A

Voltage Constant: 7.41V/KRPM

Winding Resistance: 1.24



APPLICATION REQUIREMENTS

10oz/in/torque

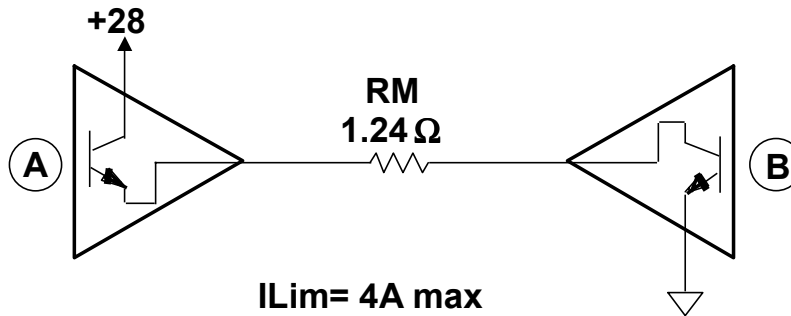
3240 RPM

24V @ 1A

Will the PA21A do? It is rated 3A peak. This application only needs 1A normally.

Ref. AN24

EVALUATION AGAINST SOA



$$4A \times 1.24\Omega = 4.96V \text{ ACROSS LOAD}$$

$$28 - 4.96 \cong 23.0V$$

23V WORST CASE STRESS ACROSS AMPLIFIER B

11.5V PER AMPLIFIER IF A CURRENT LIMITS FIRST

The above model provides us with a tool for analysis to examine worst case SOA stresses. This represents the condition for motor start-up or stall (not as demanding as instant motor reversal which is easily avoidable).

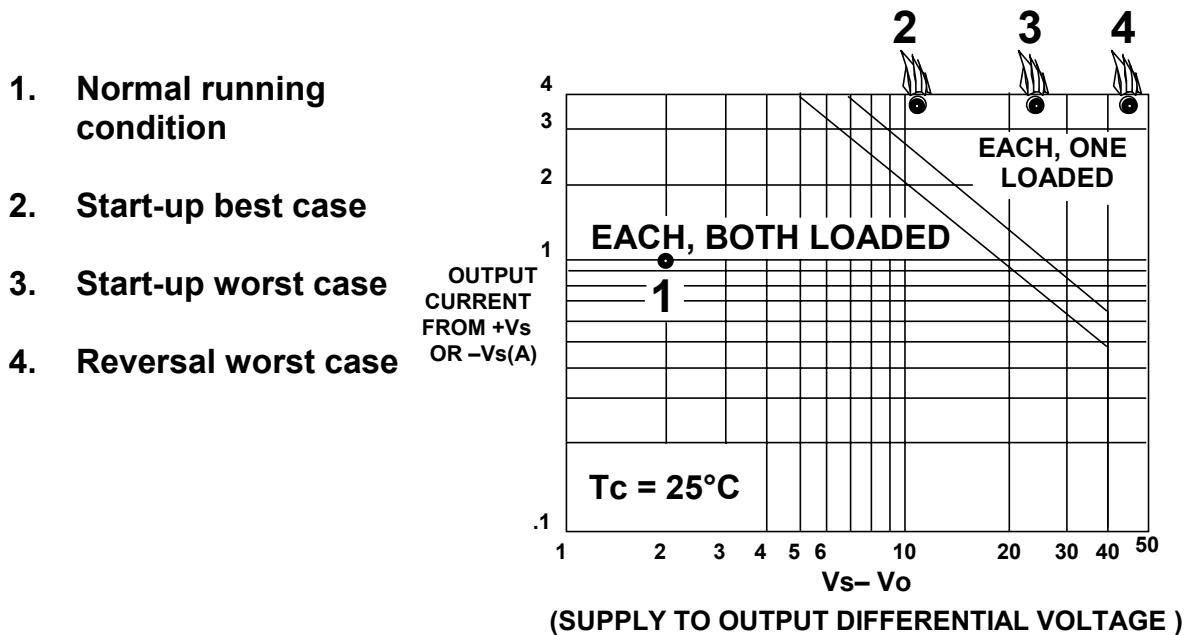
For this condition the motor is modeled as a 1.24 ohm resistance at stall. Assuming the PA21 current limit is at 4A results in a 4.96V drop across the load. Since it is not known which amplifier half will current limit first we must assume the worst case. If op amp B limits first all 23V of voltage stress will occur across it.

If op amp A were to current limit first or both op amp A and op amp B current limit at the same level then the voltage stresses would be equal at 11.5V across each.

For our SOA evaluation of the PA21 we will need to assume a 4A, 23V stress. In amplifiers with externally adjustable current limit we can guarantee op amp A current limits first by setting op amp B current limit 20% higher than that of op amp A and thereby equalizing voltage stresses across each op amp.

Ref. AN20,AN24

PA21 SAFE OPERATING AREA (SOA)



Plotted on the PA21 SOA graph are the four possible operating conditions for the PA21 when used with the Electro-Craft E540.

Point 1 is normal running condition which is well within the SOA boundaries.

Point 2 is the best case start-up condition where both op amp A and op amp B current limit at the same level or op amp A current limits first.

Point 3 is the worst case start-up condition where op amp B current limits first and bears the total voltage stress.

Point 4 is a worst case motor reversal condition with op amp B current limiting first.

It is readily apparent that with the PA21's non-adjustable internal current limit of 4A there is not sufficient SOA for driving this motor in start-up or stall conditions. Our alternatives will be either a complex soft-start circuit or power op amps with larger SOA.

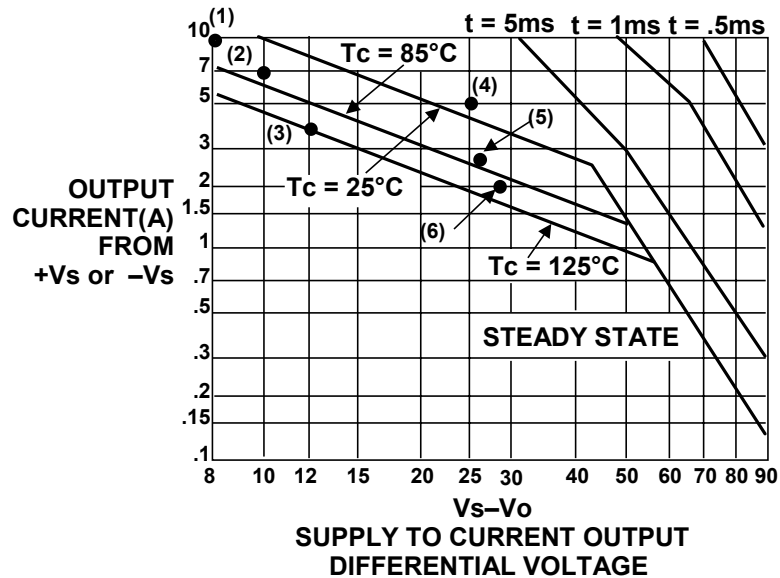
Ref. AN20,AN24

PROTECTION ALTERNATIVES

PA61 — IMPROVED SOA+Current Limit Adjust

START-UP		
I _{um}	V _s -V _o	
10A	8V	(1)
7A	10V	(2)
4A	12V	(3)

REVERSAL		
I _{um}	V _s -V _o	
5A	25V	(4)
2.5A	26V	(5)
2A	27V	(6)



Often the only solution to the conflicting requirement of protection along with reasonable motor acceleration is simply an amplifier with a larger SOA. Not only does the PA61 provide a better SOA fit but the programmable current limit provides additional flexibility in meeting SOA requirements.

Points 1 thru 6 above on the PA61 SOA plot show a variety of operating choices depending upon what start-up current is desired, whether motor reversals are a possibility, and what heatsinking is available referenced to op amp case temperature.

The following handy formulae provide a quick way for estimating these points given a properly designed bridge circuit.

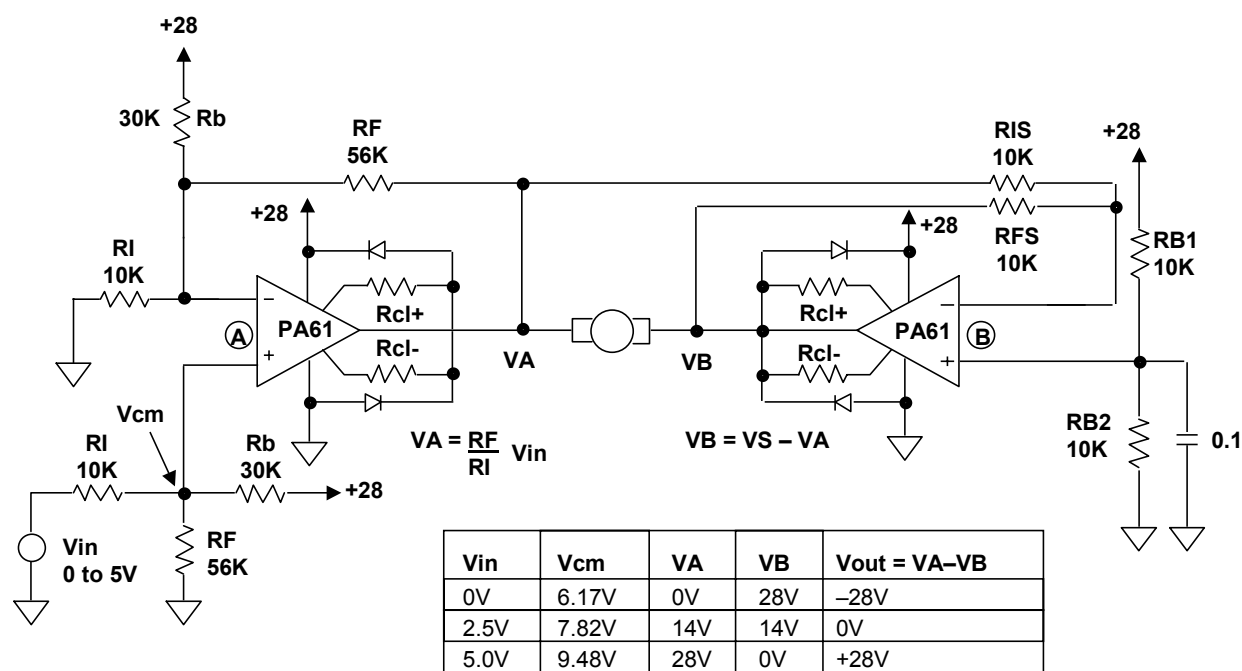
$$\text{START-UP: } V_s - V_o(\text{each op amp}) = V_s - (I_{\text{limit}} * \text{Motor resistance})/2$$

$$\text{REVERSAL: } V_s - V_o(\text{each op amp}) = 2 * V_s - (I_{\text{limit}} * \text{Motor resistance})/2$$

Where: V_s = total supply voltage.

If using a single amplifier rather than a bridge, delete the “/2” term. The reversal formula makes 2 assumptions: Prior to reversal, output voltage was saturated all the way to the rail and motor back EMF = V_s. This may not be true by virtue of input signal level, and cannot be true by virtue of the output voltage swing spec of the amplifier (saturation limit) and plus it requires a zero ohm motor. Despite all this it's a good first order approximation.

PA61 MOTOR DRIVE

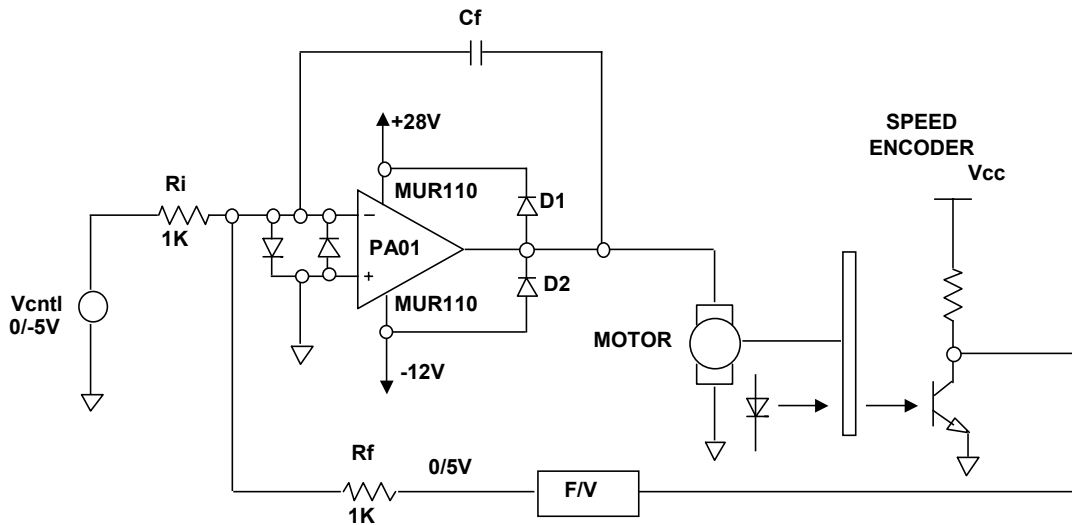


Ideal Outputs!!!

Our first alternate drive circuit for controlling the Electro-Craft motor utilizes a bridge of PA61 class “C” power op amps. Class “C” amplifiers are usually less expensive than similar class “AB” devices. While our PA61 implementation does require more components, than would our original PA21 circuit, it has the SOA to withstand start-up and even reversal conditions. Note that the PA61 has enough voltage range to handle this motor with a single amplifier. If the 28V supply is already part of the system, this may not be a good economic choice. PA73 is a 5A class “C” amplifier which would be a good candidate if high speed mechanical response is not of prime concern.

Amplifier A uses our Single Supply Non-Inverting Configuration seen previously to meet the common mode scaling requirements of the PA61. Gain scaling with this arrangement is set to try to drive the amplifier into saturation trying to achieve 0V or +28V out of the amplifier. This scaling needs to be cut back according to the saturation voltage of the specific amplifier at the specific output current level to be used. The specification is labeled Voltage Swing in the data sheet. This voltage is lost twice in a bridge circuit, once for each amplifier.

SIMPLE SPEED CONTROL



In speed control circuits the usual approach taken is to integrate the difference between an input voltage signal and a feedback signal that gives information about the speed of the motor being driven. In the application above a PA01 is being used to drive a DC motor with an integral speed encoder that outputs a pulse train whose frequency is proportional to the angular velocity of the motor. This signal is then fed to a VFC, or Voltage to Frequency Converter, that is operated in the frequency to voltage mode. The output voltage of the VFC appears across R_f to create a current into the summing node of the amplifier. Likewise, V_{cntl} appears across R_i to create a current out of the summing node. When: $V_o(VFC) = -V_{cntl}$, then no current is fed to C_f , the integrating capacitor. If there is a difference between the current fed into the summing node by the Vfc and the current removed out of the node by the control voltage the difference current is fed to the integrating capacitor resulting in a change in output voltage which acts to correct the error.

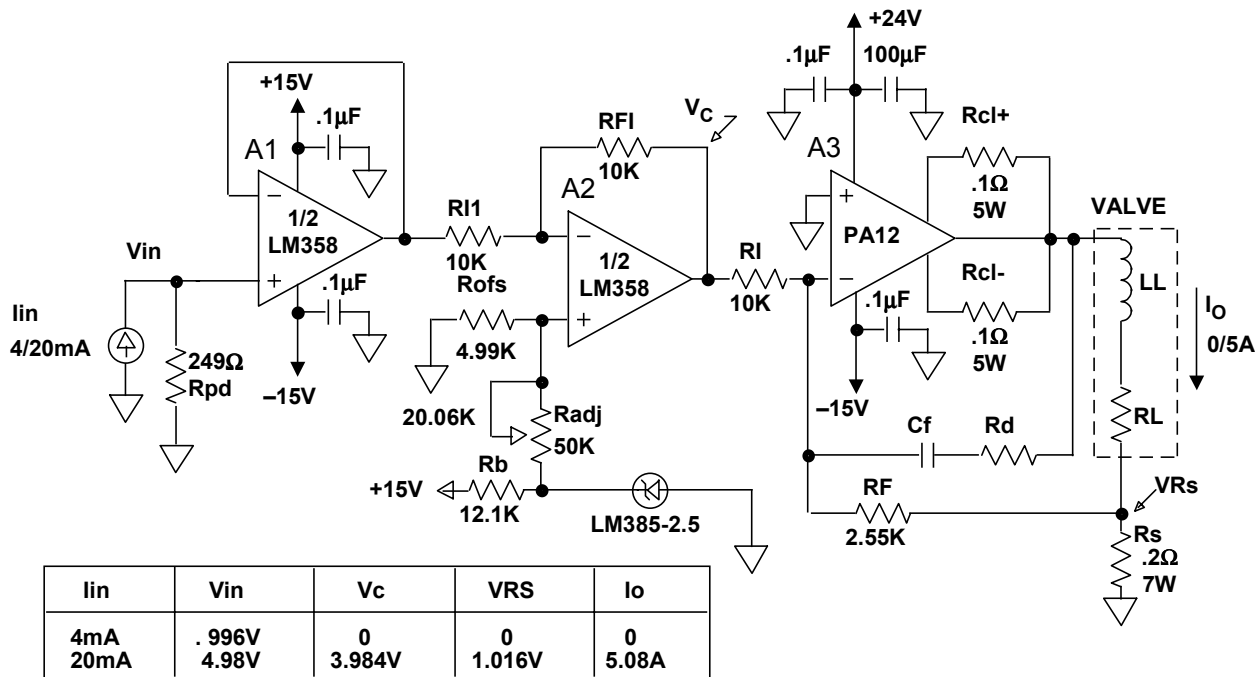
Note that since the PA01 is driving a DC motor which can generate a continuous train of high frequency kickback pulses external flyback protection diodes, MUR110's were added from the output to the supplies in order to protect the PA01's output stage.

Unless dynamic braking is used, the -12V supply needs to support amplifier quiescent current only; a maximum of 50mA for the PA01.

The SA01 was chosen for its size and cost even though its single current sense pin does not provide direction information. The fact that the current sense resistor in series with the motor is anywhere between zero and 48V is no problem for the unity gain INA117 instrumentation amplifier. The 1K Ω resistors of the filter networks have no appreciable affect on accuracy. The gain of 10 stage has more filtering.

The four SA01s share a common heatsink and fit in a single 19 inch rack along with some other power components.

VALVE CONTROL CURRENT-TO-CURRENT CONVERTER

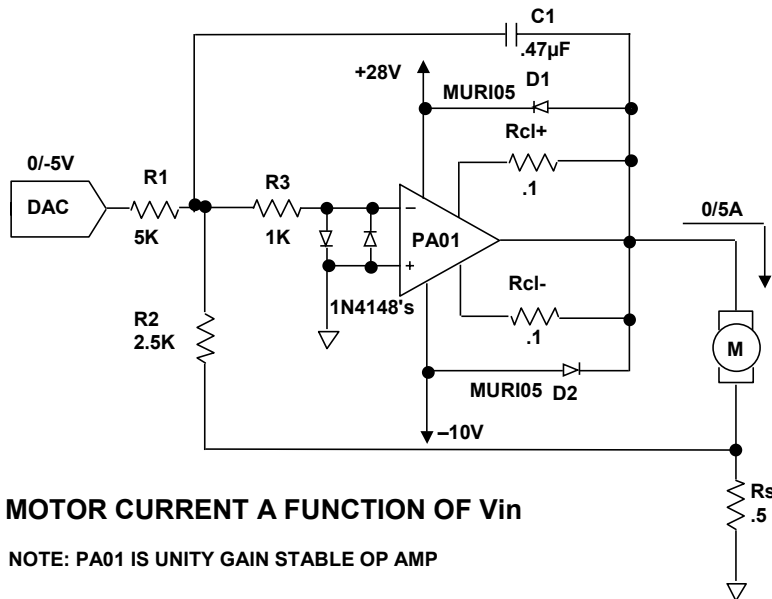


This circuit provides a Current-to-Current converter function through translation of a 4-20mA current transmitter to 0-5A output for linear control of a valve.

The 4-20mA is converted to a voltage through the use of a 249 ohm pull down resistor and buffered by A1. This voltage, V_{IN}, is then offset to zero through the use of a precision voltage reference and a summing amplifier. Voltage V_C then becomes the input command for the Voltage-to-Current conversion output stage using the PA12.

To guarantee AC small signal stability, stability analysis needs to be done using the load resistance and inductance of the actual linear valve to be used. These stability techniques we have covered previously. Be aware that valve inductance is likely a dynamic parameter changing with position of the valve.

PROGRAMMABLE TORQUE CIRCUIT

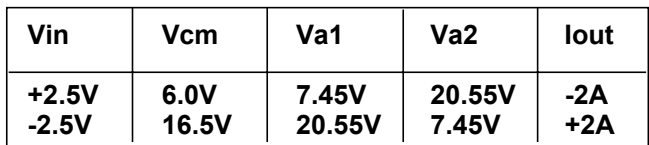


This schematic uses several tricks that we've learned. First of all, notice that the PA01 is operating from non-symmetrical supplies. The -10 volt supply is merely to provide input common mode bias. The 28 volt supply is used to supply the load current.

In a motor, torque is directly proportional to current, so this is another form of voltage to current conversion. The inverting node of the PA01 is used as a summing node. Into the summing node flow two currents, one is the input voltage from the DAC across $R1$, the second is the feedback voltage ($I_{load} * R_s$) across $R2$. These two currents are summed and the difference current is fed to $C1$ to be integrated. When the current through the motor is at the proper value the voltage across R_s will produce a current into the summing node that is equal to the current out of the summing node from the DAC. This results in no current flow to the integrating capacitor $C1$ resulting in a fixed output current.

Note that since the PA01 is driving a motor, high speed flyback diodes, MUR105s, are used to protect the amplifier's output stage against flyback voltage spikes. Also note that in integration type circuits the integration capacitor is connected directly from the output of the amplifier to the input. This means that high frequency pulses can be fed back directly to the input stage. Therefore we show 1N4148 input protection diodes and $R3$ in this application to prevent input stage damage to the PA01 caused by flyback coupling through $C1$.

SINGLE SUPPLY



Note that the $V_s - 6$ common mode voltage range is met under both conditions of output voltage swing on A1. Also note that the peak output voltage swing is limited to less than $V_s - (2 * V_{cm})$ as was mentioned in the generic case for this configuration.

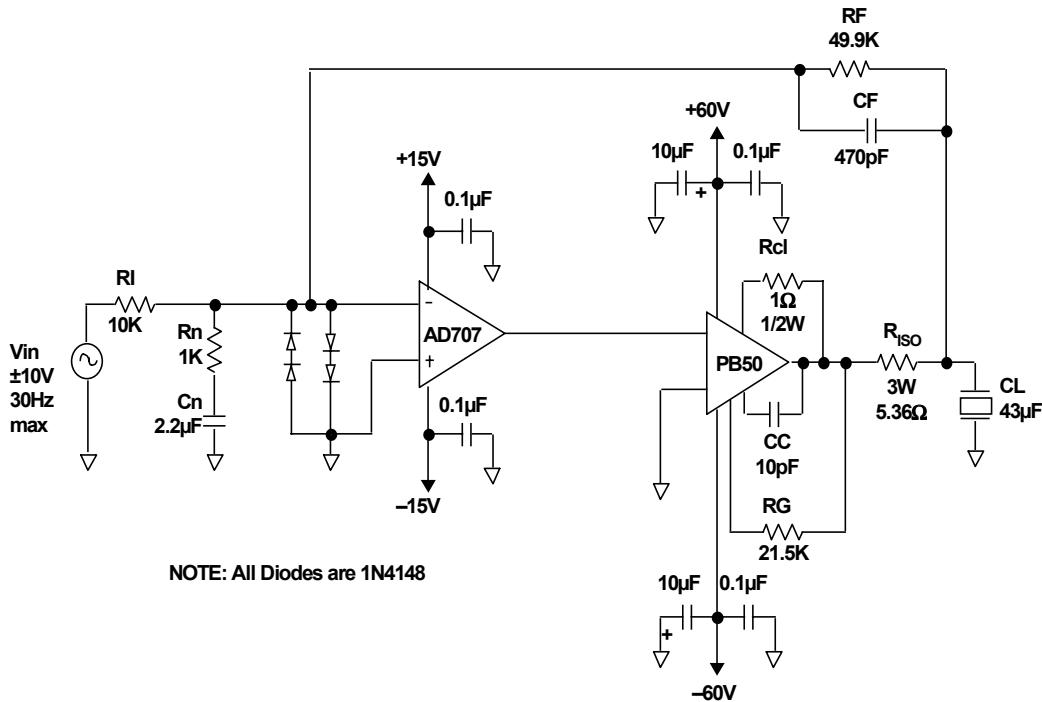
Ref. AN21

ATE APPLICATIONS

- High Voltage PPS
- High Current PPS
- AC Power Supplies
- Pin Drivers
- Waveform Generators
- Active Loads

There are an extensive array of applications for high power, high voltage, and/or high speed linear amplifiers in almost any type of automatic test equipment. Some of the most popular applications include different types of programmable power supplies. There are also ample opportunities for them to be used for waveform generation for DUT excitation.

LOW DRIFT PB50 PZT TESTER

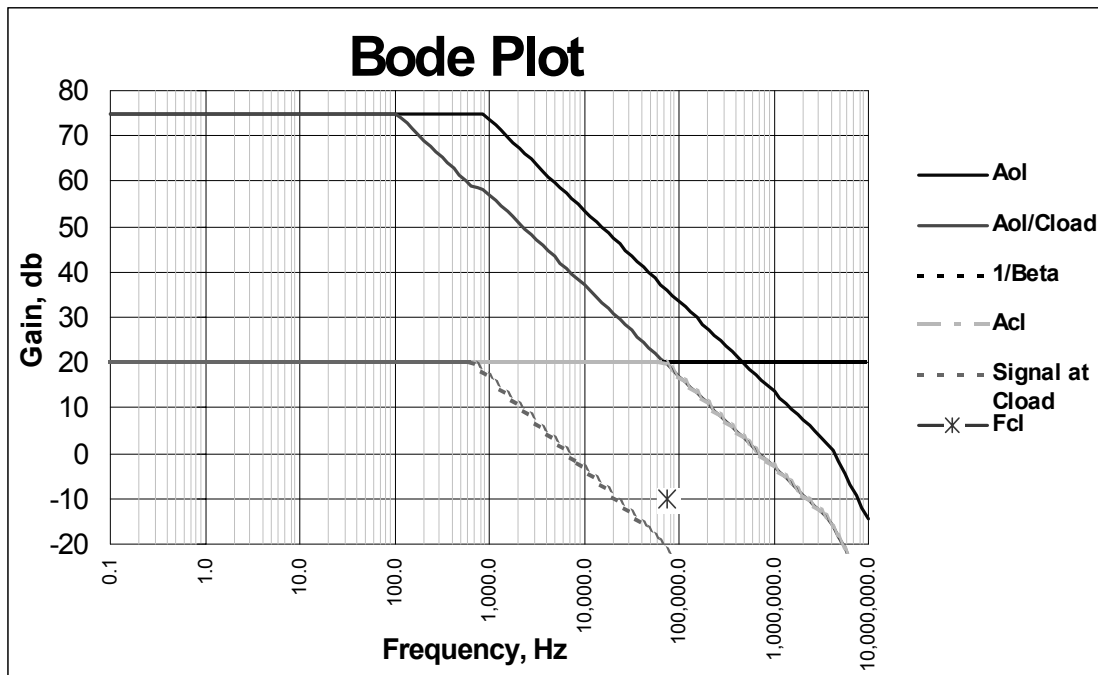


This Low Drift PB50 PZT Tester utilizes the flexibility of the PB58 power booster to provide low drift, high accuracy voltages to the PZT (Piezo Transducer) under test. The AD707 provides a composite amplifier input offset voltage of 90 μ V, and a drift of 1 μ V/ $^{\circ}$ C. Higher accuracy can be obtained with a different host amplifier or a better grade of AD707.

The PB50 is a versatile building block for ATE design that provides a low cost option for providing high voltages to devices under test. With supply voltages from ± 30 V to ± 100 V, with a slew rate of 100V/ μ S, and output current drive capability of 2A, The PB50 can provide up to 100KHz power bandwidth for high voltage test equipment. The composite amplifier approach for using this power booster allows the user to program the accuracy of the overall amplifier through selection of the front end host amplifier.

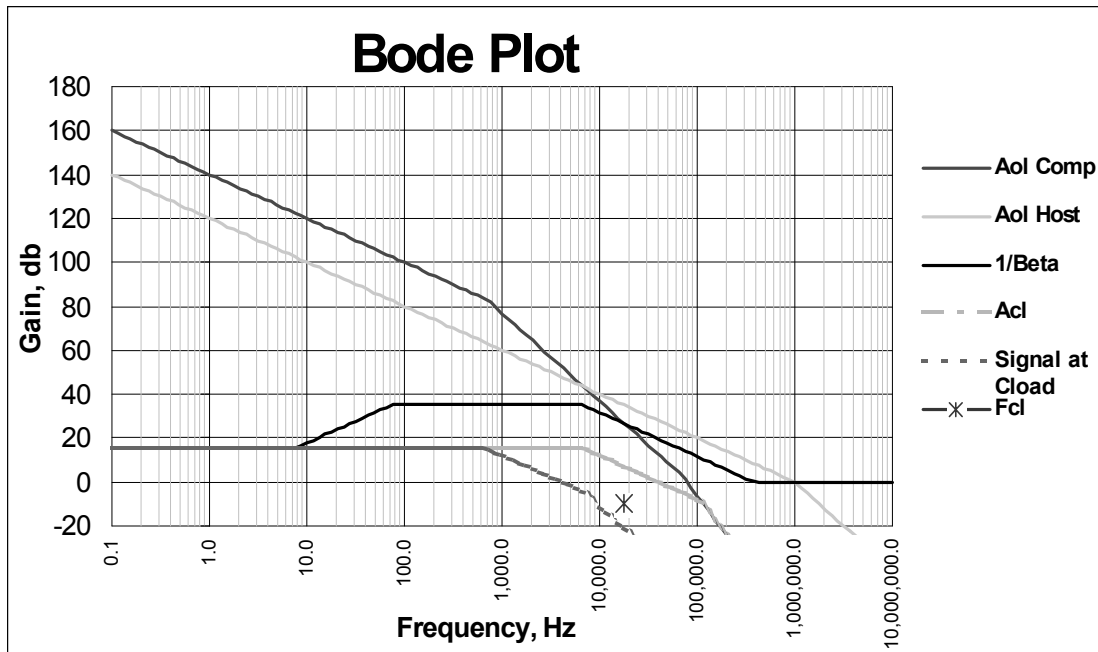
This particular implementation of the PB50 will present some stability challenges since we are driving a capacitive load with a composite amplifier. The approach to stabilizing this circuit will be to stabilize the power booster with its capacitive load and then stabilize the total composite amplifier. We don't stand a chance of stabilizing the composite amplifier if the output power booster is not stable first.

MAGNITUDE PLOT FOR PB50



Without the isolation resistor, the modified Aol curve would have changed to -40db per decade just under 1KHz giving an unacceptable intersection rate and about 2.5° phase margin rather than 90°.

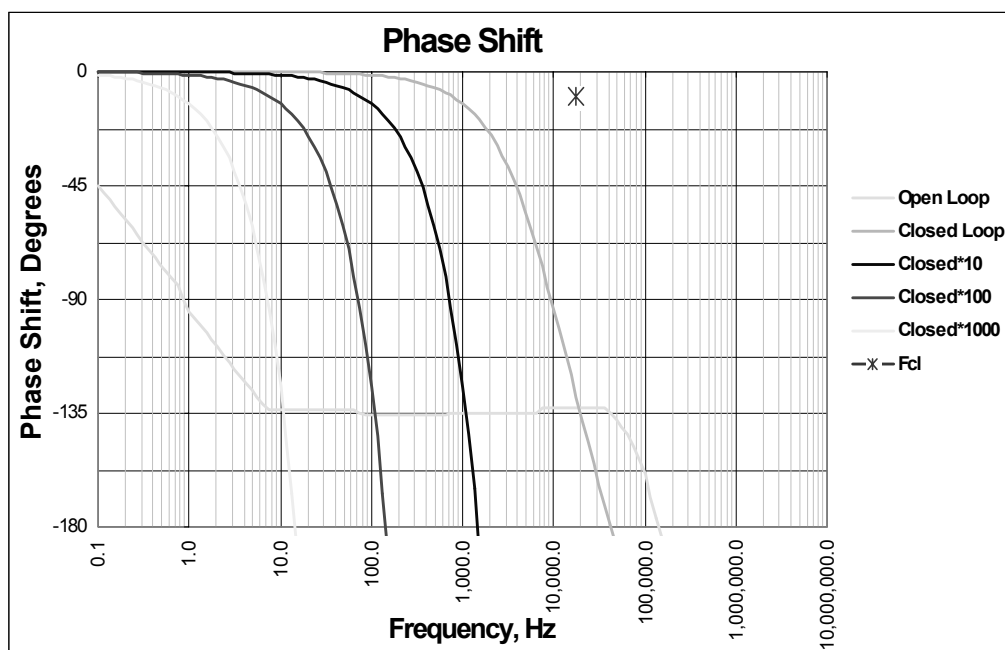
COMPOSITE MAGNITUDE PLOT



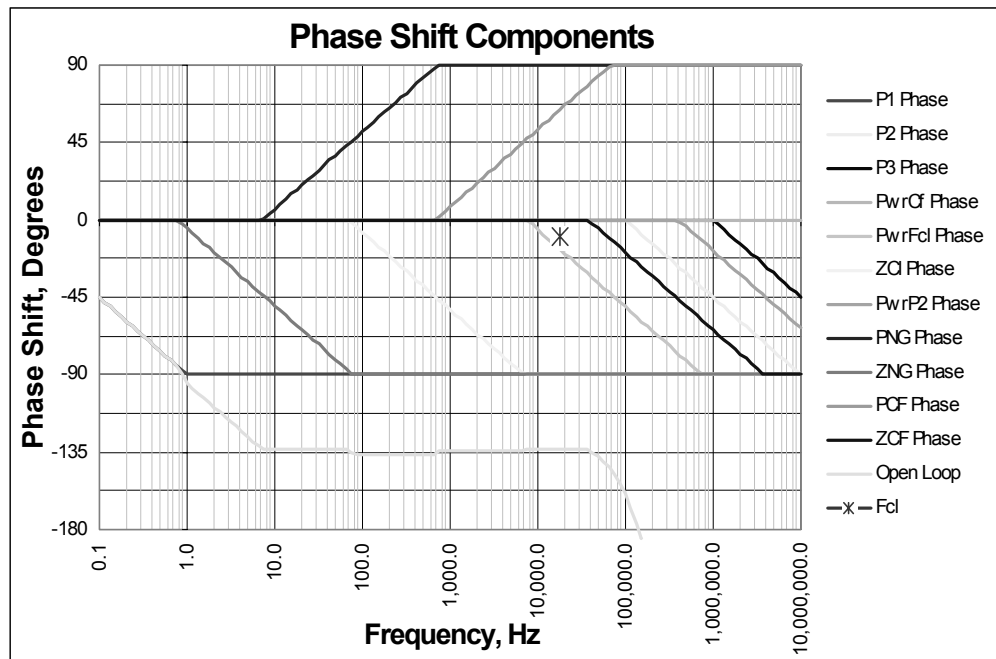
Now that the power stage is stable we add its closed loop gain to the open loop gain of the host amplifier. Note that it is the poles of the power stage rather than the host producing the -40db per decade slope in the area of interest. A roll off capacitor gives us required slope for good intersection rate and noise gain allows good placement of the actual intersection.

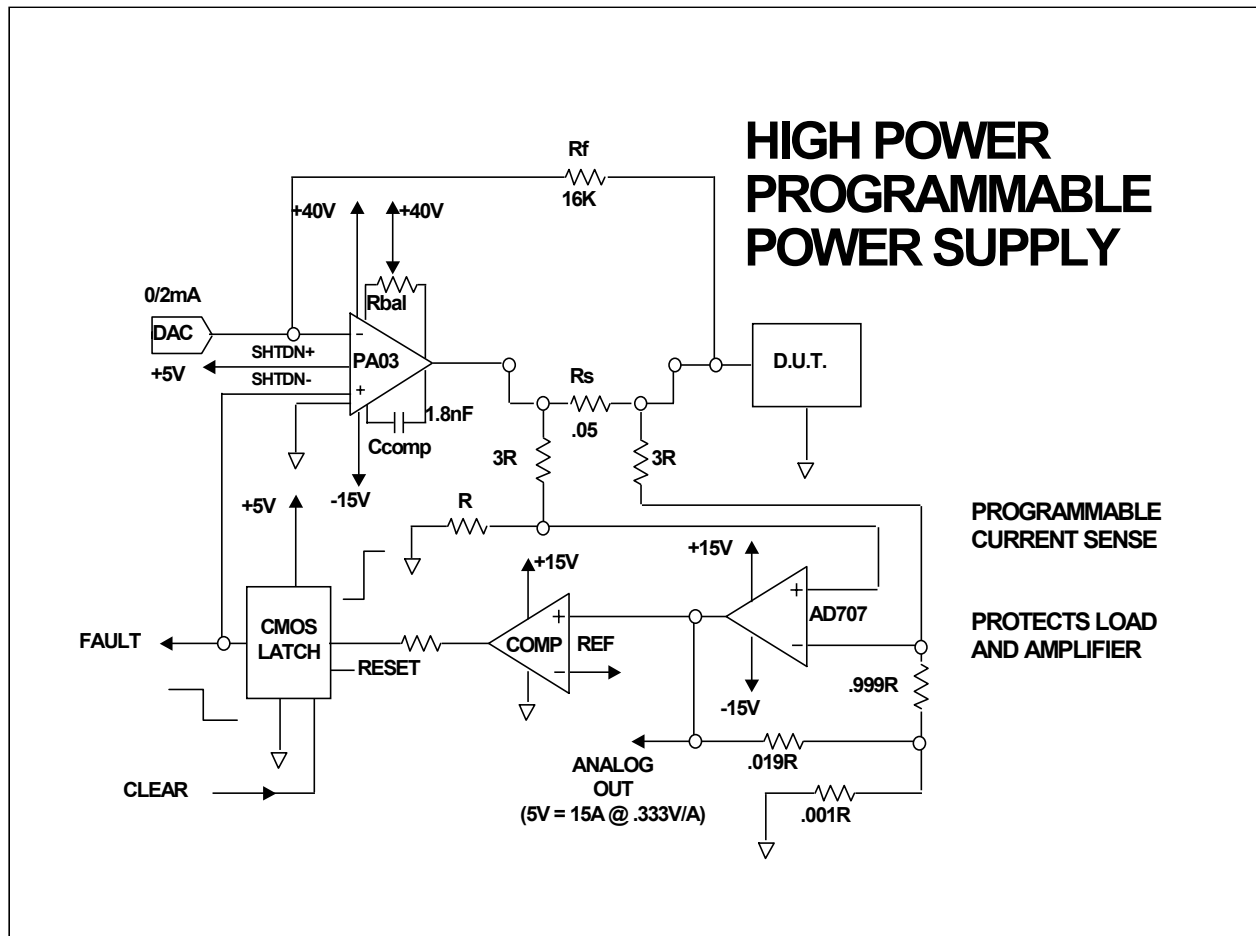
In this circuit final value selection was a result of playing "what-if", and the phase component graph was very useful. The first pole of the host amplifier is at 0.1Hz giving a 90° open loop phase shift by 1Hz. The first pole of the power stage at just under 1KHz produced 180° at less than 10KHz. Visualizing the phase components moving on the graphs and using the R-C calculator make fairly short work of the design.

COMPOSITE OPEN LOOP PHASE PLOT



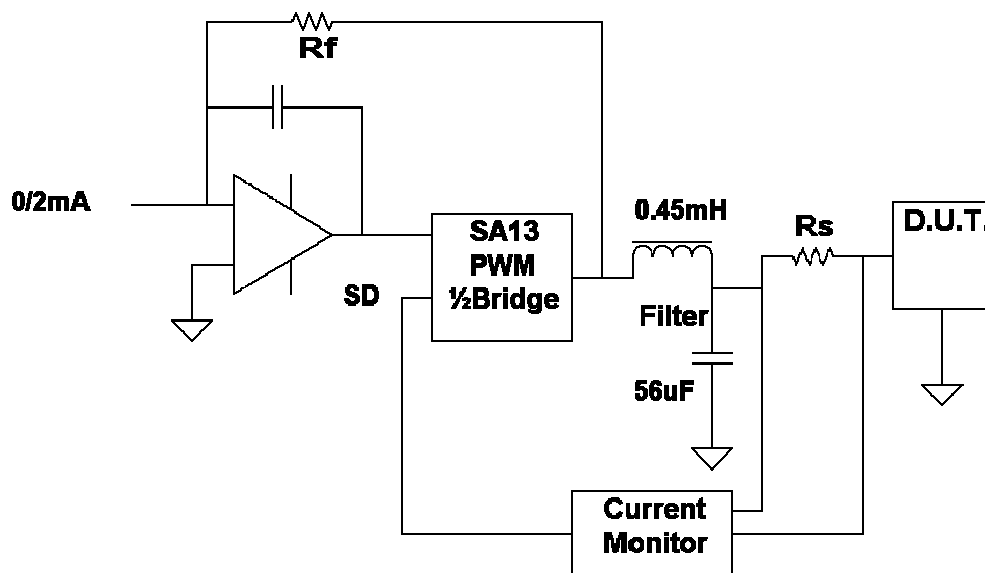
COMPOSITE OPEN LOOP PHASE PLOT





In this circuit the PA03 is being used in a simple, reliable programmable power supply which utilizes the PA03 shutdown features. It requires little calibration because the current to voltage conversion of the DA converter output is done by the power op amp itself while a 12 bit DAC (i.e. DAC80) provided accuracy levels high enough to eliminate the need for adjustment. R_s senses current to the DUT. The AD707 is configured as a difference amplifier which senses the voltage across R_s and develops an analog output signal proportional to DUT current through R_s . It is then compared to a reference voltage which determines the current level desired. The comparator will trip high once this current limit is exceeded thus tripping a CMOS latch low and resulting in a 5V differential signal between the two shutdown pins on the PA03. This circuit is explained in detail in Application Note 6 in the Apex Data Book.

PWM Alternative



The PA03 works fine but is not suitable for longer duration or higher supply voltage.

This PWM alternative keeps the same overall function and programming but reduces power dissipation dramatically. For the same test sequence described in Ap Note 6, average power is reduced by a factor of 6. The better news is that the PWM version is capable of continuous operation while dissipating only 30W compared to 306W (liquid cooling is a must) for the linear counterpart. As an added benefit, a more standard 48V supply can be used while adding very little power dissipation.

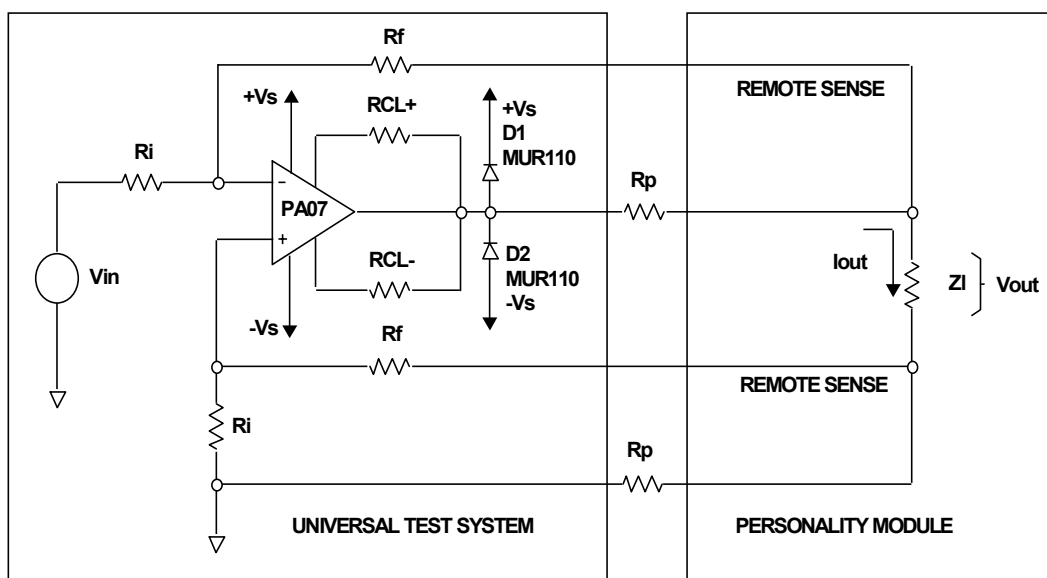
As mentioned before, the PWM circuit has more noise than the linear. The simple filter shown is capable of keeping ripple down to 100mV peak. Higher order filters can do even better.

Speed differences between linear and PWM circuits will be less than you might think. ATE test sockets almost always have large bypass capacitors. This capacitance will demand large currents to charge quickly thus being the speed bottleneck for both types of circuits. Again, good news: A single capacitance can function as filter element and bypass for the DUT socket.

On an amplifier cost basis (@100): PA03 \$350

SA13 \$265

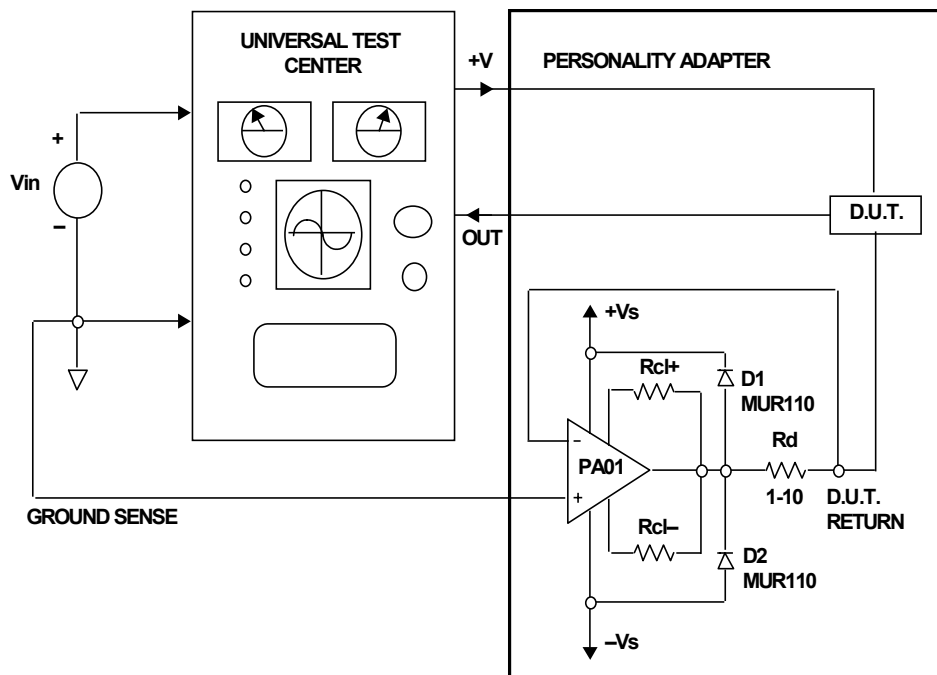
REMOTE SENSE



Universal test stations often contain a power op amp that is used to provide power to some remote load. If significant amounts of current are being delivered to this remote load, the parasitic resistance of the wiring can contribute significant errors to the measurements. For instance, 50 milliohms of wire resistance in the output and return line would result in an error voltage of 500mV with a 5A load current. When the power amplifier is configured as a differential amplifier, with the differential plus remote sense and minus remote sense lines being run directly to the load and connected across the load at the remote site, drops from the parasitic resistances become common mode signals to the difference amplifier and are rejected due to the high CMRR of the amplifier.

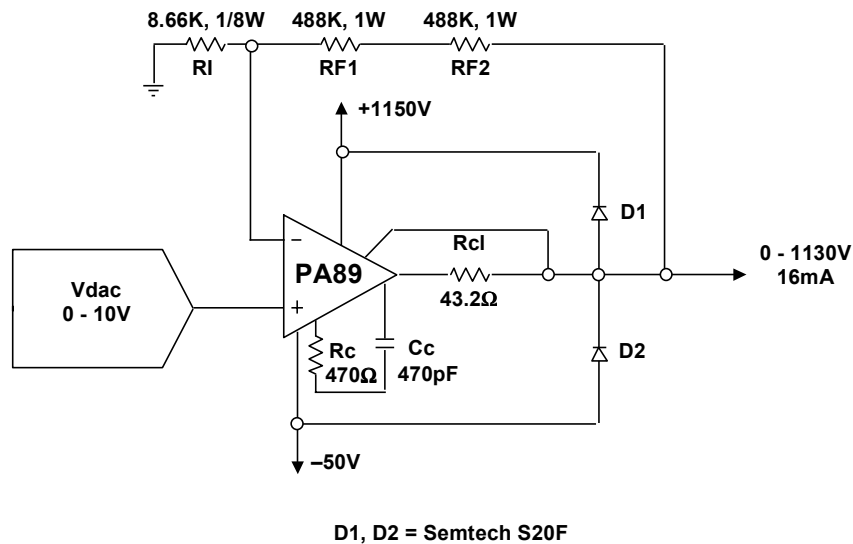
Ref. AN7

DRIVEN GROUND



Often a test rack is located quite a distance away from the actual test head where the DUT is being excited, or where measurements are being made. When the equipment at the personality adapter or the test head dumps a significant amount of current into a ground return line, enough voltage may be developed between the personality adapter and the universal test station to contribute significant errors to whatever measurements are being made. One way to solve this problem is to eliminate current flow in the ground line. This circuit accomplishes that feat by taking the reference ground from the universal test station and running a "ground sense" line over the personality adapter. This line is now used as a reference voltage input to a unity gain follower — in this case the PA01. The PA01 is used to generate a "remote ground." Now the ground current from the DUT or remote test equipment is dumped into the output of the PA01 where it is returned to one of the remote supply lines. The 1-10 ohm series resistor is used to keep power dissipation outside of the amplifier and have it dissipated in the resistor instead. Its value should be chosen such that the $I_{max} \text{ (ground current)} \times R_s = V_o \text{ max of the PA01}$.

HIGH VOLTAGE PPS



This high voltage programmable power supply utilizes the full voltage capability of the PA89. It uses asymmetrical power supplies to eliminate the necessity for biasing up the front end input DAC voltage to comply with common mode voltage requirements of the PA89, as well as providing adequate voltage headroom at the output so it can swing down to zero.

Although the PA89 can be used single supply, it ends up requiring large value resistors and high wattage resistors to bias the front end to comply with the input common mode voltage specification of $\pm V_s/2$. The output would only be guaranteed to swing within 20 volts of ground. Asymmetrical power supplies, as discussed earlier, eliminate both of these problems.

With the current limit set at 16mA the PA89 can withstand a fault condition of a short to ground on the output by using an Apex HS06 heatsink, a TW05 thermal washer, and in a 25°C ambient environment, free air convection cooling.

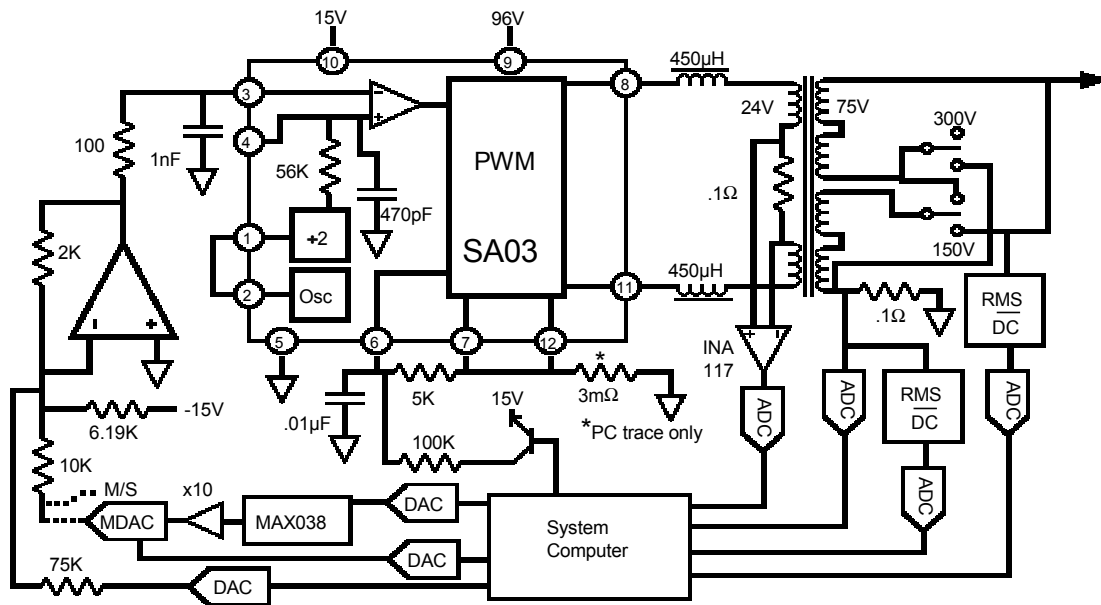
Although the PA89 generally works at low currents (<60mA), power dissipation is still a major design consideration due to the high voltage (remember $P = V \times I$).

As a high voltage amplifier the PA89 does present some unusual design considerations. The following is a quick check list of support components requiring special attention:

- 1) C_c —Compensation capacitor will see nearly the full supply voltage. In this case 1200V. Because of corona effects and partial discharge, this capacitor must be rated at twice the total supply voltage. Lower ratings can cause amplifier destruction.
- 2) R_F1 and R_F2 —Feedback resistors must be selected for power dissipation, voltage coefficient of resistance, and voltage breakdown rating.
- 3) D1 and D2—Flyback diodes must have a peak inverse voltage rating of the total supply voltage. Here we need a 1200V PIV rating minimum.

Expandable AC PPS

150/300V 47/440Hz 750W



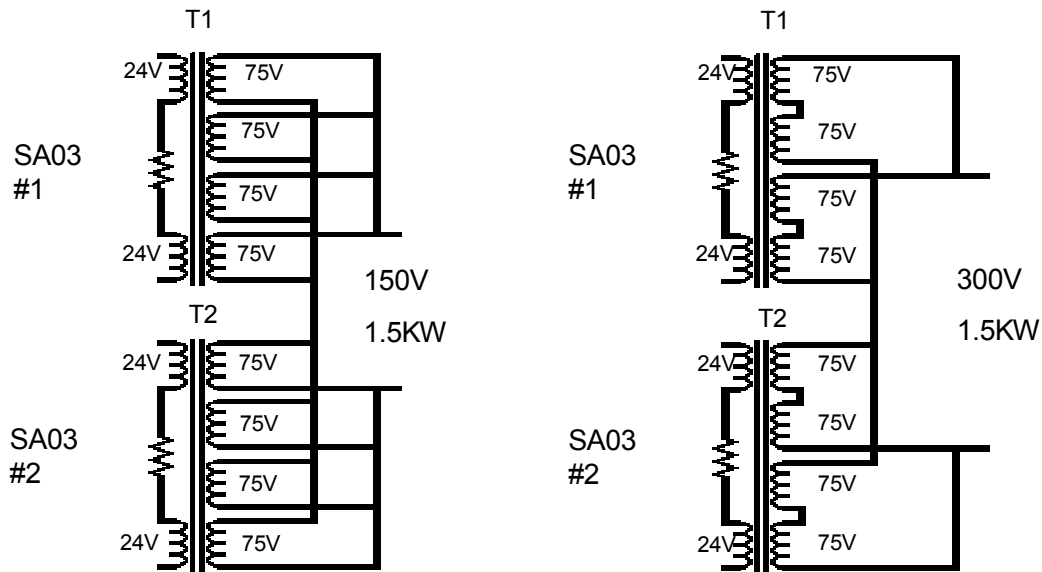
In local terms this SA03 is running open loop but overall operation is closed loop by virtue of the system computer monitoring performance and making adjustments per calibration tables and correction algorithms.

The MAX038 waveform generator 1Vpk is stepped up to 10Vpk going into the multiplying DAC. The summing amplifier is scaled for maximum peak output of 2V and is offset about 5V. The scaling for the DC correction signal is about $\pm 250\text{mV}$. The AC signal jumper allows master or slave operation of the module.

First order theory (only) dictates the power transformer should have more than enough inductance to do all the filtering. Cores used for low frequency power do not work well at all with 22KHz square waves, so some filtering is required. Using 450µH sets the pole at 435HZ and will keep 22KHz ripple current below 1.2Apk. This may need adjustment depending on the specific power transformer. The split primary allows current monitor signals containing very little AC common mode voltage.

Versions of this circuit with out programmable frequency have replaced variacs to increase voltage change speed thereby increasing value of the ATE. Another version uses step a down transformer testing very high current circuit breakers.

AC PPS Expansion

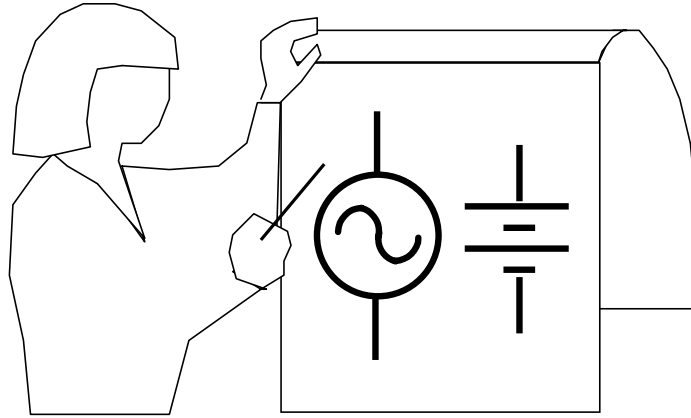


Yes, there really was a reason for four secondaries in the previous slide. With a slave module importing the AC signal from the master the two amplifiers will be in phase at the signal frequency even though they may not be in phase at the switching frequency.

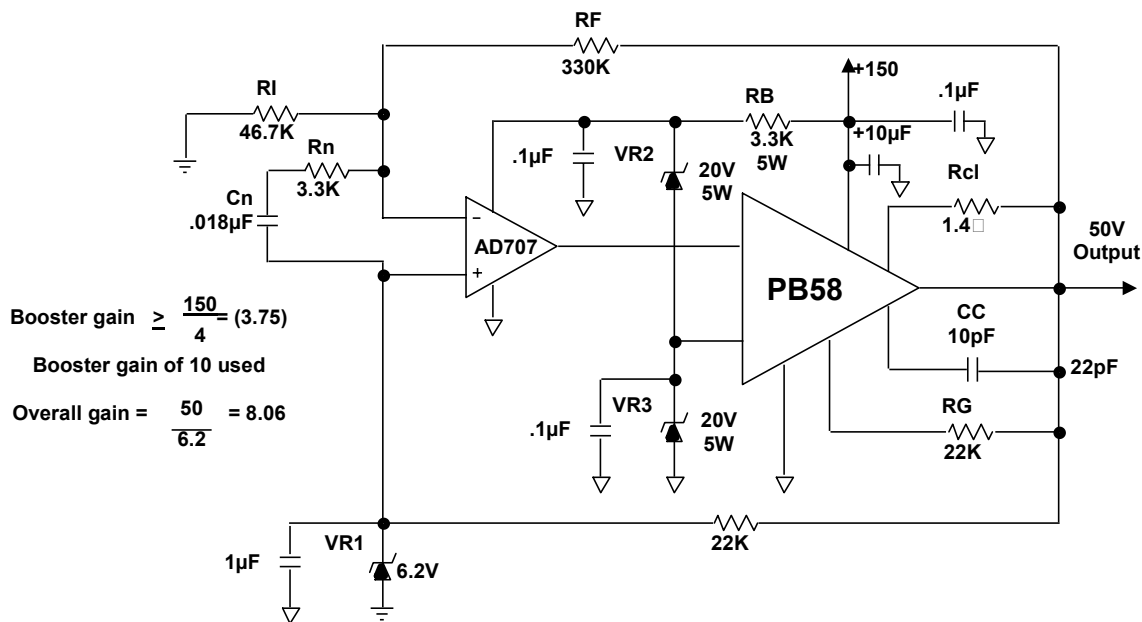
Power doubling is achieved by adding at the transformer stage rather than actually paralleling the PWM amplifiers. Frequency and magnitude are controlled by the master only, but the slave does use its own DC correction loop. Shown here are basic hoop-up for two voltage ranges with 1.5KW power capability.

The master/slave approach allows interchangeable modules in 750W and 1500W test systems.

SOURCES



VOLTAGE REGULATOR WITH PB58

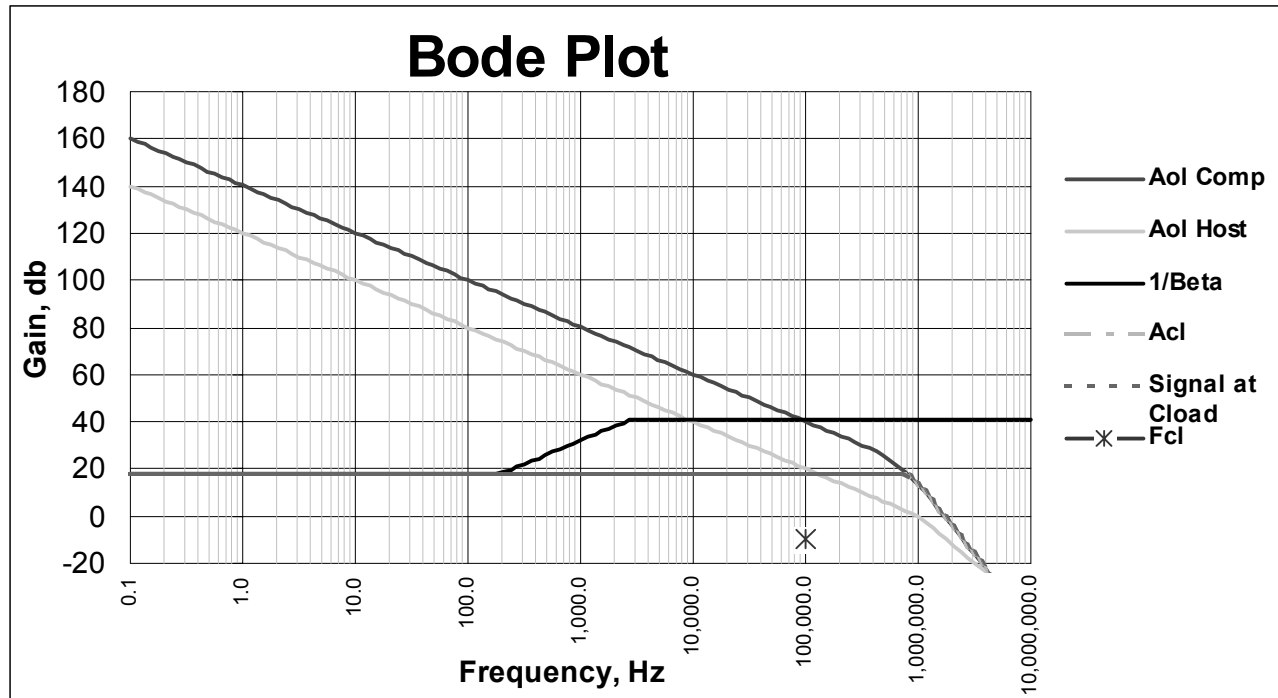


At first this may not seem to be the least costly approach to voltage regulator design. However, there is no packaged solution to regulating 150 volts down to 50 volts while being able to provide up to 500 mA (PB58 is rated up to 2A, but SOA limits us to 500 mA in this application). This regulator has both good source and good sink regulation characteristics.

This application does serve well to illustrate PB58 design techniques, and some of the limitations to be aware of. For instance, in normal applications the negative supply of PB58 must be 15 volts more negative than ground. In this application we have created a quasi-ground at the junction of VR2 and VR3 which meets this requirement. VR2 and VR3 also provide regulated supply voltage for the driver op amp.

The reference zener source is derived from the output of the regulator to improve supply rejection. The overall gain is whatever is necessary to multiply the 6.2 volt reference VR1, up to the required output voltage. In this case a gain of 8.06 for a 50 volt output. In the next few slides, we'll discuss stability considerations in the booster application.

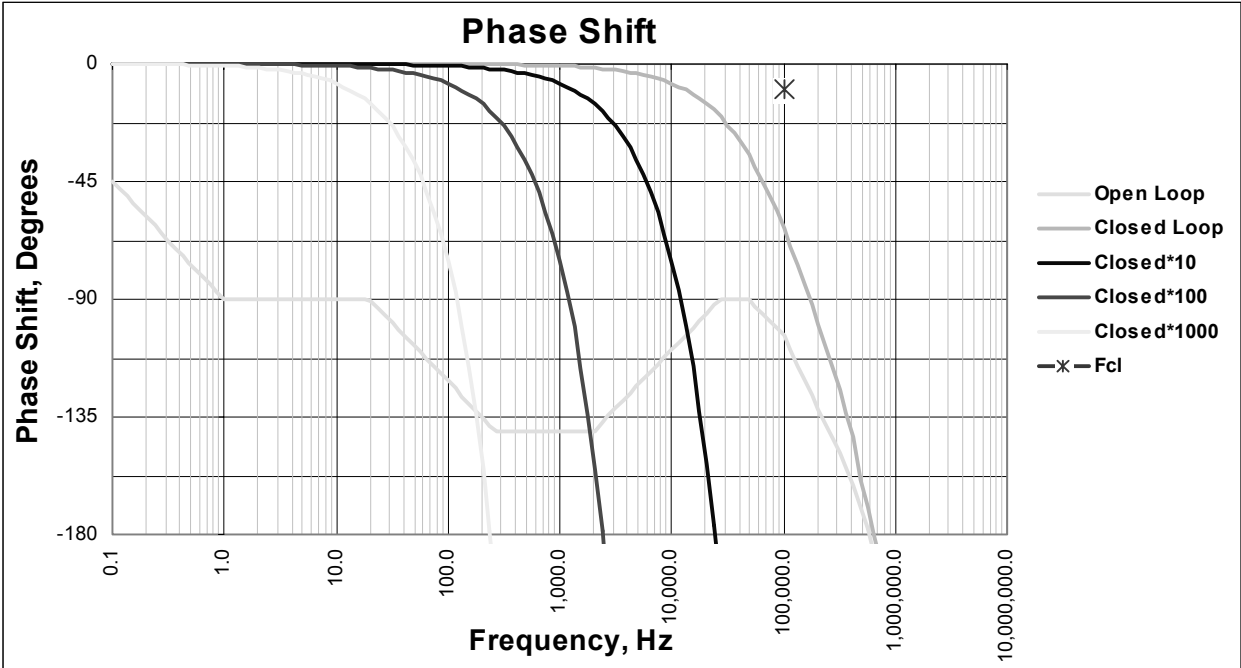
COMPOSITE MAGNITUDE PLOT



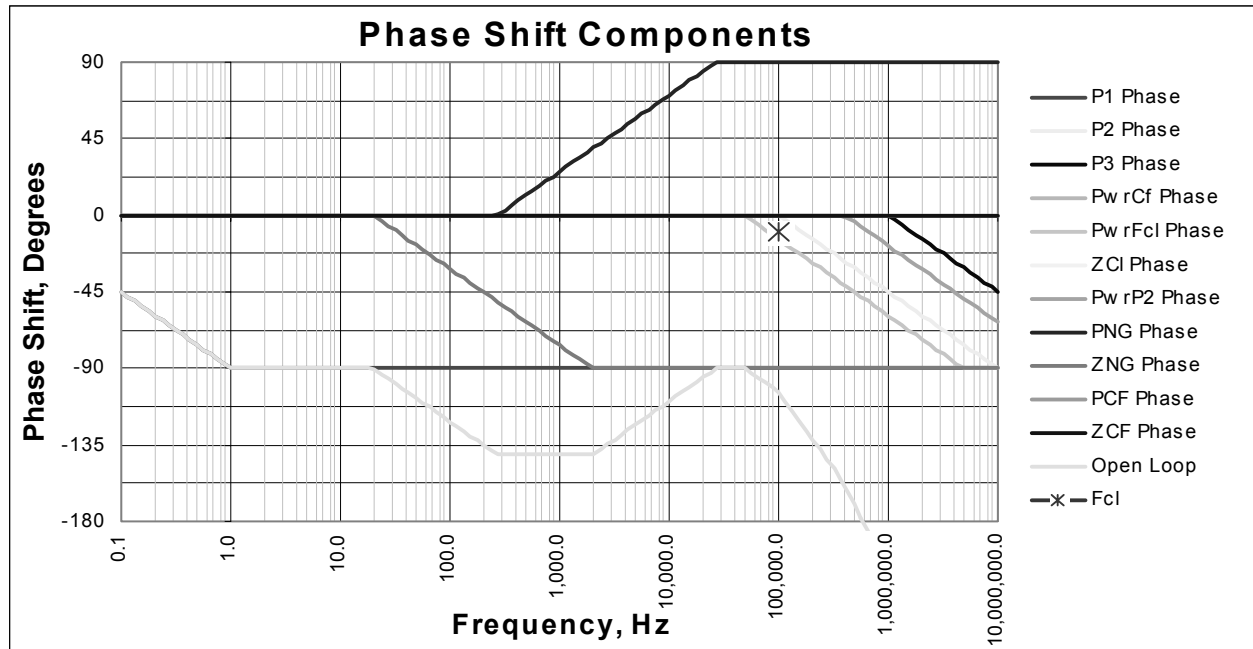
This circuit is not battling capacitive loading or inductance in the feedback path and each part of the composite would be stable on its own but the composite open loop gain reaches a slope of -60db per decade before crossing 0db.

While a DC gain of 100 (A short in place of C_n) would have made the circuit stable, the DC errors due to offset and drift would have been objectionable. Including C_n keeps DC gain at the desired level and produces a stable circuit.

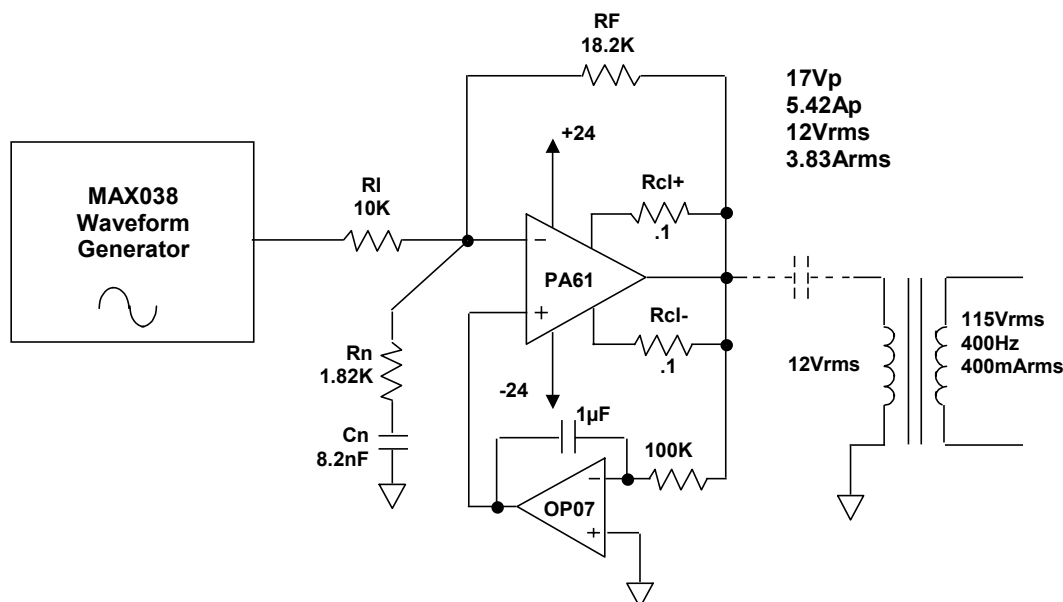
COMPOSITE OPEN LOOP PHASE PLOT



COMPOSITE OPEN LOOP PHASE PLOT



400 Hz SERVO SUPPLY



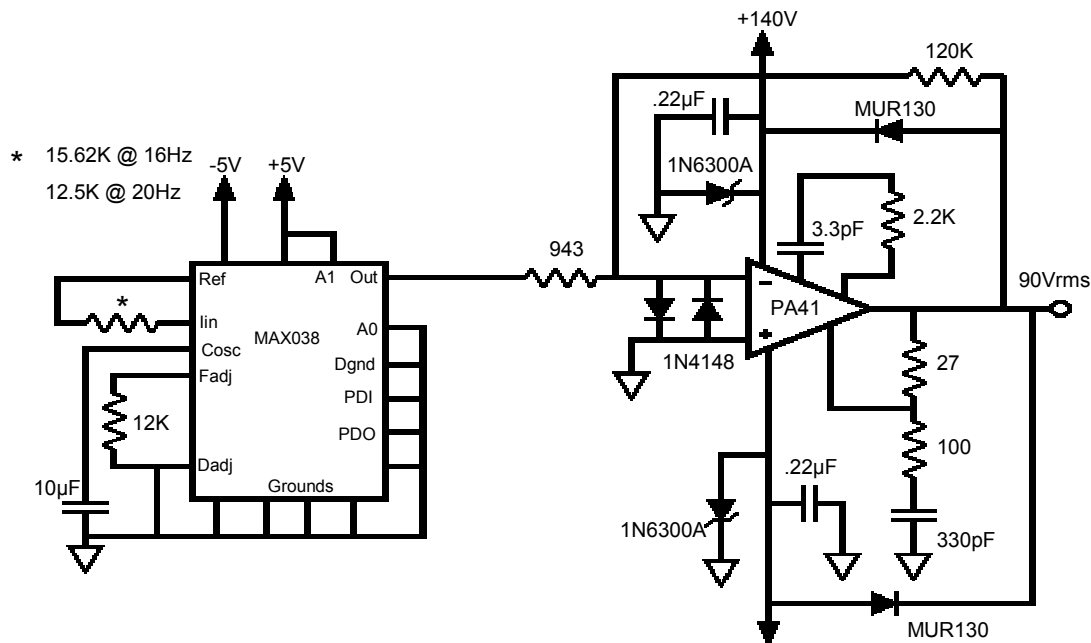
This 400Hz servo supply uses a separate oscillator to maintain oscillator stability under varying load conditions. The PA61 provides a gain of 1.8 to match the output of the industry standard 8038 waveform generator IC to the primary of a 12V to 115V step-up transformer.

The input R-C network is selected to provide unconditional stability on the PA61 with a phase margin of 45° in the 100Hz to 3kHz region. Phase margin increases to 90° at the 100kHz small signal bandwidth of this circuit. This extra phase margin allows for parasitic cable capacitance and/or capacitive loading on the output of the PA61 with guaranteed stability. The capacitor is selected for a corner frequency of 10KHz since this is well away from the 400Hz signal yet low enough to control any stability problems.

Note that the power supply is set to a value just large enough to accommodate the signal amplitude plus the amplifier's worst case output voltage swing specification. The use of minimum power supply voltage minimizes dissipation and improves efficiency.

If AC coupling should lead to unmanageable size bipolar capacitors, use an integrating amplifier (OP07 in this example) to compensate for offset voltage.

LOW POWER TELEPHONE RING GENERATOR



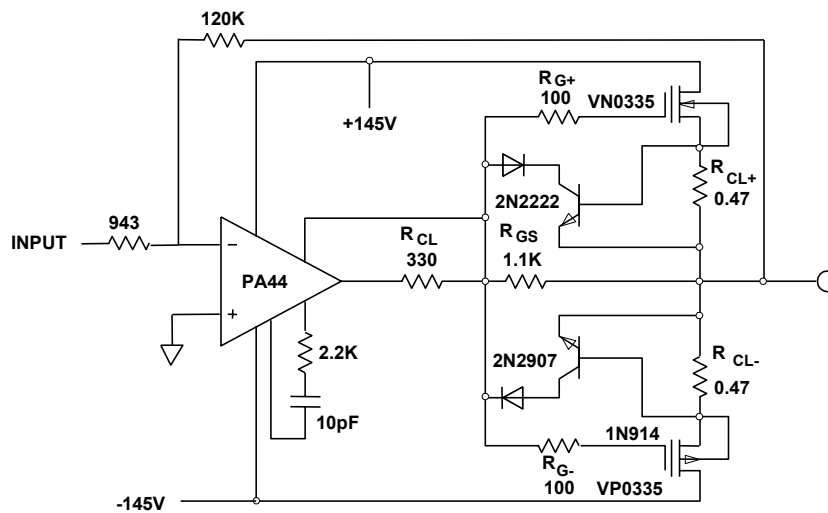
The MAX038 provides a 2Vp-p low distortion output signal. The PA41/42/44 is set for a gain of 127, boosting the overall output to 90Vrms. The recommended compensation for gains above 30 is used. If capacitive loading is at least 330pF at all times, the recommended snubber network may be omitted. The 27Ω resistor sets current limit to a nominal value of 111mA to insure peak currents of at least 88mA or 5.6W delivered to the load. This places total power dissipation at 3.8W, a level easily handled by the PA41 or PA42. Unless exotic heatsinking methods are employed, the PA44 is typically limited to about 2W. The 3.8W figure assumes resistive loading and ignores the possibility of a shorted output. Power levels must be reduced if reactive loads or shorted loads are to be encountered.

The MUR130 diodes shunt any energy on the output to the supply rails which are in turn protected against overvoltage transients by the 1N6300A transient voltage suppressors.

With the high voltage stage being a simple inverting circuit, it is very easy to scale the output down or up to 115Vrms. Summing in a DC offset could be done just as easily.

Ref. PA44 DATA SHEET

HIGH POWER TELEPHONE RING GENERATOR



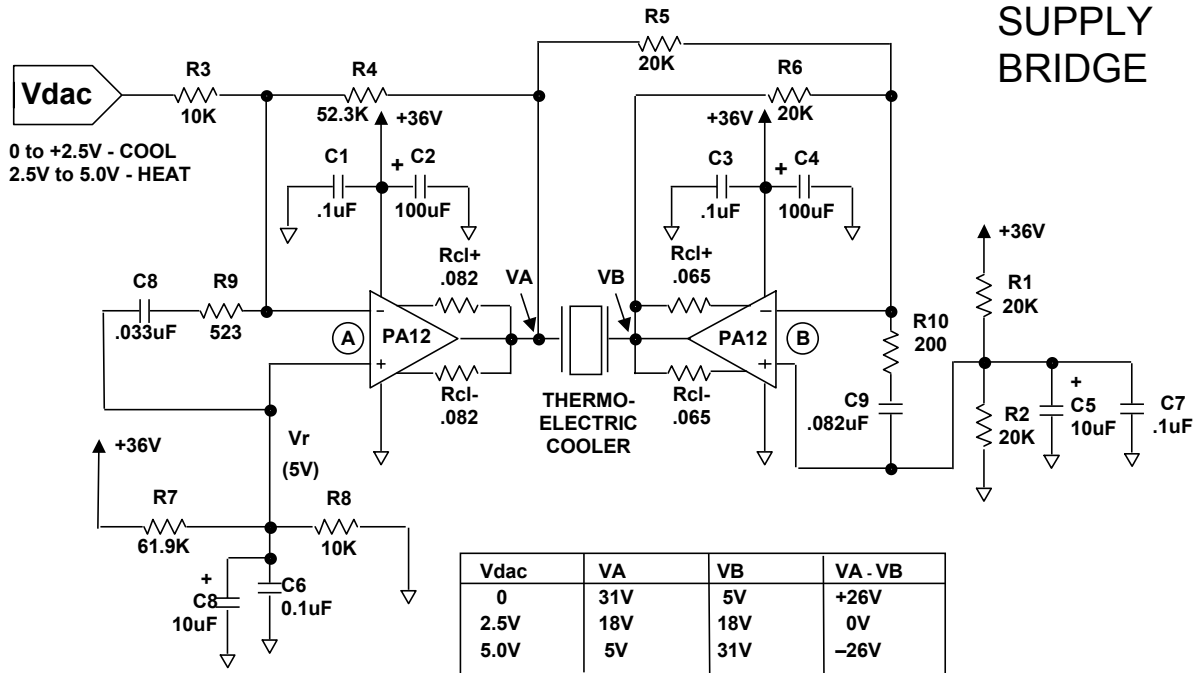
The signal source, protection requirements, and the basic operation shown here is the same as in the low power ring generator. Power supply bypassing and the use of a star grounding become much more important as power levels increase. To enable the ringing of more lines, external MOSFETs have been added. The choice of specific MOSFETs is determined entirely by current, voltage and power dissipation requirements. There are no radical differences among the different MOSFETs regarding threshold voltages or transconductance. Note that each MOSFET must be rated to handle the total supply voltage, 300 volts in this case.

Current limits have been set to a nominal of approximately 1.4A. Allowing for a 20% tolerance insures outputs of 1.1A pk or 0.78Arms. At 90Vrms, output power will be 70W and the peak dissipation requirement for each MOSFET will be 45W. At typical ringer frequencies the MOSFETs need to handle the 45W. Thermal averaging of the heatsink allows designing for 45W for the total amplifier or 22.5W per MOSFET if using multiple heatsinks.

The 330Ω current limit resistor sets the PA44 current limit to approximately 9mA. This current flowing across R_{GS} limits drive voltage on the MOSFETs to 10V. Worst case power dissipation in the PA44 will then be 1.3W due to output current plus .6W due to quiescent current totaling 1.9W. Unless you are willing to cut holes in the PC board to contact the bottom of the surface mount package with an air or liquid cooling system, this is about the limit. Typical operation will generate less than 1W in the op amp. Replacing R_{gs} with a bi-directional zener will allow a cooler running op amp at the cost of increased distortion.

THERMO-ELECTRIC COOLER

SINGLE
SUPPLY
BRIDGE



1. $V_{out} = V_A - V_B$
 $MAX V_{out} = +V_s - V_{satA} - V_{satB}$
 $= 36V - 5V - 5V = 26V_p$
2. $Gain = V_{outpp}/V_{inpp} = (V_A - V_B)_{pp} / V_{inpp}$
 $52V_{pp}/5V_{pp} = 10.4$

Gain = $2 R_4/R_3$ since we have a bridge configuration.

The voltage gain across the load is twice that of the master amplifier, A, since +1V out of the amplifier A yields -1V out of amplifier B, relative to the mid point power supply reference of +18V.

Therefore $R_4/R_3 = 5.2$

3. Offset
 $V_A - V_B = +V_s(2(1 + R_4/R_3) \frac{R_8}{R_7 + R_8} - 1) - 2(R_4/R_3)V_{dac}$

But when $V_{dac} = 0$ then $V_A - V_B = +26V$

Using $R_4/R_3 = 5.2$ and solving above yields $R_7 = 6.2 R_8$

Choosing $R_8 = 10K$ implies $R_7 = 61.9K$

4. Check for common mode voltage compliance:
 $5V$ meets the minimum common mode voltage spec.

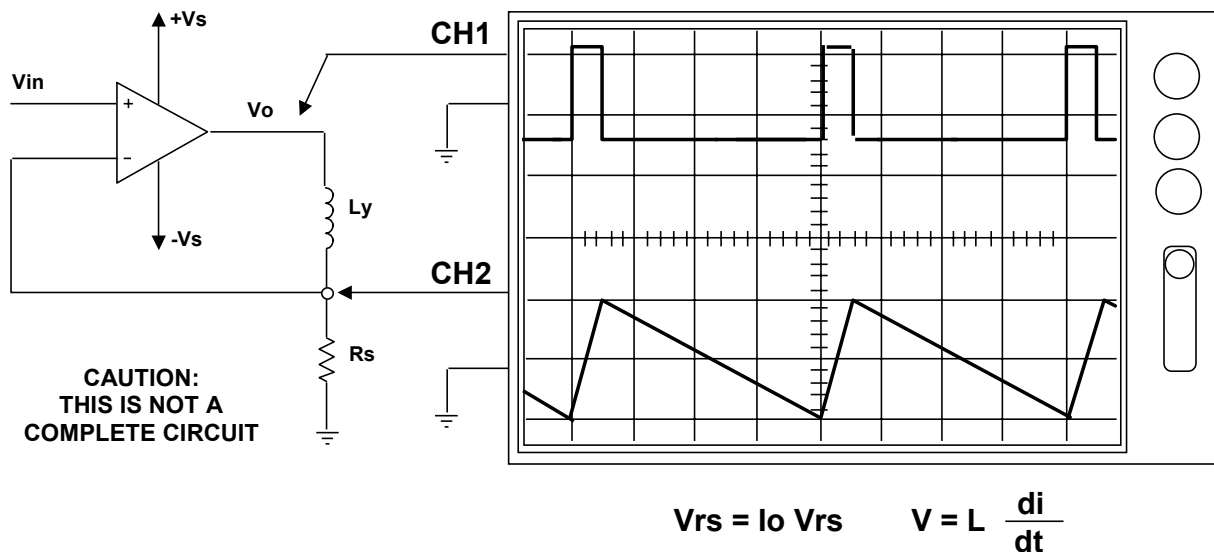
DEFLECTION

- Electromagnetic
- Electrostatic
- Dynamic Focus Control

High speed power op amps are ideal candidates for all types of deflection uses. High current, high speed models are ideal for electromagnetic deflection. Models with rapid slew rates and extended supply ranges allow rapid dl/dt of the yoke being driven. High voltage models are especially useful for electrostatic deflection and/or focus.

MAGNETIC DEFLECTION

AMPLIFIER SELECTION

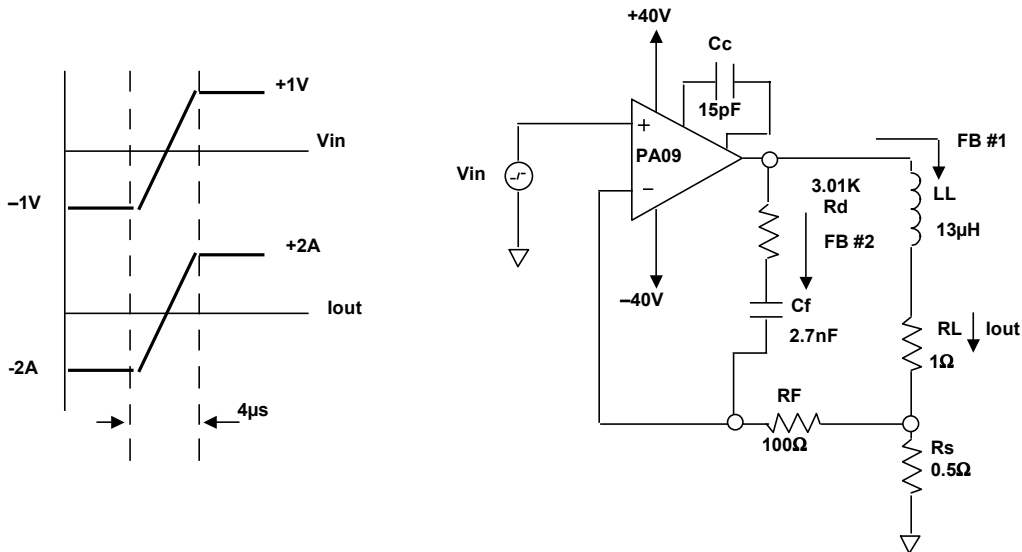


An amplifier selected for magnetic deflection must have an adequate slew rate and voltage rating to slew the current in the yoke fast enough.

These two considerations go hand in hand since the rate-of-change of current in the yoke is proportional to applied voltage. And the amplifier must slew to this applied voltage at least 10 times faster than the rate of change of current to achieve truly fast and accurate magnetic deflection.

Ref. AN5

ELECTRONIC DEFLECTION (V - I CIRCUIT)



AMPLIFIER SELECTION

STEP 1: VOLTAGE

$$V_{LL} = L_L \frac{dI_{p-p}}{dt}$$

$$V_{LL} = 13\mu H \frac{4A}{4\mu s} = 13V$$

$$V_s = V_{LL} + V_{RL} + V_{R_s} + V_{sat}$$

$$V_{s \text{ MIN}} = 13V + 2V + 1V + 8V$$

$$\text{Where: } V_{RL} = I_p R_L$$

$$V_{s \text{ MIN}} = 24V$$

$$V_{R_s} = I_p R_s$$

STEP 2: CURRENT From desired I_{out} , current must be 2A.

STEP 3: SPEED

A design rule of thumb for good performance is to select an amplifier with a minimum slew rate equal to 10 times faster than the desired current slew rate, faster will be better.

$$S.R. \text{ MIN} = \frac{V_{s \text{ MIN}}}{(.1) dt}$$

$$S.R. \text{ MIN} = \frac{24V}{(.1) (4\mu s)} = 60V/\mu s$$

STEP 4: PA09 and PA19 meet or exceed these requirements. PA09 is less expensive. Ref. AN5

PA09 Deflection Setup

STABILITY FOR INDUCTIVE LOADS

MODEL	PA09-150	Note/PBs	Rin	9999999999 Kohms	Estimated Closure Frequency =	3162.278 KHz
Rs		0.5 Ohms	Rf	0.1 Kohms	Suggested maximum bandwidth	177827.9 Hz
Lload		0.013 mH	Cf	2.7 nF	Estimated Closure Rate =	20.0 db/decade
Rload		1 Ohms	Rd	3.01 Kohms	Estimated Phase Margin =	45.63 Degrees
		Is this a Composite?	No			

Notes:

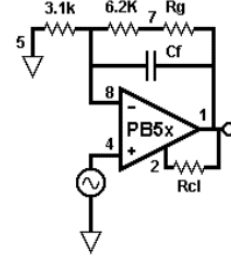
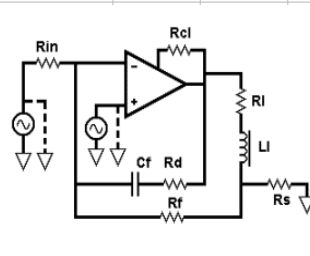
R-C Pole Calculator +:

3.01 Kohms	Rd Kohms	1.16509	AC gain db	30
20000 Hz	Rd Kohms	2.9	Rd Kohms	3.062278
2.6438 nF	Cf nF	2.081381		

28 Print Data, Bode
& Phase

29 Print Data, Bode,
Phase & Parts

Ri/(Ri+Rf)	1
Equiv Z @ Rs	0.5 Ohms
Requiv/(Ri+Requiv)	0.333333333
DC Beta	0.333333333
DC Gain	9.542425094 db
Zero R/L	18364.0319 Hz
Rin Rf	0.1 Kohms
Zero Rd/Cf	19583.48013 Hz
AC Gain	29.85520778 db
Zero Cross	177827.941 Hz



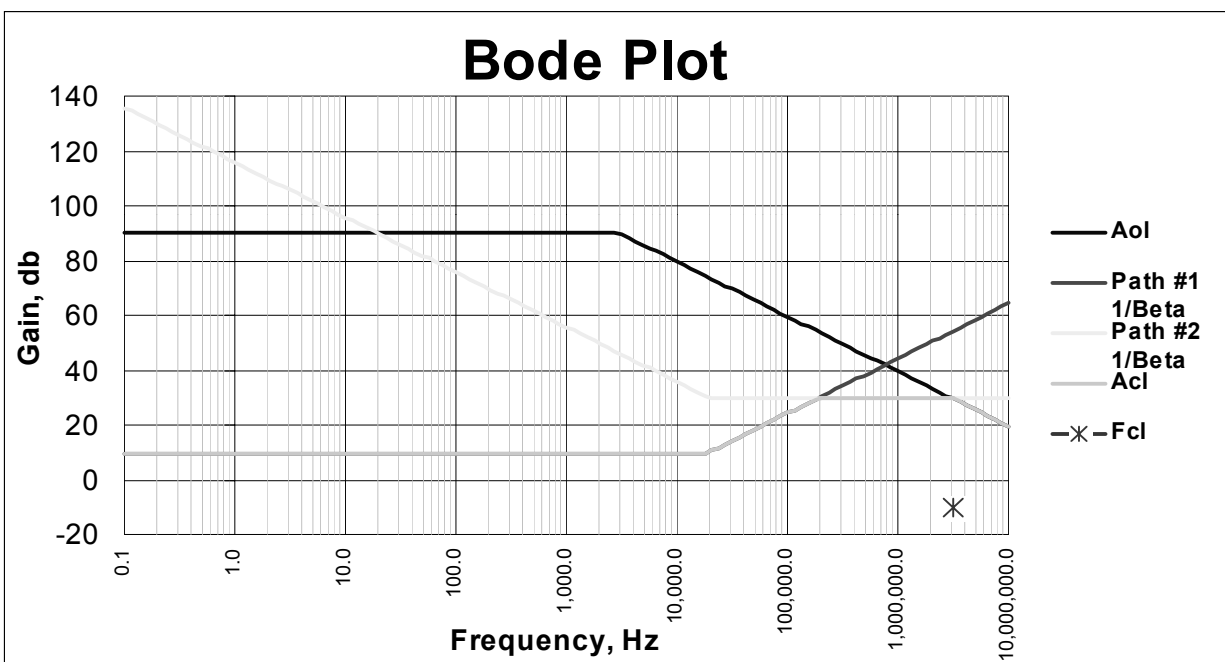
Set up the basic circuit in Power Design to see we have a 17 degree phase margin. Visualize the flat portion of feedback path #2 at about 30db. This is well below the intersection point and gives a nice round gain increase of 10x or 30 total. Estimate the line will cross the closed loop gain at about 200KHz.

Considering the inductor open and Cf shorted, AC gain will be roughly R_d/R_f . Put 3.01K and 20KHz (a decade below our estimated cross) in the R-C Pole Calculator. Enter 2.7nF for Cf.

We have good phase margin and an suggested maximum frequency of 178KHz. This suggestion is the lower of two criteria: The cross of the two feedback paths (the case here) or the frequency where loop gain is 20db (difference between open loop and closed loop gains).

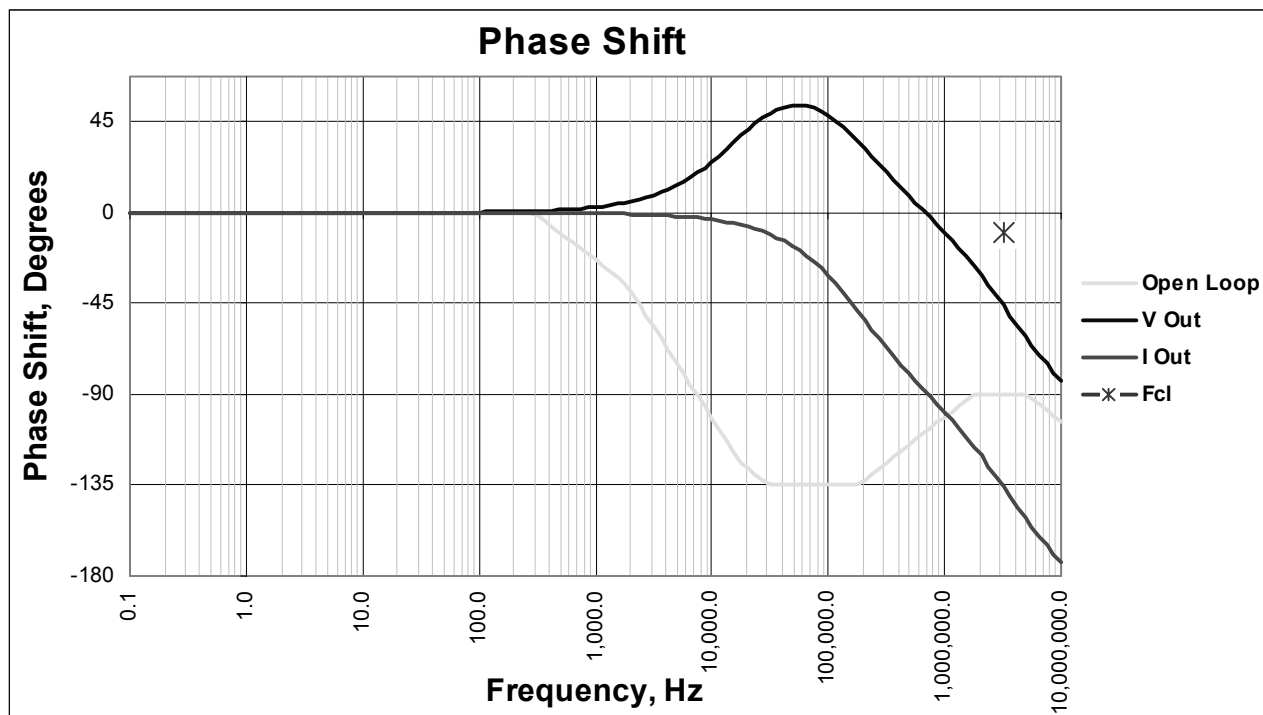
Ref. AN38

V – I MAGNITUDE PLOT FOR STABILITY



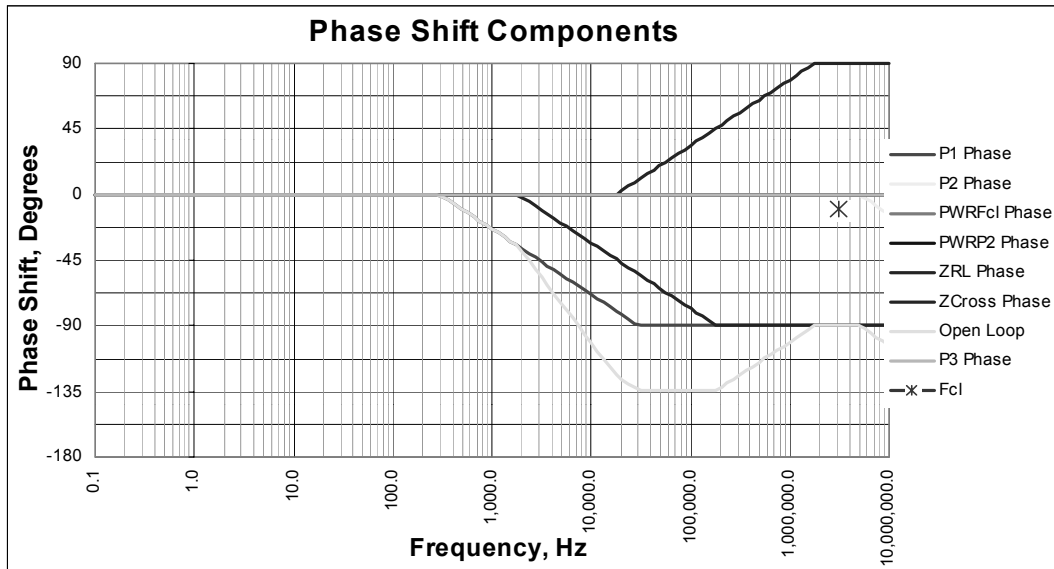
Ref. AN38

V - I OPEN LOOP PHASE PLOT FOR STABILITY



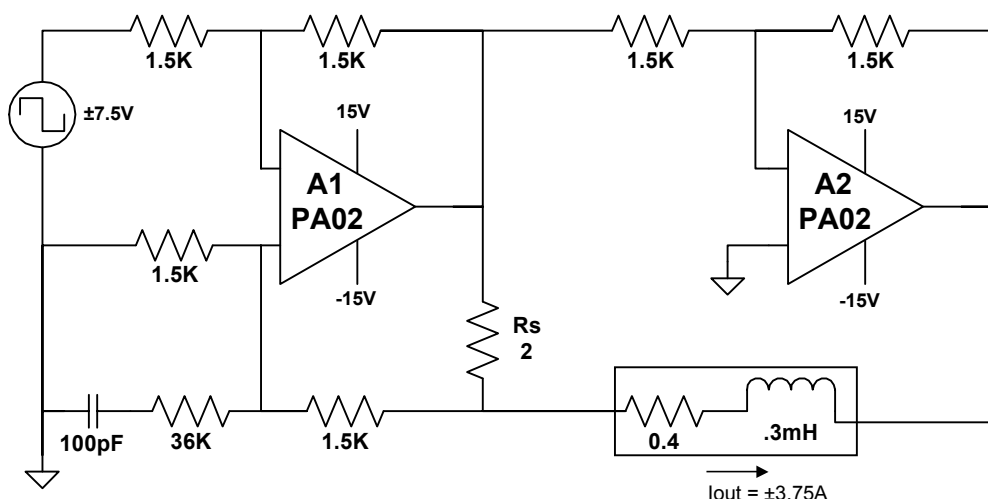
Ref. AN38

V-I Phase Components for Stability



Ref. AN38

ELECTRO-MAGNETIC DEFLECTION IMPROVED HOWLAND BRIDGE AMPLIFIER



MAXIMUM BEAM TRANSITION = 100μs

A1 is a Howland Current Pump, A2 provides a gain of -1 to drive the opposite terminal of the coil. A first glance, it might appear the choice of 2Ω for the sense resistor is quite large because the peak voltage drop across it is 7.5V, or half the supply voltage.

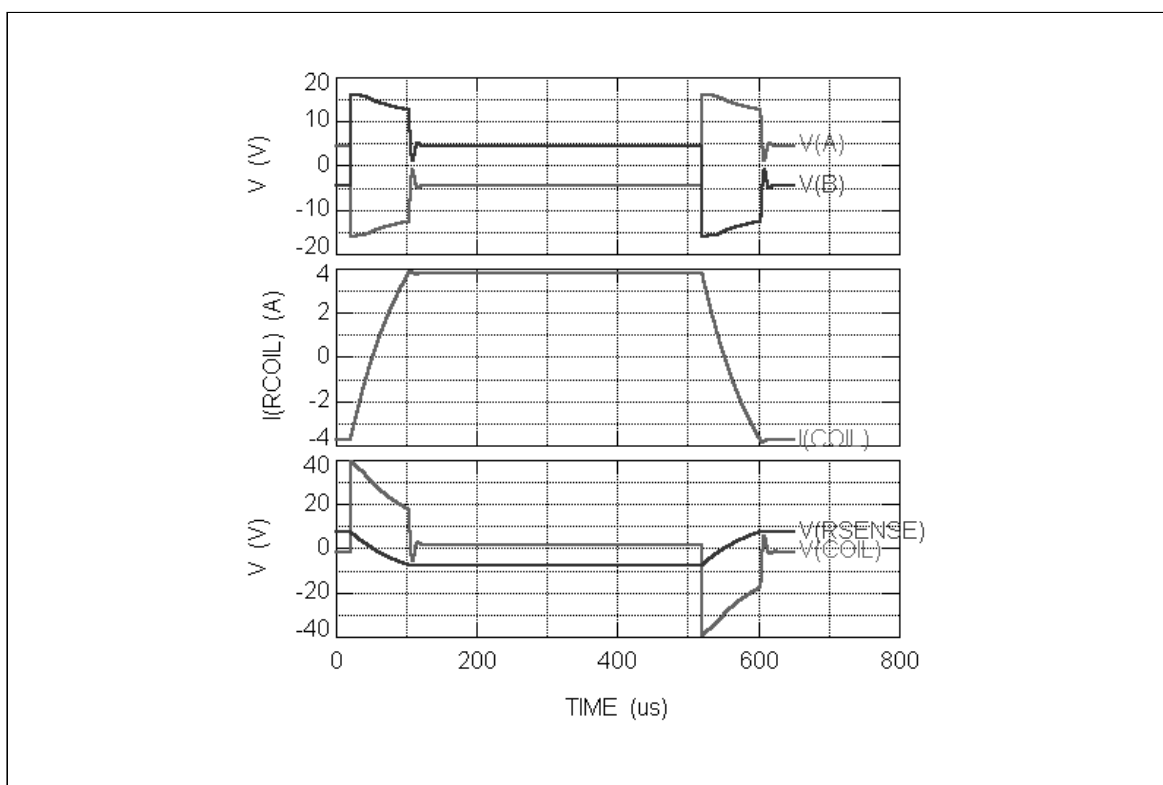
Voltage across the inductor required to move the beam is given by:

$$V_L = L * \Delta I / \Delta t \quad V_L = 300\mu H * 7.5A / 100\mu s = 22.5V$$

If one were to add to this the peak voltage drop across the coil resistance (1.5V) and the sense resistor (7.5V), it would be easy to assume a total swing of 31.5V or greater than 15V at 3.75A would be required of each amplifier.

Salvation for this problem lies in analyzing current flow direction.

Ref. AN5



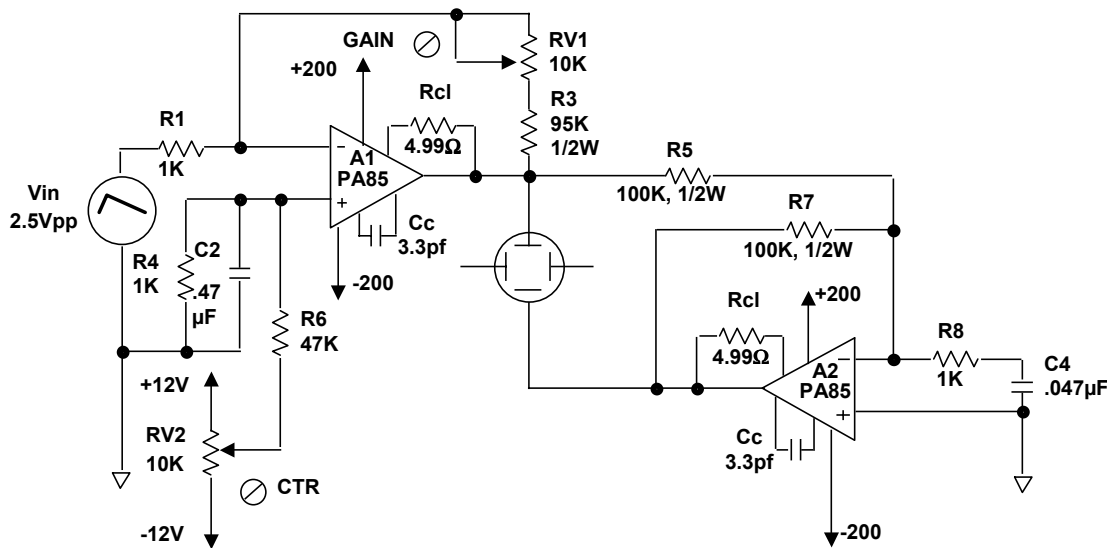
Check out the middle graph. Did you expect me to show you anything but a good current waveform? The main portion of the transition is complete in about 80 μ s and settles nicely.

In the top graph, we find surprise #1; both amplifiers are actually swinging OUTSIDE their supply rails. The “upside down” topology of the output transistors in the PA02 allows energy stored in the inductor to fly back, turning on the internal protection diodes. The result is peak voltages in the first portion of the transition greater than total supply.

In the bottom graph, we find surprise #2; stored energy in the inductor develops voltage across the sense resistor which ADDS to the op amp voltage until current crosses zero. In this manner, peak voltage across the coil is nearly 40V!

The seemingly large value of sense resistor did not kill us on voltage drive requirements and gives us two benefits: First, internal power dissipation is lower than with a smaller resistor. Secondly, with larger feedback signal levels, the amplifier closed loop gain is lower; loop gain is larger; fidelity of the current output is better; and voltage offset contributes a lower current offset error.

ELECTROSTATIC DEFLECTION AMPLIFIER



BALANCED TO MINIMIZE CRT DISTORTION

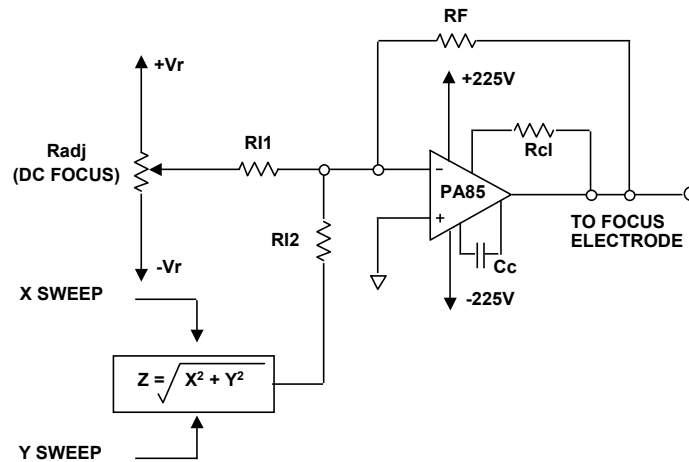
The PA85 was chosen for this application for its high voltage and high speed characteristics. Full bridge drive is utilized to provide a balanced drive to the CRT plate. Bridge drive is useful to reduce geometric distortion in electrostatic deflection applications.

A1 is the main amplifier operating at a gain of 100. This high gain permits minimal phase compensation for maximum speed performance.

Slave amplifier A2 is operated at a feedback factor of 1/2, that is an inverting unity gain. To get the same benefit of high speed that A1 enjoys due to the minimum compensation requirements, A2 is fooled into thinking it has a gain of 100 with the use of R8 and C4. This results in A2 having the same small signal bandwidth and high frequency gain as A1, which allows symmetrical bridge slew rates since A1 and A2 now use the same Cc compensation capacitor. This is the "Noise Gain Compensation" trick discussed earlier.

Ref. AN3

DYNAMIC FOCUSING



RAPID CORRECTION OF FOCUS FOR HIGH RESOLUTION DISPLAYS

In a flat screen display system the distance from the source of the beam to the screen changes as it deflects on the screen, from left to right, and from top to bottom. As a result of this a dynamic focus is required to keep the beam in focus, no matter where it is located on the screen.

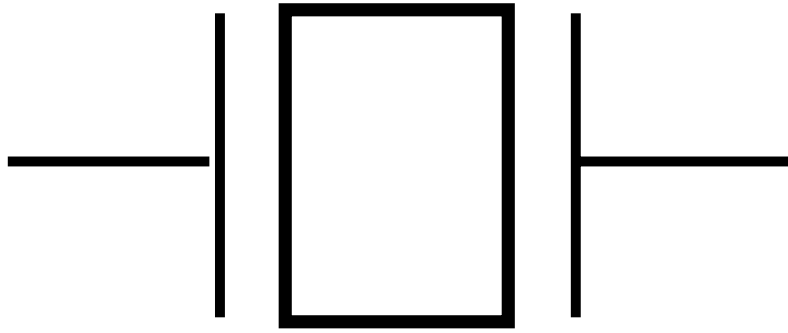
A normal CRT screen does not have to overcome these distance differences, since the distance from the source of the beam and the screen are the same no matter where you are on the screen, by virtue of the curvature of the screen.

To achieve electrostatic dynamic focus requires an amplifier with high voltage and high slew rate, as it is important to rapidly change the focus to keep the beam focused, regardless of screen position. The 450V, 1000V/μs slew rate PA85 is the ideal choice.

X and Y location sweep information is summed and scaled to provide the proper focus bias to the focus electrode. A DC offset sets the focus at the center of the screen.

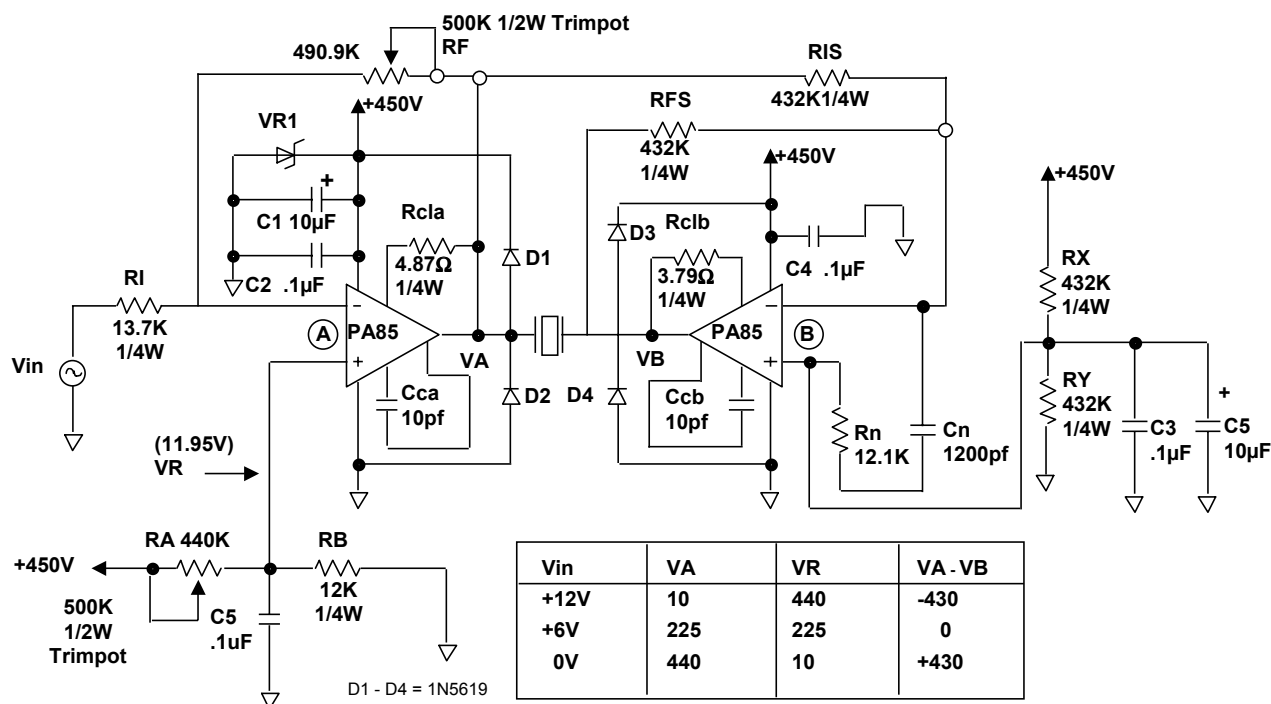
Don't forget the heatsinking on the PA85 as the high slew rate requires a high quiescent current which in combination with the high power supply voltage will result in 11.25W of quiescent power dissipation. A PA85 can cook, from a slew rate standpoint, and will literally cook without proper heatsinking!

PIEZO DRIVE APPLICATIONS



860 V_{pp} PIEZO DRIVE

SINGLE SUPPLY BRIDGE



1. $V_{out} = V_A - V_B$

$$\begin{aligned} \text{Max } V_{out} &= V_s - V_{satA} - V_{satB} \\ &= 450V - 10V - 10V = 430V \end{aligned}$$

2. $\text{Gain} = V_{outp-p} / V_{inp-p} = (V_A - V_B)_{p-p} / V_{inp-p}$

$$860V_{p-p} / 12V_{p-p} = 71.67$$

Gain = $2 R_F / R_I$ since we have a bridge configuration. That is the voltage gain across the load is twice that of the master amplifier, A, since +1V out of amplifier A yields -1V out of amplifier B, relative to the mid point power supply reference of +225V.

Therefore $R_F / R_I = 71.67 / 2 = 35.833$.

3. Offset:

$$V_A - V_B = V_s \left(2 \left(1 + \frac{R_F}{R_I} \right) \left(\frac{R_B}{R_A + R_B} \right) - 1 \right) - 2 \left(\frac{R_F}{R_I} \right) V_{in}$$

When $V_{in} = 0$ then $V_A - V_B = +430V$

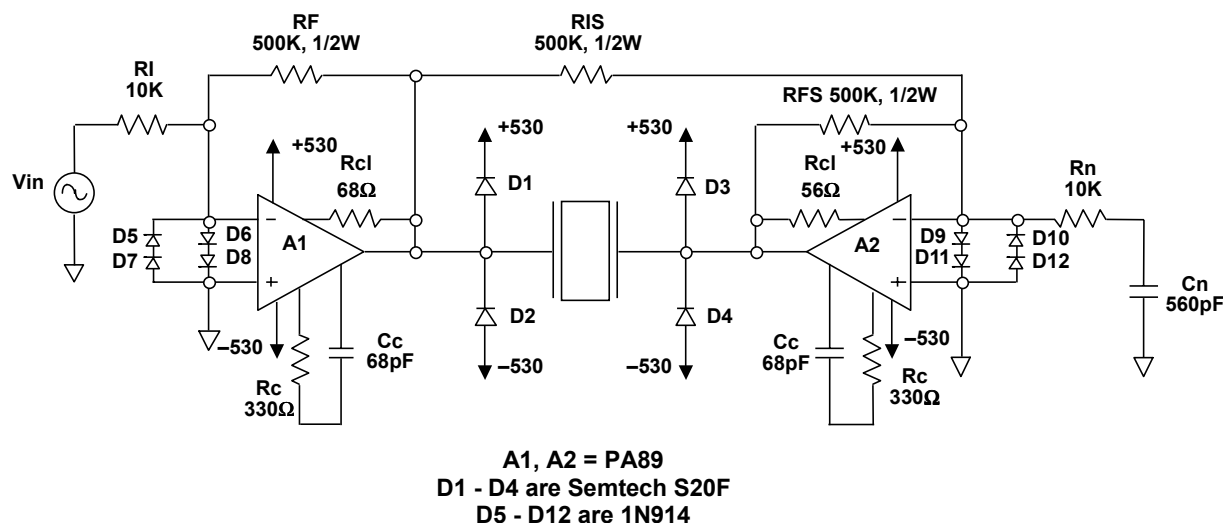
Using $R_F / R_I = 35.833$ and solving above yields $R_A = 36.669 R_B$

Choosing $R_B = 12K$ implies $R_A = 440K$.

4. Check for common mode voltage compliance: $11.95V > 10V$; OK.

Ref. AN25

+/- 1000V PIEZO BRIDGE



Piezo users appear to never have enough voltage. As soon as it was introduced the PA89 found its way into bridge circuits to drive piezos at +/-1000V and beyond.

In this application we use the dual supply bridge configuration to deliver up to almost twice the supply voltage of 530V across the load. A1 operates in a gain of 50 to translate the +/- 10V input to +/-500V out of A1. A2 then inverts this output to add an additional +/-500V across the Piezo to yield a net +/-1000V.

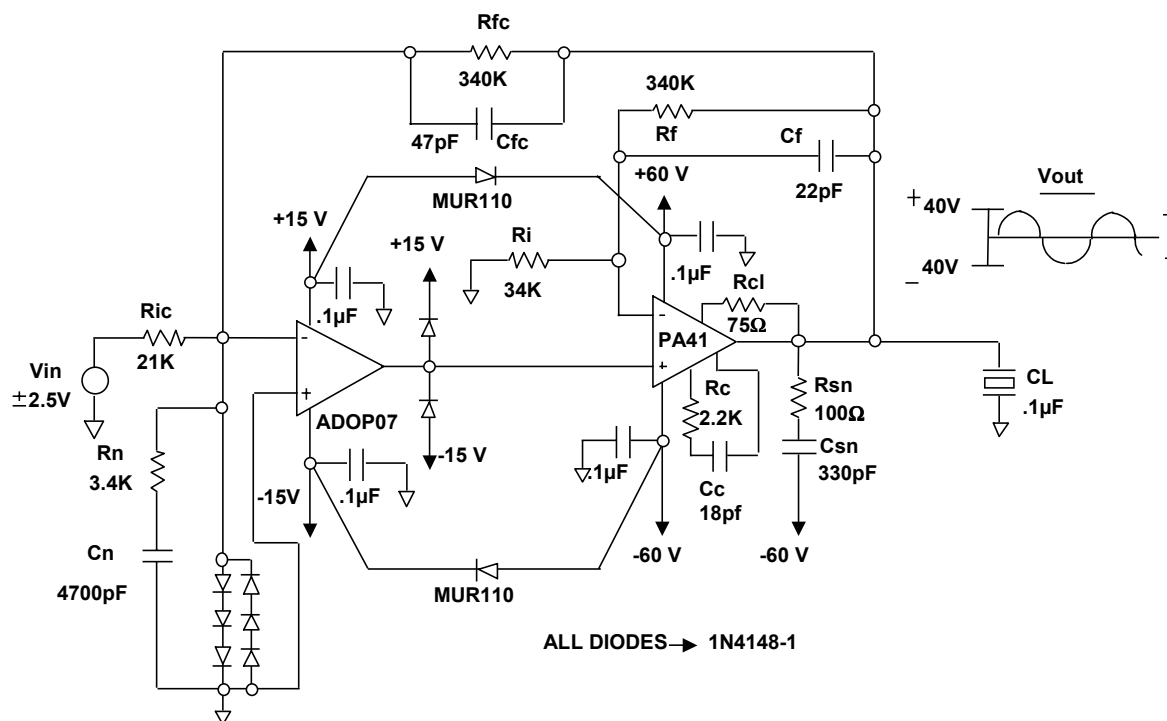
A2 uses noise gain compensation to allow its V_o/V_{in} transfer function to remain at -1, though its compensation capacitor C_c is set for a gain of 50. The noise gain will allow AC stability as well as a balanced bridge since both amplifiers are now compensated identically for the same slew rate.

Input protection diodes, output flyback diodes and proper component selection enhance reliability. Remember to select C_c capacitors with a voltage rating of at least 1100V, R_i , R_F , R_{IS} , and R_{FS} with proper power dissipation and voltage coefficient of resistance, and D1 - D4 with a PIV of at least 1100V.

As a final note remember to check the amplifiers for AC stability due to capacitive loading depending upon the capacitance of the piezo being driven.

Ref. AN25

PA41 COMPOSITE PZT DRIVE



This circuit is included as an example in Power Design.xls. It is different from most power op amps in that current limit from positive side to negative side does not match well at all.

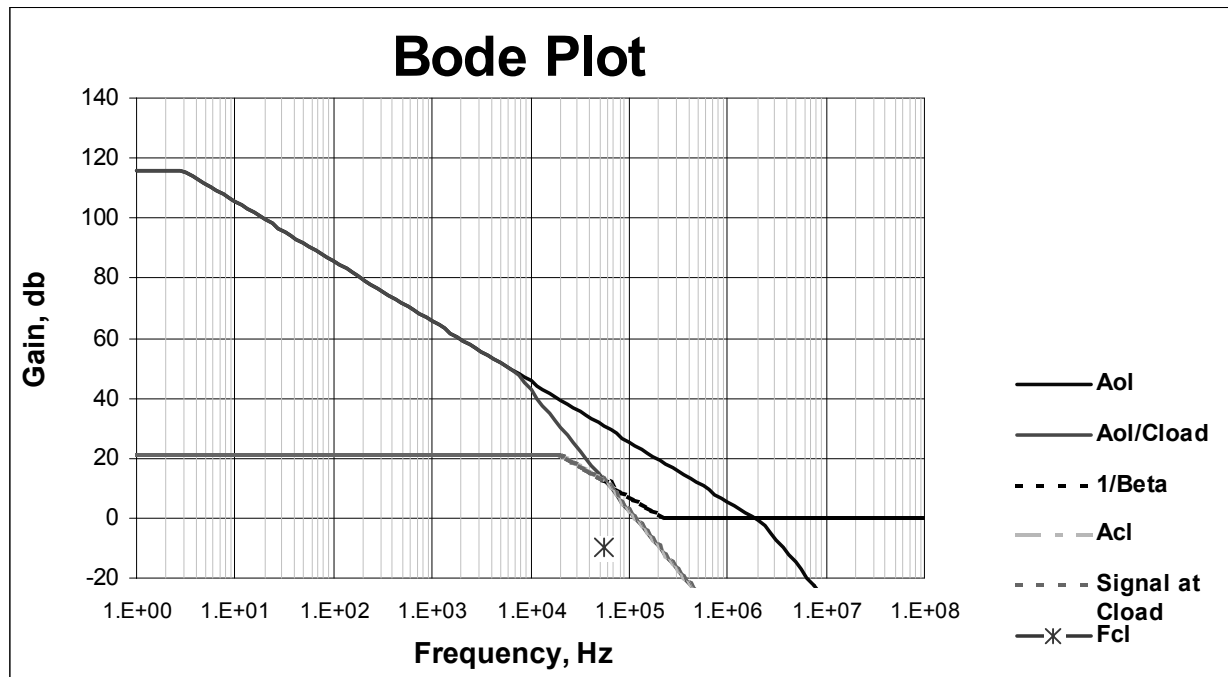
We will start by stabilizing the power stage, then the composite. Then we will examine current limit and frequency limitations imposed by this current limit.

1N4148 diodes on the input of the OP07 provide differential and common mode over voltage protection for transients through Cfc. Diodes on the output of the OP07 prevent over voltage transients that can occur through Cf, through the PA41 input protection diodes to the OP07 output through the PA41 internal input protection diodes.

Fast recovery diodes between pairs of supplies ensure that the PA41 input stage is protected from over voltage in the event the $\pm 15V$ supplies are up before the high voltage supplies.

Ref. AN19,AN25

POWER OP AMP MAGNITUDE PLOT

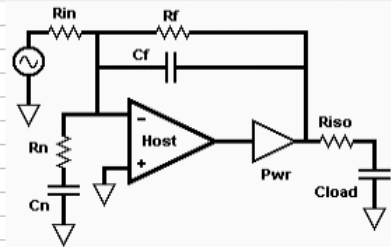


In any composite amplifier, make sure the power output stage is stable first. Any of the techniques we learned earlier can be used.

Ref. AN19,AN25

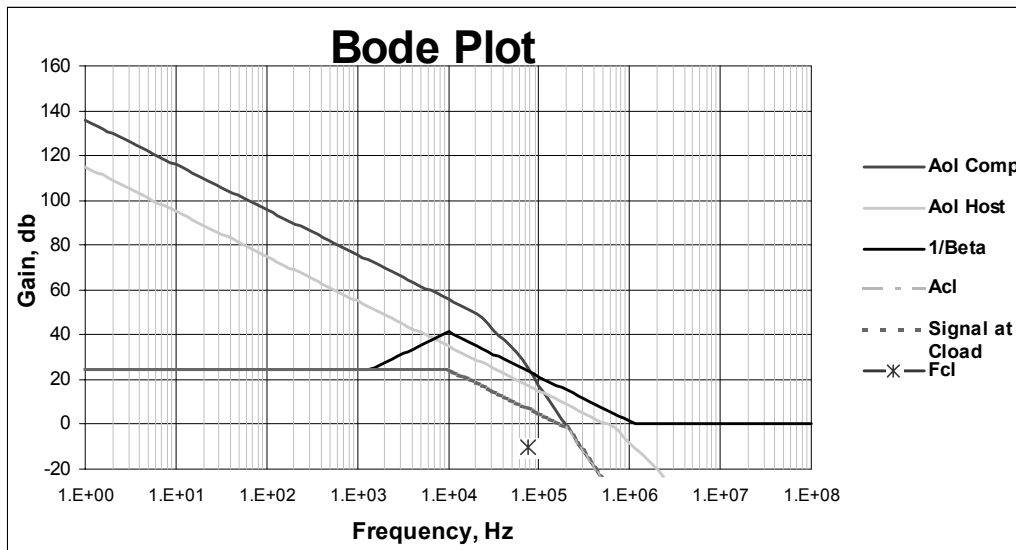
Composite Amplifier Set-up

Composite Circuits				38 Goto Main Circuit	
MODEL	OP07	READ ME		Estimated Closure Frequency =	74.98942 KHz
Aol =	135 db	Pole 1 =	0.1 Hz	Suggested maximum bandwidth	9.959633 KHz
Pole 2 =	7.00E+05 Hz	Pole 3 =	7.00E+06 Hz	Estimated Closure Rate =	40.0 db/decade
Rin	21 Kohms	Rn	3.4 Kohms	Estimated Phase Margin =	47.31884 Degrees
Rf	340 Kohms	Cn	4.7 nF		
Cf	47 pF	Using Look-Up data			
Notes:					
R-C Pole Calculator:					
9 Kohms	90 Kohms				
200 KHz	0.43 nF				
0.08842 nF	4.1125308 KHz				
1/Beta (DC)	24.7 db				
Noise Gain	16.7 db				
Pole Noise Gain	9.9596332 KHz				
Zero Noise Gain	1.460962 KHz				
Pole Cf/Rf	9.9596335 KHz				
Zero Rf/Cf	1167.1742 KHz				
Page Down for Plots.					
				30 Print Data, Bode & Phase	31 Print Data, Bode, Phase & Parts



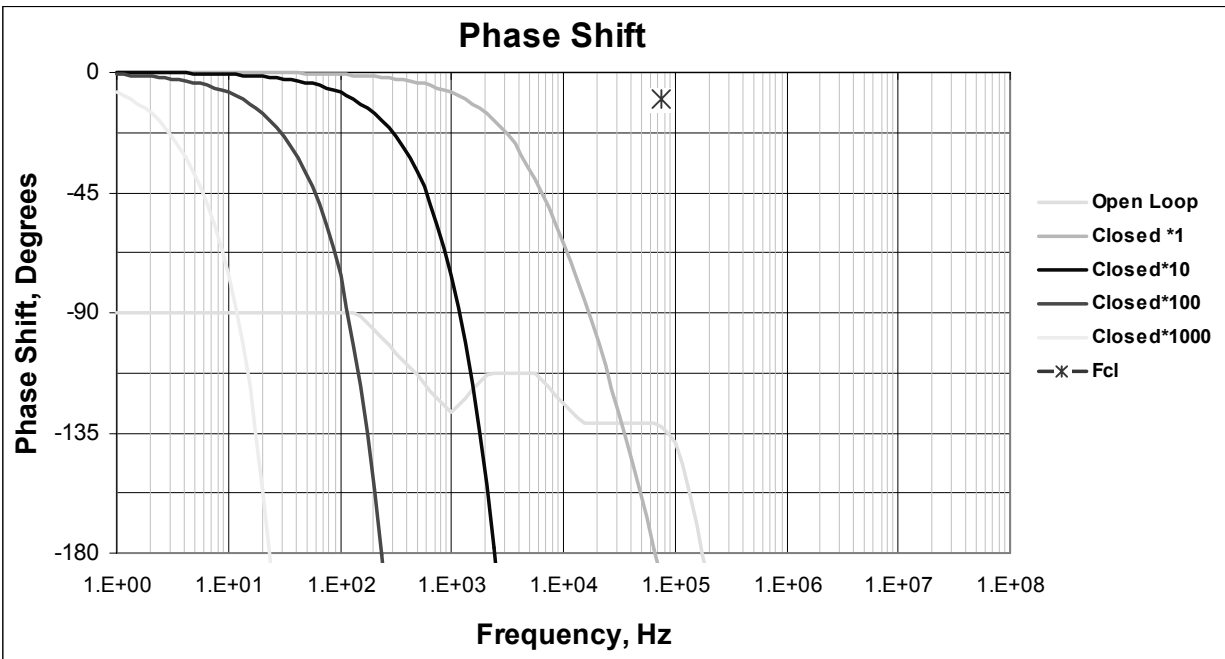
Ref. AN19,AN25,AN38

Composite Amplifier Magnitude Plot



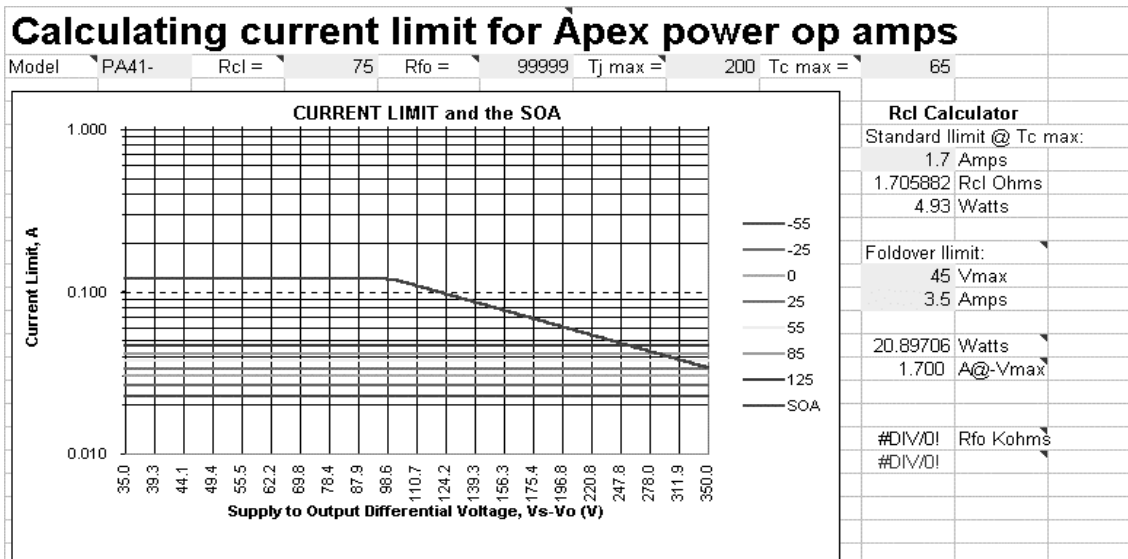
Ref. AN19,AN25,AN38

COMPOSITE AMPLIFIER OPEN LOOP PHASE PLOT



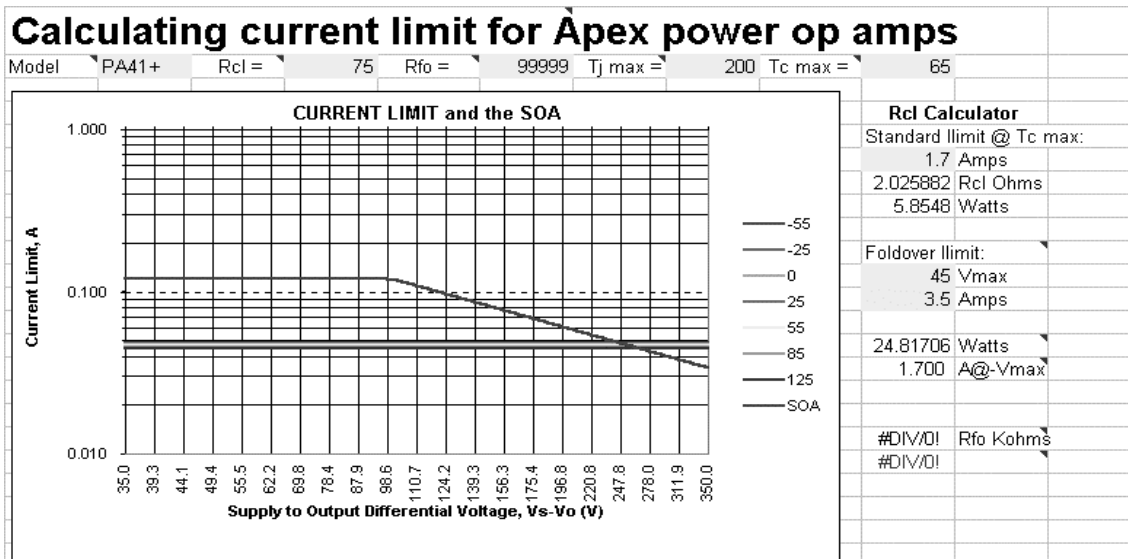
Ref. AN19,AN25,AN38

PA41 Negative Current Limit



If we can assume the PA41 never gets colder than 25°C, nominal current limit is 33mA. Again, thinking about 20% tolerance, we can count on 25mA output capability.

PA41 Positive Current Limit



Here we see the difference in limiting on the positive side. While this will not have an effect on driving our normal load because we will calculate this based on the lower negative limit, we will want to know nominal positive limit is about 47mA if any fault conditions must be tolerated.

PA41 Power Question Setup

Calculating Power Dissipation for Apex power op amps									
Model	PA41	Ta max =	30			Tj max=	150	Tc max=	85
Power for Sine Wave Outputs		Note/PA46							
Vs	60 Volts	Note/PA21,5,6							
Fmin	0.01 KHz	Note/PA04,05							
Fmax	10 KHz	Bridge ckt?							
Sig	81 Units	No							
Sig as ?	V p-p	Note/W							
Res	0 Ohms	# of Amps in parallel?							
Cap	0.1 uF	1							
Ind	0 mH								
Rcap	0 Ohms	Unipolar or Bipolar?							
Rind	0 Ohms	Bipolar							
Piq	0.192 Watts			32Results	33Results	34Results	35Results	37Define	36Results
Read Me								Sweep the	
Resonant Frequency =	503292.1 KHz					Max delta Tj =		Frequency	
At Fmax:	At Fmin:					120			
Xc hi =	159.1549	Xc =	159154.9			Max delta Tc =		65 View Last	
Xl hi =	6.28E-08	Xl =	6.28E-11			55		Frequency Sweep	
Notes:	Power Trial								

The amplifier selection, load and voltages have all been given. The only frequency that matters is the maximum (no current into a C load at DC). Our stability analysis suggested a maximum of about 10KHz (the Rf-Cf pole frequency).

Ref. AN37

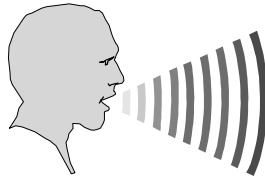
Speed is Limited by Iout

	At Fmin:	At Fmax:		At Fmin:	At Fmax:	
Z in Ohms	159154.94	159.15		Maximum AC Pint		
Phase angle	-90.00	-90.00		59.4	59.4	Vpk
RMS Amperes	0.0001799	0.1799368		42.002143	42.002143	Vrms
Peak Amperes	0.0002545	0.254469		0.0002639	0.2639072	Arms
RMS Volts	28.637825	28.637825		0.0110847	11.08467	Wrms
Peak Volts	40.5	40.5		6.966E-15	6.965E-09	Wtrue
RMS Power	0.005153	5.1529974		0.0142557	14.255742	Pin
Peak Power	0.010306	10.305995		Minimum HS:	5.45	°C/W
Power factor	0.000	0.000		Actual HS:	100	°C/W
Input power	0.01	9.72		Results in Tjmax =	391.78	°C
True power	0.00	0.00		Results in Tcmax =	327.35472	°C
Percent Efficiency =	2.55	51.99				
Vpk capability =	48.99	42.64				
Op amp internal dissipation:						
Input power	0.01	9.72		TOO *@&# HOT!!!!		
Dissipation RMS	0.01	9.72				
Dissipation Peak	0.02	17.77		CURRENT TOO HIGH!		
Total in heatsink	0.21	9.91				
WC watts & Rth	9.9118238	6.5		5.4489283	5.5067527	5.4489283

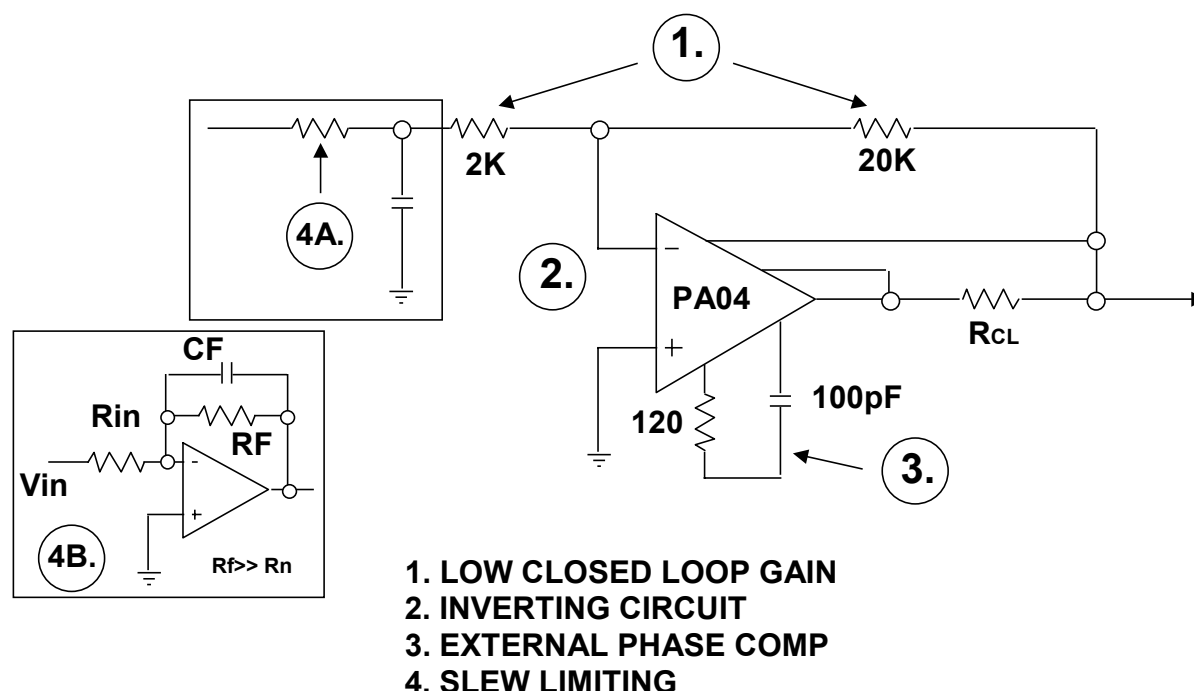
255mA would be required to drive the .1μF load at 10Kz! Notice the “CURRENT TOO HIGH!” flag at the lower right. This is based on data sheet maximum, not the current limit resistor used. Since this is 10x our capability, 1KHz will be the limit with a 75Ω current limit resistor. When this is plugged in, we will find normal operation with no heatsink is possible. To analyze fault conditions, find the lowest impedance to be encountered, assume the current limit (47mA in this case) is driven into the load and calculate the output voltage. Subtract this from the supply voltage, compare to the SOA of the amplifier and calculate a larger heatsink as required.

Ref. AN37

AUDIO



WIDE BAND - LOW DISTORTION DESIGN



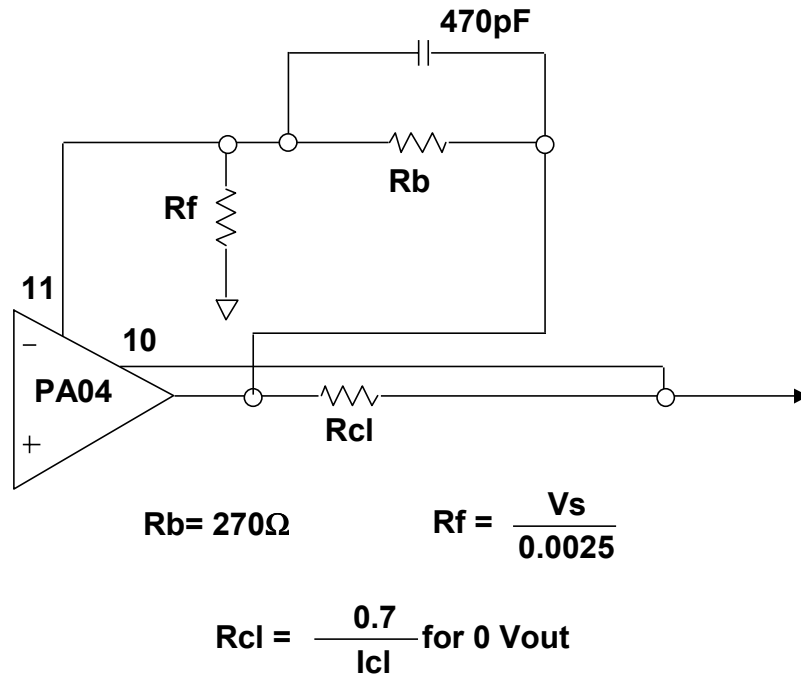
When audio or ATE applications demand the best in distortion and bandwidth, there are four basic rules to follow:

1. Low closed loop gain insures maximum reduction of distortion because of increased loop gain. However, the heavy negative feedback can cause transient response problems during rapid transitions (slew rate overload). Rule #4 will show how to solve the transient response problem.
2. The inverting configuration, by forcing both inputs to 0 (remember your basic op amp theory), eliminates common mode signals and the errors (read: nonlinearities) that they cause.
3. External phase compensation allows the designer to tailor the circuit to the minimum acceptable compensation. This increases high frequency loop gain to further reduce distortion, especially at high frequencies. Consider noise gain compensation to improve stability for low gain and small compensation capacitors.
4. Input slew rate limiting (4A) designed to keep input signal transitions within the slew rate limit of the amplifier will eliminate transient overload problems. 4B) You may use an integrator to accomplish this function, while R_F/R_I pre-amplifies the input signal to accommodate a low power stage gain. Then $C_f = V_{in}/R_{in} \cdot A_{cl} / SR$.

Ref. AN17

FOLD OVER CURRENT LIMITING FOR PA04

DOUBLES
I_{cl} AT V_o MAX



The four wire current limit of PA04 is easily adapted to foldover current limiting with the addition of two external resistors.

This effectively doubles current available at full output swing compared to current available at 0V_{out}.

This provides an extra margin of safety in audio applications.

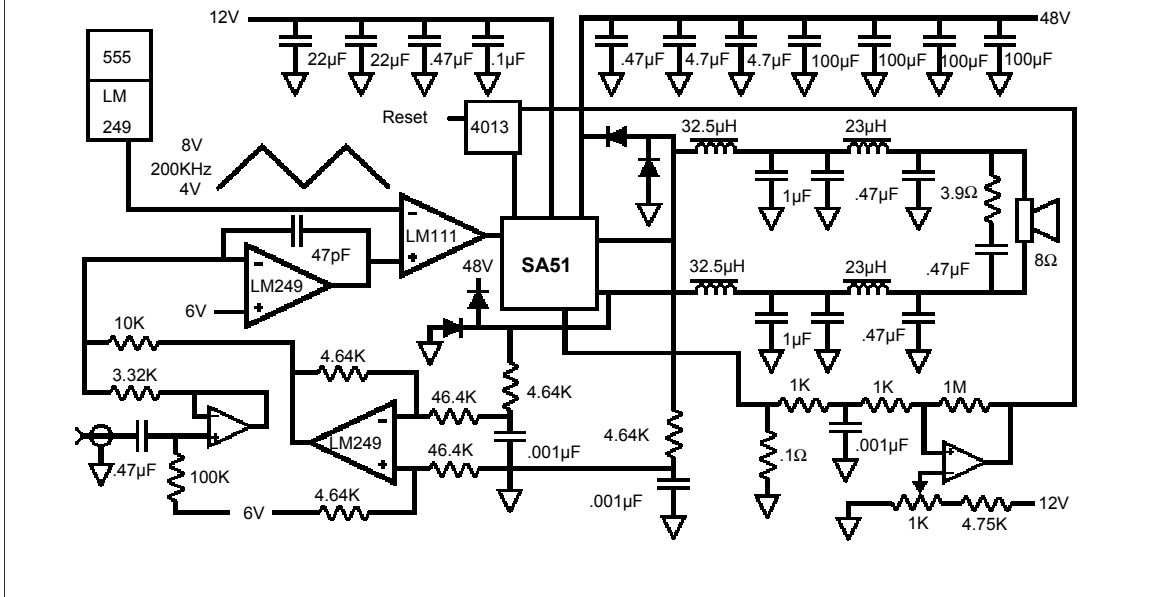
Ref. AN9

SA07 Aircraft Audio Amplifier

The differential voltage amplifier has two poles at about 23.5KHz, a gain of 1/20 and the output is referenced to 2.5V. The integrator amplifier is also referenced to 2.5V and scaled to 1Vrms inputs which are ground referenced.

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SA51 AUDIO AMPLIFIER



This class “D” audio amplifier is cost effective, cool running, good sounding and delivers up to 100W. Does any one know what this number would be if you bought the equipment as consumer audio gear?

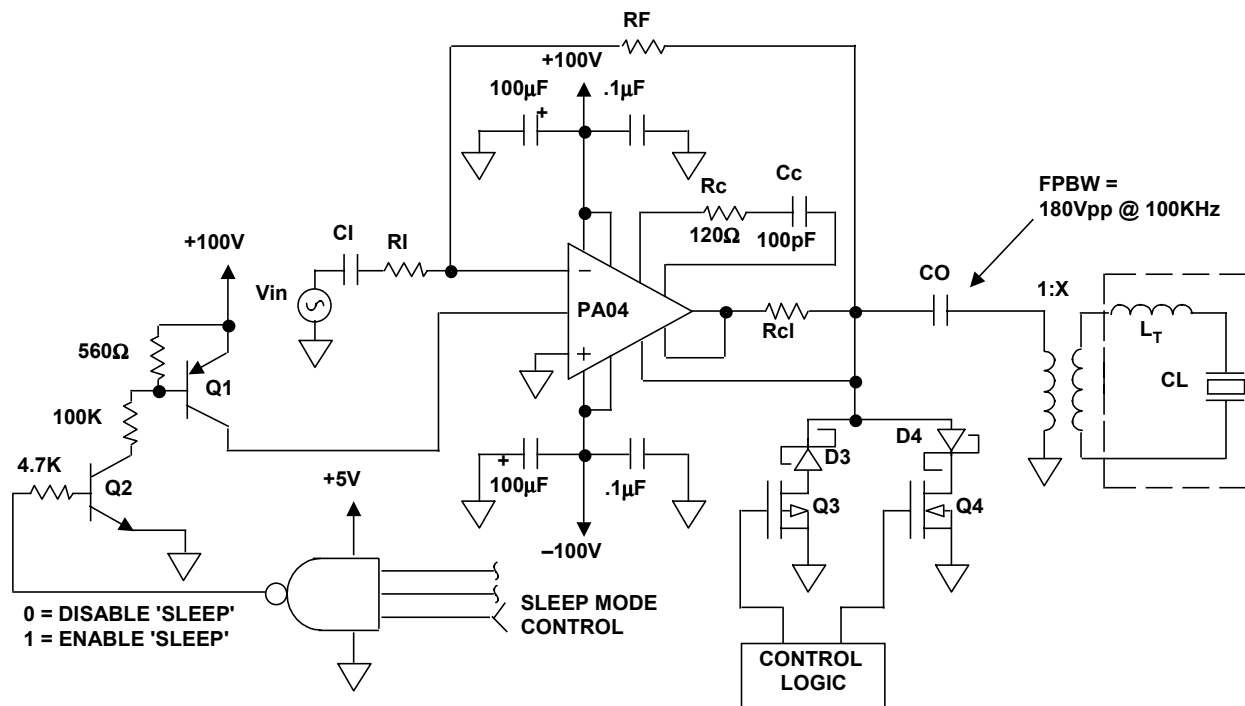
Tested efficiency of this circuit was 80.6% at 60W output, meaning 14.4W wasted. A theoretical linear power stage would dissipate 72W delivering the same output from $\pm 48V$ supplies. Again, roughly that 5:1 heatsink savings of PWM over linear.

Operation of the overall circuit is similar to previous voltage output designs except there are more functions external to the PWM amplifier. The LM111 generates the PWM duty cycle based on the 6V referenced ramp and input signals. The SA51 converts this to power pulses. The filter removes most of the 200KHz switching frequency for the speaker. The differential amplifier also converts power pulses to an analog feedback signal. Over current is detected and latched to disable the power stage. Response time in the area of $5\mu s$ is required.

Capacitor arrays seen decoupling the supplies are not overkill. Larger values do a good job at lower frequency, lower values keep ESR low at the high end. Select capacitors specified for high current switching applications.

Diodes are schottky types for both high speed and low forward voltage drop.

SONAR TRANSDUCER DRIVE



High current drive capability and wide power bandwidth make the PA04 ideally suited for sonar drive applications.

Often the amplifier is required to drive the primary of a transformer to step-up its output voltage to a desired high voltage for end drive to the sonar transducer. Because transformers do not work well when saturated it is essential to minimize DC current flow in them. AC coupling of the input signal and/or the output minimizes and/or eliminates the DC input offset voltage of the PA04 from becoming gained up by the gain of the amplifier, creating a large DC offset at the output.

Often times, either through the construction of the transformer or through an additional inductor, L_t , the sonar transducer, predominantly capacitive by nature, is tuned to look resistive for a narrow band of frequencies. This minimizes SOA stresses on the PA04. It is a good idea however to consider worst case capacitive loading reflected to the primary of the transformer onto the PA04 for AC stability considerations, should there be a possibility of non-resonant frequencies being applied to the sonar transducer drive circuit.

Another feature of the PA04 which is especially helpful in battery operations is its sleep mode function which can be used to turn the amplifier off during periods of non-use to minimize battery drain. Sleep mode quiescent current is only 5mA and the output is turned off into a high impedance state.

One caution when using sleep mode is to be aware of transients up to the supply rail that can occur during transitions into and out of sleep mode. There is no esoteric way to eliminate these internal to the op amp. If these transients would provide undesired transmissions, the problem can be cured through the use of two Schottky diodes (D3,D4) and two MOSFET switches (Q3,Q4). These components short the output of the PA04 to ground during the sleep mode transitions.

Timing logic going into sleep mode is to first command the input to zero, switch on Q3 and Q4 and then enable sleep mode. Coming out of sleep mode we would first ensure input signal is zero, ensure Q3 and Q4 are on, disable sleep mode, turn off Q3 and Q4, and finally begin transmitting with our input signal. Typical delay time to squelch the sleep mode transients is about 5-10 mS.

As a final note, to minimize SOA stresses it is advised to always start the input signal at zero crossing and exponentially ramp the amplitude if possible, since a transformer really doesn't look like a transformer until we have passed a few cycles of AC through it.

TOOLS AT YOUR COMMAND

- General Operating Considerations
- Subject Index
- Selector Guides
- Power Design.xls
- Evaluation Kits
- Sockets & Heatsinks
- Spice Files
- Data Sheets
- Application Notes
- Parameter Definitions and Test Methods
- Accessory Vendors
- Military Screening Flow
- Failure Analysis
- 800-546-2739

The Apex handbook is the world's most complete reference work when it comes to challenging power designs. Roughly a quarter of the book is application notes, a good source of "how to" and "how not to" tips and circuit ideas. Format is your choice; hard copy, CD-ROM or on line with all the latest and greatest.

Unless you're an old hand at power design, check out AN1, General Operating Considerations. It is the most important document in the entire book. While there is no substitute for *actually reading it*, at a very minimum, take note of the paragraph titles and look at the pictures.

In the back of the book is a Subject Index which may just point you to the specific information you need. Here's a sample of entries: Package drawings and marking information (Where's pin 1?), Load lines, Feedback zero compensation and Thermal capacity. You can also find many phone numbers, fax numbers and if you are inclined to visit Apex, a map.

Beat the Discrete Approach

- Time to market value?
 - Lost sales - engineering costs
- Value of 8 solder joints vs. 80?
 - Size, weight
 - Reliability
 - First pass yield, troubleshoot, rework, retest times
 - Field failure rate & serviceability
 - Logistics costs
 - Component spec, buying, stocking

Response to these design issue questions vary an amazing amount, both in time spent on the subject and in answers to specific items. Apex products are used in products where meeting the Christmas buying season is paramount, where cutting machine size by 2 doubles the value of the product and remotely located equipment where field failures would be a disaster.

This seminar has covered many of the technical issues involved with using hybrid power products but it remains your engineering challenge to integrate the various advantages into your business environment. Perhaps a few moments spent here will enhance value of your final product.



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What did you want to get from this seminar?

Did you get it? NO So-so YES

As a user of power components are you: Novice Intermediate Expert

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Applications: _____

The book: _____

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