CEL California Eastern Laboratories

APPLICATION NOTE

AN1028
Testing Dual-Chip Transistor Arrays for VCO/Buffer Amp Combinations and Two-Stage Amplifier Applications

I. Introduction

Designers of handheld wireless products share common goals: higher performance, smaller size, and lower costs. Usually the first people they turn to for help are the semiconductor manufacturers, who respond with products like NEC's new UPA8XXT Series dual-chip silicon transistor arrays. Designed for applications that require two closely matched transistors, NEC selects two neighboring NPN chips from the wafer and encapsulates them side-by-side in a miniature 1.25 X 2mm 6-pin plastic surface mount package. Each transistor is independently mounted so the devices can be configured for either dual transistor or cascode operation. Several of the devices are also available in cascade versions (Figures 1 & 2). They're especially well-suited for VCO/buffer amplifier combinations, as well as two stage amplifiers.

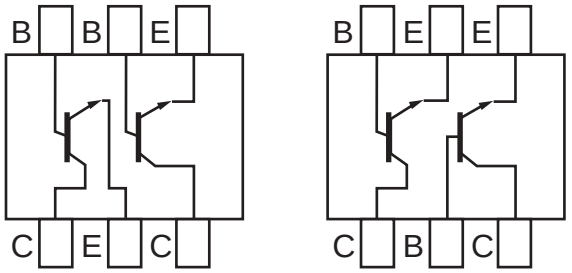

Figure 1. Cascode device (left) and the Cascade version (right)

Part Number Cascode/Cascade	f_T GHz	Ic Max (mA)	Noise Figure typ (dB)	$\|S_{21E}\|^2$ typ (dB)
UPA801T/UPA810T	7.0	100	1.2@1 GHz	9.0@1 GHz
UPA802T/UPA812T	9.0	65	1.4@1 GHz	12.0@1 GHz
UPA800T/UPA811T	10.0	35	1.9@2 GHz	7.5@2 GHz
UPA809T/UPA814T	10.0	100	1.5@2 GHz	6.5@2 GHz
UPA806T/–	12.0	30	1.5@2 GHz	8.5@2 GHz
UPA808T/–	13.5	30	1.3@2 GHz	8.5@2 GHz
UPA807T/–	15.5	10	1.5@2 GHz	9.0@2 GHz

Figure 2. Specifications: NEC Dual Chip Transistor Arrays

II. Customer's Needs

One of CEL's customers was considering using NEC's UPA808T dual chip device in a low voltage/low current design. They needed an amplifier with at least 16 dB gain and a Noise Figure of less than 2.1 dB. This design had a V_{CE} of 0.2 volts with a 1 mA collector current (I_C), and it had to be stable. Like many manufacturers today, this customer was short on time and lacked engineering resources. CEL was assigned the task of proving that the UPA808T could perform.

Evaluating DC and RF Performance

Consistent, repeatable performance is a major concern for designers of wireless products. Since the biasing of this design was very low, its operation point was very close to the knee region of the transistor. Additionally, under these biasing conditions, the collector-to-base junction was not hard-reverse biased, resulting in internal feedback to the RF signal and marginal isolation.

To demonstrate consistent DC performance, CEL plotted the IV curves of ten UPA808T devices using a curve tracer under low voltage and low current conditions. In the example shown (Figure 3), the devices were tested at up to V_{CE} = 0.5 volts and I_C = 3 mA with less than 0.5% variation noted. It was determined that the UPA808T could provide over 5 mA of linear performance when biased at V_{CE} = 0.2 volts.

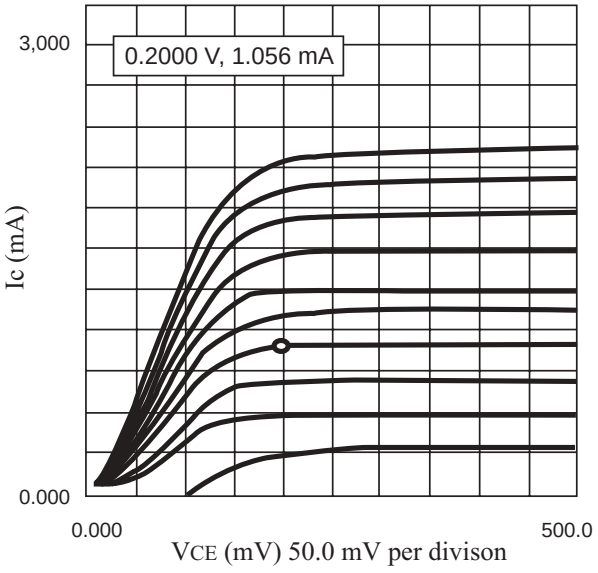

Figure 3. IV Curve Plot

Once the DC analysis was completed, Noise and S-Parameters of five devices were measured at:

V_{CE} = 0.2 V I_C = 1 mA
V_{CE} = 0.5 V I_C = 1 mA
V_{CE} = 1.0 V I_C = 1 mA

When superimposed, variations in the S-parameters' amplitude and phase did not exceed 1% across the entire group of devices.

Based on the consistent results of the DC and RF analysis, it was decided that if a few UPA808T devices could meet the customer's requirements, the performance could be repeated with other devices.

Simulating and Testing the Circuit

Using the UPA808T's S-parameters in both Common Emitter and Common Base configuration, the circuit was modeled using LIBRA (Series IV) simulation software. The simulation allowed CEL engineers to quickly analyze the design, sense its potential instability, and change the overall topology at will. It also provided good information for future laboratory tuning. Results of the simulation are shown in Figure 4.

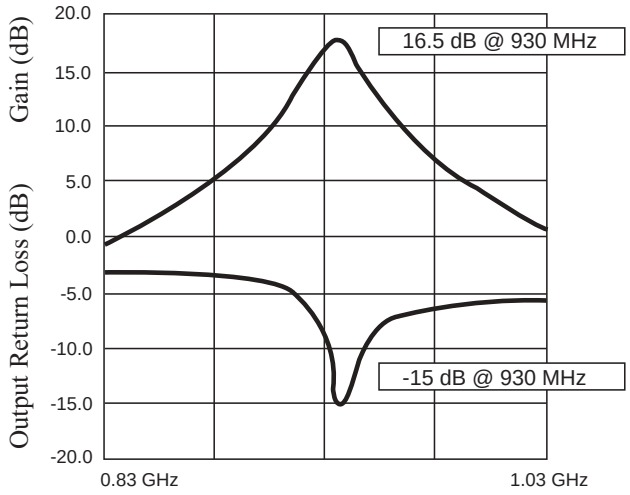

Figure 4. Gain and Output Return Loss: Simulation

The actual measured performance achieved was close to the simulated result, with the UPA808T actually exceeding the customer's Gain and Noise requirements shown in Figure 5.

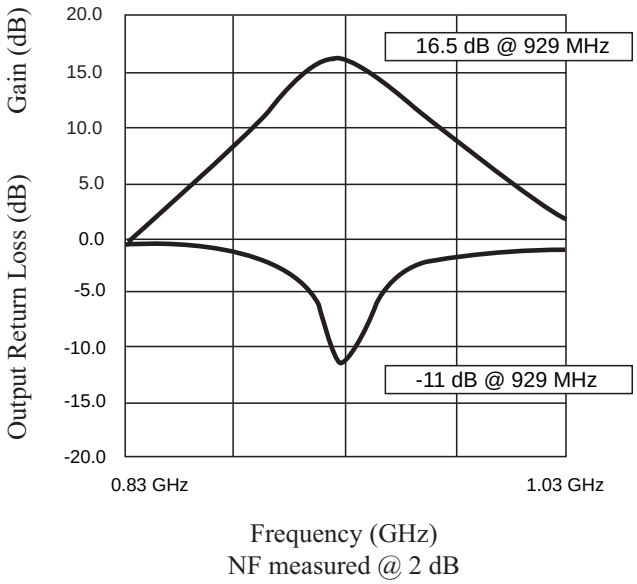

Figure 5. Gain and Output Return Loss: Actual Measured Performance

Unconditional Stability

Finally, CEL had to demonstrate the stability of the design. To do so, five different devices were tested on two boards. A double stub tuner with a VSWR of 10:1 was connected to the inputs. The output was then monitored on a spectrum analyzer as impedance was circled around the Smith Chart. The circuit showed no oscillation under these conditions.

A Good Choice

In conclusion, the performance figures and exceptional repeatability demonstrated by these dual chip arrays show they are an excellent choice for applications requiring a dense design or two closely matched transistors. This customer's design reduced the parts count, simplified the assembly, and reduced the size of the design. More importantly, the consistent performance demonstrated reduced costs of manufacturing which is a critical element in the production of high-volume consumer products.

California Eastern Laboratories
Exclusive Agents for NEC RF, Microwave and Optoelectronic semiconductor products in the U.S. and Canada
4590 Patrick Henry Drive, Santa Clara, CA 95054-1817
Telephone 408-988-3500 • FAX 408-988-0279 •Telex 34/6393
Internet: http:/WWW.CEL.COM