AN1022

APPLICATION NOTE

Designing Low Noise Amplifiers for PCS Application

ABSTRACT

This application note will review the process by which microwave amplifier designers choose their designs based on performance requirements, real estate constraint and prices. Traditionally, for small signal amplifiers, there has been three distinct and generally incompatible basic designs that have met most design goals: the high gain, low return loss amplifier, the low noise amplifier and the high output power amplifier.

With the emergence of new technologies, in particular digital communications, the need for composite amplifiers that meet specific design goals has increased. This article will demonstrate how the different basic design types can be accomplished using a low cost NEC HJ-FET in a plastic package (Part I), and how improved performance can be achieved for a low noise PCS amplifier by using series feedback techniques (Part 2). Finally, (Part 3) will introduce some device modelization techniques used in creating non linear models and will verify these models with the above mentioned circuits.

While the designs proposed may not yield the optimum design solutions for all PCS applications, it does introduce a few important RF and microwave techniques that can be applied to other digital applications.

DESIGN CONSIDERATION

In this article, the design is for a 58 MHz bandwidth amplifier at a central frequency F_C=1960 MHz. The bandwidth represents less than 3% of F_C and consideration will only be given to narrow band amplifier reactively matched designs (defined as less than 10% of F_C). There are three basic transistor amplifiers designs available to engineers: maximum gain amplifiers, low noise amplifiers and high output power amplification. In each distinct mode of operation, the FET (or Bipolar transistor) is presented with different loads and source impedance transferred from 50 Ohms. Each design goal will require a different design approach and matching networks.

DEVICE CHOICE AND CHARACTERISTIC

The device chosen for all designs is the NE34018, a low noise, low cost Gallium Arsenide Hetero-Junction Field Effect Transistor (HJ-FET) housed in a miniature (SOT-343) plastic surface mount package. This device was selected because it offers an excellent compromise between cost and the high performance associated with High Electron Mobility Transistors: Low Noise figure (0.6 dB) and high gain (16 dB typical) at 2 GHz under low bias conditions (2V, 5 mA), a prime concern for products in the mobile communication industry. Both Noise and S-Parameters for the NE 34018 are available in **Table 1**.

With a 0.6 μm by 400 μm geometry, the device is large enough to provide a reasonably high output power (output IP3 of 23 dBm typical at 2 V, 10 mA) with noise parameters optimized for the 1 to 3 GHz band (0.6 dB typical at 2 GHz). Additionally, the geometry, larger than other HJ-FETs makes it easier to design at the PCS and MMDS frequency bands both for impedance matching and stability. Other devices available to designers such as standard MESFETs (Metal Semiconductor Field Effect Transistors) were discarded because they provide a typical noise figure of 1.0 dB at 2 GHz. This leaves little margin for matching network losses and device variations when compared to typical PCS amplifier design goals. Other devices, such as PHEMTs (Pseudomorphic High Electron Mobility Transistor) have the required low noise (0.3 dB at 3 GHz), but their small geometry (0.15 μm by 180 μm) does not provide the necessary output power. Additionally, most PHEMTs are prone to instability problems at low frequencies.

GAIN MATCH THEORY

In the design of amplifiers for maximum gain, the purpose is to transform the input and output loads: Γ_S and Γ_L to the matched counterparts of the device: Γ_{SM} and Γ_{LM}. This optimal source and load impedance will allow the maximum power transfer through the 2 port network (the amplifier) and will maximize the gain: The device is simultaneously

NE34018 S-PARAMETERS

V_{DS} = 3 V, I_{DS} = 20 mA CS, I_{DSS} = 71 mA

Frequency (GHZ)	S11 MAG	S11 ANG	S21 MAG	S21 ANG	S12 MAG	S12 ANG	S22 MAG	S22 ANG
0.50	0.969	-18.7	8.662	160.8	0.016	81.1	0.667	-7.3
0.75	0.937	-27.5	8.396	152.0	0.024	77.0	0.652	-10.9
0.90	0.915	-32.7	8.209	147.0	0.028	74.8	0.641	-12.9
0.95	0.905	-34.4	8.159	145.3	0.029	74.1	0.636	-13.6
1.00	0.898	-36.1	8.096	143.6	0.031	73.3	0.632	-14.3
1.25	0.852	-44.4	7.770	135.7	0.037	70.1	0.611	-17.5
2.00	0.697	-68.4	6.775	113.9	0.056	61.4	0.539	-26.4
2.50	0.591	-84.9	6.144	100.9	0.066	56.5	0.496	-32.0
3.00	0.493	-102.7	5.553	88.9	0.075	52.1	0.458	-37.1
4.00	0.368	-141.9	4.526	68.0	0.091	44.9	0.399	-44.7
5.00	0.349	-173.2	3.790	51.2	0.107	39.9	0.343	-48.1
6.00	0.362	170.2	3.332	36.7	0.127	35.6	0.284	-50.8
7.00	0.356	154.4	3.024	22.0	0.148	28.8	0.230	-61.8
8.00	0.336	123.7	2.782	5.7	0.171	20.3	0.199	-89.6
9.00	0.385	87.0	2.523	-11.6	0.189	9.8	0.208	-127.5
10.00	0.495	62.6	2.245	-29.4	0.200	-1.8	0.234	-172.5

NOISE PARAMETERS

Frequency (GHz)	NF Min (dB)	Gamm Opt MAG	Gamm Opt MAG	r(n)
1.00	0.41	0.610	59.7	0.13
1.50	0.48	0.560	71.0	0.14
1.90	0.59	0.490	88.0	0.12
2.00	0.60	0.490	89.0	0.11
3.00	0.66	0.450	128.0	0.04

Table 1: NE34018 Noise and S-Parameters

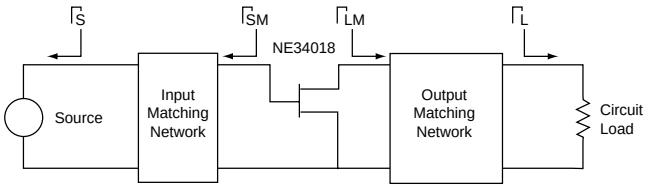


Figure 1: Circuit matching.

conjugatively matched **(Figure 1)**. From general microwave two port network theory [1], [2], the maximum gain is defined as:

$$G = |S_{21}|^2 \frac{(1-|\Gamma_{SM}|^2)(1-|\Gamma_{LM}|^2)}{|(1-\Gamma_{SM}S_{11})(1-\Gamma_{LM}S_{22})-\Gamma_{SM}\Gamma_{LM}S_{21}S_{12}|^2} \quad \textbf{(1)}$$

At this point, an important assumption can be made to simplify the calculations. The network is assumed to be unilateral (a perfect isolation between the output and the input: $S_{12} = 0$). The value of such an assumption can be assessed by the unilateral figure of merit [3]:

$$U = \frac{|S_{11}||S_{22}||S_{21}||S_{12}|}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad \textbf{(2)}$$

This formula defines the boundaries of the error introduced by the simplified calculation between the transducer power gain G and the unilateral transducer gain G_u :

$$\frac{1}{(1+U)^2} < \frac{G}{G_u} < \frac{1}{(1-U)^2} \quad \textbf{(3)}$$

If the error is deemed small enough to justify the unilateral assumption, then the unilateral transducer power gain is defined as:

$$G_u = |S_{21}|^2 \frac{(1-|\Gamma_{SM}|^2)(1-|\Gamma_{LM}|^2)}{|1-\Gamma_{SM}S_{11}|^2 |1-\Gamma_{LM}S_{22}|^2} \quad \textbf{(4)}$$

In this case, we can easily see that the gain only depends on the S-Parameters of the device and the matching to the input and to the output. The loads Γ_S and Γ_L presented to the active device allow for different designs and optimize the performance of the amplifier. Complex number theory can be utilized to demonstrate that G_u will be maximized if $\Gamma_S = S^*_{11}$ and $\Gamma_L = S^*_{22}$ (a well-known simplified matching principle) in which case the obtained maximum gain from the device is:

$$G_{u,Max} = |S_{21}|^2 \frac{1}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad \textbf{(5)}$$

Frequency Range	(MHz)	Goals (1932-1990)	Simulation (1932-1990)	Test (1932-1990)
Gain	(dB)	16 Min.	17 Min.	16.5 Min.
Noise Figure	(dB)	2 dB Max.	1.5 dB Max.	1.5 dB Max.
Input IP3	(dBm)	6 dBm Min.	6 dBm Min.	6 dBm Min.
Input Return Loss	(dB)	-18 Min.	-20 Min.	-19 Min.
Output Return Loss	(dB)	-18 Min.	-20 Min.	-20 Min.
Bias condition	(dBc/Hz)	3 V, 20 mA Max.	3 V, 20 mA Max.	3 V, 20 mA Max.
Real Estate	(Mils*Mils)	250*250	N/A	250*250
Price in 100 K Quantities	(US$)	Less than $1	N/A	Less than $1

Table 2: Maximum Gain Design Performance: Goals, simulation and tests.

This formula shows that the maximum unilateral gain of an amplifier is determined solely by the S-Parameters of the device chosen, regardless of the source or load impedance.

In reality (as can be seen by the attached S-Parameters), the isolation of this device is not perfect and consequently $S_{12} \neq 0$. The condition under which both input and output ports can be matched simultaneously to achieve a maximum gain is much more complicated. The input match depends on the load impedance and vice versa. The resulting calculations are beyond the scope of this article, however, the results are of importance in the design of microwave amplifiers. The maximum gain is found to be achieved when the device is simultaneously conjugatively matched with the source and load coefficients referenced earlier: Γ_{SM} and Γ_{LM}. Since the unilateral assumption is no longer valid, these two reflection coefficients involve elaborated complex number calculations routinely processed by linear simulators. These two loads also need to have an amplitude less than 1 to ensure both stability and the matching of a source (or load) that has the real part of its impedance positive. The equivalent and necessary condition to this equation is:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \qquad \textbf{(6)}$$

Where $\Delta = S_{11}S_{22} - S_{12}S_{21}$ **(7)**

When the device is simultaneously conjugatively matched, the maximum transducer gain is obtained with the following formula:

$$G_{max} = \left|\frac{S_{21}}{S_{12}}\right|(K \pm \sqrt{K^2 - 1}) \qquad \textbf{(8)}$$

This is the Maximum Available Gain (MAG) provided by device manufacturers and is only valid when $K>1$. If additionally, $|\Delta|<1$, the device is unconditionally stable and G_{max} will be achieved. When $K<1$, the transistor is potentially unstable and G_{max} does not exist. However, we can see that as $K \rightarrow 1$ and $K>1$, G_{max} converge towards a value called the Maximum Stable Gain (MSG) defined as:

$$^{1}MSG = \left|\frac{S_{21}}{S_{12}}\right| \qquad \textbf{(9)}$$

STABILITY MATCH

One area of interest to all designers is the stability of the circuit, especially when using Hetero-Junction FETs with very high gain levels at lower frequency. These types of FETs display a natural propensity to oscillations. The circuit is defined as unconditionally stable when it cannot oscillate under any source or load impedance. The input reflection coefficient must be less than one for all loads. This ensures a positive input resistance from the device, and a similar condition applies to the output resistance in regard to the input loads. These conditions are satisfied with the equations:

$$\left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - \Gamma_L S_{22}}\right| < 1 \quad \text{for any Source loads} \qquad \textbf{(10)}$$

$$|\Gamma_L < 1|$$

and $$\left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - \Gamma_S S_{11}}\right| < 1 \text{ for } |\Gamma_S < 1| \qquad \textbf{(11)}$$

They translate back in the K factor and the B1 factor:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \qquad \textbf{(12)}$$

And either:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \qquad \textbf{(13)}$$

or $$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \qquad \textbf{(14)}$$

In the circuit design shown in the following sections, care was taken to carry an unconditionally stable circuit by adding a shunt resistance to ground on the output (See the output resistor R1 of schematic of **Figure 2**). This stabilizing network represents an acceptable compromise between out-

put power, gain levels and stability. With such a narrow band design, it is always important to verify the stability issue over a broad frequency range (from 100 MHz to 10 GHz, in this case).

MAXIMUM GAIN DESIGN

Using these matching techniques on the NE34018 in the band of interest, the circuit was modeled using Libra as a linear simulator **(Figure 2)** with bias conditions of 3V, 20 mA. The lumped elements were all modeled using lossy elements with a finite Q factor. The topology chosen was a high pass filter on both input and output so that the designer would have better control over the impedance presented out of band at lower frequencies. At these frequencies, these filters present a mismatch with a controlled phase quantity that is chosen to avoid oscillation, they also improve stability by reducing the amount of gain generated by the device and buffer the device from the system's out of band impedances. Finaly, this type of configuration also provides DC isolation on the input and output, further reducing the need for extra components.

The simulated gain and input/output return loss performance are presented in **Figure 3**. The input load presented to the device, S11 of the device and the noise circles are shown in **Figure 4**. This match yields an excellent return loss (better than 20 dB) with a noise figure of 1.5 dB because the optimal impedance Γ_{Opt} was not presented. The circuit fabricated as seen in **Figure 5** with only five matching elements (DC supply not included) and real estate that could have been limited to 0.250" by 0.250." The actual performance is summarized in **Figure 6** at 3 V, 20 mA, and **Figure 7** at 3V, 30 mA. Although power was neither simulated nor designed for, the power performance and IP3 were measured and are presented in **Figures 8 to 11**. **Table 2** summarizes the design goals, simulated performance and actual laboratory results. Note that the simulated and actual performance of the circuit match well. However, lumped element matching values utilized to correlate these did not track exactly. This is because the simulation of the DC bias network beyond the RF Ground (C4 and C5 on the assembly drawing) was omitted, and most of the lumped capacitor have a low self-resonance, consequently they no longer act as pure capacitance. For example, a 12 pF capacitor had a self resonance around 1.5 GHz and had a definite inductive behavior beyond self-resonance. Minor tuning had to be performed to define the final circuit match. Once the optimal tuning was achieved, it was also shown that the design performance had little sensitivity to biasing. With an increased bias current, all parameters but noise figure improved. Finally, as expected, the resulting Noise Figure was not low enough for a first stage Low Noise Amplifier, despite the very low minimum noise figure inherent to the device. However, the next section will prove that an excellent performance can be achieved with the proper match.

[1] *(The MAG or MSG values are provided by California Eastern Labs in the Design Parameter Library for all NEC devices.)*

LOW NOISE MATCH

A low noise amplifier (LNA) design minimizes the noise figure of its active device by presenting an optimal source reflection coefficient $\Gamma_{S(Opt)}$ while the output circuit is designed for flat gain and overall stability to the circuit. It is a particular case of the Gain Match theory described earlier in that the input load is fixed and defined by the active device's noise parameters (specifically $\Gamma_{S(Opt)}$, and the designer has to adjust accordingly the output match to achieve both gain criteria and stability.

With an arbitrary source load, Γ_S, the device yields a noise figure, NF, given by:

$$NF = NF_{min} + \frac{4r_n \left|\Gamma - \Gamma_{S(Opt)}\right|^2}{\left|1+\Gamma_{S(Opt)}\right|^2 \left[1-\left|\Gamma_S\right|^2\right]} \quad \textbf{(15)}$$

Where $r_n=R_N/50$ is the equivalent noise resistance usually provided with the noise parameters by device manufacturers. From **(15)**, it is clear that $NF = NF_{min}$ when $\Gamma_S = \Gamma_{S(Opt)}$

Noise figure can also be expressed as:

$$NF=NF_{min}+\frac{R_N}{\Gamma_S}\left[(G_S-G_{S(Opt)})^2 + (B_A-B_{S(Opt)})^2\right] \quad \textbf{(16)}$$

Consequently, the noise expression can be simplified to**:**

$$NF = NF_{min} + \Delta NF \quad \textbf{(17)}$$

Where the term ΔNF is a measure of the additional noise generated by a source mismatched, Γ_S, compared to the optimal source $\Gamma_{S(Opt)}$. **Equation (16)** shows that noise figure contours with constant value NF_i can be defined as circles centered on:

$$C_{NF} = \frac{\Gamma_{S(Opt)}}{1+N_i} \quad \textbf{(18)}$$

$$\text{Where } N_i = \frac{N_i - NF_{min}}{4r_n}\left|1+\Gamma_{S(Opt)}\right|^2 = \frac{\left|\Gamma_S-\Gamma_{S(Opt)}\right|^2}{1-\left|\Gamma_S\right|^2} \quad \textbf{(19)}$$

This formula represents the amount of mismatch from the optimal load for a given value of NF_i. The associated radius can then be calculated as follows:

$$r_{NF} = \frac{1}{1+N_i}\sqrt{N_i^2+N_i\left(1-\left|\Gamma_{S(Opt)}\right|^2\right)} \quad \textbf{(20)}$$

In practical application, if $NF_i=NF_{min}$, then $C_{NF} = \Gamma_{S(Opt)}$, the radius of the circle is $r_{NF}=0$ and the device is matched to its minimum noise figure. On the other hand, as seen previously in Part 2, because the device is not matched to the optimal load, a mismatch loss will result, decreasing the circuit gain by a few dB to the associated gain. In a cascaded design, careful consideration should be given to achieve a compromise between noise and gain performance since the noise figure of subsequent amplifier stages will affect the overall performance of the system but will be reduced by a higher gain in the first stage.

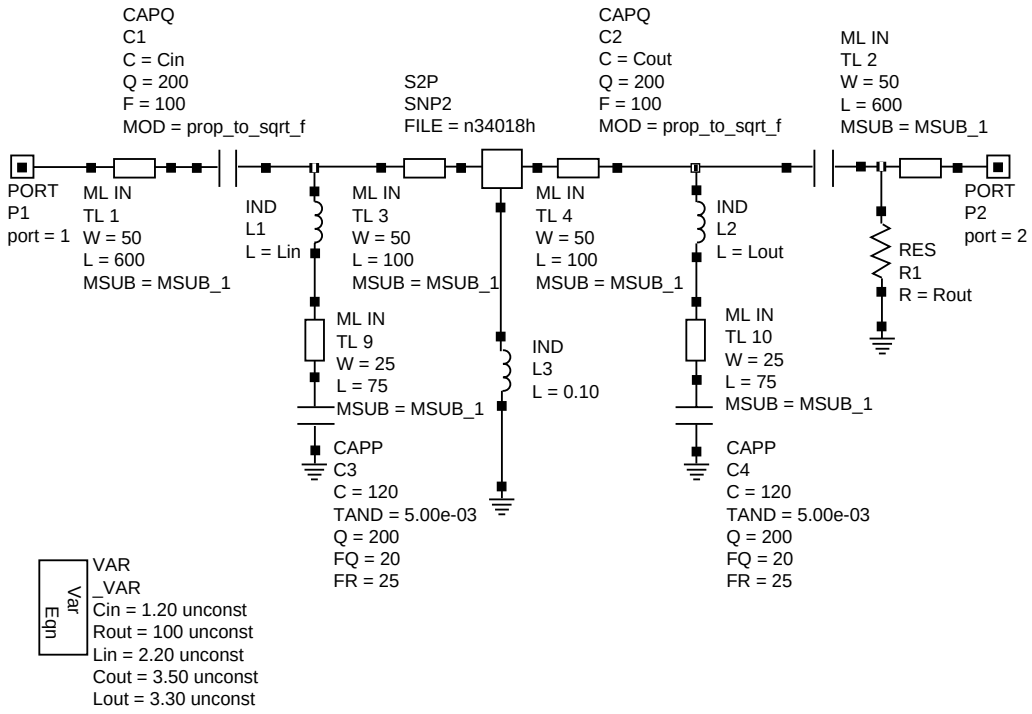


Figure 2: Maximum Gain Amplifier. Cimulation circuit 1.

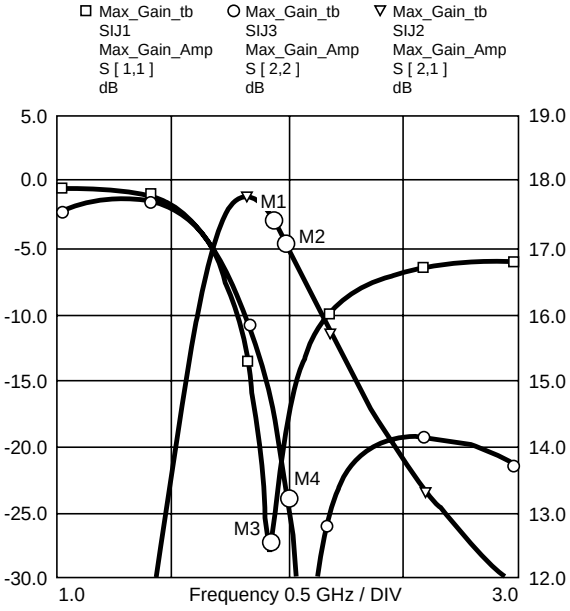


Figure 3. Max Gain amplifier simulation results.

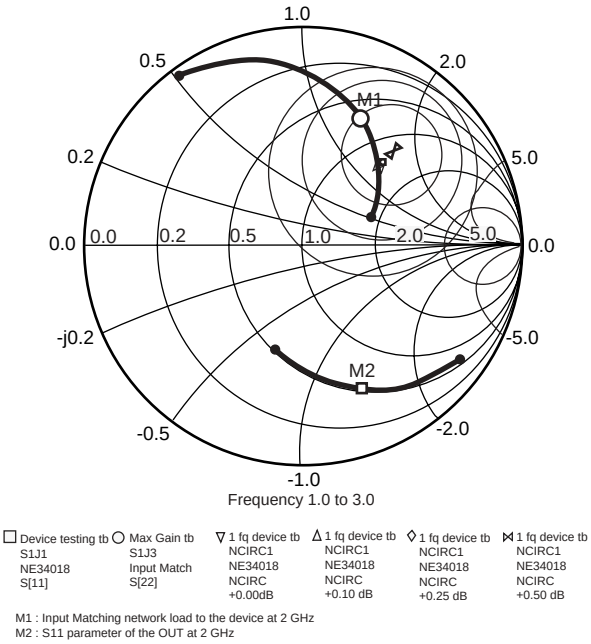
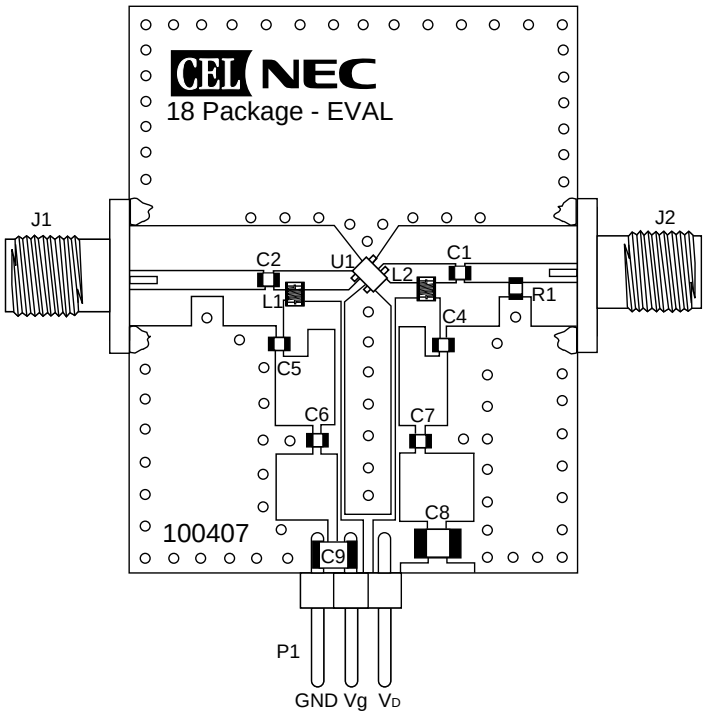


Figure 4: S-parameter, matching network and noise circles.



EVALUATION BOARD PARTS LIST, HIGH GAIN MATCH

QTY	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	SD-100407		Schematic Diagram NE34018-EVAL	14
1	TF-100413		NE34018-EVAL Test Fixture Block	13
1	LL 1608-FHIN8S	L2	1.8 nH Inductor TOKO	12
1	LL 1608-FH3N3S	L1	1.2 nH Inductor TOKO	11
1	MCR03J271	R1	0603 270 OHM RES ROHM	10
1	MCH185A1R5CK	C2	0603 1.8pF CAP ROHM	9
1	MCH185A2R2CK	C1	0603 2.2pF CAP ROHM	8
2	MCH185A121JK	C4, C5	0603 120pF CAP ROHM	7
2	MCH185C102KK	C6, C7	0603 1000pF CAP ROHM	6
2	881-6116	C8, C9	4.7 μF CAP AVX	5
1	NE34018	U1	IC NEC, HJ-FET	4
3	2340-6111 TG	P1	Pin Header 3M	3
2	2052-1215-00	J1, J2	OSM JACK OMNI SPECTRA	2
1	FD-100407	PCB	18 Package-EVAL Fabrication Drawing	1

EVALUATION BOARD PARTS LIST, LOW NOISE FIGURE MATCH

QTY	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	SD-100407		Schematic Diagram NE34018-EVAL	14
1	TF-100413		NE34018-EVAL Test Fixture Block	13
1	LL 1608-FHIN8S	L2	1.8 nH Inductor TOKO	12
1	LL 1608-FH3N3S	L1	3.3 nH Inductor TOKO	11
1	MCR03J271	R1	0603 270 OHM RES ROHM	10
1	MCH185A1R5CK	C2	0603 1.5pF CAP ROHM	9
1	MCH185A2R2CK	C1	0603 2.2pF CAP ROHM	8
2	MCH185A121JK	C4, C5	0603 120pF CAP ROHM	7
2	MCH185C102KK	C6, C7	0603 1000pF CAP ROHM	6
2	881-6116	C8, C9	4.7 μF CAP AVX	5
1	NE34018	U1	IC NEC, HJ-FET	4
3	2340-6111 TG	P1	Pin Header 3M	3
2	2052-1215-00	J1, J2	OSM JACK OMNI SPECTRA	2
1	FD-100407	PCB	18 Package-EVAL Fabrication Drawing	1

Figure 5: NE34018 Evaluation Board.

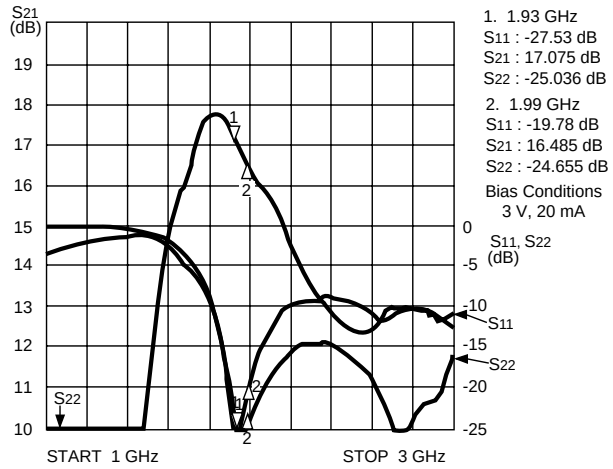


Figure 6: Maximum Gain Amplifier test results, 3 V, 20 mA.

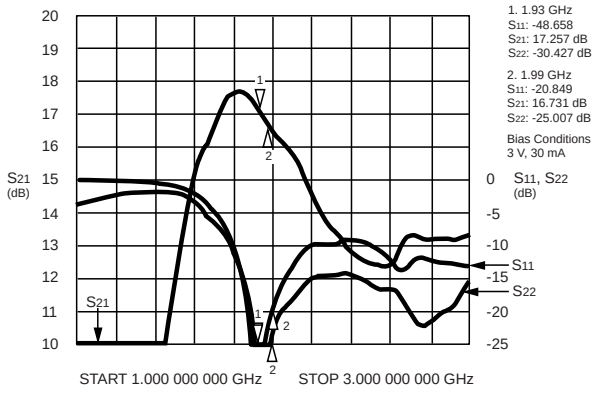


Figure 7: Maximum Gain Amplifier test results, 3 V 0 mA.

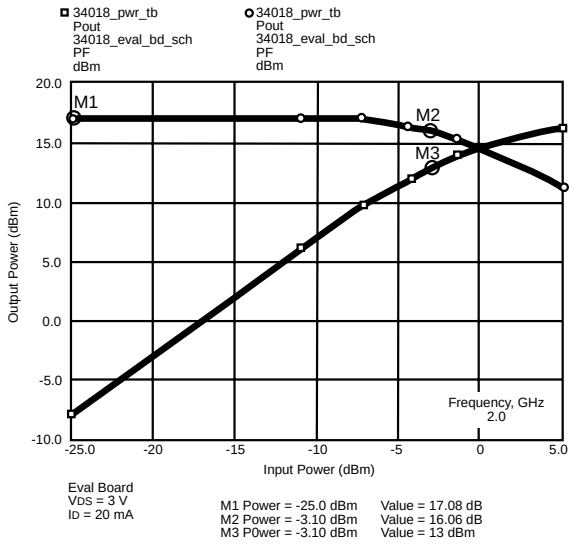


Figure 8: NE34018 evaluation board, Pin-Pout simulation.

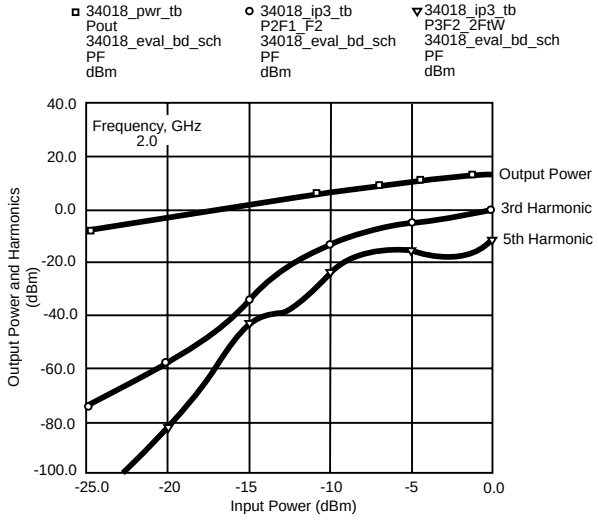
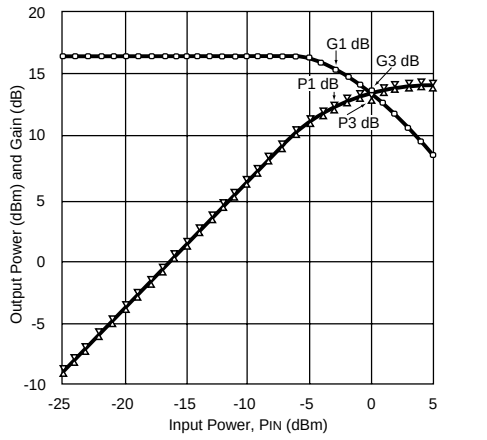


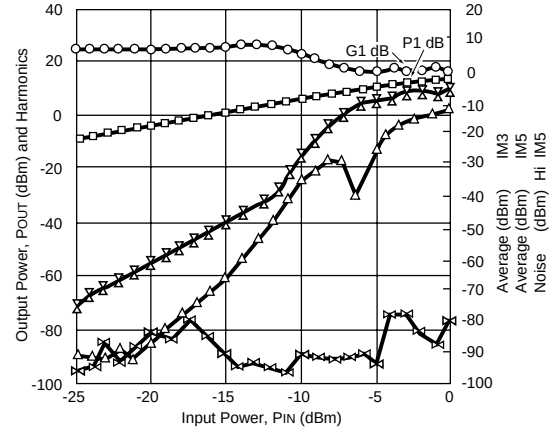
Figure 9: 2 GHz Evaluation Board, IP3 versus Pin sweep simulation.



Frequency : 2.00 GHz
Vd : -0.000 V
Id : 0.000 mA
Bias # : 1
Source impedance : 50 Ω
Load impedance : 50 Ω

Pout @ 1 dB : 12.485
Gain @ 1 dB : 15.426
Pout @ 3 dB : 13.228
Gain @ 3 dB : 13.412

Figure 10: 2 GHz evaluation board, Pout versus Pin sweep test results.



Frequency : 2.00 GHz
Vd : 3.0 V
Id : 20 mA
Bias # : 1

Pout @ P1dB : 12.508
Gain @ P1dB : 15.542
Pout @ .01 dB : 13.744
Gain @ .01 dB : 13.98

Figure 11: 2 GHz Evaluation Board, IP3 versus Pin sweep test results.

The same configuration as the optimum gain design was adopted for the low noise design (a high pass structure), and the simulation results using Libra are summarized in **Tables 3 and 4** and presented in **Figures 12, 13 and 14**. As shown in **Table 4**, the noise figure performance drastically improves to 0.7 dB, the input return loss decreased to about -5 dB, and the gain by about 2 dB. Once again, these simulated results track very closely with actual laboratory testing, as seen in **Figure 15**. The noise figure consistently measured between 0.7 and 0.8 dB at 3V, 20 mA. **Figure 5** also provides the final assembly drawing of the low noise amplifier design.

Frequency Range	**(MHz)**	**Goals (1932-1990)**	**Simulation (1932-1990)**	**Test (1932-1990)**
Gain	(dB)	15 Min.	15 Min.	15.5 Min.
Noise Figure	(dB)	0.8 dB Max.	0.75 dB Max.	0.8 dB Max.
Input Return Loss	(dB)	N/A	-5	-5
Output Return Loss	(dB)	-15 Min.	-17 Min.	-16 Min.
Bias condition	(dBc/Hz)	3 V, 20 mA Max.	3 V, 20 mA Max.	3 V, 20 mA Max.
Real Estate	(Mils*Mils)	250*250	N/A	250*250
Price in 100 K Quantities	(US$)	Less than $1	N/A	Less than $1

Table 3: Low Noise Design Performance: Goals, simulation and tests.

	Max Gain_tb SI1J PCS Amplifier	Max Gain_tb NF1 PCS Amplifier	Max Gain_tb NFMIN1 PCS Amplifier	Max Gain_tb K1 PCS Amplifier
Frequency (GHz)	S[2,1] dB	NF dB	NFMIN dB	K
1.00	12.0467	1.2887	0.7284	1.0858
1.10	13.0367	1.0898	0.6543	1.0832
1.20	13.8214	0.9497	0.6100	1.0997
1.30	14.4192	0.8507	0.5869	1.1328
1.40	14.8695	0.7812	0.5784	1.1700
1.50	15.1816	0.7337	0.5798	1.2131
1.60	15.3737	0.6972	0.6026	1.2545
1.70	15.4657	0.6845	0.6310	1.2893
1.80	15.4693	0.6899	0.6625	1.3211
1.90	15.3946	0.7088	0.6958	1.3563
2.00	15.2593	0.7211	0.7051	1.3878
2.10	15.0835	0.7331	0.7177	1.4253
2.20	14.8711	0.7508	0.7307	1.4595
2.30	14.6317	0.7725	0.7439	1.4906
2.40	14.3731	0.7967	0.7570	1.5190
2.50	14.1018	0.8222	0.7700	1.5444
2.60	13.8339	0.8476	0.7823	1.5643
2.70	13.5609	0.8717	0.7941	1.5818
2.80	13.2850	0.8935	0.8055	1.6013
2.90	13.0082	0.9118	0.8164	1.6229
3.00	12.7328	0.9252	0.8267	1.6472

Table 4: NE34018 Low Noise Amplifier, optimized for Noise Figure.

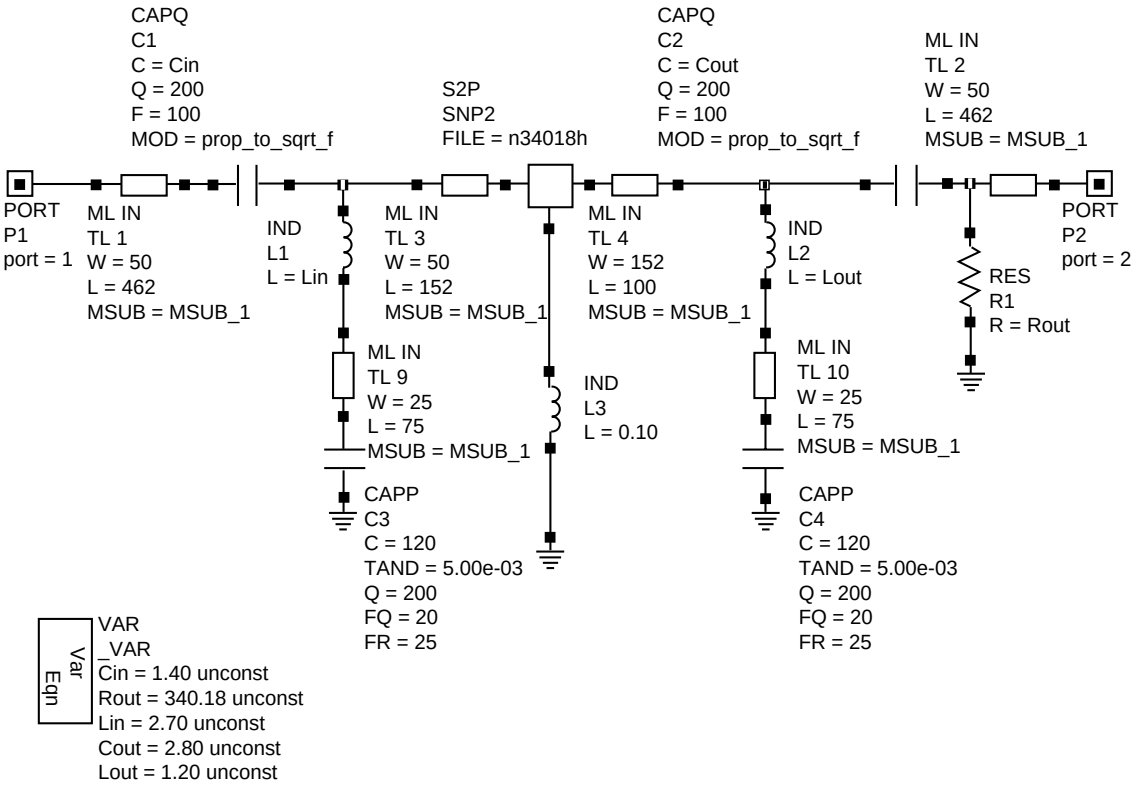


Figure 12: Low Noise Amplifier simulation circuit.

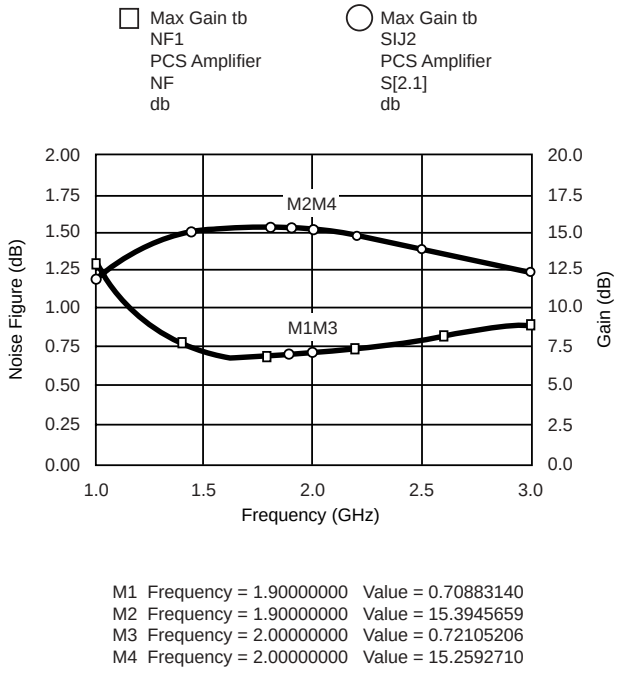


Figure 13: Noise Figure and gain simulation.

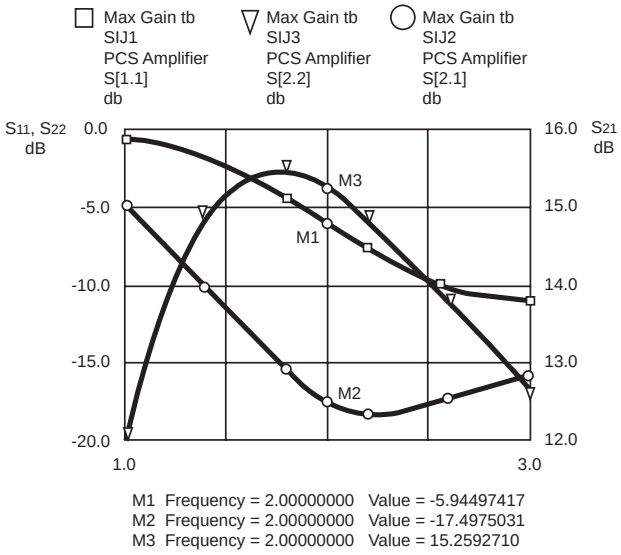


Figure 14: Input, output return loss and gain simulation.

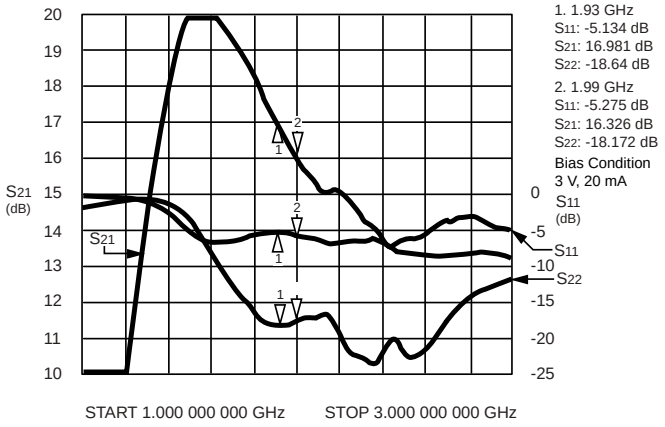
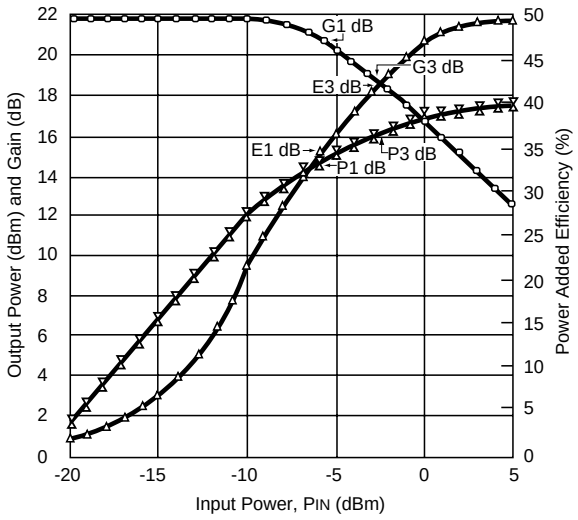


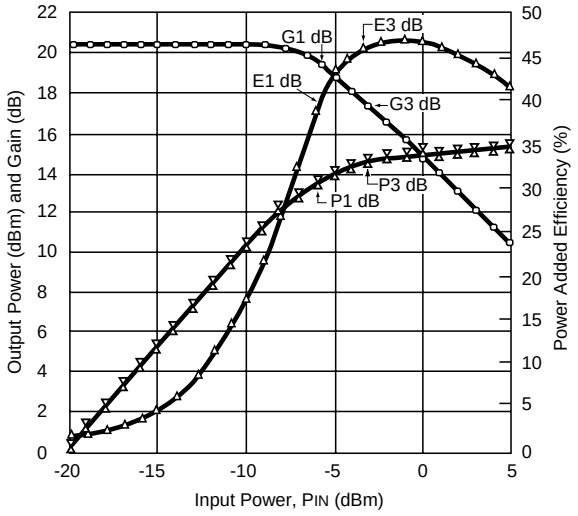
Figure 15: Evaluation board lab results.



Frequency :	2.00 GHz	Pout @ 1 dB :	14.875
Vd :	3.252 V	Gain @ 1 dB :	20.865
Id :	20.061 mA	Eff @ 1 dB :	34.625
Bias # :	1	Pout @ 3 dB :	16.08
		Gain @ 3 dB :	18.825
		Eff @ 3 dB :	42.057

Power Out
Efficiency
Gain

Figure 17: Power matched device, Pout versus Pin sweep.



Frequency :	2.00 GHz	Pout @ 1 dB :	13.617
Vd :	3.252 V	Gain @ 1 dB :	19.401
Id :	20.016 mA	Eff @ 1 dB :	39.96
Bias # :	1	Pout @ 3 dB :	14.361
		Gain @ 3 dB :	17.355
		Eff @ 3 dB :	46.359

Power Out
Efficiency
Gain

Figure 16: 2 GHz Small Signal matched device, Pout versus Pin sweep.

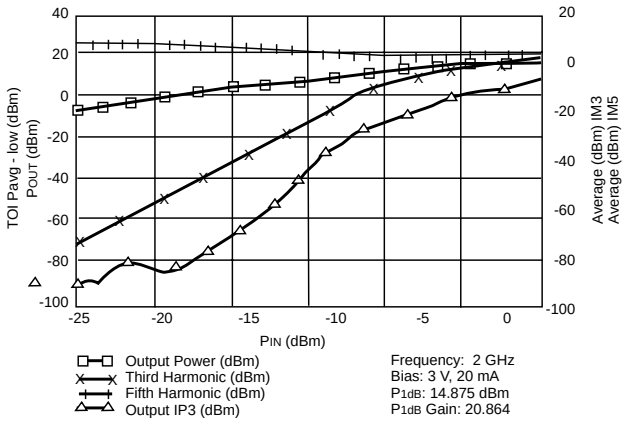


Figure 18. NE34018, 2 GHz, IP3 power matched performance.

High Power Match

Under normal circumstances, few low noise amplifier designers are concerned with the power performance of their amplifiers. However, the recent expansion of digital modulation schemes (such as QPSK or CDMA) has demanded new requirements such as a specified high linearity performance (or high output power). Since this paper focuses only on LNAs, the power amplifier design will not be addressed. However, the inter-modulation performance and some of the power concepts behind the Third Order Intercept Point (IP3) will be reviewed.

In a small signal amplifier, the power levels are low enough that distortion is negligible, and the small signal model or S-Parameters can accurately characterize the device over a wide dynamic range. When the power levels increases to where the device nears saturation, distortion becomes a problem. The transistor's parameters will vary appreciably over the signal's cycle with the input power level. Consequently, the small signal model is no longer valid. The device no longer amplifies linearly, and harmonic components start to be significant. The power performance of the circuit in class A is calculated because the device remains turned on throughout the signal's cycle under the quiescent bias point. As for the high gain and the low noise amplifier, the circuit matching will drive the overall performance of the amplifier. In this situation, the output match will have the most effect on the device's output power and once again the design will be a particular case of gain match theory. The output is fixed to an optimum load for output power while the input is designed for gain and stability criteria.

If the device is biased at V_{CC} and presented with an RF load, R_L (also known as the load line), then the AC current generates a collector output voltage, V_{out}, with its DC component being V_{CC}. The inherent size of the device will limit the maximum current that can be delivered (usually slightly above I_{DSS}) and the breakdown voltages (influenced by the fabrication process of the device) will limit the voltage swing. Assuming the signal to be a sine wave, the output power delivered to the load will be:

$$P_{Out} = \frac{V_{Out}^2}{2R_L} \leq \frac{V_{CC}}{2R_L} \qquad \textbf{(20)}$$

This represents the maximum output power that can be delivered by the device under the quiescent bias point (V_{CC}, I_{CC}) related by:

$$I_{CC} = V_{CC}/R_L.$$

To optimize the power performance under a given bias point, the designer will have to define the appropriate RF load (both real and imaginary) for the circuit. The real part will be the load line, and the imaginary part must tune out the output capacitance of the device. There are several ways to identify such desired loads. DC characteristics and the output parasitics of the device can be used with Steven Cripps' method [6] of defining the optimal match on the Smith chart. Another method is to use RF tuners to experimentally define the output impedance that will yield the best results. **Figures 16 and 17** show such an experiment. In **Figure 16**, diode tuners are used to present the conjugate match to the device and record the corresponding P_{1dB} and P_{sat} (defined in this case as the 3 dB compression point) at 3V, 20 mA. **Figure 17** exhibits the same device tuned with an optimal power load and the same conjugate source match. In this case, the 1 dB compression point improves by 1.3 dB and the saturated power by 1.7 dB. The load was changed from:

$$\Gamma_{Conjugate} = 0.54 < 24.4^{\circ} \text{ to}$$
$$Z_{Opt} = 0.45 < 72.4^{\circ}$$

Figure 18 exhibits the inter-modulation components of the device when presented with Z_{Opt}. When the optimal output impedance is known, the designer can create his output matching network in the same way Γ_{Opt}, S^*_{11} or S^*_{22} were reached and achieve optimal output power. It is important to notice that in order to avoid reducing output power performance, the stabilizing network will have to be in the input or relatively lossless.

Conclusion

This paper describes three different design topologies available to engineers. These designs address amplifiers with a special focus on the PCS band for mobile communication applications. Illustrative examples have been developed and are available as evaluation boards from California Eastern Laboratories. These boards can be used to evaluate the performance of NEC devices. These specific designs address the high gain, low return loss amplifier and the low noise amplifier and use a limited number of matching elements and real estate. Combined with a low part cost, these approaches reduce the overall cost of such an amplifier to a minimum. From a design standpoint, simulators are useful and powerful tools, however, they can be difficult to use and time consuming when a number of variables need to be optimized. This paper reviews some of the analytical techniques that engineers use before simulating and optimizing their designs. When completed, accurate translation of the simulation must be imported into a layout and a test circuit, and this often leads to another round of tuning and optimization. However, this last round is usually minimal, and eventually, laboratory results match the simulation very closely. Part Two of this paper will describe how other techniques, such as series feedback, can be applied to offer an optimal compromise between low noise, excellent input return loss and acceptable IP3 performance for PCS applications.

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