AN-SI-1001

APPLICATION NOTE

Ultrahigh Frequency Transistor Arrays: UPA101/102/103/104

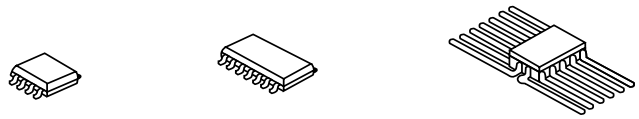
INTRODUCTION

In recent years there has been a rapidly increasing demand for high-frequency amplifiers and high-speed logic devices, chiefly in the fields of instrumentation and optical communi cations. To address these markets, integrated circuits using gallium arsenide are being developed. However, because of the high cost of the GaAs material, these GaAs ICs are frequently too expensive for their intended applications. Therefore, efforts are being made to improve the high frequency performance of Silicon ICs. There are a number of discrete silicon devices with ultra-high frequency characteristics. However, when a number of transistors are connected to configure a circuit, their operating frequency speeds deteriorate because of the parasitic inductances and capacitances of the interconnecting wiring and packages. Therefore, it is difficult to achieve the performance characteristics inherent in each individual transistor.

The DNP-II (Direct Nitride Passivated Base Surface - II) process, a newly developed process for use in Silicon Monolithic ICs, has been used for the ultrahigh frequency UPA101 through 104 transistor arrays to eliminate inter-device stray capacitances and inductances, and to improve the high frequency operation. UPA101/102/103/104 products have multiple NPN transistors on a single substrate. Each transistor has an f_T of 10 GHz. This Application Note discusses the various potential applications. It includes examples of circuits using the arrays in these applications.

SUMMARY

UPA101-104 transistor arrays have a number of NPN transistors with f_T of approximately 10 GHz on a single chip. These devices are available in miniflat packages of 8 and 14 pins, as well as in a 14-pin ceramic package with stud as shown below:



8 Pin Mini-Flat | 14 Pin Mini-Flat | 14 Pin Flat Ceramic

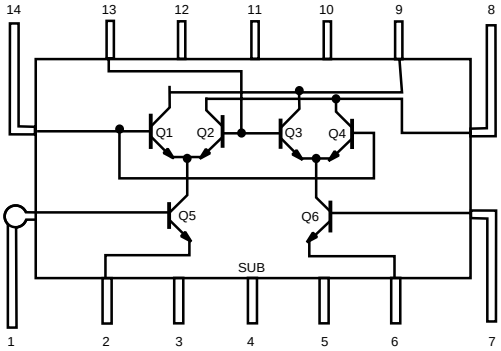
Figure 1 shows equivalent circuits of each array. The arrays have the following functions:

UPA101: Two differential amplifier circuits are connected internally to form a multiplication circuit.

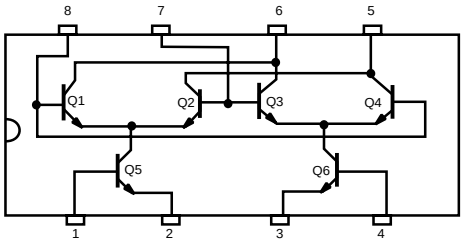
UPA102: Contains two differential amplifier circuits.

UPA103: Contains two transistors whose emitters are connected internally to configure a differential amplifier and three independent transistors for use in circuits such as emitter follower circuits.

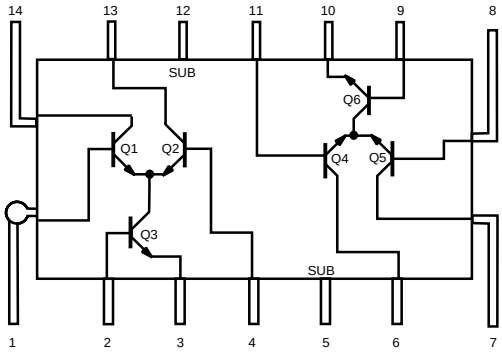
UPA104: Is a two-input addition circuit using the two inputs of one of the differential amplifiers.



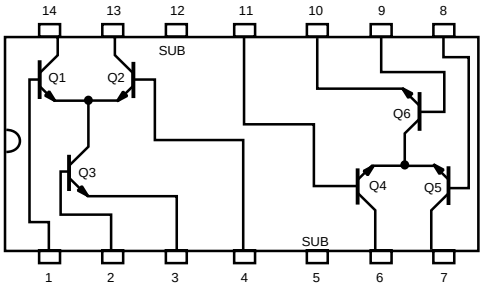
UPA101B



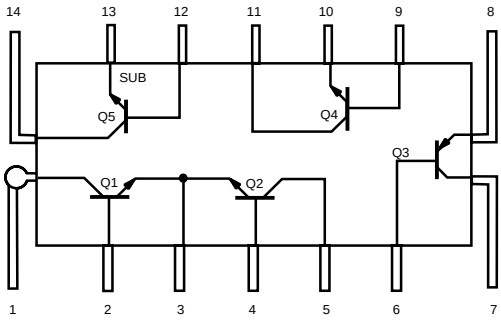
UPA101G



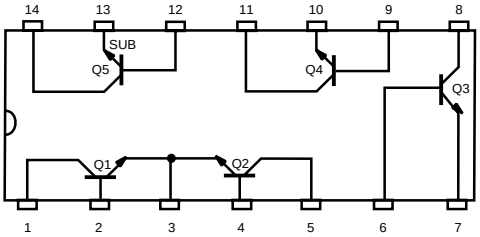
UPA102B



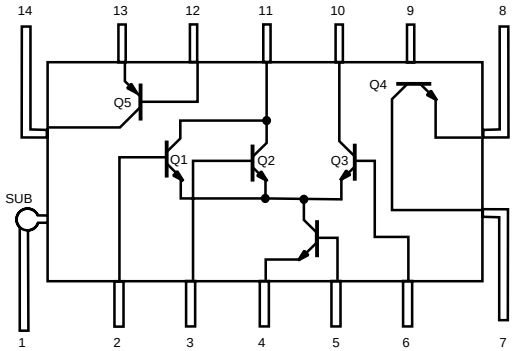
UPA102G



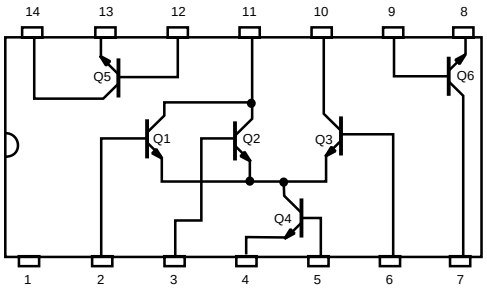
UPA103B



UPA103G



UPA104B



UPA104G

Figure 1. UPA101-104 Equivalent Circuits.

Other characteristics of these arrays are as follows:

• Since the circuits are configured on a single chip, they have excellent matching characteristics for parameters, such as V_{BE} and h_{FE}, achieving a superior balance to form a differential amplifier circuit.

• Since the transistors are internally connected, the inductance and capacitance of the wiring is very small making it possible to achieve high frequencies with these circuits.

• It is possible to miniaturize the circuits with the adoption of miniflat packages and ceramic packages with studs (flat type).

As described above, the arrays have numerous characteristics which cannot be obtained with ordinary configurations using discrete transistors.

CHARACTERISTICS OF TRANSISTORS

The DNP-II process has been applied to these products in order to achieve higher operating frequencies and speeds.

A sectional view of these transistor cells is given in Figure 2. The DNP-11 process has the following features:

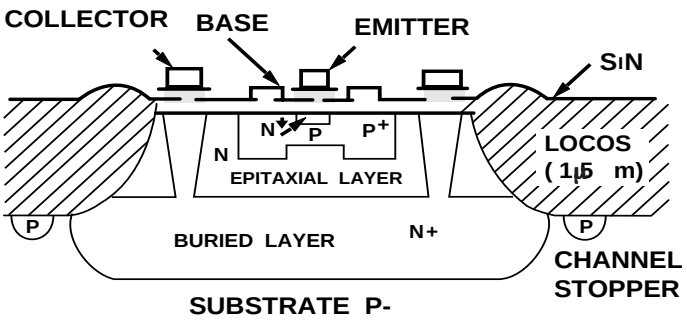


Figure 2. Transistor Cell Cross Section.

• Since oxide films are used to separate the cells, parasitic capacitance between cells is reduced.

• Emitter stripes with a width of 1 µm are formed to lower the base resistance and the junction capacitance between emitter and base.

• A high f_T is achieved by the shallow bases formed by ion implantation and laser annealing and by the use of Arsenic doped Polysilicon emitters.

• The direct nitride deposition (DNP) process is used, making it possible to improve the moisture resistance and to achieve high reliability when plastic packages are used.

All the transistors used in UPA101-104 arrays have the same structure. The f_T as a function of I_C of a single transistor is shown in Figure 3. The gain and NF are shown in Figure 4. These characteristics are measured with the unit transistors packaged in a MICRO-X package, at V_{CE} = 3 V, I_C = 10 mA, f_T = 9 GHz. Under the same bias conditions, the associated gain and NF at f = 1 GHz are 15 dB and 1.8 dB, respectively. Thus, the unit transistors are as good as the best discrete bipolar transistors in f_T, G_A and NF.

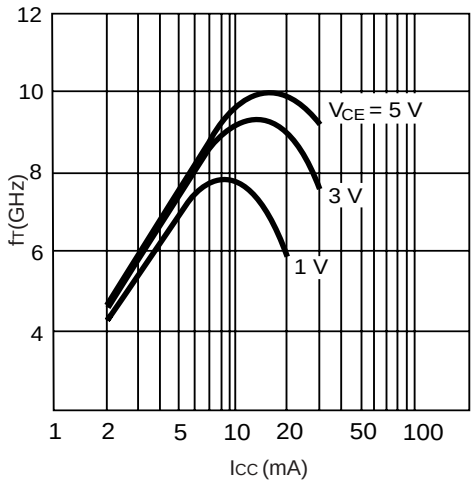


Figure 3. f_T vs. I_C Characteristics.

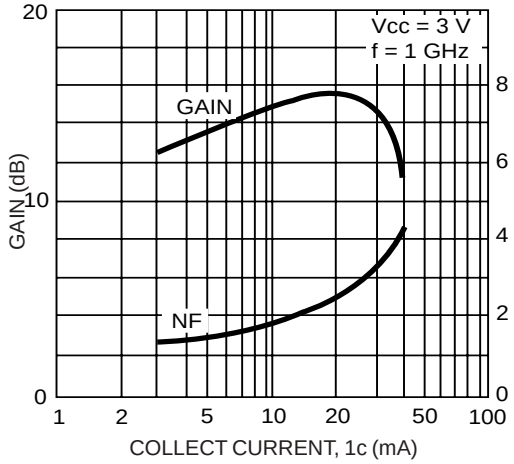


Figure 4. Gain, NF vs. I_C Characteristics.

APPLICATIONS

Applications for UPA101-104 arrays include instruments and optical communications equipment in which ultrahigh frequency and high-speed characteristics are required. The following are typical examples of possible applications for each individual product:

UPA101: Frequency converters, phase comparators, and EXOR gates.

UPA102: Differenfial amplifiers, AGC amplifiers, and inverters.

UPA103: Differential amplifiers, impedance converters, and inverters.

UPA104: OR/NOR gates.

EXAMPLES OF APPLICATION CIRCUITS AND THEIR CHARACTERISTICS

The following are examples of circuits in which UPAl01-104 arrays are used. Their typical performance characteristics are shown.

UPA101
Frequency converters are the typical application for UPA101.

Following are the advantages when using UPA101 as a frequency converter:

• Since the circuit is a multiplication circuit of the bi-differential type, UPA101 can function as a double balanced mixer (DBM) and has little leakage of RF signals and OSC, to the IF port.

• Transformers for the input output circuits are not needed.

• Variable conversion gain is possible by setting the emitter resistance and load resistance externally.

Figure 5 shows a circuit diagram of a frequency converter using UPA101G.

The circuit is biased so that the source voltage is 12 V, and the base voltages are in the vicinity of 7 V and 3.5 V. The bias resistances are chosen such that the frequency converter unit would have a circuit current of 3-4 mA. Should the output level and the tertiary distortion need improving it will be necessary to increase the circuit current.

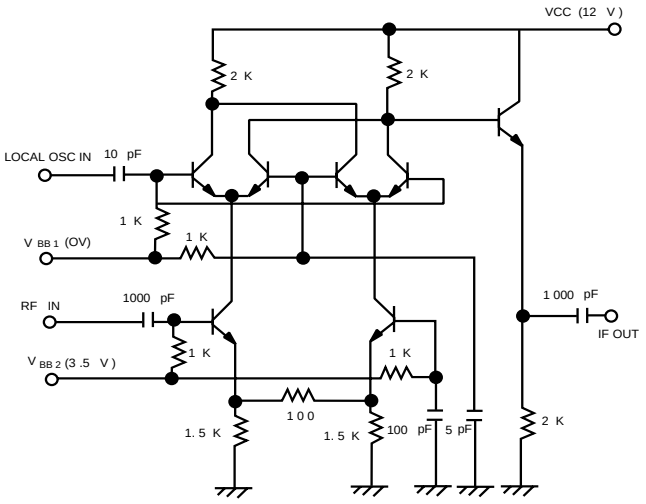


Figure 5. Example of DBM Circuit Using UPA101.

Note that when selecting the source and base voltages, it is necessary to keep the potential difference between collector C, and Emitter, E, to be 6 V or less, as 6 V is the maximum voltage rating for BV_{CEO}.

Next, if an RF signal is applied at the base of the lower transistor and a local oscillator (LO) signal is applied at the base of the upper transistor, a spectrum of frequencies in multiples of the difference of the two input frequencies will appear at the output port. Ordinarily, a low-pass filter or a band-pass filter is inserted in order to extract only the signal desired. In this example an emitter follower circuit is used to drive a 50 Ω load so that the complete output spectrum can be observed.

A bandwidth of 1 GHz at 3 dB down with conversion gain of 12 dB is achieved (refer to Figure 6). Since there is no output filter, 12 dB gain is obtained at each frequency that is 400 MHz higher than the RF and OSC signals (refer to Figure 7).

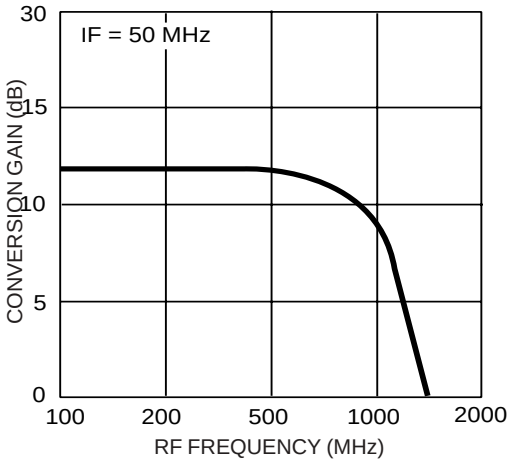


Figure 6. Conversion Gain - f Characteristics (f_{IF} = 50 MHz).

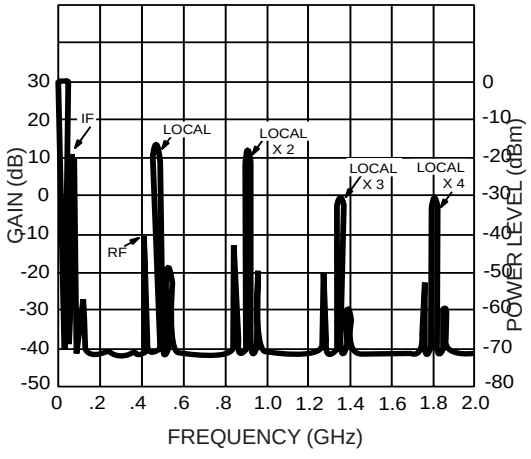


Figure 7. Output Spectrum (@ RF = 400 MHz, -30 dBm input) (Local = 450 MHz, -5 dBm input).

Ordinarily, a conversion gain of 30 dB or more can be expected when an output filter is used.

The frequency is 1.4 GHz at the point where the conversion is 0 dB. If the emitter resistance and load resistance are set so that the conversion gain is 0 dB, it is possible to use the array as a frequency converter with a maximum band of about 1.4 GHz. (The RL/RE ratio is reduced in order to lower the gain.)

This circuit is for use as a frequency converter, but it can also be used as a phase comparator when circuits such as Phase Lock Loop (PLL) are configured.

UPA102/103

The UPA102 and UPA103 arrays are more or less function ally identical. UPA102 contains two differential amplifier circuits. UPA103 contains a pair of transistors connected in common at the emitters so that a differential amplifier can be configured, as well as three single transistors which are used in circuits such as emitter follower circuits. The main application of both will be as a differential amplifier with emitter follower circuits using the 3 single transistors.

Figure 8 is a circuit diagram of the UPA 102G as a differential amplifier, and Figure 9 gives the frequency and current characteristics of the gain. The following characteristics are obtained when there is a load resistance of 100 Ω:

When Ic = 5 mA, the gain (flat part) is 8.5 dB, and the frequency band width is 1.0 GHz.

When Ic = 10 mA, the gain is 14 dB, and the frequency band width is 900 MHz.

When Ic = 20 mA, the gain is 17 dB, and the frequency band width is 700 MHz.

At each current value, the frequency, of 0 dB gain, is approximately 1.5 GHz. This matches the frequency characteristics of UPA101G as a frequency converter.

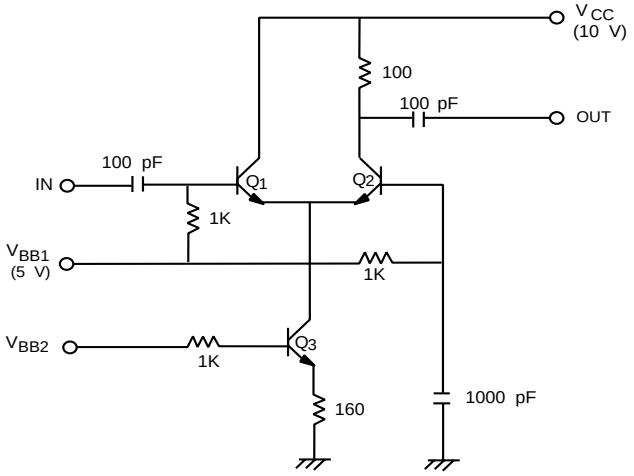


Figure 8. Circuit Diagram of Measuring Circuit Used in a Differential Amplifier.

UPA104

The UPA104 has an additional input to one side of the differ ential amplifier and 2 single transistors.

An example of a UPA104B application circuit, in which

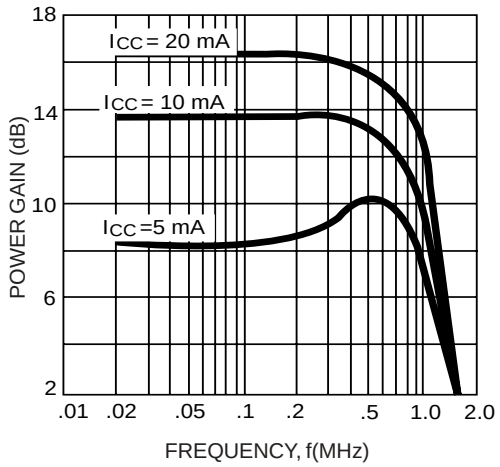


Figure 9. UPA102G Gain-Frequency Characteristics.

UPA104B is used as an OR/NOR gate of the ECL type, is shown in Figure 10. The results obtained are switching times of 500 psec (tPLH) and 250 psec (tPLH), a rise time (tR) of 750 psec, and a fall time (tF) of 500 psec. These are approximately twice the speed of state-of-the-art high-speed ECL circuits. The circuits may be used most suitably in applications for measuring instruments (in which higher processing speed properties are required) and receivers in optical communications.

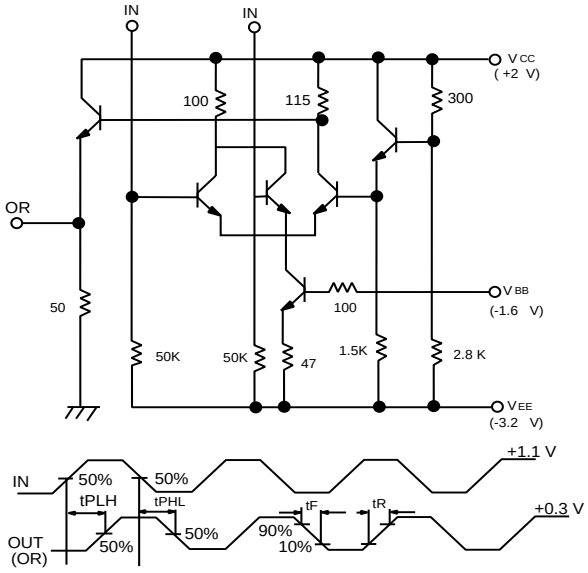


Figure 10. Example of ECL OR Circuit.
(Voltage values enclosed in parentheses are values added during measurement, not the voltage used in the actual applied circuit.)

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