AN1298

Variations in the MC68HC(7)05Cx Family

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Introduction

The Motorola MC68HC05 C Family of 8-bit microcontrollers is one of the largest and most widely used. The devices within the family have many variations, so this application note has been compiled in order to clarify the important differences. It is intended for anyone who may be developing an application using one of these devices. It is particularly useful for someone who is familiar with one member of the family, but wishes to move to another. As Motorola is constantly improving specifications and optimizing it's portfolio, the reader is encouraged to consult the latest data books for specification details and availability.

This application note discusses:

- Similarities
- Comparisons
- The A Strategy
- MC68HC705C9A and MC68HC705C12A
- Changing from Non-A to A Versions
- Changing from OTP (One-Time Programmable) to ROM Versions
- Changing from the 705C8A to the 705C9A
- Voltage, Frequency, and Temperature Tables
- Development Tools
- Related Documentation

Similarities

All members of the C Family of devices have the features discussed in this section.

16-Bit Input Capture/Output Compare Timer

The timer core is a 16-bit free-running counter, which provides the timing reference for the input capture and output compare functions. The input capture and output compare functions provide a means of latching the times at which external events occur and generating output waveforms and timing delays.

SCI (Serial Communications Interface)

The SCI allows full duplex, asynchronous RS232 or RS422 serial communication between the MCU and remote devices, including other MCUs. The transmitter and receiver operate independently, although they use the same baud rate generator.

The main SCI features are:

- Standard Mark/Space Non-Return-to Zero Format
- Full Duplex Operation
- 32 Programmable Baud Rates
- Ability to be Interrupt Driven
- Four Separate Interrupt Conditions
- Software Selectable Word Lengths of Eight or Nine Bits
- 1/16 Bit Time Noise Detection

The HC05C0, HC05C5, and 705C5 are the only members of the C Family that do not have an SCI.

SPI (Serial Peripheral Interface)

The SPI is an interface which allows several MCUs or MCUs plus peripheral devices to be interconnected within a single printed circuit board or over short distances between circuit boards. With the SPI, separate wires are required for data and clock, as the clock is not included in the data stream. The SPI may be configured in a system containing one master MCU and several slave MCUs or in a multi-master system in which an MCU is capable of being a master or a slave.

The main SPI features are:

- Full Duplex Operation
- Master and Slave Modes
- Four Programmable Master Bit Rates
- Programmable Clock Polarity and Phase
- End of Transmission Interrupt Flag
- Write Collision and Bus Contention Flags

The HC05C0, HC05C5, and 705C5 are the only members of the C Family which do not have an SPI.

Variations

The C Family device variations are summarized in **Table 1** and **Table 2** and are detailed in the following sections.

NOTE: *The HC05C5 and HC705C5 are not recommended for new designs. The HC05C8A and HC705C8A are recommended as replacements.*

Table 1. Comparisons Among the C Family Devices

	05C0	05C4	05C4A	705C4A	05CJ4	705CJ4	05C5	705C5
COP	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
COP Enable	Software	—	Mask Option	MOR	Software	Software	Mask Option	MOR
COP Timeout	Software Selectable	—	64 ms @ 4 MHz Osc	64 ms @ 4 MHz Osc	Software Selectable	Software Selectable	64 ms @ 4 MHz Osc	64 ms @ 4 MHz Osc
COP Clear	CLR Bit 0 $FFFF	—	CLR Bit 0 $1FF0	CLR Bit 0 $1FF0	CLR Bit 0 $1FF0	CLR Bit 0 $1FF0	CLR Bit 0 $1FF0	CLR Bit 0 $1FF0
Clock Monitor	No	No	No	No	No	No	No	No
STOP Disable	Config Register	No	Mask Option	No	Mask Option	No	No	No
PORTD	8-Bit Bidirectional	PD7, 5–0 Input Only	PD7, 5–0 Input Only	PD7, 5–0 Input Only	Fixed Input Port	Fixed Input Port	8-Bit Bidirectional	8-Bit Bidirectional
PORTB Pullup Interrupt	No	No	Yes, Mask Option	Yes, MOR Selectable	No	No	No	No
PC7 Drive	No	Standard	High Current	High Current	High Current	High Current	High Current, 8 Bits, Port C	High Current, 8 Bits, Port C
RAM	512	176	176	176	224	224	176	176
User EPROM, Excluding Vectors	64946 External Address Space	4144	4144	4192	3840	3840	5168	5168
Security	No	No	Yes	Yes	No	No	No	No
(Mask) Option Registers	Config Register	No	No	$1FF0–$1FF1	No	No	No	$1E80
Recommended OTP		705C4A	705C4A		705CJ4		705C5	

Table 2. Comparisons Among the C Family Devices

	05C8	05C8A	05C12	05C12A	05C9	05C9A	705C8	705C8A	705C9	705C9A
COP	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes, 2 Types	Yes	Yes, 2 Types
COP Enable	—	Mask Option	Mask Option	Mask Option	Software	Software	Software	Software + MOR	Software	Software, (C9A) + MOR (C12A)
COP Timeout	—	64 ms @ 4 MHz Osc	64 ms @ 4 MHz Osc	64 ms @ 4 MHz Osc	Software Selectable	Software Selectable	Software Selectable	Software + MOR Selectable	Software Selectable	Software + MOR Selectable
COP Clear	—	CLR $1FF0	CLR $3FF0	CLR $3FF0	Write $55/ $AA to $001D	Write $55/$AA to $001D	Write $55/ $AA to $001D	Write $55/$AA to $001D or CLR $1FF0	Write $55/$AA to $001D	Write $55/$AA to $001D or CLR $3FF0
Clock Monitor	No	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes, C9A Mode
STOP Disable	No	Mask Option	Mask Option	Mask Option	No	No	No	No	No	MOR Selectable, C12A Mode On
PORTD	PD7, 5–0 Input Only	PD7, 5–0 Input Only	PD7, 5–0 Input Only	PD7, 5–0 Input Only	PD7, 5–0 Bidirec-tional	PD7, 5–0 Bidirec-tional	PD7, 5–0 Input Only	PD7, 5–0 Input Only	PD7, 5–0 Bidirec-tional	PD7, 5–0 Bidirec-tional
PORTB Pullup Interrupt	No	Yes	Yes, Mask Option	Yes, Mask Option	No	Yes	No	Yes, MOR Selectable	No	Yes, MOR Selectable
PC7 Drive	Standard	High Current	High Current	High Current	Standard	High Current	Standard	High Current	Standard	High Current
RAM	176	176	176	176	176–352	176–352	176–304	176–304	176–352	176–352
User EPROM, Excluding Vectors	7728	7728	12080	12080	15744–15920	15744–15920	7584–7728	7584–7728	15744–15920	12032–15920
Security	No	Yes	No	Yes	No	Yes	Yes	Yes	No	Yes
(Mask) Option Registers	No	No	No	No	No	$3FDF	No	$1FF0–$1FF1, $1FDF	No	$3FF0–$3FF1, $3FDF
Recom-mended OTP	705C8A	705C8A	705C9A	705C9A	705C9A					

Programmable and Non-Programmable COP

A COP watchdog (computer operating properly) is used in a system to make sure that the software does not execute incorrectly. At regular intervals, the COP must be reset. If this does not happen, for instance, because the application software has “run away” or it has entered a loop that it cannot exit from, the COP will time out, causing the MCU to reset. **Table 3** summarizes the COPs that are available on C Family devices.

Table 3. COPs Available on C Family Devices

COP	05C0	(7)05CJ4	705C5	(7)05C4A	05C8A	705C8(A)	05C9A	705C9(A)	C12(A)
Programmable	Yes	Yes	No	No	No	Yes, A and Non-A	Yes	Yes, A and Non-A	No
Non-Programmable	No	No	Yes	Yes	Yes	Yes, A Only	No	Yes, A Only, C12A Mode Only	Yes, A and Non-A

Programmable COP

Except for the HC05C0, HC05CJ4, and the 705CJ4, the programmable COP is enabled by setting the PCOPE in the COP control register at address $001E. By using two other bits in this register, one of four timeout periods can be selected. The COP is then periodically reset by writing $55 then $AA to the COP reset register at address $001D.

On the HC05C0, the COP is enabled by setting bit 5 (COPEN) in the configuration register at location $0019. The COP is incorporated as part of the multifunction timer and the timeout period is set by manipulating two bits in the timer status and control register at address $0008. The COP is reset by writing a zero to bit 0 of location $FFFF.

On the HC05CJ4 and the HC705CJ4, the COP is enabled by setting bit 3 (COPE) of the timer control and status register at location $0013. It is incorporated as part of timer 2 and the timeout period is set by manipulating two bits in the timer 2 control and status register. The COP is reset by writing a zero to bit 0 of $1FF0.

Non-Programmable COP

Non-programmable means that the COP timeout period is fixed, unlike the other COP available where a choice of four timeout periods can be selected. It is implemented with an 18-bit ripple counter and the timeout period is 64 milliseconds at a bus rate of 2 MHz.

On the ROM 05C4A, 05C5, 05C8A and 05C12A, this COP is enabled as a metal mask option. On the EPROM devices (except the 705C5), the COP is enabled by programming bit 0 (NCOPE) of the second of the new mask option registers to a one. On the 705C4A and the 705C8A, this resides at location $1FF1 and on the EPROM version of the C12A it is at address $3FF1.

On the 705C5, there is only one mask option register at location $1E80. To enable the COP, bit 0 of this register is set to one.

To clear the COP and start a new timeout period, a zero must be written to bit 0 of $1FF0 on the 05C4A, 705C4A, 705C5, 05C8A, and 705C8A and $3FF0 on the EPROM and the ROM version of the 05C12A.

NOTE: *This means the 705C8A has two COP systems, but the matching ROM device (05C8A) has only the fixed COP timeout period. Care must, therefore, be taken when using the 705C8A for development of a ROM code for the 05C8A.*

*As seen from **Table 3**, the 705C9A also has two COP systems. The 705C9A also can be configured as the EPROM version of the 05C12A. When it is configured as a 705C9A, it is the programmable COP that is enabled, for instance, a selectable timeout period. When it is configured as the EPROM version of the C12A, it is the non-programmable COP that is enabled. See the section **MC68HC705C9A and MC68HC705C12A** for more details.*

Clock Monitor

The only C Family devices with a clock monitor are:

- HC05C9
- HC05C9A
- HC705C9
- HC705C9A
- HC705C8
- HC705C8A

On these devices, the clock monitor is enabled by setting bit 3 (CME) of the COP control register at location $001E.

Input/Output (I/O)

Port B Interrupts/Pullups

Port B pullups are available on the HC05C12 and all the A devices. The approximate input pullup current on the HC05C12 is 20 µA @ 5 volts. See **The A Strategy** section for more information on the A parts.

PC7 Drive

With the exception of the HC05CJ4 and the HC705CJ4, the increase in the output current drive capability on port C pin 7 is available only on the A devices.

On the HC05C5 and the HC705C5, port C has a high-current sink capability of 10 mA per pin.

Port D

With the exception of the HC05C0, HC05C5, HC705C5, HC05C9, HC05C9A, HC705C9, and the HC705C9A, where port D is a bidirectional port, on all other C Family devices port D is an input-only port. Also, only the HC05C0, HC05CJ4, HC705CJ4, HC05C5 and the HC705C5 have a full 8-bit port D. All other C Family devices have only seven bits of port D implemented (no PD6).

The devices with an SPI subsystem (see the **SPI (Serial Peripheral Interface)** section) share some of their port D pins with the SPI. On the HC05C9, HC05C9A, 705C9, and 705C9A, the port D data direction register must be programmed as an output if the SPI subsystem is to be

used. This is not necessary for the other devices, which have an SPI, because port D is uni-directional. However, when the SPI is enabled, the dedicated port D pins become outputs.

STOP Disable

These devices do not have a STOP disable function:

- HC05C9
- HC05C9A
- HC705C9
- HC705C9A
- HC05C4
- HC705C4A
- HC05C8
- HC705C8
- HC705C8A
- 705CJ4
- HC05C5
- HC705C5

On all other devices, except the HC05C0, STOP can be disabled by a mask option. On the HC05C0, STOP is disabled by clearing a bit in the configuration register.

The only OTP (one-time programmable) device which supports the STOP disable function is the EPROM version of the HC05C12A.

Packaging

Table 4 shows the different packages that are available for each member of the C Family.

Table 4. C Family Packages

Package	05C0	(7)05CJ4	(7)05C5	(7)05C4A	05C8A	705C8(A)	05C9A	705C9(A)	05C12(A)
40-Pin PDIP	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
44-Lead PLCC	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
44-Lead QFP	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
42-Pin SDIP	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Except for the HC05C0, the 40-pin DIP, 42-SDIP, and 44-pin QFP, packages are all pin-for-pin compatible. **Table 5** shows the only variations in the 44-PLCC package, where NC means that the pin is not connected to the die.

For the HC05C0, refer to the specification.

Table 5. Variations in Pin Assignments of 44-PLCC Package

Pin No.	05C4	05C4A	705C4A	(7)05C5	05C8	05C8A	705C8	705C8A	05C9	05C9A	705C9	705C9A
17	PB4	PB4	PB4	PB4	PB4	PB4	PB4	PB4	NC	NC	NC	NC
18	NC	NC	NC	NC	NC	NC	NC	NC	PB4	PB4	PB4	PB4
39	PD7	PD7	PD7	PD7	PD7	PD7	PD7	PD7	NC	NC	NC	NC
40	NC	NC	NC	NC	NC	NC	NC	NC	PD7	PD7	PD7	PD7
3	NC	NC	NC	NC	NC	NC	NC	NC	V_{PP}	V_{PP}	V_{PP}	V_{PP}
4	V_{PP}	V_{PP}	V_{PP}	V_{PP}/PE	V_{PP}	V_{PP}	V_{PP}	V_{PP}	NC	NC	NC	NC

NOTE: *On EPROM parts, a minimum voltage of V_{DD} must be applied to the V_{PP} pin at all times because a lower voltage could damage the device.*

EPROM Security

How the EPROM is protected varies from device to device. **Table 6** shows the different ways this feature is enabled.

Table 6. Methods of Securing EPROM on C Family Devices

Method of Securing EPROM	05C4A	705C4A	05C8A	705C8(A)	05C9A	705C9A	05C12A
Fixed During Manufacturing	Yes	No	Yes	No	Yes	No	No
Option When Using Programmer Board	No	Yes	No	Yes, A and Non-A	No	Yes	Yes
Set Bit 3 (SEC) of Option Register (1FDF)	No	Yes	No	Yes, A and Non-A	No	No	No
Set Bit 7 (SEC) of MOR ($3FF1)	No	No	No	No	No	Yes	Yes

The A Strategy

The A strategy was introduced in the C Family and other families within the Motorola 8-bit microcontroller portfolio to enhance the features that the device offered. The A features include port B interrupts/pullups, non-programmable COP, and high-current drive on port C.

Port B Interrupts/Pullups

The enabling and disabling of the port B pullups are governed by manipulating the first of two new mask option registers which have been added on the A parts. This MOR resides at address $1FF0 on the 705C4A and 705C8A and $3FF0 on the 705C9A and the EPROM version of the C12A. On the ROM versions, this option is available as a metal mask option, selected at the time of ROM code submission to the factory. By enabling these mask options, the implementation of some applications, such as a keypad, can be simplified. **Figure 1** shows the port B input/output (I/O) logic on the A devices.

The approximate input pullup current drawn from these resistors is:

- 385 µA @ 5 volts — HC05C4A, HC05C8A, HC705C9A, and HC05C12A
- 90 µA @ 5 volts — HC705C4A and HC705C8A
- 20 µA @ 5 volts — HC05C9A

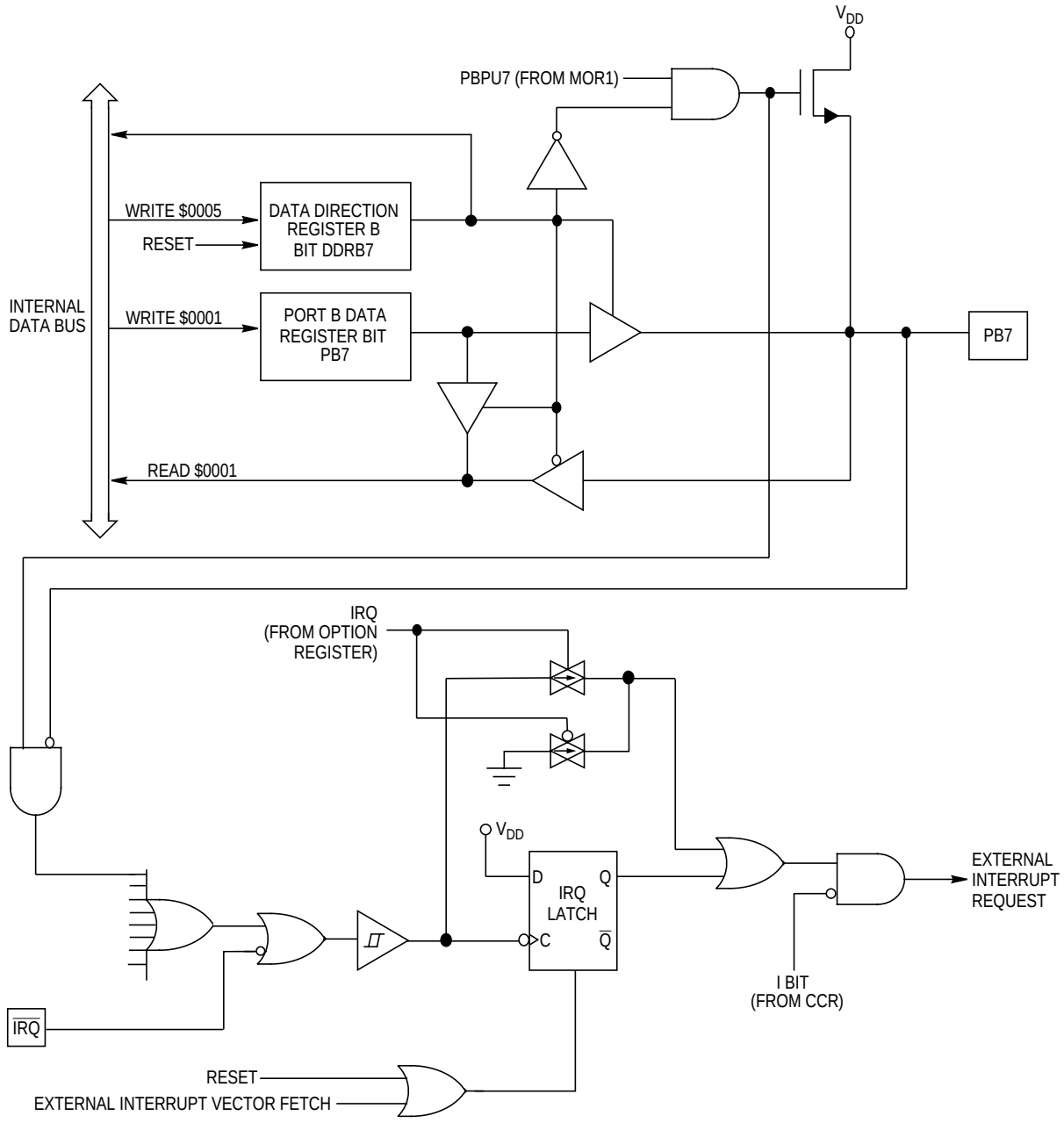

Figure 1. Port B I/O Logic on A Devices

Non-Programmable COP

On the 05C4A, 05C8A, and the 705C8A, a non-programmable COP has been added. See **Variations** for more details on the non-programmable COP.

High-Current Drive on Port C

The output current drive capability on port C bit 7 has been increased to provide enough current to drive an LED. See **Figure 2**.

Characteristic	Non-A Part	A Part
V_{DD} = 5.0 Volts PC7 Current Drive (I_{OH}) @ $V_{OH} = V_{DD} - 0.8$ Volts PC7 Current Sink (I_{OL}) @ V_{OL} = 0.4 Volts	 0.8 mA 1.6 mA	 5.0 mA 20.0 mA
V_{DD} = 3.0 Volts PC7 Current Drive (I_{OH}) @ $V_{OH} = V_{DD} - 0.3$ Volts PC7 Current Sink (I_{OL}) @ V_{OL} = 0.3 Volts	 0.2 mA 0.4 mA	 1.5 mA 6.0 mA

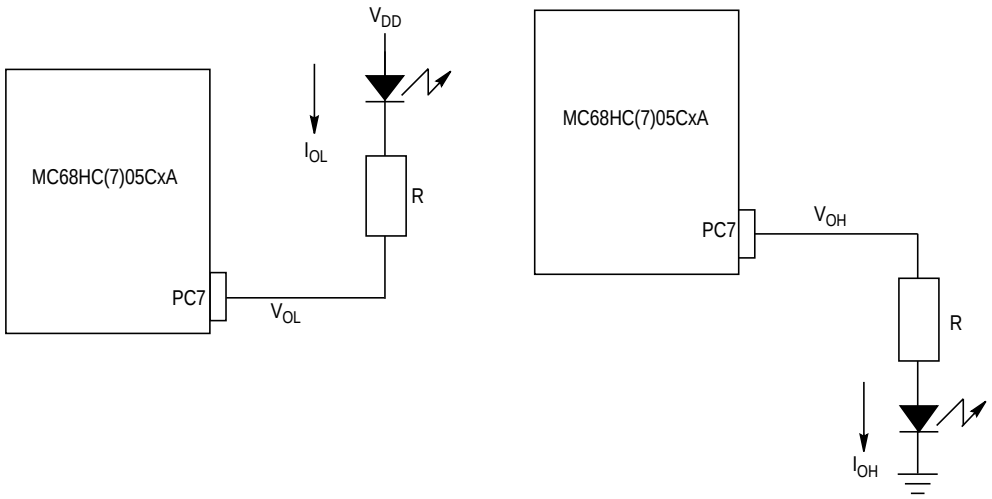

Figure 2. PC7 on the A Devices Driving an LED

MC68HC705C9A and MC68HC705C12A

The 705C9A is the EPROM version of the 05C9A, but it also can be configured as the EPROM version of the 05C12A. The desired configuration is chosen by manipulating bit 0 in the mask option register, address $3FF1. To configure the device as a C12A, this bit must be set to a one and for a C9A it must be set to a zero. **Figure 3** shows the memory map.

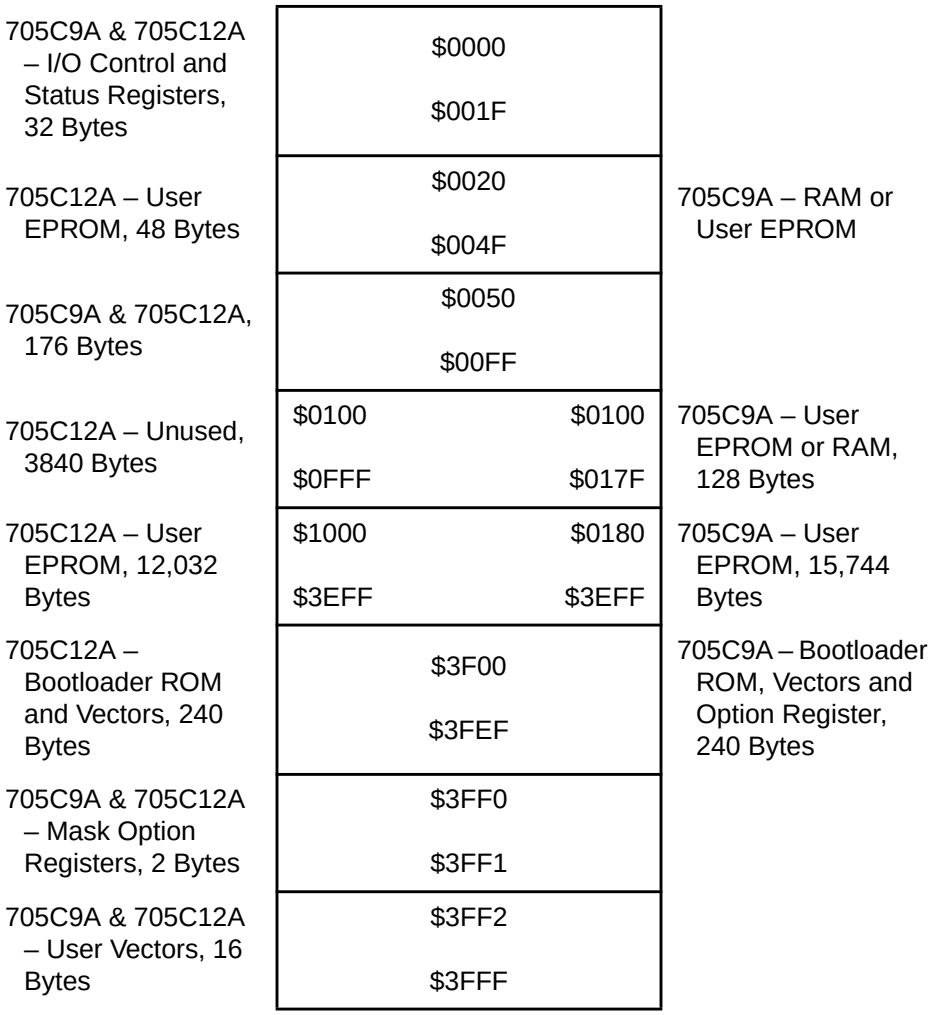

Figure 3. MC68HC705C9A/705C12A Memory Map

When configured as an HC05C9A:

- The entire 16-K memory map of the 05C9A is enabled, including dual-mapped RAM and EPROM at locations $0020–$004F.
- C12A options in the C12 mask option register are disabled.
- The C9A option register ($3FDF) is enabled, allowing software control over the IRQ sensitivity and the memory map configuration.
- The C9A COP reset register ($001D) and the C9A COP control register ($001E) are enabled, allowing software control over the C9A COP and clock monitor.
- The C12A COP clear register ($3FF0) is disabled.
- The port D data direction register ($0007) is enabled, allowing output compatibility on the seven port D pins.
- SPI output signals (MOSI, MISO, and SCK) require the corresponding bits in the port D data direction register to be set for output.
- The port D wire-OR mode control bit (bit 5 in the SPI control register) is enabled, allowing open drain configuration of port D.
- The $\overline{\text{RESET}}$ pin becomes bidirectional. This pin is driven low by an C9A COP or clock monitor timeout or during power-on reset.

When configured as an HC05C12A:

- Memory locations $0100–$0FFF are disabled, creating a memory map identical to the HC05C12A.
- C12A options in the C12 mask option register ($3FF1) are enabled. These bits control $\overline{\text{IRQ}}$ sensitivity, STOP instruction disable, and C12 COP enable.
- The C9A option register ($3FDF) is disabled, preventing software control over the $\overline{\text{IRQ}}$ sensitivity and the memory map configuration.
- The C9A COP reset register ($001D) and the C9A COP control register are disabled, preventing software control over the C9A COP and the clock monitor.
- The port D data direction register ($0007) is disabled and the seven port D pins become input only.
- SPI output signals (MOSI, MISO, and SCK) do not require the data direction register control for output capability.
- The port D wire-OR mode control bit (bit 5 of the SPI control register) is disabled, preventing open drain configuration of port D.
- The $\overline{\text{RESET}}$ pin becomes input only.

Changing from Non-A to A

When changing from the non-A parts to the A parts, note these points:

1. If the user requires compatibility when changing from the non-A to the A device, make sure that the two extra mask option registers on the A part contain $00.
2. When changing from the 705C9 to the 705C9A, remember that the erased state of the EPROM area is different. On the 705C9, the erased state is $FF. On the 705C9A, the erased state of the EPROM is $00. The erased state of the other parts remains unchanged when the other parts go to their A equivalents.
3. Shrink level — The A parts are manufactured as 1.2 μm technology or below, where the non-A parts are 1.75 μm technology. While the electrical and functional specifications of the device remain unchanged, the EMC performance of a device may change with package type, shrink level, ROM size and type of programmable memory (EPROM or ROM). Every new MCU should be treated and tested independently. Sensible application design guidelines should be used to minimize the noise presented to the MCU.

   Three application notes, designed to help customers develop good EMC behavior into their applications, are available. These can be ordered through the usual Motorola channels as documents:

   - AN1263 — “Designing for Electromagnetic Compatibility with Single-Chip MCUs”
   - AN1050 — “Designing for Electromagnetic Compatibility with HCMOS MCUs”
   - AN1259 — “System Design and Layout Techniques for Noise Reduction in MCU-Based Systems”

4. The functionality of the 705C9A bootloader is different from the 705C9. The A device has no option to dump the EPROM contents, where the non-A device does have this option. All other bootloader options remain unchanged. See **Development Tools** for more details on the bootloader options.
5. The development systems remain unchanged. For all the A devices, the emulator is the M68EM05C9A and the programmer board is the MC68HC05PGMR-2.

Changing from OTP to ROM

When changing from OTP (one-time programmable) to ROM within the C Family, note the following:

- The 705C8A has two COP systems, but the matching ROM device, the HC05C8A, has only the fixed COP timeout period. Care must be taken, therefore, when using the 705C8A for development of a ROM code for the 05C8A.
- The facility to disable stop mode on the ROM parts is not available on the EPROM parts, with the exception of the EPROM version of the 05C12A, where the STOP disable can be emulated.
- ROM security is not an option on the ROM A parts, although there is an option on the EPROM A parts. On the ROM parts, security is enabled during the manufacturing process.
- When changing from the 705C8A to the HC05C8A, note that on the ROM part the memory areas from $0020–$004F and from $0100–$015F are fixed as ROM. On the EPROM part these areas can be chosen to be RAM or ROM.

Changing from the 705C8A to the 705C9A

When changing from the 705C8A to the 705C9A, note:

- The memory maps differ on the two devices. Refer to **Figure 3** which shows the 705C9A memory map. Note the differences in the address ranges of the PROM and user vectors in the two devices and also the addresses of the mask option registers and the options register.
- The 705C8A has both the programmable and non-programmable COP. The 705C9A has the programmable COP only.
- The port B pullups have different values. The 705C8A has an approximate input pullup current of 90 μA @ 5 V. The 705C9A input pullup current is approximately 385 μA @ 5 V.
- If the SPI is being used, the 705C9A requires that port D is set up as an output by setting the appropriate bits in the port D data direction register. This is not necessary on the 705C8A because port D is an input-only port.
- There are differences in the pin assignments of the PLCC package. Refer to **Table 5** for more information.
- Differences exist in how the PROM is protected. Refer to **Table 6** for more information.

Voltage, Frequency, and Temperature Tables

Table 7 provides the voltage, speed, and temperature specifications for the C Family.

Temperature ranges are:

- 0 °C to +70 °C
- C = –40 °C to +85 °C
- V = –40 °C to 105 °C
- M = –40 °C to 125 °C

Use these part numbers when ordering the 705C4A and the 705C8A high-speed options:

- MC68HSC705C4A
- MC68HSC705C8A

The high-speed option on the ROM devices is chosen at the time of submission of ROM code to the factory.

Table 7. Voltage, Speed, and Temperature Specifications for the C Family

Device	Maximum Bus Speed/Voltage Options	Temperature	Comments
HC05C0	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz	0–70	
HC05CJ4	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz	0–70, C 0–70, C	
705CJ4	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz	0–70, C 0–70, C	
HC05C4A	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz 5 V ± 10% / 4 MHz 2.4 V to 3.6 V / 2 MHz 5 V ± 10% / 2.1 MHz 2.4 V to 3.6 V / 1 MHz	0–70, C, V, M 0–70, C, V, M 0–70 Only 0–70 Only 0–70 Only 0–70 Only	 High Speed High Speed Low Power Low Power
705C4A	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz 5 V ± 10% / 4 MHz 3.3 V ± 0.3 V / 2.1 MHz	0–70, C, V, M 0–70, C, V, M 0–70, C, V, M 0–70, C, V, M	 High Speed High Speed
HC05C5	5 V ± 10% / 2.1 MHz	0–70, C	
705C5	5 V ± 10% / 2.1 MHz	0–70, C	
HC05C8A	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz 5 V ± 10% / 4.1 MHz 2.4 V to 3.6 V / 2.1 MHz 5 V ± 10% / 2.1 MHz 2.4 V to 3.6 V / 1 MHz 1.8 V to 3.6 V / 0.5 MHz	0–70, C, V, M 0–70, C, V, M 0–70 Only 0–70 Only 0–70 Only 0–70 Only 0–70 Only	 High Speed High Speed Low Power Low Power Low Power
705C8A	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 / 1 MHz 5 V ± 10% / 4 MHz 3.3 V ± 0.3 V / 2.1 MHz	0–70, C, V, M 0–70, C, V, M 0–70, C, V, M 0–70, C, V, M	 High Speed High Speed
HC05C12A	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz 5 V ± 10% / 4 MHz 2.4 V to 3.6 V / 2.1 MHz 5 V ± 10% / 2.1 MHz 2.4 V to 3.6 V / 1 MHz 1.8 V to 3.6 V / 0.5 MHz	0–70, C, V, M 0–70, C, V, M 0–70 Only 0–70 Only 0–70 Only 0–70 Only 0–70 Only	 High Speed High Speed Low Power Low Power Low Power
HC05C9	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz	0–70, C, V, M 0–70, C, V, M	

Table 7. Voltage, Speed, and Temperature Specifications for the C Family (Continued)

Device	Maximum Bus Speed/Voltage Options	Temperature	Comments
705C9	5 V ± 10% / 2 MHz	0–70, C	
HC05C9A	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz 5 V ± 10% / 4 MHz 2.4 V to 3.6 V / 2.1 MHz 5 V ± 10% / 2.1 MHz 2.4 V to 3.6 V / 1 MHz	0–70, C, V, M 0–70, C, V, M 0–70 Only 0–70 Only 0–70 Only 0–70 Only	 High Speed High Speed Low Power Low Power
HC705C9A	5 V ± 10% / 2.1 MHz 3.3 V ± 0.3 V / 1 MHz	0–70, C 0–70, C	

Development Tools

Table 8 summarizes the development tools that are available for the C Family devices.

With the exception of the 705C5 and the 705CJ4, all the C Family EPROM parts use the M68HC05PGMR-2 programmer board. The options provided when using this programmer board, together with the bootloader codes inside the device, are:

- Program and verify PROM
- Verify PROM contents
- Secure PROM contents and verify
- Secure PROM contents and dump
- Load program into RAM and execute
- Execute program in RAM
- Dump PROM contents

NOTE: *The 705C9A is the only EPROM device which does not have the option to dump the EPROM contents.*

The 705C5 uses the MC68HC705PGMR and the 705CJ4 uses the M68PGMR05CJ4. Neither of these devices has the secure options mentioned in this application note.

Table 8. C Family Development Tools

Device	Emulator Order Number	Package	Target Cable	Comments
05C5	M68EM05C0	40 DIP	M68CBL05B + M68TB05C0P40	
		44 QFP	M68CBL05C + M68TC05C0FB44	
		42 SDIP	M68CBL05B + M68TB05C0B42	
		44 PLCC	M68CBL05C + M68TC05C0FN44	
05C4, 05C4A, 705C4A, 05CA, 05C8, 05C8A, 705C8, 705C8A, 05C9, 05C9A, 705C9, 705C9A, 05C12, 05C12A	M68EM05C9A	40 DIP	M68CBL05B + M68TB05C9P40	Use with M68PFB05 Kit or M68MMDS05
		44 QFP	M68CBL05C + M68TC05C9FB44	As Above, C4 not in QFP
		42 SDIP	M68CBL05B + M68TB05C9B42	As Above, Only 05C9, 05C9A, 705C9, 705C9A
		44 PLCC	M68CBL05C + M68TC05C4FN44; For 05C9, 05C9A – M68CLB05C + M68TC05C9FN44	As Above
05CJ4, 705CJ4	M68EM05CJ4	44 QFP	M68CBL05C + M68TC05CJ4FB44	
05C5, 705C5	M68HC05C5EVS	40 DIP	Ribbon Cable	

Related Documentation

Additional helpful documentation on this subject includes:

- AN1226 — “Use of the M68HC705C8A in Place of the MC688HC705C8”
- M68HC05AG/AD — *HC05 Applications Guide*

Device Literature

Table 9 shows the literature available for the C Family devices.

Table 9. Device Literature

Device	Title	Order Reference Number
HC05C0	General Release Specification	HC05C0GRS/D
HC05C4	Advance Information	AD1991R2
HC05C4A	General Release Specification	HC05C4AGRS/D
HC705C4A	Technical Data	MC68HC705C4A/D
HC05CJ4	General Release Specification	HC05CJ4/GRS/D
HC05C5	General Release Specification	HC05C5GRS/D
HC705C5	General Release Specification	HC705C5GRS/D
HC05C8	Advance Information	AD1991R2
HC05C8A	General Release Specification	HC05C8AGRS/D
HC705C8	Technical Data	MC68HC705C8/D
HC705C8A	Technical Data	MC68HC705C8A/D
HC05C9	Technical Data	MC68HC05C9/D
HC05C9A	General Release Specification	HC05C9AGRS/D
HC705C9A	General Release Specification	HC705C9AGRS/D
HC05C12	Technical Data	MC68HC05C12/D
HC05C12A	General Release Specification	HC05C12AGRS/D

Application Note

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