NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE *(YYMMDD)* 97-07-29

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR	b. ADDRESS *(Street, City, State, Zip Code)*	5. CAGE CODE	6. NOR NO.
	Defense Supply Center Columbus	67268	5962-R396-97
a. TYPED NAME *(First, Middle Initial, Last)*	3990 East Broad Street Columbus, OH 43216-5000	7. CAGE CODE 67268	8. DOCUMENT NO. **5962-96621**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, RADIATION HARDENED, CMOS, NAND GATES, MONOLITHIC SILICON	a. CURRENT A	b. NEW B	No users listed.

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "B".
Revisions description column; add "Changes in accordance with NOR 5962-R396-97".
Revisions date column; add "97-07-29".
Revision level block; add "B".
Rev status of sheets; for sheets 21 change from "A" to “B”.
Rev status of sheets; for sheets 22 change from "A" to “B”.
Rev status of sheets; for sheets 23 change from "A" to “B”.
Rev status of sheets; for sheets 24 change from "A" to “B”.
Rev status of sheets; for sheets 25 change from "A" to “B”.
Rev status of sheets; for sheets 26 change from "A" to “B”.

Sheet 21: NOR 5962-R184-97 sheet 8 of Appendix A for Die Physical Dimensions for Die Thickness change from “21 +/-1 mils” to “20 +/1 mils”
Revision Level Block: change from “A” to “B”
Sheet 22: NOR 5962-R184-97 sheet 9 of Appendix A for Interface Materials for Glassivation Type change from “Phosphorous doped SIO2” to “PSG “ and for Assembly Related Information for Substrate Potential change from “ Tied to V_{SS}” to “Floating or Tied to V_{DD} “
Revision Level Block: change from “A” to “B”
Sheet 23: NOR 5962-R184-97 sheet 10 of Appendix A for Die Physical Dimensions for Die Thickness change from “21 +/-1 mils” to “20 +/1 mils”
Revision Level Block: change from “A” to “B”
Sheet 24: NOR 5962-R184-97 sheet 11 of Appendix A for Interface Materials for Glassivation Type change from “Phosphorous doped SIO2” to “PSG “ and for Assembly Related Information for Substrate Potential change from “ Tied to V_{SS}” to “Floating or Tied to V_{DD} “
Revision Level Block: change from “A” to “B”
Sheet 25: NOR 5962-R184-97 sheet 12 of Appendix A for Die Physical Dimensions for Die Thickness change from “21 +/-1 mils” to “20 +/1 mils”
Revision Level Block: change from “A” to “B”
Sheet 26: NOR 5962-R184-97 sheet 13 of Appendix A for Interface Materials for Glassivation Type change from “Phosphorous doped SIO2” to “PSG “ and for Assembly Related Information for Substrate Potential change from “ Tied to V_{SS}” to “Floating or Tied to V_{DD} “
Revision Level Block: change from “A” to “B”

12. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME *(First, Middle Initial, Last)*
DSCC-VA	

d. TITLE	e. SIGNATURE	f. DATE SIGNED *(YYMMDD)*
Chief, Custom Microelectronics	RAYMOND MONNIN	97-07-29

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED *(YYMMDD)*
DSCC-VA	RONALD COUCH	97-07-29

NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE *(YYMMDD)* 97-02-24

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR	b. ADDRESS *(Street, City, State, Zip Code)*	5. CAGE CODE	6. NOR NO.
	Defense Supply Center, Columbus 3990 East Broad Street Columbus, OH 43216-5000	67268	5962-R184-97
a. TYPED NAME *(First, Middle Initial, Last)*		7. CAGE CODE 67268	8. DOCUMENT NO. **5962-96621**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, RADIATION HARDENED, CMOS, NAND GATES, MONOLITHIC SILICON	a. CURRENT	b. NEW A	No users listed.

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "A".
Revisions description column; add "Changes in accordance with NOR 5962-R184-97".
Revisions date column; add "97-02-24".
Revision level block; add "A".
Rev status of sheets; for sheets 1, 4, and 15 through 26, add "A".

Sheet 4: Add new paragraph which states; "3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document."
Revision level block; add "A".

Sheets 15 through 26: Add attached appendix A.

CONTINUED ON NEXT SHEET

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME *(First, Middle Initial, Last)*
DSCC-VAC	MONICA L. POELKING

d. TITLE	e. SIGNATURE	f. DATE SIGNED *(YYMMDD)*
CHIEF, CUSTOM MICROELECTRONICS TEAM	MONICA L. POELKING	97-02-24

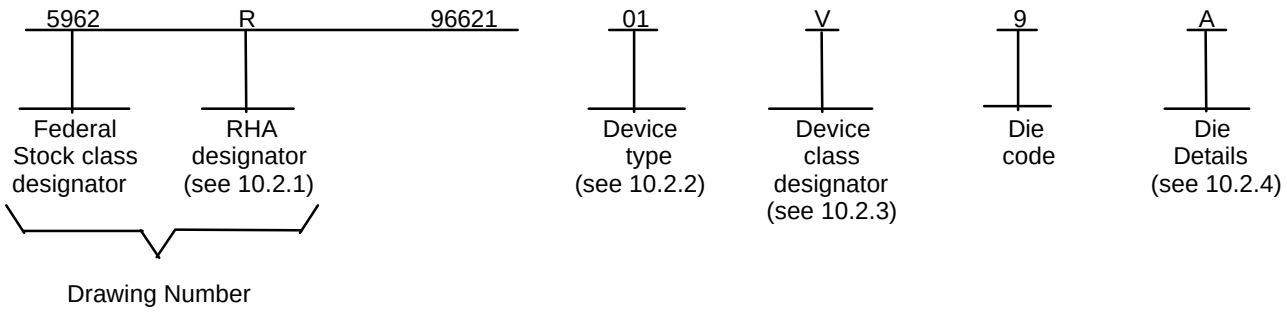
15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED *(YYMMDD)*
DSCC-VAC	CHARLES F. SAFFLE, JR.	97-02-24

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96621

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN shall be as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s) The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4011B	Radiation Hardened, CMOS, quad 2-input NAND gate
02	4012B	Radiation Hardened CMOS, dual 4-input NAND gate
03	4023B	Radiation Hardened CMOS, triple 3-input NAND gate
04	4011BN	Radiation Hardened, CMOS, quad 2-input NAND gate, neutron irradiated die

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APPENDIX A FORMS A PART OF SMD 5962-96621

05	4012BN	Radiation Hardened CMOS, dual 4-input NAND gate, neutron irradiated die
06	4023BN	Radiation Hardened CMOS, triple 3-input NAND gate, neutron irradiated die

10.2.3 Device class designator

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

10.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die Physical dimensions

Die Types	Figure number
01, 04	A-1
02, 05	A-2
03, 06	A-3

10.2.4.2 Die Bonding pad locations and Electrical functions

Die Types	Figure number
01, 04	A-1
02, 05	A-2
03, 06	A-3

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10.2.4.3 Interface Materials

Die Types	Figure number
01, 04	A-1
02, 05	A-2
03, 06	A-3

10.2.4.4 Assembly related information

01, 04	A-1
02, 05	A-2
03, 06	A-3

10.3 Absolute maximum ratings See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96621

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item Requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die Physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figures A-1, A-2 and A-3.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figures A-1, A-2, and A-3.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figures A-1, A-2, and A-3.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figures A-1, A-2, and A-3.

30.2.5 Truth table(s). The truth table(s) shall be as defined within paragraph 3.2.3 of the body of this document.

30.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.4 of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QM" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer Lot acceptance for Class V product using the criteria defined within MIL-STD-883 TM 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 TM2010 or the alternate procedures allowed within MIL-STD-883 TM5004.

40.3 Conformance inspection

40.3.1 Group E inspection Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, 4.4.4.4 and 4.4.4.5.

50. DIE CARRIER

50.1 Die carrier requirements The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96621

60. NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined with MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of Supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

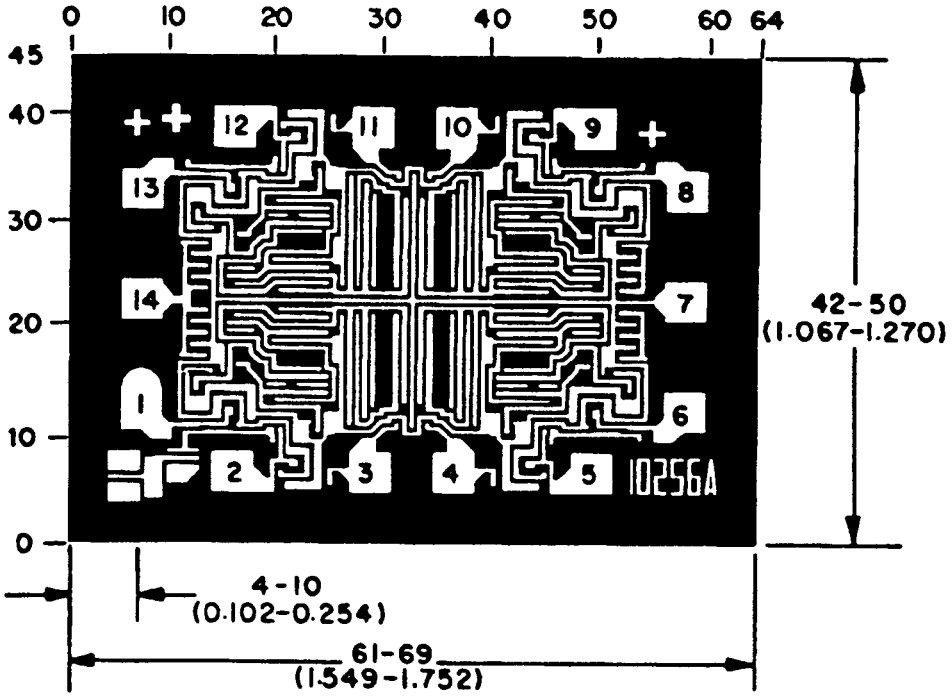
APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96621

FIGURE A-1

o DIE PHYSICAL DIMENSIONS

Die Size: 1143 x 1626 microns.
Die Thickness: 21 +/-1 mils.

o DIE BONDING PAD LOCATIONS AND ELECTRICAL FUNCTIONS



NOTE: Pad numbers reflect terminal numbers when placed in Case Outlines C, X (see Figure 1).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96621

o INTERFACE MATERIALS

Top Metallization:	Al	11.0kA - 14.0kA
Backside Metallization:	None.	
Glassivation		
Type:	Phosphorous Doped SiO2	
Thickness:	10.4kA - 15.6kA	
Substrate:	Single crystal silicon.	

o ASSEMBLY RELATED INFORMATION

Substrate Potential:	Tied to VSS.
Special assembly instructions:	Bond pad #14 (VDD) first.

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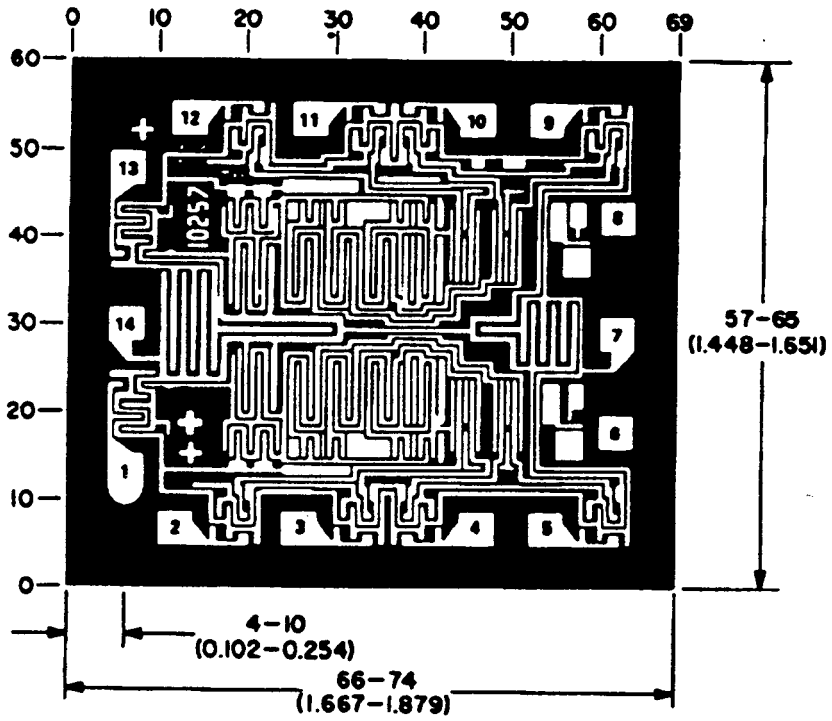
FIGURE A-2

o DIE PHYSICAL DIMENSIONS

Die Size: 1524 x 1753 microns.
Die Thickness: 21 +/-1 mils.

o DIE BONDING PAD LOCATIONS AND ELECTRICAL FUNCTIONS



NOTE: Pad numbers reflect terminal numbers when placed in Case Outlines C, X (see Figure 1).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96621

o INTERFACE MATERIALS

Top Metallization:	Al	11.0kA - 14.0kA
Backside Metallization:	None.	
Glassivation		
Type:	Phosphorous Doped SiO2	
Thickness:	10.4kA - 15.6kA	
Substrate:	Single crystal silicon.	

o ASSEMBLY RELATED INFORMATION

Substrate Potential:	Tied to VSS.
Special assembly instructions:	Bond pad #14 (VDD) first.

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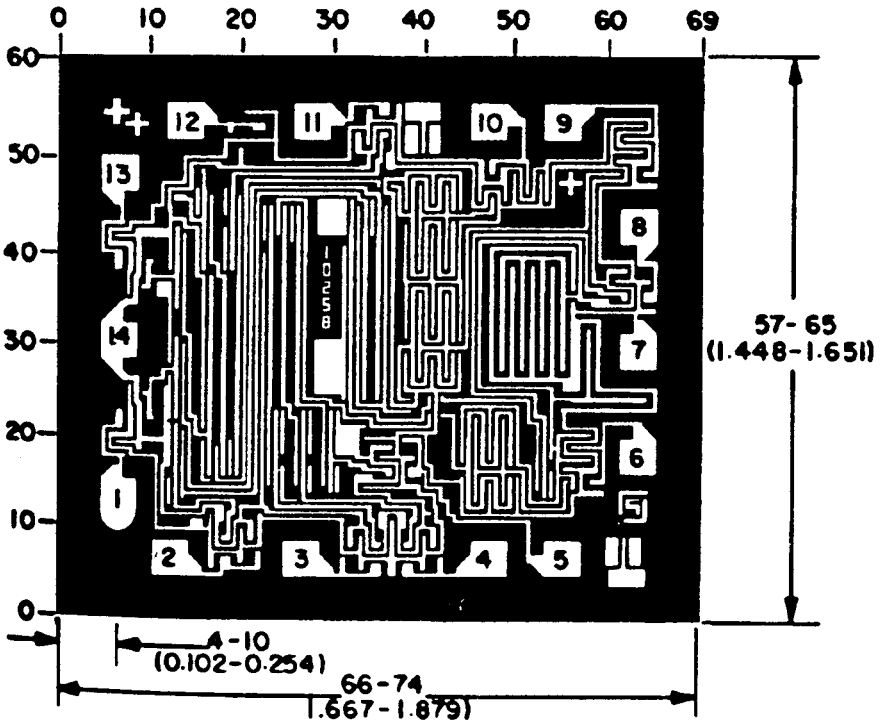
APPENDIX A FORMS A PART OF SMD 5962-96621

FIGURE A-3

o DIE PHYSICAL DIMENSIONS

Die Size: 1524 x 1753 microns.
Die Thickness: 21 +/-1 mils.

o DIE BONDING PAD LOCATIONS AND ELECTRICAL FUNCTIONS



NOTE: Pad numbers reflect terminal numbers when placed in Case Outlines C, X (see Figure 1).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96621

o INTERFACE MATERIALS

Top Metallization:	Al	11.0kA - 14.0kA
Backside Metallization:	None.	
Glassivation		
Type:	Phosphorous Doped SiO2	
Thickness:	10.4kA - 15.6kA	
Substrate:	Single crystal silicon.	

o ASSEMBLY RELATED INFORMATION

Substrate Potential:	Tied to VSS.
Special assembly instructions:	Bond pad #14 (VDD) first.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-02-24

Approved sources of supply for SMD 5962-96621 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962R9662101V9A	34371	CD4011BHSR
5962R9662102V9A	34371	CD4012BHSR
5962R9662103V9A	34371	CD4023BHSR
5962R9662104V9A	34371	CD4011BHNSR
5962R9662105V9A	34371	CD4012BHNSR
5962R9662106V9A	34371	CD4023BHNSR

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32902-0883

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS OF SHEETS															
REV															
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Dan Wonnell

CHECKED BY
Monica Poelking

APPROVED BY
Monica Poelking

DRAWING APPROVAL DATE
95-11-27

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, CMOS, NAND GATES, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96621**

SHEET 1 OF 14

DESC FORM 193
JUL 94

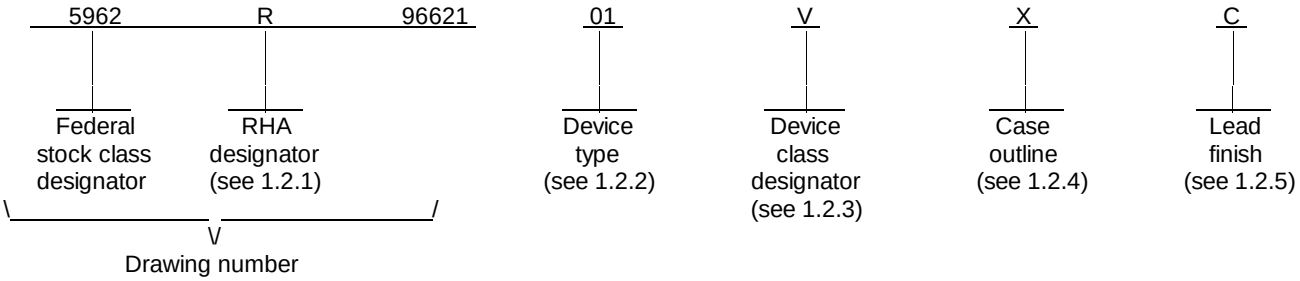
5962-E155-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4011B	Radiation hardened CMOS quad 2-input NAND gate
02	4012B	Radiation hardened CMOS dual 4-input NAND gate
03	4023B	Radiation hardened CMOS triple 3-input NAND gate
04	4011BN	Radiation hardened CMOS quad 2-input NAND gate with neutron irradiated die
05	4012BN	Radiation hardened CMOS dual 4-input NAND gate with neutron irradiated die
06	4023BN	Radiation hardened CMOS triple 3-input NAND gate with neutron irradiated die

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	CDIP2-T14	14	Dual-in-line package
X	CDFP3-F14	14	Flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD})	-0.5 V dc to +20 V dc
Input voltage range	-0.5 V dc to V_{DD} + 0.5 Vdc
DC input current, any one input	±10 mA
Device dissipation per output transistor	100 mW
Storage temperature range (T_{STG})	-65° C to +150° C
Lead temperature (soldering, 10 seconds)	+265° C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case C	24°C/W
Case X	30°C/W
Thermal resistance, junction-to-ambient Θ_{JA}):	
Case C	74°C/W
Case X	116°C/W
Junction temperature (T_J)	+175° C
Maximum power dissipation at T_A = +125°C (P_D): 4/	
Case C	0.68 W
Case X	0.43 W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	3.0 V dc to +18 V dc
Case operating temperature range (T_C)	-55° C to +125° C
Input voltage (V_{IN})	0 V to V_{DD}
Output voltage (V_{OUT})	0 V to V_{DD}
Radiation features:	
Total dose	1 x 10^5 Rads (Si)
Single event phenomenon (SEP) effective linear energy threshold, no upsets or latchup (see 4.4.4.5)	>75 MEV/(cm^2/mg) 5/
Dose rate upset (20 ns pulse)	> 5 x 10^8 Rads(Si)/s 5/
Dose rate latch-up	> 2 x 10^8 Rads(Si)/s 5/
Dose rate survivability	> 5 x 10^{11} Rads(Si)/s 5/
Neutron irradiated (device types 04, 05, and 06)	> 1 x 10^{14} neutrons/cm^2

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55° C to +125° C unless otherwise noted.
4/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the following rate:

Case C	13.5 mW/°C
Case X	8.6 mW/°C

5/ Guaranteed by design or process but not tested.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables The truth tables shall be as specified on figure 2.

3.2.4 Radiation test connections. The radiation test connections shall be as specified in table III herein.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 36 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's quality management (QM) plan. The modification in the QM plan shall not affect form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance in spection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 or as modified in the device manufacturer's quality management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity (ESDS) qualification inspection. ESDS testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 or as specified in the QM plan including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Units
					Min	Max	
Supply current	I_{DD}	V_{DD} = 20 V, V_{IN} = V_{DD} or GND	All	1		0.5	µA
				2		50	
		M, D, L, R 2/		1		2.5	
		V_{DD} = 18 V, V_{IN} = V_{DD} or GND		3		0.5	
		V_{DD} = 5 V, V_{IN} = V_{DD} or GND 1/		1, 3		0.25	
				2		7.5	
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND 1/		1, 3		0.5	
				2		15	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND 1/		1, 3		0.5	
				2		30	
Input leakage current LOW	I_{IL}	V_{DD} = 20 V, V_{IN} = V_{DD} or GND	All	1	-100		nA
				2	-1000		
		V_{DD} = 18 V, V_{IN} = V_{DD} or GND		3	-100		
Input leakage current HIGH	I_{IH}	V_{DD} = 20 V, V_{IN} = V_{DD} or GND	All	1		100	nA
				2		1000	
		V_{DD} = 18 V, V_{IN} = V_{DD} or GND		3		100	
Output voltage, LOW	V_{OL}	V_{DD} = 15 V, no load	All	1, 2, 3		50	mV
		V_{DD} = 5 V, no load 1/				50	
		V_{DD} = 10 V, no load 1/				50	
Output voltage, HIGH	V_{OH}	V_{DD} = 15 V, no load 3/	All	1, 2, 3	14.95		V
		V_{DD} = 5 V, no load 1/			4.95		
		V_{DD} = 10 V, no load 1/			9.95		
Low level output current (sink)	I_{OL}	V_{DD} = 5 V V_O = 0.4 V	All	1	0.53		mA
				2 1/	0.36		
				3 1/	0.64		
		V_{DD} = 10 V V_O = 0.5 V	All	1	1.4		
				2 1/	0.9		
				3 1/	1.6		
		V_{DD} = 15 V V_O = 1.5 V	All	1	3.5		
				2 1/	2.4		
				3 1/	4.2		

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level output current (source)	I_{OH}	V_{DD} = 5 V V_{OUT} = 4.6 V	All	1		-0.53	mA
				2 1/		-0.36	
				3 1/		-0.64	
		V_{DD} = 5 V V_{OUT} = 2.5 V	All	1		-1.8	
				2 1/		-1.15	
				3 1/		-2.0	
		V_{DD} = 10 V V_{OUT} = 9.5 V	All	1		-1.4	
				2 1/		-0.9	
				3 1/		-1.6	
		V_{DD} = 15 V V_{OUT} = 13.5 V	All	1		-3.5	
				2 1/		-2.4	
				3 1/		-4.2	
Input voltage	V_{IL}	V_{DD} = 5 V V_{OH} > 4.5 V, V_{OL} < 0.5 V	All	1, 2, 3		1.5	V
		V_{DD} = 10 V V_{OH} > 9.0 V, V_{OL} < 1.0 V 1/		1, 2, 3		3	
		V_{DD} = 15 V V_{OH} > 13.5 V, V_{OL} < 1.5 V		1, 2, 3		4	
	V_{IH}	V_{DD} = 5 V V_{OH} > 4.5 V, V_{OL} < 0.5 V	All	1, 2, 3	3.5		
		V_{DD} = 10 V V_{OH} > 9.0 V, V_{OL} < 1.0 V 1/		1, 2, 3	7		
		V_{DD} = 15 V V_{OH} > 13.5 V, V_{OL} < 1.5 V		1, 2, 3	11		
N threshold voltage	V_{NTH}	V_{DD} = 10 V, I_{SS} = -10 µA	All	1	-0.7	-2.8	V
		M, D, L, R 2/			-0.2	-2.8	
N threshold voltage, delta	ΔV_{NTH}	V_{DD} = 10 V, I_{SS} = -10 µA, M, D, L, R 2/	All	1		±1.0	
P threshold voltage	V_{PTH}	V_{SS} = 0.0 V, I_{DD} = 10 µA	All	1	0.7	2.8	
		M, D, L, R 2/		1	0.2	2.8	
P threshold voltage, delta	ΔV_{PTH}	V_{SS} = 0.0 V, I_{DD} = 10 µA M, D, L, R 2/	All	1		±1.0	

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Functional tests		V_{DD} = 2.8 V, V_{IN} = V_{DD} or GND	All	7	$V_{OH} > V_{DD}/2$	$V_{OL} < V_{DD}/2$	V
		V_{DD} = 20 V, V_{IN} = V_{DD} or GND		7			
		V_{DD} = 18 V, V_{IN} = V_{DD} or GND	All	8A			
		M, D, L, R 2/	All	7			
		V_{DD} = 3.0 V, V_{IN} = V_{DD} or GND	All	8B			
		M, D, L, R 2/	All	7			
Input capacitance	C_{IN}	Any input, See 4.4.1c 1/	All	4		7.5	pF
Propagation delay time, any input to output	t_{PHL}, t_{PLH}	V_{DD} = 5 V, V_{IN} = V_{DD} or GND 4/	All	9		250	ns
				10, 11		338	
		M, D, L, R 2/		9		338	
		V_{DD} = 10 V 1/, 4/		9		120	
		V_{DD} = 15 V 1/, 4/		9		90	
Transition time	t_{THL}, t_{TLH}	V_{DD} = 5 V, V_{IN} = V_{DD} or GND 4/	All	9		200	ns
				10, 11		270	
		V_{DD} = 10 V 1/, 4/		9		100	
		V_{DD} = 15 V 1/, 4/		9		80	

1/ These tests are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which affect these characteristics.

2/ Devices supplied to this drawing will meet all levels M, D, L, R of irradiation. However, this device is only tested at the 'R' level. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ For accuracy, voltage is measured differentially to V_{DD}. Limit is 0.050 V Max.

4/ C_L = 50 pF, R_L = 200 kΩ, Input t_R, t_F < 20 ns.

Device type	01, 04	02, 05	03, 06
Case outlines	C and X		
Terminal number	Terminal symbol		
1	A	J = $\overline{A}\overline{B}\overline{C}\overline{D}$	A
2	B	A	B
3	J = $\overline{A}\overline{B}$	B	D
4	K = $\overline{C}\overline{D}$	C	E
5	C	D	F
6	D	NC	K = $\overline{D}\overline{E}\overline{F}$
7	V_{SS}	V_{SS}	V_{SS}
8	F	NC	C
9	E	E	J = $\overline{A}\overline{B}\overline{C}$
10	L = $\overline{E}\overline{F}$	F	L = $\overline{G}\overline{H}\overline{I}$
11	M = $\overline{G}\overline{H}$	G	I
12	G	H	H
13	H	K = $\overline{E}\overline{F}\overline{G}\overline{H}$	G
14	V_{DD}	V_{DD}	V_{DD}

NOTE: NC = no connection

FIGURE 1. Terminal connections.

Device types 01 and 04

Inputs		Outputs
A, C, E, and G	B, D, F, and H	J, K, L, and M
H	H	L
X	L	H
L	X	H

NOTE: X = Don't care

Device type 02 and 05

Inputs				Outputs
A, E	B, F	C, G	D, H	J, K
H	H	H	H	L
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H

NOTE: X = Don't care

Device types 03 and 06

Inputs			Outputs
A, D, G	B, E, H	C, F, I	J, K, L
H	H	H	L
X	X	L	H
X	L	X	H
L	X	X	H

NOTE: X = Don't care

FIGURE 2. Truth tables

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. Tests shall be sufficient to validate the limits defined in table I herein.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-I-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron irradiation. Neutron irradiation for devices 04, 05 and 06 shall be conducted in wafer form using a neutron fluence of approximately 1×10^{14} neutrons/cm^2.

4.4.4.3 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.4 herein).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 2/ 3/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11 3/
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7 and 9 and deltas.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see Table I)

Table IIB. Burn-in and operating life test Delta parameters (+25°C)

Parameter	Symbol	Delta Limits
Supply current	I_{DD}	±0.1 µA
Output current (sink) V_{DD} = 5.0 V	I_{OL}	±20%
Output current (source) V_{DD} = 5.0 V, V_{OUT} = 4.6 V	I_{OH}	±20%

4.4.4.5 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25° C and the maximum rated operating temperature ±10° C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

Table III Irradiation test connections device types 01 and 04.

Open	Ground	V_{DD} = 10 V ±0.5 V
3,4,10,11	7	1,2,5,6,8,9,12,13,14

Table III Irradiation test connections device types 02 and 05.

Open	Ground	V_{DD} = 10 V ±0.5 V
1,6,8,13	7	2,3,4,5,9,10,11,12,14

Table III Irradiation test connections device types 03 and 06.

Open	Ground	V_{DD} = 10 V ±0.5 V
6,9,10	7	1,2,3,4,5,8,11,12,13,14

1/ Each pin except V_{DD} and GND will have a series resistor of 47KΩ ±5%, for irradiation testing.

4.5 Methods of inspection. Methods of inspection shall be as specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-11-27

Approved sources of supply for SMD 5962-96621 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 and QML-38535 during the next revision. MIL-BUL-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103 and QML-38535.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962R9662101VCC	34371	CD4011BDMSR
5962R9662101VXC	34371	CD4011BKMSR
5962R9662102VCC	34371	CD4012BDMSR
5962R9662102VXC	34371	CD4012BKMSR
5962R9662103VCC	34371	CD4023BDMSR
5962R9662103VXC	34371	CD4023BKMSR
5962R9662104VCC	34371	CD4011BDNSR
5962R9662104VXC	34371	CD4011BKNSR
5962R9662105VCC	34371	CD4012BDNSR
5962R9662105VXC	34371	CD4012BKNSR
5962R9662106VCC	34371	CD4023BDNSR
5962R9662106VXC	34371	CD4023BKNSR

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32902-0883