
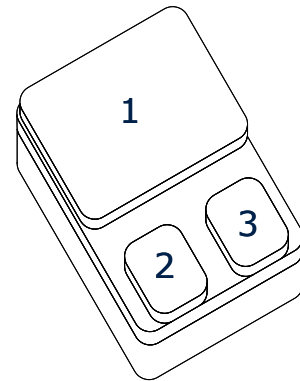


HiRel RadHard Power-MOS

- Low $R_{DS(on)}$
- Single Event Effect (SEE) hardened
LET 55, Range: 90 μ m
 $V_{GS} = -15V$, $V_{DS} = 250V$, approved
 $V_{GS} = -20V$, $V_{DS} = 160V$, approved
- Total Ionisation Dose (TID) hardened
100 kRad approved (Level R)
- Hermetically sealed
- N-channel
-  **ESA Space Qualified**
ESCC Detail Spec. No.: 5205/027



Type	Marking	Pin Configuration				Package
		1	2	3	-	
BUY25CS54A-01	-	D	G	S	-	SMD2

Maximum Ratings

Parameter	Symbol	Values	Unit
Drain Source Voltage	V_{DS}	250	V
Gate Source Voltage	V_{GS}	+/- 20	V
Drain Gate Voltage	V_{DG}	250	V
Continuous Drain Current $T_C = 25^\circ C$ $T_C = 100^\circ C$	I_D	54 34	A
Continuous Source Current	I_S	54	A
Drain Current Pulsed, t_p limited by T_{jmax}	I_{DM}	214	Apk
Total Power Dissipation ¹⁾	P_{tot}	250	W
Operating and Storage Temperature	T_{op}	-55 to + 150	$^\circ C$
Avalanche Energy	E_{AS}	380	mJ

Thermal Characteristics

Thermal Resistance (Junction to Case)	$R_{th JC}$	0.5	K/W
Soldering Temperature	T_{sol}	250	$^\circ C$

Notes.:

1) For $T_S \leq 25^\circ C$. For $T_S > 25^\circ C$ derating is required.

Electrical Characteristics, at $T_A=25^\circ\text{C}$; unless otherwise specified

Parameter	Symbol	Values		Unit
		min.	max.	
DC Characteristics				
Breakdown Voltage Drain to Source $I_D = 0.25\text{mA}$, $V_{GS} = 0\text{V}$	B_{VDSS}	250	-	V
Gate Threshold Voltage $I_D = 1.0\text{mA}$, $V_{DS} \geq V_{GS}$	$V_{GS(th)}$	2.0	4.0	V
Gate to Source Leakage Current $V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$	I_{GSS}	-	+/-100	nA
Drain Current $V_{DS} = 200\text{V}$, $V_{GS} = 0\text{V}$	I_{DSS}	-	25	μA
Drain Source On Resistance ¹⁾ $V_{GS} = 10\text{V}$, $I_D = 34\text{A}$	$r_{DS(ON)}$	-	0.03	Ω
Source Drain Diode, Forward Voltage ^{1), 2)} $V_{GS} = 0\text{V}$, $I_S = 54\text{A}$	V_{SD}	-	1.2	V

AC Characteristics

Turn-on Delay Time $V_{DD} = 50\% V_{DS}$, $I_D = 34\text{A}$, $R_G = 4.7\Omega$	$t_{d(ON)}$	-	80	ns
Rise Time $V_{DD} = 50\% V_{DS}$, $I_D = 34\text{A}$, $R_G = 4.7\Omega$	t_r	-	80	ns
Turn-off Delay Time $V_{DD} = 50\% V_{DS}$, $I_D = 34\text{A}$, $R_G = 4.7\Omega$	$t_{d(OFF)}$	-	130	ns
Fall Time $V_{DD} = 50\% V_{DS}$, $I_D = 34\text{A}$, $R_G = 4.7\Omega$	t_f	-	80	ns
Reverse Recovery Time $V_{DD} < 50\% V_{DS}$, $I_D = 54\text{A}$	t_{rr}	-	700	ns
Common Source Input Capacitance $V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$	C_{iss}	9.0	14.0	nF
Common Source Output Capacitance $V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$	C_{oss}	600	1000	pF
Common Source Reverse Transfer Capacitance $V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$	C_{rss}	5	30	pF
Total Gate Charge $V_{DD} = 50\% V_{DS}$, $V_{GS} = 10\text{V}$, $I_D = 54\text{A}$	Q_G	-	180	nC

Notes.:

- 1) Pulsed Measurement: Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2.0\%$.
2) Measured within 2.0 mm of case.

Electrical Characteristics

 at $T_A = 125^\circ\text{C}$; unless otherwise specified

Parameter	Symbol	Values		Unit
		min.	max.	
DC Characteristics				
Gate Threshold Voltage $I_D = 1.0\text{mA}$, $V_{DS} \geq V_{GS}$	$V_{GS(th)}$	1.5	-	V
Gate to Source Leakage Current $V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$	I_{GSS}	-	+/-200	nA
Drain Current $V_{DS} = 200\text{V}$, $V_{GS} = 0\text{V}$	I_{DSS}	-	250	μA
Drain Source On Resistance ¹⁾ $V_{GS} = 10\text{V}$, $I_D = 34\text{A}$	$r_{DS(ON)}$	-	0.07	Ω

Notes.:

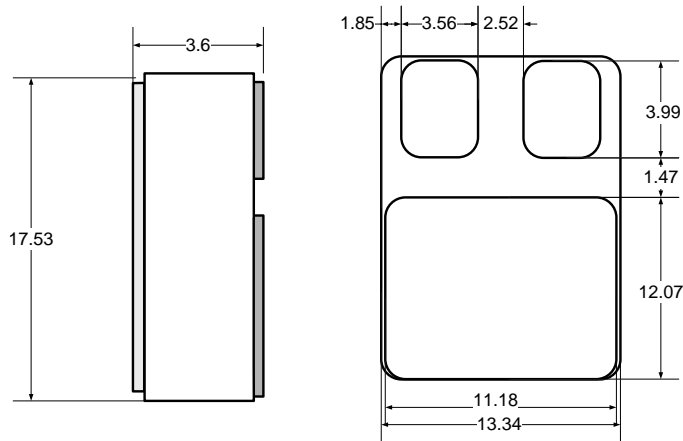
 1) Pulsed Measurement: Pulse Width < 300 μs , Duty Cycle < 2.0%.

Electrical Characteristics

 at $T_A = -55^\circ\text{C}$; unless otherwise specified

Parameter	Symbol	Values		Unit
		min.	max.	
DC Characteristics				
Gate Threshold Voltage $I_D = 1.0\text{mA}$, $V_{DS} \geq V_{GS}$	$V_{GS(th)}$	-	5.0	V

SMD2 Package



Dimensions are typical [mm]

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