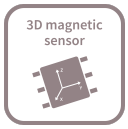
Usermanual TLI493D-W2BW

Low Power 3D Hall Sensor with I²C Interface and Wake Up Function

TLI493D-W2BW

About this document



Scope and purpose

This document provides product information and descriptions regarding:

- I²C Registers
- I²C Interface
- Wake Up mode
- Diagnostic

Intended audience

This document is aimed at engineers and developers of hard and software using the sensor TLI493D-W2BW.

Table of contents

1 I²C Register

The TLI493D-W2BW includes several registers that can be accessed via Inter-Integrated Circuit interface (I²C) to read data as well as to write and configure settings.

1.1 Register overview

A bitmap overview is presented in ***Figure 1***. Basically the following sections are available:

- measurement data (green bits in registers 00_H till 05_H)
- sensor status and diagnostics (grey bits in registers 05_H, 06_H, 10_H and 11_H)
- configuration parameters such as the power mode (orange bits in registers 10_H, 11_H, 13_H and 14_H)
- Wake Up values in registers (blue bits in registers 07_H till $0F_H$)

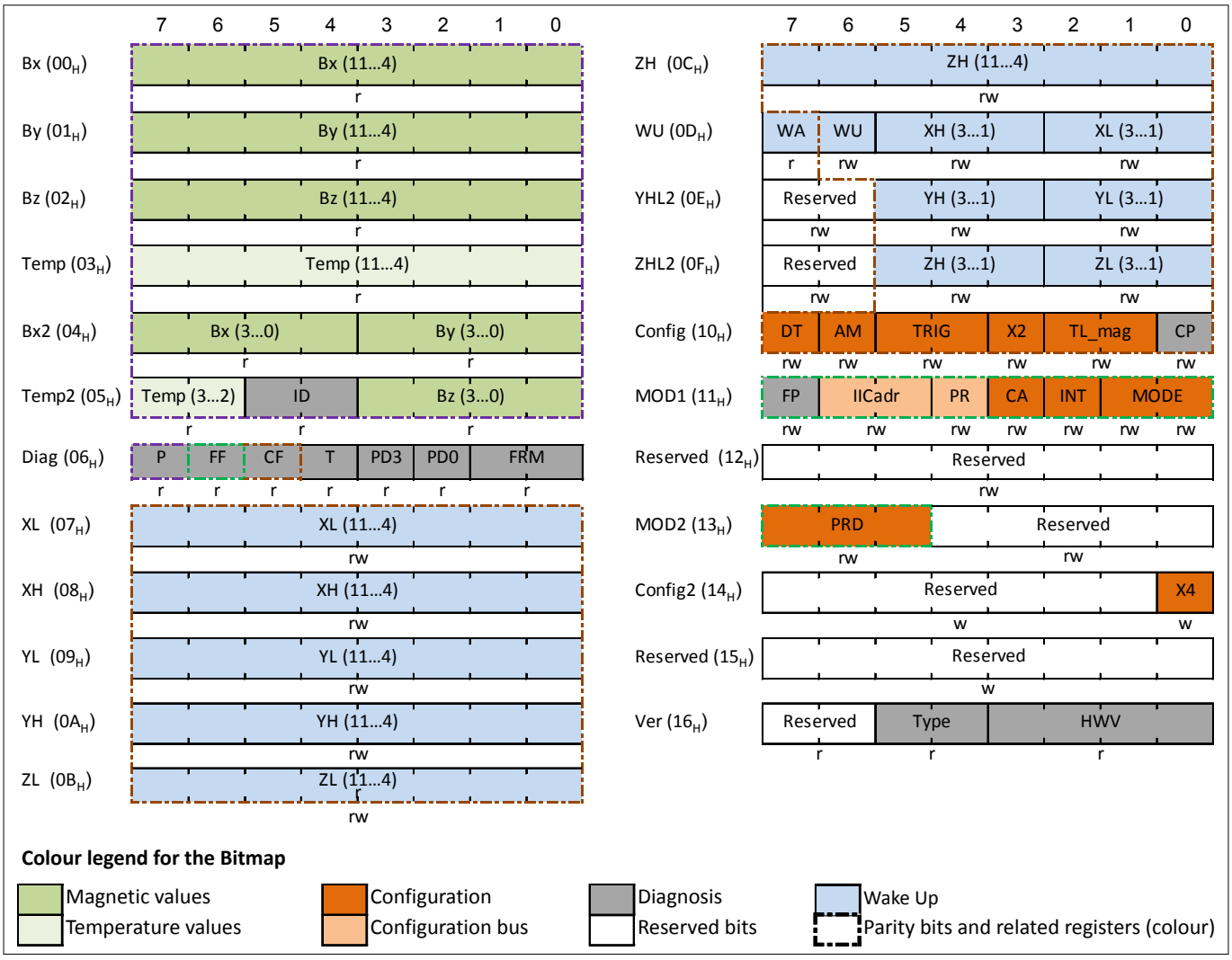


Figure 1 TLI493D-W2BW Bitmap

The diagnostic register 06_H contains parity information as a diagnostic mechanism. The bitmap illustrates this and marks the relationship of the sections to this flags with different colored lines/frames around the bit contents.

Table 1 Register overview

Register name	Register long name	Address
Bx, By and Bz	*Magnetic values MSBs*	00_H, 01_H, 02_H
Temp	*Temperature value MSBs*	03_H
Bx2	*Magnetic values LSBs*	04_H
Temp2	*Temperature and magnetic LSBs and device address*	05_H
Diag	*Sensor diagnostic and status register*	06_H
XL, YL and ZL	*Wake Up lower threshold MSBs*	07_H, 09_H, $0B_H$
XH, YH and ZH	*Wake Up upper threshold MSBs*	08_H, $0A_H$, $0C_H$
WU	*Wake Up enable and X thresholds LSBs*	$0D_H$
YHL2	*Wake Up Y thresholds LSBs*	$0E_H$
ZHL2	*Wake Up Z thresholds LSBs*	$0F_H$
Config	*Configuration register*	10_H
MOD1	*Power mode, interrupt, address, parity*	11_H
Reserved	*Reserved register*	12_H
MOD2	*Low Power Mode update rate*	13_H
Config2	*Configuration register 2*	14_H
Reserved	*Reserved register*	15_H
Ver	*Version register*	16_H

1.2 Register description

The I²C registers can be read or written at any time. It is recommended to read measurement data in a synchronized fashion, i.e. after an interrupt pulse (/INT). This avoids reading inconsistent sensor or diagnostic data, especially in fast mode. Additionally, several flags can be checked to ensure the register values are consistent and the ADC was not running at the time of readout.

1.2.1 Bit types

The TLI493D-W2BW contains read bits, write bits and reserved bits.

Table 2 Bit Types

Abbreviation	Function	Description
r	Read	Read only bit
w	Write	Write only bit
rw	Read/write	Readable and writable bit
	Reserved	Bits that must keep the default values • For write bits: write back the reset value stated in the register description • For read/write bits: if available write back the reset value stated in the register description. Otherwise a read prior to write is required (these bits are device specific)

1.2.2 Measurement data and registers combined in the I²C parity bit "P"

The I²C communication of the registers in this chapter is protected with the parity bit "P", described in the Diag register with the address 06_H. See also ***Figure 1*** - parity bits and related registers.

To make sure all data is consistent, the registers from 00_H to 06_H should be read with the same I²C command. Otherwise, the sampled data (X, Y, Z, Temperature) may correspond to different conversion cycles.

Magnetic values MSBs

Register names	Address	Reset Value
Bx, By and Bz	00_H, 01_H, 02_H	80_H

7							0
Bx, By and Bz (11...4)							

Field	Bits	Type	Description
Bx, By and Bz	7:0	r	**Bx, By and Bz values** Signed value as two's complement from the HALL probes in the x, y and z-direction of the magnetic field. Contains the eight Most Significant Bits. If Bz is deactivated the Bz value is the reset value.

Back to ***TLI493D-W2BW Bitmap***.

Temperature value MSBs

Register name	Address	Reset Value
Temp	03_H	80_H

7							0
Temp (11...4)							

Field	Bits	Type	Description
Temp	7:0	r	**Temperature value** Signed value as two's complement. If the temperature measurement is deactivated, the Temp value is the reset value.

Back to ***TLI493D-W2BW Bitmap***.

Magnetic values LSBs

Register name	Address	Reset Value
Bx2	04_H	00_H

7				4	3			0
Bx (3...0)					**By** (3...0)			

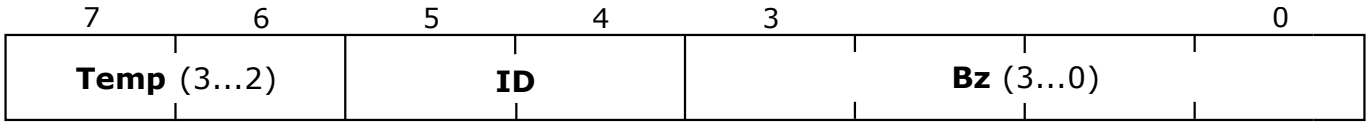
Field	Bits	Type	Description
Bx	7:4	r	**Bx value** Signed value as two's complement from the HALL probes in the x-direction of the magnetic field. Contains the four Least Significant Bits.

Field	Bits	Type	Description
By	3:0	r	**By value** Signed value as two's complement from the HALL probes in the y-direction of the magnetic field. Contains the four Least Significant Bits.

Back to ***TLI493D-W2BW Bitmap***.

Temperature and magnetic LSBs and device address

Register name	Address	Reset Value
Temp2	05_H	(Product Type A0) 00_H (Product Type A1) 10_H (Product Type A2) 20_H (Product Type A3) 30_H



Field	Bits	Type	Description
Temp	7:6	r	**Temperature value** Signed value as two's complement. If the temperature measurement is deactivated, the Temp value is the reset value.
ID	5:4	r	**ID** Readback of the sensor ID, from ***IICadr*** . µC shall verify the address sent by the sensor. See ***Table 4*** .
Bz	3:0	r	**Bz value** Signed value as two's complement from the HALL probes in the z-direction of the magnetic field. Contains the four Least Significant Bits. If Bz is deactivated the Bz value is 0_H.

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1.2.3 Wake Up and registers combined in the I²C parity flag "CF"

The I²C communication of the registers in this chapter is protected by the parity bit ***CF***, which is described in the Diag register with the address 06_H. See also ***Figure 1*** - parity bits and related registers.

Wake Up lower threshold MSBs

Register names	Address	Reset Value
XL, YL and ZL	07_H 09_H $0B_H$	80_H

1 I²C Register

Field	Bits	Type	Description
XL, YL and ZL	7:0	rw	**Wake Up lower threshold** Defines the lower threshold MSBs of the magnetic field in the x, y and z-direction at or below which the sensor enables the /INT, if ***INT*** bit = 0_B. See ***Equation 2***.

Back to ***TLI493D-W2BW Bitmap***.

Wake Up upper threshold MSBs

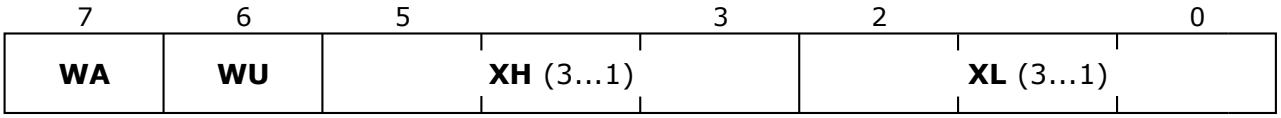
Register names	Address	Reset Value
XH, YH and ZH	08_H $0A_H$ $0C_H$	$7F_H$

Field	Bits	Type	Description
XH, YH and ZH	7:0	rw	**Wake Up upper threshold** Defines the upper threshold MSBs of the magnetic field in the x, y and z direction at or above which the sensor enables the /INT, if ***INT*** bit = 0_B. See ***Equation 2***.

Back to ***TLI493D-W2BW Bitmap***.

Wake Up enable and X thresholds LSBs

Register name	Address	Reset Value
WU	$0D_H$	38_H



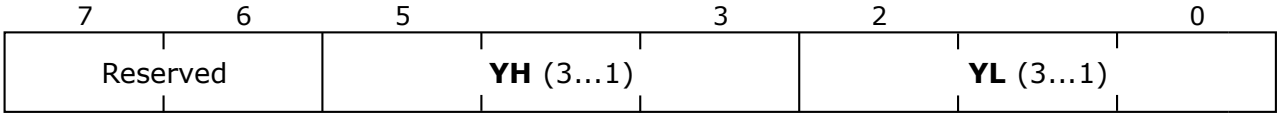
Field	Bits	Type	Description
WA	7	r	**Wake Up mode active** Flag that reports whether the Wake Up mode is disabled or enabled. If 0_B the Wake Up mode is disabled. If 1_B the Wake Up mode is enabled. This bit can be checked if the Wake Up function is disabled or enabled. As long as the ***WA*** bit = 0_B, the /INT will be asserted according ***Table 5***.

Field	Bits	Type	Description
WU	6	rw	**Enables Wake Up mode** If 0_B the Wake Up mode will be disabled. If 1_B the Wake Up mode will be enabled. The following conditions must be fulfilled: • The device is configured to full or short range sensitivity • ***CP*** parity bit (register 10_H) must be odd • Configuration parity must be flagged (***CF*** bit = 1_B) Interrupts /INT will be sent when the measurement data is ≥ upper or ≤ lower Wake Up threshold.
XH	5:3	rw	**Wake Up X upper threshold** Defines the upper threshold LSBs of the magnetic field in the x-direction at or above the sensor enables the /INT, if ***INT*** bit = 0_B. See ***Equation 2***.
XL	2:0	rw	**Wake Up X lower threshold** Defines the lower threshold LSBs of the magnetic field density in the x-direction at or below the sensor enables the /INT, if ***INT*** bit = 0_B. See ***Equation 2***.

Back to ***TLI493D-W2BW Bitmap***.

Wake Up Y thresholds LSBs

Register name	Address	Reset Value
YHL2	$0E_H$	38_H



Field	Bits	Type	Description
Reserved	7:6	rw	**Factory settings** Do not modify, only write reset value.
YH	5:3	rw	**Wake Up Y upper threshold** Defines the upper threshold LSBs of the magnetic field in the y-direction at or above which the sensor enables the /INT, if ***INT*** bit = 0_B. See ***Equation 2***.
YL	2:0	rw	**Wake Up Y lower threshold** Defines the lower threshold LSBs of the magnetic field density in the y-direction at or below which the sensor enables the /INT, if ***INT*** bit = 0B. See ***Equation 2***.

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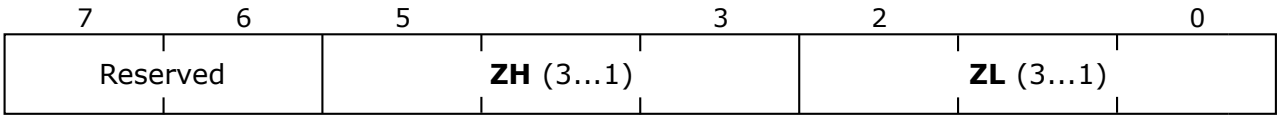
Wake Up Z thresholds LSBs

Register name	Address	Reset Value
ZHL2	$0F_H$	38_H

1 I²C Register



Field	Bits	Type	Description
Reserved	7:6	rw	**Reserved** Do not modify, only write reset value.
ZH	5:3	rw	**Wake Up Z upper threshold** Defines the upper threshold LSBs of the magnetic field in the z-direction at or above which the sensor enables the /INT, if ***INT*** bit = 0_B. See ***Equation 2***.
ZL	2:0	rw	**Wake Up Z lower threshold** Defines the lower threshold LSBs of the magnetic field density in the z-direction at or below which the sensor enables the /INT, if ***INT*** bit = 0_B. See ***Equation 2***.

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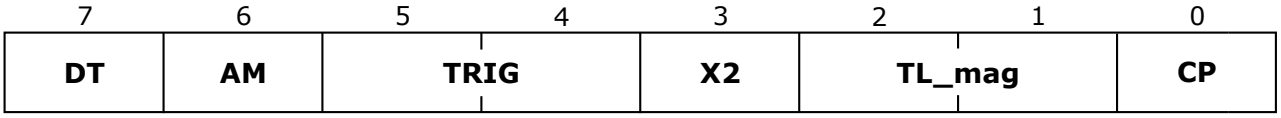
Configuration register

Register names	Address	Reset Value
Config	10_H	01_H



Field	Bits	Type	Description
DT	7	rw	**Disable Temperature** If 0_B temperature measurement is enabled. If 1_B temperature measurement is disabled. This means the Bx, By and Bz channels are measured. The Temp channel is disabled and contains the reset value until a new conversion with Temp is done.
AM	6	rw	**X/Y Angular Measurement** If 0_B the Bz measurement is enabled. If 1_B and DT bit = 1_B: the Bz measurement is disabled. This means the Bx and By channel is measured. The channels Bz and Temp contain the reset values until a new conversion with Bz and Temp is done If 1_B and DT bit = 0_B: must not be used.
TRIG	5:4	rw	**Trigger options** If PR bit = 1_B (1-byte read protocol), the TRIG bits define the trigger mode of the device: If 00_B no ADC trigger on read If 01_B ADC trigger on read before first MSB. If $1x_B$ ADC trigger on read after register 05_H. If PR bit = 0_B these bits have no effect.

Field	Bits	Type	Description
X2	3	rw	**Short range sensitivity** When this bit is set, the sensitivity of the Bx, By, and Bz ADC-conversion is doubled by a longer ADC integration time. The Temp result will not change, neither in sensitivity nor conversion time. The X2 bit interacts with the X4 bit of register 14_H. See ***Table 3***.
TL_mag	2:1	rw	**Magnetic temperature compensation** There are two bits for setting the sensitivity over temperature of the sensor to compensate a magnet temperature coefficient. If $00_B \rightarrow TC_0$ (no compensation) If $01_B \rightarrow TC_1$ If $10_B \rightarrow TC_2$ If $11_B \rightarrow TC_3$
CP	0	rw	**Wake Up and configuration parity** The registers 07_H through 10_H (including 10_H) without the WA and the reserved bits are odd parity protected with this bit. On startup or reset, this parity is false and the ***CF*** bit in the status register 06_H is cleared. Thus the ***CP*** bit has to be corrected once after startup or a reset. If this parity bit is incorrect during a write cycle, the Wake Up is disabled.

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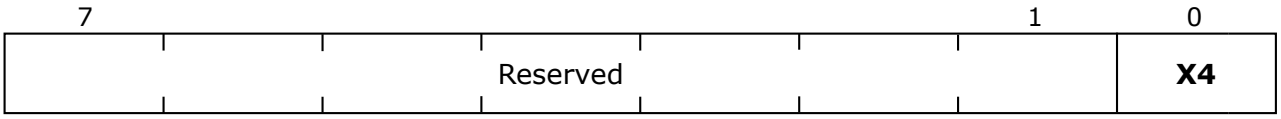
1.2.4 Advanced configuration register

The device provides an additional configuration register to enable the extra short range for an increased sensitivity.

Configuration register 2

Register name	Address	Reset Value
Config2	14_H	00_H



Field	Bits	Type	Description
Reserved	7:1	w	**Factory settings** Do not modify, only write reset value.
X4	0	w	**Extra short range sensitivity** The X4 bit can only be set to 1_B if the X2 bit has been set to 1_B before. Otherwise the write command will have no effect. The X4 bit can be cleared independently of the X2 bit. When this bit is set, the sensitivity of Bx, By and Bz is four times higher compared and to the full range sensitivity by a longer ADC integration time. The Temp result will not change, neither in sensitivity nor conversion time. See ***Table 3***

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Table 3 Range configuration with the X2 and X4 bit

X2 bit	X4 bit	Bx (11...0)	By (11...0)	Bz (11...0)	T (11...2)
0_B	0_B	Bx full range	By full range	Bz full range	T full range
0_B	1_B	Bx full range	By full range	Bz full range	T full range
1_B	0_B	Bx short range	By short range	Bz short range	T full range
1_B	1_B	Bx extra short-range	By extra short range	Bz extra short range	T full range

1.2.5 Mode registers combined in the I²C parity flag "FF"

The I²C communication of the registers in this chapter is protected with the parity bit "FF", described in the Diag register with the address 06_H. See also ***Figure 1*** - parity bits and related registers.

Power mode, interrupt, address, parity

Register name	Address	Reset Value
MOD1	11_H	(Product Type A0) 80_H (Product Type A1) 20_H (Product Type A2) 40_H (Product Type A3) $E0_H$

7	6	5	4	3	2	1	0
FP	**IICadr**		**PR**	**CA**	**INT**	**MODE**	

Field	Bits	Type	Description
FP	7	rw	**Fuse parity** The registers 11H and 13H (bits 7:5) are odd parity protected with this bit. If this parity bit is incorrect please see ***FF*** bit. To exit this state a sensor reset is necessary.
IICadr	6:5	rw	**I²C address** Bits can be set to 00_B, 01_B, 10_B or 11_B to define the slave address in bus configuration. See ***Table 4*** and data sheet.
PR	4	rw	**I²C 1-byte or 2-byte read protocol** If 0_B this is the 2-byte read protocol: <start> <I²Cadr.> <reg.adr.> <data of reg.adr.> <data of reg.adr.+1> …. <stop> If 1_B this is the 1-byte read protocol: <start> <I²Cadr.> <data of reg.00_H> <data of reg.01_H> …. <stop> See ***I²C read commands***
CA	3	rw	**Collision avoidance and clock stretching** The CA bit interacts with the ***INT*** bit, see ***Table 5*** and ***Collision avoidance and clock stretching***.

1 I²C Register

Field	Bits	Type	Description
INT	2	rw	**Interrupt** If 1_B /INT disabled If 0_B /INT enabled: After a completed measurement and ADC-conversion, an /INT pulse will be generated. Enabled ***Wake Up mode*** or ***Collision avoidance*** may suppress the /INT pulse. The INT bit interacts with the ***CA*** bit, see ***Table 5*** .
MODE	1:0	rw	**Power mode** If 00_B Low Power Mode: Cyclic measurements and ADC-conversions with a update rate, defined in the ***PRD*** registers. “No ADC trigger” must be used, see ***Table 6*** and ***TRIG***. If 01_B Master Controlled Mode (Power Down mode): Measurement triggering depends on the ***PR*** bit and is possible with I²C sub address byte (see ***Table 6***) or bits. If 10_B is reserved and must not be used. If 11_B Fast Mode: The measurements and ADC-conversions are running continuously. It is recommended to set INT = 0_B and use a I²C clock up to 1 MHz.

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Table 4 Device address overview

The addresses are selected to ensure a minimum Hamming distance of 4 between them.

Product Type	Default address[1)] write	Default address[1)] read	***IICadr*** (bit-6)	***IICadr*** (bit-5)	***ID*** (bit-5)	***ID*** (bit-4)
A0	$6A_H$	$6B_H$	0_B	0_B	0_B	0_B
A1	44_H	45_H	0_B	1_B	0_B	1_B
A2	$F0_H$	$F1_H$	1_B	0_B	1_B	0_B
A3	88_H	89_H	1_B	1_B	1_B	1_B

Table 5 /INT (interrupt), collision avoidance and clock stretching configuration

CA	INT	Configuration
0_B	0_B	/INT and collision avoidance enabled Clock stretching disabled
0_B	1_B	/INT and collision avoidance disabled Clock stretching enabled This configuration must not be used: • in fast mode • with the “read” trigger-bits (7:5) = 010_B or 011_B (see ***Table 6***) • with the trigger option ***TRIG*** bit = 01_B.

1 See data sheet ordering information

Table 5 /INT (interrupt), collision avoidance and clock stretching configuration (continued)

CA	INT	Configuration
1_B	0_B	/INT enabled and collision avoidance disabled Clock stretching disabled
1_B	1_B	/INT and collision avoidance disabled Clock stretching disabled

Low Power Mode update rate

Register name	Address	Reset Value
MOD2	13_H	(bits 7:5) 000_B

7	5	4	0
PRD		Reserved	

Field	Bits	Type	Description
PRD	7:5	rw	**Update rate settings** If 000_B typ. update frequency $f_{Update} \approx 770$ Hz. If 001_B typ. update frequency $f_{Update} \approx 97$ Hz. If 010_B typ. update frequency $f_{Update} \approx 24$ Hz. If 011_B typ. update frequency $f_{Update} \approx 12$ Hz. If 100_B typ. update frequency $f_{Update} \approx 6$ Hz. If 101_B typ. update frequency $f_{Update} \approx 3$ Hz. If 110_B typ. update frequency $f_{Update} \approx 0.4$ Hz. If 111_B typ. update frequency $f_{Update} \approx 0.05$ Hz.
Reserved	4:0	rw	**Factory settings** Do not modify, read before write required.

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1.2.6 Diagnostic, reserved, status, and version registers

The device provides diagnostic and status information in register 06_H and version information in register 16_H.

Sensor diagnostic and status register

Register name	Address	Reset Value
Diag	06_H	60_H

7	6	5	4	3	2	1	0
P	FF	CF	T	PD3	PD0	FRM	

Field	Bits	Type	Description
P	7	r	**Bus parity** This bit adds up to an odd parity of the registers 00_H through 05_H (including 05_H), described in ***Measurement data and registers combined in the I²C parity bit "P"***. The parity bit is generated during the I²C readout. The address byte, register byte and acknowledge bits are not included in the parity sum. If the parity calculated by the microcontroller after I²C reads is incorrect, these values must be treated as invalid.
FF	6	r	**Fuse parity flag** Provides a flag from the internal fuse parity check of registers 11_H to 15_H. This parity check includes the ***FP*** bit. If 1_B parity is OK. If 0_B the parity is not correct. The sensor must be considered defective and must no longer be used. A sensor with an invalid fuse parity disconnects its SDA. It will automatically go to low-power mode and only uses the /INT signal to communicate the error (collision avoidance is enabled).
CF	5	r	**Wake Up and configuration parity flag** Provides a flag from the internal configuration and Wake Up parity check of registers 07_H through 10_H (including 10_H) without the WA and the reserved bits. This parity check includes the ***CP*** bit. If 1_B parity is OK. If 0_B parity is not OK, or after startup or after reset the ***CP*** bit is false to indicate a reset of all registers. Thus the ***CP*** bit has to be corrected once after startup or a reset.
T	4	r	**T bit** If 1_B and device is configured to extra short range: data in registers 00_H till 05_H are valid measurement data. If 0_B and device is configured to full or short range: data in registers 00_H till 05_H are valid measurement data. Otherwise: data in registers 00_H till 05_H are invalid measurement data.
PD3	3	r	**Power-down flag 3** If 1_B ADC-conversion of Temp is completed and valid measurement data can be read out. Thus it must be 1_B at readout. If 0_B ADC-conversion of Temp is running and read measurement data are invalid. Any readout with PD3 bit = 0_B should be considered invalid. At startup, this is 0_B until one ADC conversion has been performed. The value then changes to 1_B.

1 I²C Register

Field	Bits	Type	Description
PD0	2	r	**Power-down flag 0** If 1_B the ADC conversion of Bx is completed and valid measurement data can be read out. Thus it must be 1_B at readout. If 0_B the ADC conversion of Bx is running and read measurement data are invalid. Any readout with PD0 bit = 0_B should be considered invalid. At startup, this is 0_B until one ADC conversion has been performed. The value then changes to 1_B.
FRM	1:0	r	**Frame counter** Increments at every updated ADC-conversion, once a X/Y/Z/T or X/Y/Z or X/Y conversion is completed and the new measurement data have been stored in the registers 00_H till 05_H. The microcontroller shall check if bits change in consecutive conversion runs.

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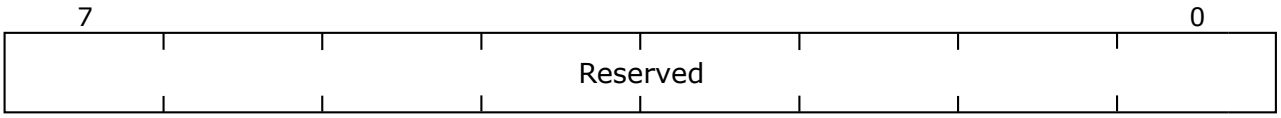
Reserved register

Register name	Address	Reset Value
Reserved	12_H	device specific



Field	Bits	Type	Description
Reserved	7:0	rw	**Factory settings** Do not modify, read before write required.

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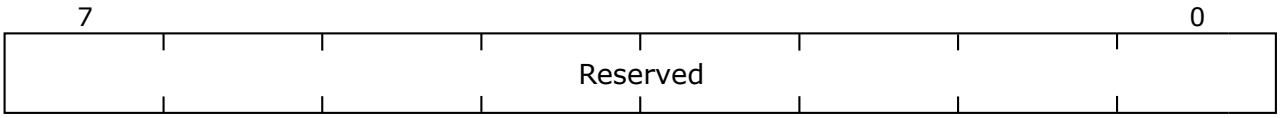
Reserved register

Register name	Address	Reset Value
Reserved	15_H	00_H



Field	Bits	Type	Description
Reserved	7:0	w	**Factory settings** Do not modify, only write reset value.

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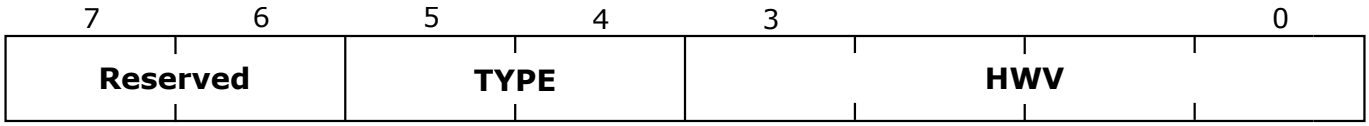
Version register

Register name	Address	Reset Value
Ver	16_H	$C9_H$, $D9_H$ or $E9_H$

1 I²C Register



Field	Bits	Type	Description
Reserved	7:6	r	**Factory settings**
TYPE	5:4	r	**Chip feature** If 00_B, 10_B or 01_B: device with Wake Up feature.
HWV	3:0	r	**Hardware revision** If 9_H it is the B21 design step.

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2 I²C Interface

The TLI493D-W2BW uses Inter-Integrated Circuit (I²C) as the communication interface with the microcontroller.

The I²C interface has three main functions:

- Sensor configuration
- Transmit measurement data
- Interrupt handling

This sensor provides two I²C read protocols:

- 16-bit read frame (µC is driving data), so called ***2-byte read command***.
- 8-bit read frame (µC is driving data), so called ***1-byte read command***.

2.1 I²C protocol description

The TLI493D-W2BW provides one I²C write protocol, based on 2 bytes and two I²C read protocols. Default is the 2-byte read protocol. With the ***PR*** bit it can be selected, if the 1-byte read protocol or the 2-byte read protocol is used.

2.1.1 General description

- The interface conforms to the I²C fast mode specification (400kBit/sec max.), but can be driven faster according to the data sheet.
- The TLI493D-W2BW does not support “repeated starts”. Each addressing requires a start condition.
- The interface can be accessed in any power mode.
- The data transmission order is Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- A I²C communication is always initiated with a start condition and concluded with a stop condition by the master (microcontroller). During a start or stop condition the SCL line must stay “high” and the SDA line must change its state: SDA line falling = start condition and SDA line rising = stop condition.
- Bit transfer occur when the SCL line is “high”.
- Each byte is followed by one ACK bit. The ACK bit is always generated by the recipient of each data byte.
  - If no error occurs during the data transfer, the ACK bit will be set to “low”.
  - If an error occurs during the data transfer, the ACK bit will be set to “high”.
  - If the communication is finished (before the Stop condition), the ACK bit must be set to “high”.

2.1.2 I²C write command

Write I²C communication description:

- The purpose of the sensor address is to identify the sensor with which communication should occur. The sensor address byte is required independently of the number of sensors connected to the microcontroller.
- The register address identifies the register in the bitmap (according to ***Figure 1***) with which the first data byte will be written.
- Data bytes are transmitted as long as the SCL line generates pulses. Each additional data byte increments the register address until the stop condition occurs.
- Bytes transmitted beyond the register address frame are ignored and the corresponding ACK bit is sent “high”, indicating an error.

The I²C write communication frame consists of:

- The start condition.
- The sensor address, according to .
- Write command bit = “low” (read = “high”).

- Acknowledge ACK.
- Trigger bits, according to ***Table 6***.
- The register address, according to ***Figure 1***.
- Acknowledge ACK.
- Writing of one or several bytes to the sensor, each byte followed by an acknowledge ACK.
- The stop condition.

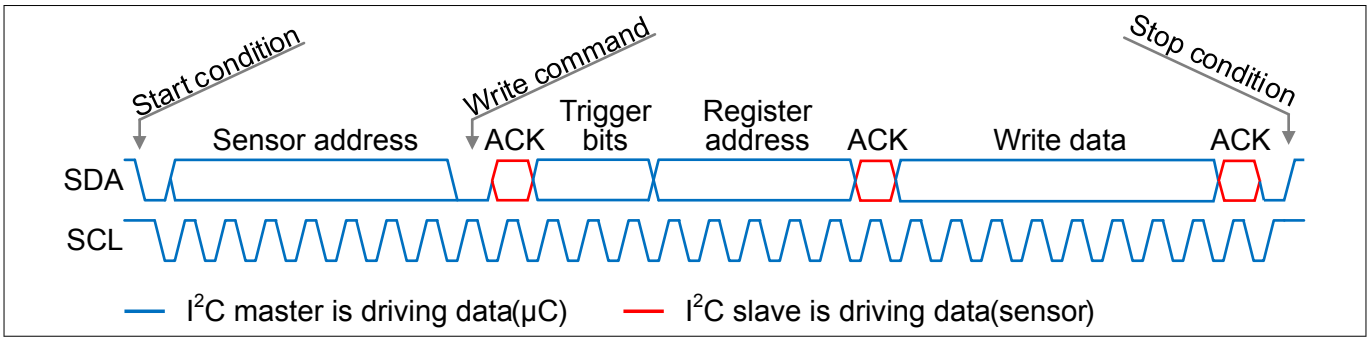

Figure 2 General I²C write frame format: Write data from microcontroller to sensor

Trigger bits in the I²C protocol

The trigger bits are used in Power Down Mode. The Power Down Mode is used in the Master Controlled Mode, when no measurement is running. Thus the trigger bits are relevant for the Master Controlled Mode as well.

For a more silent measurement environment it is recommended to separate the measurement and the communication as much as possible, by using the trigger bits = 001_B or trigger bits = 100_B and communicate between two measurements with reduced overlap of measurement and communication.

Table 6 I²C trigger bits

Read/Write command	Trigger-bit 7	Trigger-bit 6	Trigger-bit 5	Trigger command
0_B	0_B	0_B	0_B	no ADC trigger
0_B	0_B	0_B	1_B	ADC trigger after write frame is finished, ***Figure 4***
0_B	0_B	1_B	0_B	no ADC trigger
0_B	0_B	1_B	1_B	ADC trigger after write frame is finished, ***Figure 4***
0_B	1_B	0_B	0_B	no ADC trigger
0_B	1_B	0_B	1_B	ADC trigger after write frame is finished, ***Figure 4***
0_B	1_B	1_B	0_B	no ADC trigger
0_B	1_B	1_B	1_B	must not be used
1_B	0_B	0_B	0_B	no ADC trigger
1_B	0_B	0_B	1_B	no ADC trigger
1_B	0_B	1_B	0_B	ADC trigger before first MSB, ***Figure 3***
1_B	0_B	1_B	1_B	ADC trigger before first MSB, ***Figure 3***
1_B	1_B	0_B	0_B	ADC trigger after register 05_H ***Figure 5***
1_B	1_B	0_B	1_B	ADC trigger after register 05_H, ***Figure 5***
1_B	1_B	1_B	0_B	ADC trigger after register 05_H, ***Figure 5***
1_B	1_B	1_B	1_B	must not be used

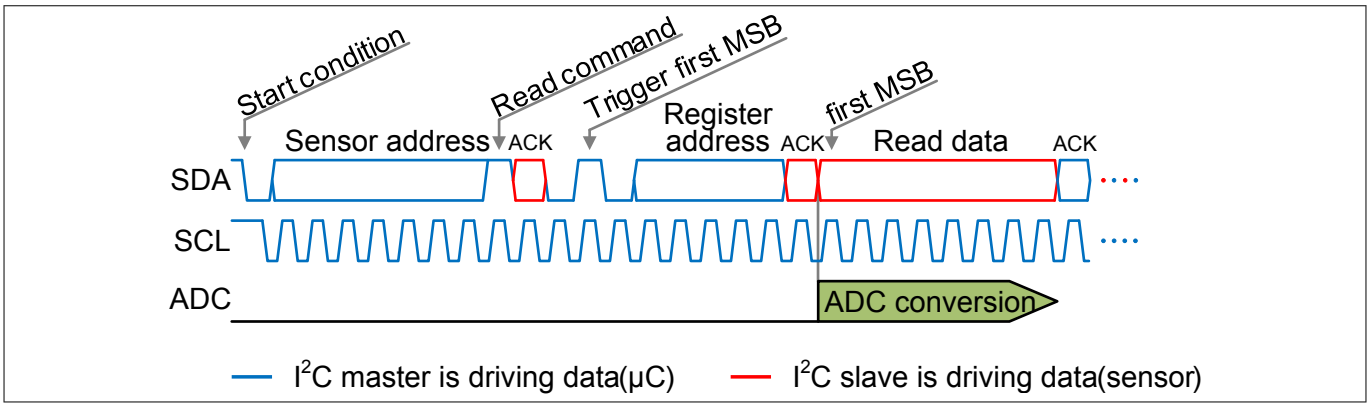

Figure 3 ADC trigger before sending first MSB of data registers, I²C trigger bits 010_B

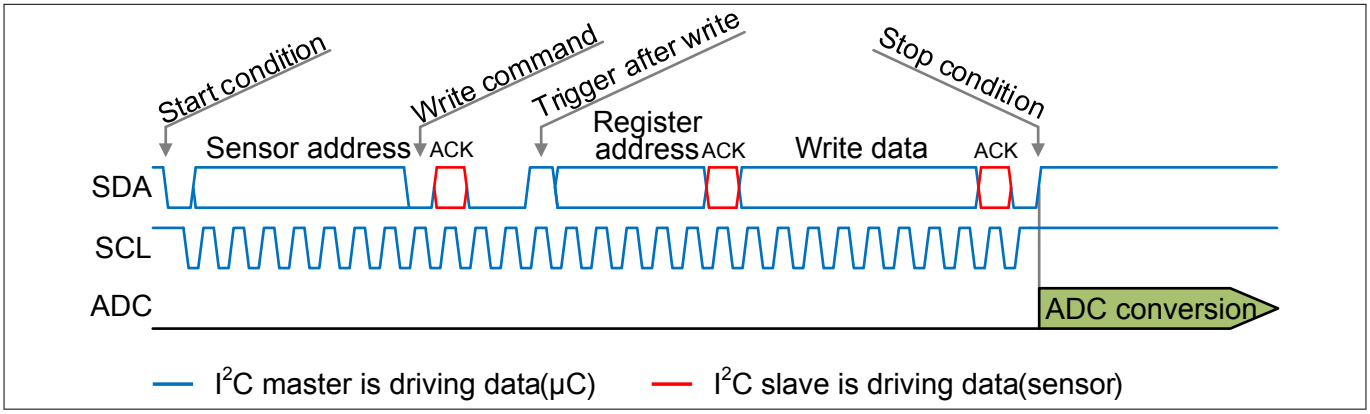

Figure 4 ADC trigger after write frame is finished, I²C trigger bits 001_B

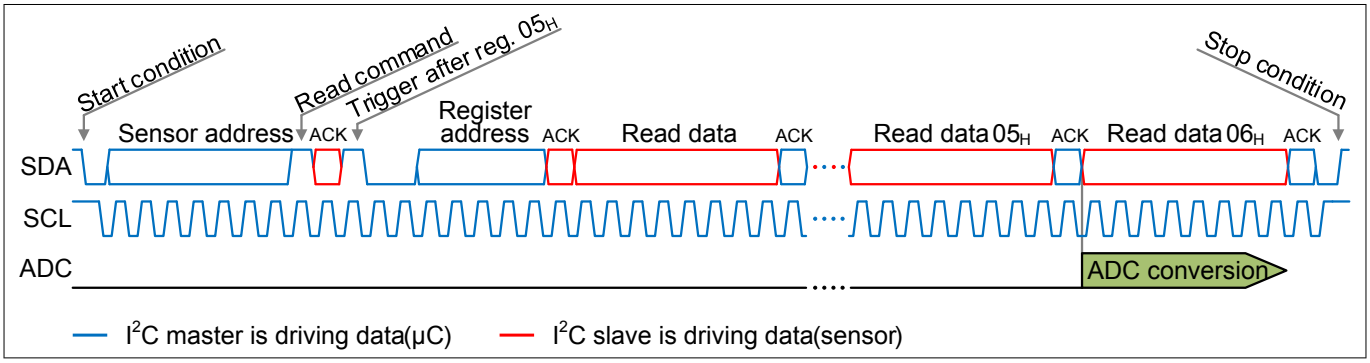

Figure 5 ADC trigger after register 05_H, I²C trigger bits 100_B

Example I²C write communication

An example of a write communication is provided in ***Figure 6***.
In this example the sensor with the address $6A_H$ / $6B_H$ (see ***Table 4***) should be configured for:

- Master Controlled Mode
- /INT disabled
- Clock stretching enabled
- No trigger of a measurement
- Other settings should be kept as is

Implementation:

- The microcontroller generates a start condition

- Configuration changes can only be performed with a write command. The address for write operation of this sensor is $6A_H = 01101010_B$
- If the sensor detects no error, the ACK = 0_B is transmitted back to the microcontroller
- No measurement is performed if the trigger bits = 000_B
- The register to change the required settings is 11_H according the bitmap ***Figure 1*** = 10001_B
- If the sensor detects no error, the ACK = 0_B is transmitted back to the microcontroller
- The parity bit "FP" is the odd parity of the registers 11_H and 13_H (bits 7:5), see ***FP*** register, thus it is not possible to quantify it in this example
- The sensor address should not be changed, i.e. the sensor address $6A_H$ / $6B_H$ should be kept. Thus the ***IICadr*** bits = 00_B, see ***IICadr*** registers
- The 2-byte protocol should be kept as is. Thus the ***PR*** bit = 0_B
- In order to enable clock stretching and disable /INT the ***CA*** bit must be set to 0_B and the ***INT*** bit must be set to 1_B (see ***Table 5***)
- To use the Master Controlled Mode the ***MODE*** bits must be set to 01_B
- If the sensor detects no error the ACK = 0_B is transmitted back to the microcontroller
- The microcontroller generates the stop condition

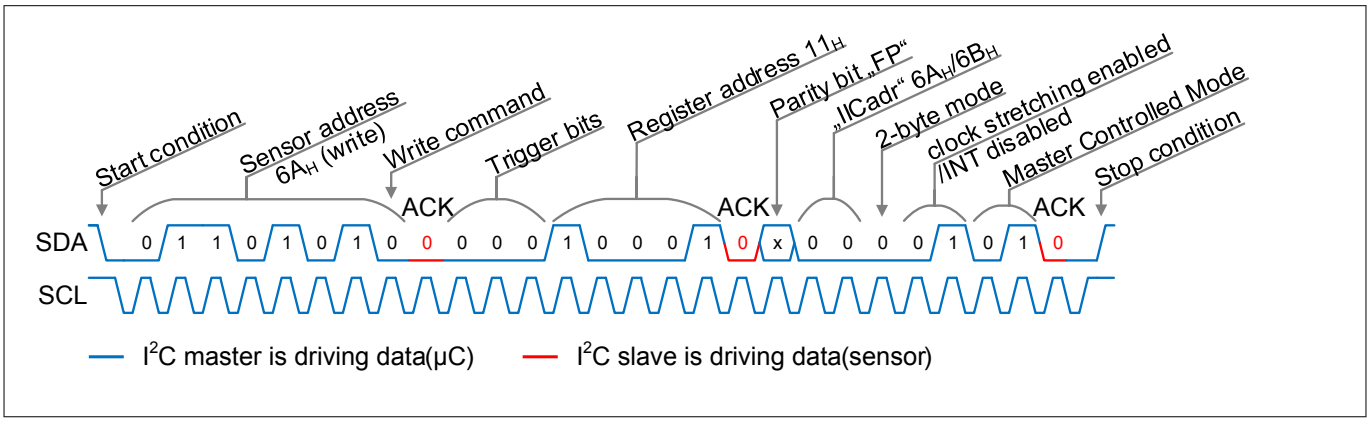

Figure 6 Example I²C frame format 2-byte: Write data from microcontroller to sensor

2.1.3 I²C read commands

Read I²C communication description:

- The purpose of the sensor address is to identify the sensor with which communication should occur. The sensor address byte is required independently of the number of sensors connected to the microcontroller.
- Only available in the 2-byte read command: The register address identifies the register in the bitmap (according ***Figure 1***) from which the first data byte will be read. In the 1-byte read command the read out starts always at the register address 00_H.
- As many data bytes will be transferred as long as pulses are generated by the SCL line. Each additional data byte increments the register address. Until the stop condition occurs.
- If bytes are read beyond the register address frame the sensor keeps the SDA = 1_B.
- If the microcontroller reads data and does not acknowledge the sensor data (ACK = 1_B) the sensor keeps the SDA = 1_B until the next stop condition.

2.1.3.1 2-byte read command

The I²C read communication frame consists of:

- The start condition
- The sensor address, according to ***Table 4***
- Read command bit = "high" (write = "low")

- Acknowledge ACK
- Trigger bits, according to ***Table 6***
- The register address, according to ***Figure 1***
- Acknowledge ACK
- Reading of one or several bytes from the sensor, each byte followed by an acknowledge ACK
- The stop condition

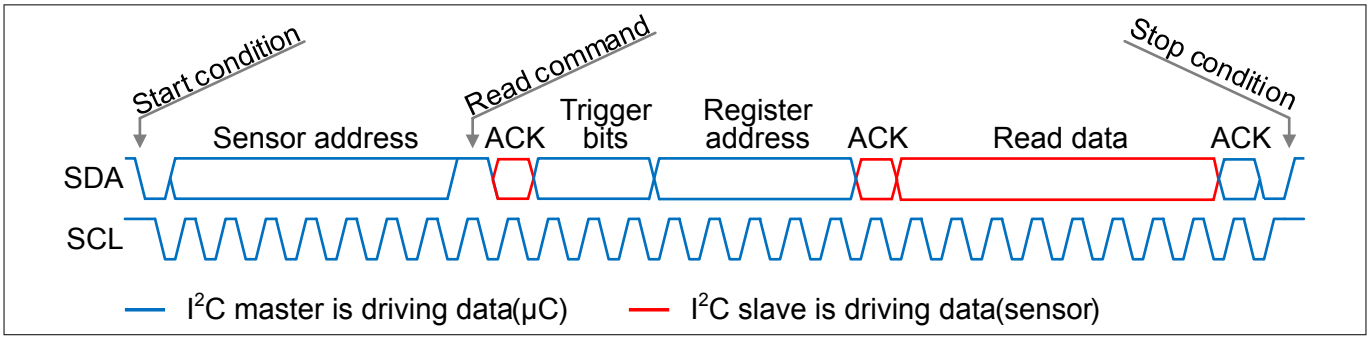

Figure 7 General I²C frame format 2-byte: Read data from sensor to microcontroller

2.1.3.2 1-byte read command

The 1-byte read mode can be entered, by configuring the ***PR*** bit with an write communication. For example with the write cycle:

- start condition
- $6A_H$ (sensor address)
- 11_H (register address)
- $XXX1\ XXXX_B$ (***PR*** bit = 1_B)
- stop condition

The I²C communication frame consists of:

- The start condition
- The sensor address, according to ***Table 4***
- Read command bit = “high” (write = “low”)
- Acknowledge ACK
- Reading of one or several bytes from the sensor, each byte followed by an acknowledge ACK
- The stop condition

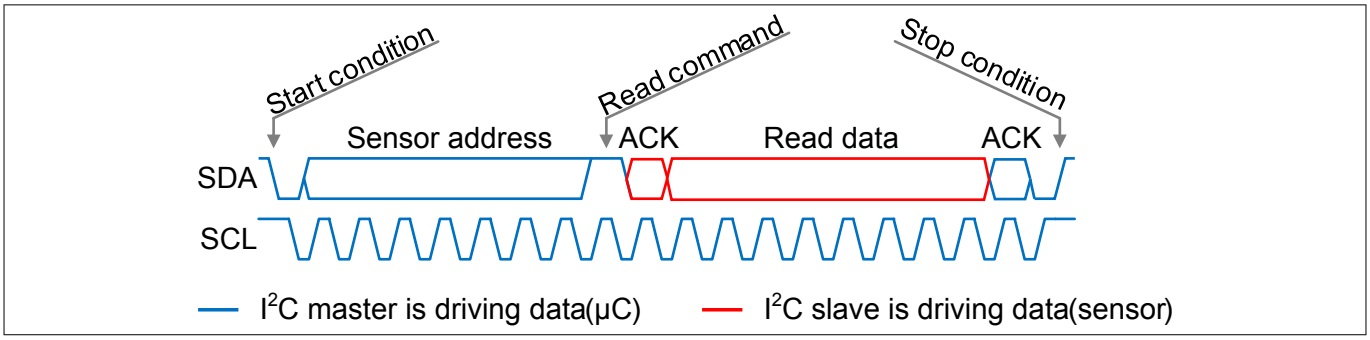

Figure 8 General I²C frame format 1-byte: Read data from sensor to microcontroller

Example I²C 1-byte read communication

An example of a read communication is provided in ***Figure 9***.

In this example, the sensor with the address $F0_H$ / $F1_H$ (see ***Table 4***) should read out the measurement values, registers 00_H - 05_H and the diagnostic register 06_H:

Implementation:

- The microcontroller generates a start condition
- The address for read operation of this sensor is $F1_H = 11110001_B$. This address value must be transmitted by the microcontroller to the sensor
- If the sensor detects no error, the ACK = 0_B is transmitted back to the microcontroller
- The microcontroller must go on clocking the SCL line
- The sensor transmits 8 data bits of register 00_H to the microcontroller
- If the microcontroller detects no error the ACK = 0_B is transmitted back to the sensor
- The microcontroller must go on clocking the SCL line
- The sensor transmits 8 data bits of register 01_H to the microcontroller
- ...
- After transmitting the register 06_H the microcontroller transmits a NACK
- The microcontroller generates the stop condition

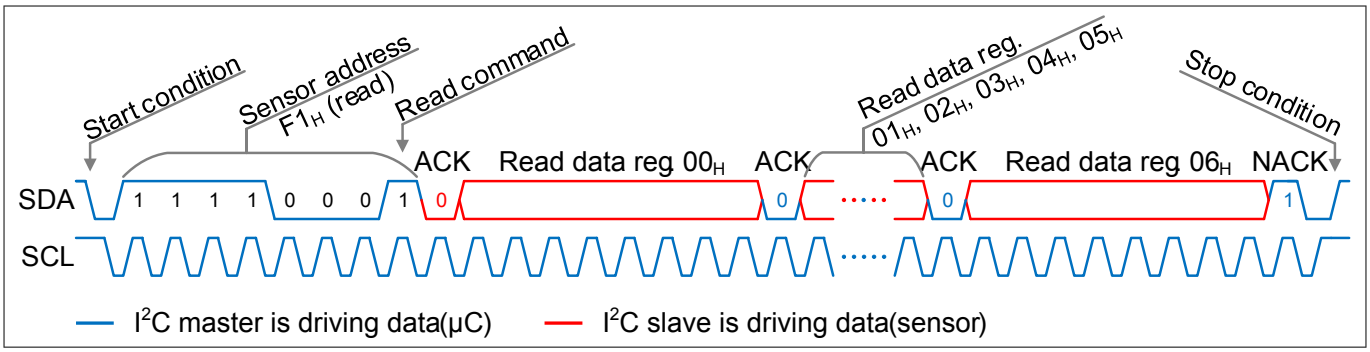

Figure 9 Example I²C frame format 1-byte: Read data from sensor to microcontroller

2.2 Collision avoidance and clock stretching

Using the configuration bits ***CA*** and ***INT***, collision avoidance and clock stretching can be configured, see ***Table 5***.

The usage of the collision avoidance and clock stretching feature depends on the implemented application circuit which are described in the product datasheet. ***Table 7*** provides an overview.

Table 7 Default and alternative application circuit

	Default application circuit	**Alternative application circuit**
Description	/INT and SCL pin are shorted	/INT and SCL pin are separately connected
Benefits	Only two communication pins	No dual use of I²C clock line
Collision avoidance	Recommended to enable if /INT signal is used to avoid collisions on the I²C clock signal	Recommended to disable
Clock stretching	Supported	Not supported

2.2.1 Collision avoidance

If the collision avoidance feature is enabled, the sensor will not transmit an /INT pulse between an I²C start and stop condition. This allows to short the /INT pin with the SCL pin (default application circuit) without the risk that an /INT pulse disturbs an ongoing communication. An suppressed /INT pulse will not be repeated.

An example without collision avoidance and clock stretching is shown in ***Figure 10***. In this example:

- The data read out starts while the ADC conversion is running
- The sensor interrupt disturbs the I²C clock, causing an additional SCL pulse which shifts the data read out by one bit

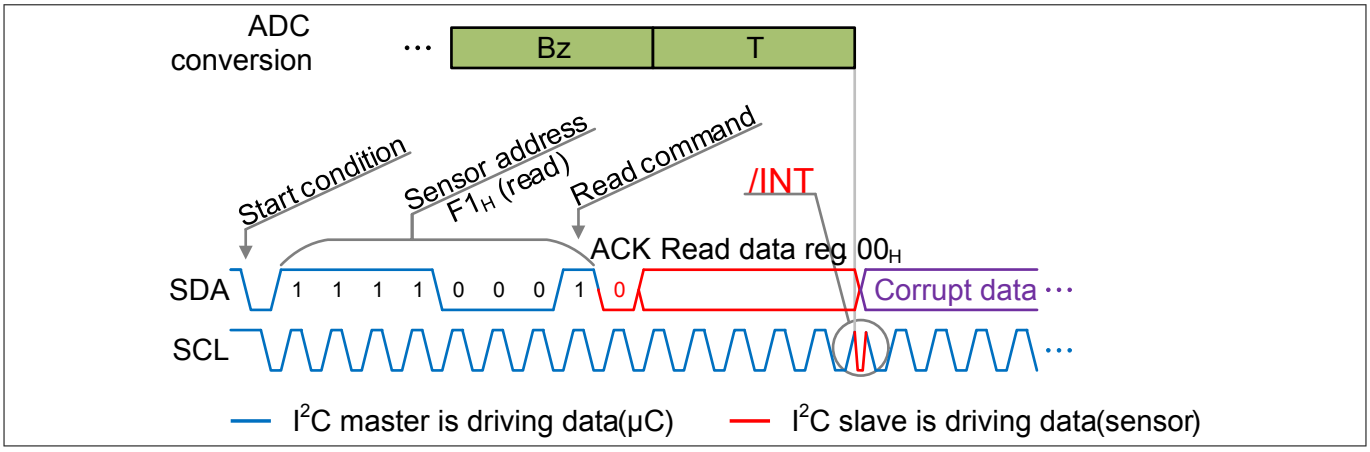

Figure 10 Example without collision avoidance CA bit =1$_B$ and INT bit = 0$_B$ (default application circuit)

The same example communication but with activated collision avoidance is shown in ***Figure 11***. Now the /INT pulse is suppressed and the communication is not disturbed.

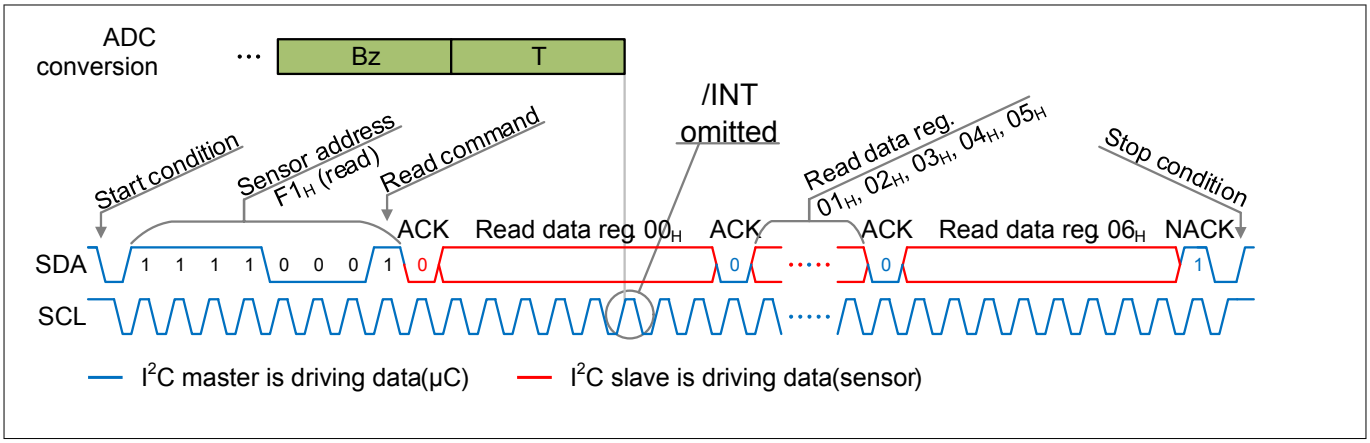

Figure 11 Example with collision avoidance CA bit =0$_B$ and INT bit = 0$_B$

2.2.2 Clock stretching

If the clock stretching feature is enabled, the sensor can delay an I²C readout while an ADC conversion is ongoing to avoid the readout of inconsistent data. To use clock stretching it must be supported by the I²C master.

The sensor pulls down the I²C clock line in the following condition:

- /INT pin and SCL are shorted (default application circuit)
- An ADC conversion is in progress
- The sensor is addressed for register read (writes are never affected by clock stretching)
- The sensor is about to transmit the valid ACK in response to the I²C addressing of the microcontroller

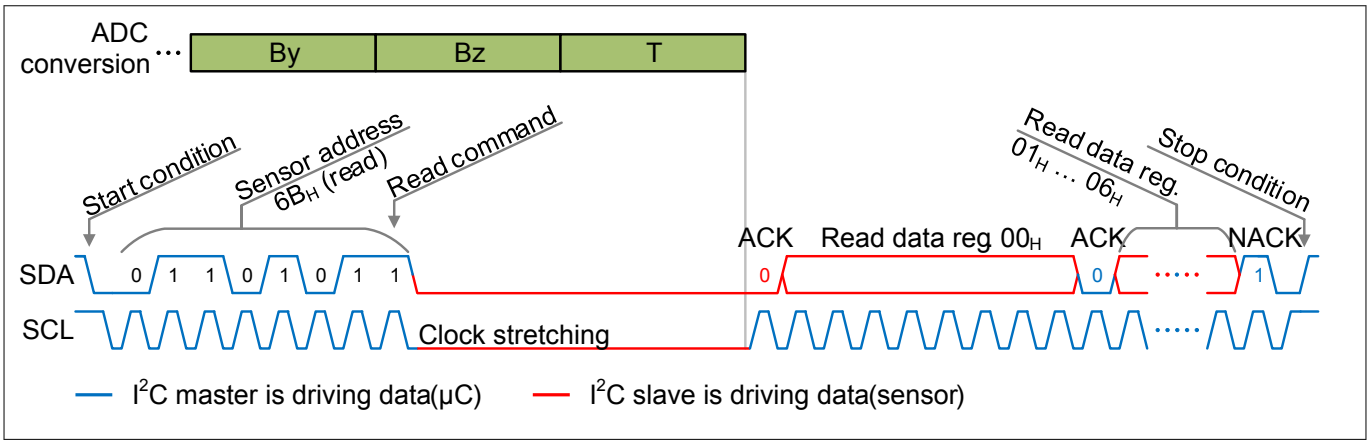

Figure 12 Example with clock stretching CA bit =0_B and INT bit = 1_B (default application circuit)

2.3 Sensor reset by I²C

If the microcontroller is reset, the communication with the sensor may be corrupted, possibly causing the sensor to enter an incorrect state. The sensor can be reset via the I²C interface by sending the following command sequence from the microcontroller to the sensor:

- Start condition
- Sending FF_H
- Stop condition
- Start condition
- Sending FF_H
- Stop condition
- Start condition
- Sending 00_H
- Stop condition
- Start condition
- Sending 00_H
- Stop condition
- 30 µs delay

After a reset, the sensor must be reconfigured to the desired settings. The reset sequence uses twice the identical data to assure a proper reset, even when an unexpected /INT pulse occurs.

Spikes can be interpreted as bus signals causing an action. For example when the collision avoidance feature is active and if the SDA line spikes together with SCL line this could be interpreted as start condition, blocking further /INT pulses until a stop condition appears on the bus. In such a case the sensor must be reset in order to initialize it. If the sensor does not respond after the reset, it must be considered defective.

Such spikes may occur as the sensor powers up. Because of this we recommend to using the reset sequence after each power up before configuring the sensor.

If the microcontroller resets during an ongoing I²C communication, the SDA line could get stuck low. This would block the I²C bus and is a well-known limitation of the I²C interface. To recover from this situation please use the reset sequence described in this chapter.

2.4 Sensor Initialization and Readout example

To ensure that both the microcontroller and the sensor are synchronized and properly initialized, it is recommended to apply the I²C reset and upload the fuse register settings each time the microcontroller is reset, see ***Figure 13***.

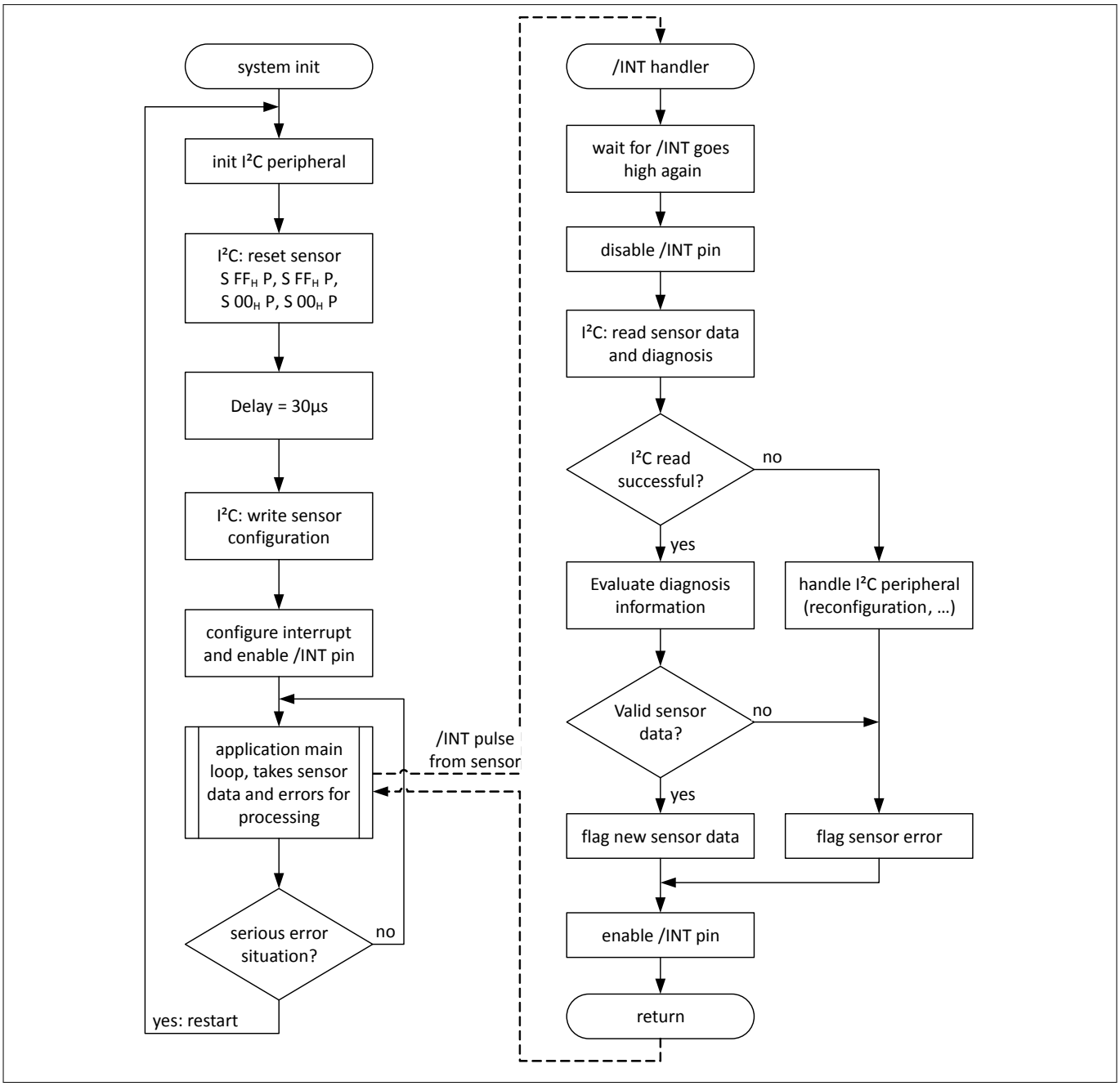

Figure 13 Microcontroller software flowchart for TLI493D-W2BW

2.5 Loss of V_{DD} impact on I²C bus

If the SDA or SCL line is pulled “low” and the sensor is disconnected from the V_{DD} supply line, the affected I²C line will most likely get a stuck in the Low state and will interfere with the communication on the bus.

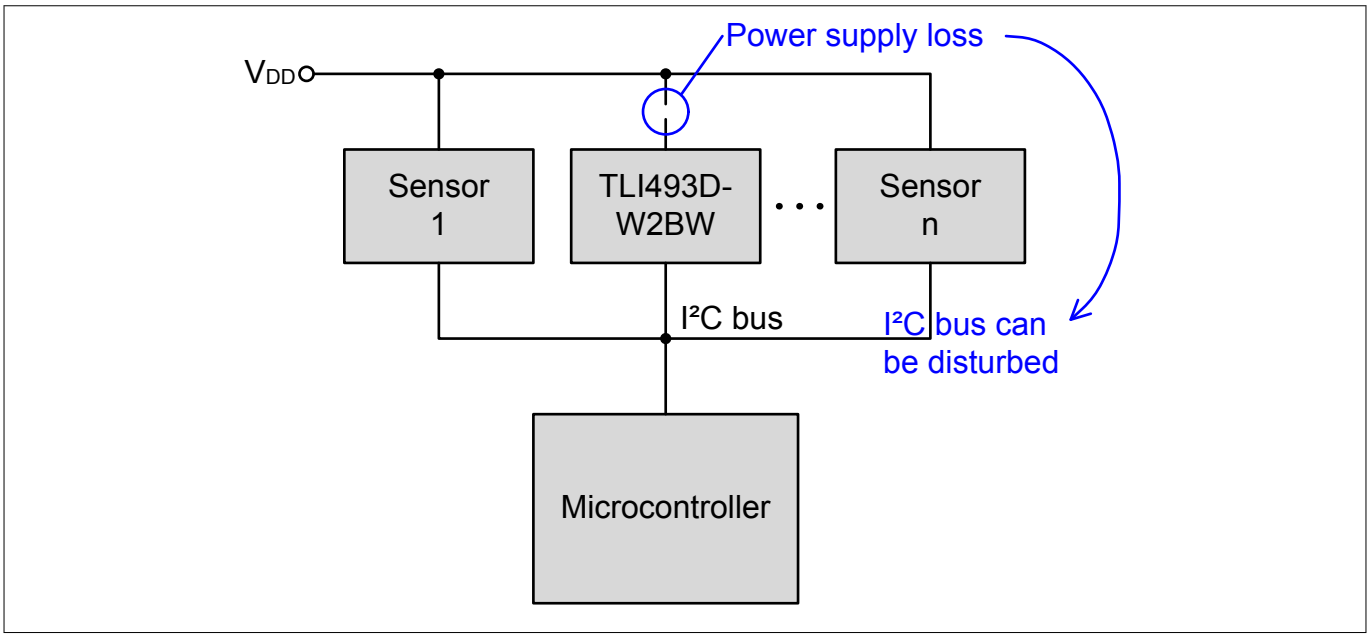

Figure 14 Example of I²C bus and a TLI493D-W2BW with disconnected V_{DD}

When V_{DD} is pulled to GND the SDA and SCL line will not disturb the bus.

3 Wake Up mode

The Wake Up mode (or short WU mode) is intended to be used together with the automated sensor modes (e.g. Low Power mode or Fast mode). In principle, it works with the Master Controlled mode as well, but it might not really be useful there because a controlled trigger usually implies the need to acquire a new measurement.

This WU mode can be used to allow the sensor to continue making magnetic field measurements while the µC is in the power-down state, which means the microcontroller will only consume power and access the sensor if relevant measurement data is available. This can be done either by using static thresholds (for example for applications where only movements of magnets away from a default position are relevant) or by using dynamic thresholds (where any movement over a specific uncertainty limit should be detected once). The figure below illustrates these two cases.

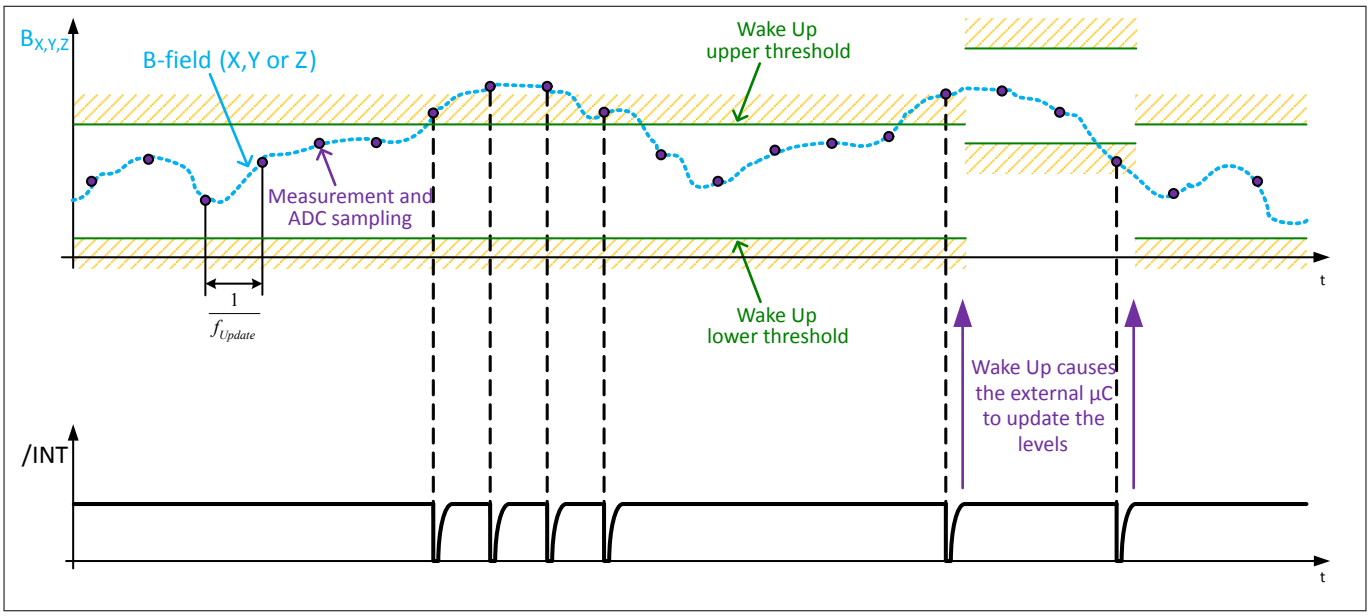

Figure 15 Static or Dynamic Wake Up Threshold Operation of the TLI493D-W2BW

This dynamic WU mode operation offers another option which is particularly useful in Fast mode with limited I²C bus capabilities and/or low bit rates. In this case, the WU mode can act as a “data filter” to reduce the bus load by preventing sensor data from being read that does not change significantly. So due to an interrupt, the new WU levels are adapted to the actual value read (for each X, Y, Z channel individually). This provides low latencies for detecting changes but reduces interrupts caused by similar values. If the collision avoidance feature is also used, the readout may take even longer than one conversion time (but this readout speed adds to the overall signal latency as well). As the thresholds also need to be set, a complete data read and set of new WU thresholds is not even feasible with the fastest specified bit rate within one sensor sample time in Fast mode.

The next figure illustrates this more clearly:

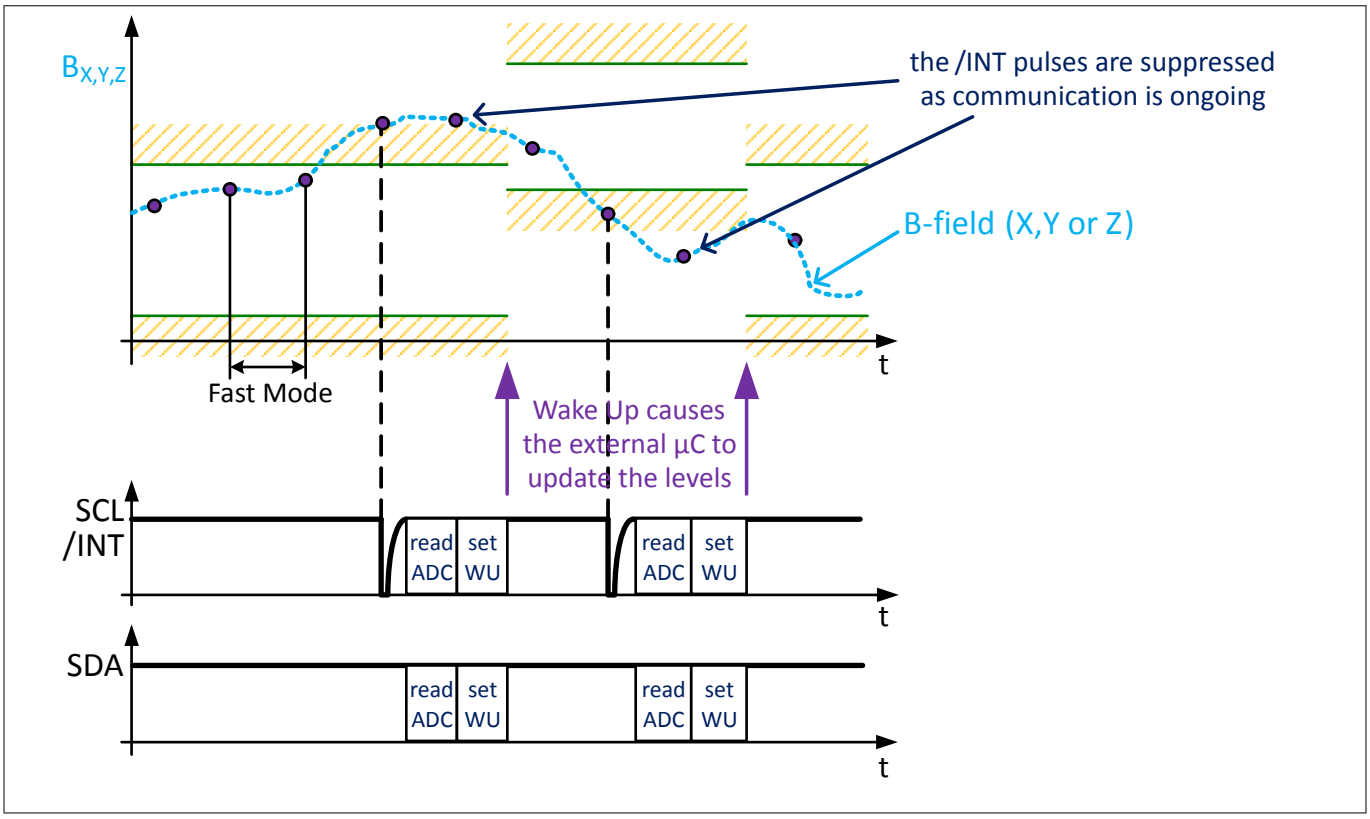

Figure 16 Dynamic Wake Up Threshold Operation of the TLI493D-W2BW for Bandwidth Reduction

To sum this up, we can state that this dynamic WU mode operation together with the Fast mode set allows detecting and reading significant value changes with low latency, even if the bit rate of the I²C cannot be set fast enough to read the data for each set of sensor data generated.

3.1 Wake Up activation

The Wake Up function can be activated with the ***WU*** bit and by modifying at least one of the Wake Up threshold registers of address 07_H to $0F_H$, see ***Configuration registers combined in the I²C parity flag "CF"***. The Wake Up function is only supported if the device is configured to full or short range sensitivity.

Please note that the Wake Up registers cover bit 11 to bit 1. Bit 0 is not accessible, but internally set with 0_B to get a 12-bit value, for comparison with the 12-bit magnetic field value registers Bx, By and Bz.

3.2 Wake Up constraints

The Wake Up threshold range disabling /INT pulses between upper threshold and lower threshold is limited to a window of the half output range.

This window itself can be moved inside the full output range, as illustrated in ***Figure 17***.

$$\text{„Wake Up upper threshold“}_D > \text{„Wake Up lower threshold“}_D$$

Equation 1

$$\text{„Wake Up upper threshold“}_D - \text{„Wake Up lower threshold“}_D < 2048_D LSB_{12}$$

Equation 2

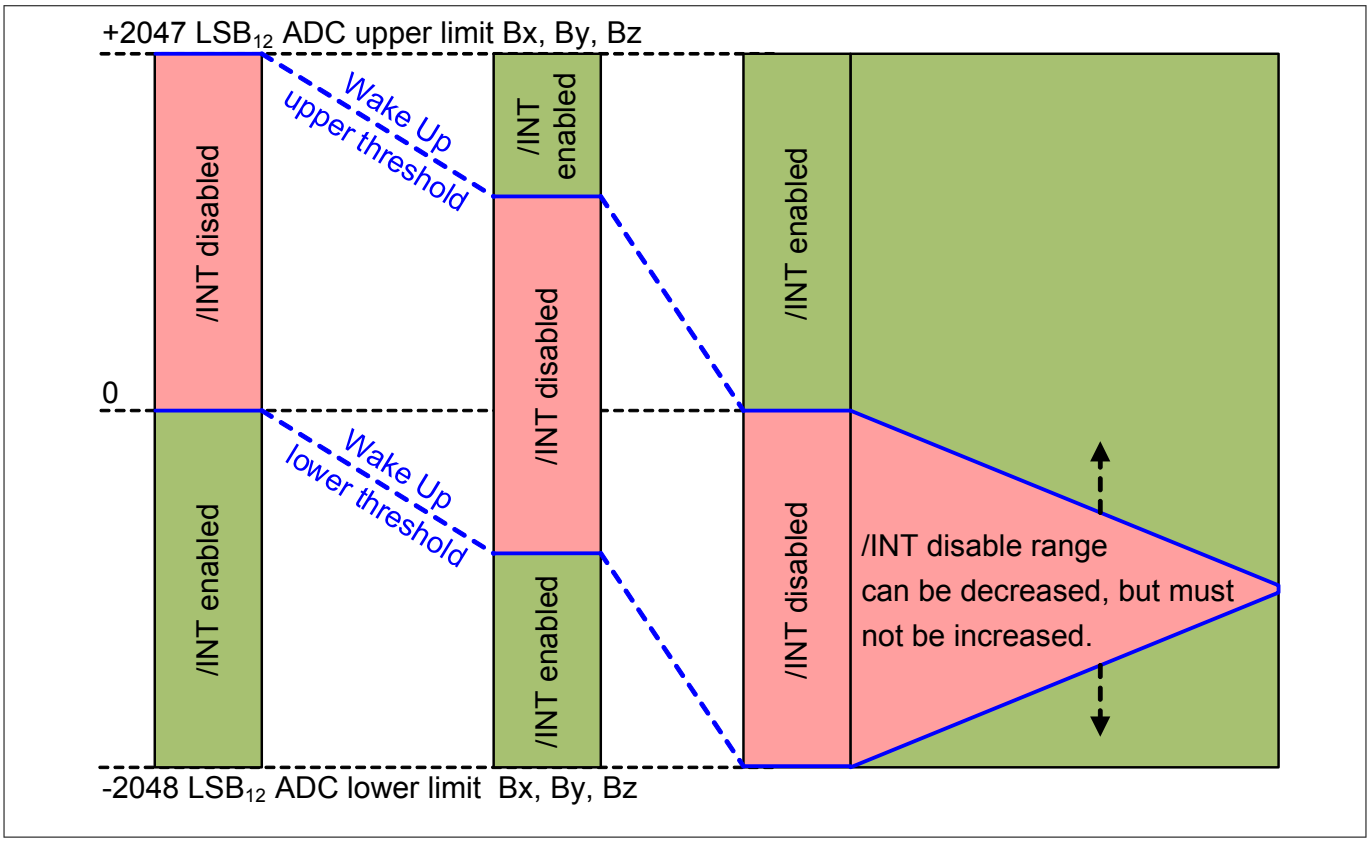

Figure 17 Wake Up enable and disable range examples

3.3 Wake Up in combination with the angular mode

In angular mode, see ***DT*** and ***AM*** bit, the

- "Wake Up Y upper threshold" must be written to the registers $0C_H$ and $0F_H$ (5 ... 3)(ZH in ***Figure 1***)
- "Wake Up Y lower threshold" must be written to the registers $0B_H$ and $0F_H$ (3 ... 1)(ZL in ***Figure 1***)

4 Diagnostic

The sensor TLI493D-W2BW provides diagnostic functions. These functions are running in the background, providing results, which can be checked by the microcontroller for the verification of the measurement results.

To ensure the integrity of received data the following diagnostic functions are available.

4.1 Parity bits and parity flags

Parity bits:

- ***FP*** (mode parity bit)
- ***CP*** (Wake Up and configuration parity bit)
- ***P*** (bus parity bit)

Parity flags:

- ***FF*** (mode parity flag)
- ***CF*** (Wake up and configuration parity flag)

4.2 Power-down flags

During measurements and during ADC conversion, the sensor monitors if the supply voltage is correct and if the conversion is finished. This is indicated by the ***PD3*** and ***PD0*** registers.

4.3 Frame counter

The frame counter ***FRM*** register is incremented by one when a conversion is completed.

5 Terminology

A	
ACK	Achknowledge
ADC	Analog/Digital Converter
adr	address
E	
EMC	Electromagnetic Compatibility
G	
GND	Ground
I	
ID	IDentification
I²C (I2C)	Inter - Integrated Circuit
/INT	Interrupt pin, Interrupt signal
L	
LSB	Least Significant Bits
M	
Magnetic field	Magnetic flux density that the sensor measures
min	minimum
MSB	Most Significant Bit
max	maximum
P	
PCB	Printed Circuit Boards
R	
reg	register
S	
SCL	Clock pin
SDA	Data pin
Sensor	Refers to the TLI493D-W2BW product
Sensor module	Refers to the TLI493D-W2BW product and all the passive elements in the customer‘s module
Supply	Refers to the sensor supply pins V_{DD} and GND (the unused pins are assumed to be connected to GND as well)
V	
V_{DD}	Supply voltage
µ	
µC	Microcontoller

6 Revision history

Revision	Date	Changes
Ver. 1.00	2020-07-28	Initial release
Ver. 1.10	2020-11-02	Updated ***Configuration register*** Updated ***Wake Up enable and X thresholds LSBs*** Updated ***Sensor diagnostic and status register*** Updated ***Wake Up activation***

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Edition 2020-11-02

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-oaa1583397543587

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