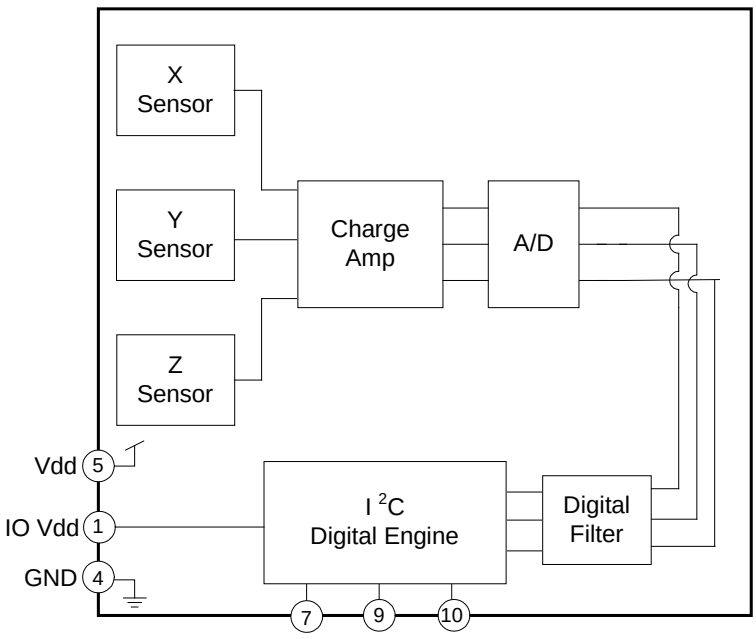
Kionix®	**± 2g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KXTF9-4100** **Rev. 3** **Jul-2010**

Product Description

The KXTF9 is a tri-axis +/-2g, +/-4g or +/-8g silicon micromachined accelerometer with integrated orientation, tap/double tap, and activity detecting algorithms. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning, and intelligent user-programmable application algorithms. The accelerometer is delivered in a 3 x 3 x 0.9 mm LGA plastic package operating from a 1.8 – 3.6V DC supply. I^2C interface is used to communicate to the chip to configure and check updates to the orientation, Directional Tap™ detection and activity monitoring algorithms.

Functional Diagram



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Kionix®	**± 2g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KXTF9-4100** **Rev. 3** **Jul-2010**

Product Specifications

Table 1. Mechanical

(specifications are for operation at 1.8V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	85
Zero-g Offset		mg	-125	-	+125
Zero-g Offset Variation from RT over Temp.		mg/ºC		0.7 (xy) 0.4 (z)	
Sensitivity (12-bit)[1]	GSEL1=0, GSEL=0 (± 2g)	counts/g	988	1024	1060
	GSEL1=0, GSEL0=1 (± 4g)		494	512	530
	GSEL1=1, GSEL0=0 (± 8g)		247	256	265
Sensitivity (8-bit)[1]	GSEL1=0, GSEL=0 (± 2g)	counts/g	61	64	67
	GSEL1=0, GSEL0=1 (± 4g)		30	32	34
	GSEL1=1, GSEL0=0 (± 8g)		15	16	17
Sensitivity Variation from RT over Temp.		%/ºC		0.01 (xy) 0.03 (z)	
Offset Ratiometric Error (V_{dd} = 1.8V ± 5%)		%		0.3	
Sensitivity Ratiometric Error (V_{dd} = 1.8V ± 5%)		%		0.4 (xy) 0.2 (z)	
Self Test Output change on Activation		g		0.9 (x) 0.8 (y) 0.7 (z)	
Mechanical Resonance (-3dB)[2]		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		1	
Cross Axis Sensitivity		%		2	

Notes:

1. Resolution and acceleration ranges are user selectable via I^2C.
2. Resonance as defined by the dampened mechanical sensor.

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Table 2. Electrical

(specifications are for operation at 1.8V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Operating	V	1.8	1.8	3.6
I/O Pads Supply Voltage (V_{IO})		V	1.7		V_{dd}
Current Consumption	All On (Res = 1)	µA	470	570	670
	All On (RES = 0)			230	
	Standby			0.1	
Output Low Voltage[1]		V	-	-	0.3 * V_{io}
Output High Voltage		V	0.9 * V_{io}	-	-
Input Low Voltage		V	-	-	0.2 * V_{io}
Input High Voltage		V	0.8 * V_{io}	-	-
Input Pull-down Current		µA		0	
Start Up Time[2]	RES = 0	ms		0.050	
	RES = 1, ODR = 25 Hz			80	
	RES = 1, ODR = 50Hz			40	
	RES = 1, ODR = 100Hz			20	
	RES = 1, ODR = 200Hz			10	
	RES = 1, ODR = 400Hz			5	
	RES = 1, ODR = 800Hz			2.5	
Power Up Time[3]		ms		20	
I^2C Communication Rate		KHz			400
Output Data Rate (ODR)[4]		Hz	25	50	800
Bandwidth (-3dB)[5]	RES = 0	KHz		1.59	
	RES = 1	Hz		ODR/2	

Notes:

1. Assuming I^2C communication and minimum 1.5Kohm pull-up resistor on SCL and SDA pins.
2. Start up time is from PC1 set to valid outputs.
3. Power up time is from Vdd valid to device boot completion.
4. User selectable through I^2C.
5. User selectable and dependant on ODR and RES.

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Table 3. Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Absolute Limits	V	-0.3	-	6.0
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."

HF

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

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Application Schematic

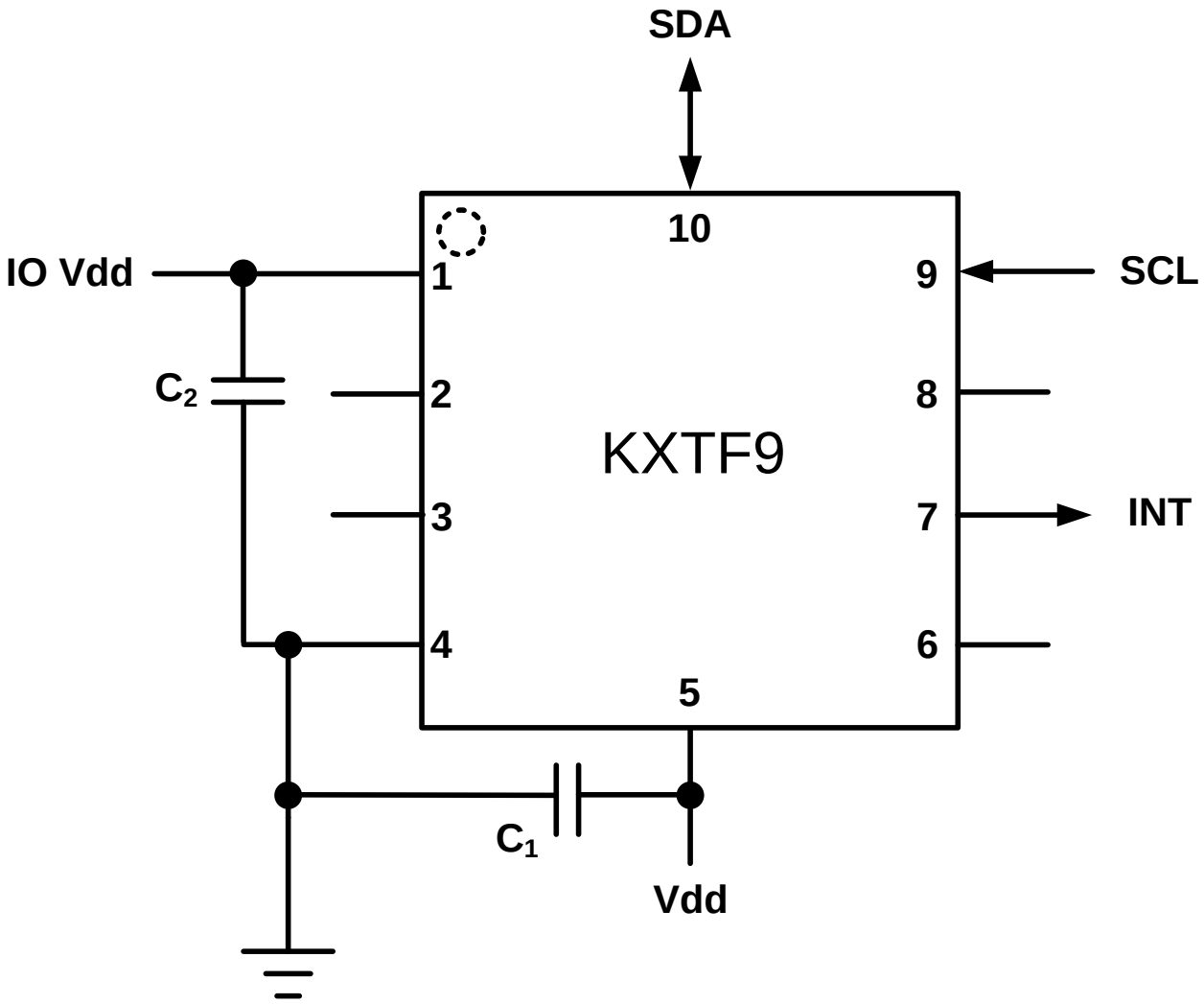

Table 4. KXTF9 Pin Descriptions

Pin	Name	Description
1	IO Vdd	The power supply input for the digital communication bus. Decouple this pin to ground with a 0.1uF ceramic capacitor.
2	DNC	Reserved – Do Not Connect
3	DNC	Reserved – Do Not Connect
4	GND	Ground
5	Vdd	The power supply input. Decouple this pin to ground with a 1uF ceramic capacitor.
6	DNC	Reserved – Do Not Connect
7	INT	Physical Interrupt
8	DNC	Reserved – Do Not Connect
9	SCL	I^2C Serial Clock
10	SDA	I^2C Serial Data

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Test Specifications

***Special Characteristics**:*

These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

Table 5. Test Specifications

Parameter	Specification	Test Conditions
Zero-g Offset @ RT	0 +/- 128 counts	25C, Vdd = 1.8 V
Sensitivity @ RT	1024 +/- 36 counts/g	25C, Vdd = 1.8 V
Current Consumption -- Operating	470 <= Idd <= 670 uA	25C, Vdd = 1.8 V

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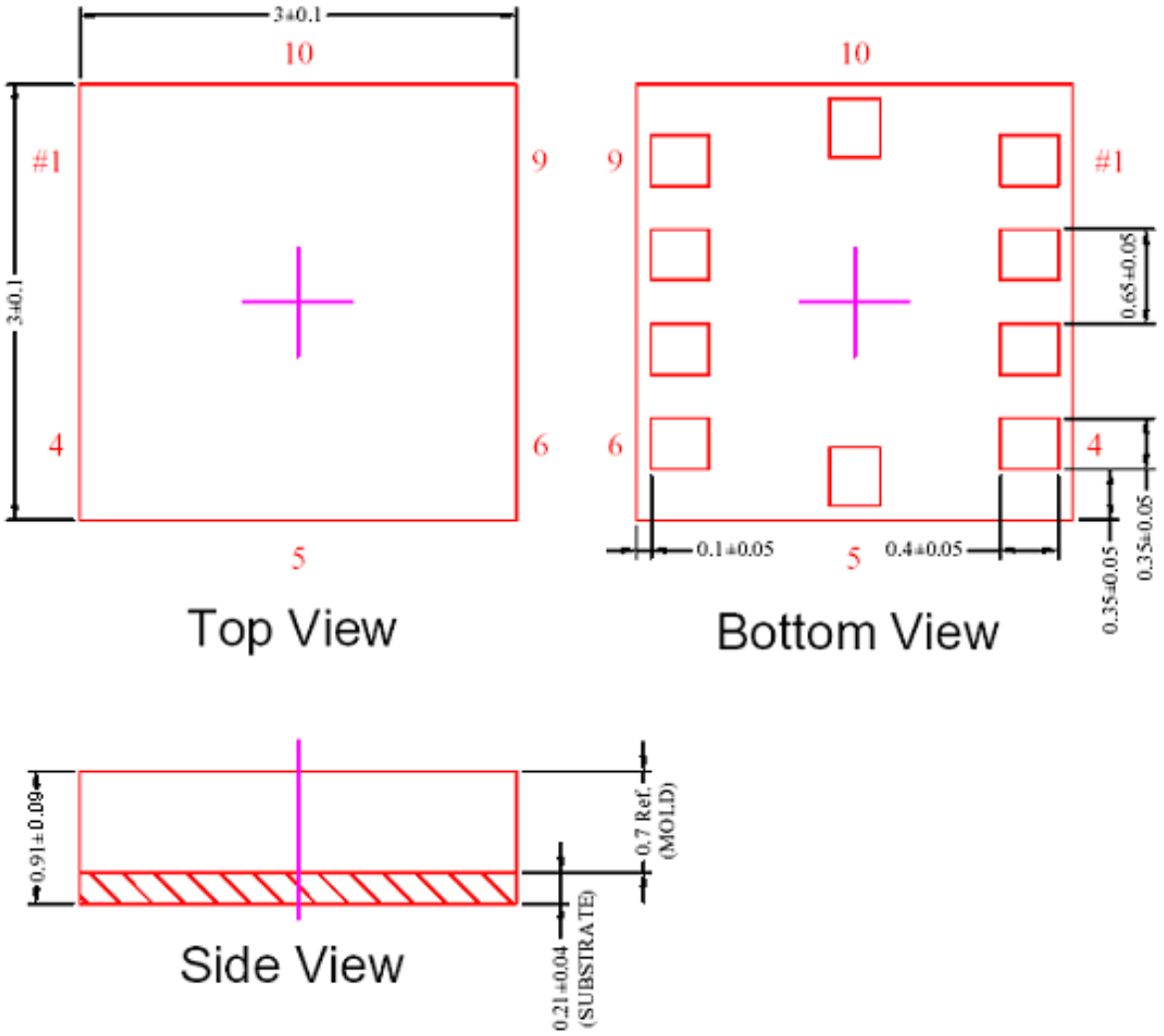
Package Dimensions and Orientation

3 x 3 x 0.9 mm LGA



All dimensions and tolerances conform to ASME Y14.5M-1994

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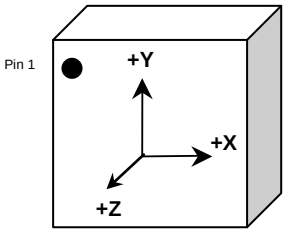
Orientation

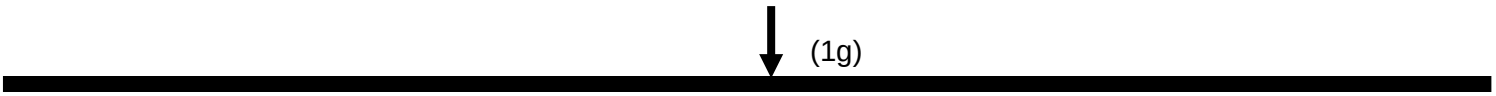


When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0 (± 2g)

Position	1		2		3		4		5		6	
Diagram									Top / Bottom		Bottom / Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	1024	64	0	0	3072	192	0	0	0	0
Y (counts)	1024	64	0	0	3072	192	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	1024	64	3072	192
X-Polarity	**0**		**+**		**0**		**-**		**0**		**0**	
Y-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



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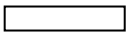
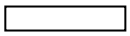
Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

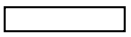
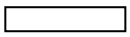
GSEL1=0, GSEL0=1 (± 4g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	512	32	0	0	3584	224	0	0	0	0
Y (counts)	512	32	0	0	3584	224	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	512	32	3584	224
X-Polarity	**0**		**+**		**0**		**-**		**0**		**0**	
Y-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=0 (± 8g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	256	16	0	0	3840	240	0	0	0	0
Y (counts)	256	16	0	0	3840	240	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	256	16	3840	240
X-Polarity	**0**		**+**		**0**		**-**		**0**		**0**	
Y-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

Earth's Surface

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KXTF9 Digital Interface

The Kionix KXTF9 digital accelerometer has the ability to communicate on the I²C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 6 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 6. Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KXTF9 has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KXTF9 always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are high.

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The Slave Address associated with the KXTF9 is 0001111.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To

conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^2C bus is now free.

Writing to a KXTF9 8-bit Register

Upon power up, the Master must write to the KXTF9's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KXTF9 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KXTF9 to which 8-bit register the Master will be writing the data. Since this is I^2C mode, the MSB of the RA command should always be zero (0). The KXTF9 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KXTF9 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KXTF9 is now stored in the appropriate register. The KXTF9 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

Reading from a KXTF9 8-bit Register

When reading data from a KXTF9 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KXTF9 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KXTF9 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KXTF9 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KXTF9 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page.

If a receiver cannot transmit or receive another complete byte of data until it has performed some other function, it can hold SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases SCL.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I²C bus and how the Master and Slave interact during these transfers. Table 7 defines the I²C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 7. I²C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

KXTF9 Embedded Registers

The KXTF9 has 39 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. Table 8 below provides a listing of the accessible 8-bit registers and their addresses.

Register Name	Type Read/Write	I2C Read/Write Address Hex	Binary
XOUT_HPF_L	R	0x00	0000 0000
XOUT_HPF_H	R	0x01	0000 0001
YOUT_HPF_L	R	0x02	0000 0010
YOUT_HPF_H	R	0x03	0000 0011
ZOUT_HPF_L	R	0x04	0001 0100
ZOUT_HPF_H	R	0x05	0001 0101
XOUT_L	R	0x06	0000 0110
XOUT_H	R	0x07	0000 0111
YOUT_L	R	0x08	0000 1000
YOUT_H	R	0x09	0000 1001
ZOUT_L	R	0x0A	0001 1010
ZOUT_H	R	0x0B	0001 1011
DCST_RESP	R	0x0C	0000 1100
Not Used	-	0x0D	0000 1101
Not Used	-	0x0E	0000 1110
WHO_AM_I	R	0x0F	0000 1111
TILT_POS_CUR	R	0x10	0001 0000
TILT_POS_PRE	R	0x11	0001 0001
Kionix Reserved	-	0x12	0001 0010
Kionix Reserved	-	0x13	0001 0011
Kionix Reserved	-	0x14	0001 0100
INT_SRC_REG1	R	0x15	0001 0101
INT_SRC_REG2	R	0x16	0001 0110
Not Used	-	0x17	0001 0111
STATUS_REG	R	0x18	0001 1000
Not Used	-	0x19	0001 1001
INT_REL	R	0x1A	0001 1010
CTRL_REG1*	R/W	0x1B	0001 1011
CTRL_REG2*	R/W	0x1C	0001 1100
CTRL_REG3*	R/W	0x1D	0001 1101
INT_CTRL_REG1*	R/W	0x1E	0001 1110
INT_CTRL_REG2*	R/W	0x1F	0001 1111

INT_CTRL_REG3*	R/W	0x20	0010 0000
DATA_CTRL_REG*	R/W	0x21	0010 0001
Not Used	-	0x22 – 0x27	-
TILT_TIMER*	R/W	0x28	0010 1000
WUF_TIMER*	R/W	0x29	0010 1001
Not Used	-	0x2A	0010 1010
TDT_TIMER*	R/W	0x2B	0010 1011
TDT_H_THRESH*	R/W	0x2C	0010 1100
TDT_L_THRESH*	R/W	0x2D	0010 1101
TDT_TAP_TIMER*	R/W	0x2E	0010 1110
TDT_TOTAL_TIMER*	R/W	0x2F	0010 1111
TDT_LATENCY_TIMER*	R/W	0x30	0011 0000
TDT_WINDOW_TIMER*	R/W	0x31	0011 0001
Reserved	-	0x32 – 0x39	-
SELF_TEST	R/W	0x3A	0011 1010
Reserved	-	0x3B – 0x59	-
WUF_THRESH*	R/W	0x5A	0101 1010
Reserved	-	0x5B	0101 1011
TILT_ANGLE*	R/W	0x5C	0101 1100
Reserved	-	0x5D – 0x5E	-
HYST_SET*	R/W	0x5F	0101 1111

* Note: When changing the contents of these registers, the PC1 bit in CTRL_REG1 must first be set to “0”.

Table 8. KXTF9 Register Map

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KXTF9 Register Descriptions

Accelerometer Outputs

These registers contain up to 12-bits of valid acceleration data for each axis depending on the setting of the RES bit in CTRL_REG1, where the acceleration outputs are represented in 12-bit valid data when RES = '1' and 8-bit valid data when RES = '0'. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Figure 9 below.

12-bit Data	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111 1111	+1.999g	+3.998g	+7.996g
0111 1111 1110	+1.998g	+3.996g	+7.992g
…	…	…	…
0000 0000 0001	+0.001g	+0.002g	+0.004g
0000 0000 0000	0.000g	0.000g	0.000g
1111 1111 1111	-0.001g	-0.002g	-0.004g
…	…	…	…
1000 0000 0001	-1.999g	-3.998g	-7.996g
1000 0000 0000	-2.000g	-4.000g	-8.000g

8-bit Data	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111	+1.984g	+3.968g	+7.936g
0111 1110	+1.968g	+3.936g	+7.872g
…	…	…	…
0000 0001	+0.016g	+0.032g	+0.064g
0000 0000	0.000g	0.000g	0.000g
1111 1111	-0.016g	-0.032g	-0.064g
…	…	…	…
1000 0001	-1.984g	-3.968g	-7.936g
1000 0000	-2.000g	-4.000g	-8.000g

Figure 9. Acceleration (g) Calculation

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XOUT_HPF_L

X-axis high-pass filtered accelerometer output least significant byte

R	R	R	R	R	R	R	R
XOUTD3	XOUTD2	XOUTD1	XOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x00h

XOUT_HPF_H

X-axis high-pass filtered accelerometer output most significant byte

R	R	R	R	R	R	R	R
XOUTD11	XOUTD10	XOUTD9	XOUTD8	XOUTD7	XOUTD6	XOUTD5	XOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x01h

YOUT_HPF_L

Y-axis high-pass filtered accelerometer output least significant byte

R	R	R	R	R	R	R	R
YOUTD3	YOUTD2	YOUTD1	YOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x02h

YOUT_HPF_H

Y-axis high-pass filtered accelerometer output most significant byte

R	R	R	R	R	R	R	R
YOUTD11	YOUTD10	YOUTD9	YOUTD8	YOUTD7	YOUTD6	YOUTD5	YOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x03h

ZOUT_HPF_L

Z-axis high-pass filtered accelerometer output least significant byte

R	R	R	R	R	R	R	R
ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I2C Address: 0x04h

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ZOUT_HPF_H

Z-axis high-pass filtered accelerometer output most significant byte

R	R	R	R	R	R	R	R
ZOUTD11	ZOUTD10	ZOUTD9	ZOUTD8	ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x05h

XOUT_L

X-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
XOUTD3	XOUTD2	XOUTD1	XOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x06h

XOUT_H

X-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
XOUTD11	XOUTD10	XOUTD9	XOUTD8	XOUTD7	XOUTD6	XOUTD5	XOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x07h

YOUT_L

Y-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
YOUTD3	YOUTD2	YOUTD1	YOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x08h

YOUT_H

Y-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
YOUTD11	YOUTD10	YOUTD9	YOUTD8	YOUTD7	YOUTD6	YOUTD5	YOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x09h

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ZOUT_L

Z-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I2C Address: 0x0Ah

ZOUT_H

Z-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
ZOUTD11	ZOUTD10	ZOUTD9	ZOUTD8	ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x0Bh

DCST_RESP

This register can be used to verify proper integrated circuit functionality. It always has a byte value of 0x55h unless the DCST bit in CTRL_REG3 is set. At that point this value is set to 0xAAh. The byte value is returned to 0x55h after reading this register.

R	R	R	R	R	R	R	R	
DCSTR7	DCSTR6	DCSTR5	DCSTR4	DCSTR3	DCSTR2	DCSTR1	DCSTR0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01010101

I^2C Address: 0x0Ch

WHO_AM_I

This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is 0x01h.

R	R	R	R	R	R	R	R	
WIA7	WIA6	WIA5	WIA4	WIA3	WIA2	WIA1	WIA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000001

I^2C Address: 0x0Fh

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Tilt Position Registers

These two registers report previous and current position data that is updated at the user-defined ODR frequency and is protected during register read. Table 9 describes the reported position for each bit value.

TILT_POS_CUR

Current tilt position register

R	R	R	R	R	R	R	R	Reset Value
0	0	LE	RI	DO	UP	FD	FU	00100000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x10h

TILT_POS_PRE

Previous tilt position register

R	R	R	R	R	R	R	R	Reset Value
0	0	LE	RI	DO	UP	FD	FU	00100000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x11h

Bit	Description
LE	Left State (X-)
RI	Right State (X+)
DO	Down State (Y-)
UP	Up State (Y+)
FD	Face-Down State (Z-)
FU	Face-Up State (Z+)

Table 9. KXTF9 Tilt Position

Interrupt Source Registers

These two registers report function state changes. This data is updated when a new state change or event occurs and each applications result is latched until the interrupt release register is read. The motion interrupt bit WUFS can be configured to report data in an unlatched manner via the interrupt control registers.

INT_SRC_REG1

This register reports which axis and direction detected a single or double tap event, per Table 10.

R	R	R	R	R	R	R	R
0	0	TLE	TRI	TDO	TUP	TFD	TFU
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x15h

Bit	Description
TLE	X Negative (X-) Reported
TRI	X Positive (X+) Reported
TDO	Y Negative (Y-) Reported
TUP	Y Positive (Y+) Reported
TFD	Z Negative (Z-) Reported
TFU	Z Positive (Z+) Reported

Table 10. KXTF9 Directional Tap™ Reporting

INT_SRC_REG2

This register reports which function caused an interrupt. Reading from the interrupt release register will clear the entire contents of this register.

R	R	R	R	R	R	R	R
0	0	0	DRDY	TDTS1	TDTS0	WUFS	TPS
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x16h

DRDY *indicates that new acceleration data is available. This bit is cleared when acceleration data is read or the interrupt release register is read.*
DRDY = 0 – new acceleration data not available
DRDY = 1 – new acceleration data available

TDTS1, TDTS0 *indicates whether a single or double-tap event was detected per Table 11.*

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TDTS1	TDTS0	Event
0	0	No Tap
0	1	Single Tap
1	0	Double Tap
1	1	DNE

Table 11. Directional Tap™ Event Description

TPS *reflects the status of the tilt position function.*
TPS = 0 – tilt position state has not changed
TPS = 1 – tilt position state has changed

STATUS_REG

This register reports the status of the interrupt.

R	R	R	R	R	R	R	R
0	0	0	INT	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x18h

INT *reports the combined interrupt information of all enabled functions. This bit is released to 0 when the interrupt source latch register (1Ah) is read.*
INT = 0 – no interrupt event
INT = 1 – interrupt event has occurred

INT_REL

Latched interrupt source information (INT_SRC_REG1 and INT_SRC_REG2), the status register, and the physical interrupt pin (7) are cleared when reading this register.

R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

I^2C Address: 0x1Ah

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CTRL_REG1

Read/write control register that controls the main feature set.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PC1	RES	DRDYE	GSEL1	GSEL0	TDTE	WUFE	TPE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x1Bh

PC1 *controls the operating mode of the KXTF9.*
PC1 = 0 - stand-by mode
PC1 = 1 – operating mode

RES *determines the performance mode of the KXTF9. Note that to change the value of this bit, the PC1 bit must first be set to "0".*
RES = 0 – low current, 8-bit valid
RES = 1- high current, 12-bit valid

DRDYE *enables the reporting of the availability of new acceleration data on the interrupt. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

DRDYE = 0 – availability of new acceleration data not reflected on interrupt pin (7)
DRDYE = 1- availability of new acceleration data reflected on interrupt pin (7)

GSEL1, GSEL0 *selects the acceleration range of the accelerometer outputs per Table 12. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

GSEL1	GSEL0	Range
0	0	+/-2g
0	1	+/-4g
1	0	+/-8g
1	1	NA

Table 12. Selected Acceleration Range

TDTE *enables the Directional Tap™ function that will detect single and double tap events. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

TDTE = 0 – disable
TDTE = 1- enable

WUFE *enables the Wake Up (motion detect) function that will detect a general motion event. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

WUFE = 0 – disable
WUFE = 1- enable

TPE *enables the Tilt Position function that will detect changes in device orientation. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

TPE = 0 – disable
TPE = 1- enable

CTRL_REG2

Read/write control register that controls tilt position state enabling. Per Table 13, if a state's bit is set to one (1), a transition into the corresponding orientation state will generate an interrupt. If it is set to zero (0), a transition into the corresponding orientation state will not generate an interrupt. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
0	0	LEM	RIM	DOM	UPM	FDM	FUM	00111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x1Ch

Bit	Description
LEM	Left State
RIM	Right State
DOM	Down State
UPM	Up State
FDM	Face-Down State
FUM	Face-Up State

Table 13. Tilt Position State Enabling

CTRL_REG3

Read/write control register that provides more feature set control. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SRST	OTPA	OTPB	DCST	OTDTA	OTDTB	OWUFA	OWUFB	01001101
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x1Dh

SRST *initiates software reset, which performs the RAM reboot routine. This bit will remain 1 until the RAM reboot routine is finished.*
SRST = 0 – no action
SRST = 1 – start RAM reboot routine

OTPA, OTPB *sets the output data rate for the Tilt Position function per Table 14. The default Tilt Position ODR is 12.5Hz.*

OTPA	OTPB	Output Data Rate
0	0	1.6Hz
0	1	6.3Hz
1	0	12.5Hz
1	1	50Hz

Table 14. Tilt Position Function Output Data Rate

DCST *initiates the digital communication self-test function.*
DCST = 0 – no action
DCST = 1 – sets ST_RESP register to 0xAAh and when ST_RESP is read, sets this bit to 0 and sets ST_RESP to 0x55h

OTDTA, OTDTB *sets the output data rate for the Directional Tap™ function per Table 15. The default Directional Tap™ ODR is 400Hz.*

OTDTA	OTDTB	Output Data Rate
0	0	50Hz
0	1	100Hz
1	0	200Hz
1	1	400Hz

Table 15. Directional Tap™ Function Output Data Rate

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OWUFA, OWUFB *sets the output data rate for the general motion detection function and the high-pass filtered outputs per Table 16. The default Motion Wake Up ODR is 50Hz.*

OWUFA	OWUFB	Output Data Rate
0	0	25Hz
0	1	50Hz
1	0	100Hz
1	1	200Hz

Table 16. Motion Wake Up Function Output Data Rate

INT_CTRL_REG1

This register controls the settings for the physical interrupt pin (7). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
0	0	IEN	IEA	IEL	IEU	0	0	00010000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x1Eh

IEN *enables/disables the physical interrupt pin (7)*
IEN = 0 – physical interrupt pin (7) is disabled
IEN = 1 – physical interrupt pin (7) is enabled

IEA *sets the polarity of the physical interrupt pin (7)*
IEA = 0 – polarity of the physical interrupt pin (7) is active low
IEA = 1 – polarity of the physical interrupt pin (7) is active high

IEL *sets the response of the physical interrupt pin (7)*
IEL = 0 – the physical interrupt pin (7) latches until it is cleared by reading INT_REL
IEL = 1 – the physical interrupt pin (7) will transmit one pulse with a period of 0.05ms

IEU *sets an alternate unlatched response for the physical interrupt pin (7) when the motion interrupt feature (WUF) only is enabled.*
IEU = 0 – the physical interrupt pin (7) latches or pulses per the IEL bit until it is cleared by reading INT_REL
IEU = 1 – the physical interrupt pin (7) will follow an unlatched response if the motion interrupt feature is enabled

INT_CTRL_REG2

This register controls motion detection axis enabling. Per Table 17, if an axis' bit is set to one (1), a motion on that axis will generate an interrupt. If it is set to zero (0), a motion on that axis will not generate an interrupt. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
XBW	YBW	ZBW	0	0	0	0	0	11100000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x1Fh

Bit	Description
XBW	X-Axis Motion
YBW	Y-Axis Motion
ZBW	Z-Axis Motion

Table 17. Motion Detection Axis Enabling

INT_CTRL_REG3

This register controls the tap detection direction axis enabling. Per Table 18, if a direction's bit is set to one (1), a single or double tap in that direction will generate an interrupt. If it is set to zero (0), a single or double tap in that direction will not generate an interrupt. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
0	0	TLEM	TRIM	TDOM	TUPM	TFDM	TFUM	00111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x20h

Bit	Description
TLEM	X Negative (X-)
TRIM	X Positive (X+)
TDOM	Y Negative (Y-)
TUPM	Y Positive (Y+)
TFDM	Z Negative (Z-)
TFUM	Z Positive (Z+)

Table 18. Directional Tap™ Axis Mask

DATA_CTRL_REG

Read/write control register that configures the acceleration outputs. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
0	0	HPFROA	HPROB	0	OSAA	OSAB	OSAC	00000010
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x21h

HPFROA, HPFROB *sets the roll-off frequency for the first-order high-pass filter in conjunction with the output data rate (OWUFA, OWUFB) that is chosen for the HPF acceleration outputs that are used in the Motion Wake Up (WUF) application per Table 19. Note that this roll-off frequency is also applied to the X, Y and Z high-pass filtered outputs.*

High-Pass Filter Configuration			
HPFROA	**HPFROB**	**Beta**	**HPF Roll-Off (Hz)**
0	0	7/8	ODR / 50
0	1	15/16	ODR / 100
1	0	31/32	ODR / 200
1	1	63/64	ODR / 400

Table 19. High-Pass Filter Roll-Off Frequency

OSAA, OSAB, OSAC *sets the output data rate (ODR) for the low-pass filtered acceleration outputs per Table 20.*

OSAA	OSAB	OSAC	Output Data Rate	LPF Roll-Off
0	0	1	25Hz	12.5Hz
0	1	0	50Hz	25Hz
0	1	1	100Hz	50Hz
1	0	0	200Hz	100Hz
1	0	1	400Hz	200Hz
1	1	0	800Hz	400Hz
1	1	1	Does Not Exist	Does Not Exist

Table 20. LPF Acceleration Output Data Rate (ODR)

TILT_TIMER

This register is the initial count register for the tilt position state timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 14. A new state must be valid as many measurement periods before the change is accepted. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TSC7	TSC6	TSC5	TSC4	TSC3	TSC2	TSC1	TSC0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x28h

WUF_TIMER

This register is the initial count register for the motion detection timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 16. A new state must be valid as many measurement periods before the change is accepted. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
WUFC7	WUFC6	WUFC5	WUFC4	WUFC3	WUFC2	WUFC1	WUFC0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x29h

TDT_TIMER

This register contains counter information for the detection of a double tap event. Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 15. TDT_TIMER represents the minimum time separation between the first tap and the second tap in a double tap event. The Kionix recommended default value is 0.3 seconds (0x78h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TDTC7	TDTC6	TDTC5	TDTC4	TDTC3	TDTC2	TDTC1	TDTC0	01111000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x2Bh

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TDT_H_THRESH

This register represents the 9-bit jerk high threshold to determine if a tap is detected. The Performance Index (PI) is the jerk signal that is expected to be less than this threshold, but greater than the TDT_L_THRESH threshold during single and double tap events. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0". The Kionix recommended default value is 182 (0xB6h) and the Performance Index is calculated as:

$$X' = X(\text{current}) - X(\text{previous})$$
$$Y' = Y(\text{current}) - Y(\text{previous})$$
$$Z' = Z(\text{current}) - Z(\text{previous})$$

$$PI = |X'| + |Y'| + |Z'|$$

Equation 1. Performance Index

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TTH8	TTH7	TTH6	TTH5	TTH4	TTH3	TTH2	TTH1	10110110
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x2Ch

TDT_L_THRESH

This register represents the 7-bit jerk low threshold to determine if a tap is detected. The Performance Index (PI) is the jerk signal that is expected to be greater than this threshold and less than the TDT_H_THRESH threshold during single and double tap events. This register also contains the LSB of the TDT_H_THRESH threshold. The Kionix recommended default value is 26 (0x1Ah). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TTH0	TTL6	TTL5	TTL4	TTL3	TTL2	TTL1	TTL0	00011010
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x2Dh

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TDT_TAP_TIMER

This register contains counter information for the detection of any tap event. Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 17. In order to ensure that only tap events are detected, these time limits are used. A tap event must be above the performance index threshold (TDT_THRESH) for at least the low limit (FTDL0 – FTDL2) and no more than the high limit (FTDH0 – FTDH4). The Kionix recommended default value for the high limit is 0.05 seconds and for the low limit is 0.005 seconds (0xA2h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
FTDH4	FTDH3	FTDH2	FTDH1	FTDH0	FTDL2	FTDL1	FTDL0	10100010
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x2Eh

TDT_TOTAL_TIMER

This register contains counter information for the detection of a double tap event. Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 17. In order to ensure that only tap events are detected, this time limit is used. This register sets the total amount of time that the two taps in a double tap event can be above the PI threshold (TDT_L_THRESH). The Kionix recommended default value for TDT_TOTAL_TIMER is 0.09 seconds (0x24h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
STD7	STD6	STD5	STD4	STD3	STD2	STD1	STD0	00100100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x2Fh

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TDT_LATENCY_TIMER

This register contains counter information for the detection of a tap event. Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 17. In order to ensure that only tap events are detected, this time limit is used. This register sets the total amount of time that the tap algorithm will count samples that are above the PI threshold (TDT_L_THRESH) during a potential tap event. It is used during both single and double tap events. However, reporting of single taps on the physical interrupt pin (7) will occur at the end of the TDT_WINDOW_TIMER. The Kionix recommended default value for TDT_LATENCY_TIMER is 0.1 seconds (0x28h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TLT7	TLT6	TLT5	TLT4	TLT3	TLT2	TLT1	TLT0	00101000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x30h

TDT_WINDOW_TIMER

This register contains counter information for the detection of single and double taps. Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 17. It defines the time window for the entire tap event, single or double, to occur. Reporting of single taps on the physical interrupt pin (7) will occur at the end of this tap window. The Kionix recommended default value for TDT_WINDOW_TIMER is 0.4 seconds (0xA0h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TWS7	TWS6	TWS5	TWS4	TWS3	TWS2	TWS1	TWS0	10100000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x31h

SELF_TEST

When 0xCA is written to this register, the MEMS self-test function is enabled. Electrostatic-actuation of the accelerometer, results in a DC shift of the X, Y and Z axis outputs. Writing 0x00 to this register will return the accelerometer to normal operation.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
1	1	0	0	1	0	1	0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x3Ah

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WUF_THRESH

This register sets the acceleration threshold, WUF Threshold that is used to detect a general motion input. The KXTF9 will ship from the factory with WUF_THRESH set to a change in acceleration of 0.5g. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
WUFTH7	WUFTH6	WUFTH5	WUFTH4	WUFTH3	WUFTH2	WUFTH1	WUFTH0	00001000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x5Ah

TILT_ANGLE

This register sets the tilt angle that is used to detect the transition from Face-up/Face-down states to Screen Rotation states. The KXTF9 ships from the factory with tilt angle set to a low threshold of 26° from horizontal. A different default tilt angle can be requested from the factory. Note that the minimum suggested tilt angle is 10°. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	00001100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x5Ch

HYST_SET

This register sets the Hysteresis that is placed in between the Screen Rotation states. The KXTF9 ships from the factory with HYST_SET set to +/-15° of hysteresis. A different default hysteresis can be requested from the factory. Note that when writing a new value to this register the current values of RES0, RES1, RES2 and RES3 must be preserved. These values are set at the factory and must not change. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
RES2	RES1	RES0	HYST4	HYST3	HYST2	HYST1	HYST0	---10100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

I^2C Address: 0x5Fh

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KXTF9 Embedded Applications

Orientation Detection Feature

The orientation detection feature of the KXTF9 will report changes in face up, face down, +/- vertical and +/- horizontal orientation. This intelligent embedded algorithm considers very important factors that provide accurate orientation detection from low cost tri-axis accelerometers. Factors such as: hysteresis, device orientation angle and delay time are described below as these techniques are utilized inside the KXTF9.

Hysteresis

A 45° tilt angle threshold seems like a good choice because it is halfway between 0° and 90°. However, a problem arises when the user holds the device near 45°. Slight vibrations, noise and inherent sensor error will cause the acceleration to go above and below the threshold rapidly and randomly, so the screen will quickly flip back and forth between the 0° and the 90° orientations. This problem is avoided in the KXTF9 by choosing a 30° threshold angle. With a 30° threshold, the screen will not rotate from 0° to 90° until the device is tilted to 60° (30° from 90°). To rotate back to 0°, the user must tilt back to 30°, thus avoiding the screen flipping problem. This example essentially applies +/- 15° of hysteresis in between the four screen rotation states. Table 21 shows the acceleration limits implemented for ϕ_T =30°.

Orientation	X Acceleration (g)	Y Acceleration (g)
0°/360°	$-0.5 < a_x < 0.5$	$a_y > 0.866$
90°	$a_x > 0.866$	$-0.5 < a_y < 0.5$
180°	$-0.5 < a_x < 0.5$	$a_y < -0.866$
270°	$a_x < -0.866$	$-0.5 < a_y < 0.5$

Table 21. Acceleration at the four orientations with +/- 15° of hysteresis

The KXTF9 allows the user to change the amount of hysteresis in between the four screen rotation states. By simply writing to the HYST_SET register, the user can adjust the amount of hysteresis up to +/- 45°. The plot in Figure 1 shows the typical amount of hysteresis applied for a given digital count value of HYST_SET.

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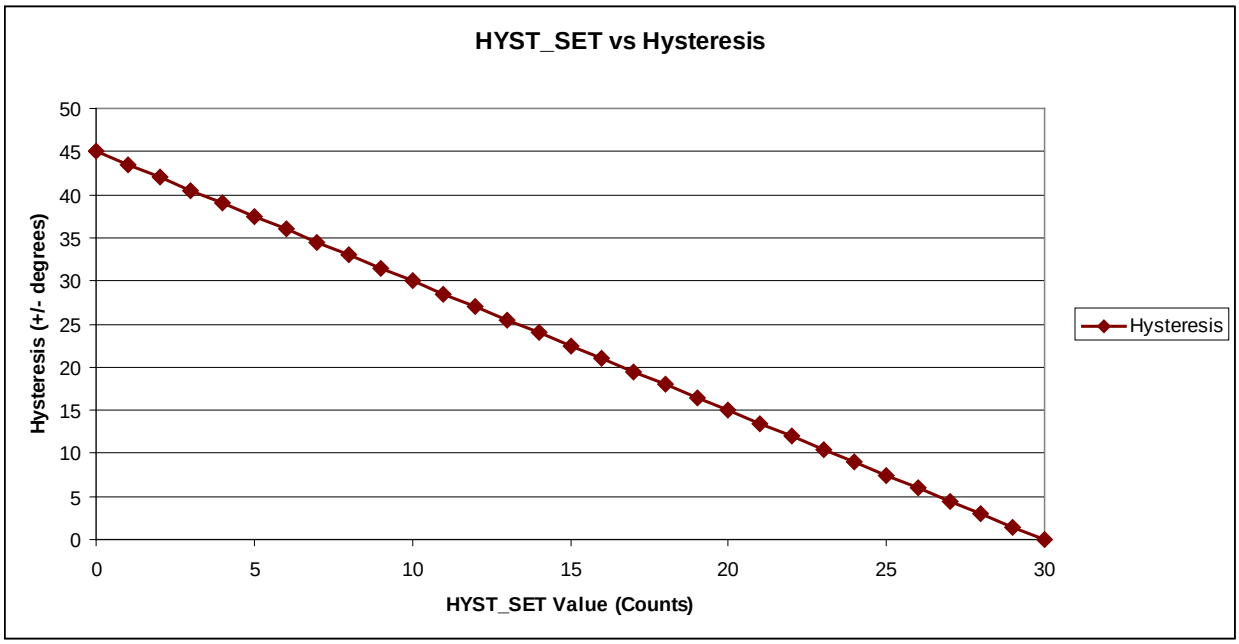

Figure 1. HYST_SET vs Hysteresis

Device Orientation Angle (aka Tilt Angle)

To ensure that horizontal and vertical device orientation changes are detected, even when it isn't in the ideal vertical orientation – where the angle θ in Figure 2 is 90°, the KXTF9 considers device orientation angle in its algorithm.

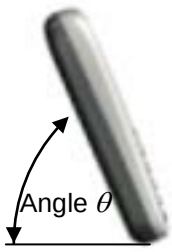

Figure 2. Device Orientation Angle

As the angle in Figure 2 is decreased, the maximum gravitational acceleration on the X-axis or Y-axis will also decrease. Therefore, when the angle becomes small enough, the user will not be able to make the screen orientation change. When the device orientation angle approaches 0° (device is flat on a desk or table), $a_x = a_y = 0g$, $a_z = +1g$, and there is no way to determine which way the screen should be oriented, the internal algorithm determines that the device is in either the face-up or face-down orientation, depending on the sign of the z-axis. The KXTF9 will only change the

screen orientation when the orientation angle is above the factory-defaulted/user-defined threshold set in the TILT_ANGLE register. Equation 2 can be used to determine what value to write to the TILT_ANGLE register to set the device orientation angle.

$$\text{TILT\_ANGLE (counts)} = \sin\theta * (32 \text{ (counts/g)})$$

Equation 2. Tilt Angle Threshold

Tilt Timer

The 8-bit register, TILT_TIMER can be used to qualify changes in orientation. The KXTF9 does this by incrementing a counter with a size that is specified by the value in TILT_TIMER for each set of acceleration samples to verify that a change to a new orientation state is maintained. A user defined output data rate (ODR) determines the time period for each sample. Equation 3 shows how to calculate the TILT_TIMER register value for a desired delay time.

$$\text{TILT\_TIMER (counts)} = \text{Delay Time (sec)} \times \text{ODR (Hz)}$$

Equation 3. Tilt Position Delay Time

Motion Interrupt Feature Description

The Motion interrupt feature of the KXTF9 reports qualified high-pass filtered acceleration based on the Wake Up (WUF) threshold. If the high-pass filtered acceleration on any axis is greater than the user-defined wake up threshold (WUF_THRESH), the device has transitioned from an inactive state to an active state. When configured in the unlatched mode, the KXTF9 will report when the motion event finished and the device has returned to an inactive state. Equation 4 shows how to calculate the WUF_THRESH register value for a desired wake up threshold.

$$\text{WUF\_THRESH (counts)} = \text{Wake Up Threshold (g)} \times 16 \text{ (counts/g)}$$

Equation 4. Wake Up Threshold

A WUF (WUF_TIMER) 8-bit raw unsigned value represents a counter that permits the user to qualify each active/inactive state change. Note that each WUF Timer count qualifies 1 (one) user-defined ODR period (OWUF). Equation 5 shows how to calculate the WUF_TIMER register value for a desired wake up delay time.

$$\text{WUF\_TIMER (counts)} = \text{Wake Up Delay Time (sec)} \times \text{OWUF (Hz)}$$

Equation 5. Wake Up Delay Time

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Figure 3 below shows the latched response of the motion detection algorithm with WUF Timer = 10 counts.

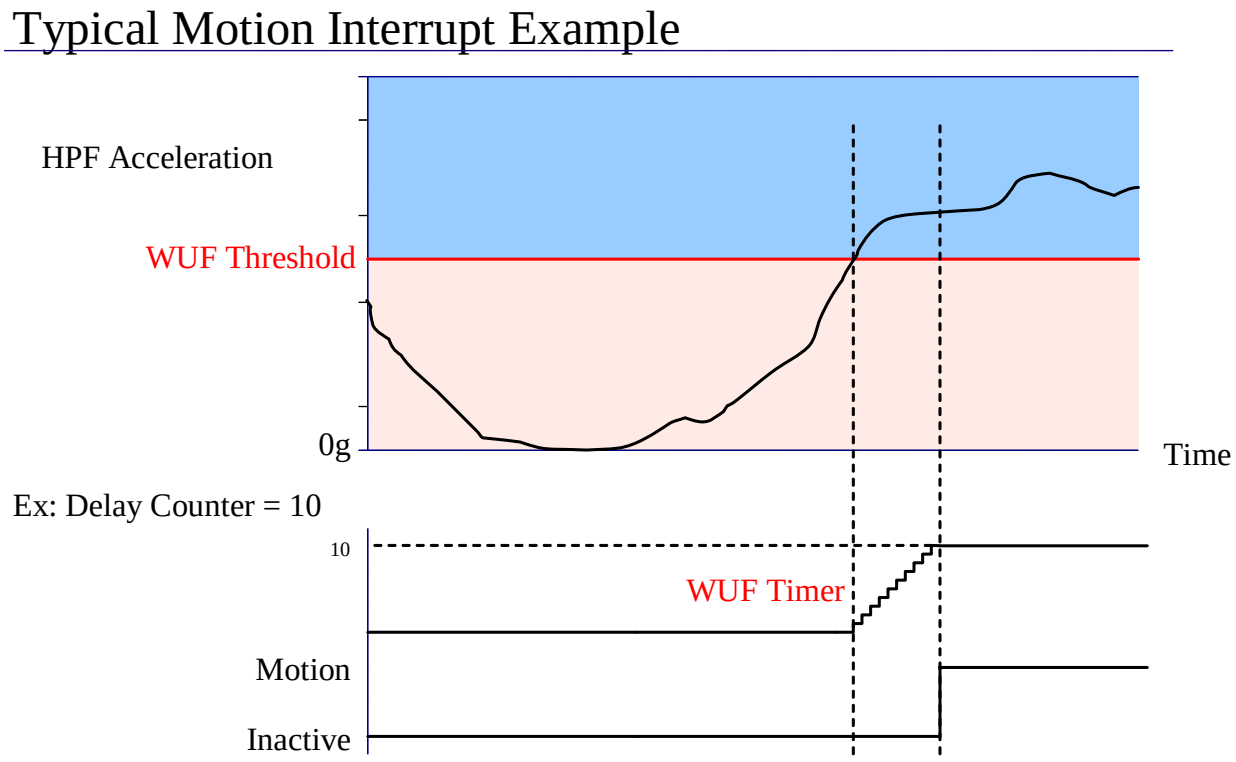

Figure 3. Latched Motion Interrupt Response

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Figure 4 below shows the unlatched response of the motion detection algorithm with WUF Timer = 10 counts.

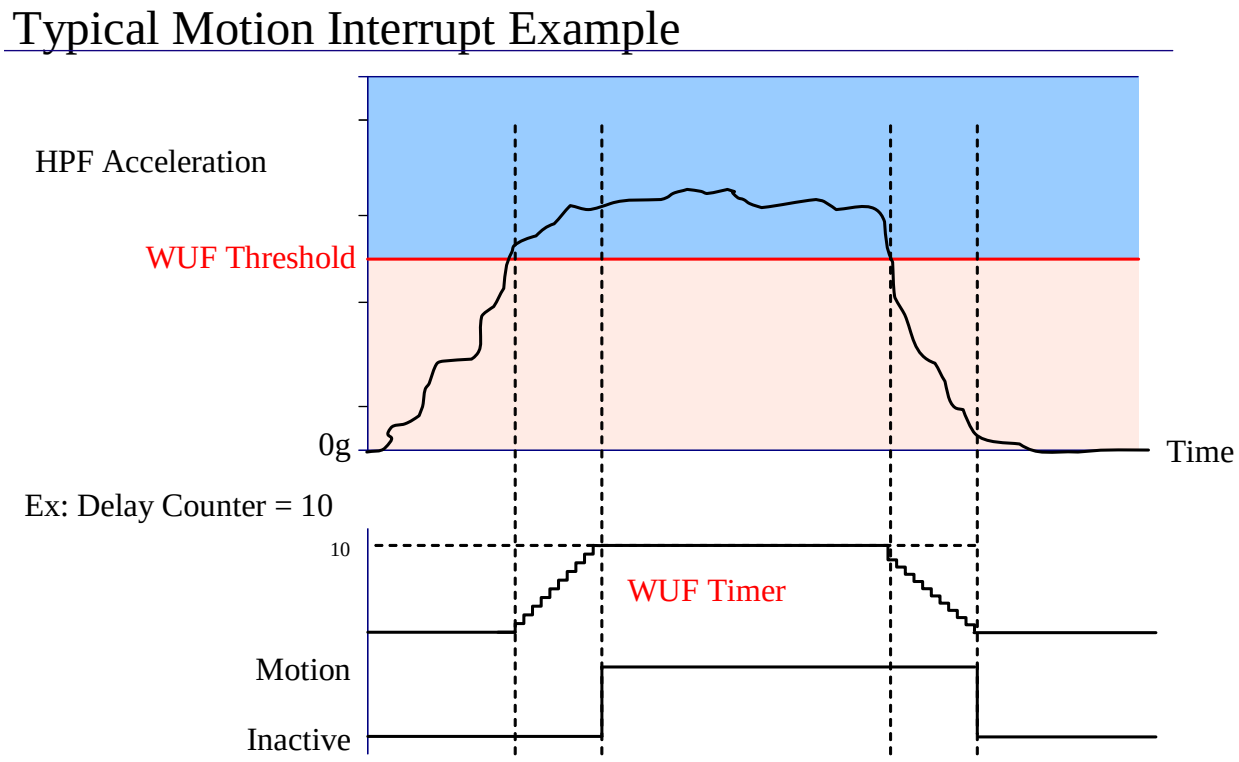

Figure 4. Unlatched Motion Interrupt Response

Directional Tap Detection Feature Description

The Directional Tap Detection feature of the KXTF9 recognizes single and double tap inputs and reports the acceleration axis and direction that each tap occurred. Eight performance parameters, as well as a user-selectable ODR are used to configure the KXTF9 for a desired tap detection response.

Performance Index

The Directional Tap™ detection algorithm uses low and high thresholds to help determine when a tap event has occurred. A tap event is detected when the previously described jerk summation exceeds the low threshold (TDT_L_THRESH) for more than the tap detection low limit, but less than the tap detection high limit as contained in TDT_TAP_TIMER. Samples that exceed the high limit (TDT_H_THRESH) will be ignored. Figure 5 shows an example of a single tap event meeting the performance index criteria.

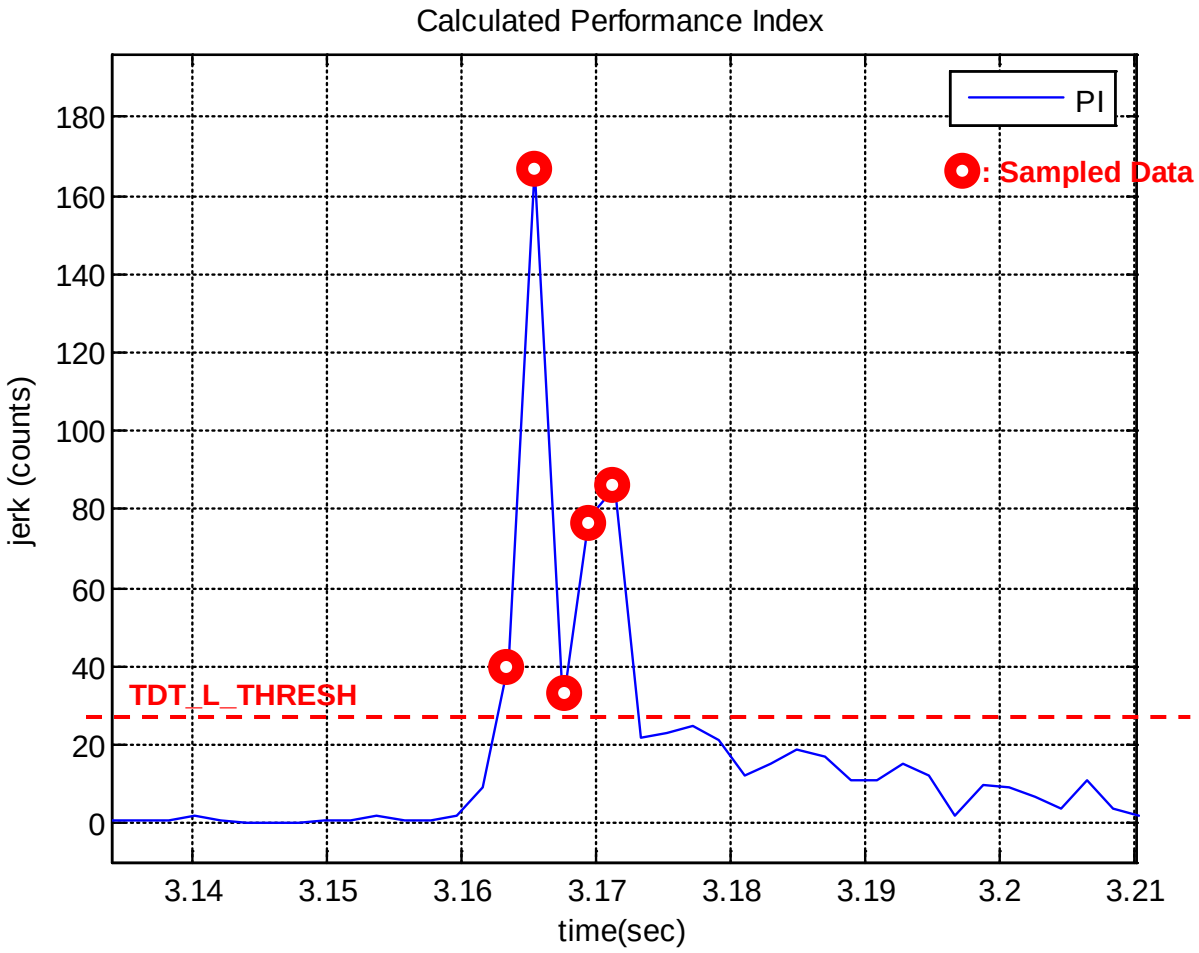

Figure 5. Jerk Summation vs Threshold

Single Tap Detection

The latency timer (TDT_LATENCY_TIMER) sets the time period that a tap event will only be characterized as a single tap. A second tap has to occur outside of the latency timer. If a second tap occurs inside the latency time, it will be ignored as it occurred too quickly. The single tap will be reported at the end of the TDT_WINDOW_TIMER. Figure 6 shows a single tap event meeting the PI, latency and window requirements.

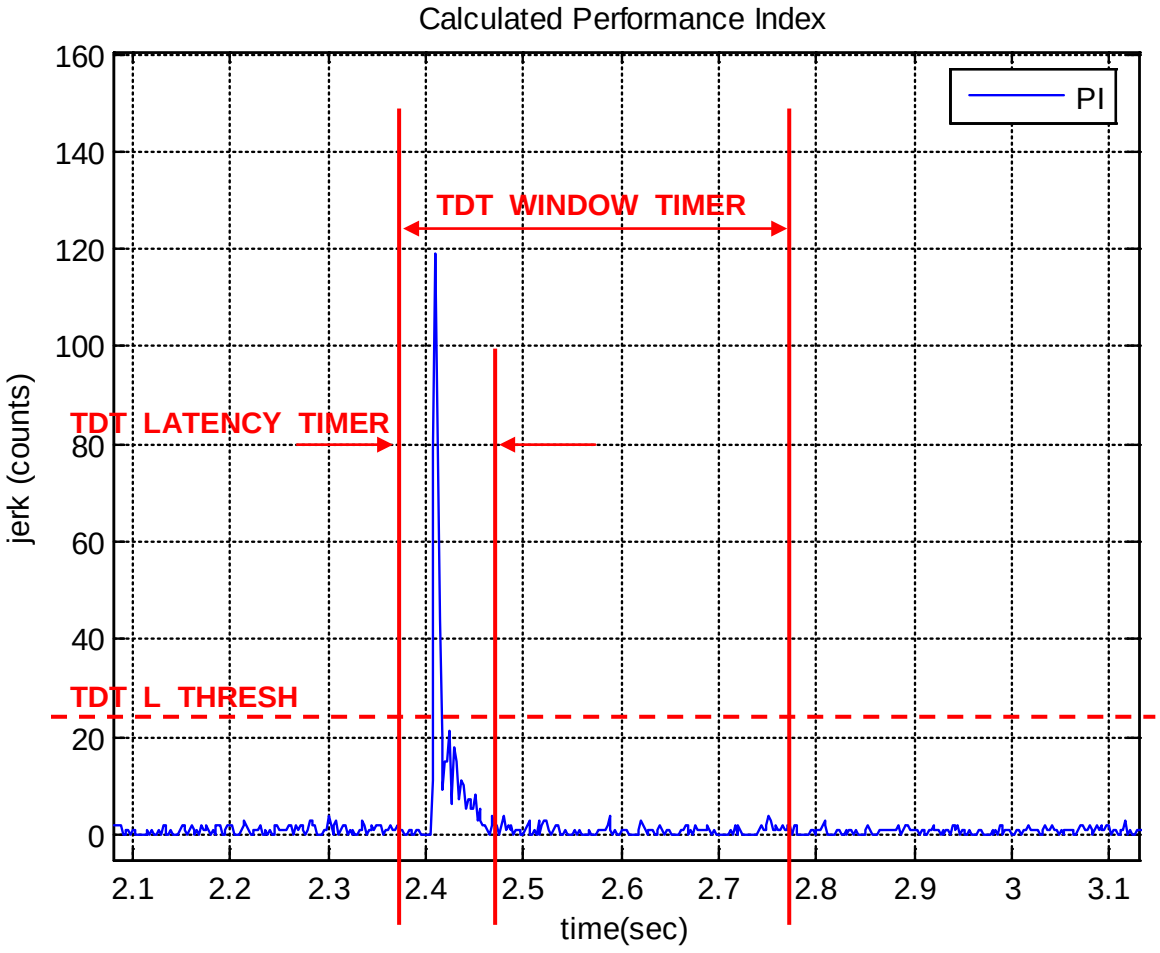

Figure 6. Single Directional Tap™ Timing

Double Tap Detection

An event can be characterized as a double tap only if the second tap crosses the performance index (TDT_L_THRESH) outside the TDT_TIMER. This means that the TDT_TIMER determines the minimum time separation that must exist between the two taps of a double tap event. Similar to the single tap, the second tap event must exceed the performance index for the time limit contained in TDT_TAP_TIMER. The double tap will be reported at the end of the second TDT_LATENCY_TIMER. Figure 7 shows a double tap event meeting the PI, latency and window requirements.

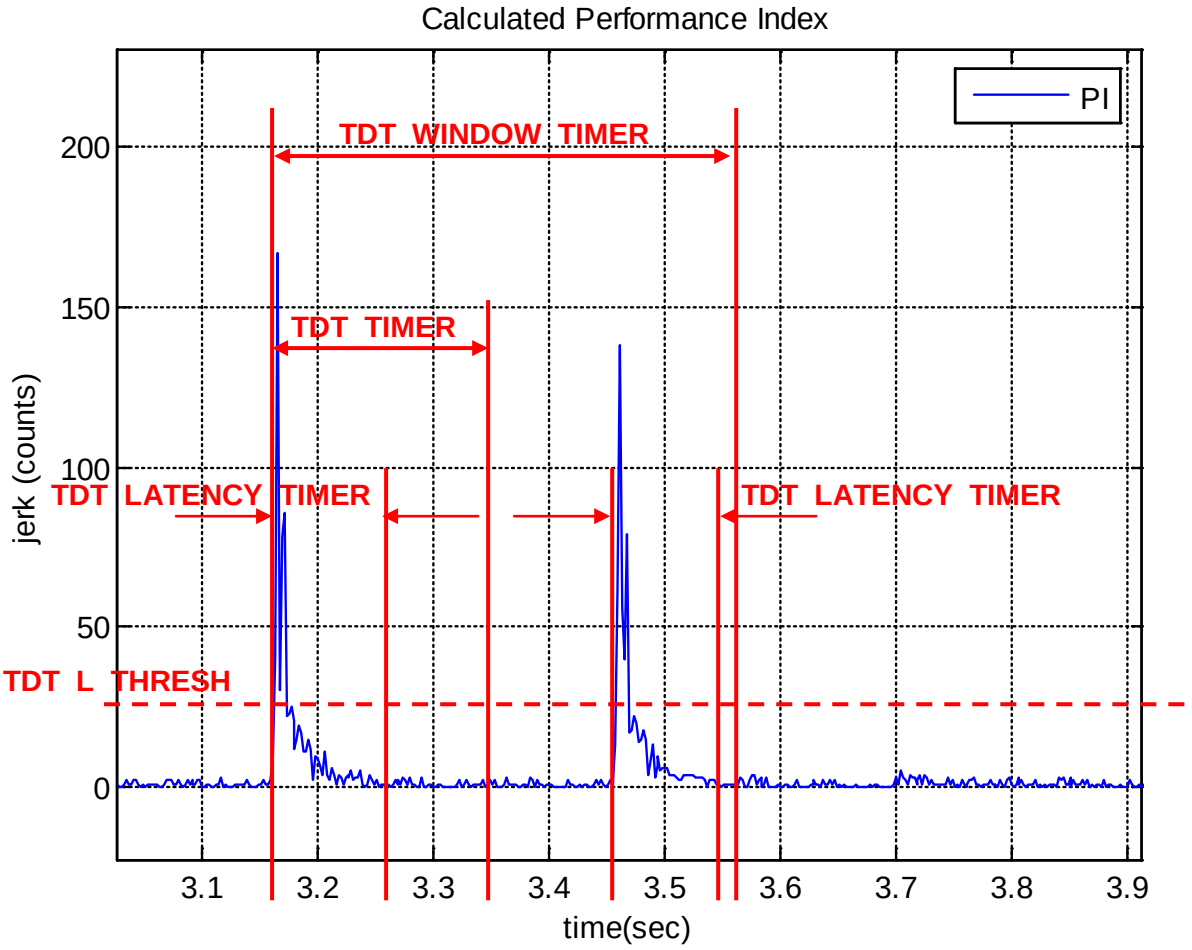

Figure 7. Double Directional Tap™ Timing

Kionix®	**± 2g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KXTF9-4100** **Rev. 3** **Jul-2010**

Revision History

REVISION	DESCRIPTION	DATE
1	Initial Release	18-Dec-2009
2	Corrected default register values and Table 15 references.	16-Mar-2010
3	Removed all references to 12.5 Hz ODR related to acceleration output registers and changed axes labels in Figures 3 and 4.	01-Jul-2010

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