MS3110 Universal Capacitive Readout™ IC

Description:

The Universal Capacitive Readout™ IC (MS3110) is a general purpose, ultra-low noise CMOS IC intended to support a variety of MEMS sensors that require a high resolution capacitive readout interface. The MS3110 requires only a single +5VDC supply and some decoupling components. No additional components are required.

MEMS sensors (such as accelerometers, rate sensors, and other sensors that can be modeled as variable capacitors) require a readout electronic interface that can sense small changes in capacitance. The MS3110 is capable of sensing capacitance changes down to 4.0 aF/rtHz, typical.

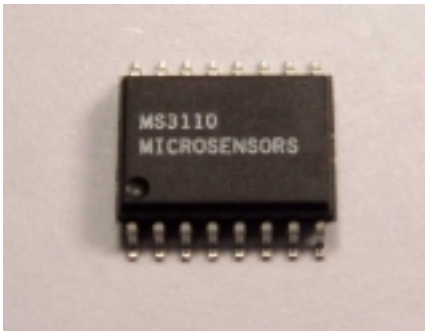
The MS3110 interfaces to either a differential capacitor pair or a single capacitive sensor. A high-level voltage output signal that is linear with full range of sense capacitance is provided. The MS3110 also includes an on-chip capacitive DAC (up to 10pF) for initial differential adjustments and/or for quasi-differential operation with a dummy capacitor. The MS3110 has provisions for trimming the gain and output offset. Bandwidth is also user programmable. An on-chip EEPROM is provided to store trim and program settings.

Features:

- Capacitance resolution: 4.0aF/rtHz
- Sensor modes: single variable or dual differential variable
- On-chip dummy capacitor for quasi-differential operation and initial adjustment
- Gain and DC offset trim
- Programmable bandwidth adjustment 0.5 to 8kHz (9 steps)
- 2.25VDC output for ADC reference/ratiometric operation
- Single supply of +5.0VDC
- On-chip EEPROM for storage of settings
- Available in die or 16-pin SOIC

Applications:

Pressure Sensors	*Accelerometers (low g)*
Velocity Sensors	*Displacement*
Rate Sensors	*Fluid Control*
Touch Sensors	*Flow Sensors*
Motion Sensors	*Gas Sensors*



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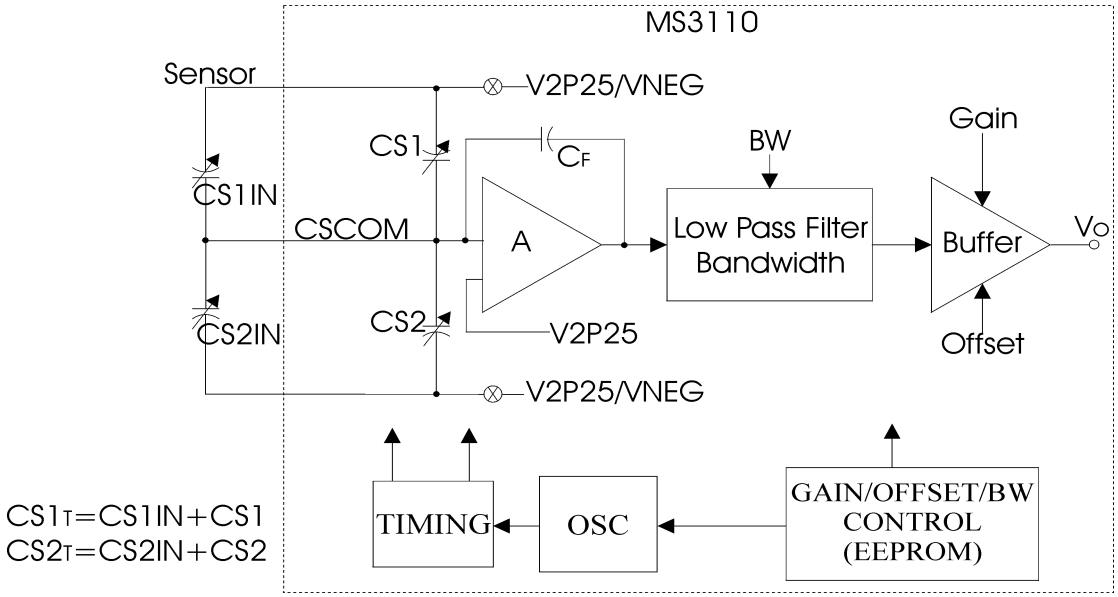
Functional Block Diagram:



Electrical Characteristics T=25 °C Unless Otherwise Spec.	Min	Typ	Max	Unit
Power Supply Voltage (+V)	4.75	5.00	5.25	V
Power Supply Current On +V		2.9	3.5	mA
Power Supply Ripple Requirement On +V			100	µV
Digital DM Inputs	- 0.5		V+	V
EEPROM Programming Voltage		16	18	V
All Other Inputs	- 0.5		V+	V
V2P25 (2.25V Reference) Trimmed	2.237		2.263	V
V2P25(2.25V Reference) Temperature Stability, Trimmed	-50		50	ppm/°C
Input Sense Capacitance($CS1_T$,$CS2_T$)	0.25		10	pF
Resolution/Input-referred Noise			4.0	aF/rtHz
CS1 Array Coarse Offset Trimmable Range, Nominal	0		9.7	pF
CS2 Array Coarse Offset Trimmable Range, Nominal	0		1.2	pF
CF Array Coarse Gain Trimmable Range, Nominal	0		19.44	pF
CF, CS1, and CS2 Trim steps	0.018	0.020	0.022	pF
Bandwidth Selection (9 steps)	500		8000	Hz
Bandwidth Tolerance	-25		+25	%
Output Voltage Range	0.5		4.0	V
Output Offset @ $CS2_T$-$CS1_T$=0, SOFF=0		2.25		V

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Electrical Characteristics	Min	Typ	Max	Unit
Output Offset @ CS1IN=CS2IN, SOFF=1		0.5		V
Output Fine Offset Trim Step		6		mV/step
Output Fine Gain Selectable Range	-15		+15	%
Output Fine Gain Trim Step		0.12		%
Output Load Resistance			10	KΩ
Output Load Capacitance		100	250	pF
Output Source and Sink Currents	3	5	9	mA
Operating Temperature Range (T_{op})	-40		+85	°C
ESD Rating			2.0	KV

THEORY OF OPERATION

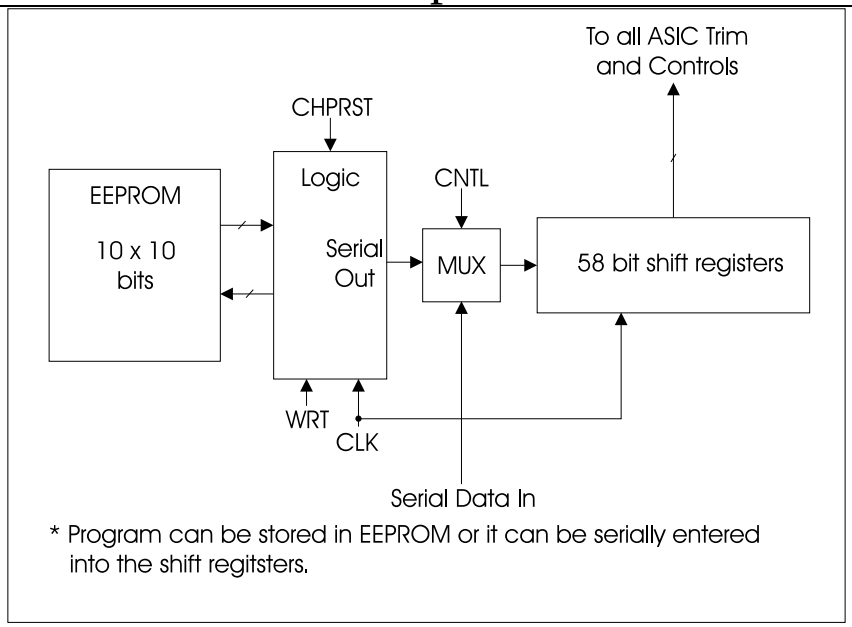
The MS3110 senses the change in capacitance between two capacitors and provides an output voltage proportional to that change. The capacitors to be sensed are an external balanced pair, CS1IN and CS2IN. The output voltage is a function of the change between the sensing capacitances $CS2_T$ and $CS1_T$ according to the following:

Transfer Function: $VO = GAIN * V2P25 * 1.14 * (CS2_T-CS1_T)/CF + VREF$

Where VO is the output Voltage
Gain = 2 or 4V/V nominal
V2P25 = 2.25 VDC nominal
$CS2_T$ = CS2IN + CS2
$CS1_T$ = CS1IN + CS1
CF is selected to optimize for input sense capacitance range, CF ≥ 1.5pF.
VREF can be set to 0.5V or 2.25V DC for $\Delta CS= CS2_T-CS1_T =0$. For 0.5V DC, the dynamic sensor capacity is constrained by $CS2_T$ greater or equal to $CS1_T$.

PROGRAMMING SPECIFICATIONS

To allow for such a large range of options, several program modes and trims are incorporated into the MS3110. The user has the option to store the settings into an on-chip EEPROM, which sends the data to the on-chip control registers, or program the control registers directly without memory storage. Both require serial input data, clock, and write signals. Programming the EEPROM requires a +16 VDC supply.



Nomenclature, definitions, and mapping into the EEPROM are provided below. Information regarding the ranges to which the bias and reference frequency should be set is also provided.

Programming Map and Modes

EEPROM Nomenclature and Description

The following programming bit descriptions and their programming map are presented below.

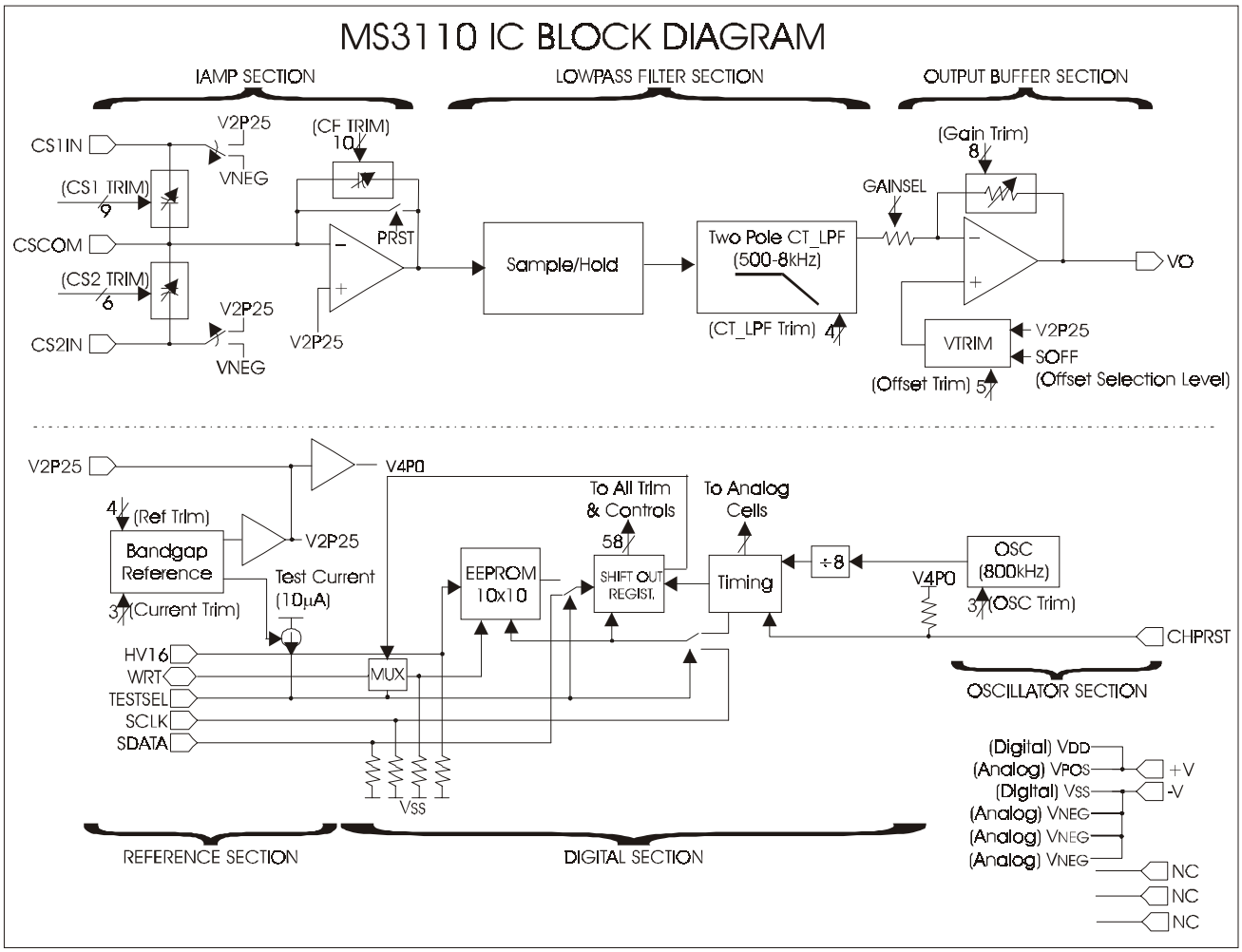
Nomenclature and Descriptions

Name	No. bits	Description
R[2:0]	3	Current Reference Trim Bits
T[3:0]	4	Voltage Reference Trim Bits
D[2:0]	3	Oscillator Trim Bits
B[7:0]	8	Output Buffer Gain Trim
OFF[4:0]	5	Output Buffer Offset Trim
SOFF	1	Output Buffer Output Offset Level Control
CSELCT[3:0]	4	Continuous-Time LPF Bandwidth Trim
GAINSEL	1	Output Buff Gain Selection
CF[9:0]	10	IAMP Feedback Capacitor Selection
CS1_[8:0]	9	IAMP Balance Capacitor Trim
CS2_[5:0]	6	IAMP Balance Trim Capacitor Selection

EEPROM Location Mapping:

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 9	R2	R1	R0	T3	T2	T1	T0	D0	D1	D2
ADDR 8		B0	B1	B2	B3	B4	B5	B6	B7	OFF0
ADDR 7	OFF1	OFF2	OFF3	OFF4	SOFF	CSELCT 3	CSELCT 2	CSELCT 1	CSELCT0	
ADDR 6		GAINSEL		CF9	CF8	CF7	CF6	CF5	CF4	CF3
ADDR 5	CF2	CF1	CF0	CS1_8	CS1_7	CS1_6	CS1_5	CS1_4	CS1_3	CS1_2
ADDR 4	CS1_1	CS1_0	CS2_0	CS2_1	CS2_2	CS2_3	CS2_4	CS2_5		
ADDR 3-0										

All other locations are unused.



Programming Truth Tables

Bias Control Registers

Two trims are included in the master bias circuitry, bandgap trim and current reference trim. The bandgap reference voltage can be trimmed to an optimum voltage with a trim range of +/-5.1%.

Since the 2.25VDC reference tracks the bandgap reference voltage, the user can monitor the variation through pin V2P25. The reference level can be trimmed in 20 mV steps. Thus variations of the 2.25V Reference can be trimmed over process. An abridged version of the truth table is included below.

V2P25 Reference Voltage Trim (~19mV /step)

T3	T2	T1	T0	Voltage Trim
0	0	0	0	+5.1%
1	0	0	0	Nominal
1	1	1	1	-5.1%

FOR ALL APPLICATIONS, the V2P25 voltage reference should be trimmed to 2.25V +\- 10mV.

The current reference can also be monitored and trimmed. The current monitor point is brought out to the TESTSEL pin that normally selects the mode of operation for the MS3110. It also serves to monitor the internal bias current of 10µA, typical when the pin is tied to logic low. The Current reference can be trimmed in 0.8µA steps. An abridged version of the truth table is included below.

Current Reference Trim (~0.8µA/step)

R2	R1	R0	Current Trim
0	0	0	+32%
1	1	0	Nominal
1	1	1	-32%

FOR ALL APPLICATIONS, the current reference should be trimmed to 10µA +\- 2µA.

Note that if an external pull-up resistor is placed on the TESTSEL pin of the MS3110 IC, the pull-up current must be factored into the total current, or the external pull-up resistor needs to be removed before the current measurement is performed.

Oscillator Control Registers

The MS3110 has the option to trim the oscillator over process. The truth table for trim is presented below.

Oscillator Trim

D2	D1	D0	Frequency Trim
0	0	0	Nominal
0	0	1	+15%
0	1	0	+24%
0	1	1	+33%
1	0	0	Nominal
1	0	1	-35%
1	1	0	-47%
1	1	1	-81%

FOR ALL APPLICATIONS, the Oscillator frequency reference should be trimmed to 100KHz +\- 5KHz. Monitoring can be done via CS2IN (PIN-4) or CS1IN (PIN-6).

Input Amplifier Control Registers

The analog front-end includes a capacitance transimpedance amplifier (IAMP) with a programmable feedback capacitor. The capacitor includes 10 bits of programmability in 19fF (+/- 20%) steps. The programmability allows the user to optimize the feedback capacitor for range and performance. An abridged version of the programming truth table is included below.

Feedback Capacitor Array CF (9:0) Binary Weighted (in 19fF steps)

CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	Capacitor (pF)
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0.019
0	0	0	0	0	0	0	0	1	0	0.038
:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	9.728
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	19.437

The MS3110 is designed to receive a pseudo-differential input sense capacitor arrangement. However, the user may wish to configure the MS3110 to sense a single-ended sense capacitor. For singled-ended operation, the balanced capacitor array CS1 is provided. The CS1 capacitor array gives the user the option to operate in single-ended mode over the entire 0.2pF-10pF range if desired. The capacitor includes 9 bits of programmability in 19fF+/- 20% steps. The resolution of 19fF allows the user to balance the CS1 capacitance with the CS2 external capacitance to minimize offset. An abridged version of the programming truth table is included on the next page and the block diagram shows the location which the feedback capacitor in the signal path.

Balance Capacitor Array CS1 (8:0) Binary Weighted (in 19fF steps)

CS1_8	CS1_7	CS1_6	CS1_5	CS1_4	CS1_3	CS1_2	CS1_1	CS1_0	Cap (pF)
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0.019
0	0	0	0	0	0	0	1	0	0.038
:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	4.864
:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	9.709

When the MS3110 is operated differentially, the external sensing capacitors that are connected to the CS1IN and CS2IN are usually mismatched; this leads to a DC offset in the output signal path. The CS1 Capacitor array along with the CS2 Capacitor array assists in reducing the DC offset by balancing the common-mode capacitance to within 19fF +/- 20% resolution. An abridged version of the programming truth table for the CS2 array is also included below.

Trim Capacitor Array CS2 (5:0) Binary Weighted (in 19fF steps)

CS2_5	CS2_4	CS2_3	CS2_2	CS2_1	CS2_0	Cap (pF)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.019
0	0	0	0	1	0	0.038
:	:	:	:	:	:	:
1	0	0	0	0	0	0.608
:	:	:	:	:	:	:
1	1	1	1	1	1	1.197

Lowpass Filter Control Registers

The two-pole lowpass filter section is designed with a programmable bandwidth ranging from 500Hz to 8kHz. The bandwidth selection error falls within +/-21% for any desired filter frequency within this filter range.

The truth table and the respective nominal 3dB bandwidths are included below.

Continuous-Time LPF Controls

CSELCT3	CSELCT2	CSELCT1	CSELCT0	Bandwidth (KHz)
0	0	0	0	8.0
0	0	0	1	5.8
0	0	1	0	4.2
0	0	1	1	3.0
0	1	0	0	2.0
0	1	0	1	1.4
0	1	1	0	1.0
0	1	1	1	0.8
1	0	0	0	0.5

*1001-1111 are unused states.

Output Buffer Control Registers

The output buffer is designed with three programmable features; offset reference level control, fine trim of DC offset, and fine trim of signal path gain. The offset reference level control allows two reference levels for the output signal. They are nominally 0.5V for single-variable mode and 2.25V for differential mode. The truth table is provided below.

Offset Reference Level Control

SOFF	Output Offset
0	VREF~2.25V
1	~0.5V

The fine trim for DC offset for the output buffer ranges +/- 100mV in 6.25mV steps. An abridged version of the truth table is included below and is applicable for GAINSEL = 0.

DC Offset Trim Control (~ 6.25mV/step)

OFF4	OFF3	OFF2	OFF1	OFF0	Offset Trim
0	0	0	0	0	-100mV
1	0	0	0	0	Nominal
1	1	1	1	1	100mV

The fine trim for signal path gain for the output buffer ranges +/- 0.3V/V in 0.0024V/V steps, the nominal gain can be set to 2V/V or 4V/V. An abridged version of the truth table is included below.

Gain Control (~ 0.0024 V/V per step) For GAINSEL=0

B7	B6	B5	B4	B3	B2	B1	B0	Gain Trim
0	0	0	0	0	0	0	0	-15%
1	0	0	0	0	0	0	0	Nominal
1	1	1	1	1	1	1	1	+15%

Nominal Output Buffer Gain Setting Control

GAINSEL	GAIN V/V
1	4
0	2

TIMING SPECIFICATIONS:

Write into EEPROM

+16 VDC Specifications

Programming the EEPROM in the MS3110 requires a +16V +/-0.5V DC supply.

Serial Data Stream Definition and Timing

Four pins are required for programming the on-chip EEPROM. They are HV16 (+16VDC), SDATA, SCLK, and WRT. SDATA, SCLK, and WRT are detailed as follows.

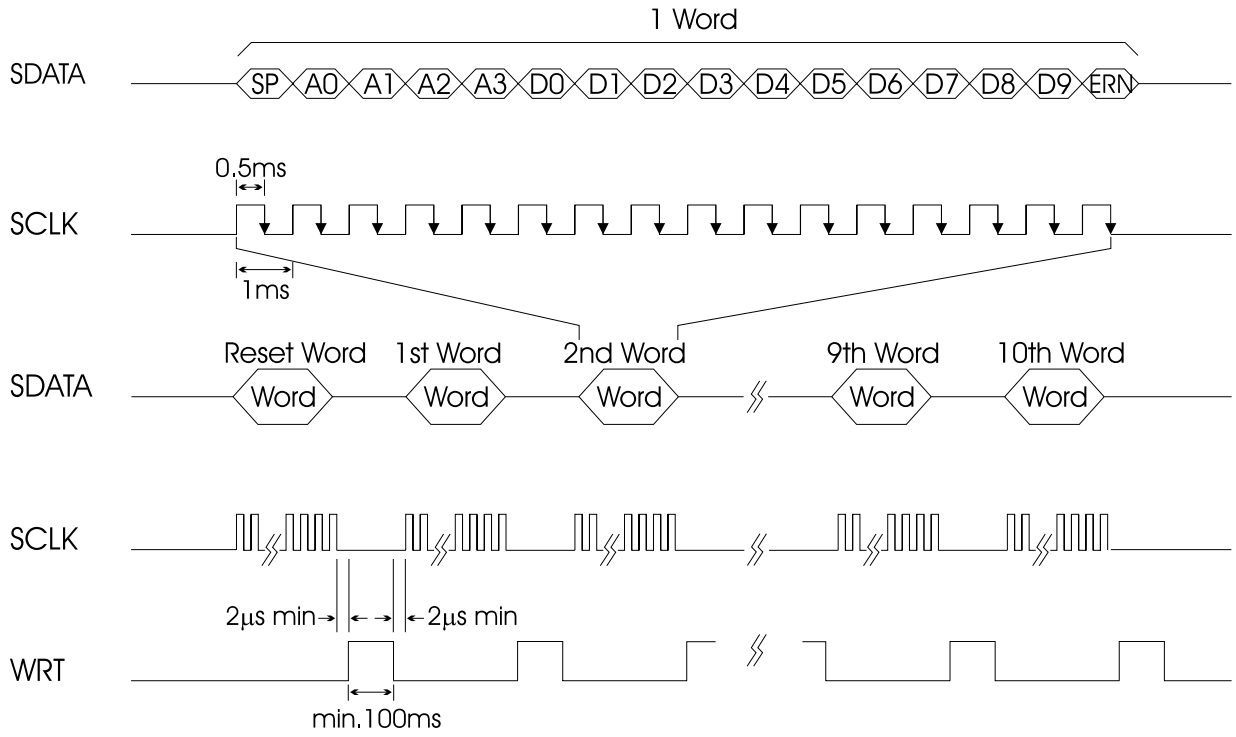
The 16-bit input data stream per address for writing to the EEPROM Memory Map is defined below. The first bit into the shift register is SP and the last bit is ERN. This represents a portion of the SDATA, or serial data stream.

ERN D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 A3 A2 A1 A0 SP (first in)

During the Erase mode, ERN is set to logic 0, and the bits following ERN are all don't care conditions. This will erase the entire memory map. Then ERN is set to logic 1 followed by the D (9:0) and A (3:0) and SP. D (9:0) writes the bits in the location map, A (3:0) represents the address location to write to, and SP is a spare bit. A timing diagram showing the relationship of these waveforms is shown. Note that the first two lines represent an expanded picture of the latter three lines.

Note that not all 10 addresses need to be included in the timing diagram. Only the addresses that require a change in the memory need be included.

EEPROM WRITE MODE TIMING DIAGRAM

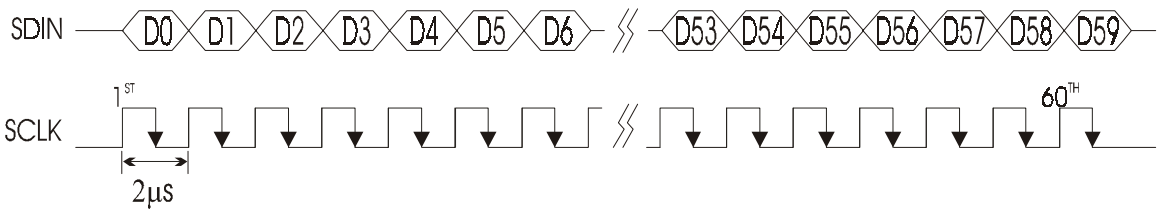


Note: tr, tf < 100ns
A total of 11 Words will be written. (1 Reset Word, 10 Write Words)
The serial data input 'SDATA' is clocked in at falling edge of the clock 'SCLK'.
The EEPROM write mode will always begin with a Reset Word set to all zeros to erase all bits in the memory.
After the Reset Word, ERN will be set to "1" during the rest of the write cycle.
HV16 needs 16V during the write mode.

Control Register Write Via External Serial Data

The MS3110 is designed with the ability to bypass the EEPROM and load the trim and control data externally into the on-chip Shift Registers. With the TESTSEL pin tied to logic low (active), the user can apply the serial data stream and the clock which the registers strobe to program the trim and controls into the shift registers. There are 58 positions to fill in the data stream. The timing diagram is shown on the next page. The order which the trims and controls are shown below are based on 60 strobe edges. Note that the user can option for 58 strobe edges and ignore the first two don't care bits, and that the HV16 and WRT pins remain unused in this mode.

VOLATILE REGISTER WRITE MODE - TIMING DIAGRAM



NOTE: TESTSEL is set to logic "0" during this test.
During this test, EEPROM is inhibited from writing data to the registers.
Data will be written to the register externally by setting serial data and clock (see above).
tr, tf < 100ns
Data is clocked in at the falling edge of the SCLK.

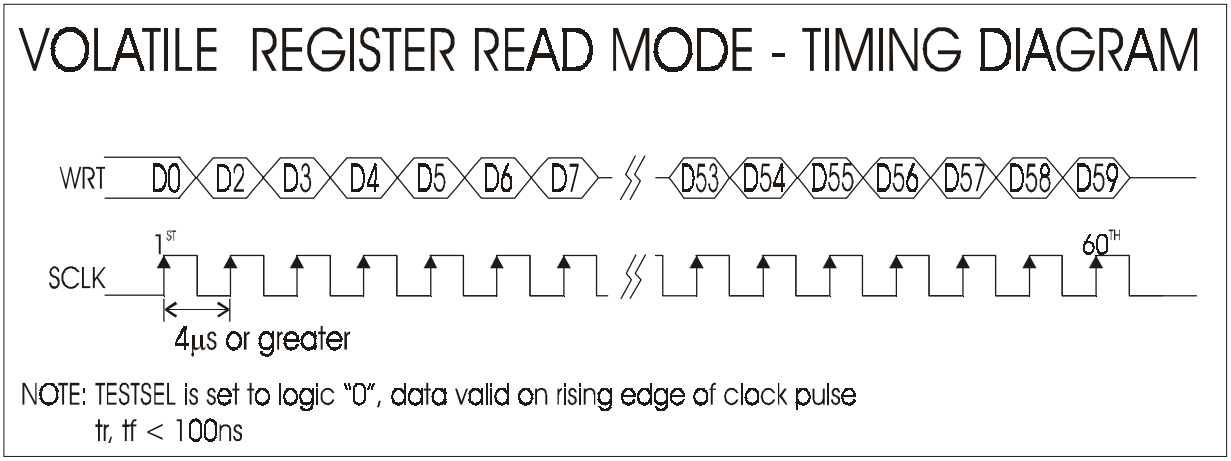
August 18, 2000

SERIAL DATA WRITE SEQUENCE & MAPPING

DX	CNTL NAME	DX	CNTL NAME	DX	CNTL NAME	DX	CNTL NAME
D0	Don't Care	D15	CS1_7	D30	Don't Care	D45	B3
D1	Don't Care	D16	CS1_8	D31	CSELCT0	D46	B2
D2	CS2_5	D17	CF0	D32	CSELCT1	D47	B1
D3	CS2_4	D18	CF1	D33	CSELCT2	D48	B0
D4	CS2_3	D19	CF2	D34	CSELCT3	D49	Don't Care
D5	CS2_2	D20	CF3	D35	SOFF	D50	D2
D6	CS2_1	D21	CF4	D36	OFF4	D51	D1
D7	CS2_0	D22	CF5	D37	OFF3	D52	D0
D8	CS1_0	D23	CF6	D38	OFF2	D53	T0
D9	CS1_1	D24	CF7	D39	OFF1	D54	T1
D10	CS1_2	D25	CF8	D40	OFF0	D55	T2
D11	CS1_3	D26	CF9	D41	B7	D56	T3
D12	CS1_4	D27	Don't Care	D42	B6	D57	R0
D13	CS1_5	D28	GAINSEL	D43	B5	D58	R1
D14	CS1_6	D29	Don't Care	D44	B4	D59	R2

Volatile Register Read Out / EEPROM Verification

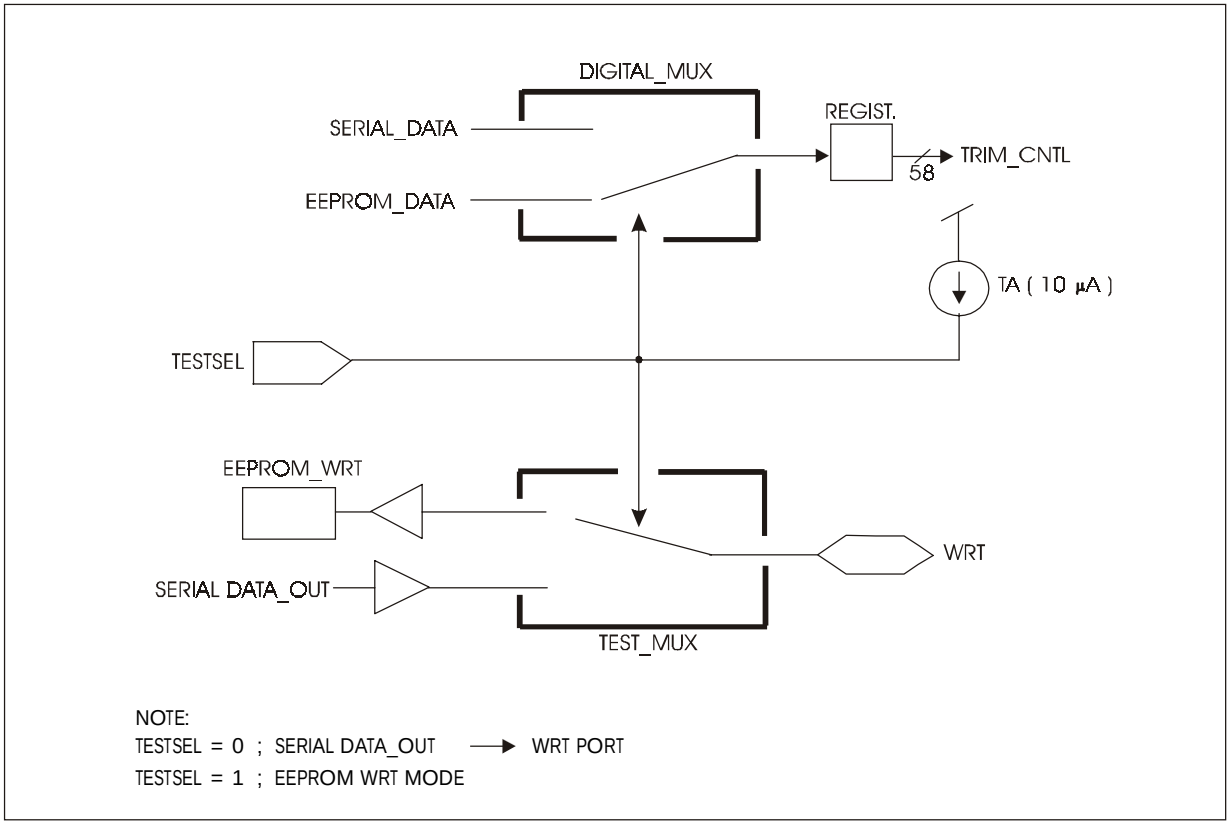
The shift register can be read out to verify the proper settings for the trim and controls; EEPROM data retention can also be verified in the following way. With the TESTSEL pin tied to logic low (active), the signal is intended to be a serial data output format gated by the external clock signal. TESTSEL active low will also enable an analog mux that directs this serial data out to the WRT port. The programming clock is injected into SCLK. A total of 58 bits fall out of the data stream. A timing relationship is shown below. The data output order is also shown below based on 60 strobe edges. Note that the user can option for 58 strobe edges and ignore the last two don't care bits.



Volatile register Readout – Timing Diagram

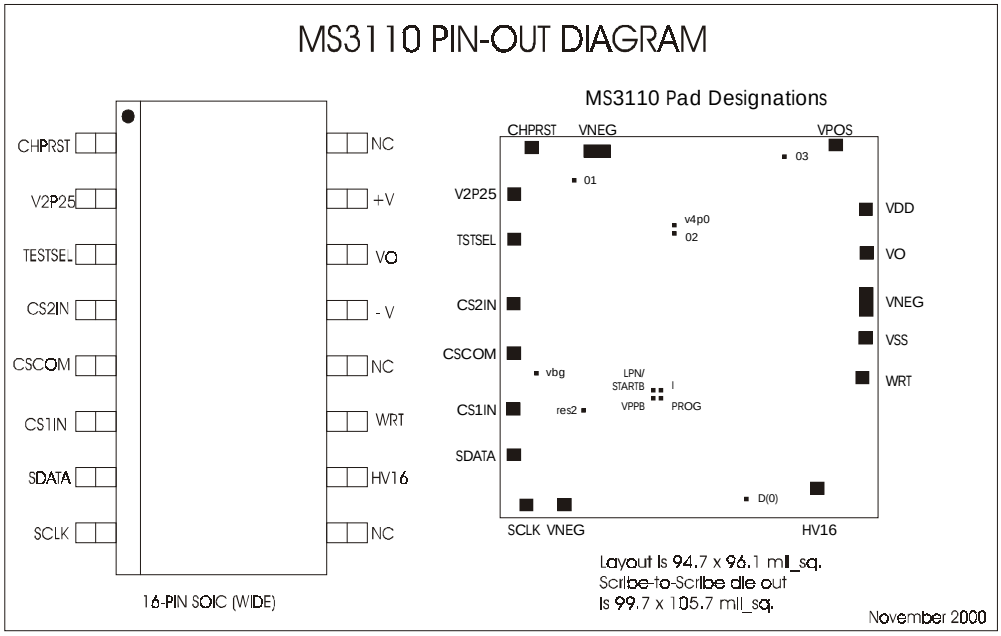
SERIAL DATA READ SEQUENCE & MAPPING

DX	CNTL NAME	DX	CNTL NAME	DX	CNTL NAME	DX	CNTL NAME
D0	CS2_5	D15	CF0	D30	CSELCT1	D45	B1
D1	CS2_4	D16	CF1	D31	CSELCT2	D46	B0
D2	CS2_3	D17	CF2	D32	CSELCT3	D47	Don't Care
D3	CS2_2	D18	CF3	D33	SOFF	D48	D2
D4	CS2_1	D19	CF4	D34	OFF4	D49	D1
D5	CS2_0	D20	CF5	D35	OFF3	D50	D0
D6	CS1_0	D21	CF6	D36	OFF2	D51	T0
D7	CS1_1	D22	CF7	D37	OFF1	D52	T1
D8	CS1_2	D23	CF8	D38	OFF0	D53	T2
D9	CS1_3	D24	CF9	D39	B7	D54	T3
D10	CS1_4	D25	Don't Care	D40	B6	D55	R0
D11	CS1_5	D26	GAINSEL	D41	B5	D56	R1
D12	CS1_6	D27	Don't Care	D42	B4	D57	R2
D13	CS1_7	D28	Don't Care	D43	B3	D58	Don't Care
D14	CS1_8	D29	CSELCT0	D44	B2	D59	Don't Care



Serial Data Readout

PIN DESCRIPTION 16-SOIC and DIE



SOIC Pin No.	Name	Description
1	CHPRST	IC Reset, internally pulled up. Normally 4.0V
2	V2P25	2.25V DC Reference.
3	TESTSEL	Test Select. Enables the user to bypass the on-chip EEPROM and program the IC directly.
4	CS2IN	Capacitor sensor input 2, to be connected with the upper electrode.
5	CSCOM	Capacitor sensor common, to be connected to the common sensor node.
6	CS1IN	Capacitor sensor input 1, to be connected with the upper sensor electrode.
7	SDATA	Serial Data Input, used for the serial data input port for programming the EEPROM or the IC registers directly. This node is internally pulled down.
8	SCLK	Serial Clock Input, serves as the strobe which the IC latches the serial data. This node is internally pulled down.
9	NC	No Connect.
10	HV16	16VDC input port, tied to 16V when Writing to EEPROM and Grounded otherwise.
11	WRT	Write Select. Enables the user to program the on-chip EEPROM.
12	NC	No Connect
13	-V	Negative Voltage Rail, usually 0V.
14	VO	IC Signal Path Voltage Output.
15	+V	Positive Voltage Rail, usually +5V.
16	NC	No Connect

PROGRAMMING/EVALUATION BOARD

An Evaluation/Programming Board is available from MicroSensors for testing the MS3110 and serves two major functions in its evaluation. The first function gives the end user the ability to program the EEPROM of the MS3110, serially program the IC in test mode and bypassing the EEPROM. The end user is then able to customize the MS3110 to his/her application by enabling various features and adjusting trims. The second function allows the end user to break-away a section of the test board for further evaluation. An MS3110 IC can be placed on the breakaway section along with other external components for characterization and evaluation.

A diagram of the Evaluation Board is shown below.

MS3110 Evaluation PCB Layout Diagram