PIC16(L)F18426/46

PIC16(L)F18426/46 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F18426/46 devices that you have received conform functionally to the current device data sheet (DS40001985**A**), except for the anomalies described in this document. The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below. The errata described in this document will be addressed in future revisions of the PIC16(L)F18426/46 silicon.

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of the *'Silicon Issue Summary'* table apply to the current silicon revision (A1).

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (http://www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   4.1. For MPLAB IDE 8, select ***Programmer*** > ***Reconnect***.
   4.2. For MPLAB X IDE, select ***Window*** > ***Dashboard*** and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID
		A1
PIC16F18426	0x30D2	0x8005
PIC16LF18426	0x30D3	0x8005
PIC16F18446	0x30D4	0x8005
PIC16LF18446	0x30D5	0x8005

Note: Refer to the **Device/Revision ID** section in the current *"PIC16(L)F184XX Memory Programming Specification"* (DS40001970) for a detailed information on Device Identification and Revision IDs for your specific device.

Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions
				A1
NVM	WRERR bit Operation	1.1.1	NVMERR bit is set by device Reset after being cleared by software.	X
MSSP	SPI	1.2.1	SSPBUF may be corrupted by writes to other GPR/SFRs.	X
Electrical Specifications	Nonvolatile Memory (NVM) Endurance for LF Devices	1.3.1	NVM self-writes on LF devices may not work properly at specified voltage levels and temperatures.	X
Analog-to-Digital Converter With Computation (ADC^2)	ADC^2 Burst Average mode	1.4.1	ADC^2 Burst Average mode while in "Non-Continuous Double Sample" mode is buggy.	X
Windowed Watchdog Timer	Window Operation	1.5.1	Window feature of the WWDT does not operate correctly in DOZE mode.	X
Device Configuration	CONFIG2	1.6.1	Bit 2 of PWRTS<1:0> in the CONFIG2 register is not functional.	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

Table of Contents

1. Silicon Errata Issues

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Nonvolatile Memory (NVM)

1.1.1 WRERR Bit Operation

When a Reset is issued while an NVM high voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the WRERR condition.

Work around

None.

Affected Silicon Revisions

A1							
X							

1.2 Module: Master Synchronous Serial Port (MSSP)

1.2.1 MSSP SPI Slave Mode

When operating in SPI Slave mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit Shift register may become corrupted. The transmitted slave byte cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

Work around

Method 1 (Interrupt based using nSS):

1. Connect the nSS line to both the nSS input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that nSS == 0 when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.
4. Continue program execution.
5. When the Interrupt Service Routine (ISR) is invoked, do either of the following:

5.1. Add a delay that ensures the first SCK clock will be complete, or

5.2. Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

Method 2 (Bit polling based using nSS):

1. Load SSPBUF with the data to be transmitted.
2. Poll the nSS line and wait for the nSS to go active (while(!PORTx.nSS == 0)).
3. When nSS is active (nSS == 0), do either of the following:
   3.1. Add a delay that ensures the first SCK clock will be complete, or
   3.2. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Once one of these two methods are complete, it is safe to return to program execution.

Method 3 (nSS not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Affected Silicon Revisions

A1							
X							

1.3 Module: Electrical Specifications

1.3.1 Nonvolatile Memory (NVM) for LF Devices

V_{DD_MIN} for parameter (D002) is 2.0V for temperatures between -40°C and 25°C.

Work around

None.

Affected Silicon Revisions

A1							
X							

1.4 Module: Analog-to-Digital Converter with Computation (ADCC)

1.4.1 ADC^2 Burst Average Mode

When the ADC^2 is operated in Burst Average mode (MD = `0b011` in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = `0` in the ADCON0 register and DSEN = `1` in the ADCON1 register), the value in the ADCNT register does not increment beyond '`0b1`' toward the value in the ADRPT register.

Work around

When operating the ADC^2 in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = `1` in the ADCON0 register) and set the Stop-on-Interrupt bit (SOI bit in the ADCON3

register). After the interrupt occurs, perform appropriate threshold calculations in the software and re-trigger ADC^2 as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC^2 in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register) compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A1							
X							

1.5 Module: Windowed Watchdog Timer (WWDT)

1.5.1 Window Operation in DOZE Mode

When the Windowed mode of operation is enabled in DOZE mode, a window violation error is issued even though the window is open and has been armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around

Method 1:

Use the Windowed mode of operation in any other than DOZE mode. If disabling the DOZE mode is not an option, use the WWDT module without the Window being enabled.

Method 2:

If the device is in DOZE mode, perform the arming process for the window in NORMAL mode and return to the DOZE mode.

Method 3:

If there is an ISR in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A1							
X							

1.6 Module: Device Configuration

1.6.1 PWRTS<1> Power-up Timer Selection Not Implemented

Bit 2 of PWRTS<1:0> in the CONFIG2 register is not functional. This bit is the upper bit of the Power-Up Timer Selection bits, PWRTS <1:0>. This means that the functions selected by PWRTS = 11 and PWRTS = 10 are not available.

Work around

The other functions selected by PWRTS = 01 and PWRTS = 00 are available.

Affected Silicon Revisions

A1							
X							

2. Revision History

Doc Rev.	Date	Comments
A	07/2018	Initial document release.
B	07/2018	Fixed typo in Table 1.

The Microchip Web Site

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