SECTION 1 — HIGH–SPEED LOGIC

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high–speed logic is the most direct way to improve system performance and Emitter–Coupled Logic (ECL) is one of today's fastest forms of digital logic. Emitter–coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

MECL PRODUCTS

Motorola introduced the original monolithic emitter–coupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III (MC1600 series), MECL 10K, PLL (MC12000 series) and the new MECL 10H families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1 ns edge speeds and propagation delays along with greater than 500 MHz flip–flop toggle rates, make MECL III useful for high–speed test and communications equipment. Also, this family is used in the high–speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in large high–speed systems showed the need for an easy–to–use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10K is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy — MECL 10K gates use less than one–half the power of MECL III.

Motorola introduced the MECL 10H product family in 1981. This latest MECL family features 100% improvements in propagation delay and clock speeds while maintaining power supply currents equal to MECL 10K. MECL 10H is voltage compensated allowing guaranteed dc and switching parameters over a ±5% power supply range. Noise margins have been improved by 75% over the MECL 10K series.

Compatibility with MECL 10K and MECL III is a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10H devices are pin out/functional duplications of the MECL 10K series devices. The emphasis of this family will be placed on more powerful logic functions having more complexity and greater performance. With 1.0 ns propagation delays and 25 mW per gate, MECL 10H is one of the best speed–power families of any ECL logic family available today.

MECL at +5V(PECL)

Any single supply ECL device is also a PECL device, making the PECL portfolio as large as the existing ECL one. (Note: The dual supply translator devices cannot operate at +5V and ground and cannot be considered PECL devices.)

ECL devices in the PECL mode, must have the input/output DC specifications adjusted for proper operation. ECL levels (DC) are referenced from the V_{CC} level. To calculate the PECL DC specifications, ECL levels are added to the new V_{CC}.

EXAMPLE:

PECL V_{OH} = New V_{CC} + ECL V_{OH}, 5.0V + (–0.81V) = 4.190V and is the max V_{OH} level at 25°C for a PECL device. Follow the same procedure to calculate all input/output DC specifications for a device used in a PECL mode. The V_{TT} supply used to sink the parallel termination currents is also referenced from the V_{CC} supply and is V_{CC}–2.0V. The PECL V_{TT} supply = +5V – 2V = +3.0V and should track the V_{CC} supply one–to–one for specified operation.

Since ECL is referenced from the V_{CC} rail, any noise on the V_{CC} supply will be reflected on the output waveshape at a one–to–one ratio. Therefore, noise should be kept as low as possible for best operation. Devices in a PECL system cannot have V_{CC} vary more than 5% to assure proper AC operation. See Motorola Application Note AN1406/D "*Designing With PECL (ECL at +5.0V)*" for more details.

AC performance in the PECL mode is equal to the AC performance in the ECL mode, if the pitfalls set forth in Application Note (AN1406/D) are avoided.

MECL FAMILY COMPARISONS

Feature	MECL 10H	MECL 10K		MECL III
		10,100 Series	10,200 Series	
1. Gate Propagation Delay	1.0 ns	2.0 ns	1.5 ns	1.0 ns
2. Output Edge Speed*	1.0 ns	3.5 ns	2.5 ns	1.0 ns
3. Flip–Flop Toggle Speed	250 MHz min	125 MHz min	200 MHz min	300–500 MHz min
4. Gate Power	25 mW	25 mW	25 mW	60 mW
5. Speed Power Product	25 pJ	50 pJ	37 pJ	60 pJ

*Output edge speed: MECL 10K/10H measured 20% to 80%, MECL III measured 10% to 90% of E out.

Figure 1 — GENERAL CHARACTERISTICS

Ambient Temperature Range	MECL 10H	MECL 10K	MECL III	PLL
0° to 75°C	MC10H100 Series			MC12000 Series
–30°C to +85°C		MC10100 Series MC10200 Series	MC1600 Series	MC12000 Series

Figure 2 — OPERATING TEMPERATURE RANGE

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Figure 1 and Figure 2 provide the basic parameters of the MECL 10H, MECL 10K, and MECL III families. But these provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power–supply design and reduces costs.

Low Cross–Talk due to low–current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10H and MECL 10K series). A basic MECL 10K gate consumes less than 8 mW in on–chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No “Line Drivers” are listed in MECL families, because *every* device is a line driver.

Wire–ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted–pair transmission lines as long as 1000 feet.

Wire–Wrap Capability is possible with the MECL 10K family because of the slow rise and fall time characteristic of the circuits.

Open Emitter–Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistors of approximately 50 kΩ permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

Motorola’s MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10K is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for larger systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers. However, the high bandwidths of MECL 10H, MECL 10K, MECL III, and MC12,000 are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL has continued to grow in the industrial market through complex medical electronic products and high performance process control systems.

BASIC CONSIDERATIONS FOR HIGH–SPEED LOGIC DESIGN

High–speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium–speed systems, become highly important at state–of–the–art speeds.
2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.
3. The possibility of “crosstalk” between adjacent signal leads is proportionately increased in high–speed systems.
4. Electrical noise generation and pick–up are more detrimental at higher speeds.

In general, these four characteristics are speed– and frequency–dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect–wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent “gate delay” is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10K and MECL 10H Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state–of–the–art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 3 and Figure 4). The solution, as in RF technology, is to employ “transmission–line” practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low–impedance, emitter–follower outputs of MECL circuits facilitate transmission–line practices without upsetting the voltage levels of the system.*

The increased affinity for crosstalk in high–speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high–speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10K and MECL 10H, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.*

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high–speed operation.

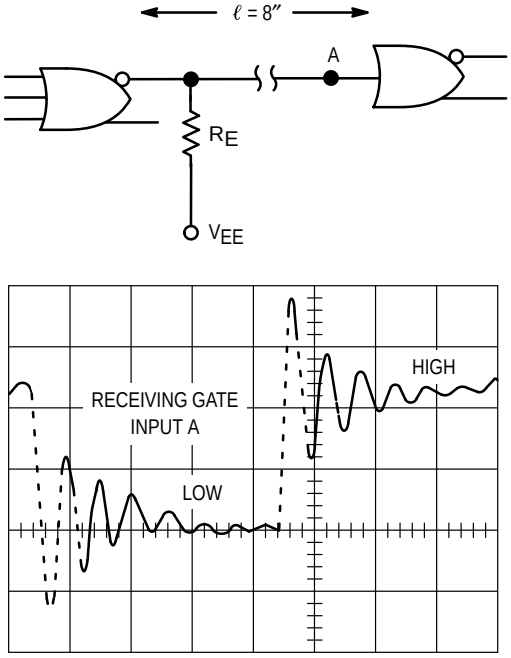

Figure 3 — UNTERMINATED TRANSMISSION LINE (No Ground Plane Used)

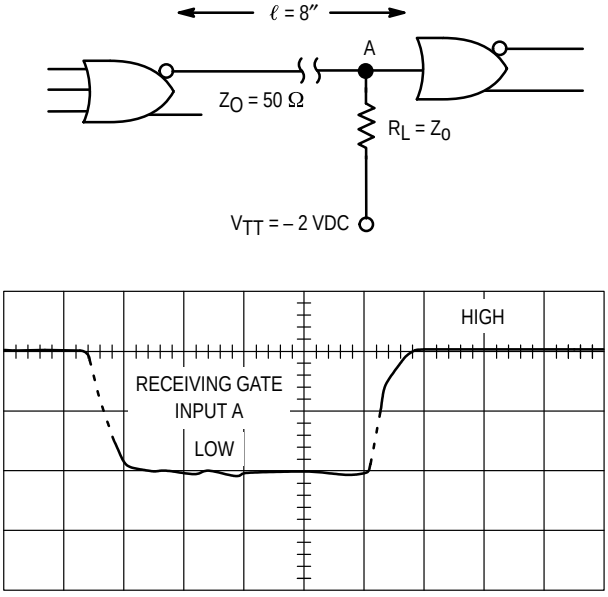

Figure 4 — PROPERLY TERMINATED TRANSMISSION LINE (Ground Plane Added)

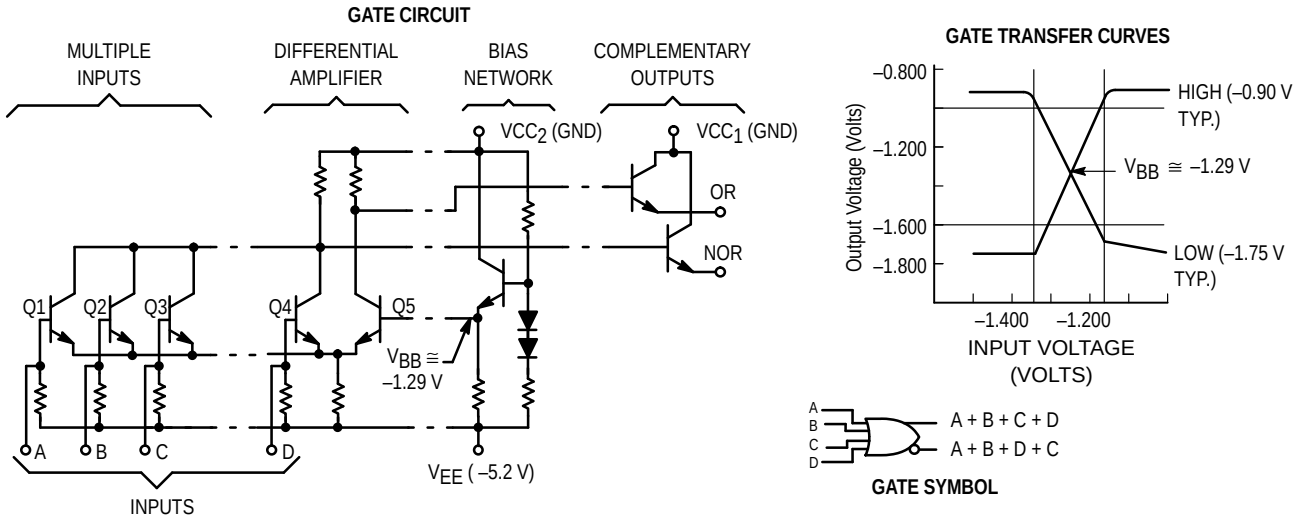

Figure 5 — MECL 10K GATE STRUCTURE AND SWITCHING BEHAVIOR

CIRCUIT DESCRIPTION

The typical MECL 10K circuit, Figure 5, consists of a differential–amplifier input circuit, a temperature and voltage compensated bias network, and emitter–follower outputs to restore dc levels and provide buffering for transmission line driving. High fan–out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power–supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function. The design of the MECL 10H gate is unchanged, with two exceptions. The bias network has been replaced with a voltage regulator, and the differential amplifier source resistor has been replaced with a constant current source. (See section 2 for additional MECL 10H information.)

Power–Supply Connections — Any of the power supply levels, V_{TT}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: V_{CC} = 0, V_{TT} = –2.0 V, V_{EE} = –5.2 V.

System Logic Specifications — The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of V_{OL} = –1.75 V to a HIGH state of V_{OH} = –0.9 V with respect to ground.

Positive logic is used when reference is made to logical “0’s” or “1’s.” Then

“0” = –1.75 V = LOW

typical

“1” = –0.9 V = HIGH

Circuit Operation — Beginning with all logic inputs LOW (nominal –1.75 V), assume that Q1 through Q4 are cut off because their P–N base–emitter junctions are not conducting, and the forward–biased Q5 is conducting. Under these conditions, with the base of Q5 held at –1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or –2.09 V. (The 0.8 V differential is a characteristic of this P–N junction.) The base–to–emitter differential across Q1 — Q4 is then the difference between the common emitter voltage (–2.09 V) and the LOW logic level (–1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the –1.75 V LOW state to the –0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common–emitter point rises from –2.09 V to –1.7 (one diode drop below the –0.9 V base voltage of the input transistor), and since the base voltage of the fixed–bias transistor (Q5) is held at –1.29 V, the base–emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 – Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 – Q4 and Q5 are transferred through the output emitter–follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Current:

I_{CC} Total power supply current drawn from the positive supply by a MECL unit under test.

I_{CBO} Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.

I_{CCH} Current drain from V_{CC} power supply with all inputs at logic HIGH level.

I_{CCL} Current drain from V_{CC} power supply with all inputs at logic LOW level.

I_E Total power supply current drawn from a MECL test unit by the negative power supply.

I_F Forward diode current drawn from an input of a saturated logic–to–MECL translator when that input is at 0.4V.

I_{in} Current into the input of the test unit when a maximum logic HIGH ($V_{IH\ max}$) is applied at that input.

I_{INH} HIGH level input current into a node with a specified HIGH level ($V_{IH\ max}$) logic voltage applied to that node. (Same as I_{in} for positive logic.)

I_{INL} LOW level input current, into a node with a specified LOW level ($V_{IL\ min}$) logic voltage applied to that node.

I_L Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.

I_{OH} HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.

I_{OL} LOW level output current: the current flowing into the output, at a specified LOW level output voltage.

I_{OS} Output short circuit current.

I_{out} Output current (from a device or circuit, under such conditions mentioned in context).

I_R Reverse current drawn from a transistor input of a test unit when V_{EE} is applied to that input.

$I_{R'}$ Reverse current leakage into an input of a saturated logic MECL/PECL translator when that input is at V_{CC}.

I_{SC} Short–circuit current drawn from a translator saturating output when that output is at ground potential.

Voltage:

V_{BB} Reference bias supply voltage.

V_{BE} Base–to–emitter voltage drop of a transistor at specified collector and base currents.

V_{CB} Collector–to–base voltage drop of a transistor at specified collector and base currents.

V_{CC} General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).

V_{CC1} Most positive power supply voltage (output devices). (Usually ground for MECL devices.)

V_{CC2} Most positive power supply voltage (current switches and bias driver). (Usually ground for MECL devices.)

V_{EE} Most negative power supply voltage for a circuit (usually –5.2 V for MECL devices).

V_F Input voltage for measuring I_F on TTL interface circuits.

V_{IH} Input logic HIGH voltage level (nominal value).

$V_{IH\ max}$ Maximum HIGH level input voltage: The most positive (least negative) value of high–level input voltage, for which operation of the logic element within specification limits is guaranteed.

V_{IHA} Input logic HIGH threshold voltage level.

$V_{IHA\ min}$ Minimum input logic HIGH level (threshold) voltage for which performance is specified.

$V_{IH\ min}$ Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Input logic LOW voltage level (nominal value).

$V_{IL\ max}$ Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{ILA} Input logic LOW threshold voltage level.

$V_{ILA\ max}$ Maximum input logic LOW level (threshold) voltage for which performance is specified.

$V_{IL\ min}$ Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{in} Input voltage (to a circuit or device).

V_{max} Maximum (most positive) supply voltage, permitted under a specified set of conditions.

V_{OH} Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.

V_{OHA} Output logic HIGH threshold voltage level.

$V_{OHA\ min}$ Minimum output HIGH threshold voltage level for which performance is specified.

$V_{OH\ max}$ Maximum output HIGH or high–level voltage for given inputs.

$V_{OH\ min}$ Minimum output HIGH or high–level voltage for given inputs.

V_{OL} Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.

V_{OLA} Output logic LOW threshold voltage level.

$V_{OLA\ max}$ Maximum output LOW threshold voltage level for which performance is specified.

Voltage (cont.):

$V_{OL\ max}$ Maximum output LOW level voltage for given inputs.

$V_{OL\ min}$ Minimum output LOW level voltage for given inputs.

V_{TT} Line load–resistor terminating voltage for outputs from a MECL device.

Time Parameters:

t+ Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.

t– Waveform fall time (HIGH to LOW), 90% to 10%, or 80% to 20%, as specified.

t_r Same as t+

t_f Same as t–

t+– Propagation Delay, see NO TAG on page NO TAG.

t–+ Propagation Delay, see NO TAG on page NO TAG.

t_{pd} Propagation delay, input to output from the 50% point of the input waveform at pin x (falling edge noted by — or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by – or rising edge noted by +). (Cf NO TAG on page NO TAG.)

$t_{x\pm y\pm}$

t_{x+} Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified.

t_{x-} Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified.

f_{Tog} Toggle frequency of a flip–flop or counter device.

f_{shift} Shift rate for a shift register.

Read Mode (Memories)

t_{ACS} Chip Select Access Time

t_{RCS} Chip Select Recovery Time

t_{AA} Address Access Time

Write Mode (Memories)

t_W Write Pulse Width

t_{WSD} Data Setup Time Prior to Write

t_{WHD} Data Hold Time After Write

t_{WSA} Address setup time prior to write

t_{WHA} Address hold time after write

t_{WSCS} Chip select setup time prior to write

t_{WHCS} Chip select hold time after write

t_{WS} Write disable time

t_{WR} Write recovery time

Temperature:

T_{stg} Maximum temperature at which device may be stored without damage or performance degradation.

T_J Junction (or die) temperature of an integrated circuit device.

T_A Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.

θ_{JA} Thermal resistance of an IC package, junction to ambient.

θ_{JC} Thermal resistance of an IC package, junction to case.

lfpm Linear feet per minute.

θ_{CA} Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e_g Signal generator inputs to a test circuit.

TP_{in} Test point at input of unit under test.

TP_{out} Test point at output of unit under test.

D.U.T. Device under test.

C_{in} Input capacitance.

C_{out} Output capacitance.

Z_{out} Output impedance.

P_D The total dc power applied to a device, not including any power delivered from the device to a load.

R_L Load Resistance.

R_T Terminating (load) resistor.

R_p An input pull–down resistor (i.e., connected to the most negative voltage).

P.U.T. Pin under test.

MECL POSITIVE AND NEGATIVE LOGIC

INTRODUCTION

The increasing popularity and use of emitter coupled logic has created a dilemma for some logic designers. Saturated logic families such as TTL have traditionally been designed with the NAND function as the basic logic function, however, the basic ECL logic function is the NOR function (positive logic). Therefore, the designer may either design ECL systems with positive logic using the NOR, or design with negative logic using the NAND. Which is the more convenient? On the one hand the designer is familiar with positive logic levels and definitions, and on the other hand, he is familiar with implementing systems using NAND functions. Perhaps a presentation of the basic definitions and characteristics of positive and negative logic will clarify the situation and eliminate misunderstanding.

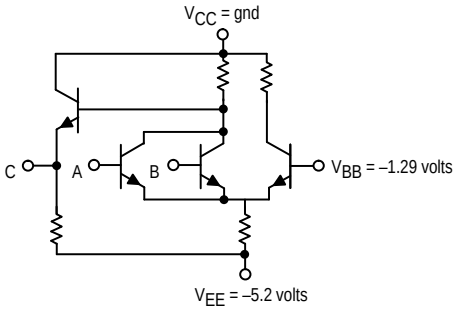

Table 1

INPUTS		OUTPUT
A	B	C
LO	LO	HI
LO	HI	LO
HI	LO	LO
HI	HI	LO

HI = –0.9 volts
LO = –1.7 volts

Table 2

NEGATIVE LOGIC

INPUTS		OUTPUT
A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

$C = \overline{A \bullet B}$

Table 3

POSITIVE LOGIC

INPUTS		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

$C = \overline{A + B}$

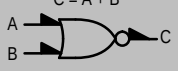

Figure 6 — Basic MECL Gate Circuit and Logic Function In Positive and Negative Nomenclature.

LOGIC EQUIVALENCIES

Binary logic must have two states to represent the binary 1 and 0. With ECL the typical states are a high level of –0.9 volts and a low level of –1.7 volts. Two choices are possible then to represent the binary 1 and 0. Positive logic defines the 1 or "true" state as the most positive voltage level, whereas negative logic defines the most negative voltage level as the 1 or "true" state. Because of the difference in definition of states, the basic ECL gate is a NOR function in positive logic and is a NAND function in negative logic.

Figure 6 more clearly shows the above comparison of functions. Table 1 lists the output voltage level as a function of input voltage levels of the MECL gate circuit shown. Table 2 translates the voltage levels into the appropriate negative logic levels which show the function to be $C = \overline{A \bullet B}$; that is, the circuit performs the NAND function. Table 3 translates the equivalent positive logic function into $C = \overline{A + B}$, the NOR function.

Similar comparisons could be made for other positive logic functions. As an example, the positive OR function translates to the negative AND function. Figure 7 shows a comparison of several common logic functions.

Any function available in a logic family may be expressed in terms of positive or negative logic, bearing in mind the definition of logic levels. The choice of logic definition, as previously stated, is dependent on the designer. Motorola provides both positive and negative logic symbols on data sheets for the popular MECL 10,000 logic series.

Figure 7 — Comparative Positive and Negative Logic Functions.

		POSITIVE LOGIC					
INPUTS							
A	B	AND	OR	NAND	NOR	EXOR	COIN*
LO	LO	LO	LO	HI	HI	LO	HI
LO	HI	LO	HI	HI	LO	HI	LO
HI	LO	LO	HI	HI	LO	HI	LO
HI	HI	HI	HI	LO	LO	LO	HI
A	B	OR	AND	NOR	NAND	COIN*	EXOR
INPUTS							
		NEGATIVE LOGIC					

*Coincidence

SUMMARY

Conversion from one logic form to another or the use of a particular logic form need not be a complicated process. If the designer uses the logic form with which he is familiar and bears in mind the previously mentioned definition of levels, problems arising from definition of logic functions should be minimized.

REFERENCE

Y. Chu, Digital Computer Design Fundamentals
New York, McGraw–Hill, 1962