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MOTOROLA

MC33411A/B

Advance Information

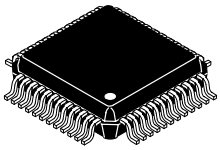
900 MHz Analog Cordless Phone Baseband with Compander

900 MHz ANALOG CORDLESS PHONE BASEBAND WITH COMPANDER

SEMICONDUCTOR TECHNICAL DATA

The MC33411 900 MHz Analog Cordless Phone Baseband system is designed to fit the requirements of a 900 MHz analog cordless telephone system. Included are three PLLs (Phase–Locked Loops). Two are intended for use with external VCOs and 64/65 or 128/129 dual modulus prescalers, and can control the transmit and receive (LO1) frequencies for 900 MHz communication. The third PLL is configured as the 2nd local oscillator (LO2), and is functional to 80 MHz. Also included are muting, audio gain adjust (internal and external), low battery/carrier detect, and a wide range for the PLL reference frequency. The power supply range is 2.7 to 5.5 V. ”A” version devices have programmable MCU clock out and reference oscillator disable functions, whereas these functions are always enabled for ”B” version devices.

- Complete Expander/Compressor for Superior Noise Rejection
- Two PLLs and a LO Suitable for a 900 MHz System
- Minimal External Components
- Transmit Path Includes Adjustable Gain Amplifier, Filters, Mute, Compressor with Bypass and Limiter
- Receive Path Contains Data Slicer, Adjustable Gain Amplifier, Sidetone Attenuator, Filters, Expander with Bypass, Mute, Volume Control and Power Amplifier
- Dual A/Ds are Provided to Monitor RSSI and V_{CC}
- Independent Power Amplifier with Differential Outputs and Mute
- Selectable Frequency for Switched Capacitor Filters, PLLs and the LO
- Reference Frequency Source can be a Crystal or System Clock
- Serial µP Port to Control Gain, Mute, Frequency Selection, Phase Detector Gain, Power Down Modes, Low Battery Detect and Others
- Power Supply Range: 2.7 to 5.5 V
- Power Down Modes for Power Conservation

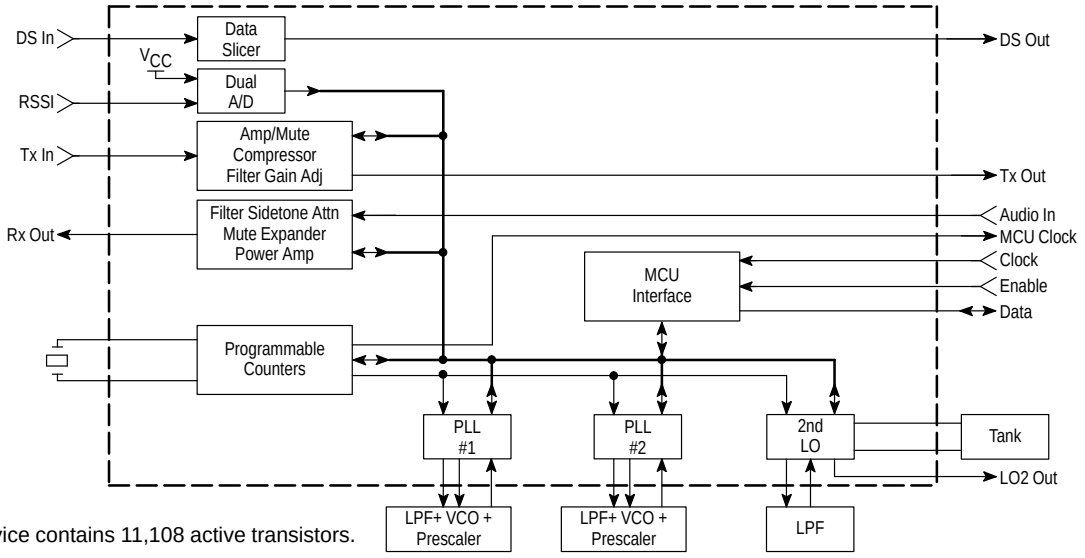


FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

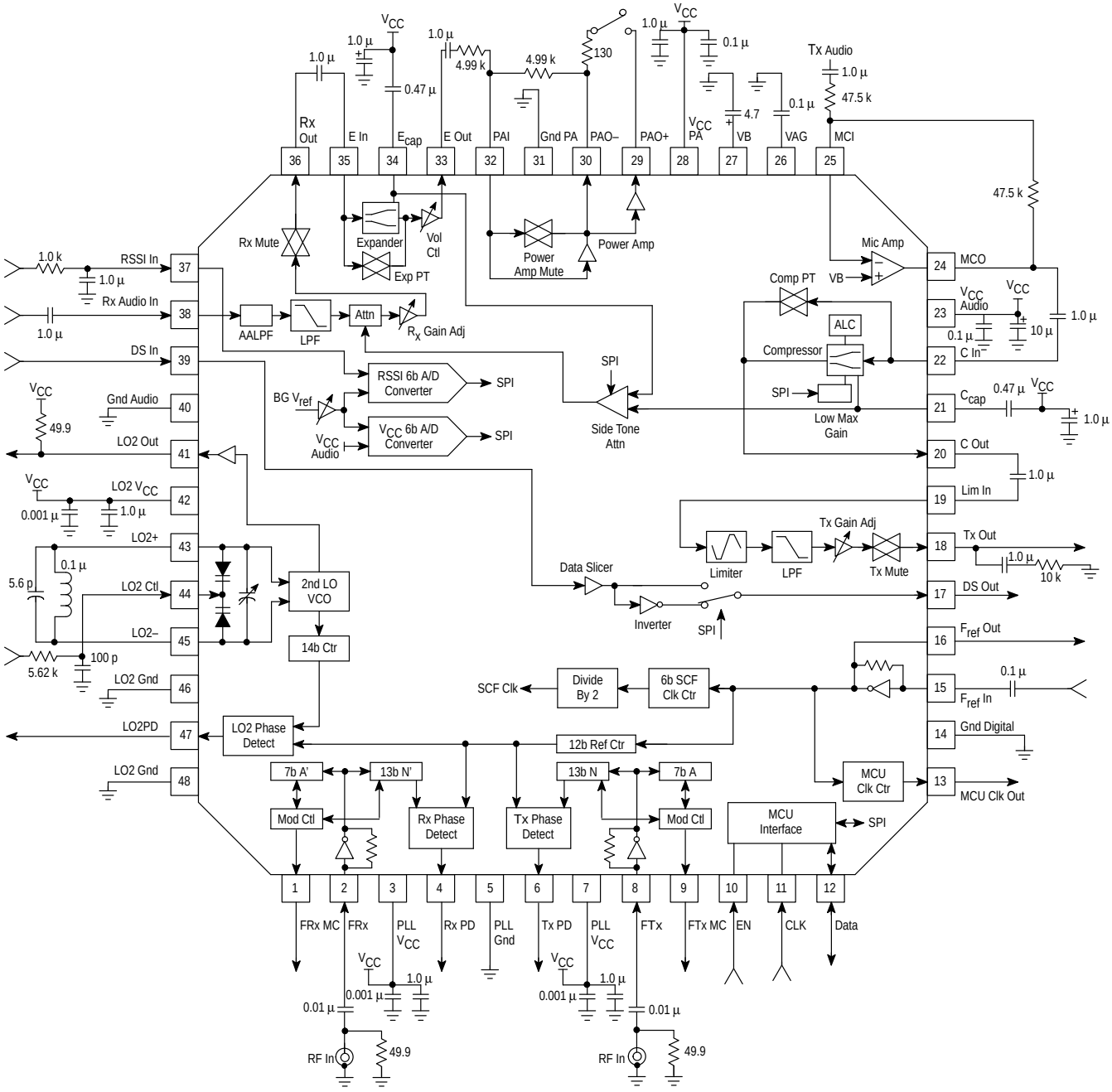
Device	Operating Temperature	Package
MC33411AFTA	T_A = –20 to 70°C	LQFP–48
MC33411BFTA		

Simplified Block Diagram



This device contains 11,108 active transistors.

Figure 1. Test Circuit



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 6.0	V
Junction Temperature	T_J	–6.5 to 150	°C
Maximum Power Dissipation	P_D	150	mW

NOTES: 1. Meets Human Body Model (HBM) ≤2000 V and Machine Model (MM) ≤200 V.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.6	5.5	Vdc
Operating Ambient Temperature	T_A	–20	–	70	°C
Input Voltage Low (Data, CLK, EN)	V_{il}	–	–	0.3	V
Input Voltage High (Data, CLK, EN)	V_{ih}	Tx PLL V_{CC} – 0.3	–	–	V
Frequency Range ($F_{ref\ in}$)	F_{range}	4.0	–	18.25	MHz
Bandgap Reference Voltage	V_B	–	1.5	–	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Static Current					
Active Mode (R5/8 to 0 = 0; R6/7 = 0)	ACT I_{CC}	–	15	20	mA
Receive Mode (R5/8, 7, 3, 2, 0 = 0; R6/7 = 0; R5/6,5,4,1 = 1)	Rx I_{CC}	–	10	13	mA
Standby Mode (R5/0 = 0; R6/7 = 0; R5/8 to 1 = 1)	STD I_{CC}	–	500	1500	µA
Inactive Mode, A only (R5/8 to 0 =1; R6/7 = 1)	INA I_{CC}	–	10	15	µA
Data Slicer Only	DS I_{CC}	–	100	–	µA
RSSI/Batt A/D Only	AD I_{CC}	–	70	–	µA
Tx Audio Only	TxA I_{CC}	–	1.4	–	mA
Rx Audio Only	RxA I_{CC}	–	1.4	–	mA
PA Only	PA I_{CC}	–	1.0	–	mA
2nd LO/F_{ref} Only	2LO I_{CC}	–	6.0	–	mA
Rx PLL/F_{ref} Only	RxPLL I_{CC}	–	1.0	–	mA
Tx PLL/F_{ref} Only	TxPLL I_{CC}	–	1.0	–	mA
Ref Osc Only, ”A” version only	ROSC I_{CC}	–	500	–	µA
Reference Voltage, Unadjusted	V_B	1.38	1.5	1.62	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Rx AUDIO PATH							
Absolute Gain (V_{in} = –20 dBV)	Rx Audio In	E Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to E_{out} for V_{in} = –20 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	E In	E Out	G_t	 –21 –42	 –20 –40	 –19 –38	dB
Total Harmonic Distortion (V_{in} = –20 dBV)	Rx Audio In	PAO–	THD	–	0.7	1.0	%
Maximum Input Voltage (V_{CC} = 2.7 V)	Rx Audio In			–	–11.5	–	dBV
Maximum Output Voltage (Increase input voltage until output voltage THD = 5%, then measure output voltage)	E In	E Out	V_{Omax}	–2.0	0	–	dBV

NOTES: 1. Values specified are pure numbers to the base 10.
2. Typical performance parameters indicate the potential of the device under ideal operating conditions.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Rx AUDIO PATH (continued)							
Input Impedance		RxAudio In E In	Z_{in}	– –	600 7.5	– –	kΩ
Attack Time E_{cap} = 0.5 μF, R_{filt} = 40 k	E In	E Out	t_a	–	3.0	–	mS
Release Time E_{cap} = 0.5 μF, R_{filt} = 40 k	E In	E Out	t_r	–	13.5	–	mS
Compressor to Expander Crosstalk (V_{in} = –10 dBV, $V_{E\ In}$ = AC Gnd)	MCI	E Out	C_T	–	–90	–60	dB
Rx Muting (V_{in} = –20 dBV, Rx Gain Adj = 01111)	Rx Audio In	E Out	M_e	–	–84	–60	dB
Rx High Frequency Corner (V_{in} = –20 dBV) SCF Counter = 31_d	Rx Audio In	Rx Out	Rx f_{ch}	3.6	3.8	4.0	kHz
Low Pass Filter Passband Ripple (V_{in} = –20 dBV)	Rx Audio In	Rx Out	Ripple	–	0.4	0.6	dB
Rx Gain Adjust Range	Rx Audio In	Rx Out	Rx Range	–	–9.0 to 10	–	dB
Rx Gain Adjust Steps	Rx Audio In	Rx Out	Rx n	–	20	–	
Audio Path Noise, C–Message Weighting (V_{in} = AC Gnd)	Rx Audio In	 Rx Out E Out PA Out	EN	 – – –	 –85 <–95 <–95	 – – –	dBV
Volume Control Adjust Range	Rx Audio In	E Out	$V_{CtRange}$	–	–14 to 16	–	dB
Volume Control Levels	E In	E Out	V_{cn}	–	16	–	
Side Tone Attenuate Selections	Rx Audio In	Rx Out	STA_n	–	4	–	
Side Tone Attenuate (Referenced to E In) Selection = 00 Selection = 01 Selection = 10 Selection = 11		E Out	STA	 – – – –	 0.0 1.5 3.0 5.2	 – – – –	dB
Side Tone Attenuate Threshold (C Out/E In)			STA_{thr}	–	–3.0	–	dB
POWER AMP/MUTE (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, f_{in} = 1.0 kHz)							
Output Swing, ±5.0 mA load (V_{PAO+} @ –5.0 mA – V_{PAO+}@ 5.0 mA)	PAI	PAO+	V_{Omax}	1.3	2.4	–	V_{pp}
Output Swing, ±5.0 mA load ($V_{PAO–}$ @ –5.0 mA – $V_{PAO–}$@ 5.0 mA)	PAI	PAO–	V_{Omax}	1.3	2.4	–	V_{pp}
Output Swing, No Load	PAI	PAO+	V_{Omax}	–	2.7	–	V_{pp}
Output Swing, No Load	PAI	PAO–	V_{Omax}	–	2.7	–	V_{pp}
Maximum Output Current		PAO–, PAO+	I_{Omax}	–	±5.0	–	mA
Power Amp Mute (V_{in} = –20 dBV, RL = 130 Ω)	PAI	PAO–	M_{sp}	–	–92	–60	dB
MIC AMP (V_{CC} = 3.6 V, T_A = 25°C, Active Mode, f_{in} = 1.0 kHz)							
Open Loop Gain	MCI	MCO	AVOL	–	100.000	–	V/V
Gain Bandwidth	MCI	MCO	GBW	–	100	–	kHz
Maximum Output Swing (RL = 10 kΩ)	MCI	MCO	V_{Omax}	–	3.2	–	V_{pp}

NOTES: 1. Values specified are pure numbers to the base 10.
2. Typical performance parameters indicate the potential of the device under ideal operating conditions.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Tx AUDIO PATH (V_{CC} = 3.6 V, Limiter, Mutes, ALC disabled, T_A = 25°C, Gain = 1, Active Mode, f_{in} = 1.0 kHz)							
Absolute Gain (V_{in} = –10 dBV)	MCI	TX Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to Tx Out for V_{in} = –10 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	MCI	Tx Out	G_t	 –11 –17	 –10 –15	 –9.0 –13	dB
Total Harmonic Distortion (V_{in} = –10 dBV)	MCI	Tx Out	THD	–	0.5	1.2	%
Maximum Output Voltage (Increase input voltage until output voltage THD = 5%, then measure output voltage. Tx Gain Adj = 8.0 dB)	MCI	Tx Out	V_{Omax}	–8.0	–5.0	–	dBV
Input Impedance		C In	Z_{in}	–	10	–	kΩ
Attack Time C_{cap} = 0.5 µF, R_{filt} = 40 k	C In	Tx Out	t_a	–	3.0	–	mS
Release Time C_{cap} = 0.5 µF, R_{filt} = 40 k	C In	Tx Out	t_r	–	13.5	–	mS
Expander to Compressor Crosstalk (V_{in} = –20 dBV, PA no load, VC_{in} = AC Gnd)	E In	Tx Out	C_T	–	–60	–40	dB
Tx Muting (V_{in} = –10 dBV)	MCI	Tx Out	M_c	–	–88	–60	dB
ALC Output Level (When Enabled) V_{in} = –10 dBV V_{in} = –2.5 dBV	MCI	Tx Out	ALC_{out}	 –15 –13	 –13 –11	 –8.0 –6.0	dBV
ALC Slope (When Enabled) V_{in} = –10 dBV V_{in} = –2.5 dBV	MCI	Tx Out	Slope	0.1	0.25	0.4	dB/dB
ALC Input Dynamic Range	C In	Tx Out	DR	–	–16 to –2.5	–	dBV
Limiter Output Level (When Enabled, V_{in} = –2.5 dBV)	Lim In	Tx Out	V_{lim}	–10	–7.0	–	dBV
Tx High Frequency Corner (V_{in} = –10 dBV, Unity Gain) SCF Counter = 31_d	Lim In	Tx Out	Tx f_{ch}	3.45	3.65	3.85	kHz
Low Pass Filter Passband Ripple (V_{in} = –10 dBV)	Lim In	Tx Out	Ripple	–	0.4	1.0	dB
MCU Clock or SCF Spurs (V_{in} = –10 dBv, relative to SCF or MCU Fundamental)	Lim In	Tx Out	–	–	–25	–	dBc
Maximum Compressor Gain (V_{in} = –70 dBV) R6/8 = 0 R6/8 = 1	MCI	Tx Out	AV_{max}	 – –	 21 12	 – –	dB
Tx Gain Adjust Range	Lim In	Tx Out	Tx Range	–	–9.0 to 10	–	dB
Tx Gain Adjust Steps	Lim In	Tx Out	Tx N	–	20	–	
DATA AMP COMPARATOR (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
Hysteresis	DS In	DS Out	Hys	20	42	60	mV
Threshold Voltage	DS In	DS Out	V_T	–	V_{CC} – 0.7	–	V
Input Impedance		DS In	Z_{in}	200	250	280	kΩ
Output Impedance		DS Out	Z_{out}	–	100	–	kΩ
Output High Voltage (V_{in} = V_{CC} – 1.0 V, I_{oh} = 0 mA)	DS In	DS Out	V_{oh}	V_{CC} Audio – 0.1	V_{CC} Audio	–	V
Output Low Voltage (V_{in} = V_{CC} – 0.4 V, I_{ol} = 0 mA)	DS In	DS Out	V_{ol}	–	0.1	0.4	V
Maximum Frequency	DS In	DS Out	F_{max}	–	10	–	kHz

NOTES: 1. Values specified are pure numbers to the base 10.
2. Typical performance parameters indicate the potential of the device under ideal operating conditions.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI/LOW BATTERY A/D (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
RSSI Voltage Range Minimum (R5/17–12 = 0) Interim (R5/17–12 = 100000) Maximum (R5/17–12 = 1)	RSSI In	SPI	RSSI Range	 – .744 –	 0 – 1.6	 – .792 –	V
Low Battery Detect Operating Range Minimum Interim (R5/23–18 = 101111) Maximum (R5/23–18 = 1)	V_{CC} Audio	SPI	LOWB Range	 – 2.7 –	 2.7 – 3.75	 – 3.1 –	V
Differential Non–linearity	RSSI In/ V_{CC} Audio	SPI	A/D DNL	–1.0	±0.5	1.0	LSB
Resolution	RSSI In/ V_{CC} Audio	SPI	Resolution	–	6	–	Bits
Input Current		RSSI In	I_{in}	–80	20	80	nA
REFERENCE FREQUENCY (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode)							
Input Current High (V_{in} = V_{CC})		$F_{ref\ in}$	I_{ih}	2.0	5.0	15	µA
Input Current Low (V_{in} = 0 V)		$F_{ref\ in}$	I_{il}	–15	–5.0	–2.0	µA
Minimum Input Voltage F_{ref} In	$F_{ref\ in}$	$F_{ref\ out}$	V_{in}	300	–	–	mVpp
Input Impedance		$F_{ref\ in}$	Z_{in}	–	2.9 pF||11.6 kΩ	–	
Output Impedance		$F_{ref\ out}$	Z_{out}	–	2.5 pF||4.5 kΩ	–	
MICROPROCESSOR INTERFACE (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
Input Low Voltage	Data/EN /CLK		V_{il}	0	–	0.3	V
Input High Voltage	Data/EN /CLK		V_{ih}	Tx PLL V_{CC} – 0.3	–	Tx PLL V_{CC}	V
Input Current Low (V_{in} = 0.3 V, Standby Mode) Data, EN, CLK		Data, EN, CLK	I_{il}	–5.0	0.4	–	µA
Input Current High (V_{in} = 3.3 V, Standby Mode) Data, EN, CLK		Data, EN, CLK	I_{ih}	–	1.6	5.0	µA
Hysteresis Voltage Data, EN, CLK		Data, EN, CLK	V_{hys}	–	1.0	–	V
Maximum Clock Frequency	CLK		F_{max}	2.0	–	–	MHz
Input Capacitance Data, EN, CLK		Data, CLK, EN	C_{in}	–	8.0	–	pF
EN to CLK Setup Time		EN, CLK	t_{suEC}	–	200	–	nS
Data to CLK Setup Time		Data, CLK	t_{suDC}	–	100	–	nS
Hold Time		Data, CLK	t_h	–	90	–	nS
Recovery Time		EN, CLK	t_{rec}	–	90	–	nS
Input Pulse Width		EN, CLK	t_w	–	100	–	nS
MCU Interface Power–Up Delay			t_{puMCU}	–	100	–	µS
Output High Voltage (I_{oh} = 0 mA)		MCU Clk Out	V_{oh}	Tx PLL V_{CC} – 0.3	3.5	–	V

NOTES: 1. Values specified are pure numbers to the base 10.
2. Typical performance parameters indicate the potential of the device under ideal operating conditions.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
MICROPROCESSOR INTERFACE (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
Output Low Voltage (I_{ol} = 0 mA)		MCU Clk Out	V_{ol}	–	0.1	0.3	V
Output High Voltage (I_{oh} = 0 mA)		Data	V_{oh}	Tx PLL V_{CC} – 0.3	3.5	–	V
Output Low Voltage (I_{ol} = 0 mA)		Data	V_{ol}	–	0.1	0.3	V
Rx/Tx PLL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or Receive Mode)							
Output Source Current (V_{PD} = 0.5 V or V_{CC} – 0.5 V) ±100 µA mode ±400 µA mode		 Rx PD & Tx PD	I_{oh}	 –130 –520	 –100 –400	 –70 –280	µA
Output Sink Current (V_{PD} = 0.5 V or V_{CC} – 0.5 V) ±100 µA mode ±400 µA mode		 Rx PD & Tx PD	I_{ol}	 70 280	 100 400	 130 520	µA
Current Match, ±100 µA mode or ±400 µA mode, V_{PD} = V_{CC} / 2 (i.e., 100 x (ABS (I_{oh} / I_{ol})))		Rx PD Tx PD	Match	80	100	125	%
Output Off Current (V_{PD} = V_{CC} /2),±100 µA mode or ±400 µA mode		Rx PD Tx PD	I_{oz}	–80	5.0	80	nA
Input Current Low (V_{in} = 0 V)		FRx FTx	I_{il}	–10	–7.5	–	µA
Input Current High (V_{in} = V_{CC})		FRx FTx	I_{ih}	–	10	14	µA
Input Bias Voltage		FRx FTx	V_{bias}	–	1.5	–	V
Output Voltage High (I_{oh} = 0 mA, Voltage Mode)		FRxMC	V_{oh}	–	Rx PLL V_{CC} – 0.1	–	V
Output Voltage High (I_{oh} = 0 mA, Voltage Mode)		FTxMC	V_{oh}	–	Tx PLL V_{CC} – 0.1	–	V
Output Voltage Low (I_{ol} = 0 mA, Voltage Mode)		FRxMC FTxMC	V_{ol}	–	0.1	–	V
Output Current High (V_{oh} = 0.8 V, Current Mode)		FRxMC FTxMC	I_{oh}	–130	–100	–70	µA
Output Current Low (V_{ol} = 0.8 V, Current Mode)		FRxMC FTxMC	I_{ol}	70	100	130	µA
Maximum Input Frequency		FRx FTx	F_{max}	20	–	–	MHz
Input Voltage Swing		FRx FTx	V_{in}	200	–	1200	mVpp
Modulus Control Prop Delay	FRx FTx	FRxMC FTxMC	–	–	20	–	nS
LO2 PLL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode)							
Output Source Current (V_{PD} = 0.5 V or V_{CC} – 0.5 V) ±100 µA mode ±400 µA mode		LO2PD	I_{oh}	 –130 –520	 –100 –400	 –70 –280	µA
Output Sink Current (V_{PD} = 0.5 V or V_{CC} – 0.5 V) ±100 µA mode ±400 µA mode		LO2PD	I_{ol}	 70 280	 100 400	 130 520	µA
Current Match, ±100 µA mode or ±400 µA mode, V_{PD} = V_{CC} / 2 (i.e., 100 x (ABS (I_{oh} / I_{ol})))		LO2PD	Match	80	100	125	%

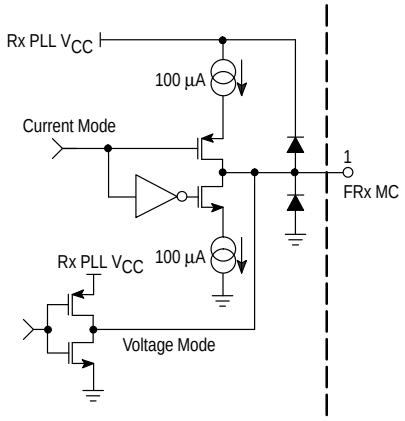
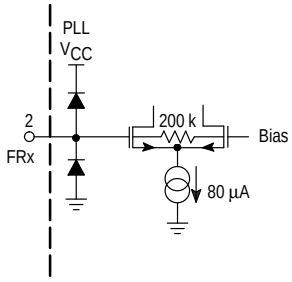
NOTES: 1. Values specified are pure numbers to the base 10.
2. Typical performance parameters indicate the potential of the device under ideal operating conditions.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode, Rx Gain = 01111, Vol Adj = 0111, f_{in} = 1.0 kHz, unless otherwise noted.)

Characteristics	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
LO2 PLL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode)							
Output Off Current (V_{PD} = V_{CC} /2)		LO2PD	I_{oz}	–80	5.0	80	nA
Input Current Low (V_{in} = 0.5 V)		LO2Ctl	I_{il}	–1.0	–0.02	–	µA
Input Current High (V_{in} = V_{CC} – 0.5 V)		LO2Ctl	I_{ih}	–	0.02	1.0	µA
Input Voltage Range		LO2Ctl	V_{range}	0.4	–	V_{CC}	V
Maximum 2nd LO Frequency				65	80	–	MHz
LO2 Out Drive (25 Ω load)			V_{out}	112	180	245	mVpp
COUNTERS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active Mode)							
12–Bit Reference Counter Range [Note 1]				–	3 to 4095	–	
13–Bit N Counter Range [Note 1]				–	3 to 8191	–	
7–Bit A Counter Range [Note 1] 64/65 Modulus Prescaler 128/129 Modulus Prescaler				 – –	 0 to 63 0 to 127	 – –	
14–Bit LO2 Counter Range [Note 1]				–	12 to 16383	–	
6–Bit Counters (for SCF) [Note 1]				–	3 to 63	–	

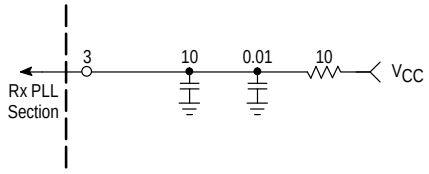
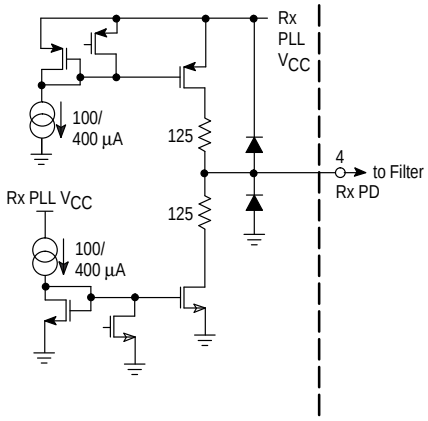
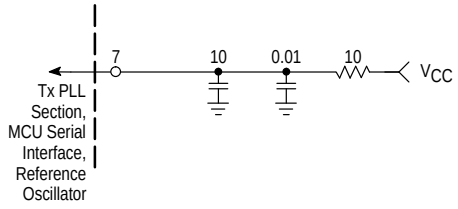
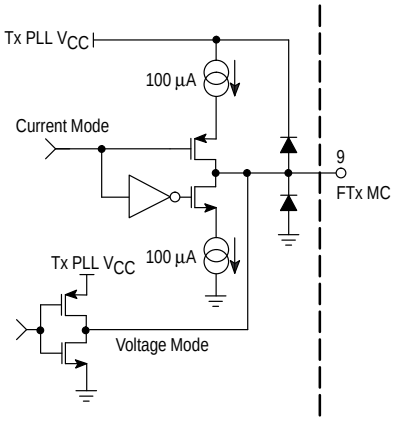
NOTES: 1. Values specified are pure numbers to the base 10.
2. Typical performance parameters indicate the potential of the device under ideal operating conditions.

PIN FUNCTION DESCRIPTION

Pin	Symbol/Type	Description	Description
1	FRx MC (Output)		Modulus Control Output for the Rx PLL section. Can be set to output in current mode or voltage mode, selectable with bit 3/16.
2	FRx (Input)		Receives the signal from the external 64/65 or 128/129 prescaler. DC bias is at 1.3 V.

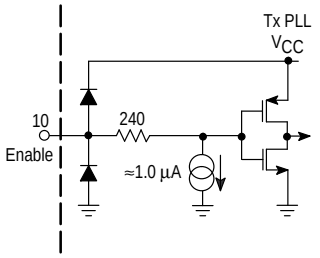
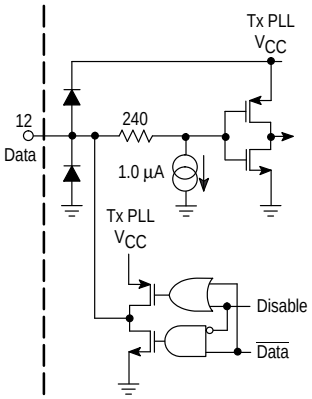
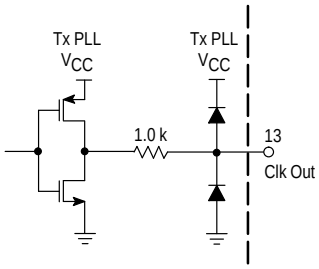
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
3	Rx PLL V_{CC} (Input)		Supply pin for the Rx PLL section. Allowable range is 2.7 to 5.5 V and must be within 0.5 V of all other V_{CC} pins. Good bypassing is required and isolation with a 10 Ω resistor is recommended.
4	Rx PD (Output)		Rx Phase Detector Output. The output either sources or sinks current, or neither, depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the PLL reference frequency are present. Output current is either ±100 µA or ±400 µA, selectable with bit 2/20.
5	PLL Gnd		Ground pin for the PLL section. A direct connection to a ground plane is strongly recommended.
6	Tx PD (Output)	Same as Pin 4, except powered from Tx PLL V_{CC}.	Tx Phase Detector Output. Description same as for Pin 4, except bit 1/20 controls the current level.
7	Tx PLL V_{CC} (Input)		Supply pin for the Tx PLL section, MCU Serial Interface, MCU Clock Counter, and the Reference Oscillator. Allowable range is 2.7 to 5.5 V and must be within 0.5 V of all other V_{CC} pins. Good bypassing is required and isolation with a 10 Ω resistor is recommended.
8	FTx (Input)	Same as Pin 2.	Receives the signal from the external 64/65 or 128/129 prescaler. DC bias is at 1.5 V.
9	FTx MC (Output)		Modulus Control Output for the Tx PLL section. Can be set to output in a current mode or a voltage mode, selectable with bit 3/16.

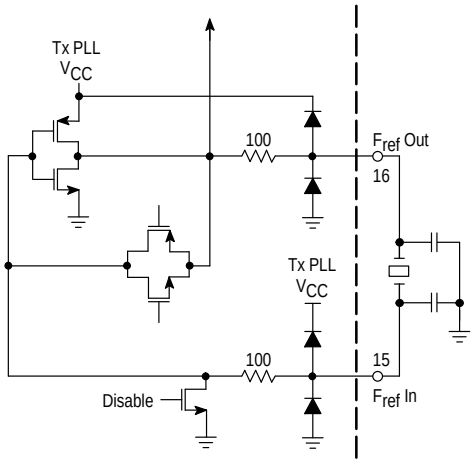
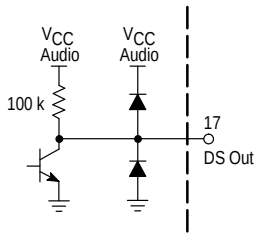
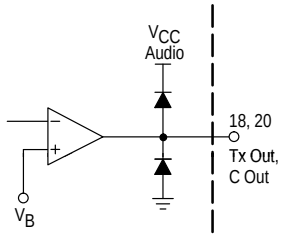
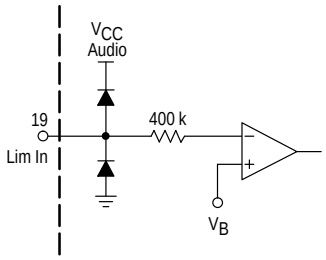
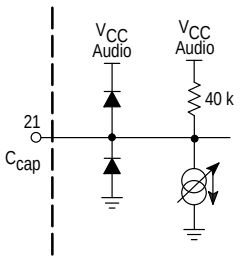
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
10	EN (Input)		Enable Input for the MCU Interface section. Hysteresis threshold is within 0.5 V of ground and V_{CC}. See text for proper waveform required at this pin.
11	CLK (Input)	Same as Pin 10.	Clock Input for the MCU Interface section. Hysteresis threshold is within 0.5 V of ground and V_{CC}. Data is written or read out on clock's rising edge. Maximum clock rate is 2.0 MHz.
12	Data (I/O)		Data I/O line for the MCU Interface section. Both address and data are provided to/from this pin. Input threshold is within 0.5 V of ground and V_{CC}. Data is written or read out on clock's rising edge.
13	MCU Clk Out (Output)		The microprocessor clock output is derived from the reference oscillator and a programmable divider with divide ratios of 2 to 312.5. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low–pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes. 1) For the MC33411A the Clk Out can be disabled via the MCU interface. 2) For the MC33411B this output is always active (on).
14	Gnd Digital		Ground for the Data, MCU Clk Out, and F_{ref} Out digital Outputs. A direct connection to the ground plane is strongly recommended.

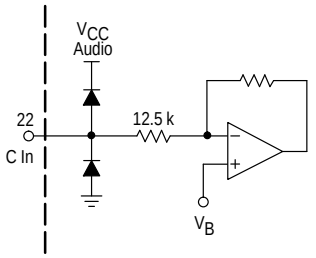
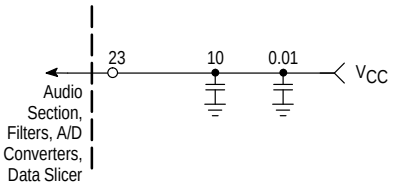
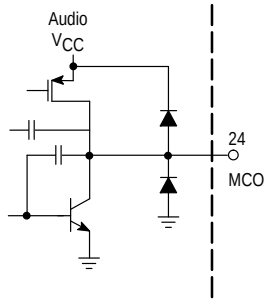
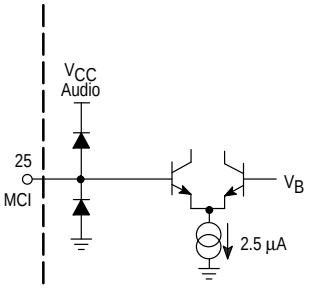
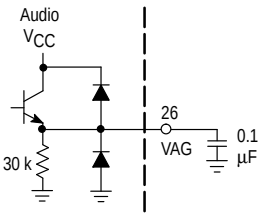
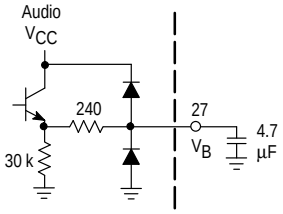
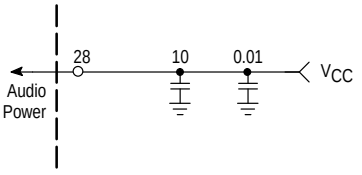
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
15, 16	F_{ref} In, F_{ref} Out		Reference Frequency Input for various portions of the circuit, including the PLLs, SCF clock, etc. A crystal (4 to 18.25 MHz) may be connected as shown, or an external frequency source may be capacitor coupled to Pin 15. See text for crystal requirements. 1) For the MC33411A the F_{ref} Out can be disabled via the MCU interface. 2) For the MC33411B this output is always active (on).
17	DS Out (Output)		Data Slicer Output (open collector with internal 100 kΩ pull–up resistor).
18	Tx Out (Output)		Tx Out is the Tx path audio output. Internally this pin has a low–pass filter circuitry with –3.0 dB bandwidth of 4.0 kHz. Tx gain and mute are programmable through the MCU interface. This pin is sensitive to load capacitance.
20	C Out (Output)		C Out is the compressor output.
19	Lim In (Input)		Lim In is the limiter input. This pin is internally biased and has an input impedance of 400 kΩ. Lim In must be ac–coupled.
21	C_{cap}		C_{cap} is the compressor rectifier filter capacitor pin. It is recommended that an external filter capacitor to V_{CC} audio be used. A practical capacitor range is 0.1 to 1.0 μF. The recommended value is 0.47 μF.

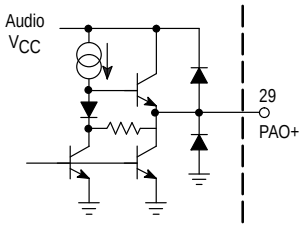
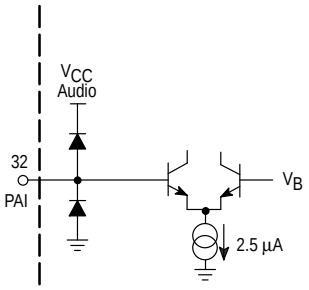
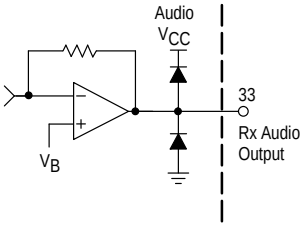
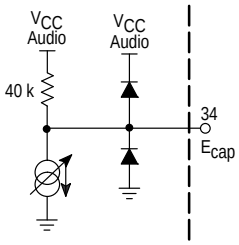
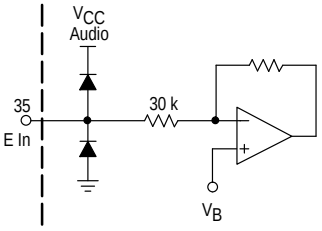
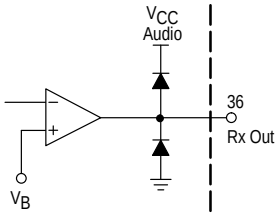
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
22	C In (Input)		C In is the compressor input. This pin is internally biased and has an input impedance of 12.5 kΩ. C In must be ac–coupled.
23	V_{CC} Audio (Input)		Supply input for the audio section, filters, A/D Converters, and Data Slicer. Allowable range is 2.7 to 5.5 V. Good bypassing is required.
24	MCO (Output)		Output of the Microphone amplifier. Maximum output swing is ≈3.0 V_{pp} for V_{CC} ≥ 3.0 V. Maximum output current is >1.0 mA peak.
25	MCI (Input)		Inverting input of the microphone amplifier. Gain and frequency response are set with external resistors and capacitors from this pin to the audio source and to MCO.
26	VAG (Output)		Analog ground for the audio section filters. VAG is equal to VB and is buffered from VB. Maximum current which can be sourced from this pin is 500 µA.
27	V_B (Output)		An internal 1.5 V reference for several sections. This voltage is adjustable with bits 3/20–17. Maximum source current is 100 µA. PSRR, noise and crosstalk depends on the external capacitor.
28	V_{CC} PA (Input)		Supply pin for the power amplifier outputs. Allowable range is 2.7 to 5.5 V. Good bypassing is required.

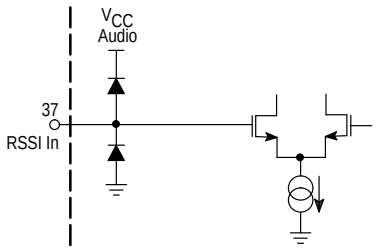
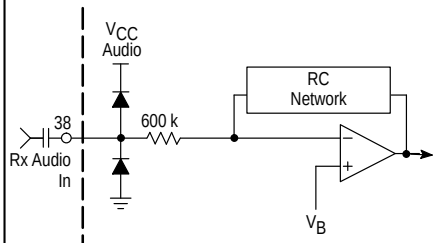
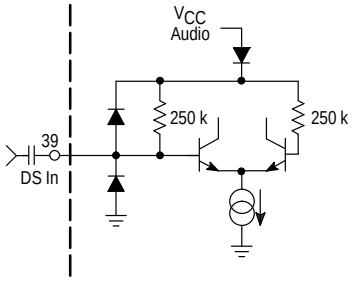
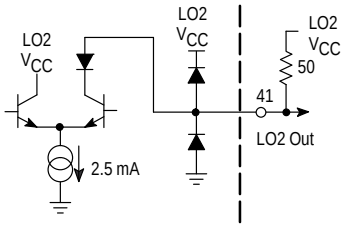
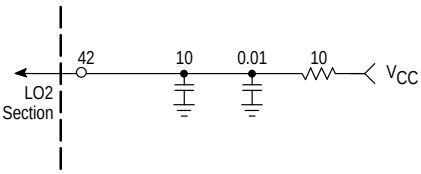
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
29	PAO+ (Output)		Output of the second power amplifier. This amplifier is set for unity inverting gain and is driven by PAO–. Maximum swing is 2.9 V_{pp} and maximum output current is >5.0 mA peak. DC level is ≈1.5 V.
30	PAO– (Output)	Same as Pin 29.	Output of the first power amplifier. Its gain is set with external resistors and capacitors from this pin to PAI. Output capability is the same as Pin 28.
31	Gnd PA		Ground pin for the power amplifier outputs. A direct connection to a ground plane is strongly recommended.
32	PAI (Input)		Inverting input of the power amplifier. Gain and frequency response are set with external resistors and capacitors from this pin to the audio source and to PAO–.
33	E Out (Output)		Expander output. This output is sensitive to load capacitance. Maximum output signal level is ≈2.5 V_{pp}. Maximum output current is >1.0 mA.
34	E_{cap}		E_{cap} is the expander rectifier filter capacitor pin. Connect an external filter capacitor between V_{CC} audio and E_{cap}. The recommended capacitance range is 0.1 to 1.0 µF. The suggested value is 0.47 µF.
35	E In (Input)		The expander input pin is internally biased and has input impedance of 30 kΩ.
36	Rx Out (Output)		Rx Out is the Rx audio output. An internal low–pass filter has a –3.0 dB bandwidth of 4.0 kHz.

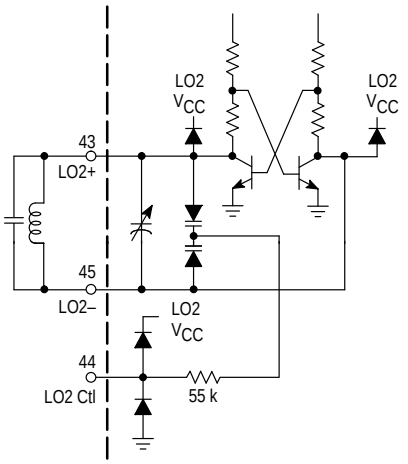
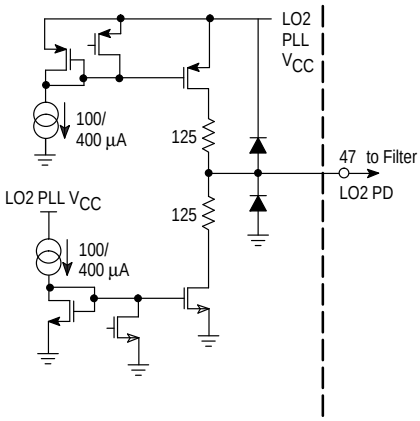
NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
37	RSSI In (Input)		Voltage input to RSSI A/D converter. Full scale is 0 to 1.6 V.
38	Rx Audio In (Input)		Input to the Rx Audio Path. Input impedance is 600 kΩ. Input signal must be capacitor coupled
39	DS In (Input)		Input for the digital data from the RF Receiver section. Input impedance is 250 kΩ. Hysteresis is internally provided. Input signal level must be between 50 and 700 mVpp.
40	Gnd Audio		Ground pin for the audio section. A direct connection to a ground plan is strongly recommended.
41	LO2 Out (Output)		Buffered output of the 2nd LO. This high frequency output is a current, requiring an external pullup resistor.
42	LO2 VCC (Input)		Supply pin for the LO2 section. Allowable range is 2.7 to 5.5 V and must be within 0.5 V of all other VCC pins. Good bypassing is required and isolation with a 10 Ω resistor is recommended.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol/Type	Description	Description
43, 45	LO2+, LO2–		The 2nd LO. External tank components are required. The internal capacitance across the pins is adjustable from 0 to 7.6 pF for fine tuning performance with bits 7/20–18.
44	LO2 Ctl (Input)		LO2 Control is the dc control input for this VCO. Typically it is the output of the low–pass filter fed from the phase detector output.
46	LO2 Gnd		Ground pin for the LO2 section. A direct connection to a ground plane is strongly recommended.
47	LO2PD (Output)		LO2 Phase Detector Output. The output either sources or sinks current, or neither, depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the PLL reference frequency are present. Output current is either ±100 µA or ±400 µA, selectable with bit 3/14.
48	LO2 Gnd		Ground pin for the LO2 section. A direct connection to a ground plane is strongly recommended.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

FUNCTIONAL DESCRIPTION

The following text, graphics, tables and schematics are provided to the user as a source of valuable technical information about the MC33411. This information originates from thorough evaluation of the device performance. This data was obtained by using units from typical wafer lots. It is important to note that the forgoing data and information was from a limited number of units. By no means is the user to assume that the data following is a guaranteed parametric. Only the minimum and maximum limits identified in the electrical characteristics tables found earlier in the spec are guaranteed.

Note: In the following descriptions, control bits in the MCU Serial Interface for the various functions will be identified by register number and bit number. For example, bit 3/19 indicates bit 19 of register 3. Bits 5/14–11 indicates register 5, bits 14 through 11. Please refer to Figure 1.

General Circuit Description

The MC33411A/B is a low power baseband IC designed to interface with the MC13145 UHF Wideband Receiver and MC13146 Transmitter for applications up to 2.0 GHz. The devices are primarily designated to be used for 900 MHz ISM band in a CT–900, low power, dual conversion cordless phone, but other applications such as data links with analog processing could be developed. This device contains complete baseband transmit and receive processing sections, a transmit and receive PLL section, a programmable PLL second local oscillator usable to 80 MHz, RSSI and low battery detect circuitry and serial interface for a microprocessor.

”A” versions of the device have the ability to disable either the reference oscillator or MCU clock outputs. This feature is useful for systems where the MCU has an internal clock, allowing the user to place the MC33411 into Inactive (lowest power consumption) mode. The ”A” version is also useful for systems where the MCU has a dedicated clock source, allowing for lower power consumption from the MC33411 by disabling the MCU clock output.

”B” versions of the device are intended for systems where the MCU clock will always be driven from the MC33411. These bits are purposefully ”hard–wired” to the enable state to ensure proper operation of the reference oscillator and MCU clock output even during battery discharge/recharge cycles.

All internal registers are completely static – no refreshing is required under normal operation conditions.

DC Current

Figures 2 through 5 are the current consumption for Inactive (MC33411 ”A” version only), Standby, Receive, and Active modes versus supply voltages. Figures 6 and 7 show the typical behavior of current consumption in relation to temperature.

Figure 8 illustrates the effect of the MCU clock output frequency to supply current during Active mode.

Figure 2. Supply Current versus Supply Voltage (Inactive Mode)

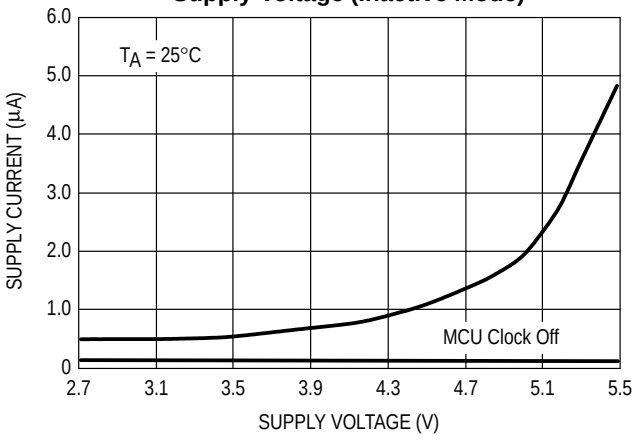


Figure 3. Supply Current versus Supply Voltage (Standby Mode)

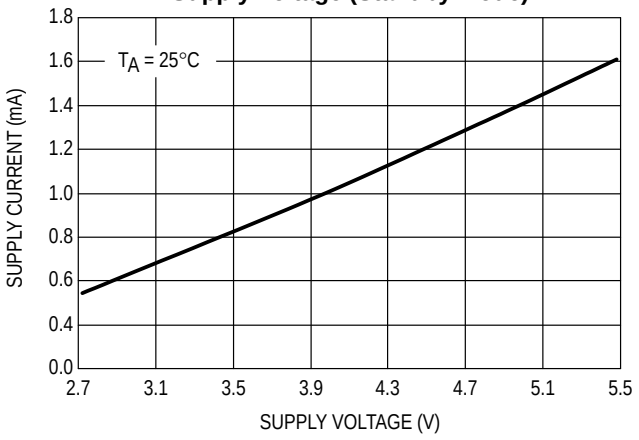


Figure 4. Supply Current versus Supply Voltage (Receive Mode)

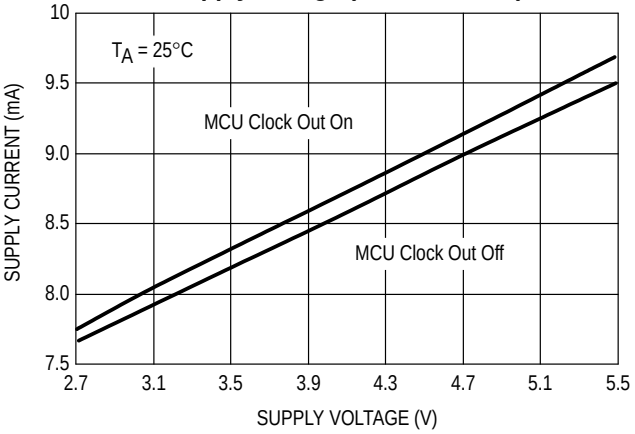


Figure 5. Supply Current versus Supply Voltage (Active Mode)

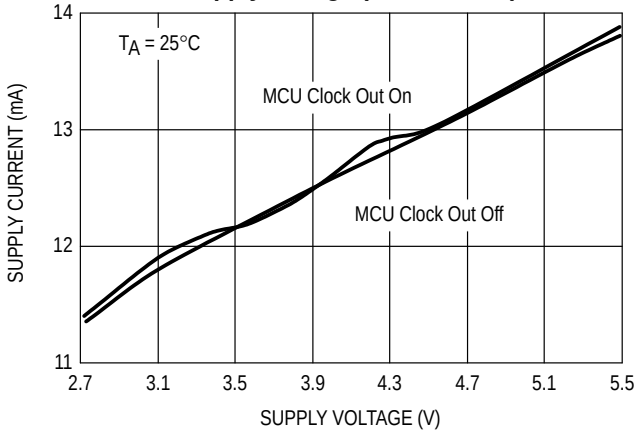


Figure 6. Supply Current versus Temperature Normalized to 25°C (Standby Mode)

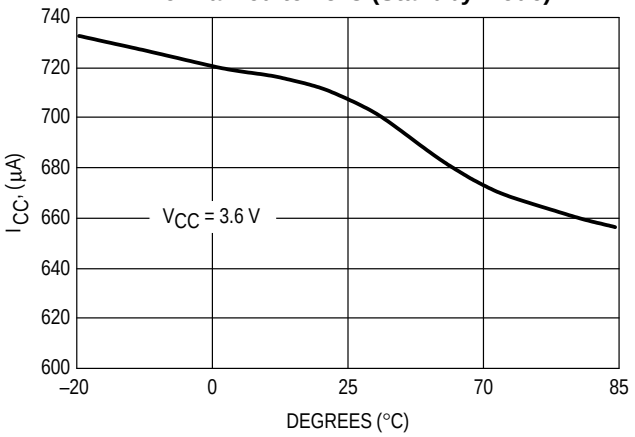


Figure 7. Supply Current versus Temperature Normalized to 25°C (Receive & Active Mode)

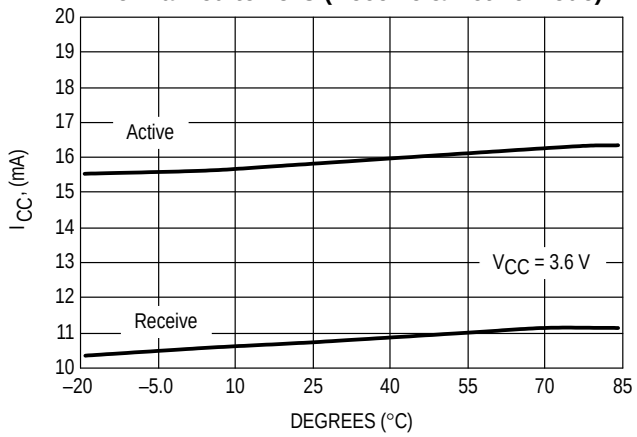


Figure 8. Supply Current versus MCU Clock Output Frequency (Active Mode)

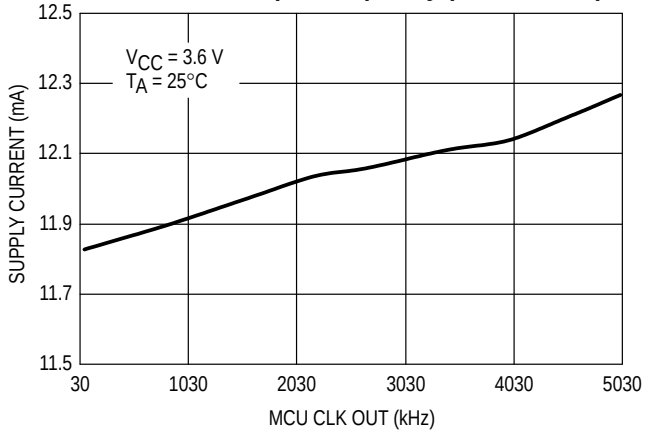


Table 1. Tx Gain Adjust Programming (Register 7)

Gain Control Bit #9	Gain Control Bit #8	Gain Control Bit #7	Gain Control Bit #6	Gain Control Bit #5	Gain Ctl #	Gain/Attenuation Amount
					<6	–9.0 dB
0	0	1	1	0	6	–9.0 dB
0	0	1	1	1	7	–8.0 dB
0	1	0	0	0	8	–7.0 dB
0	1	0	0	1	9	–6.0 dB
0	1	0	1	0	10	–5.0 dB
0	1	0	1	1	11	–4.0 dB
0	1	1	0	0	12	–3.0 dB
0	1	1	0	1	13	–2.0 dB
0	1	1	1	0	14	–1.0 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1.0 dB
1	0	0	0	1	17	2.0 dB
1	0	0	1	0	18	3.0 dB
1	0	0	1	1	19	4.0 dB
1	0	1	0	0	20	5.0 dB
1	0	1	0	1	21	6.0 dB
1	0	1	1	0	22	7.0 dB
1	0	1	1	1	23	8.0 dB
1	1	0	0	0	24	9.0 dB
1	1	0	0	1	25	10 dB
–	–	–	–	–	>25	10 dB

Transmit Speech Processing System

This portion of the audio path goes from ”Tx Audio” to ”Tx Out”. The gain of the microphone amplifier is set with external resistors to receive the audio from the microphone hybrid or any other audio source. The MCO output has rail–to–rail capability. The ”Tx Audio” pin will be ac–coupled. The audio transmit signal path includes automatic level control (ALC) (also referred to as the Compressor), Tx mute, limiter, filters, and Tx gain adjust. The ALC provides ”soft” limiting to the output signal swing as the input voltage slowly increases. With this technique the gain is slightly lowered to help reduce distortion of the audio signal. The limiter section provides hard limiting due to rapidly changing singal levels, or transients. The ALC, TX mute, and limiter functions can be enabled or disabled vis the MCU serial interface. The Tx gain adjust can also be remotely controlled to set different desired signal levels.

The adjustable gain stage provides 20 levels of gain in 1.0 dB increments. It is controlled with bits 7/9–5 as shown in Table 1. The effect of the gain setting under various ALC/Limiter On/Off settings is shown in Figure 9.

The Low–Pass Filter before the gain stage is a switched capacitor filter with a corner frequency at 3.7 kHz. This frequency is dependent upon the SCF clock, nominaly set to 165 kHz and is directly proportional to the SCF clock. The filter response for inband, ripple, wideband, as well as phase and group delay, are shown in Figures 10 through 14.

The mute switch at Pin 18 will mute a minimum of 60 dB. Bit 6/2 controls the mute. The limiter can be disabled by programming a logic 1 into 6/5.

The compressor with ALC transfer characteristic is shown in Figure 15. The ALC gain is controlled by bits 6/11–12. If both bits are programmed to a logic 0, the ALC gain is set to 5.0 dB. If bit 6/11 is set to a logic 1, the ALC gain will be set to 10 dB, whereas if bit 6/12 is set to a logic 1 the ALC gain will be 25 dB. The ALC function may be disabled by programming a logic 1 into bit 6/6.

The compressor low maximum gain can be set with bit 6/8. Programming this bit to a logic 0 sets the maximum gain to 23 dB. A lower maximum gain, nominally 13.5 dB, is achieved by programming the bit to a logic 1. The entire compressor can be bypassed (i.e., 0 dB) by programming bit 6/4 to a logic 1.

Figures 16 through 22 describe the characteristics of the compressor, ALC, and limiter.

Figure 9. Tx Audio Output Voltage versus Gain Control Setting

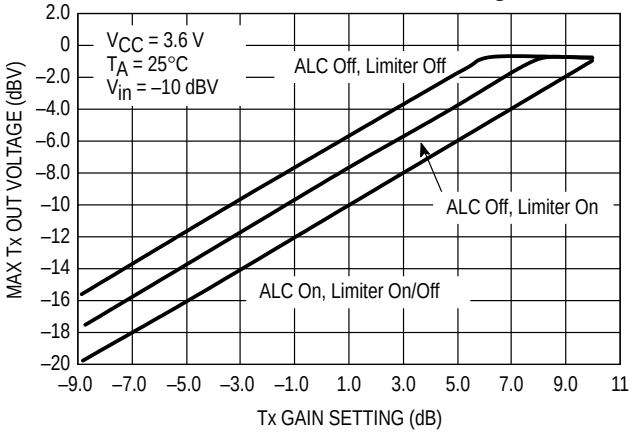


Figure 10. Lim In to Tx Out Gain versus Frequency (Inband)

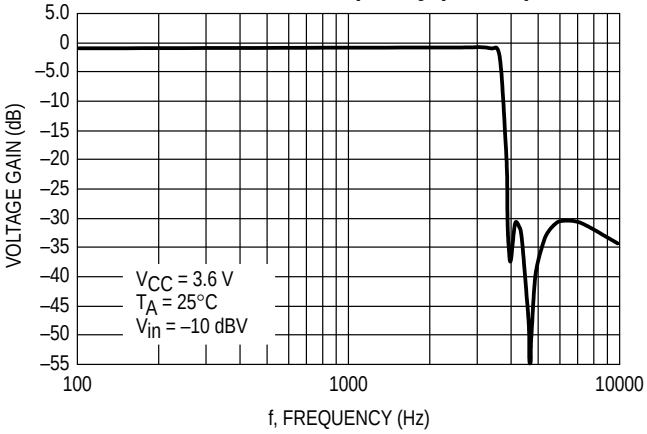


Figure 11. Lim In to Tx Out Gain versus Frequency (Ripple)

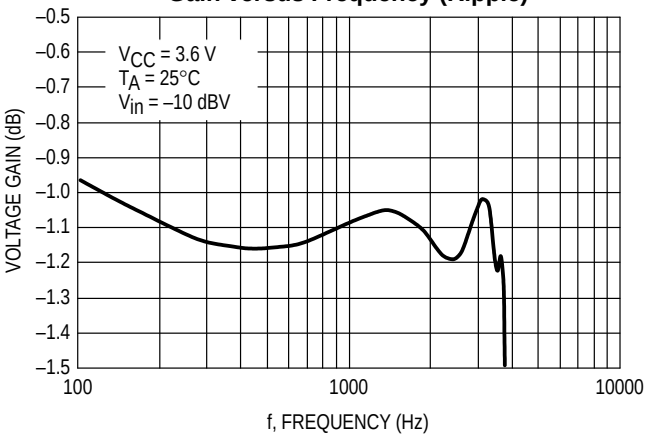


Figure 12. Lim In to Tx Out Gain versus Frequency (Wideband)

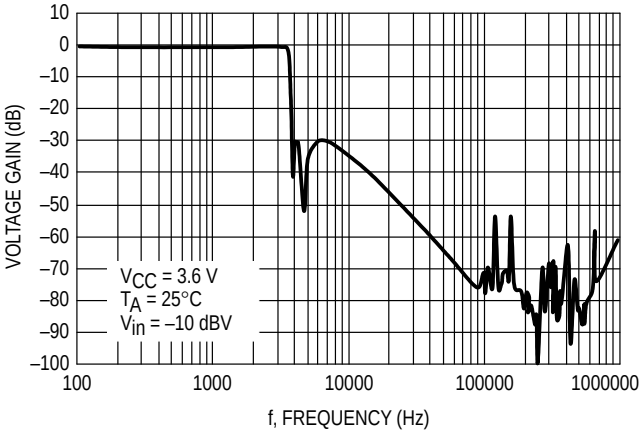


Figure 13. Lim In to Tx Out Phase versus Frequency

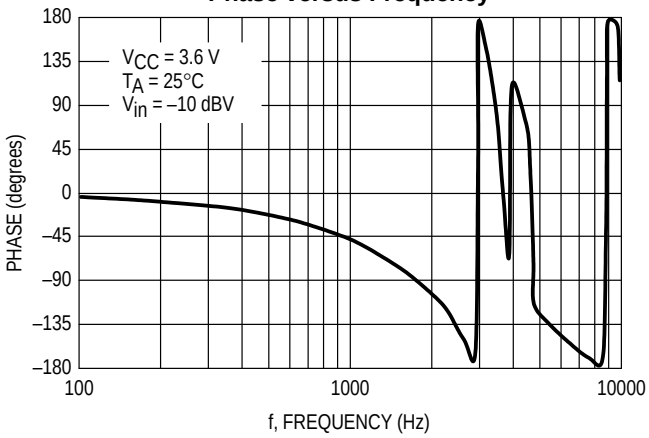


Figure 14. Lim In to Tx Out Group Delay versus Frequency

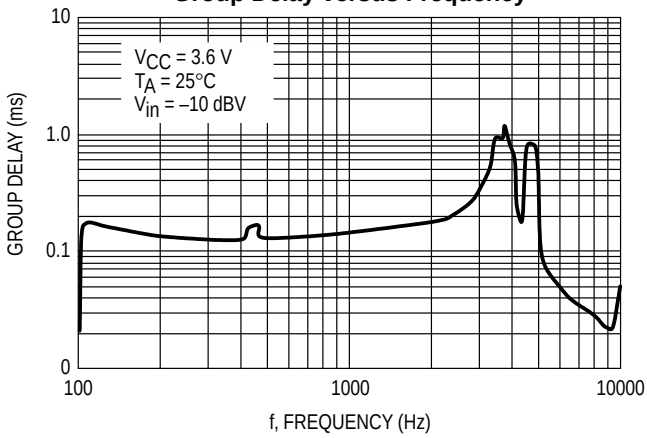


Figure 15. Compressor Characteristic with Programmable Compressor Maximum Gain

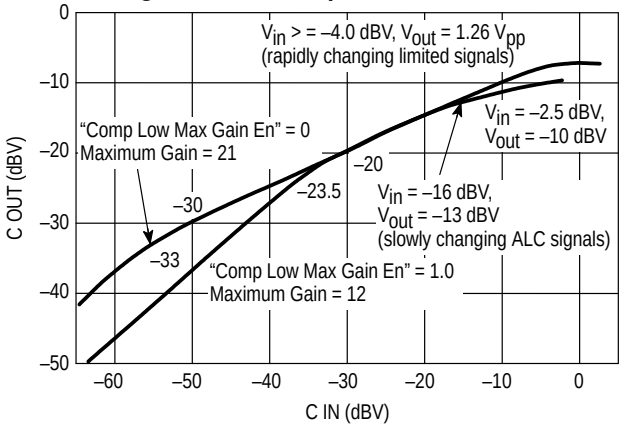


Figure 16. Tx Audio Compressor Response (Distortion & Amplitude, ALC off, Lim off)

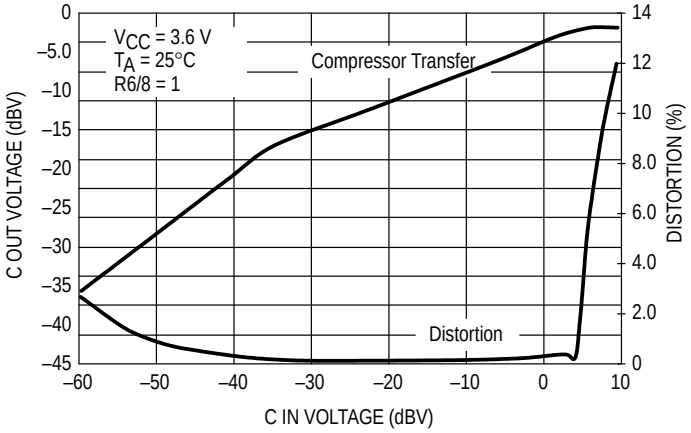


Figure 17. Tx Audio Compressor Response (Distortion & Amplitude, ALC off, Lim off)

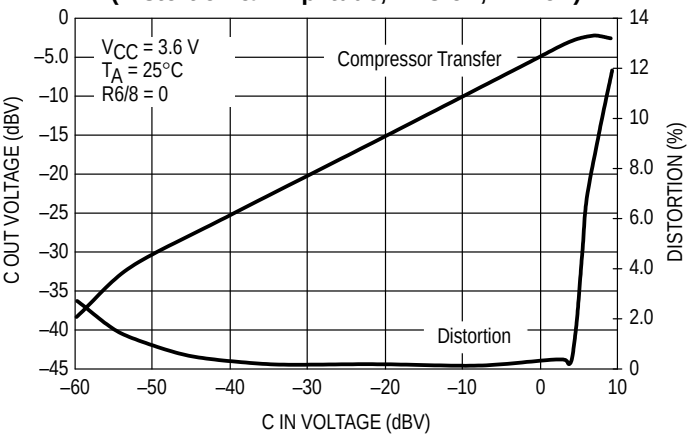


Figure 18. Tx Output Audio Response (Lim & ALC off)

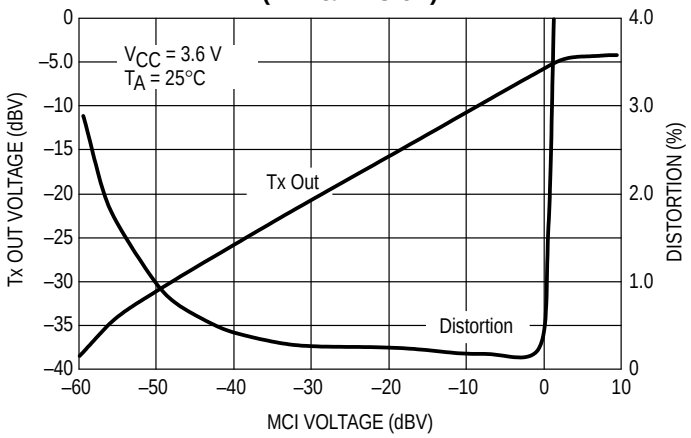


Figure 19. Tx Output Audio Response (Lim on, ALC off)

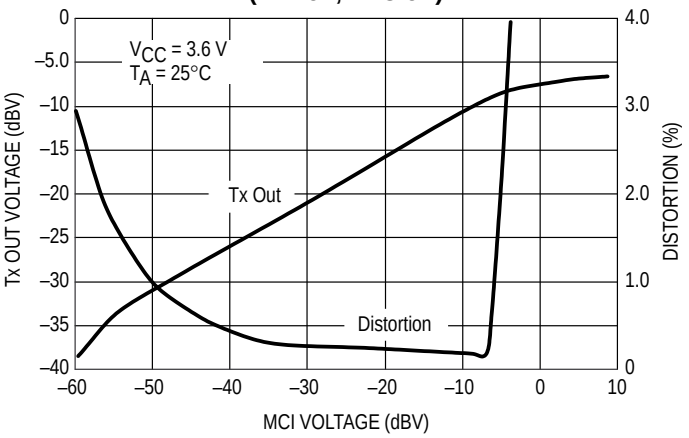


Figure 20. Tx Output Audio Response (Lim off, ALC on)

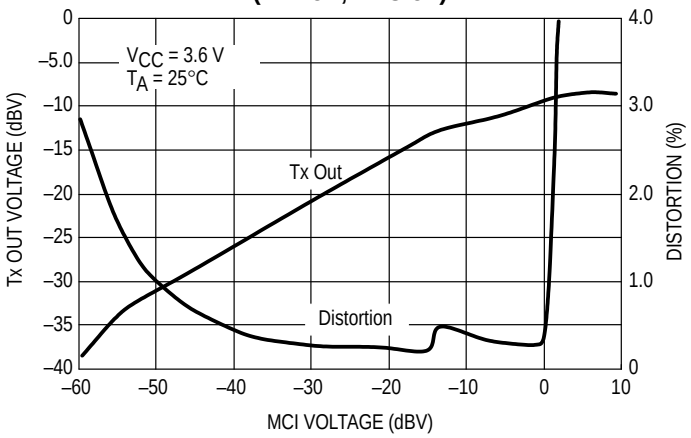


Figure 21. Tx Output Audio Response (Lim off, R6/11 = 1)

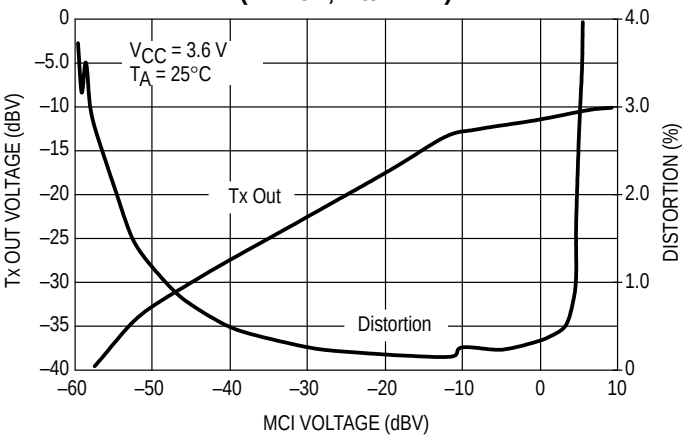
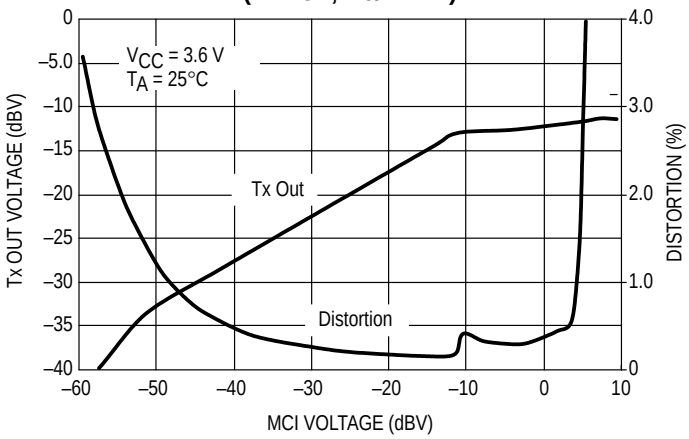


Figure 22. Tx Output Audio Response (Lim off, R6/12 = 1)



Data Slicer

The data slicer will receive the low level digital signal from the RF receiver section at Pin 39. The input signal to the data slicer must be >200 mVpp. Hysteresis of 40 mV is internally provided. The output of the data slicer will be same waveform, but with an amplitude of 0 to V_{CC}, and can be observed at Pin 17 if bits 5/9–8 are set to 00. The output can be inverted by setting bit 5/9 = 1. The data slicer can be disabled by setting bit 5/8 = 1.

Receive Audio Path

The Receive Audio Path (Pins 38, 36–33) consists of an anti–aliasing filter, a low–pass filter, side tone attenuator, gain adjust stage, a mute switch, expander and volume control.

The switched capacitor low–pass filter is an 8 pole filter, with a corner frequency at 3.8 kHz. This is designed to provide bandwidth limiting in the audio range.

The gain stage provides 20 dB of gain adjustment in 1.0 dB steps, measured from Pin 38 to 36. Bits 7/4–0 are used to set the gain according to Table 3. The mute switch, controlled by bit 6/1, will mute a minimum of 60 dB.

When the compressor output is within 3.0 dB of the expander input level, the Rx output (Pin 36) can be attenuated (referenced to the expander output) by bits 6/10–9. For 6/10–9 = 00, the attenuation is 0 dB. For the other combinations, 6/10–9 = 01, attenuation = 3.0 dB; 6/10–9 = 10, attenuation = 6.0 dB; and 6/10–9 = 11, attenuation = 10.4 dB (See Table 2).

The expander can be bypassed by setting bit 6/3 = 1.

Table 3 shows the various gain control settings which can be accessed in Register 7. Table 4 is the volume control settings, also located in Register 7.

Figures 23 through 31 illustrate the various characteristics of the reveive audio path.

Table 2. Side Tone Attenuate Programming

Side Tone Attenuate Bit #1	Side Tone Attenuate Bit #0	Select #	Side Tone Attenuate Amount at Expander Input	Side Tone Attenuate Amount at Expander Output
0	0	0	0 dB	0 dB
0	1	1	1.5 dB	3.0 dB
1	0	2	3.0 dB	6.0 dB
1	1	3	5.2 dB	10.4 dB

Table 3. Rx Gain Adjust Programming (Register 7)

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Ctl #	Gain/Attenuation Amount
–	–	–	–	–	<6	–9.0 dB
0	0	1	1	0	6	–9.0 dB
0	0	1	1	1	7	–8.0 dB
0	1	0	0	0	8	–7.0 dB
0	1	0	0	1	9	–6.0 dB
0	1	0	1	0	10	–5.0 dB
0	1	0	1	1	11	–4.0 dB
0	1	1	0	0	12	–3.0 dB
0	1	1	0	1	13	–2.0 dB

Table 3. Rx Gain Adjust Programming (Register 7) (continued)

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Ctl #	Gain/Attenuation Amount
0	1	1	1	0	14	–1.0 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1.0 dB
1	0	0	0	1	17	2.0 dB
1	0	0	1	0	18	3.0 dB
1	0	0	1	1	19	4.0 dB
1	0	1	0	0	20	5.0 dB
1	0	1	0	1	21	6.0 dB
1	0	1	1	0	22	7.0 dB
1	0	1	1	1	23	8.0 dB
1	1	0	0	0	24	9.0 dB
1	1	0	0	1	25	10 dB
–	–	–	–	–	>25	10 dB

Table 4. Volume Control Programming

Volume Control Bit #13	Volume Control Bit #12	Volume Control Bit #11	Volume Control Bit #10	Volume Ctl #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Figure 23. Rx Out Maximum Output Voltage versus Gain Control Setting

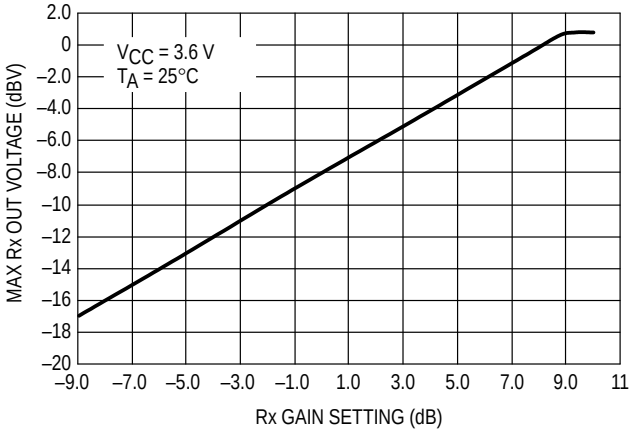


Figure 24. E Out Maximum Output Voltage versus Volume Control Setting

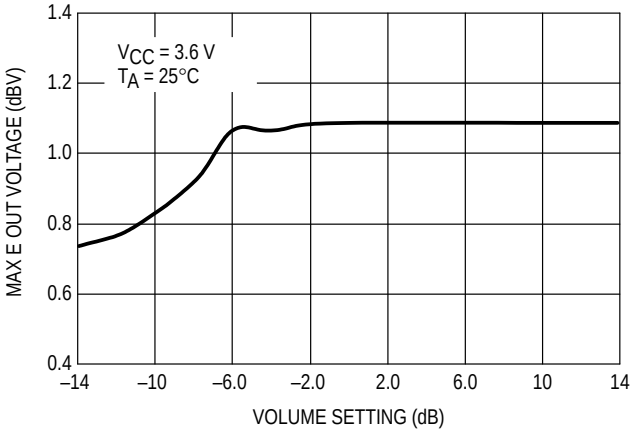


Figure 25. Rx Audio In to Rx Out Gain versus Frequency (Inband)

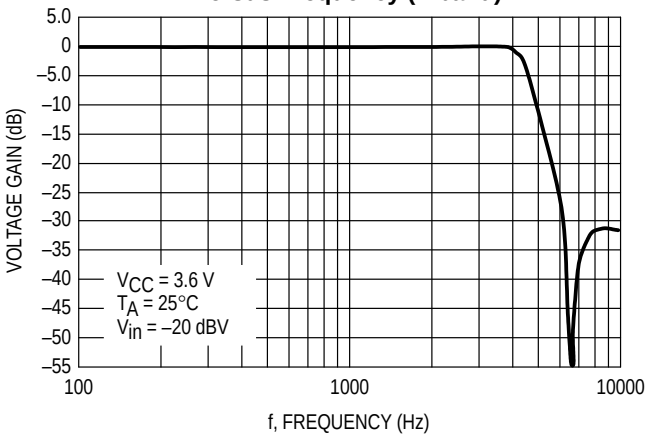


Figure 26. Rx Audio In to Rx Out Gain versus Frequency (Ripple)

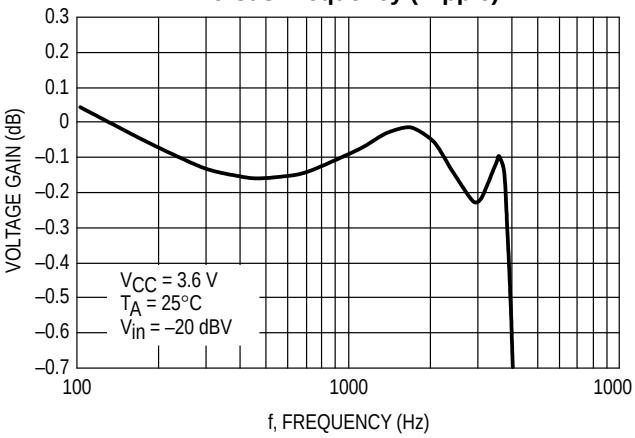


Figure 27. Rx Audio In to Rx Out Gain versus Frequency (Wideband)

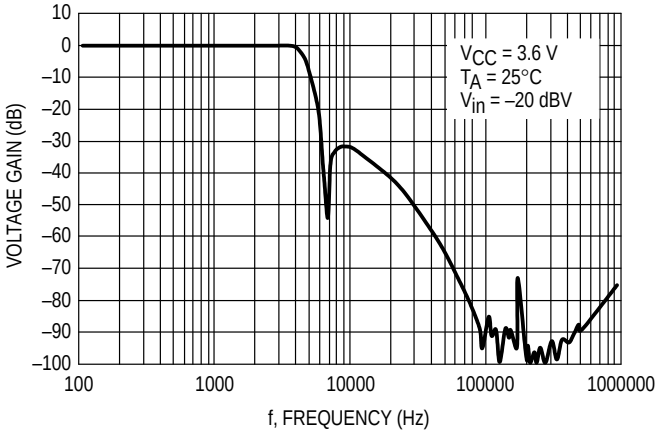


Figure 28. Rx Audio In to Rx Out Phase versus Frequency

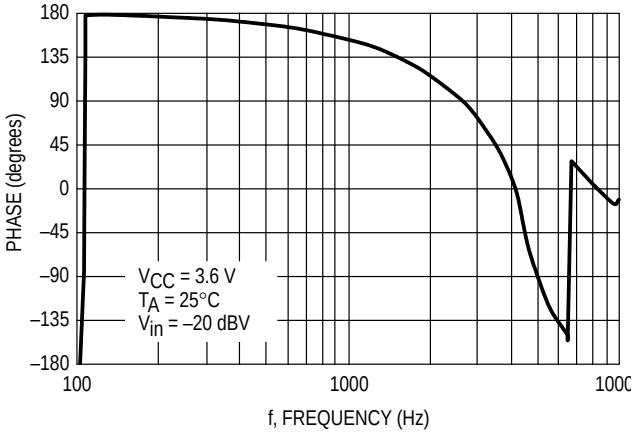


Figure 29. Rx Audio In to Rx Out Group Delay versus Frequency

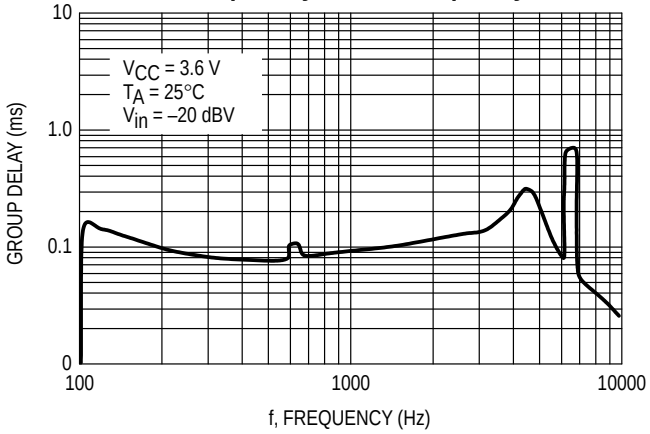


Figure 30. AALPF Response Gain versus Frequency

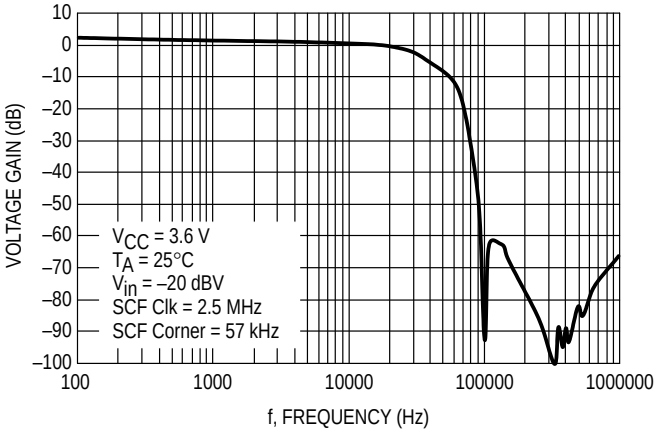
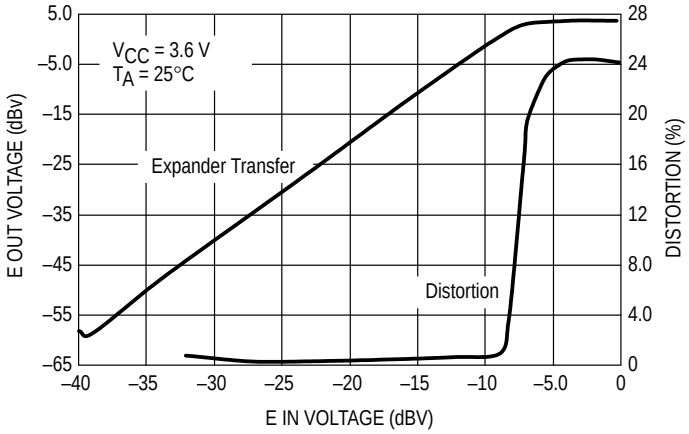


Figure 31. E In to E Out Transfer Curve



Power Amplifiers

The power amplifiers (Pins 29, 30, 32) are designed to drive the earpiece in a handset, or the telephone line via a hybrid circuit in the base unit. Each output (PAO+ and PAO–) can source and sink 5.0 mA, and can swing 1.3 V_{pp} each. For high impedance loads, each output can swing 2.7 V_{pp} (5.4 V_{pp} differential). The gain of the amplifiers is set with a feedback resistor from Pin 30 to 32, and an input resistor at Pin 32. The differential gain is 2x the resistor ratio. Capacitors can be used for frequency shaping. The pins' dc level is VB (≅1.5 V).

The Mute switch, controlled with bit 6/0, will provide 60 dB of muting with a 50 kΩ feedback resistor. The amount of muting will depend on the value of the feedback resistor.

Figures 32 and 33 show the power amplifier swing/distortion for V_{CC} = 3.6 V, and Figure 34 illustrates the maximum swing capability for various value of V_{CC}.

Figure 32. Power Amplifier Maximum Output Swing

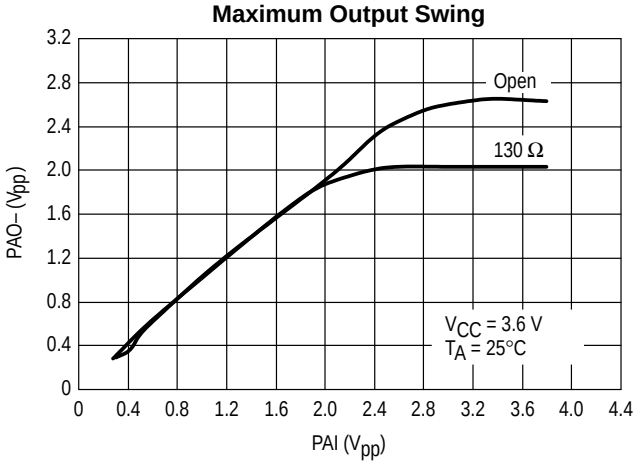


Figure 33. Power Amplifier Distortion

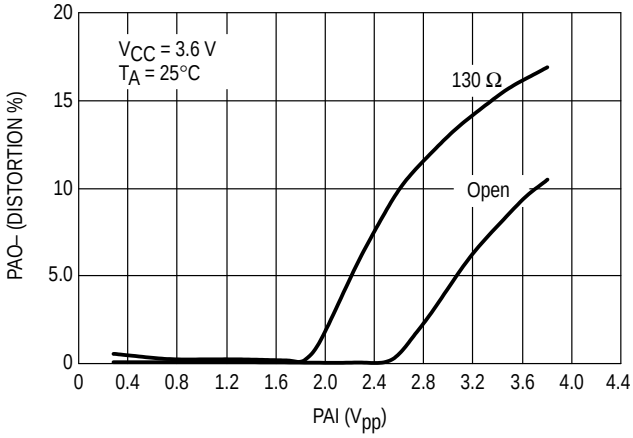
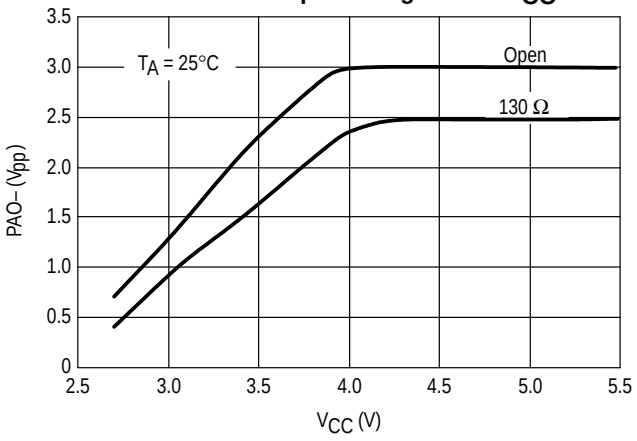


Figure 34. Power Amplifier Maximum Output Swing versus V_{CC}



Reference Oscillator/MCU Clk Out

The reference oscillator provides the frequency basis for the three PLLs, the switched capacitor filters, and the MCU clock output. The source for the reference clock can be a crystal in the range of 4.0 to 18.25 MHz connected to Pins 15 & 16, or it can be an external source connected to F_{ref} In (Pin 15). The reference frequency is directed to:

a. A programmable 12–bit counter (register bits 4/11–0) to provide the reference frequency for the three PLLs. The 12–bit counter is to be set such that, in conjunction with the programmable counters within each PLL, the proper frequencies can be produced by each VCO.

b. A programmable 6–bit counter (register bits 4/17–12), followed by a ÷2 stage, to set the frequency for the switched capacitor filters to 165 kHz, or as close to that as possible.

c. A programmable 3–bit counter (register bits 7/16–14) which provides the MCU clock output (see Tables 5 and 6).

A representation of the reference oscillator is given by Figures 35 and 36.

Figure 35. Reference Oscillator Schematic

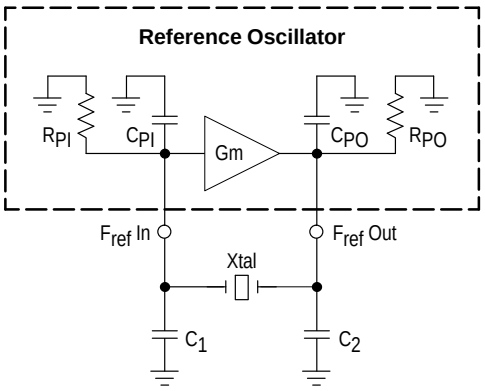


Figure 36. Reference Oscillator Input and Output Impedance

Input Impedance (R_{PI} // C_{PI})	11.6 kΩ // 2.9 pF
Output Impedance (R_{PO} // C_{PO})	4.5 kΩ // 2.5 pF

Figures 37 and 38 show a typical gain/phase response of the oscillator. Load capacitance (C_L), equivalent series resistance (ESR), and even supply voltage will have an effect on the oscillator response as shown in Figures 39 and 40. It should be noted that optimum performance is achieved when C1 equals C2 (C1/C2 = 1).

Figure 41 represents the ESR versus crystal load capacitance for the reference oscillator. This relationship was defined by using a 6.0 dB minimum loop gain margin at 3.6 V. This is considered the minimum gain margin to guarantee oscillator start–up.

Oscillator start–up is also significantly affected by the crystal load capacitance selection. In Figure 39, the relationship between crystal load capacitance and ESR can be seen. The lower the load capacitance the better the performance.

Given the desired crystal load capacitance, C1 and C2 can be determined from Figure 42. It should also be pointed out that current consumption increases when C1 ≠ C2.

Be careful not to overdrive the crystal. This could cause a noise problem. An external series resistor on the crystal output can be added to reduce the drive level, if necessary.

Figure 37. Reference Oscillator Open Loop Gain versus Frequency

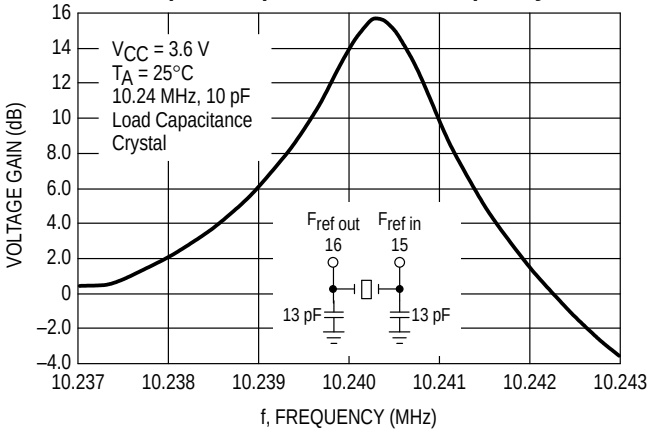


Figure 38. Reference Oscillator Open Loop Phase versus Frequency

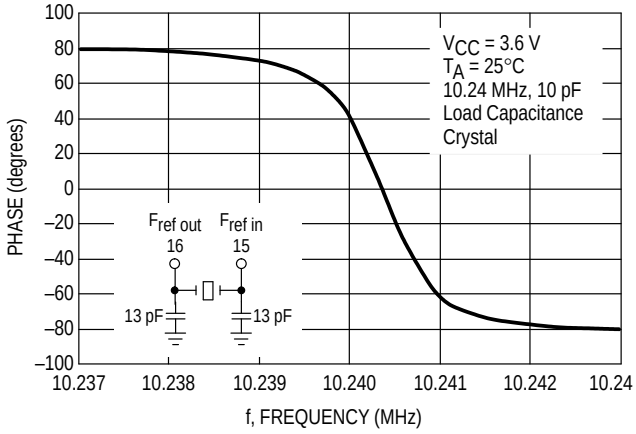


Figure 39. Reference Oscillator Startup Time versus Total ESR – Inactive to Rx Mode

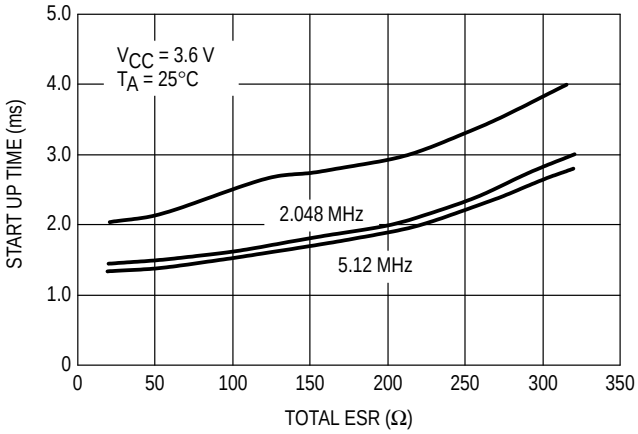


Figure 40. Reference Oscillator Open Loop Gain versus ESR

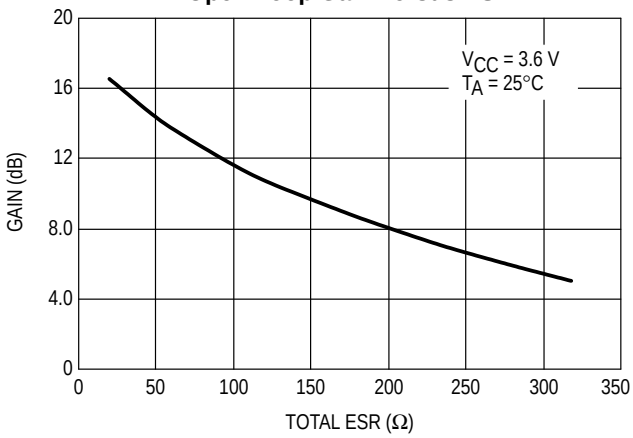


Figure 41. Maximum ESR versus Crystal Load Capacitance (C1 = C2)

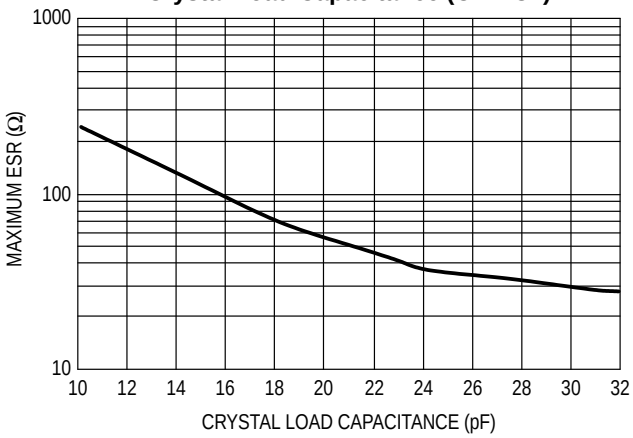


Figure 42. Optimum Values for C1, C2 versus Equivalent Required Parallel Capacitance

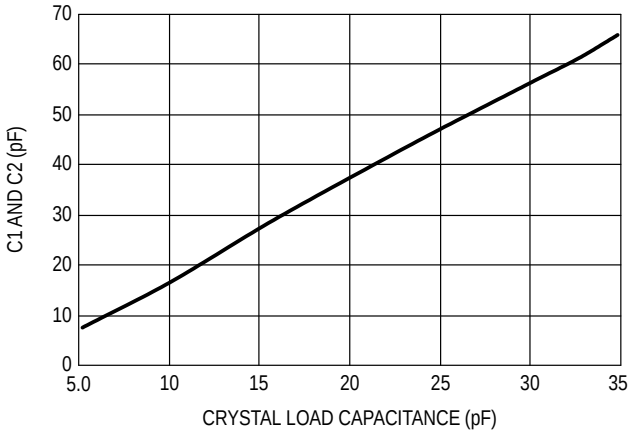


Table 5. MCU Clock Divider Programming

MCU Clk Bit #16	MCU Clk Bit #15	MCU Clk Bit #14	Clk Out Divider Value
0	0	0	2.0
0	0	1	3.0
0	1	0	4.0
0	1	1	5.0
1	0	0	2.5
1	0	1	20
1	1	0	80
1	1	1	312.5

Table 6. MCU Clock Divider Frequencies

Crystal Frequency	Clock Output Divider							
	2.0	2.5	3.0	4.0	5.0	20	80	312.5
10.24 MHz	5.12 MHz	4.096 MHz	3.413 MHz	2.56 MHz	2.048 MHz	512 kHz	128 kHz	32.768 kHz
11.15 MHz	5.575 MHz	4.46 MHz	3.717 MHz	2.788 MHz	2.23 MHz	557 kHz	139 kHz	35.68 kHz
12 MHz	6.0 MHz	4.8 MHz	4.0 MHz	3.0 MHz	2.4 MHz	600 kHz	150 kHz	38.4 kHz

Transmit and Receive (LO1) PLL Sections

The transmit and receive PLLs (Pins 6–9 and 1–4, respectively) are designed to be part of a 900 MHz system. In a typical application the Transmit PLL section will be set up to generate the transmit frequency, and the Receive PLL section will be set up to generate the LO1 frequency. The two sections are identical, and function independently. External requirements for each include a low–pass filter, a 900 MHz VCO, and a 64/65 or 128/129 dual modulus prescaler.

The frequency output of the VCO is to be reduced by the dual modulus prescaler, and then input to the MC33411 (at Pin 8 or 2). That frequency is then further reduced by the programmable 13–bit counter (bits 1/19–7 or 2/19–7), and provided to one side of the Phase Detector, where it is compared with the PLL reference frequency. The output of the phase detector (at Pin 6 or 4) is a Three–State charge pump which drives the VCO through the low–pass filter. Bits 1/20 and 2/20 set the gain of each of the two charge pumps to either 100/2π μA/radian or 400/2π μA/radian. The polarity of the two phase detector outputs is set with bits 1/21 and 2/21. If the bit = 0, the appropriate PLL is configured to operate with a non–inverting low–pass filter/VCO combination. If the low–pass filter/VCO combination is inverting, the polarity bit should be set to 1.

The 7–bit A and A' counters (bits 1/6–0 and 2/6–0) are to be set to drive the Modulus Control input of the 64/65 or 128/129 dual modulus prescalers. The Modulus Control outputs (Pins 9 and 1) can be set to either a voltage mode (logic 1) or a current mode (logic 0) with bit 3/16.

To calculate the settings of the N and A registers, the following procedure is used:

$$\frac{f_{VCO}}{f_{PLL}} = Nt \text{ (Nt must be an integer)} \quad \textbf{(1)}$$

$$\frac{Nt}{P} = N \quad \textbf{(2)}$$

A = Remainder of Equation 2 (decimal part of N x P) **(3)**

where: f_{VCO} = the VCO frequency
f_{PLL} = the PLL Reference Frequency set within the MC33411
P = the smaller divisor of the dual modulus prescaler (64 for a 64/65 prescaler)
N = the whole number portion is the setting for the N (or N') counter within the MC33411
A = the setting for the A (or A') counter within the MC33411

For example, if the VCO is to provide 910 MHz, and the internal PLL reference frequency is 50 kHz, then the equations yield:

$$Nt = \frac{910 \times 10^6}{50 \times 10^3} = 18,200$$

$$N = \frac{18,200}{64} = 284.375$$

$$A = 0.375 \times 64 = 24$$

The N register setting is 284 (0 0001 0001 1100), and the A register setting is 24 (001 1000).

2nd LO (LO2)

This PLL is designed to be the 2nd Local Oscillator in a typical 900 MHz system, and is designed for frequencies up to 80 MHz. The VCO and varactor diodes are included, and are to be used with an external tank circuit (Pins 43–45).

Bits 4/20–18 are used to select an internal capacitor, with a value in the range of 0 to 7.6 pF, to parallel the varactor diodes and the tank's external capacitor. This permits a certain amount of fine tuning of the oscillator's performance. See Table 7.

A buffered output is provided to drive, e.g., a mixer. The frequency is set with the programmable 14–bit counter (bits 3/13–0) in conjunction with the PLL reference frequency. For example, if the reference frequency is 50 kHz, and the 2nd LO frequency is to be 63.3 MHz, the 14–bit counter needs to be set to 1266_d (00 0100 1111 0010). The output level is dependent on the value of the impedance at Pin 41, partly determined by the external pull–up resistor.

The output of the phase detector is a Three–State charge pump which drives the varactor diodes through an external low–pass filter. Bit 3/14 sets the gain of the charge pump to either $100/2\pi$ μA/radian (logic 0) or $400/2\pi$ μA/radian (logic 1). Bit 3/15 sets its polarity – if 0, the PLL is configured to operate with a non–inverting low–pass filter/VCO combination. If the low–pass filter/VCO combination is inverting, the polarity bit should be set to 1. Please note that the 2nd LO VCO on the MC33411 is of the non–inverting type. Figures 43 through 45 describe the response of the 2nd LO.

Table 7. LO2 Capacitor Select Programming

LO2 Capacitor Select Bit #20	LO2 Capacitor Select Bit #19	LO2 Capacitor Select Bit #18	Select #	LO2 Capacitor Select Value
0	0	0	0	0 pF
0	0	1	1	1.1 pF
0	1	0	2	2.2 pF
0	1	1	3	3.3 pF
1	0	0	4	4.3 pF
1	0	1	5	5.4 pF
1	1	0	6	6.5 pF
1	1	1	7	7.6 pF

Figure 43. Varicap Capacitance versus Control Voltage

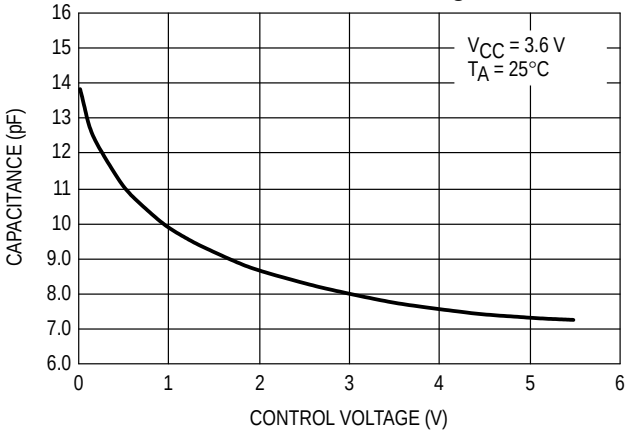


Figure 44. Minimum Overall Q versus Coil Inductance for LO2

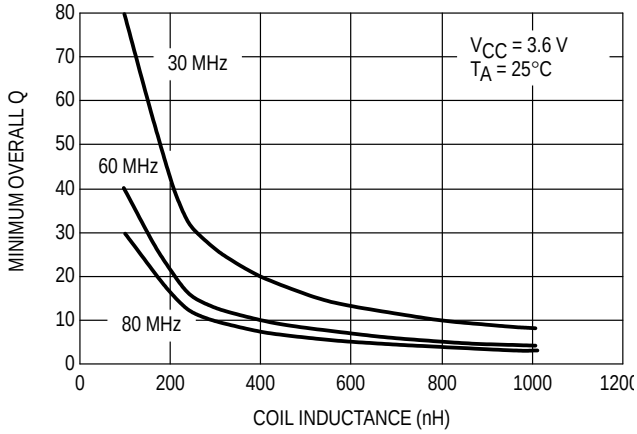
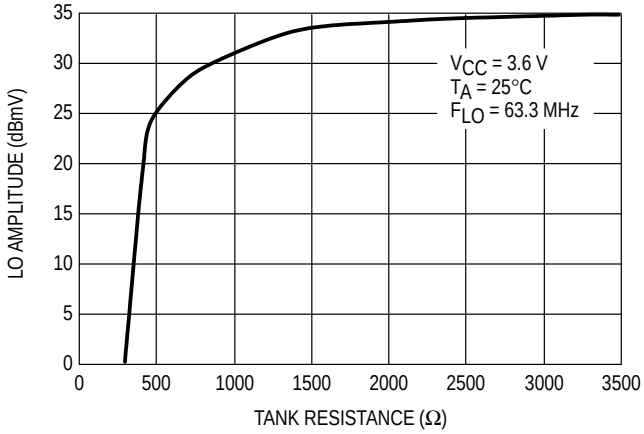


Figure 45. LO2 Amplitude versus Overall Tank Parallel Resistance

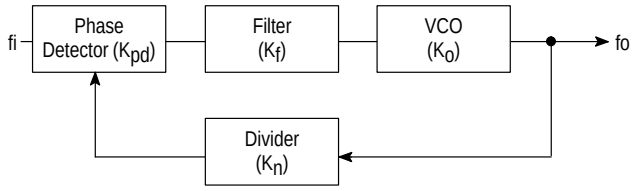


Loop Filter Characteristics

Let's consider the following discussion on loop filters. The fundamental loop characteristics, such as capture range, loop bandwidth, lock–up time, and transient response are controlled externally by loop filtering.

Figure 46 is the general model for a Phase Lock Loop (PLL).

Figure 46. PLL Model



Where:

K_{pd} = Phase Detector Gain Constant
K_f = Loop Filter Transfer Function
K_o = VCO Gain Constant
K_n = Divide Ratio (N)
fi = Input frequency
fo = Output frequency
fo/N = Feedback frequency divided by N

From control theory the loop transfer function can be represented as follows:

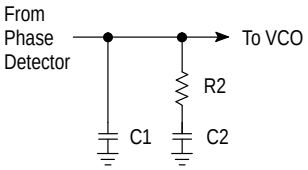
$$A = \frac{K_{pd}\ K_f\ K_o}{K_n} \quad \text{Open loop gain}$$

K_{pd} can be either expressed as being 200 μA/4π or 800 μA/4π. More details about performance of different type PLL loops, refer to Motorola application note AN535.

The loop filter can take the form of a simple low pass filter. A current output, type 2 filter will be used in this discussion since it has the advantage of improved step response, velocity, and acceleration.

The type 2 low pass filter discussed here is represented as follows:

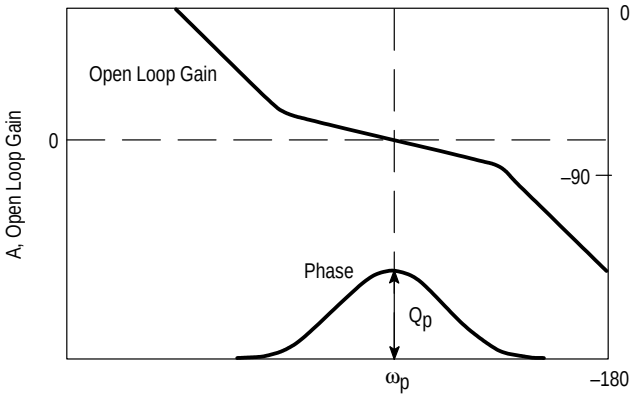
Figure 47. Loop Filter with Additional Integrating Element



From Figure 47, capacitor C1 forms an additional integrator, providing the type 2 response, and filters the discrete current steps from the phase detector output. The function of the additional components R2 and C2 is to create a pole and a zero (together with C1) around the 0 dB point of the open loop gain. This will create sufficient phase margin for stable loop operation.

In Figure 48, the open loop gain and the phase is displayed in the form of a Bode plot. Since there are two integrating functions in the loop, originating from the loopfilter and the VCO gain, the open loop gain response follows a second order slope (–40 dB/dec) creating a phase of –180 degrees at the lower and higher frequencies. The filter characteristic needs to be determined such that it is adding a pole and a zero around the 0 dB point to guarantee sufficient phase margin in this design (Qp in Figure 48).

Figure 48. Bode Plot of Gain and Phase in Open Loop Condition



The open loop gain including the filter response can be expressed as:

$$A_{openloop} = \frac{K_{pd}K_o(1 + j\omega(R2C2))}{j\omega K_n\left(j\omega\left(1 + j\omega\left(\frac{R2C1C2}{C1+C2}\right)\right)\right)} \quad \textbf{(4)}$$

The two time constants creating the pole and the zero in the Bode plot can now be defined as:

$$T1 = \frac{R2C1C2}{C1 + C2} \qquad T2 = R2C2 \quad \textbf{(5)}$$

By substituting equation (5) into (4), it follows:

$$A_{openloop} = \left(\frac{K_{pd}K_oT1}{\omega^2C1K_nT2}\right)\left(\frac{1 + j\omega T2}{1 + j\omega T1}\right) \quad \textbf{(6)}$$

The phase margin (phase + 180) is thus determined by:

$$Q_p = \arctan(\omega T2) – \arctan(\omega T1) \quad \textbf{(7)}$$

At $\omega=\omega_p$, the derivative of the phase margin may be set to zero in order to assure maximum phase margin occurs at ω_p (see also Figure 48). This provides an expression for ω_p:

$$\frac{dQ_p}{d\omega} = 0 = \frac{T2}{1 + (\omega T2)^2} – \frac{T1}{1 + (\omega T1)^2} \quad \textbf{(8)}$$

$$\omega = \omega_p = \frac{1}{\sqrt{T2T1}} \quad \textbf{(9)}$$

Or rewritten:

$$T1 = \frac{1}{\omega_p{}^2T2} \quad \textbf{(10)}$$

By substituting into equation (7), solve for T2:

$$T2 = \frac{\tan\left(\frac{Q_p}{2} + \frac{\pi}{4}\right)}{\omega_p} \quad \textbf{(11)}$$

By choosing a value for ω_p and Q_p, T1 and T2 can be calculated. The choice of Q_p determines the stability of the loop. In general, choosing a phase margin of 45 degrees is a good choice to start calculations. Choosing lower phase margins will provide somewhat faster lock–times, but also generate higher overshoots on the control line to the VCO. This will present a less stable system. Larger values of phase margin provide a more stable system, but also increase lock–times. The practical range for phase margin is 30 degrees up to 70 degrees.

The selection of ω_p is strongly related to the desired lock–time. Since it is quite complicated to accurately calculate lock time, a good first order approach is:

$$T\_lock \approx \frac{3}{\omega_p} \quad \textbf{(12)}$$

Equation (12) only provides an order of magnitude for lock time. It does not clearly define what the exact frequency difference is from the desired frequency and it does not show the effect of phase margin. It assumes, however, that the phase detector steps up to the desired control voltage without hesitation. In practice, such step response approach is not really valid. If the two input frequencies are not locked, their phase maybe momentarily zero and force the phase detector into a high impedance mode. Hence, the lock times may be found to be somewhat higher.

In general, ω_p should be chosen far below the reference frequency in order for the filter to provide sufficient attenuation at that frequency. In some applications, the reference frequency might represent the spacing between channels. Any feedthrough to the VCO that shows up as a spur might affect adjacent channel rejection. In theory, with the loop in lock, there is no signal coming from the phase detector. But in practice small current pulses and leakage currents will be supplied to both the VCO and the phase detector. The external capacitors may show some leakage, too. Hence, the lower ω_p, the better the reference frequency is filtered, but the longer it takes for the loop to lock.

As shown in Figure 48, the open loop gain at ω_p is 1 (or 0 dB), and thus the absolute value of the complex open loop gain as shown in equation (6) solves C1:

$$C1 = \left(\frac{K_{pd}K_oT1}{\omega^2K_nT2}\right)\sqrt{\frac{\left(1+\omega_pT2\right)^2}{\left(1+\omega_pT1\right)^2}} \quad \textbf{(13)}$$

With C1 known, and equation (5) solve C2 and R2:

$$C2 = C1\left(\frac{T2}{T1} - 1\right) \quad \textbf{(14)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(15)}$$

The VCO gain is dependent on the selection of the external inductor and the frequency required. The free running frequency of the VCO is determined by:

$$f = \frac{1}{2\pi\sqrt{LC_T}} \quad \textbf{(16)}$$

In which L represents the external inductor value and C_T represents the total capacitance (including internal capacitance) in parallel with the inductor. The VCO gain can be easily calculated via the internal varicap transfer curve shown in Figure 43.

As can be derived from Figure 43, the varicap capacitance changes 2.0 pF over the voltage range from 1.0 V to 3.0 V:

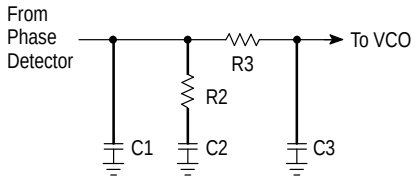
$$\Delta Cvar = \frac{2.0\ pF}{2.0\ V} \quad \textbf{(17)}$$

Combining (16) with (17) the VCO gain can be determined by:

$$K_O = \frac{1}{j2.0V}\left\{\frac{1}{2\pi\sqrt{LC_T}} - \frac{1}{2\pi\sqrt{L\left(C_T + \frac{\Delta Cvar}{2}\right)}}\right\} \quad \textbf{(18)}$$

Although the basic loopfilter previously described provides adequate performance for most applications, an extra pole may be added for additional reference frequency filtering. Given that the channel spacing is based on the reference frequency, and any feedthrough to the first LO may effect parameters like adjacent channel rejection and intermodulation. Figure 49 shows a loopfilter architecture incorporating an additional pole.

Figure 49. Loop Filter with Additional Integrating Element



For the additional pole formed by R3 and C3 to be efficient, the cut–off frequency must be much lower than the reference frequency. However, it must also be higher than ω_p in order not to compromise phase margin too much. The following equations were derived in a similar manner as for the basic filter previously described.

Similarly, it can be shown:

$$A_{openloop} = -\frac{K_{pd}K_o}{K_n\omega^2\left((C1 + C2 + C3) - \omega^2 C1C2C3R2R3\right)} + \frac{1 + j\omega T2}{1 + j\omega T1} \quad \textbf{(19)}$$

In which:

$$T1 = \frac{(C1 + C2)T2 + (C1C2)T3}{C1 + C2 + C3 - \omega^2 C1T2T3} \quad \textbf{(20)}$$

$$T2 = R2C2 \quad \textbf{(21)} \qquad T3 = R3C3 \quad \textbf{(22)}$$

From T1 it can be derived that:

$$C2 = \frac{(T1 + T2)C3 - C1\left(T2 + T3 - T1 + \omega^2 T1T2T3\right)}{T3 - T1} \quad \textbf{(23)}$$

In analogy with (13), by forcing the loopgain to 1 (0 dB) at ω_p, we obtain:

$$C1(T1 + T2) + C2T3 + C3T2 = \left(\frac{K_{pd}K_o}{K_n\omega_p{}^2}\right)\sqrt{\frac{1 + \left(\omega_p T2\right)^2}{1 + \left(\omega_p T1\right)^2}} \quad \textbf{(24)}$$

Solving for C1:

$$C1 = \frac{(T2 - T1)T3C3 - (T3 - T1)T2C3 + (T3 - T1)\left(\frac{K_{pd}K_oT1}{\omega_p{}^2K_n}\right)\sqrt{\frac{1+\left(\omega_p T2\right)^2}{1+\left(\omega_p T1\right)^2}}}{(T3 - T1)T2 + (T3 - T1)T3 - \left(T2 + T3 - T1 + \omega_p{}^2T1T2T3\right)T3} \quad \textbf{(25)}$$

By selecting ω_p via (12), the additional time constant expressed as T3, can be set to:

$$T3 = \frac{1}{K\omega_p} \quad \textbf{(26)}$$

The K–factor shown determines how far the additional pole frequency will be separated from ω_p. Selecting too small of a K–factor, the equations may provide negative capacitance or resistor values. Too large of a K–factor may not provide the maximum attenuation.

By selecting R3 to be 100 kΩ, C3 becomes known and C1 and C2 can be solved from the equations. By using equations (11) and (10), time constants T2 and T1 can be derived by selecting a phase margin. Finally, R2 follows from T2 and C2.

A test circuit with the following components and conditions was constructed with these results:

Loop Filter (See Figure 49):
- C1 = 470 pF
- R2 = 68 kΩ
- C2 = 3.9 nF
- R3 = 270 kΩ
- C3 = 82 pF

LO2 Tank:
- Ctotal = 39.3 pF
- Lext = 150 nH, Q = 50 @ 250 MHz
- Reference Frequency = 10.24 MHz (unadjusted)
- R Counter = 205
- LO2 Counter = 1266
- AC Load = 25 Ω
- Frequency of LO2 = 63.258 MHz
- Phase Noise @ 50 kHz offset = –107 dBc
- Sidebands @ 50 kHz & 100 kHz offsets = –69 dBc

Low Battery/ RSSI Voltage Measurement

Both the Low Battery (bits 5/23–18) and RSSI (bits 5/17–12) measurement circuits have a 6–bit A/D converter whose value may be read back via the SPI. The A/D's sample their voltages at a frequency equal to the internal SCF clock frequency divided by 128. The Low Battery Measurement A/D senses and divides by 2.5 the supply voltage (at Pin 23). Please note that the minimum Low Battery Detect (LBD) voltage is 2.7 V, since there is no guarantee that the device will operate below this value. The RSSI Measurement senses the voltage at Pin 37.

These values are compared to the internal reference VB (≈1.5 V) which is available at Pin 37. The value read back from the LBD A/D will therefor be approximately:

$$N(\text{for LBD}) \approx \frac{63\ (V_{CC})}{2.5(VB)(1.07)} \quad \textbf{(27)}$$

and for the RSSI

$$N(\text{for RSSI}) \approx \frac{63\ (\text{RSSIVoltage})}{(VB)(1.07)} \quad \textbf{(28)}$$

VB Voltage Adjust and Characteristics

VB has a production tolerance of ±8%, and can be adjusted over a ±9% range using bits 3/20–17. The adjustment steps will be ≈1.2% each (See Table 8). If desired, VB can be used to bias external circuitry, as long as the load current on this pin does not exceed 10 μA. V_B varies by less than ±0.5% over supply voltage, referenced to V_{CC} = 3.6 V.

The value of the de–coupling capacitor connected from VB to ground affects both the noise and crosstalk from the receive and transmit audio paths, so the value should be chosen with caution. Figures 50 and 51 show this relationship.

Table 8. VB Voltage Reference Programming

V_{ref} Adjust Bit #20	V_{ref} Adjust Bit #19	V_{ref} Adjust Bit #18	V_{ref} Adjust Bit #17	V_{ref} Adjust #	Voltage Reference Adjustment Amount
0	0	0	0	0	–9.0%
0	0	0	1	1	–7.8%
0	0	1	0	2	–6.6%
0	0	1	1	3	–5.4%
0	1	0	0	4	–4.2%
0	1	0	1	5	–3.0%
0	1	1	0	6	–1.8%
0	1	1	1	7	–0.6%
1	0	0	0	8	0.6%
1	0	0	1	9	1.8%
1	0	1	0	10	3.0%
1	0	1	1	11	4.2%
1	1	0	0	12	5.4%
1	1	0	1	13	6.6%
1	1	1	0	14	7.8%
1	1	1	1	15	9.0%

Figure 50. Crosstalk/Noise from C In to E Out versus VB Capacitor

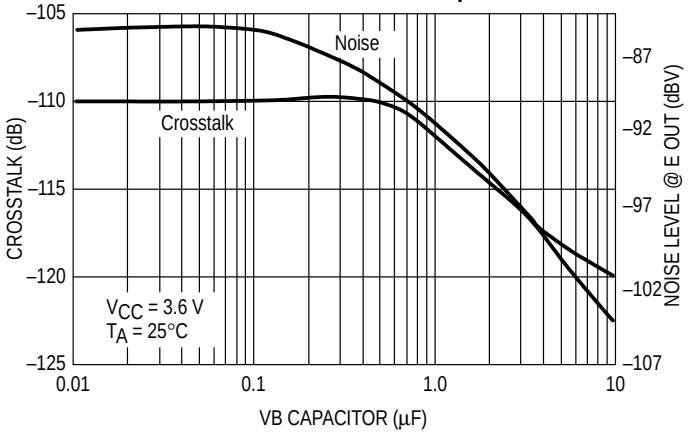
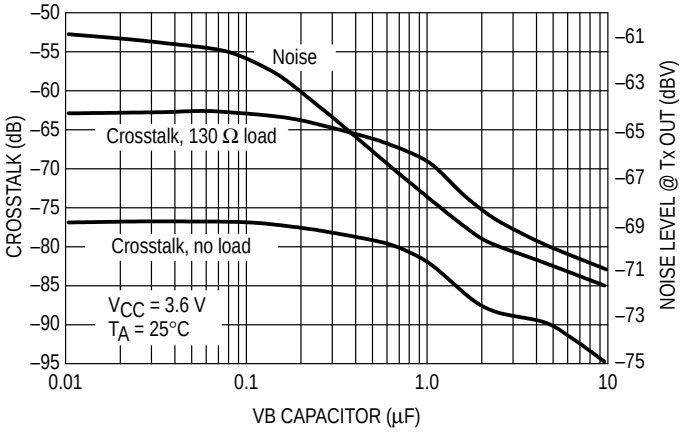


Figure 51. Crosstalk/Noise from E In to Tx Out versus VB Capacitor



MCU Serial Interface

The MCU Serial Interface is a 3–wire interface, consisting of a Clock line, an Enable line, and a bi–directional Data line. The interface is always active, i.e., it cannot be powered down as all other sections of the MC33411 are disabled and enabled through this interface.

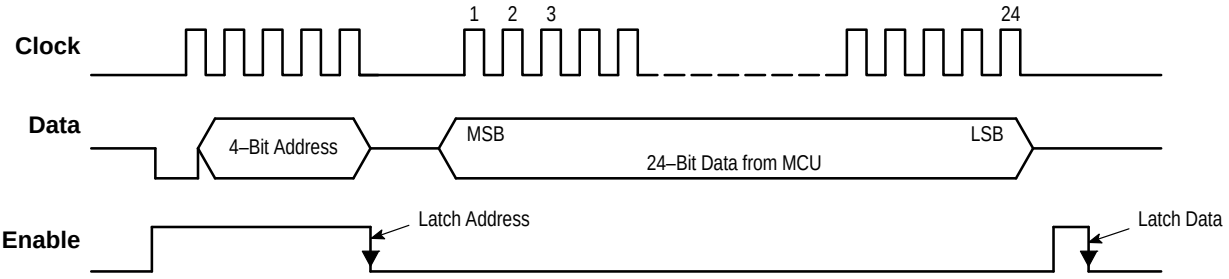
After the device power–up (or whenever a reset condition is required), the MCU should perform the following steps:

1. Initialize the Data line to a high impedance state.
2. Initialize the Clock line to a logic low.
3. Initialize the Enable line to a logic low.
4. Pulse the Clock line a minimum of once (RZ format) while leaving the Enable line continuously low. This places the SPI port into a known condition.
5. Load all registers with their desired initial values.

The clock (Return–to–Zero format) must be supplied to the MC33411 at Pin 11 to write or read data, and can be any frequency up to 2.0 MHz. The clock need not be present when data is not being transferred. The Enable line must be low when data is not being transferred.

Internally there are 7 data registers, 24–bits each, addressed with 4–bits ranging from $h1 to $h7 (see Tables 9 and 10). Register 5, bits 23–12 are read–only bits, while all other register bits are Read/Write. All unused/unimplemented bits are reserved for Motorola use only. The contents of the 7 registers can be read out at any time. All bits are written in, or read out, on the clock's positive transition. The write and read operations are as follows:

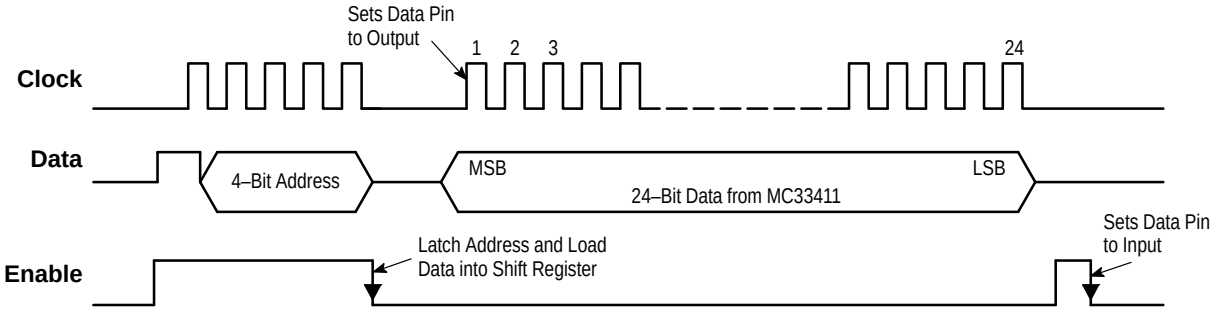
Figure 52. Writing Data to the MC33411



a. Write Operation:
   – To write data to the MC33411, the following sequence is required (see Figure 52):
6. The Enable line is taken high.
7. Five bits are entered:
   – The first bit must be a 0 to indicate a Write operation.
   – The next four bits identify the register address (0001–0111). The MSB is entered first.
8. The Enable line is taken low. At this transition, the address is latched in and decoded.
9. The Enable line is maintained low while the data bits are clocked in. The MSB is entered first, and the LSB last. If 24–bits are written to a register which has less than 24 active bits (e.g., register 6), the unassigned bits are to be 0.
10. After the last bit is entered, the Enable line is to be taken high and then low. The falling edge of this pulse latches in the just entered data. The clock line must be at a logic low and must not transition in either direction during this Enable pulse.
11. The Enable line must then be kept low until the next communication.

Note: If less than 24 bits are to be written to a data register, it is not necessary to enter the full 24 bits, as long as they are all lower order bits. For example, if bits 0–6 of a register are to be updated, they can be entered as 7 bits with 7 clock cycles in step 4 above. However, if this procedure is used, a minimum of 4 bits, with 4 clock pulses, must be entered.

Figure 53. Reading Data from the MC33411



b. Read Operation:
   – To read the output bits (bits 5/23–12), or the contents of any register, the following sequence is required (see Figure 53):

1. The Enable line is taken high.
2. Five bits are entered:
   – The first bit must be a 1 to indicate a Read operation.
   – The next four bits identify the register address (0001–0111). The MSB is entered first.
3. The Enable line is taken low. At this transition, the address is latched in and decoded, and the contents of the selected register is loaded into the 24–bit output shift register. At this point, the Data line (Pin 12) is still an input.
4. While maintaining the Enable line low, the data is read out. The first clock rising edge will change the Data line to an output, and the MSB will be present on this line.
5. The full contents of the register are then read out (MSB first, LSB last) with a total of 24 clock rising edges, including the one in step 4 above. It is recommended that the MCU read the bits after the clock's falling edge.
6. After the last clock pulse, the Enable line is to be taken high and then low. The falling edge of this pulse returns the Data Pin to be an input. The clock line must be at a logic low and must not transition in either direction during this Enable pulse.
7. The Enable line must then be kept low until the next communication.

Power Supply/Power Saving Modes

The power supply voltage, applied to all V_{CC} pins, can range from 2.7 to 5.5 V. All V_{CC} pins must be within ±0.5 V of each other, and each must be bypassed. It is recommended a ground plane be used, and all leads to the MC33411 be as short and direct as possible. To reduce the possibility of device latch–up, it is highly recommended that the Audio, Synthesizer and RF V_{CC} portions of the chip be isolated from the main supply through 10 to 25 Ω resistors (see the Evaluation PCB Schematic, Figure 54). This also provides RF–to–Audio noise isolation. The supply and ground pins are distributed as follows:

1. Pin 23 provides power to the audio section. Pin 40 is the ground pin.
2. Pin 28 provides power to the speaker amplifier section. Pin 31 is the ground pin.
3. Pin 3 provides power to the Rx PLL section. Pin 5 is the ground pin.
4. Pin 7 provides power to the Tx PLL section, and the MCU interface. Pin 5 is the ground pin.
5. Pin 42 provides power to the 2nd LO section. Pins 46 and 48 are the ground pins.
6. Pin 14 is the ground pin for the digital circuitry. Power for the digital circuitry is derived from Pin 23.

To conserve power, various sections can be individually disabled by using bits 5/7–0 and 6/7 (setting a bit to 1 disables the section).

1. Reference Oscillator Disable (bit 5/0) – The reference oscillator at Pins 15 and 16 is disabled, thereby denying a clock to the three PLLs and the switched capacitor filters. This function is not available on the "B" version.
2. Tx PLL Disable (bit 5/1) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 6 will be in a Hi–Z state.
3. Rx PLL Disable (bit 5/2) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 4 will be in a Hi–Z state.
4. LO2 PLL Disable (bit 5/3) – The VCO, 14–bit counter, output buffer, and phase detector are disabled. The charge pump output at Pin 47 will be in a Hi–Z state.
5. Power Amplifier Disable (bit 5/4) – The two speaker amplifiers are disabled. Their outputs will go to a high impedance state.
6. Rx Audio Path Disable (bit 5/5) – The anti–aliasing filter, low–pass filter, and variable gain stage are disabled.
7. Tx Audio Path Disable (bit 5/6) – Disables the microphone amplifier and low–pass filter.
8. Low Battery/RSSI Measurement Disable (bit 5/7) – Both 6–bit A/Ds are disabled.
9. Data Slicer Disable (bit 5/8) – The data slicer is disabled and DS Out goes to high impedance.
10. MCU Clock Disable (bit 6/7) – The MCU clock counter is disabled and the MCU Clock Output will be in a Hi–Z state. This function is not available on the "B" version.

Note: The 12–bit reference counter is disabled if the three PLLs are disabled (bits 5/1–3 = 1).

Table 9. Register Map

Reg Add	Reg Num	MSB Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
0001	1			Tx Polarity Select	Tx PD Cur Sel	MSB	13–Bit Tx N Counter Divide Value											LSB	MSB	7–Bit Tx A Counter Divide Value					LSB
0010	2			Rx Polarity Select	Rx PD Cur Sel	MSB	13–Bit Rx N' Counter Divide Value											LSB	MSB	7–Bit Rx A' Counter Divide Value					LSB
0011	3				VB Voltage Reference Adjust				FTxMC/ FRxMC Mode	LO2 Polarity Select	2nd LO PD Cur Sel	MSB	14–Bit 2nd LO Counter Divide Value												LSB
0100	4	Test Modes			LO2 Capacitor Select			6–Bit Switched Capacitor Filter Counter Divide Value						MSB	12–Bit Reference Counter Divide Value											LSB
0101	5	6–Bit Battery Voltage A/D Output							6–Bit RSSI A/D Output					Unused Register Bits		Data Slicer Invert	Data Slicer Disable	RSSI & Batt. A/D Disable	Tx Audio Disable	Rx Audio Disable	Power Amp Disable	2nd LO PLL Disable	Rx PLL Disable	Tx PLL Disable	Ref Osc Disable*
0110	6												ALC Gain = 25	ALC Gain = 10	Side Tone Attenuate Select		Comp. Low Max. Gain En.	MCU Clk Disable*	ALC Disable	Limiter Disable	Compres– ser Pass– through	Expander Pass– through	Tx Mute	Rx Mute	Power Amp Mute
0111	7								MCU Clock Divide Select			Volume Control				Tx Gain Adjust					Rx Gain Adjust				

* These bits not included in "B" version.

Table 10. Register Map: Power–Up Defaults

Reg Add	Reg Num	MSB Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
0001	1			Tx Polarity Select	Tx PD Cur Sel	MSB	13–Bit Tx N Counter Divide Value											LSB	MSB	7–Bit Tx A Counter Divide Value					LSB
				0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0010	2			Rx Polarity Select	Rx PD Cur Sel	MSB	13–Bit Rx N' Counter Divide Value											LSB	MSB	7–Bit Rx A' Counter Divide Value					LSB
				0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0011	3				VB Voltage Reference Adjust				FTxMC/ FRxMC Mode	LO2 Polarity Select	2nd LO PD Cur Sel	MSB	14–Bit 2nd LO Counter Divide Value												LSB
					0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0100	4	Test Modes			LO2 Capacitor Select			6–Bit Switched Capacitor Filter Counter Divide Value						MSB	12–Bit Reference Counter Divide Value											LSB
		0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0101	5	6–Bit Battery Voltage A/D Output							6–Bit RSSI A/D Output					Unused Register Bits		Data Slicer Invert	Data Slicer Disable	RSSI & Batt. A/D Disable	Tx Audio Disable	Rx Audio Disable	Power Amp Disable	2nd LO PLL Disable	Rx PLL Disable	Tx PLL Disable	Ref Osc Disable*
														0	0	0	0	0	0	0	0	0	0	0	0
0110	6												ALC Gain = 25	ALC Gain = 10	Side Tone Attenuate Select		Comp. Low Max. Gain En.	MCU Clk Disable*	ALC Disable	Limiter Disable	Compres– ser Pass– through	Expander Pass– through	Tx Mute	Rx Mute	Power Amp Mute
													0	0	0	0	0	0	0	0	0	0	0	0	0
0111	7								MCU Clock Divide Select			Volume Control				Tx Gain Adjust					Rx Gain Adjust				
									0	1	1	0	1	1	1	0	1	1	1	1	0	1	1	1	1

* These bits not included in "B" version.

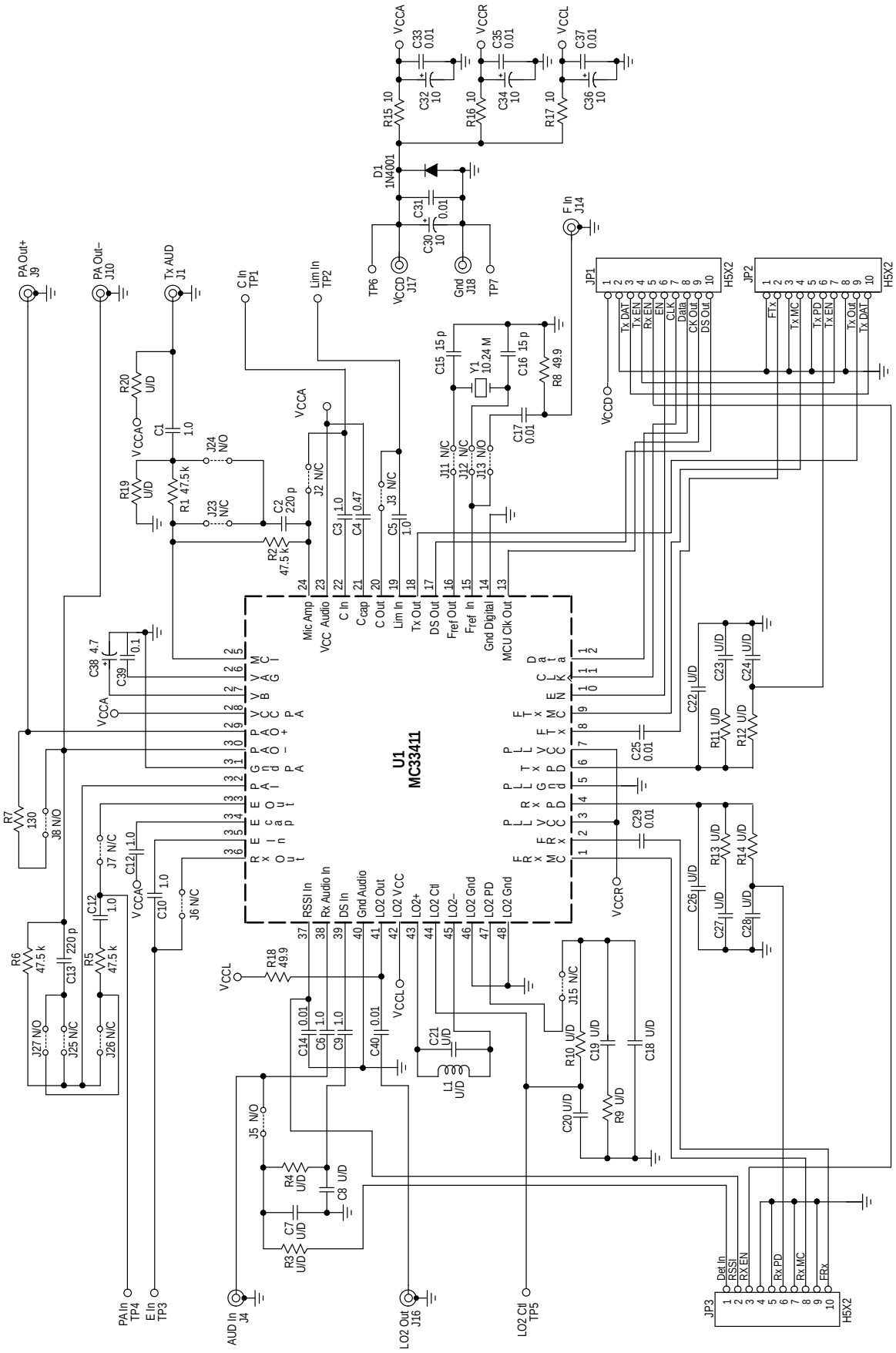
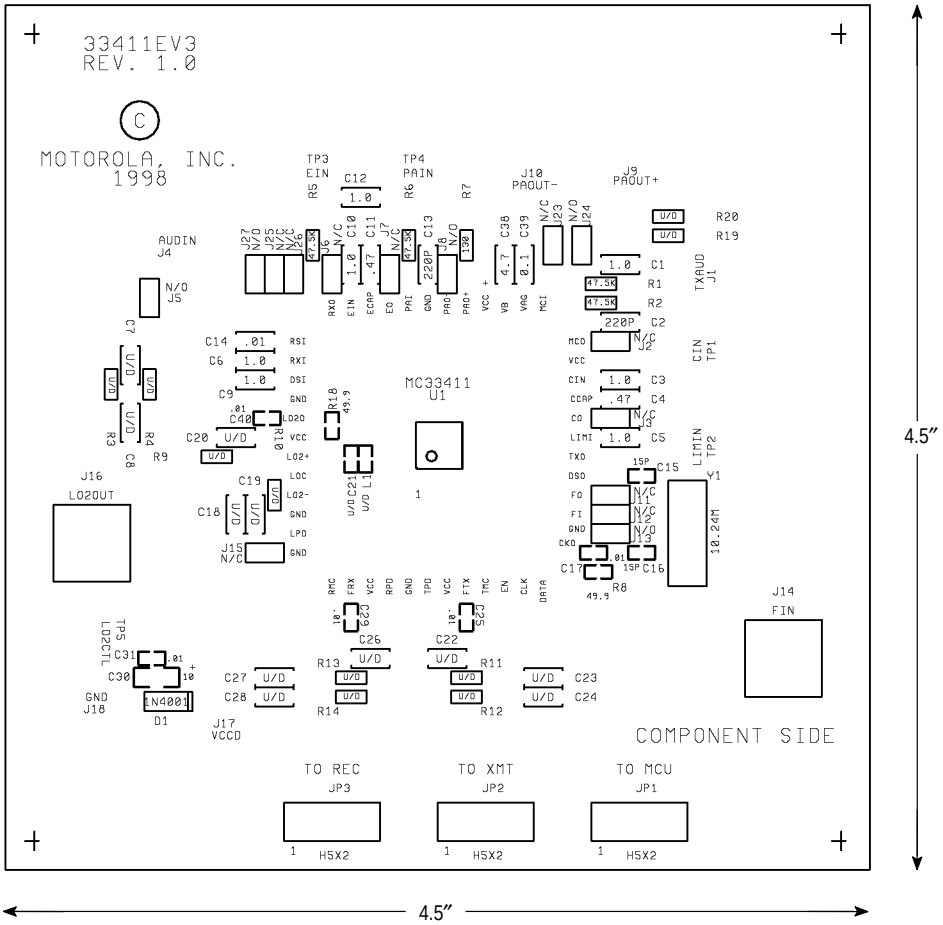


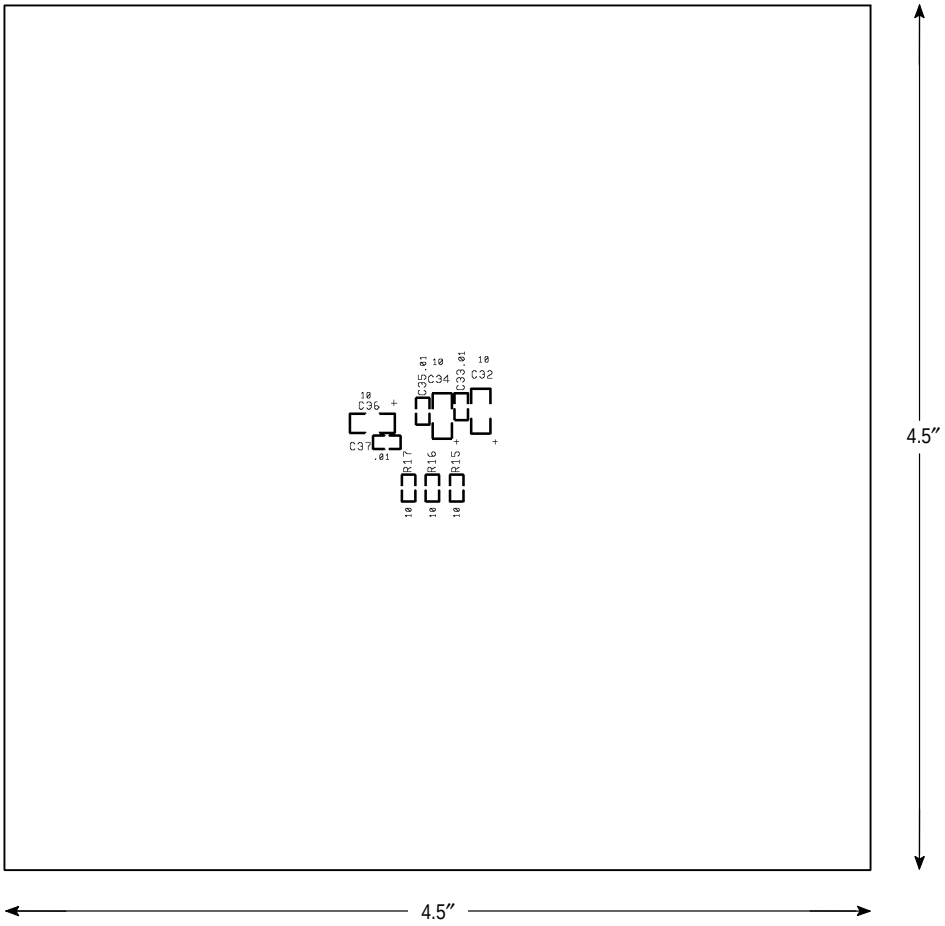
Figure 54. MC33411A/B Evaluation PCB Schematic

Figure 55. MC33411A/B Evaluation PCB Component Side



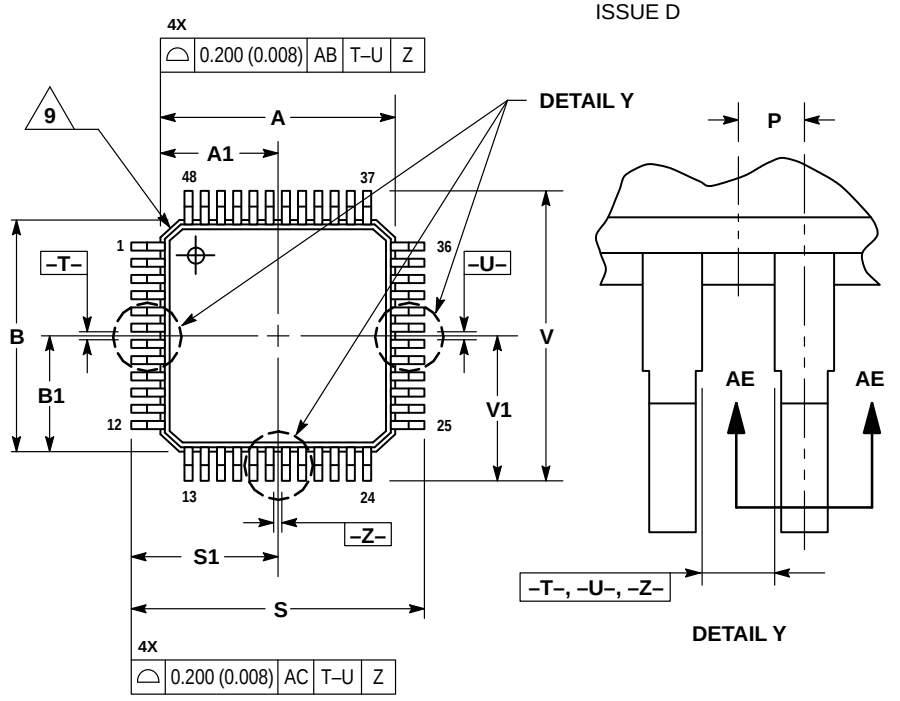
C1,C3,C5,C6,C9,C10,C12	1.0	J5,J8,J13,J24,J27	N/O
C13,C2	220 p	J9	PAOUT+
C4,C11	0.47	J10	PAOUT–
L1,R3,R4,C7,C8,R9,R10,	User defined	J14	F In
R11,R12,R13,R14,C18,R19,		J16	LO2 Out
C19,R20,C20,C21,C22,C23,		J17,TP6	V_{CCD}
C24,C26,C27,C28		J18,TP7	Gnd
C14,C17,C25,C29,C31,C33,	0.01	J19,J20,J21,J22	TP
C35,C37,C40		R1,R2,R5,R6	47.5 k
C15,C16	15 p	R7	130
R15,R16,R17,C30,C32,C34,	10	R8,R18	49.9
C36		TP1	C In
C38	4.7	TP2	Lim In
C39	0.1	TP3	E In
D1	1N4001	TP4	PA In
H1,H2,H3,H4	None	TP5	LO2 Ctl
JP1,JP2,JP3	H5X2	U1	MC33411
J1	Tx Aud	Y1	10.24 M
J2,J3,J6,J7,J11,J12,J15,	N.C.		
J23,J25,J26			
J4	Aud In		

Figure 56. MC33411A/B Evaluation PCB Solder Side



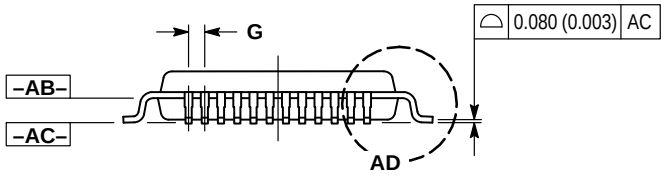
OUTLINE DIMENSIONS

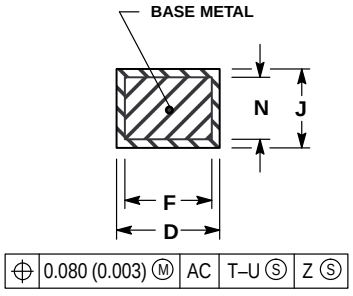
FTA SUFFIX
PLASTIC PACKAGE
CASE 932–02
(LQFP–48)
ISSUE D



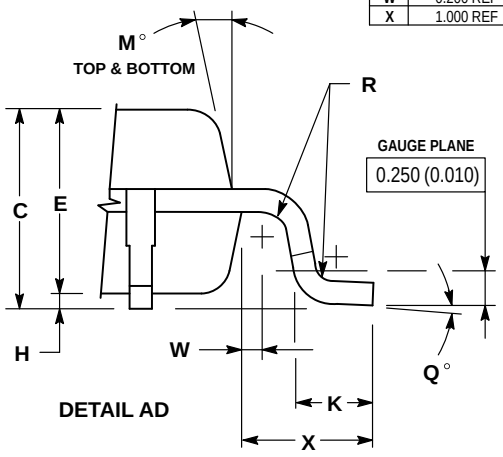
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12 °REF		12 °REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	





SECTION AE–AE



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