Super Matched Bipolar Transistor Pair Sets New Standards for Drift and Noise

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Matched bipolar transistor pairs are a very powerful design tool, yet have received less and less attention over the last few years. This is primarily due to the proliferation of high-performance monolithic circuits which are replacing many designs previously implemented with discrete components. State-of-the-art circuitry, however, is still the realm of the discrete component, especially because of recent improvements in the components themselves.

It has become clear in the past few years that ultimate performance in monolithic transistor pairs was being limited by statistical fluctuations in the material itself and in the processing environment. This led to a matched transistor pair fabricated from many different individual transistors physically located in a manner which tended to average out any residual process or material gradients. At the same time, the large number of parallel devices would reduce random fluctuations by the square root of the number of devices.

The LM194 is the end result. It is a monolithic bipolar matched transistor pair which offers an order-of-magnitude improvement in matching properties and parasitic base and emitter resistance over conventional transistor pairs. This was accomplished without compromising breakdown voltage or current gain. The LM194 is specified at 40V minimum collector-to-emitter breakdown voltage and has a minimum h_{FE} of 500 at 1 mA collector current. Maximum offset voltage is 50 μV over a collector current range of 1 μA to 1 mA. Maximum h_{FE} mismatch is 2%. Common mode rejection of offset voltage (dV_{OS}/dV_{CB}) is 124 dB minimum. An added benefit of paralleling many transistors is the resultant drop in overall r_{bb} and r_{ee}, which are 40Ω and 0.4Ω respectively. This makes the logarithmic conformity of emitter-base voltage to collector current excellent even at higher current levels where other devices become non-theoretical. In addition, broadband noise is extremely low, especially at higher operating currents.

The key to the success of the LM194 is the nearly one-to-one correlation between measured parameters and those predicted by a theoretical bipolar transistor model. The relationship between emitter-base voltage and collector current, for instance, is perfectly logarithmic over an extremely wide range of collector currents, deviating in the pA range because of leakage currents and above several milliamperes due to the finite 0.4Ω emitter resistance. This gives the LM194 a distinct advantage in non-linear designs where true logarithmic behavior is essential to circuit accuracy. Of equal importance is the absolute nature of the logarithmic constant, both between the two halves of the device and from unit to unit. The relationship can be expressed as:

$$V_{BE_1} - V_{BE_2} = \frac{kT}{q} \ln \left(\frac{I_{C_1}}{I_{C_2}} \right)$$

This relationship holds true both within a single transistor where I_{C_1} and I_{C_2} represent two different operating currents and between the two halves of the LM194 where collector currents are unbalanced. Of particular importance is the fact that the kT/q logarithmic constant is an absolute quantity dependent only on Boltzman's constant (k), absolute temperature (T), and the charge on the electron (q). Since these values are independent of processing, there is virtually no variation from unit to unit at a fixed temperature. Lab measurements indicate that the logarithmic constant measured at a 10:1 collector current ratio does not vary more than $\pm$0.5% from its theoretical value. Applications such as logarithmic converters, multipliers, thermometers, voltage references, and voltage-controlled amplifiers can take advantage of this inherent accuracy to provide adjustment-free precision circuits.

APPROACHING THEORETICAL NOISE

In many low-level amplifier applications, the limiting factor on performance is noise. With bipolar transistors, the theoretical value for emitter-base voltage noise is a function only of absolute temperature and collector current.

$$e_n = kT \sqrt{\frac{2}{qI_C}} \quad \text{Volts}/\sqrt{\text{Hz}}$$

This formula indicates that voltage noise can be reduced to low levels by simply raising collector current. In fact, that is exactly what happens until collector current reaches a level where parasitic transistor noise limits any further reduction. This ''noise floor'' is usually created by and modeled as an equivalent resistor (r_{bb}') in series with the base of the transistor. Low parasitic base resistance is therefore an important factor in ultra-low-noise applications where collector current is pushed to the limits. The 40Ω equivalent r_{bb}' of the LM194 is considerably lower than that of other small-signal transistors. In addition, this device has no excess noise at lower current levels and coincides almost exactly with the predicted values. A low-noise design can be done on paper with a minimum of bench testing.

Another noise component in bipolar transistors is base current noise. For any finite source impedance, current noise must be considered as a quadrature addition to voltage noise.

$$\begin{matrix}\text{total equivalent} \\ \text{input voltage noise}\end{matrix} = e_N = \sqrt{e_n^2 + (i_n \bullet r_s)^2} \text{Volts}/\sqrt{\text{Hz}}$$

where r_s is the source impedance

In the LM194, base current noise is a well-defined function of collector current and can be expressed as:

$$i_n = \sqrt{\frac{2q \bullet I_C}{h_{FE}}} \quad \text{Amps}/\sqrt{\text{Hz}}$$

To find the collector current which yields the minimum overall equivalent input noise with a given source impedance, the total noise formula can be differentiated with respect to I_C and set equal to zero for finding a minimum.

$$e_N^2 = e_n^2 + (i_n^2 \bullet r_s^2) + 4\,kT \bullet r_s$$

$$(4\,kT \bullet r_s = \text{noise}^2 \text{ of } r_s)$$

$$= \frac{2k^2 \bullet T^2}{q \bullet I_C} + \frac{2q \bullet I_C \bullet r_s^2}{h_{FE}} + 4kT \bullet r_s$$

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$$\frac{d(V_N^2)}{d(I_C)} = \frac{-2k^2 \bullet T^2}{q \bullet I_C^2} + \frac{2q \bullet r_s^2}{h_{FE}} = 0$$

$$I_C \text{ (optimum)} = \frac{kT}{q} \bullet \frac{\sqrt{h_{FE}}}{r_s}$$

For very low source impedances, the 40Ω r_{bb}' of the LM194 should be added to r_s in this calculation. A plot of noise figure versus collector current (see curve) shows that the formula does indeed predict the optimum value. The curves are very shallow, however, and actual current can be varied by 3:1 without losing more than 1 dB noise figure in most cases. This may be a worthwhile tradeoff if low bias current ($I_C < I_{opt}$) or wide bandwidth ($I_C > I_{opt}$) is also important *Figure 1* is a plot of best obtainable noise figure versus

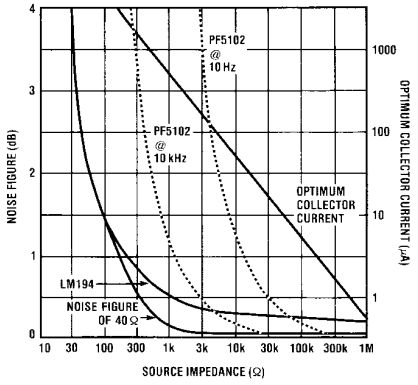

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FIGURE 1. Noise Figure vs Source Impedance

source impedance for the LM194 and a very low noise junction FET (PF5102). Collector current for the LM194 is optimized for each source impedance and is also plotted on the graph using the right side scale. The PF5102 is operated at a constant 1 mA. It is obvious that the bipolar device gives significantly better noise figures for low source impedances and/or low frequencies. FETs are particularly poor at very low frequencies (< 10 Hz) and offer advantages only for very high source impedances.

REACTIVE SOURCES

Calculations may also be done to derive an optimum collector current when the signal source is reactive. In this case, upper and lower frequencies (f_H and f_L) must be specified. Also, optimum current is different for an amplifier with a summing junction input ($Z_{IN} = 0$) as compared to a high impedance input ($Z_{IN} \gg X_C, X_L$). The formulas below give optimum collector current for noise within the frequency band f_L to f_H. For audio applications, lowest "perceived" noise may be somewhat different because of the variation in sensitivity of the ear to frequencies in the audio range (Fletcher-Munson effect).

Capacitive source into high impedance:

$$I_C \text{ (opt)} = \frac{kT}{q} \bullet C \bullet 2\pi \bullet \sqrt{h_{FE}} \bullet \sqrt{f_H \bullet f_L}$$

Capacitive source into summing junction:

$$I_C \text{ (opt)} = \frac{kT}{q} \times \frac{\sqrt{h_{FE}}}{R_f} \times \sqrt{\frac{4\pi^2 \bullet R_f^2 \bullet C^2 (f_L^2 + f_H^2 + f_L \bullet f_H)}{3} + \frac{4\pi \bullet R_f \bullet C \bullet (f_H + f_L)}{2} + 1}$$

Inductive source into high impedance:

$$I_C \text{ (opt)} = \frac{\frac{kT}{q} \bullet \sqrt{h_{FE}}}{2\pi \bullet L} \sqrt{\frac{3}{f_L^2 + f_H^2 + f_L \bullet f_H}}$$

Keep in mind that the simple formula for total input-referred noise, though accurate in itself, does not take into account the effects of noise created in additional stages or noise injected from supply lines. In most cases voltage gain of the LM194 stage will be sufficient to swamp out second stage effects. For this to be true, first stage gain must be at least $3 \bullet v_{n2}/v_N$, where v_{n2} is the voltage noise of the second stage and v_N is the desired total input referred voltage noise. A simple formula for voltage gain of an LM194 stage, assuming no second stage loading, is given by:

$$A_V = \frac{(R_L)(I_C)}{kT/q} \text{ where } R_L \text{ is the load resistor}$$

Noise injected from power supplies is an often overlooked problem in low noise designs. This is probably in part due to the use of IC op amps with their high power supply rejection ratio and differential inputs. Many low-noise designs are single-ended and do not enjoy the inherent supply rejection of differential designs. For a single-ended amplifier with its load resistor tied directly to the power supply, noise on the supply must be no higher than $(R_L \bullet I_C \bullet v_N)/(3\ kT/q)$ or noise performance will be degraded. For a differential stage (see *Figure 2*) with the common emitter resistor tied to the negative supply and the collector resistors tied to the positive supply, supply noise is not generally a problem, at least at low frequencies. For this to be true at higher frequencies, the capacitance at the collector nodes must be kept low and balanced. In an unbalanced situation, noise from either supply will feed through unattenuated at higher frequencies where the reactance of the capacitor is much lower than the collector resistance.

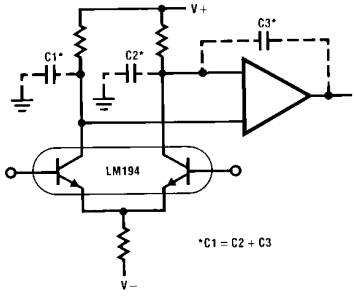

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FIGURE 2. High Frequency Power Supply Rejection

BANDWIDTH CONSIDERATIONS

Because of its large area, the LM194 has capacitance-limited bandwidth. The $h_{fe} \bullet f$ product is roughly 0.08 MHz per microampere of collector current, yielding an f_t of 80 MHz at $I_C = 1$ mA and 800 kHz at $I_C = 10\ \mu A$.

Collector-base capacitance on the LM194 is somewhat higher than ordinary small-signal transistors due to the large device geometry. C_{ob} is 17 pF at $V_{CE} = 5V$. For high gain stages with finite source impedance, the Millering effect of C_{ob} will usually be the limiting factor on voltage gain band-

width. At $I_C = 100\ \mu A$ and $R_L = 50\ k\Omega$, for instance, DC voltage gain will be $(R_L)(I_C)/(kT/q) = 200$, but bandwidth will be limited to

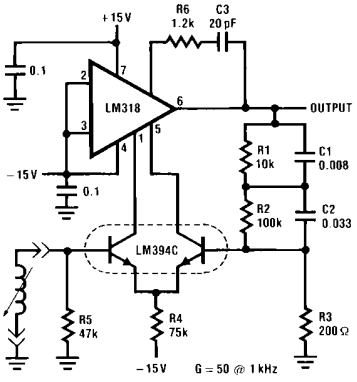
$$BW = \frac{kT/q}{(2\pi)(R_L)(I_C)(R_s)(C_{ob})} = 50\ kHz$$

for a source impedance (R_S) of 1 kΩ.

LOW NOISE APPLICATIONS

Figures 3 and *4* represent two different approaches to low noise designs. In *Figure 3*, the LM194 is used to replace the input stage of an LM118 high speed operational amplifier to create an ultra-low-distortion, low-noise RIAA-equalized phono preamplifier. The internal input stage of the LM118 is shut off by tying the unused inputs to the negative supply. This allows the LM194 to be used in place of the internal input stage, avoiding the loop stability problems created when extra stages are added. The stability problem is especially critical in an RIAA circuit where 100% feedback is used at high frequencies. Performance of this circuit exceeds the ability of most test equipment to measure it. As shown in the accompanying chart, *Figure 3*, harmonic distortion is below the measurable 0.002% level over most of the operating frequency and amplitude range. Noise referred to a 10 mV input signal is 90 dB down, measuring 0.55 μV_{RMS} and 70 pA_{RMS} in a 20 kHz bandwidth. More importantly, the noise figure is less than 2 dB when the amplifier is used with standard phono cartridges, which have an equivalent wideband (20 kHz) noise of 0.7 μV[1]. Further improvements in amplifier noise characteristics would be of little use because of the noise generated by the cartridge itself.

A special test was performed to check for "Transient Intermodulation Distortion"[2]. 10 kHz and 11 kHz were mixed 1:1 at the input to give an RMS output voltage of 2V (input = 200 mV). The resulting 1 kHz intermodulation product measured at the output was 80 μV. This calculates to 0.004% distortion, an incredibly low level considering that the 1 kHz has 14 dB (5:1) gain with respect to the 10 kHz signal in an RIAA circuit. Of special interest also is the use of all DC coupling. This eliminates the overload recovery problems associated with coupling and bypass capacitors. Worst case



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NOTE: Cartridge is assumed to have less than 5 kΩ DC resistance. Do not capacitor couple the cartridge. R1, R2, and R3 should be low noise metal film resistors.

FREQUENCY (Hz)	TOTAL HARMONIC DISTORTION				
20	<0.002	<0.002	<0.002	<0.002	<0.002
100	<0.002	<0.002	<0.002	<0.002	<0.002
1k	<0.002	<0.002	<0.002	<0.002	<0.002
10k	<0.002	<0.002	<0.002	0.0025	<0.003
20k	<0.002	<0.002	0.004	0.004	0.007
	0.03	0.1	0.3	1.0	5.0

OUTPUT AMPLITUDE (V) RMS

FIGURE 3. Ultra Low Noise RIAA Phono Preamplifier

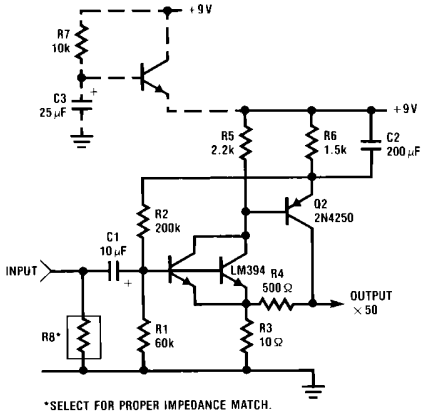

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FIGURE 4. Ultra Low Noise Preamplifier

DC output offset voltage is about 1V with a cartridge having 1 kΩ DC resistance.

The single-ended amplifier shown in *Figure 4* was designed for source impedances below 250Ω. At this level, the LM194 should be biased at 2.5 mA (or higher) collector current. Unfortunately, r_{bb}', even at 40Ω, is the limiting factor on noise at these current levels. To achieve better performance, the two halves of the LM194 are paralleled to reduce r_{bb}' to 20Ω. Total input voltage noise for this design is given by:

$$e_N = \sqrt{4kT(r_{bb}' + R_3) + e_n^2}$$
$$= \sqrt{0.504 + 0.096} = 0.775\ nV/\sqrt{Hz}$$

The current noise is 1.2 $pA/\sqrt{Hz}$, and when this flows through a 250Ω source resistance, it causes an additional 0.30 $nV/\sqrt{Hz}$. Since the Johnson noise of a 250Ω resistor is 2.0 $nV/\sqrt{Hz}$, the noise figure is:

$$NF = 20 \log \frac{\sqrt{(2\ nV)^2 + (0.3\ nV)^2 + (0.775\ nV)^2}}{2nV} = 0.74\ dB$$

Several unique features of this circuit should be pointed out. First, it has only one internal capacitor which functions as an AC bypass for both stages. Second, no input stage load resistor bypassing is used, yet the circuit achieves 56 dB supply rejection referred to input. The optional supply filter shown in dotted lines improves this by an additional 50 dB and is necessary only if supply noise exceeds 20 $nV/\sqrt{Hz}$. Finally, the problem of AC coupling the 10Ω feedback impedance is eliminated by using a DC biasing scheme which biases both stages simultaneously without relying on feedback from the output.

Harmonic distortion is very low for a ''simple'' two stage design. At 300 mV output, total harmonic distortion measured 0.016%. For normal signal levels of 50 mV and below, distortion was lost in the noise floor. Small-signal bandwidth is 3 MHz.

An ideal application for this amplifier is as a head pre-amp for moving-coil phono cartridges. These cartridges have very low output impedance ($< 50\Omega$ at low frequencies) and have a full-output signal below 1 mV. Obviously, the preamp used for such a low signal level must have superb noise properties. The amplifier shown has a total RMS input noise of 0.11 μV in a 20 kHz bandwidth, yielding a signal-to-noise ratio of 70 dB when used with a 40Ω source impedance at a 0.5 mV signal level.

LOW-NOISE, LOW-DRIFT INSTRUMENTATION AMPLIFIER HAS WIDE BANDWIDTH

The circuit in *Figure 5* is a high-performance instrumentation amplifier for low-noise, low-drift, wide-bandwidth applications. Input noise voltage is 2 nV/$\sqrt{\text{Hz}}$ up to 20 kHz, rising

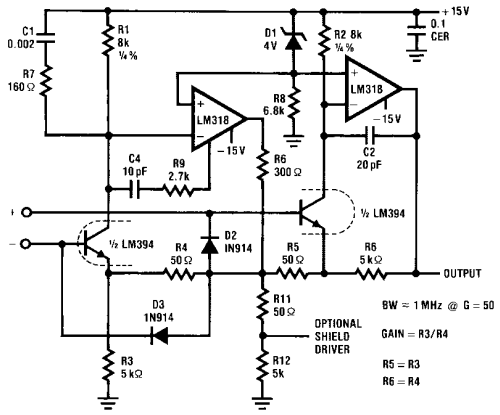

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FIGURE 5. Low Drift-Low Noise Instrumentation Amplifier

to 3.5 nV/$\sqrt{\text{Hz}}$ at 100 kHz. Bandwidth at a gain of 50 is 1 MHz and gain can be varied over the range of 10−100 simply by changing the value of R_3 and R_6. Input offset voltage drift is determined by the LM194 and the tracking of the (R_1–R_2), (R_3–R_6), and (R_4–R_5) pairs. 20 ppm/°C mismatch on all pairs will generate 1.1 μV/°C referred to input, dominating the drift due to the LM194. Resistor pairs which track to 5 ppm/°C or better are recommended for very low drift applications. Input bias current is about 1 μA, rather high for general purpose use, but necessary in this case to achieve wide bandwidth and low noise. The tight matching of the LM194, however, reduces input offset current to 20 nA, and input offset current drift to 0.5 nA/°C. Input bias current drift is under 10 nA/°C. In terms of source impedance, total input referred voltage drift will be degraded 1 μV/°C for each 100Ω of unbalanced source resistance and 0.05 μV/°C for each 100Ω of balanced source resistance. DC common mode rejection of this amplifier is extremely good, depending mostly on the match of the ratio of R_3/R_4 to R_5/R_6. 0.1% matching gives better than 90 dB. Rejection will improve with tighter matching and is not limited by the LM194 until CMRR approaches 120 dB. High frequency CMRR is also very good, measuring 80 dB at 20 kHz and 60 dB at 100 kHz. Settling time for a 10V output step is 1.5 μs to 0.1%, and 5 μs to 0.01%. Distortion with 10 $V_{p\text{-}p}$ output is virtually unmeasurable ($< 0.002\%$) at low frequencies, rising to 0.1% at 50 kHz, and 1% at 200 kHz.

LOW DRIFT DESIGNS

Offset voltage drive in the LM194 quite closely follows the theoretical value derived by differentiating the logarithmic formula. In other words it is a function only of the original offset voltage. If V_{OS} is the original room temperature offset voltage, drift of offset as given by differentiation yields:

$$\frac{d(V_{OS})}{dT} = \frac{\left(d\,kT/q \ln e^{\frac{V_{OS}}{kT/q}}\right)}{dT}$$

$$= \frac{V_{OS}}{T}$$

At room temperature (T = 297°K), 1 mV of offset voltage will generate 1 mV/297°K = 3.37 μV/°C drift. The LM194 with a maximum offset voltage of 50 μV could be expected to have a maximum offset voltage drift of 0.17 μV/°C. Lab measurements indicate that it does not deviate from this theoretical drift by more than 0.1 μV/°C. This means the LM194 can be specified at 0.3 μV/°C drift without an individual drift test on each device. In addition, if initial offset voltage is zeroed out, maximum drift will be less than 0.1 μV/°C. The zeroing, of course, must be done in a way that theoretically zeroes drift. This is best done as shown in *Figure 6* with a small trimpot used to unbalance collector load resistors. (See National's Application Note AN-3.)

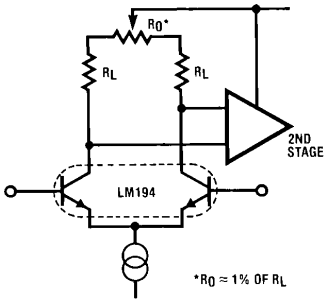

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FIGURE 6. Zeroing Offset and Drift

To obtain optimum performance from such a low-drift device, strict attention must be paid to sources of drift external to the device itself. These include thermocouple effects, mismatch in load-resistor temperature coefficients, second-stage loading, collector leakage, and finite source impedance.

Thermocouple effects in ultra-low-drift amplifiers are often the limiting factor in performance. The copper-to-Kovar (LM194 leads) thermocouple will generate 35 μV/°C. This sounds extremely high, but is not a problem if all input leads on the LM194 are at the same temperature. For optimum drift performance, the differential lead temperature where copper connects to Kovar should not exceed 0.5 millidegrees per degree change in ambient. If the LM194 is mounted on a printed circuit board, emitter and base leads should be soldered to identical size pads and the package orientation should place emitter and base leads on isothermal lines if any significant power is being dissipated on the board. The board should be kept in a still-air environment to minimize the effects of circulating air currents. ''Still'' air is particularly important when the LM194 leads are soldered di-

rectly to wires and when low (< 10 Hz) noise is critical. Individual wires in air can easily generate a differential end temperature of 10 millidegrees in an ordinary room ambient, even with the wires twisted together. This can cause up to 1 μV_{p-p} fluctuation in offset voltage. The 0.001 Hz to 10 Hz noise of the LM194 operating differentially at 100 μA is typically 40 nV_{p-p} (see *Figure 7*), so the thermally generated signal represents a 25:1 degradation of low frequency noise.

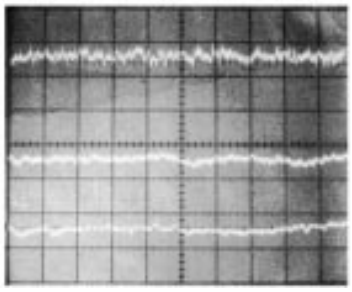

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FIGURE 7. Low Frequency Noise of Differential Pair. Unit must be in still air environment so that differential lead temperature is held to less than 0.0003°C.

If the load resistors used to bias the LM194 do not have identical temperature coefficients, they will contribute to offset voltage drift. A 1 ppm/°C mismatch in resistor drift will generate 0.026 μV/°C drift in the LM194. Resistors with 10 ppm/°C differential drift will seriously degrade the drift of an otherwise perfect circuit design. Resistors specified to track better than 2 ppm/°C are available from several manufacturers including Vishay, Julie, RCL, TRW, and Tel Labs.

Source impedance must be considered in a low-drift amplifier since voltage drift at the output can result from drift of the base currents of the LM194. Base current changes at about −0.8%/°C. This is equal to 2 nA/°C at a collector current of 100 μA and an h_{FE} of 400. If drift error caused by the changing base current is to be kept to less than 0.05 μV/°C, source unbalance cannot exceed 25Ω in this example. If a balanced condition exists, source impedance is still limited by the base current mismatch of the LM194. Worst case offset in the base current is 2%, and this offset can have a temperature drift of up to 2%/°C, yielding a change in offset current of up to

$$(2\%)(100\ \mu A)(2\%/°C)/h_{FE} = 0.1\ nA/°C$$

at a collector current of 100 μA. This limits balanced source impedances to 500Ω at collector currents of 100 μA if drift error is to be kept under 0.05 μV/°C. For higher source impedances, collector current must be reduced, or drift trimming must be used.

Collector-leakage effects on drift are generally very low for temperatures below 50°C. At higher temperatures, leakage can be a factor, especially at low collector currents. At 70°C, total collector leakage (to base and substrate) is typically 2 nA, increasing at 0.2 nA/°C. Assuming a 10% mismatch between collector leakages, input-referred drift will be 0.05 μV/°C at a collector current of 10 μA, and 0.005 μV/°C at 100 μA. At 125°C, input referred drift will be 1.5 μV/°C and 0.15 μV/°C respectively.

The amplifier used in conjunction with the LM194 may contribute significantly to drift if its own drift characteristics are poor. An LM194 operated with 2.5 V_{DC} across its load resistors has a voltage gain of approximately 100. If the second stage amplifier has a voltage drift of 20 μV/°C (normal for an amplifier with V_{OS} = 6 mV) the drift referred to the LM194 inputs will be 0.2 μV/°C, a significant degradation in drift. Amplifiers with low drift such as the LM108A or LM308A (5 μV/°C max) are recommended.

For the ultimate in low drift applications, the residual drift of the LM194 can be zeroed out. This is particularly easy because of the known relationship between a change in room-temperature offset and the resultant change in offset drift. The zeroing technique involves only one oven test to establish initial drift. The drift can then be reduced to below 0.03 μV/°C with a simple room-temperature adjustment. The procedure is as follows: (See *Figure 8*.)

1. Zero the offset voltage at room temperature (T_A).
2. Raise oven temperature to desired level (T_H) and measure offset voltage.
3. Bring circuit back to room temperature and adjust offset voltage to (V_{OS} at T_H) • (T_A)/(T_H − T_A). (T is in °K.)
4. Re-adjust offset voltage to zero with an external reference source by summing the two signals. (Do not re-adjust the offset of the LM194.)

This technique can be extended to include drift correction for source-generated drift as well since the basic correcting mechanism *is independent of the source of drift*.

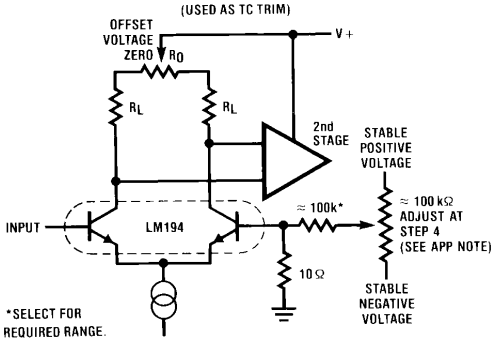

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FIGURE 8. Correcting for Residual or Source Generated Drift

VOLTAGE REFERENCE

Voltage references utilizing the bandgap voltage of silicon were first used 8 years ago, and have since gained wide acceptance in such circuits as the LM109, LM113, LM340, LM117, μA7800, AD580, and REF 01. The theory has been well publicized and is not reiterated here.

The circuit in *Figure 9* is a micropower version of a bandgap technique first used by Analog Devices. It operates off a single 2.5V to 6V supply and draws only 25 μA idling current. Two AA penlight cells will power the reference for over a year of continuous operation. Maximum output current is 0.5 mA, with an output resistance of 0.2Ω. Line regulation is ~0.01%/V and output noise is 20 μV_{RMS} over a 10 kHz bandwidth. Temperature drift is less than ±50 ppm/°C when the output is trimmed to 1.21V. Much lower drift can be obtained by adjusting the output of each reference to the

optimum value. A 1% shift in output voltage changes drift 33 ppm/°C. Temperature range is −25°C to +100°C.

The LM194 is the entire reference in this design, supplying both V_{BE} and ΔV_{BE} portions of the reference. One half LM114 delivers a constant bias current to the LM4250. The other half, in conjunction with the 2N4250 PNP, ensures startup of the circuit under worst cast (2.4k) load current. R_1–R_2 and R_4–R_5 should track to 50 ppm/°C. R_6 should have a TC of under 250 ppm/°C. The circuit is stable for capacitive loads up to 0.047 μF. C_2 is optional, for improved ripple rejection.

STRAIN GAUGE AMPLIFIER

The instrumentation amplifier shown in *Figure 10* is an example of an ultra-low-drift design specifically optimized for strain-gauge applications. A typical strain-gauge bridge has one end grounded and the other driven by a 3-to-10 volt precision voltage reference. The differential output signal of the bridge has a 1.5 to 5 volt common-mode level and a typical full-scale differential signal level of 5–50 mV. Source impedance is in the range of 100Ω to 500Ω, with an impedance imbalance of less than 2%. This amplifier has been specifically optimized for these types of signals. It has a +1V to +10V common mode range, a full scale input of 20 mV (1 mV to 100 mV is possible) and fully balanced inputs with a differential input impedance > 10 MΩ. Common mode input impedance is 100 MΩ. Common mode rejection ratio is 120 dB at 60 Hz, 114 dB at 1 kHz, and 94 dB at 10 kHz referred to input. Power supply rejection at DC is 114 dB on the V+ supply and 108 dB on the V− supply. Small signal bandwidth is > 50 kHz and slew rate is 0.1 V/μs. Gain error is determined by the accuracy of R_9, R_8, R_4, and R_3. For the values shown, gain is 500. R_3 can be varied to set gain as desired from 250 (800Ω) to 10,000 (20Ω). Gain non-linearity is < 0.05% for a 10V output and < 0.012% for a 5V output). R_7 is a +0.3%/°C positive-temperature-coefficient wirewound resistor for compensation of gain with temperature. Without this resistor, gain change with temperature is 0.007%/°C. If R_7 is omitted, replace R_9 with 12.4 kΩ.

Input offset voltage drift is determined primarily by resistor mismatches between R_1/R_2 and R_5/R_6. If either of these ratios drifts by 5 ppm/°C, an input offset voltage drift of 0.15 μV/°C will be created. Other resistor drifts contribute to gain error only. R_{12} is used to adjust room temperature offset voltage to zero.

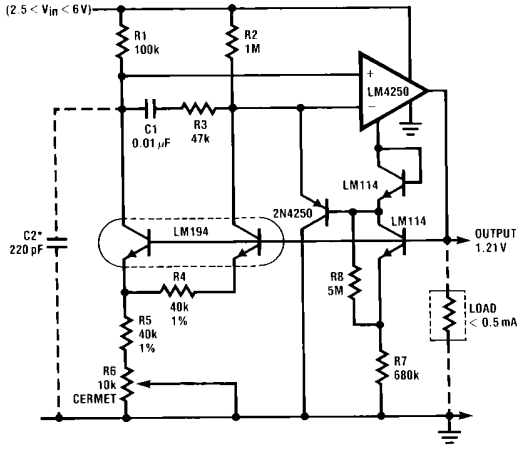

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FIGURE 9. Micropower Reference

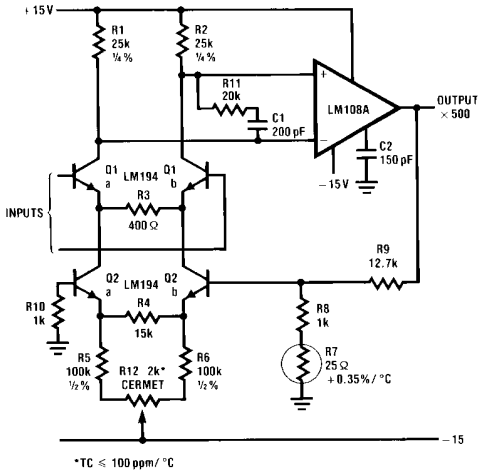

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FIGURE 10. Strain Gauge Instrumentation Amplifier

THERMOCOUPLE AMPLIFIER WITH COLD JUNCTION COMPENSATION

Thermocouple amplifiers need low offset voltage drift, good gain accuracy, low noise, and most importantly, cold-junction compensation. The amplifier in *Figure 11* does all that and more. It is specifically designed for ease of calibration so that repeated oven cycling is not required for calibration of gain and zero. Also, no mathematical calculations are required in the calibration procedure.

The circuit is basically a non-inverting amplifier with the gain set to give 10 mV/(°F or °C) at the output. This output sensitivity is arbitrary and can be set higher or lower. Cold-junction compensation is achieved by deliberately unbalancing the collector currents of the LM194 so that the resulting input offset voltage drift is just equal to the thermocouple output (α) at room temperature. By combining the formulas for offset voltage versus current imbalance and offset voltage drift, the required ratio of collector currents is obtained.

$$\frac{d(V_{os})}{dT} = \frac{V_{OS}}{T} = \frac{k}{q} \ln \frac{I_{C_1}}{I_{C_2}}$$

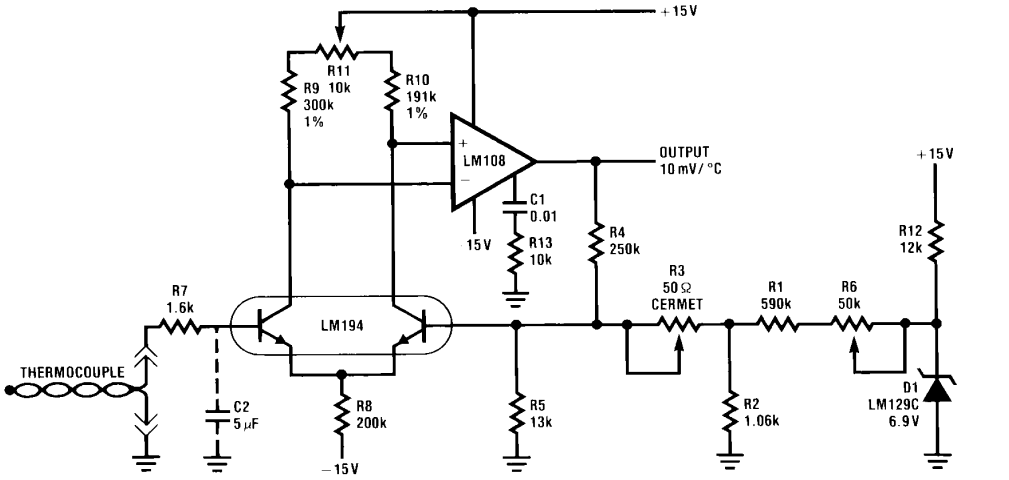
$$\ln \frac{I_{C_1}}{I_{C_2}} = \frac{q \bullet V_{OS}}{k \bullet T} = \frac{q \bullet \alpha}{k}$$

$$\frac{I_{C_1}}{I_{C_2}} = e^{\frac{q \bullet \alpha}{k}}$$

(α = thermocouple output in V/°C)

This technique does require that the LM194 be at the same temperature as the thermocouple cold junction. The thermocouple leads should be terminated close to the LM194.

The deliberate offset voltage created across the LM194 inputs must be subtracted out with an external reference which is also used to zero shift the output to read directly in °C or °F. This is done in a special way so that at some arbitrarily selected temperature (T_1), the gain adjustment has no effect on zero, vastly simplifying the calibration procedure. Design equations for the circuit are shown with the schematic in descending order of their proper use. Also shown is the calibration procedure, which requires only one oven trip for both gain and zero. Use of the nearest pocket calculator should yield all resistor values in a few minutes. The values shown on the schematic are for a 10 mV/°C output with a Chromel-Alumel thermocouple delivering 40 μV/°C, with T_1 selected at room temperature (297°K). All resistors except R_8 and R_{12} should be 1% metal film types



1. Select R9 = 300 kΩ
2. Set R10 equal to R9 • $e^{-\alpha(1.16 \times 10^4)}$
3. R8 = 200k
4. Select R4 in the range 50 kΩ to 250 kΩ
5. $R5 = \frac{(R4)(T_1)(\alpha)}{S(T_1 - T_0) - \alpha(T_1)}$
6. $R2 = \frac{\alpha(R4)(R5)(1 - E^*/100)}{(S - \alpha)\left[R5 - \frac{\alpha(R4)}{S - \alpha}\right]}$
7. $R1 = \frac{[(R2) \bullet V_Z - \alpha(T_1)]}{\alpha(T_1)}(0.95)$
8. $R3 = \frac{(E)(R2)}{50}$
9. R7 = (R9/R10)(R2)
10. R6 = R1/10

E = Gain error allowed for ($\approx$2.5%)

T_1 = Temperature in °K at which it is desired to have the gain control not interact with the zero control

T_0 = Temperature in °K at which the desired temperature scale (°C or °F) is equal to zero

S = Required output scale factor. Use V/°C even though actual output may be in °F

V_Z = Zener reference voltage

α = Thermocouple output in V/°C

Values shown on schematic are for 10 mV/°C.

See below for 10 mV/°F values using a Chromel-Alumel thermocouple with room temperature for T_1.

R1 = 367k, R2 = 629Ω, R3 = Ω, R4 = 250k, R5 = 4.08k, R6 = 50k, R7 = 1k, R10 = 191k

CALIBRATION:*

a. Set oven to T_1 and adjust R6 to give proper output (zero adjust).

b. Raise (or lower) oven to T_2 and adjust R3 to give proper output at T_2 (gain adjust).

c. Return to room temperature and short thermocouple and D1 to ground. Adjust R11 to give proper output (room ambient) in °K or °R.

For 10 mV/°C, this is 2.98V @ T_A = 25°C.

For 10 mV/°F, this is 5.37V @ T_A = 77°F.

d. Remove shorts and re-adjust R6 if necessary to zero output.

Note: Steps C and D can be eliminated if exact cold junction compensation is not required. R11 is simply shorted out. Compensation will be within ±5% without adjustment ($\leq$0.05°C/°C).

*Thermocouple only in oven.

FIGURE 11. Thermocouple Amplifier with Cold-Junction Compensation

for low thermocouple effects (resistors *do* generate thermocouple voltages if their ends are at different temperatures) and should have low temperature coefficients. R_9 and R_{10} should track to 10 ppm/°C. R_3, R_6, and R_{11} should not have a TC higher than 250 ppm/°C. R_1, R_2, and R_4 should track to 20 ppm/°C. C_2 can be added to reduce spikes and noise from long thermocouple lines.

Input impedance for this circuit is $>$ 100 MΩ, so high thermocouple impedance will not affect scale factor. ''Zero shift'' due to input bias current is approximately 1°C for each 400Ω of thermocouple lead resistance with a 40 μV/°C thermocouple.

No provision is made for correction of thermocouple non-linearity. This could be accomplished with a slight nonlinearity introduced into R_4 with additional resistors and diodes. Another possibility is to digitize the output and correct the nonlinearity digitally with a ROM programmed for a specific thermocouple type.

POWER METER

The power meter in *Figure 12* is a good example of minimum-parts-count design. It uses only one transistor pair to provide the complete (X) • (Y) function. The circuit is intended for 117 V_{AC} ± 50 V_{AC} operation, but can be easily modified for higher or lower voltages. It measures true (non-reactive) power being delivered to the load and requires no external power supply. Idling power drain is only 0.5W. Load current sensing voltage is only 10 mV, keeping load voltage loss to 0.01%. Rejection of reactive load currents is better than 100:1 for linear loads. Nonlinearity is about 1% full scale when using a 50 μA meter movement. Temperature correction for gain is accomplished by using a copper shunt (+0.32%/°C) for load-current sensing. This circuit measures power on negative cycles only, and so cannot be used on rectifying loads.

LOW COST MATHEMATICAL FUNCTIONS

Many analog circuits require a mathematical function to be performed on one or more signals other than the standard addition, subtraction, or scaling which can be accomplished with resistor networks. The circuits shown in *Figures 13* through *15* are examples of low-cost function generating circuits using the LM394 with operational amplifiers. The logarithmic relationship of V_{BE} to I_C on the LM394 is utilized in each case to log-antilog the input signals so that addition and subtraction can be used to multiply, divide, square, etc. When transistors are used in this manner, matching is very critical. A 1 mV offset in V_{BE} appears as a *4% of signal* error even in the best case where operation is restricted to one quadrant. Parasitic emitter or base resistance (r_{ee}', r_{bb}') can also seriously degrade accuracy. At I_C = 100 μA and h_{FE} = 100, each Ω of emitter resistance and each 100Ω of base resistance will cause 0.4% signal error. Most matched transistor pairs available today have significant parasitic resistances which severely limit their use in high-accuracy circuits. The LM394, with offset guaranteed below 0.15 mV and a typical emitter-referred total parasitic resistance of 0.4Ω gives an order of magnitude improvement in accuracy to nonlinear designs at all current levels.

MULTIPLIER/DIVIDER

The circuit in *Figure 13* will give an output proportional to the product of the (X) and (Y) inputs divided by the Z input. All inputs must be positive, limiting operation to one quadrant, but this restriction removes the large error terms found in 2- and 4-quadrant designs. In a large percentage of cases, analog signals requiring multiplication are of one polarity only and can be inverted if negative. A nice feature of this design is that all gain errors can be trimmed to zero at one point. R_5 is paralleled with 2.4 MΩ to drop its nominal value 2%. R_8 then gives a ±2% gain trim to account for errors in R_1, R_2, R_5, R_7, and any offset in Q_1 or Q_2. For very low level inputs, offset voltage in the LM308s may create large percentage errors referred to input. A simple scheme for offsetting any of the LM308s to zero is shown in dotted lined; the + input of the appropriate LM308 is simply tied to R_x instead of ground for zeroing. The summing mode of operation on all inputs allows easy scaling on any or all inputs. Simply set the input resistor equal to ($V_{IN(max)}$)/(200 μA). V_{OUT} is equal to:

$$V_{OUT} = \frac{\left(\frac{X}{R_1}\right)\left(\frac{Y}{R_2}\right)(R_5)}{\frac{Z}{R_7}}$$

Input voltages above the supply voltage are allowed because of the summing mode of operation. Several inputs may be summed at ''X'', ''Y,'' or ''Z.''

Proper scaling will improve accuracy by preventing large current imbalances in Q_1 and Q_2, and by creating the largest possible output swing. Keep in mind that any multiplier scheme must have a reference and this circuit is no different. For a simple (X) • (Y) or (X)/Z function, the unused input must be tied to a reference voltage. Perturbations in this reference will be seen at the output as scale factor changes, so a stable reference is necessary for precision work. For less critical applications, the unused input may be tied to the positive supply voltage, with R = V^+/200 μA.

SQUARE ROOT

The circuit in *Figure 14* will generate the square root function at low cost and good accuracy. The output is a current which may be used to drive a meter directly or be converted to a voltage with a summing junction current-to-voltage converter. The −15V supply is used as a reference, so it must be stable. A 1% change in the −15V supply will give a ½% shift in output reading. No positive supply is required when an LM301A is used because its inputs may be used at the same voltage as the positive supply (ground). The two 1N457 diodes and the 300 kΩ resistor are used to temperature compensate the current through the diode-connected ½ LM394.

SQUARING FUNCTION

The circuit in *Figure 15* will square the input signal and deliver the result as an output current. Full scale input is 10V, but this may be changed simply by changing the value of the 100 kΩ input resistor. As in the square root circuit, the −15V supply is used as the reference. In this case, however, a 1% shift in supply voltage gives a 1% shift in output signal. The 150 kΩ resistor across the base-emitter of ½ LM394 provides slight temperature compensation of the reference current from the −15V supply. For improved accuracy at low input signal levels, the offset voltage of the LM301A should be zeroed out, and a 100 kΩ resistor should be inserted in the positive input to provide optimum DC balance.

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1. See National's *Audio Handbook*.

2. *The Audio Amateur*, volume VIII, number 1, Feb. 1977.

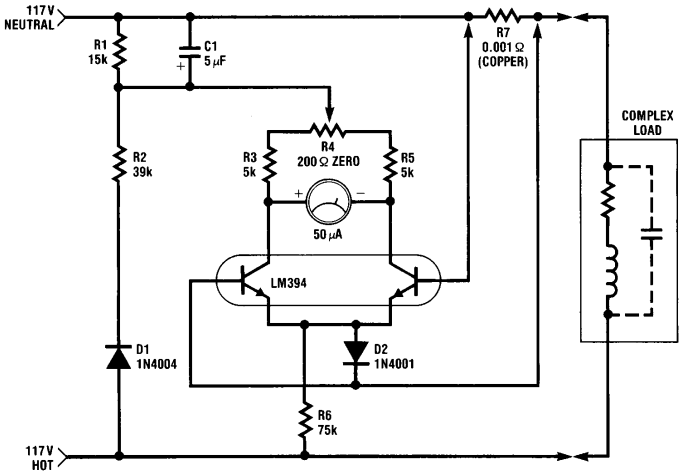

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FIGURE 12. Power Meter (1 kW f.s.)

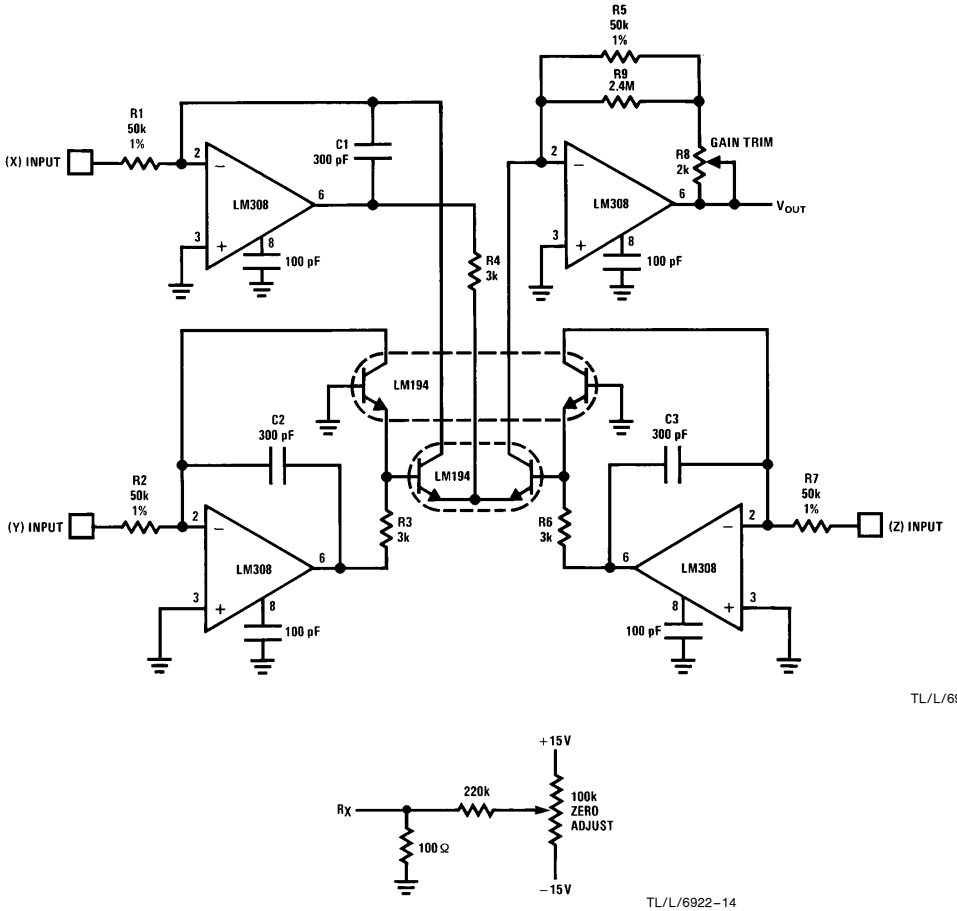

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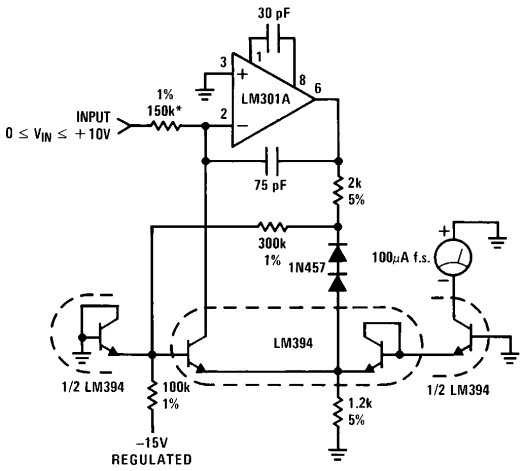
FIGURE 13. High Accuracy One Quadrant Multiplier/Divider



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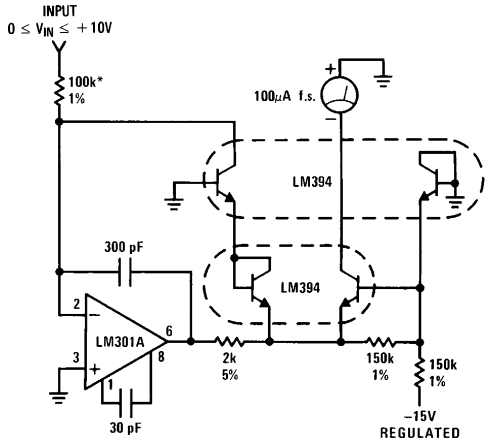
*Trim for full scale accuracy.

FIGURE 14. Low Cost Accurate Square Root Circuit
$I_{OUT} = 10^{-5}\sqrt{10\ V_{IN}}$



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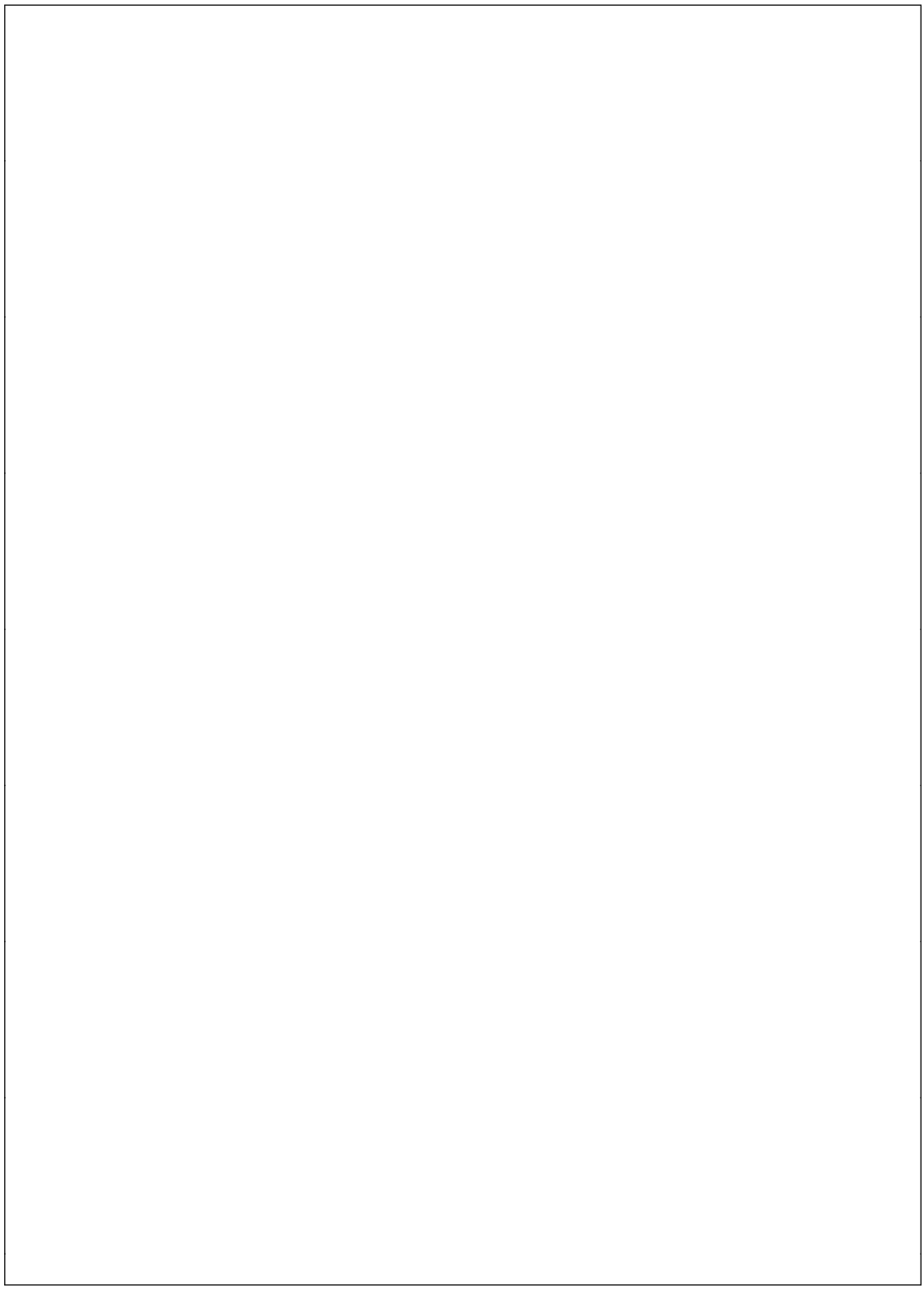
*Trim for full scale accuracy.

FIGURE 15. Low Cost Accurate Squaring Circuit
$I_{OUT} = 10^{-6}\,(V_{IN})^2$



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