AR598

Avalanche Capability of Today's Power Semiconductors

ON Semiconductor™

http://onsemi.com

R Borras, P Aloisi, D Shumate*
ON Semiconductor, France, USA*
Paper published at the EPE Conference '93, Brighton 9/93.

ARTICLE REPRINT

Abstract. Power semiconductors are used to switch high currents in fractions of a second and therefore belong inherently to a world of voltage spikes. To avoid unnecessary breakdown voltage guardbands, new generations of semiconductors are now avalanche rugged and characterized in avalanche energy.

This characterization is often far from application conditions and thus quite useless to the designer. It is easy to verify that an energy rating is not the best approach to a ruggedness quantification because of avalanche energy fluctuations with test conditions.

A physical and thermal analysis of the failure mechanisms leads to a new characterization method generating easy–to–use data for safe designs. The short–term avalanche capability will be discussed with an insight of the different technologies developed to meet these new ruggedness requirements.

Keywords. Avalanche, breakdown, unclamped inductive switching energy, safe operating areas.

INTRODUCTION

One obvious trend for new power electronic designs is to work at very high switching frequencies in order to reduce the volume and weight of all the capacitive and inductive elements. The consequence is that most applications today require switching very high currents in fractions of a microsecond and therefore generate L x dI/dt voltage spikes due to parasitic inductance. Unfortunately these undesirable voltage levels sometimes reach the breakdown voltage of power semiconductors that are not intended to be used in avalanche.

The necessity for avalanche rugged power semiconductors has clearly been perceived by many semiconductor manufacturers who have come up with avalanche–energy rated devices.

This paper will show the limits of an energy–based characterization model. It will concentrate on three different devices: Ultra Fast recovery Rectifiers, Schottky Barrier Rectifiers and MOSFETs. It will study their main failure mechanisms and show the technological improvements that guarantee an enhanced ruggedness.

This will lead to a new characterization that will help the designer choose correctly between overall cost and reliability.

LIMITS OF AN AVALANCHE ENERGY CHARACTERIZATION

Practically all the characterizations are based on the following Unclamped Inductive Switching (UIS) test circuit (Fig 1).

The energy is first stored in inductor L by turning on transistor Q for a period of time proportional to the peak current desired in the inductor. When Q is turned off, the inductor reverses its voltage and avalanches the Device Under Test until all its energy is transferred. The DUT can be a rectifier or a MOSFET (the gate should always be shorted to the source).

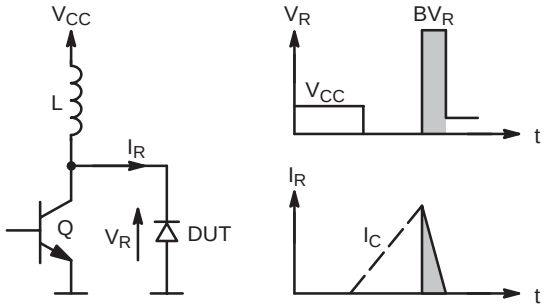

Figure 1. Standard UIS Characterization Circuit.

The standard characterization method consists in increasing the peak current in the inductor until the device fails. The energy that the device can sustain without failing becomes a figure of merit of the ruggedness to avalanche:

$$Waval = 1/2\ L\ I_{peak}^2\ BV_{(DUT)} / (BV_{(DUT)} - V_{CC}) \qquad [1]$$

The main limit of this method is that the energy level that causes a failure in the DUT is not a constant but a function of L and V_{CC}. This results of the fact that the avalanche duration is function of the current decay slope $(BV_{(DUT)}–V_{CC})/L$:

Table 1. Peak Current and Energy Causing Failures in a 1 A, 1000 V Ultra Fast Recovery Rectifier.

Inductor Value:	10 mH	50 mH	100 mH
Peak Current:	1.7 A	0.9 A	0.8 A
Energy:	14 mJ	20 mJ	32 mJ

Table 1 indicates that the failure is not caused by an energy (i.e. it is not independent of the avalanche duration) but rather by a current level that has to be derated versus time: the devices can sustain a low current for a long period of time (high energy) but at high avalanche currents they will fail after a few microseconds (low energy).

Therefore, unless the designer has a parasitic inductance of value L in his circuit, the standard characterization data will be useless, or worse, it might lead to an overestimate of the ruggedness of his application: because parasitic inductances are often an order of magnitude less than the test circuit inductance, the expected energy capability leads to excessive current levels.

The UIS test circuit is very easy to implement: the only important point is that the transistor has to have a breakdown voltage higher than the DUT. For low breakdown voltage devices, a MOSFET might be preferred to the bipolar transistor.

The advantages of using a MOSFET are multiple: it is a more rugged device, it is much easier to drive and its switching characteristics can be controlled by adding a resistor in series with the gate. It is mandatory to limit this switching speed to avoid having an avalanche energy measurement dependent on the gate drive (i.e. gate resistor and gate to source voltage values).

Anyhow, it is possible to generate very useful information with this UIS test circuit by varying the inductor value. It is also very important to present the data independently of the values of V_{CC} and L. One solution can be to plot the maximum peak current versus the avalanche duration (Fig 2):

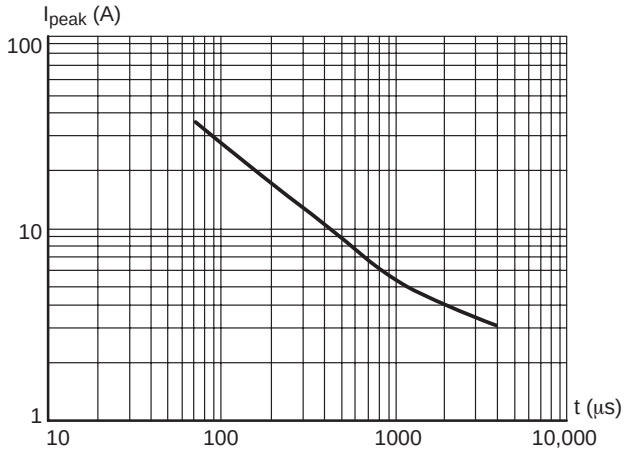

Figure 2. Maximum Peak Current versus Avalanche Duration for a 15 A, 60 V MOSFET in an UIS Test Circuit.

The advantage of this new graph is that the designer can easily calculate the safety margin of his application and he will not be mislead by an energy value that depends on too many different parameters. If he knows the value of the parasitic inductance in his circuit he will be able to determine its maximum peak current.

For instance, let us assume that the designer uses the 15 A, 60 V MOSFET characterized in Figure 2. This device sustains 500 mJ with an inductor of 75 mH according to equation [1]. Its typical breakdown voltage is 80 V.

If the supply voltage V_{DD} is 12 V and the parasitic inductance L is 250 μH, then the avalanche duration and maximum peak current are related by

$$I_{peak} = t\,(BV_{DSS} - V_{DD}) / L \qquad [2]$$

This relationship can be added to Figure 2 (see Fig 3):

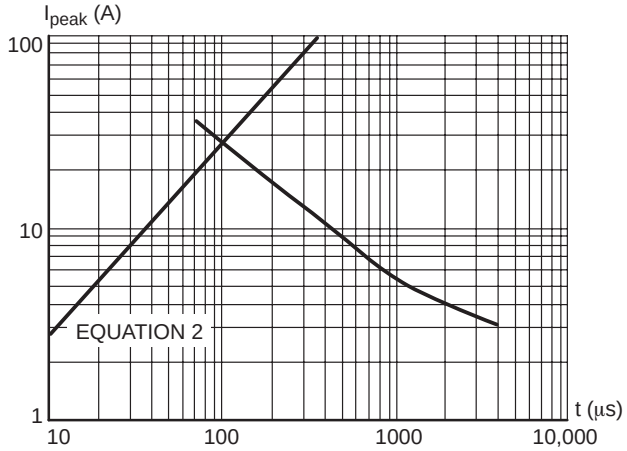

Figure 3. Figure 2 + equation [2].

Thus the maximum peak current that can flow through the parasitic inductance L is approximately 28 A instead of 58 A that would have resulted of using equation [1].

UNDERSTANDING THE FAILURE MECHANISMS

Physical Approach

The following microscope photographs show the failure locations for an Ultra Fast Recovery Rectifier (UFR), a Schottky Barrier Rectifier (SBR) and a MOSFET:

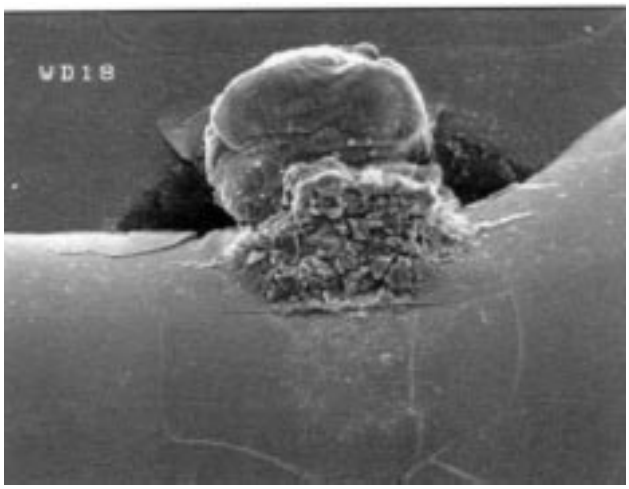

Figure 4. 4 A, 1000 V UFR Avalanche Failure.

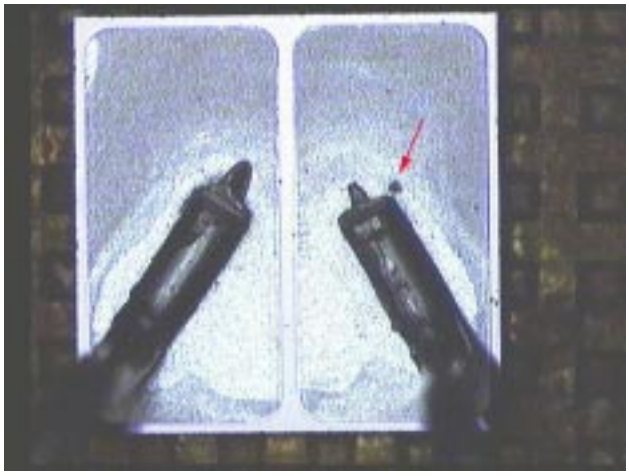

Figure 5. 25 A, 35 V SBR Avalanche Failure.

Figure 6. 20 A, 500 V MOSFET Avalanche Failure.

These photographs show that the failure is generally a punchthrough. The melt–through hole dimensions depend on the current level and avalanche duration.

A close look at the electrical characteristics of failed rectifiers on a curve tracer show three levels of degradation: low stressed diodes have a normal forward characteristic but show an unusual leakage current before entering breakdown as if they had a high–value resistor in parallel: this resistance can be explained by a small punchthrough. For medium degradation levels, the value of this pseudo–resistance decreases and becomes visible in the forward characteristic of the diode. Finally, when the punchthrough reaches considerable dimensions, the device looks very similar to a low value resistor.

The failure does not always appear in the same region of the die. For instance, high voltage UFRs have their punch-through always located in a corner, MOSFETs often fail in the corners or on the sides whereas SBRs have randomly located failures.

Thermal Approach

Transient thermal response graphs generated by a standard ΔV_{DS} method show the junction temperature evolution for forward and avalanche constant current conduction in a MOSFET. These graphs (Fig 7) prove that the silicon efficiency during avalanche and forward currents are similar.

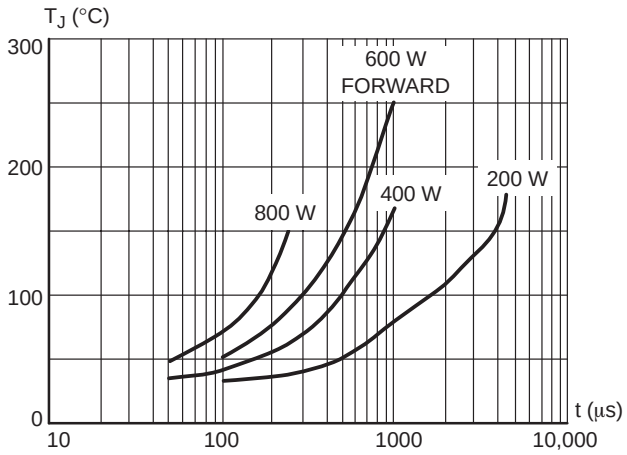

Figure 7. 15 A, 60 V MOSFET Transient Thermal Response for 800 W, 400 W, 200 W Avalanche and 600 W Forward Conduction.

Figure 7 can be used to generate a transient thermal resistance graph by plotting the temperature divided by the power: the four graphs should then normally match. Some slight differences show that the transient thermal resistance increases with the current level: i.e. the 800 W curve (10 A constant avalanche current) has a higher transient thermal resistance than the 200 W (2.5 A). Therefore the thermal efficiency in a MOSFET is not perfectly homogeneous versus the avalanche current.

A similar analysis on an UFR or an SBR shows poor thermal efficiency in avalanche. This can be shown by comparing the temperature rise after 1 ms for forward and avalanche conduction pulses of same power (400 W):

MOSFET	ΔT_{direct}=160°C	$\Delta T_{avalanche}$=180°C	ratio=0.9
UFR	ΔT_{direct}=120°C	$\Delta T_{avalanche}$=175°C	ratio=0.7
SBR	ΔT_{direct}=100°C	$\Delta T_{avalanche}$=150°C	ratio=0.7

Electrical Approach

Considering the transient thermal responses of a device, it is possible to simulate the instantaneous junction temperature for any sort of power pulse.

Conducting this simulation on the data generated by the UIS test it is possible to show that all the parts fail when they reach a “critical temperature” (Fig 8):

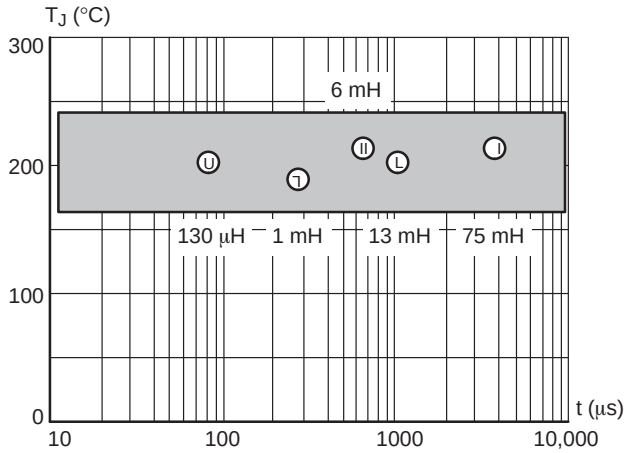

Figure 8. 15A, 60V MOSFET Failure Points and Critical Temperature for different Inductor Values.

At these critical temperatures the intrinsic carrier concentration, ni, reaches levels close to those of the doping concentrations:

$$ni \text{ is proportional to } T^{3/2} e^{-Eg/2kT} \quad [3]$$

where T is the absolute temperature, Eg the energy bandgap and k is Boltzmann’s constant.

At 200°C, ni exceeds 2 10^{14} cm^{-3} which corresponds to a 1000 V material epitaxy concentration level. This means that when the junction temperature reaches 300°C, the rectifier looks more like a resistor than a diode. A local thermal runaway then generates a hot spot and a punchthrough as can be seen in Figures 4, 5 and 6.

This failure analysis has shown that the failure mechanism is essentially thermal: the devices are heated by the BV_R x I_R power dissipation. Unfortunately, this power does not remain constant because the UIS circuit generates a linear current decay and also the breakdown voltage varies with the current level and with the junction temperature.

In order to have a complete characterization of the device it is interesting to see how it reacts to a constant avalanche current and different ambient temperatures.

NEW CHARACTERIZATION METHOD PROPOSAL

During the prototype phase, it is easier for the designer to measure the avalanche current and duration than the circuit’s parasitic inductance. Therefore, the characterization should be based on easy to measure parameters. The failure analysis proves that the main cause of degradation is the inability to handle an excessive power (avalanche current I_R multiplied by breakdown voltage BV_R). A proper characterization should present the maximum power capability versus time.

As the avalanche voltage varies only slightly with the current level, the proposed method is based on avalanching a device at a constant current and presenting the maximum current capability versus time:

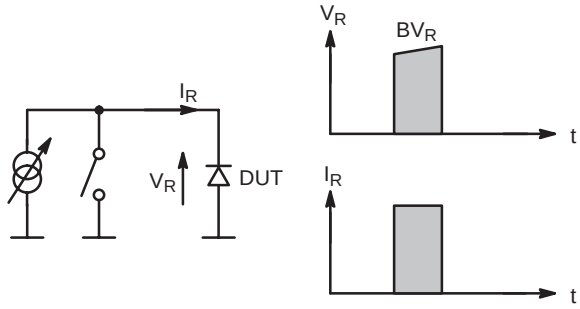

Figure 9. Constant Current Characterization Circuit.

Different test circuits similar to Figure 9 have been proposed by Gauen (1) and Pshaenich (2). Some unexpected failures in MOSFETs suggest that the DUT should always be referenced to ground. Unlike UFRs and SBRs, MOSFETs react differently whether they are tied to ground or floating around a fluctuating voltage. Many floating transistors fail at very low stress levels probably due to capacitive coupled currents that turn–on the internal parasitic transistor.

The test circuit shown in Figure 9 sets a constant avalanche current through the device until it fails, this duration can then be plotted for different current levels. This generates a graph similar to the UIS method, except that the current is constant instead of decreasing linearly.

This leads to the definition of a “Safe Avalanching Area” (Fig 10) that will guarantee a short–term reliability if the device is used within this clearly defined area.

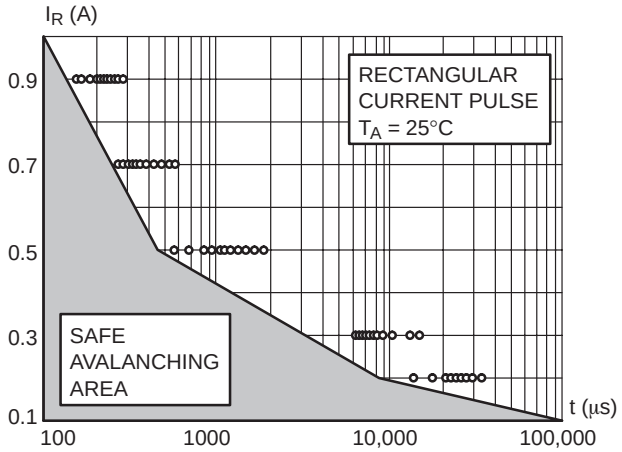

Figure 10. 1 A, 30 V SBR Save Avalanching Area.

This graph gives the maximum avalanche duration for any value of avalanche current.

The Safe Avalanching Area is generated by taking a safety margin from the failure points. Another approach would be to dynamically measure the temperature as in Figure 7 and generate an area defined by a maximum allowable junction temperature.

As the failure mechanism is related to a peak junction temperature, it is necessary to give Safe Avalanching Areas for different ambient temperatures (Fig 11):

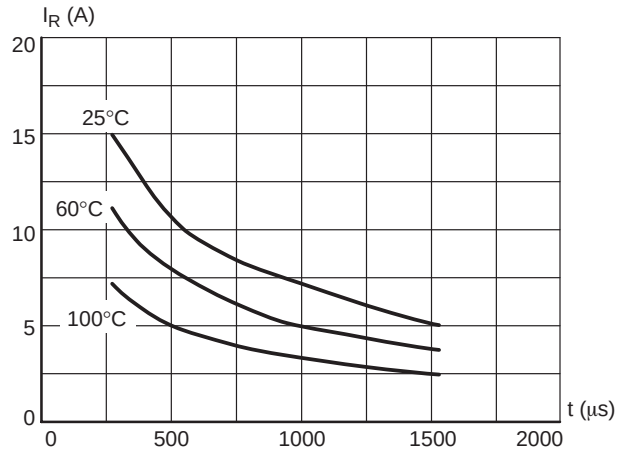

Figure 11. 25 A, 35 V SBR Safe Avalanching Areas for different ambient temperatures.

When the data in Figures 10 and 11 is plotted on log/log axes instead of lin/log or lin/lin, an interesting feature appears (Fig 12):

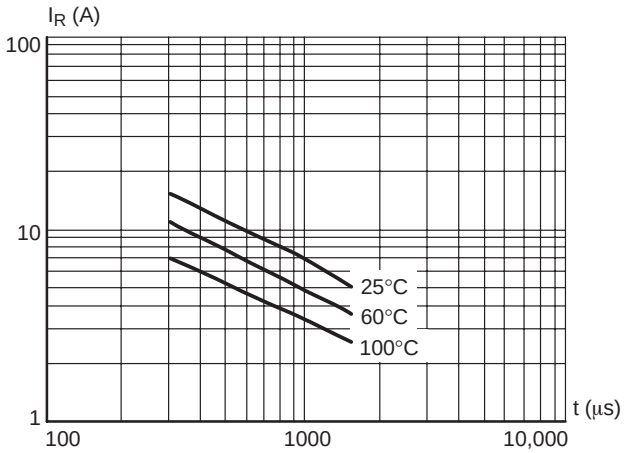

Figure 12. Figure 12 on log/log axes.

Figure 12 shows a linear relationship between current and time on a log/log plot. This means that:

$$\text{so} \quad \begin{aligned} &\log(I_R) = A \log(t) + B, \\ &I_R = k\, T^A \end{aligned} \qquad [4]$$

where k is a constant function of the die size, the breakdown voltage and other parameters. Constant A can be extracted from Figure 12 and similar figures for UFRs and MOSFETs:

$$I_R = k\, T^{-0.55} \qquad [5]$$

Relation [5] is a consequence of heat propagation laws which explain that the temperature in a semiconductor rises proportionally to $t^{0.5}$ (for a constant current pulse and as long as the temperature remains within the silicon die). This can be seen in any transient thermal resistance graph.

A standard thermal calculation shows that:

$$\text{or} \quad \begin{aligned} &T_J = T_A + P_D\, Rth_{JA}(t), \\ &P_D = (T_J - T_A) / Rth_{JA}(t) \end{aligned} \qquad [6]$$

where:

T_J, T_A are the junction and ambient temperatures,
P_D is the power dissipation,
$Rth_{JA}(t)$ is the transient thermal resistance.

Given a constant power pulse and for values of t less than 1 ms, [6] is equivalent to:

$$\text{so} \quad \begin{aligned} &I_R\, B_{VR} = (T_J - T_A) / (k\, t^{0.5}) \\ &I_R = k\, t^{-0.5} \end{aligned} \qquad [7]$$

This relation is similar to [5]. For avalanche durations of less than 500 μs the heat propagates within the silicon only. For longer durations the heat reaches the solder and the package so the propagation characteristics are modified. The devices heat faster or slower and therefore the I_R=f(t) slope changes. Empirical data shows that A in relation [4] remains within –0.5 to –0.6.

Relation [7] can also be expressed by:

$$I_R^2\, t = k \qquad \text{(k:constant)} \qquad [7bis]$$

This rule of thumb works out much better than the, unfortunately too common, 1/2 L I^2 law.

For example, when applied to the example following Figure 2 (which is UIS and not Constant Current generated) to determine the maximum peak current in a 250 μH inductor and by choosing for instance the 9 A, 500 μs point, relation [7bis] can be written:

$$9A^2\ 500\ \mu s = Ipeak^2\ 100 \mu s$$

This gives a conservative value of 20 A instead of a real value of 28 A whereas the 1/2 L I^2 method generates a catastrophic 58 A value.

TECHNOLOGY TRADEOFFS

Ultra Fast Recovery Rectifiers

The UFR devices are based on a Mesa technology (Fig 13) with a Phosphorus doped (n–type) substrate. The heavily doped N+ substrate is followed by a lighter N– epitaxial layer. The P+ is diffused into the epitaxy to form the P–N junction. The passivation follows the perimeter of the die.

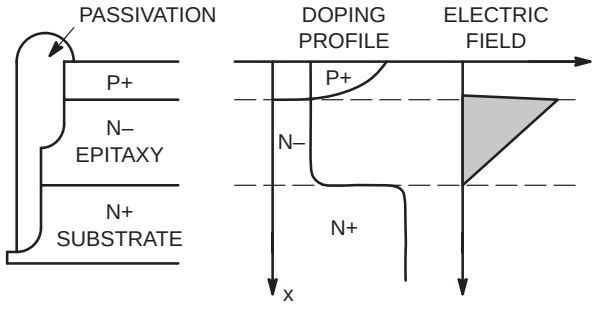

Figure 13. UFR Technology, Profile and Electric Field.

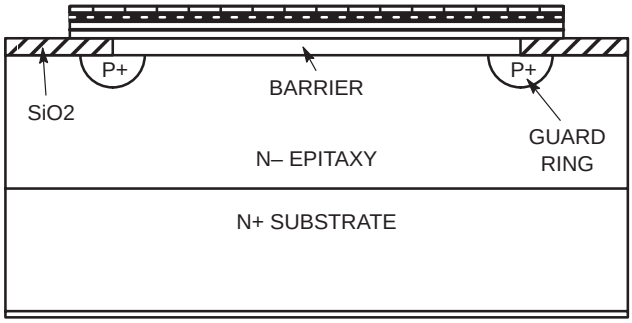

Figure 14. SBR Technology with P–N Guard Rings

The epitaxy characteristics determine the major electrical parameters of the device. A designed experiment was conducted varying the epitaxy thickness and resistivity. The output responses were the forward voltage, the breakdown voltage, the leakage current and the avalanche capability. A wide range of epitaxy materials was chosen to determine the general trends for all the effects.

Although the results were predictable for the static parameters, the avalanche capability results were not.

A key issue is the electric field extension. If it terminates before the substrate the avalanche capability increases by increasing the epitaxy resistivity. If the field extends into the N+ region (reach–through) the avalanche capability is considerably reduced.

The avalanche capability is proportional to the die size and not to the perimeter. This confirms that the avalanche current is vertical and not only a surface or passivation related phenomenon.

The failures always occur in the corners where the electric field is most critical. These failures are essentially function of the thermal characteristics of the device when conducting avalanche currents. Therefore the avalanche capability decreases when the ambient temperature increases and the failures can normally be predicted by Safe Avalanching Areas such as Figure 12.

Some unexpected defects though can radically degrade the avalanche capability. Defects in the epi such as pipes cause premature failures but can often be screened by a leakage current test that eliminates soft breakdown devices. Defects in the passivation can generate parasitic oscillations during breakdown.

Schottky Rectifiers

Due to P–N junction guard rings, SBR devices are very similar to UFRs when conducting avalanche currents. These rectifiers have very low breakdown voltages and therefore very thin epitaxy layers. This probably explains that the avalanche–related failures occur anywhere on the die surface: the thin N– region is relatively more heterogeneous with respect to avalanche capability and thermal dissipation than a thick UFR epitaxy.

MOSFETs

MOSFETs can also be compared to UFRs as long as the internal parasitic bipolar transistor (due to the P–tub) does not turn–on. The latest MOSFET generations reduce the P– resistance to avoid biasing this NPN.

While analyzing different constant current test circuits, it appeared that devices used in a floating configuration can have very poor avalanche capabilities.

Due to their cellular technology, MOSFETs conduct very efficiently avalanche currents. They can sustain avalanche power levels close to those of forward conduction ratings.

CONCLUSION

The necessity of characterizing the avalanche capability of power semiconductors has been explained. An analysis of the standard UIS test circuit has shown the limits of a characterization based on energy ratings. Throughout a discussion of the main failure mechanisms, a new thermal approach has been proposed to help designers set safety levels in their designs. This paper sets new standards for characterizing avalanche ruggedness.

Acknowledgements

The authors would like to thank Jean–Michel REYNES, design engineer at ON Semiconductor Toulouse, for his help in understanding the failure mechanisms.

References

1. Gauen, K., 1987, “Specifying Power MOSFET Avalanche Stress Capability”, Power Technics Magazine, January
2. Pshaenich, A., 1985, “Characterizing Overvoltage Transient Suppressors”, Powerconversion International, June/July
3. Cherniak, S., “A Review of Transients and The Means of Suppression”, ON Semiconductor Application Note AN843
4. Wilhardt, J., “Transient Power Capability of Zener Diodes”, ON Semiconductor Application Note AN784

PUBLICATION ORDERING INFORMATION

GLOBAL Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative