

MC10ELT22, MC100ELT22

5V Dual TTL to Differential PECL Translator

The MC10ELT/100ELT22 is a dual TTL to differential PECL translator. Because PECL (Positive ECL) levels are used only +5 V and ground are required. The small outline 8-lead package and the low skew, dual gate design of the ELT22 makes it ideal for applications which require the translation of a clock and a data signal.

- 1.2 ns Typical Propagation Delay
- < 300 ps Typical Output to Output Skew
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts
- Operating Range: $V_{CC} = 4.75 \text{ V}$ to 5.25 V with $GND = 0 \text{ V}$
- No Internal Input Pulldown Resistors

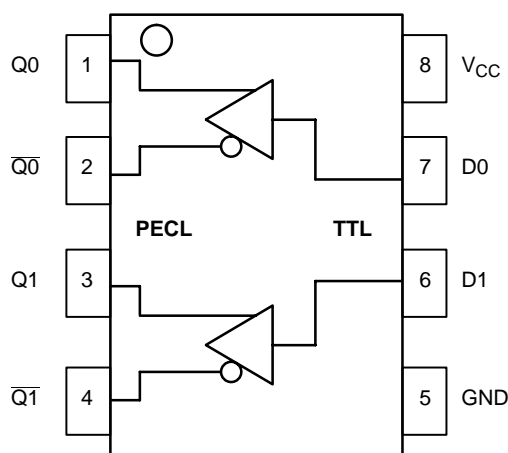


Figure 1. Logic Diagram and Pinout Assignment

PIN DESCRIPTION

PIN	FUNCTION
$Q_n, \overline{Q_n}$	PECL Differential Outputs*
D_n	TTL Inputs
V_{CC}	Positive Supply
GND	Ground

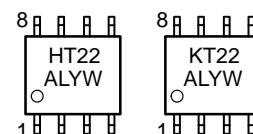
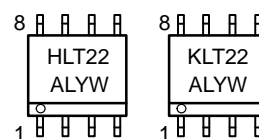
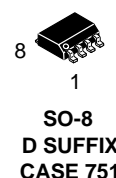
* Output state undetermined when inputs are open.



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MARKING DIAGRAMS*



H = MC10
K = MC100
A = Assembly Location

L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping**
MC10ELT22D	SO-8	98 Units/Rail
MC10ELT22DR2	SO-8	2500 Tape & Reel
MC100ELT22D	SO-8	98 Units/Rail
MC100ELT22DR2	SO-8	2500 Tape & Reel
MC10ELT22DT	TSSOP-8	98 Units/Rail
MC10ELT22DTR2	TSSOP-8	2500 Tape & Reel
MC100ELT22DT	TSSOP-8	98 Units/Rail
MC100ELT22DTR2	TSSOP-8	2500 Tape & Reel

**For additional tape and reel information, see Brochure BRD8011/D.

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ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model	> 2 KV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	51
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V		7	V
V_{IN}	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	7	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

MC10ELT22, MC100ELT22

10ELT SERIES PECL DC CHARACTERISTICS $V_{CC} = 5.0 \text{ V}$; GND = 0.0 V (Note 3)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			22			22			22	mA
V_{OH}	Output HIGH Voltage (Note 4)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 4)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

3. Output parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.25 \text{ V}$.

4. Outputs are terminated through a 50 ohm resistor to $V_{CC} - 2 \text{ volts}$.

100ELT SERIES PECL DC CHARACTERISTICS $V_{CC} = 5.0 \text{ V}$; GND = 0.0 V (Note 5)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			22			22			22	mA
V_{OH}	Output HIGH Voltage (Note 6)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 6)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

5. Output parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.25 \text{ V}$.

6. Outputs are terminated through a 50 ohm resistor to $V_{CC} - 2 \text{ volts}$.

TTL INPUT DC CHARACTERISTICS $V_{CC} = 4.75 \text{ V}$ to 5.25 V ; $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	$V_{IN} = 2.7 \text{ V}$			20	μA
I_{IHH}	Input HIGH Current	$V_{IN} = 7.0 \text{ V}$			100	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.5 \text{ V}$			-0.6	mA
V_{IK}	Input Clamp Diode Voltage	$I_{IN} = -18 \text{ mA}$			-1.2	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

AC CHARACTERISTICS $V_{CC} = 4.75 \text{ V}$ to 5.25 V ; GND = 0.0 V

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Input Frequency					500					MHz
t_{PLH}	Propagation Delay (Note 7) 1.5 V to 50%	0.6		1.2	0.9	1.2	1.5	0.6		1.35	ns
t_{PHL}	Propagation Delay (Note 7) 1.5 V to 50%	0.4		1.0	0.5	0.8	1.1	0.7		1.30	ns
t_{skew}	Within-Device Skew (Note 8) Device-to-Device Skew (Note 9)		50 300	100 600		50 300	100 600		50 350	100 750	ps
t_{JITTER}	Random Clock Jitter (RMS)					0.5					ps
t_r/t_f	Output Rise/Fall Time (20-80%)	0.4		1.6	0.4		1.6	0.4		1.6	ns

7. Specifications for standard TTL input signal.

8. Skew is measured between outputs under identical transitions and conditions on any one device.

9. Device-to-Device Skew for identical transitions at identical V_{CC} levels.

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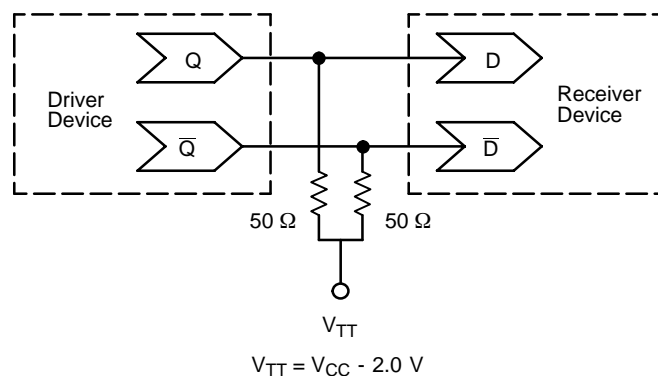


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 - Termination of ECL Logic Devices.)

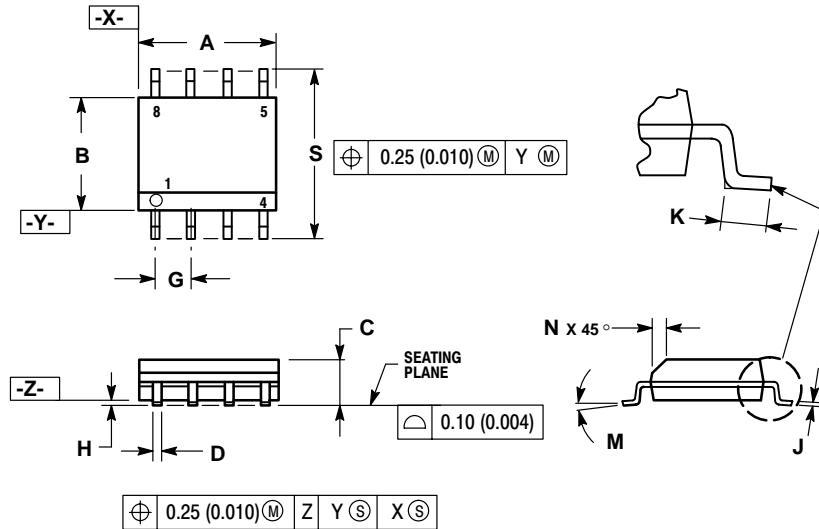
Resource Reference of Application Notes

AN1404	- ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
AN1405	- ECL Clock Distribution Techniques
AN1406	- Designing with PECL (ECL at +5.0 V)
AN1503	- ECLinPS I/O SPICE Modeling Kit
AN1504	- Metastability and the ECLinPS Family
AN1560	- Low Voltage ECLinPS SPICE Modeling Kit
AN1568	- Interfacing Between LVDS and ECL
AN1596	- ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	- Using Wire-OR Ties in ECLinPS Designs
AN1672	- The ECL Translator Guide
AND8001	- Odd Number Counters Design
AND8002	- Marking and Date Codes
AND8020	- Termination of ECL Logic Devices
AND8090	- AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

