

# DATA SHEET

## **BSS110**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC07

1995 Apr 07

**Philips Semiconductors**



**PHILIPS**

P-channel enhancement mode  
vertical D-MOS transistor

BSS110

FEATURES

- Low threshold voltage
- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

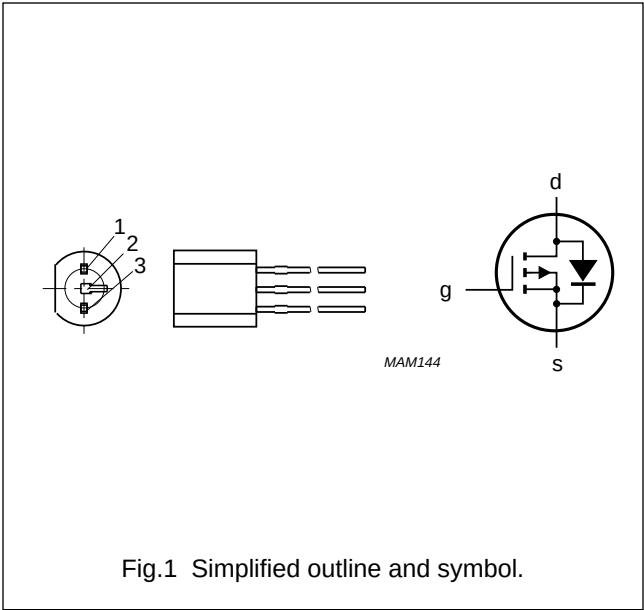
- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

PINNING - TO-92 variant

| PIN | SYMBOL | DESCRIPTION |
|-----|--------|-------------|
| 1   | s      | source      |
| 2   | g      | gate        |
| 3   | d      | drain       |



CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

| SYMBOL     | PARAMETER                        | CONDITIONS                                       | MIN. | MAX.     | UNIT     |
|------------|----------------------------------|--------------------------------------------------|------|----------|----------|
| $V_{DS}$   | drain-source voltage (DC)        |                                                  | –    | –50      | V        |
| $V_{GSO}$  | gate-source voltage (DC)         | open drain                                       | –    | $\pm 20$ | V        |
| $V_{GSth}$ | gate-source threshold voltage    | $I_D = -1\text{ mA}$ ; $V_{DS} = V_{GS}$         | –0.8 | –2       | V        |
| $I_D$      | drain current (DC)               |                                                  | –    | –170     | mA       |
| $R_{DSon}$ | drain-source on-state resistance | $I_D = -170\text{ mA}$ ; $V_{GS} = -10\text{ V}$ | –    | 10       | $\Omega$ |
| $P_{tot}$  | total power dissipation          | up to $T_{amb} = 25\text{ }^\circ\text{C}$       | –    | 830      | mW       |

# P-channel enhancement mode vertical D-MOS transistor

BSS110

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL    | PARAMETER                      | CONDITIONS                                            | MIN. | MAX.     | UNIT               |
|-----------|--------------------------------|-------------------------------------------------------|------|----------|--------------------|
| $V_{DS}$  | drain-source voltage (DC)      |                                                       | –    | –50      | V                  |
| $V_{GSO}$ | gate-source voltage (DC)       | open drain                                            | –    | $\pm 20$ | V                  |
| $I_D$     | drain current (DC)             |                                                       | –    | –170     | mA                 |
| $I_{DM}$  | peak drain current             |                                                       | –    | –520     | mA                 |
| $P_{tot}$ | total power dissipation        | up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; note 1 | –    | 830      | mW                 |
| $T_{stg}$ | storage temperature            |                                                       | –65  | +150     | $^{\circ}\text{C}$ |
| $T_j$     | operating junction temperature |                                                       | –    | 150      | $^{\circ}\text{C}$ |

## THERMAL CHARACTERISTICS

| SYMBOL        | PARAMETER                                   | CONDITIONS | VALUE | UNIT |
|---------------|---------------------------------------------|------------|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient | note 1     | 150   | K/W  |

### Note to the “Limiting values” and “Thermal characteristics”

1. Device mounted on a printed-circuit board, maximum lead length 4 mm.

## CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

| SYMBOL                                    | PARAMETER                        | CONDITIONS                                                                                | MIN. | TYP. | MAX.     | UNIT          |
|-------------------------------------------|----------------------------------|-------------------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{(BR)DSS}$                             | drain-source breakdown voltage   | $V_{GS} = 0$ ; $I_D = -10\text{ }\mu\text{A}$                                             | –50  | –    | –        | V             |
| $V_{GSth}$                                | gate-source threshold voltage    | $V_{DS} = V_{GS}$ ; $I_D = -1\text{ mA}$                                                  | –0.8 | –    | –2       | V             |
| $I_{DSS}$                                 | drain-source leakage current     | $V_{GS} = 0$ ; $V_{DS} = -40\text{ V}$                                                    | –    | –    | –100     | nA            |
|                                           |                                  | $V_{GS} = 0$ ; $V_{DS} = -50\text{ V}$                                                    | –    | –    | –10      | $\mu\text{A}$ |
|                                           |                                  | $V_{GS} = 0$ ; $V_{DS} = -50\text{ V}$ ; $T_j = 125\text{ }^{\circ}\text{C}$              | –    | –    | –60      | $\mu\text{A}$ |
| $I_{GSS}$                                 | gate leakage current             | $V_{DS} = 0$ ; $V_{GS} = \pm 20\text{ V}$                                                 | –    | –    | $\pm 10$ | nA            |
| $R_{DSon}$                                | drain-source on-state resistance | $V_{GS} = -10\text{ V}$ ; $I_D = -170\text{ mA}$                                          | –    | –    | 10       | $\Omega$      |
| $ y_{fs} $                                | forward transfer admittance      | $V_{DS} = -25\text{ V}$ ; $I_D = -170\text{ mA}$                                          | 50   | –    | –        | mS            |
| $C_{iss}$                                 | input capacitance                | $V_{GS} = 0$ ; $V_{DS} = -25\text{ V}$ ; $f = 1\text{ MHz}$                               | –    | 25   | 45       | pF            |
| $C_{oss}$                                 | output capacitance               | $V_{GS} = 0$ ; $V_{DS} = -25\text{ V}$ ; $f = 1\text{ MHz}$                               | –    | 15   | 25       | pF            |
| $C_{rss}$                                 | reverse transfer capacitance     | $V_{GS} = 0$ ; $V_{DS} = -25\text{ V}$ ; $f = 1\text{ MHz}$                               | –    | 3.5  | 12       | pF            |
| <b>Switching times</b> (see Figs 2 and 3) |                                  |                                                                                           |      |      |          |               |
| $t_{on}$                                  | turn-on time                     | $V_{GS} = 0\text{ to }-10\text{ V}$ ; $V_{DD} = -40\text{ V}$ ;<br>$I_D = -200\text{ mA}$ | –    | 3    | –        | ns            |
| $t_{off}$                                 | turn-off time                    | $V_{GS} = -10\text{ to }0\text{ V}$ ; $V_{DD} = -40\text{ V}$ ;<br>$I_D = -200\text{ mA}$ | –    | 7    | –        | ns            |

P-channel enhancement mode  
vertical D-MOS transistor

BSS110

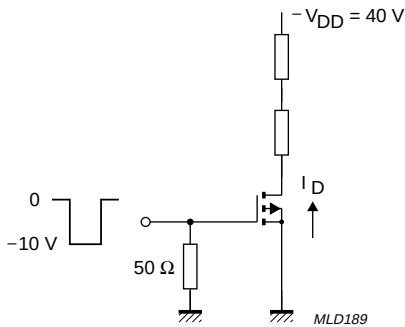


Fig.2 Switching time test circuit.

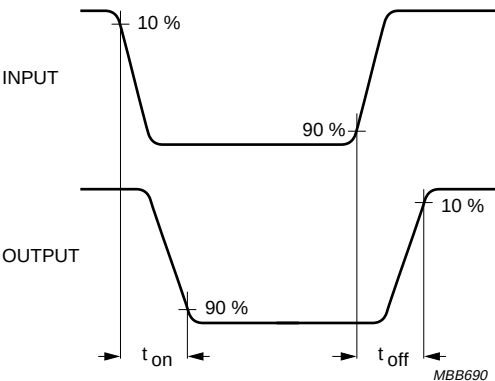


Fig.3 Input and output waveforms.

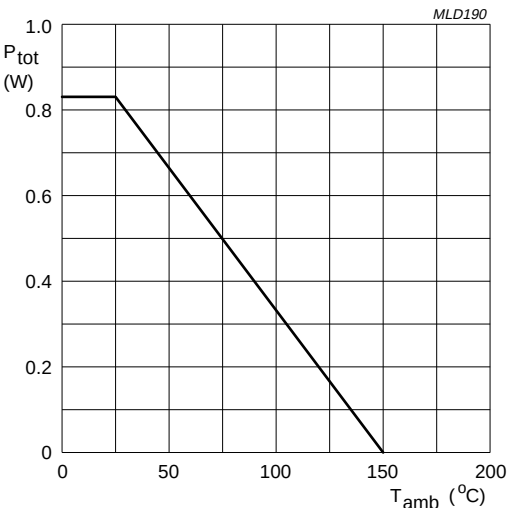
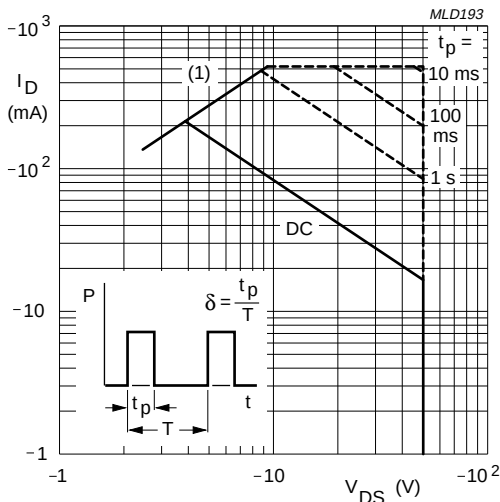


Fig.4 Power derating curve.

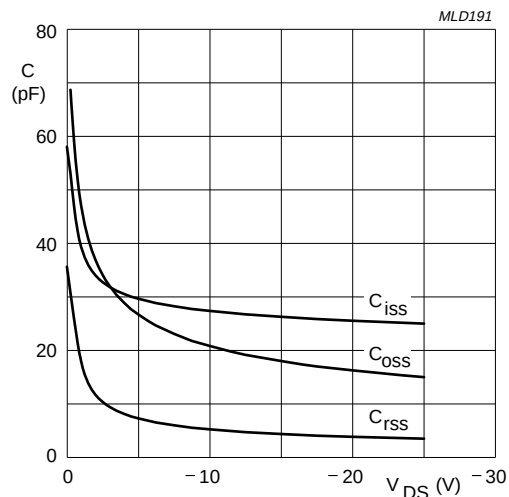


$\delta = 0.01$ .  
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ .  
(1)  $R_{DSon}$  limitation.

Fig.5 DC SOAR.

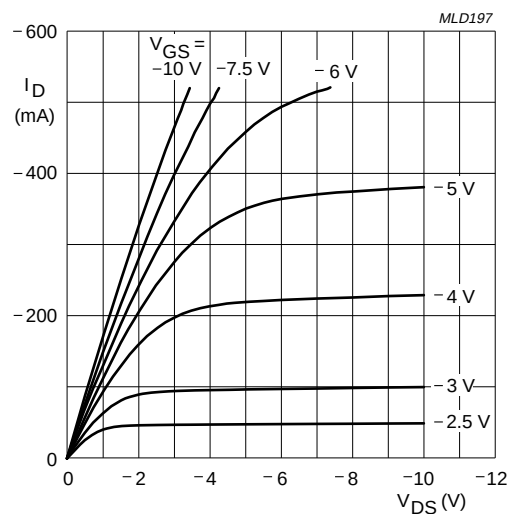
# P-channel enhancement mode vertical D-MOS transistor

## BSS110



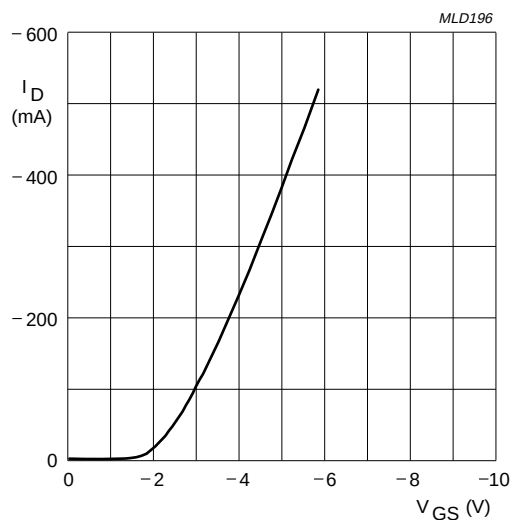
$V_{GS} = 0$ .  
 $T_j = 25^\circ\text{C}$ .  
 $f = 1\text{ MHz}$ .

Fig.6 Capacitance as a function of drain source voltage; typical values.



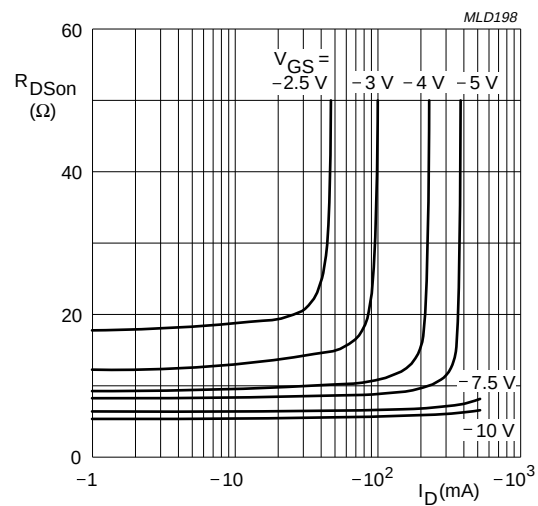
$T_j = 25^\circ\text{C}$ .

Fig.7 Typical output characteristics.



$V_{DS} = -10\text{ V}$ .  
 $T_j = 25^\circ\text{C}$ .

Fig.8 Typical transfer characteristics.

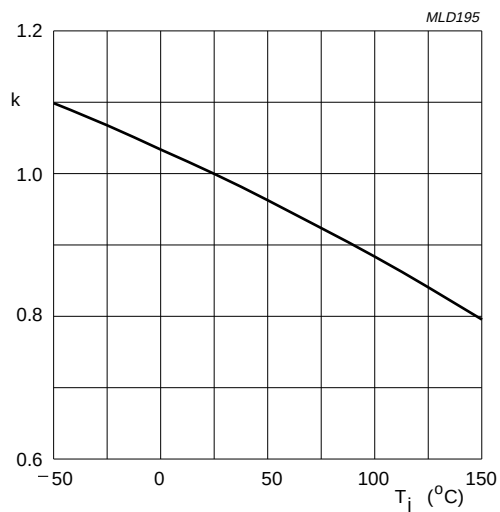


$T_j = 25^\circ\text{C}$ .

Fig.9 Drain-source on-state resistance as a function of drain current; typical values.

# P-channel enhancement mode vertical D-MOS transistor

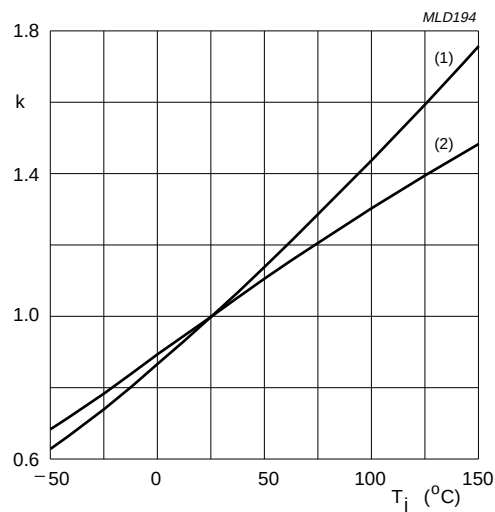
BSS110



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25^\circ\text{C}}$$

$I_D = -1 \text{ mA}; V_{DS} = V_{GS}.$

Fig.10 Temperature coefficient of gate-source threshold voltage.

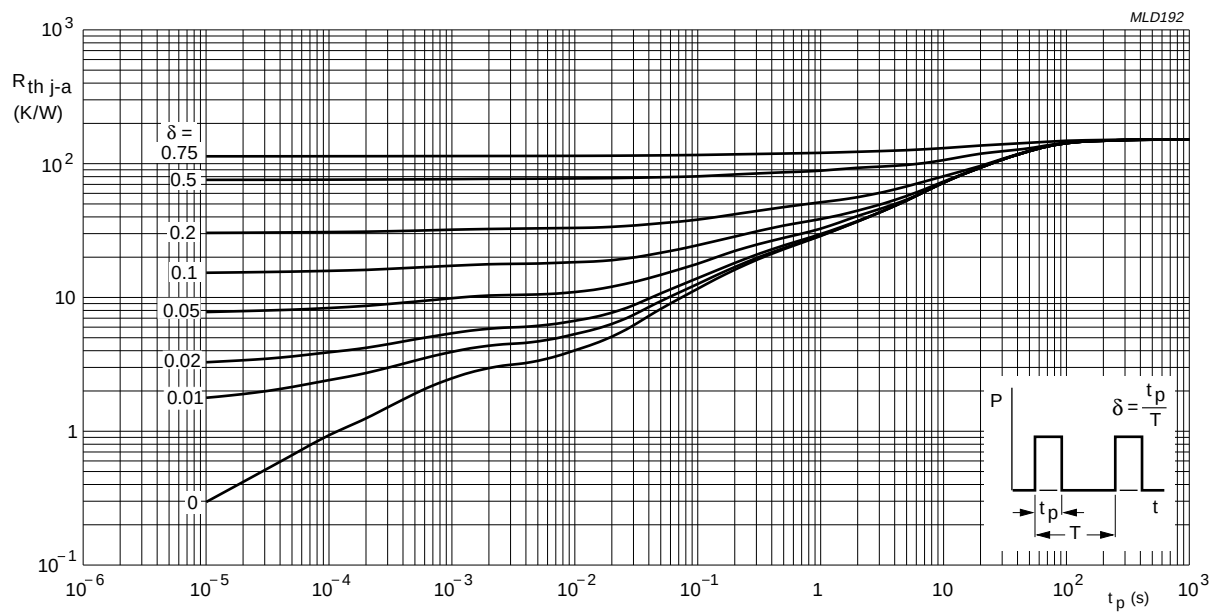


$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

(1)  $I_D = -170 \text{ mA}; V_{GS} = -10 \text{ V}.$

(2)  $I_D = -20 \text{ mA}; V_{GS} = -2.4 \text{ V}.$

Fig.11 Temperature coefficient of drain-source on-state resistance.



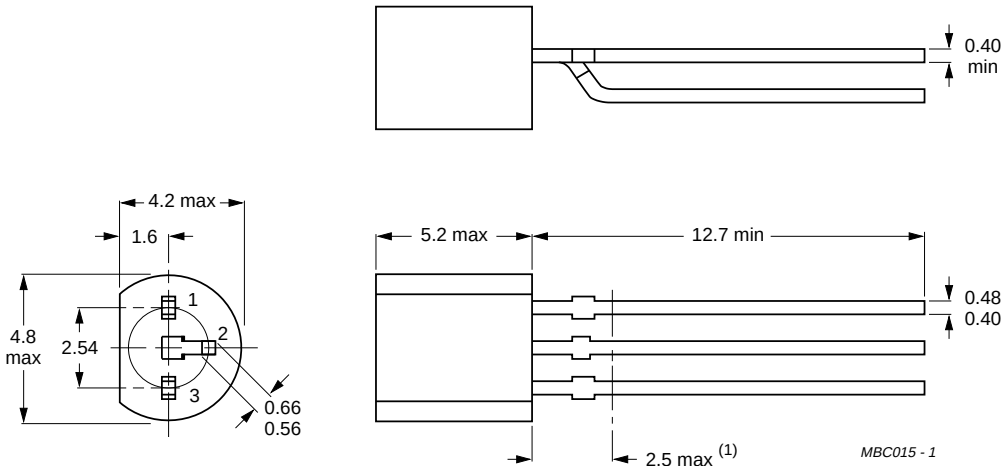
$T_{amb} = 25^\circ\text{C}.$

Fig.12 Thermal resistance from junction to ambient as a function of pulse time; typical values.

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vertical D-MOS transistor

BSS110

PACKAGE OUTLINE



Dimensions in mm.  
(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.13 TO-92 variant.

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BSS110

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**DEFINITIONS**

| <b>Data Sheet Status</b>                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                       |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification                                                                                                                                                                                                                                                                                                                                                                                                                                   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification                                                                                                                                                                                                                                                                                                                                                                                                                                 | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification                                                                                                                                                                                                                                                                                                                                                                                                                                     | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                       |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |                                                                                       |
| <b>Application information</b>                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                       |
| Where application information is given, it is advisory and does not form part of the specification.                                                                                                                                                                                                                                                                                                                                                       |                                                                                       |

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