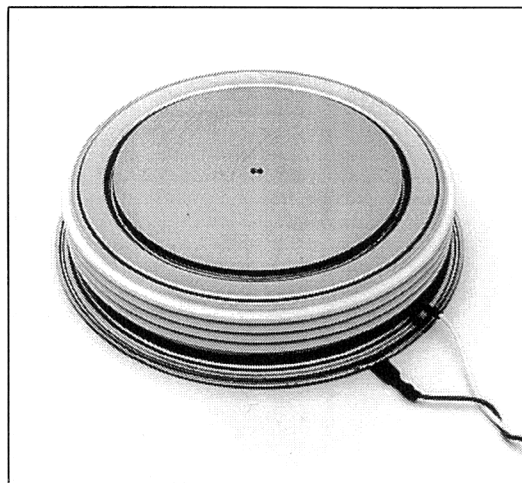
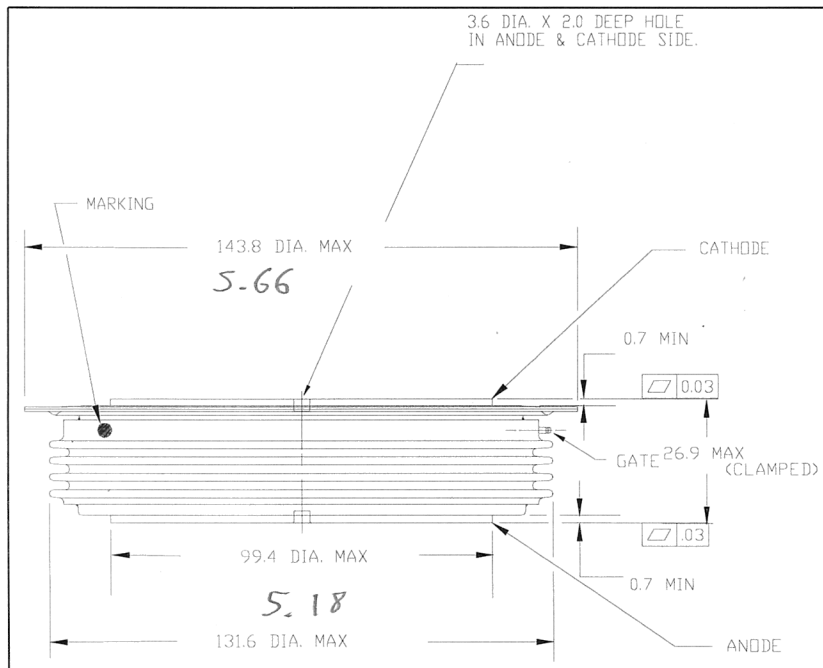




The TDS5 is a low voltage, high current, thin pack disc SCR employing a amplifying gate structure. This thin package provides greater cooling thus maximizing high current performance. The amplifying gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I^2t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls
- Plating Rectifiers

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
 EXAMPLE: TDS512503DH is a 1200V-24500A SCR with 200ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating I_{avg}	Current Code	Turn-Off T_q	Gate I_{GT}	Leads
TDS5	1400	14	5000	50	0	3	
	1200	12					
	1000	10			500us	200ma	12"
	800	08			(typ.)	(max)	



Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	1400	Volts
Average On-State Current, $T_C=70^{\circ}C$	$I_{T(Avg.)}$	5000	A
RMS On-State Current, $T_C=70^{\circ}C$	$I_{T(RMS)}$	7854	A
Average On-State Current, $T_C=53^{\circ}C$	$I_{T(Avg.)}$	6000	A
RMS On-State Current, $T_C=53^{\circ}C$	$I_{T(RMS)}$	9425	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	90,000	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	84,852	A
Fuse Coordination I^2t , 60Hz	I^2t	3.38E+07	A ² s
Fuse Coordination I^2t , 50Hz	I^2t	3.60E+07	A ² s
Critical Rate-of-Rise of On-State Current	di/dt	100	A/us
Repetitive			
Critical Rate-of-Rise of On-State Current	di/dt	300	A/us
Non-Repetitive			
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_j	-40 to+125	$^{\circ}C$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^{\circ}C$
Approximate Weight		6.5	lb
		2.95	Kg
Mounting Force		16,000-20,000	lbs
		71.2 - 89.0	KNewtons

Information presented is based upon manufacturers testing and projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

Electrical Characteristics, Tj=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	I_{DRM}	Tj=125°C, V_{DRM} =Rated			200	ma
Repetitive Peak Reverse Leakage Current	I_{RRM}	Tj=125°C, V_{RRM} =Rated			200	ma
Peak On-State Voltage	V_{TM}	Tj=125°C, I_{TM} =4000A			1.00	V
V_{TM} Model, Low Level	V_0	Tj=125°C			0.782	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	15% $I_{TM} - \pi \cdot I_{TM}$			4.97E-05	Ω
V_{TM} Model, High Level	V_0	Tj=125°C			1.011	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	$\pi \cdot I_{TM} - I_{TSM}$			3.59E-05	Ω
V_{TM} Model, 4-Term	A	Tj=125°C			0.800	
$V_{TM} = A + B \cdot \ln(I_{TM}) +$	B	15% $I_{TM} - I_{TSM}$			-0.024	
$C \cdot (I_{TM}) + D \cdot (I_{TM})^{1/2}$	C				2.40E-05	
	D				4.80E-03	
Turn-On Delay Time	t_d	$V_D = 0.5 \cdot V_{DRM}$ Gate Drive: 40V - 20 Ω		3		us
Turn-Off Time	t_q	Tj=125°C $dv/dt = 20V/us$ to 67% V_{DRM}			500	us
$dv/dt_{(Crit)}$	dv/dt	Tj=125°C Exp. Waveform $V_D = 67\%$ Rated	800			V/us
Gate Trigger Current	I_{GT}	Tj=25°C $V_D = 12V$	30	150	200	ma
Gate Trigger Voltage	V_{GT}		0.8	2.0	4.0	V
Peak Reverse Gate Voltage	V_{GRM}				5	V

Thermal Characteristics

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Thermal Resistance						
Junction to Case	$R\theta_{jc}$	Double side cooled		0.007	0.007	°C/Watt
Case to Sink	$R\theta_{cs}$	Double side cooled		0.001	0.0015	°C/Watt

 Thermal Impedance Model $Z\theta_{jc}$ Double side cooled

$$Z\theta_{jc}(t) = \sum(A(N) \cdot (1 - \exp(-t/\tau(N))))$$

where:

N = 1 2 3 4

 $A(N) = 1.43E-04 \quad 9.08E-04 \quad 2.37E-03 \quad 3.50E-03$
 $\tau(N) = 2.62E-03 \quad 2.31E-02 \quad 3.05E-01 \quad 3.60E+00$