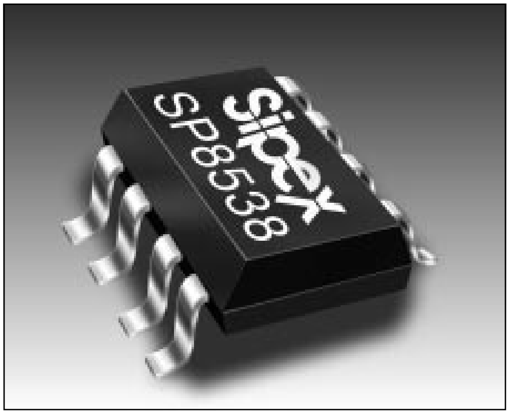
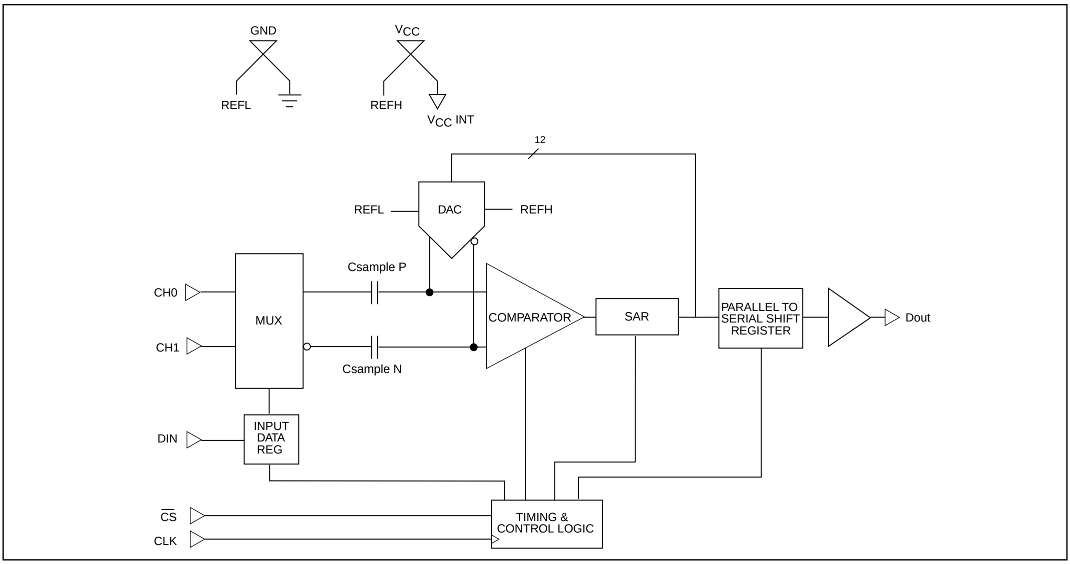
Micropower Sampling 12-Bit A/D Converter

- Low Cost
- 12-Bit Serial Sampling ADC
- 8-Pin NSOIC Plastic Package
- Low Power including Automatic Shutdown: 250µA
- Programmable Input Configuration: Full differential or 2 channel single-ended
- Single Suppply 3.0V to 5.5V operation
- Half Duplex Digital Serial Interface
- Sample Rate: 40µS



DESCRIPTION…

The **SP8538** is a very low power 12-Bit data acquisition chip. The **SP8538** typically draws 250µA of supply current when sampling at 25 kHz. Supply current drops linearly as the sample rate is reduced. The ADC automatically powers down when not performing conversions, drawing only leakage current. The **SP8538** is available in 8-Pin NSOIC packages, specified over Commercial, Industrial and Extended temperature ranges. The **SP8538** is best suited for Battery-Operated Systems, Portable Data Acquisition Instrumentation, Battery Monitoring, and Remote Sensing applications. The serial port allows efficient data transfer to a wide range of microprocessors and microcontrollers over 3 or 4 wires.



SP8538 Block Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

(TA=+25˚C unless otherwise noted) ....
VCC to GND 7.0V
Vin to GND .... -0.3 to VCC +0.3V
Digital input to GND .... -0.3 to VCC +0.3V
Digital output to GND .... -0.3 to VCC +0.3V
Operating Temperature Range
  Commercial (J, K Version) .... 0˚C to 70˚C
  Industrial (A, B Version) .... -40˚C to +85˚C
Lead Temperature (Solder 10Sec) .... +300˚C
Storage Temperature .... -65˚C to +150˚C
Power Dissipation to 70˚C 500mW

CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

Unless otherwise noted the following specifications apply for VCC=5V or 3.3V with limits applicable for Tmin to Tmax. Typical applies for Ta=25˚C.

	VCC=5.0V			VCC=3.3V				
PARAMETERS	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
DC ACCURACY		12			12		Bits	
Resolution								
Integral Linearity								
J,A			±2.0			±2.0	LSB	
K,B			±1.0			±1.0	LSB	
Differential Linearity Error								
J,A			±2.0			±2.0	LSB	No Missing Codes
K,B			±1.0			±1.0	LSB	No Missing Codes
Gain Error								
J,A			±10			±10	FSR	Externally Trimmable to Zero
K,B			±8			±8	FSR	Externally Trimmable to Zero
Offset Error								
J,A			±5			±5	FSR	Externally Trimmable to Zero
K,B			±3			±3	FSR	Externally Trimmable to Zero
ANALOG INPUT								
Input Impedance								
On Channel		20			20		pF	
		100					MΩ	
Off Channel		3			3		pF	
		100					MΩ	
Input Bias Current		1			1		nA	
MULTIPLEXER								
Crosstalk			-90			-90	dB	Off to On Channel
Feedthrough			-90			-90	dB	Off to On Channel
CONVERSION SPEED								
Sample Time		1.5			1.5		clock cycles	See Timing Diagrams
Conversion Time		12			12		clock cycles	See Timing Diagrams
Complete Cycle			25			7.35	kHz	See Timing Diagrams
Clock Period	2.25			2.9			µs	See Timing Diagrams
Clock High Time	1.0			1.4			µs	See Timing Diagrams
Clock Low Time	1.0			1.4			µs	See Timing Diagrams

SPECIFICATIONS (cont.)

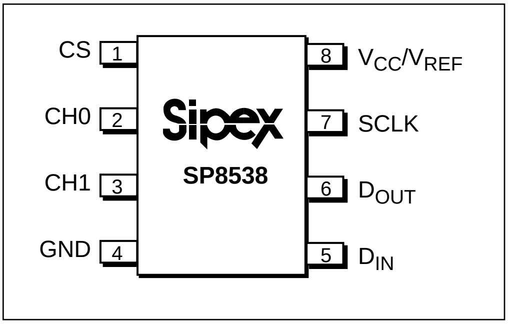
Unless otherwise noted the following specifications apply for VCC=5V or 3.3V with limits applicable for Tmin to Tmax. Typical applies for Ta=25˚C.

PARAMETERS	VCC=5.0V MIN.	VCC=5.0V TYP.	VCC=5.0V MAX.	VCC=3.3V MIN.	VCC=3.3V TYP.	VCC=3.3V MAX.	UNITS	CONDITIONS
SAMPLE & HOLD								
Acquisition Time			3.38			4.35	µs	.01% Accuracy
Common Mode Rejection			-70			-70	dB	Full Differential Mode f_{CM} = 12.5 kHz
DIGITAL INPUTS								
Input Low Voltage, VIL			0.8			0.8	Volts	V_{DD}=5V ±5%
Input High Voltage, VIH	2.0			2.0			Volts	V_{DD}=5V ±5%
Input Current IIN		±1.0			±1.0		µA	
Input Capacitance		3.0			3.0		pF	
DIGITAL OUTPUTS								
Data Format								
Data Coding								See Timing Diagram
VOH	4.0			2.0			Volts	V_{DD}=5V ±5%, IOH=-0.4mA
VOL			0.4			0.4	Volts	V_{DD}=5V ±5%, IOH=+1.6mA
AC ACCURACY								
Spurious free Dynamic Range (SFDR)		-86	-80		-86	-80	dB	For all FFT's (Full Differential Mode) If V_{CC} = 5V fsample = 25kHz
Total Harmonic Distortion (THD)		-86	-80		-86	-80	dB	fin = 12kHz
Signal to Noise & Distortion (SINAD)	70	73		70	73		dB	If V_{CC} = 3.3V fsample = 20kHz fin = 9.5kHz
Signal to Noise (SNR)	71	73.5		71	73.5		dB	
SAMPLING DYNAMICS								
Acquisition Time to 0.01%		2	3.38		2	4.35	µs	
-3dB Small Signal BW		5			4		MHz	
Aperture Delay		20			30		nS	
Aperture Jitter		150			150		ps	
Common-Mode Rejection	-70	-76		-70	-76		dB	f_{CM} = 12.5 kHz
POWER SUPPLIES							Volts	
VDD	+3.0	+5.0	+5.5	+3.0	+3.3	+5.5		
Supply Current Operation Mode		250			150		µA	($\overline{CS}$=0)
Shutdown Mode		2			2		µA	($\overline{CS}$=1)
Power Dissipation								
Operating Mode		1.25			0.5		mW	
Shutdown Mode		10			10		µW	
TEMPERATURE RANGE								
Commercial	0˚ to +70˚C			0˚ to +70˚C			˚C	
Industrial	-40˚ to +85˚C			-40˚ to +85˚C			˚C	
Storage	-65˚ to +150˚C			-65˚ to +150˚C			˚C	

SPECIFICATIONS (cont.)
Recommended Operating Conditions

SYMBOL	PARAMETERS	VCC=5.0V MIN.	VCC=5.0V TYP.	VCC=5.0V MAX.	VCC=3.3V MIN.	VCC=3.3V TYP.	VCC=3.3V MAX.	UNITS
V_{CC}	Supply Voltage	+3.0	+5.0	+5.5	+3.0	+3.3	+5.5	Volts
f_{CLK}	Clock Frequency			444			125	kHz
t_{CVC}	Total Cycle Time	40			140			µS
t_{hDI}	Hold Time D_{IN} After CLK^	50	10		80	10		nS
t_{suCS}	Setup Time CSv Before CLK^	100			100			nS
t_{suDI}	Setup Time, D_{IN} Stable Before CLK^	100			100			nS
t_{WHCLK}	CLK High Time	1			1.4			µS
T_{WHCLK}	CLK Low Time	1			1.4			µS
T_{WHCS}	$\overline{CS}$ High Time between Data Transfers Cycles	100			100			nS

PIN DESCRIPTION



PIN ASSIGNMENTS

Pin 1- $\overline{CS}$ - Chip Select.

Pin 2- CH0 - Channel 0

Pin 3- CH2 - Channel 1

Pin 4- GND - Ground

Pin 5- D_{IN} - Data In

Pin 6 - D_{OUT} - Data Out

Pin 7- CLK - Serial Clock

Pin 8- V_{CC} - V_{CC}/V_{REF}

DESCRIPTION

The **SP8538** is a 12 bit sampling ADC with a programmable two channel multiplexer and serial data interface. The ADC samples and converts 12 bits of data in 40 µS with a 5V supply voltage applied. The **SP8538** will also operate at a 3.0V supply at 50µS throughput. The device automatically shuts down to a ±3 µA (MAX) level as soon as the chip is deselected. ($\overline{CS}$'=1) Serial data output is available in an MSB first or LSB first format.

FEATURES

Two program bits, which are shifted into the device prior to conversion, determine the input configuration. In the single ended MUX configuration the input signal will be applied to either channel 1 or channel 2 and will be ground referenced. The maximum full scale range is VCC. In the full differential mode, the signal will be applied between channel 1 and channel 2. The signals applied at each input may both be dynamic. This is in contrast with pseudo differential devices which must have input low held at a constant level during conversion. The converter will provide significant common mode rejection when used in this manner. Both inputs must remain between ground and VCC for proper conversion.

The device uses a capacitive DAC architecture which provides the sampling behavior. This results in full Nyquist performance at the fastest throughput rate (25 KHz) the device is capable of.

The power supply voltage is variable from 3.0V to 5.5V which provides supply flexibility. At the 5.0V supply level, conversion plus sampling time is 40uS and supply current is 250µA (1.25 mW). With a 3.3V supply the conversion plus sampling time is 50(µS and current is reduced to 150 µA (0.5 mW MAX).

The device features automatic shutdown and will shutdown to a ±3 µA power level as $\overline{CS}$ is brought high (de-selected). Power is also proportional to throughput rate, as determined by the users clock rate and varies from 250 µA at 40µS to 6.25 µA at 1.6 mS.

Examples:

Throughput rate	Power
40 µS	250 µA
80 µS	125 µA
160 µS	62.5 µA
1.6 mS	6.25 µA

MUX ADDRESSING

Mux Addressing		Channel #		GND	Comments
SGL/DIFF	ODD/SIGN	0	1		
0	0	+	–		Different Mux Mode
0	1	–	+		
1	0	+		–	Single Ended
1	1		+	–	

The device can be configured such that it delivers serial data MSB first requiring 17 clock periods for a full conversion. Alternately, the device can be programmed to deliver 12 bits of data MSB first, followed by the same 12 bits of data LSB first. This sequence will require 28 clock periods to complete. Please refer to the timing diagram.

Circuit Operation

The device will ignore any leading zeros applied to the DIN pin even if chip select' is low. After chip select' ($\overline{CS}$') is brought low and the START bit is clocked in to the converter, the conversion sequence is initiated. Three additional bits are clocked in immediately following the START bit: SGL/DIFF, ODD/SIGN & MSBF. The second and third bits clocked in determine the MUX configuration (see MUX addressing table). The fourth bit determines the data output format (MSB first or LSB first). Please refer to the timing diagram.

The SGL/DIFF bit when zero sets the input MUX for full differential mode and when one, sets the input MUX for single ended mode. The ODD/SIGN bit when zero sets channel zero as the positive input (ground referred for single ended operation and referred to channel one in differential mode). With the ODD/SIGN bit one, channel one will be the positive input (ground referred for single ended operation and referred to channel zero in differential mode).

With MSBF set to one the output data stream will be MSB through LSB, with MSBF set to zero the output data stream will be MSB through LSB followed by the same data in LSB through MSB format.

The **SP8538** is a SAR converter with full differential multiplexed front end, capacitive DAC, precision comparator, Successive Approximations Register, control logic and data output register. After the input is sampled and held the conversion process begins. The DAC MSB is set and its output is compared with the signal input, if the DAC output is greater that than the input, the comparator outputs a one which is latched into the SAR and simultaneously made available at the ADC serial output pin. Each bit is tested in a similar manner until the SAR contains a code which represents the signal input to within ±1/2 LSB. During this process the SAR content has been shifted out of the ADC serially. If the MSB first format was chosen, the data will appear at the DOUT pin MSB through LSB in 17 clock periods. If the LSB first format was chosen then during conversion the data will appear at the DOUT pin just as before (MSB through LSB) but the LSB will be followed by D1, D2 through the MSB. This sequence will require 28 clock periods. Note that the Chip Select' pin must be toggled high between conversions. The DOUT pin will be in a high impedance state whenever Chip Select' is high. After Chip Select' has been toggled and brought low again, the converter is ready to accept another START bit and begin a new conversion.

Full Differential Sampling

The **SP8538** can be configured for single-ended sampling (i.e. CH0-ground or CH1-ground) or full differential sampling (CH0-CH1 or CH1-CH0). In the full differential sampling configuration, both inputs are sampled and held simultaneously. Because of the balanced differential sampling, dynamic common mode noise riding along the input signal is cancelled above and beyond DC noise. This is a significant improvement over psuedo-differential sampling schemes, where the low side of the input must remain constant during the conversion, and therefore only DC noise (i.e. signal offset) is cancelled. If AC common mode noise is left to be converted along with the differental component, the output signal will be degraded.

Full differential sampling allows flexibility in converting the input signal. If the signal low-side is already tied to a ground elsewhere in the system, it can be hardwired to the low side channel (i.e. CH0 or CH1) which acts as a signal ground sense, breaking a potential ground loop. It is also possible to drive the inputs balanced differential, as long as both inputs are within the power rails. In this configuration, both the high and low signals have the same impedance looking back to ground, and therefore pick up the same noise along the physical path from signal source (i.e. sensor, transducer, battery) to converter. This noise becomes common mode, and is cancelled out by the differential sampling of the **SP8538**.

Layout Considerations

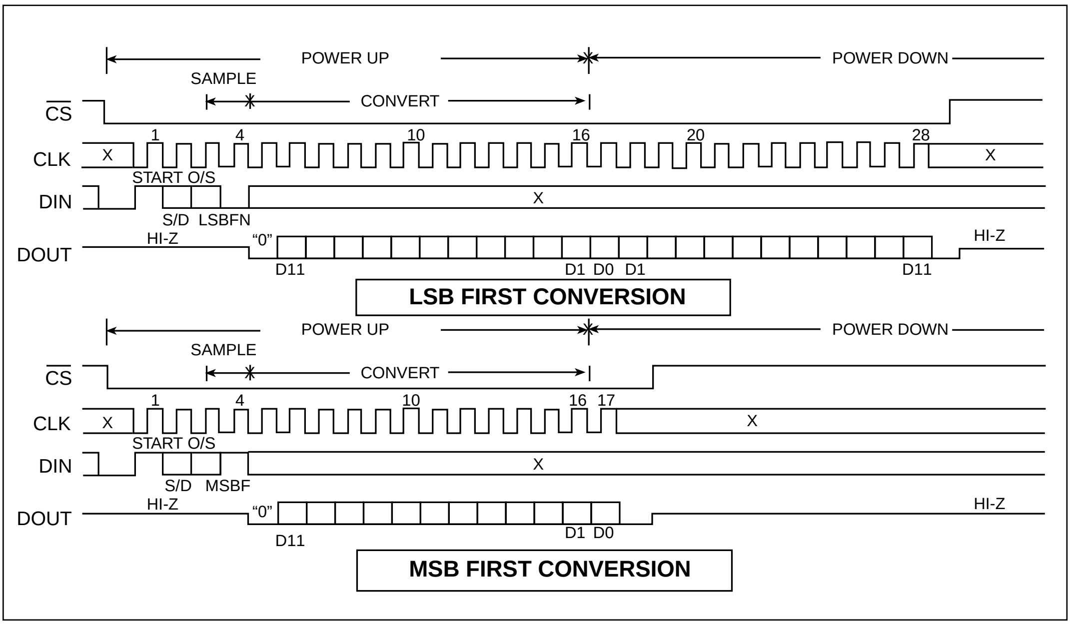
To preserve the high resolution and linearity of the **SP8538** attention must be given to circuit board layout, ground impedance and bypassing.

A circuit board layout which includes separate analog and digital ground planes will prevent the coupling of noise into sensitive converter circuits and will help to preserve the dynamic performance of the device. The analog input signal should be referenced to the ground pin of the converter. This prevents any voltage drops that occur in the power supply's common return from appearing in series with the input signal.

If separate analog and digital ground planes are not possible, care should be used to prevent coupling between analog and digital signals. If analog and digital lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated by a circuit board trace which is connected to common.

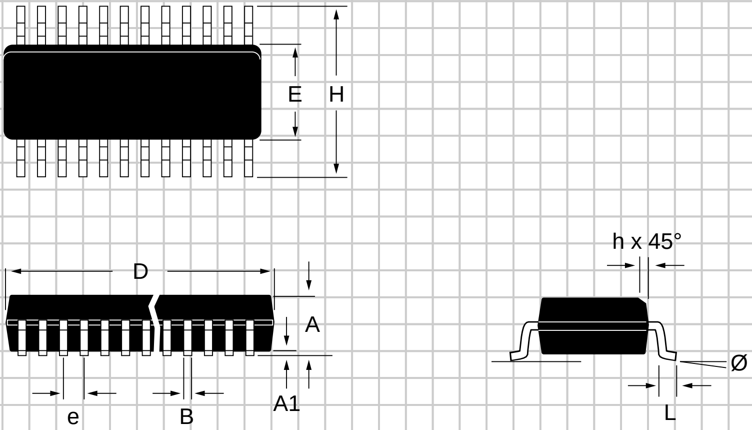
The **SP8538** VCC pin is also the reference pin for the device. This means that noise on the VCC pin will be proportionally represented as noise in the converters output data. A noise signal of 1.22mV (at a 5V supply) will produce 1 LSB of error in the output data. The VCC pin should be bypassed to the ground pin with a parallel combination of a 6.8μF tantalum and a 0.1μF ceramic capacitor. To maintain maximum system accuracy, the supply connected to the VCC pin should be well isolated from digital supplies and wide load variations. A separate conductor from the supply regulator to the A/D converter will limit the effects of digital switching elsewhere in the system. Power supply noise can degrade the converters performance. Especially corrupting are noise and spikes from a switching power supply.

To avoid introducing distortion when driving the A/D converter input, the input signal source should be able to charge the **SP8538's** equivalent 20 pF of input capacitance from zero volts to the signal level in 1.5 clock periods.



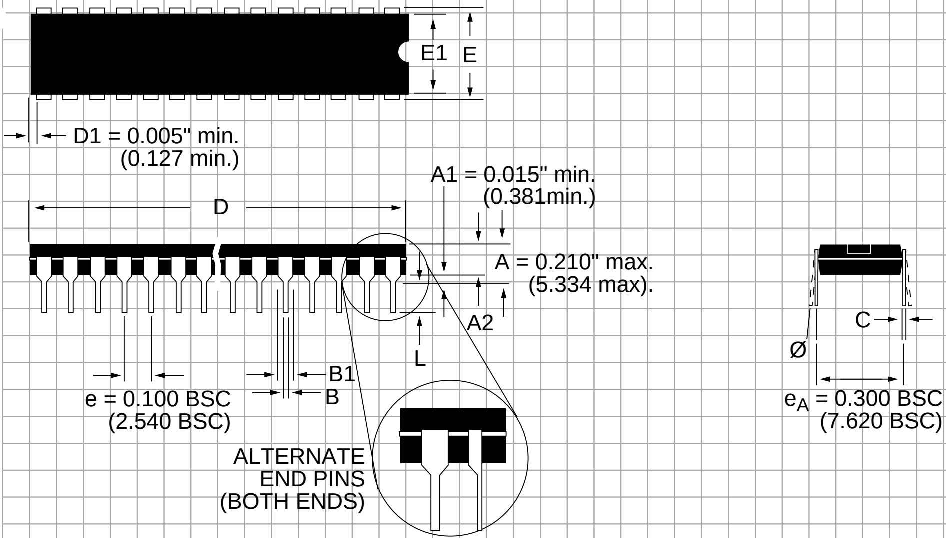
SP8538 Timing Diagram

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN			
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)			
A1	0.004/0.010 (0.102/0.249	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)			
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)			
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)			
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)			
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)			
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)			
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)			
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)			
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)			

PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN	18–PIN	20–PIN	22–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

ORDERING INFORMATION

Model	Linearity (LSB)	Temperature Range	Package
SP8538BN	±1.0	–40˚C to +85˚C	8-pin, 0.3" Plastic DIP
SP8538KN	±1.0	–0˚C to +70˚C	8-pin, 0.3" Plastic DIP
SP8538BS	±1.0	–40˚C to +85˚C	8-pin, 0.15" Plastic SOIC
SP8538KS	±1.0	–0˚C to +70˚C	8-pin, 0.15" Plastic SOIC
SP8538AN	±2.0	–40˚C to +85˚C	8-pin, 0.3" Plastic DIP
SP8538JN	±2.0	–0˚C to +70˚C	8-pin, 0.3" Plastic DIP
SP8538AS	±2.0	–40˚C to +85˚C	8-pin, 0.15" Plastic SOIC
SP8538JS	±2.0	–0˚C to +70˚C	8-pin, 0.15" Plastic SOIC

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