Understanding MOSFET Data

The following outline explains how to read and use Supertex MOSFET data sheets. The approach is simple and care has been taken to avoid getting lost in a maze of technical jargon.

The VN0104/VN0106/VN0109 data sheet was chosen as an example because this is one of the most popular devices and has the largest choice of packages. The product nomenclature shown applies only to Supertex proprietary products.

Device Structure

V: Vertical DMOS (discretes & quads)

D: Vertical Depletion-Mode DMOS discretes

T: Low threshold vertical DMOS discretes

A: Lateral DMOS arrays

L: Lateral DMOS discretes

Type of Channel

- N-Channel, or
- P-Channel

Design

Supertex Family number

Drain-to-Source Breakdown Voltage divided by 10.

04:	40 V
06:	60 V
09:	90V

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speed are desired.

This section outlines main features of the product

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

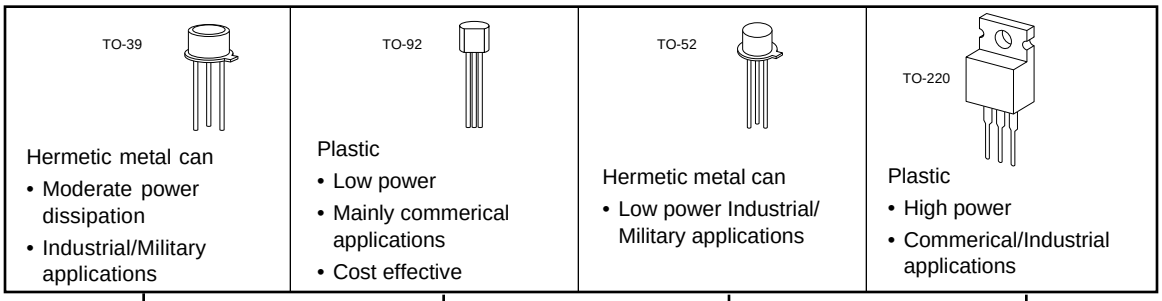
BV_{DSS}/ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package						
			TO-39	TO-92	TO-52	TO-220	Quad P-DIP	Quad C-DIP	DICE
40V	3Ω	2.0A	VN0104N2	VN0104N3	VN0104N9	VN0104N5	VN0104N6	VN0104N7	VN0104ND
60V	3Ω	2.0A	VN0106N2	VN0106N3	VN0106N9	VN0106N5	VN0106N6	VN0106N7	VN0106ND
90V	3Ω	2.0A	VN0109N2	VN0109N3	VN0109N9	VN0109N5	—	—	VN0109ND

Drain to source breakdown voltage & drain to gate breakdown voltage

Maximum resistance from drain to source when device is fully turned on

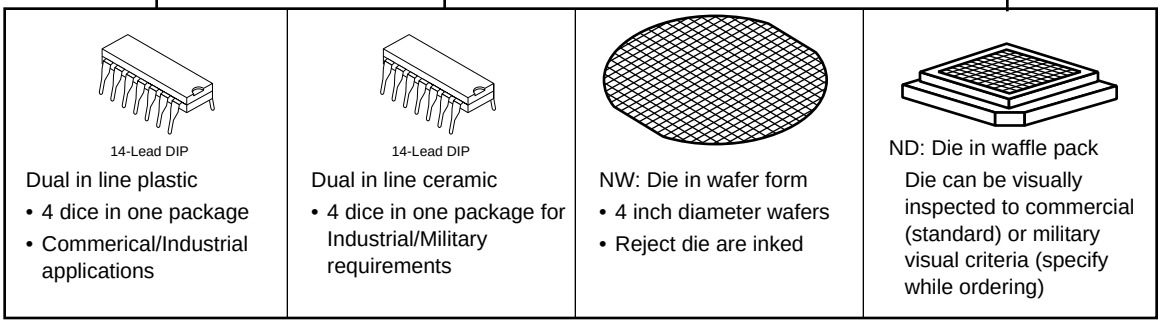
Minimum drain current when device is fully turned on

Package Options



Ordering Information

BV_{DSS}/ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package						
			TO-39	TO-92	TO-52	TO-220	Quad P-DIP	Quad C-DIP	DICE
40V	3Ω	2.0A	VN0104N2	VN0104N3	VN0104N9	VN0104N5	VN0104N6	VN0104N7	VN0104ND
60V	3Ω	2.0A	VN0106N2	VN0106N3	VN0106N9	VN0106N5	VN0106N6	VN0106N7	VN0106ND
90V	3Ω	2.0A	VN0109N2	VN0109N3	VN0109N9	VN0109N5	—	—	VN0109ND



Absolute Maximum Ratings

Extreme conditions a device can be subjected to electrically and thermally. Stress in excess of these ratings will usually cause permanent damage.

Ratings given in product summary.

Drain-to Source Voltage	BV_{DSS}
Drain-to-Gate	BV_{DGS}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature	300°C

V_{GS}

- Most Supertex FETs are rated for ±20V
- ± voltage handling capability allows quick turn off by reversing bias.
- External protection should be used when there is a possibility of exceeding this rating. Stress exceeding ±20V will result in gate insulation degradation and eventual failure.

Maximum allowable temperature at leads while soldering, 1.6mm away from case for 10 seconds.

- All Supertex devices can be stored and operated satisfactorily within these junction temperature (T_J) limits.
- Appropriate derating factors from curves and change in parameters due to reduced/ elevated temperatures have to be considered when temperature is not 25°C.
- Operation at T_J below maximum limit can enhance operating life.

Thermal Characteristics

Device characteristics affecting limits of heat produced and removed from device. Die size, $R_{DS(ON)}$ and packaging type are the main factors determining these thermal limitations.

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	0.8A	2.5A	3.5W	125	35	0.8A	2.5A
TO-92	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-52	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-220	1.5A	2.5A	15.0W	70	8	1.5A	2.5A
Plastic DIP Ceramic DIP	See DMOS Arrays & Special Functions section						

I_D (continuous)

Maximum continuous current carrying capability of device.

- Depends mainly on:
  - A. $R_{DS(ON)}$ - on state resistance
  - B. P_D - maximum power dissipation for package
  - C. Die size
  - D. Maximum junction temperature

I_D (pulsed)

Maximum non-continuous pulse current carrying capability for a 300 µS 2% duty cycle pulsed.

- Depends mainly on :
  - A. $R_{DS(ON)}$
  - B. P_D max
  - C. Diameter of bonding wire
  - D. Die size
  - E. Maximum junction temperature

Power Dissipation

- Maximum power package can dissipate when case temperature is 25°C.
- When case temperature is higher than 25°C, use P_D vs. T_C curve to determine dissipation permissible.

θ_{ja}

Thermal resistance from junction to air.

- Depends mainly on package and die size

θ_{jc}

Thermal resistance from junction to case.

- Depends mainly on package and die size
- To determine T_J use equation $T_J = P_D \times \theta_{jc} + T_A$

I_{DR}

Continuous current handling capability of drain to source diode.

- Factors affecting value same as I_D (continuous)

I_{DRM}

300 µS, 2% duty cycle pulsed. Current handling capability of drain source diode.

- Factors affecting this parameter same as I_D (pulsed)

Electrical Characteristics

The following DC parameters are 100% tested with 300µS, 2% duty cycle pulsed at 25°C, BV_{DSS}, $V_{GS(TH)}$, I_{DSS}, $I_{D(ON)}$ & $R_{DS(ON)}$.

- $\Delta V_{GS(TH)}$ and $\Delta R_{DS(ON)}$ are guaranteed by design ie., when device is functional for other DC parameters, these two parameters will not deviate from published values.
- Since a representative sample is adequate to assure consistency of specs, A.C. parameters are sample tested on a lot/batch basis.
- High temperature testing on sample basis when requested with hi-rel processing.
- Refer to section 3 "power MOS structures" for test circuits used for measurement.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0109	90			V	V_{GS} = 0, I_D = 1mA
		VN0106	60				
		VN0104	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	V_{GS} = 0, V_{DS} = Max Rating
					100		V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	V_{GS} = 5V, V_{DS} = 25V
			2.0	2.5			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.0	5	Ω	V_{GS} = 5V, I_D = 250mA
				2.5	3		V_{GS} = 10V, I_D = 1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1	%/°C	V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance		300	450		mmho	V_{DS} = 25V, I_D = 0.5A
C_{iss}	Input Capacitance			45	60	pF	
C_{oss}	Common Source Output Capacitance			20	25		
C_{rss}	Reverse Transfer Capacitance			5	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V I_D = 1A R_{GEN} = 25Ω
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			5	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V_{GS} = 0, I_{SD} = 1.0A
t_{rr}	Reverse Recovery Time			400		ns	V_{GS} = 0, I_{SD} = 1.0A

BV_{DSS}

- Please see product summary (part I)
- Positive temperature coefficient. See curve BV_{DSS} vs. T_J.

$V_{GS(TH)}$

- Voltage required from gate to source to turn on device to certain I_D current value given in "condition" column.
- I_D measurement condition is low for small die and higher for larger die.

$\Delta V_{GS(TH)}$

- Threshold voltage reduces when temperature increases and vice versa.
- Value at temperature other than 25 °C can be determined by $V_{GS(TH)}$ (normalized) vs. T_J curve.

I_{GSS}

- Since the gate is insulated from the rest of device by a silicon dioxide insulating layer, this parameter depends on thickness/integrity of layer and size of device.
- Measured at maximum permissible voltage from gate to source: ±20V.
- Values of this parameter are often tens/ hundreds of times less than published maximum value. Electrical screening is done at 100nA since test equipment functions slowly at lower values, which is not practical for mass production. Consult factory for screening lower values.

I_{DSS}

- This is the leakage current from drain to source when device is fully turned off.
- Measured by applying maximum permissible voltage between drain and source (BV_{DSS}) and gate shorted to source (V_{GS} = 0)
- Special electrical screening possible at lower values since max. published values are higher to achieve practical testing speeds.

$I_{D(ON)}$

- Defined as the minimum drain current when device is turned on.
- Supertex measures $I_{D(ON)}$ min. at two test conditions:

  V_{GS} = 5V and V_{GS} = 10V, to give the designer a look at both logic level turn on and full turn on

  Although Supertex specifies a typical value of $I_{D(ON)}$, the designer should use minimum value as the worst case.

$R_{DS(ON)}$

- Drain to source resistance measured when device is partially turned on at V_{GS} = 5V, and fully turned on at V_{GS} = 10V.
- Designers should use maximum values for worst case condition.
- When better turn on characteristics (ie., low $R_{DS(ON)}$) is required for logic level inputs, Supertex's low threshold TN & TP devices may be used.
- Typical value of $R_{DS(ON)}$ can be calculated at various V_{GS} conditions by using output characteristics or saturation characteristics family of curves (I_D vs. V_{DS}).
- $R_{DS(ON)}$ increases with higher drain currents. $R_{DS(ON)}$ curve has a slight slope for low values of I_D, but rises rapidly for high values.

$\Delta R_{DS(ON)}$

- Positive temperature coefficient.
- Enhances stability due to current sharing during parallel operation.

Switching Characteristics

- Extremely fast switching compared to bipolar transistors, due to absence of minority carrier storage time during turn off.
- Switching times depend almost totally on interelectrode capacitance, R_S (source impedance) and R_L (load impedance) as shown on test circuit.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0109	90			V	V_{GS} = 0, I_D = 1mA
		VN0105	60				
		VN0104	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	V_{GS} = 0, V_{DS} = Max Rating
					100		V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	V_{GS} = 5V, V_{DS} = 25V
			2.0	2.5			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.0	5	Ω	V_{GS} = 5V, I_D = 250mA
				2.5	3		V_{GS} = 10V, I_D = 1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1	%/°C	V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance		300	450		mmho	V_{DS} = 25V, I_D = 0.5A
C_{iss}	Input Capacitance			45	60	pF	
C_{oss}	Common Source Output Capacitance			20	25		
C_{rss}	Reverse Transfer Capacitance			5	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V I_D = 1A R_{GEN} = 25Ω
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V_{GS} = 0, I_{SD} = 1.0A
t_{rr}	Reverse Recovery Time			400		ns	V_{GS} = 0, I_{SD} = 1.0A

G_{FS}

- Represents gain of the device and can be compared to H_{FE} of a bipolar transistor.
- Value is the ratio of change in I_D for a change in V_{GS}

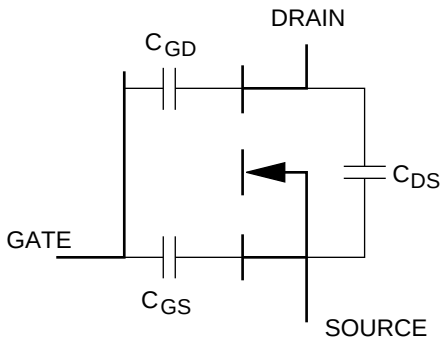
$$G_{FS} = \frac{\Delta I_D}{\Delta V_{GS}}$$

- Rises rapidly with increasing I_D, and then becomes constant in the saturation region. See G_{FS} vs. I_D curve.

C_{ISS}, C_{RSS}, C_{OSS}

- Please see section 3 in Databook "Power MOSFET Electrical Performance" for interelectrode capacitances and equivalent circuit.
- Supertex interdigitated structures have lowest C_{ISS} in the industry for comparable die sizes and exhibit excellent switching characteristics.
- Values of these capacitances are high at low voltages across them. Please see capacitance vs V_{DS} curves for details.
- Negligible effect of temperature on capacitances.
- The following equation may be used for calculating effective value of C_{ISS} with "Miller Effect."

$C_{ISS} = C_{GS} + (1+G_{FS} R_L) C_{GD}$



$C_{ISS} = C_{GD} + C_{GS}$

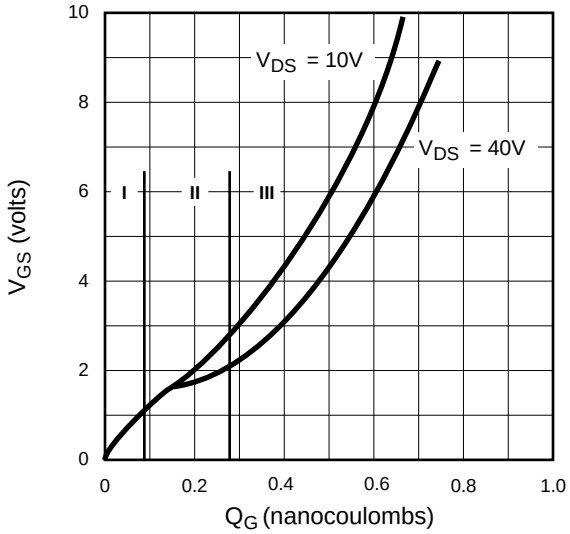
$C_{OSS} = C_{GD} + C_{DS}$

$C_{RSS} = C_{GD}$

$T_{d(ON)}$

During this period, the drive circuit charges C_{ISS} up to $V_{GS(TH)}$. Since no drain current flows prior to turn on, V_{DS} and consequently C_{ISS} remain constant. Region I on the V_{GS} vs. Q_G curve shows linear change in voltage with increasing Q_G.

Gate Drive Dynamic Characteristics



Switching Characteristics (continued)

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0109	90			V	V_{GS} = 0, I_D = 1mA
		VN0106	60				
		VN0104	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	V_{GS} = 0, V_{DS} = Max Rating
					100		V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	V_{GS} = 5V, V_{DS} = 25V
			2.0	2.5			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.0	5	Ω	V_{GS} = 5V, I_D = 250mA
				2.5	3		V_{GS} = 10V, I_D = 1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1	%/°C	V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance		300	450		mmho	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance			45	60	pF	
C_{OSS}	Common Source Output Capacitance			20	25		
C_{RSS}	Reverse Transfer Capacitance			5	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V I_D = 1A R_{GEN} = 25Ω
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V_{GS} = 0, I_{SD} = 1.0A
t_{rr}	Reverse Recovery Time			400		ns	V_{GS} = 0, I_{SD} = 1.0A

t_r

- When C_{ISS} is driven to a voltage exceeding $V_{GS(TH)}$, conduction from drain source begins. G_{FS} increases causing increase in C_{ISS} due to "Miller Effect" Charge requirements to Region II increase considerably. Gain stabilizes in Region III and "Miller Effect" is nullified, resulting in a linear change in V_{GS} for increase in Q_G.

$t_{d(OFF)}$

- The sequence of events now begins to reverse. C_{ISS} discharges through R_{GEN}. The rise of V_{DS} is initially slowed by increase of output capacitance.

t_f

- V_{DS} rises as the load resistor charges the output capacitance.

V_{SD}

- This is the forward voltage drop of the parasitic diode between drain and source.
- Diode my be used as a commutator in H bridge configurations or in a synchronous rectifier mode. Excessive fly back voltages may be clamped by this diode in a totem pole configuration.

t_{RR}

- The reverse recovery time is the time needed for the carrier gradient, formed during forward biasing, to be depleted when the biasing is reversed.
- An external fast recovery diode may be connected from drain to source to improve recovery time.