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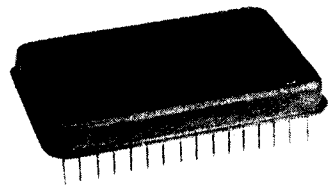


ADC803

High-Speed ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 12-BIT RESOLUTION
- ±0.012% LINEARITY ERROR MAXIMUM (C GRADE)
- NO MISSING CODES −55°C to +125°C (S GRADE)
- HIGH SINAD RATIO: 72dB
- LOW HARMONIC DISTORTION: −73dB
- CONVERSION TIME: 500ns, 8 bits
  670ns, 10 bits
  1.5μs, 12 bits

DESCRIPTION

The ADC803 is a high speed successive approximation analog-to-digital converter utilizing state-of-the-art IC and laser-trimmed thin film components.

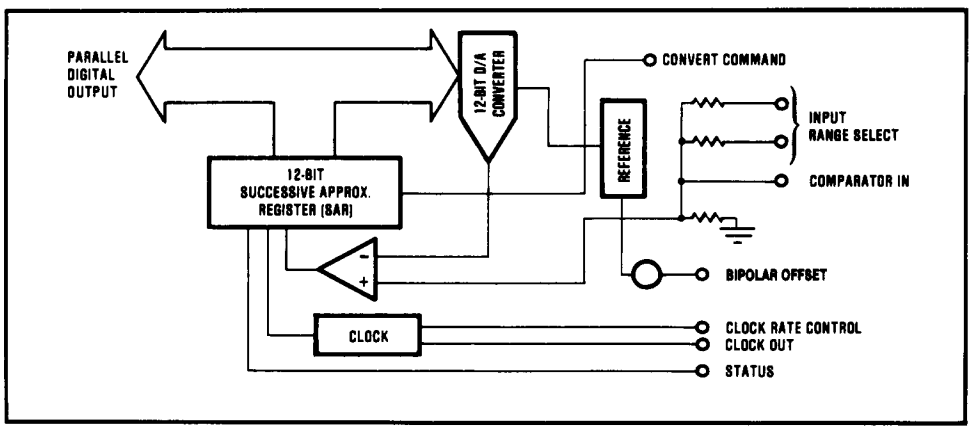
It is complete with internal reference, clock, and comparator and is packaged in a 32-pin metal package. Conversion time is set at the factory to 1.5μs.

With user-adjusted conversion time set at 1μs, ±1LSB accuracy can be achieved. The gain and offset errors may be externally trimmed to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of 0V to -10V, ±5V, and ±10V.

Output codes available are complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



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PDS-493D

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, 1.5μs conversion time, and after 6-minute warm-up unless otherwise noted.

MODEL	ADC803CM			ADC803BM			ADC803SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			12			12	Bits
INPUTS										
ANALOG										
Voltage Ranges: Bipolar		±5, ±10			*			*		V
Unipolar		0 to −10			*			*		V
Impedance: −10V to 0V, ±5V		1.4			*			*		kΩ
±10V		2.4			*			*		kΩ
DIGITAL										
Convert Command		Negative pulse 50ns wide (min) trailing edge (0 to 1) initiates conversion.								
Logic Loading		4			*			*		TTL Loads
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error[1]		±0.04	±0.1		±0.08	±0.2		+0.04	+0.1	%
Offset Error[1]: Unipolar		±0.05	±0.2		±0.07	±0.3		*	*	% of FSR[2]
Bipolar		±0.02	±0.1		*	±0.2		*	*	% of FSR
Linearity Error:										
1.5μs Conversion Time		±0.009	±0.012			±0.020		±0.012	±0.015	% of FSR
1.0μs Conversion Time		±0.015	±0.020		±0.020					% of FSR
Differential Linearity Error:										
1.5μs Conversion Time		±0.012	±0.015			±0.020		*	*	% of FSR
1.0μs Conversion Time			±0.024		±0.024			*		% of FSR
Inherent Quantization Error		1/2			*			*		LSB
POWER SUPPLY SENSITIVITY										
Gain and Offset: +15VDC		±0.0038			*			*		% of FSR/%V_{CC}
−15VDC		±0.0005			*			*		% of FSR/%V_{CC}
+5VDC		±0.001			*			*		% of FSR/%V_{DD}
Conversion Time: +15VDC		±0.7			*			*		%/%V_{CC}
−15VDC		None			*			*		%/%V_{CC}
+5VDC		±0.8			*			*		%/%V_{DD}
CONVERSION TIME										
Factory Set	1.3		1.5	*		*	*		*	μs
Range of Adjustments	0.8		2.2	*		*	*		*	μs
DRIFT										
Gain		±10	±30		±15	*		*	*	ppm of FSR/°C
Offset: Unipolar		±2	±7		±3	*		*	*	ppm of FSR/°C
Bipolar		±3	±10		±5	*		*	*	ppm of FSR/°C
Linearity Error										
−25°C to +85°C:										
1.5μs Conversion Time		±0.012	±0.018			±0.024			*	% of FSR
1.0μs Conversion Time		±0.015			±0.020				*	% of FSR
−55°C to +125°C:										
1.7μs Conversion Time, max.[4]								±.015	±.024	% of FSR
Differential Linearity Error										
−25°C to +85°C:										
1.5μs Conversion Time		±0.012	±0.018			±0.024				% of FSR
1.0μs Conversion Time		±0.015			±0.024					% of FSR
−55°C to +125°C:										
1.7μs Conversion Time, max[4]								±.015	±.024	% of FSR
Conversion Time		±0.1			*			*		% of FSR
No Missing Code Temp. Range:										
1.5μs Conversion Time	−25		+85	*		*				°C
1.7μs Conversion Time, max[4]							−55		+125	°C

ADC803 dynamic performance characteristics are described in a report titled "Analogue-to-Digital Converter Performance Tests Using the Fast Fourier Transform" by R. A. Belcher, University College of Swansea, Wales, U.K. (available from Burr-Brown on letterhead request).

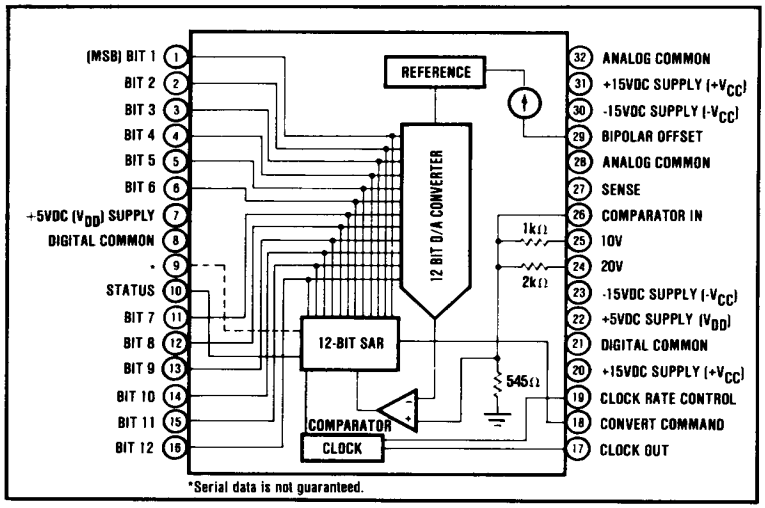
ELECTRICAL (CONT)

MODEL	ADC803CM			ADC803BM			ADC803SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT										
DIGITAL DATA										
Parallel										
Output Codes: Unipolar	Complementary Straight Binary				*			*		
Bipolar	Bipolar Offset Binary				*			*		
Output Drive	6			*			*			TTL Loads
Status	Logic "1" during Conversion				*			*		
Status Output Drive	6			*			*			TTL Loads
Internal Clock:										
Clock Output Drive	3			*			*			TTL Loads
Frequency (without external clock adjustment)		8			*			*		MHz
POWER SUPPLY REQUIREMENTS										
Power Consumption										
Rated Voltage: Analog ($\pm V_{CC}$)	±14.25	±15.0	±15.75	*	*	*	*	*	*	VDC
Digital (V_{DD})	+4.75	+5.0	+5.25	*	*	*	*	*	*	VDC
Supply Drain: +15V		+27	+32		*	*		*	*	mA
−15V		−38	−55		*	*		*	*	mA
+5V		+180	+210		*	*		*	*	mA
TEMPERATURE RANGE (AMBIENT)										
Specification	−25		+85	*		*	−55		+125	°C
Storage	−55		+125	*		*	*		*	°C

*Same specification as for ADC803CM.

NOTES: (1) Adjustable to zero. See Optional Gain and Offset Adjustment section. (2) FSR means Full Scale Range. For example, unit connected for ±10V has 20V FSR. (3) See Optional Clock Rate Control section. For faster conversion time at less resolution, see section on External Short Cycle. (4) Conversion time is factory-set at approximately 1.4μs at +25°C. As temperature increases, the conversion time increases. At +125°C the conversion time will be no more than 1.7μs. No Missing Codes is guaranteed over −55°C to +125°C provided the conversion time is allowed to increase with temperature.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

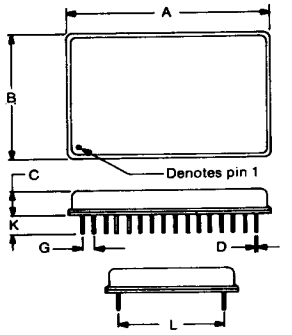
Analog Supply Voltage To Analog Common	±18V
Digital Supply Voltage To Digital Common	+7V
Digital Controls Inputs	+5.5V
Analog Inputs	±15V
Operating Temperature: Ambient	+125°C
Case	+135°C
Storage Temperature	+125°C

ORDERING INFORMATION

ADC803 X M Q

- Basic Model Number
- Performance Grade Code
  - B, C = −25°C to +85°C
  - S = 55°C to +125°C
- Package Code
  - M = Metal DIP
- Reliability Screening
  - Q Q-Screened

MECHANICAL



Pin numbers shown for reference only. Numbers may not be marked on package.

Pin 1 can be identified from bottom of unit by either a contrasting color of glass seal or a square corner. Case is tied to Digital Common.

NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane. Pin 8 connected to case.

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Kovar, Nickel plated
HERMETICITY: Gross Leak Test
MATING CONNECTOR: 2302MC Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

THEORY OF OPERATION

The accuracy of a successive approximation analog-to-digital converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry matching and tracking properties of the ladder and scaling networks, power supply rejection, reference errors and the dynamic errors of the DAC and comparator. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the transfer function (Figure 1) about the zero point and Offset drift shifts the transfer function left or right over the operating temperature range. Linearity error is not adjustable but it is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the best fit straight line transfer function of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB. The ADC803 is guaranteed to have no missing codes over the specified temperature range.

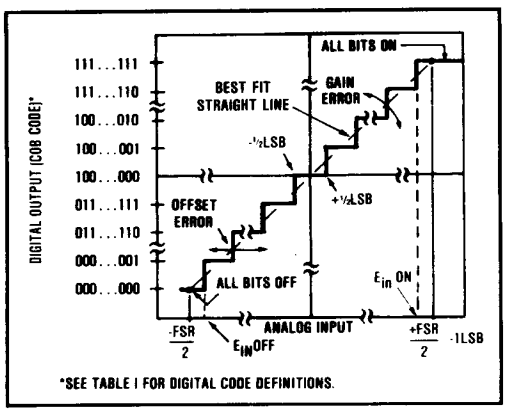


FIGURE 1. Input versus Output for an Ideal Bipolar A/D Converter.

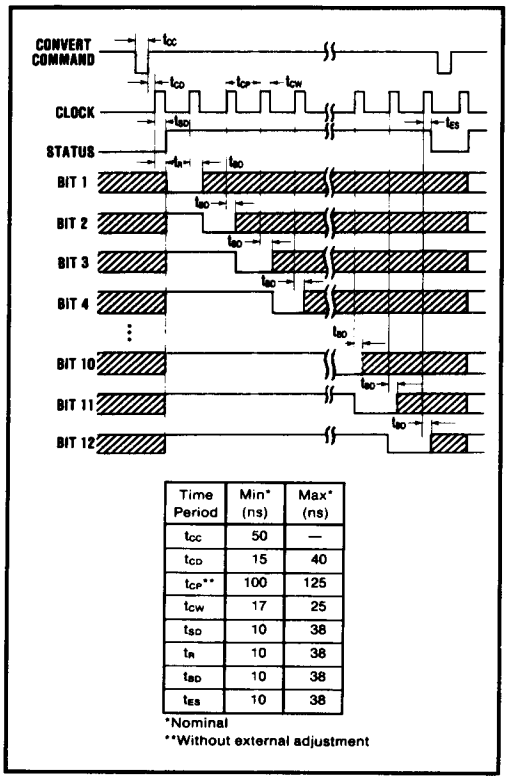
TIMING CONSIDERATIONS

The timing diagram (Figure 2) shows the relationship between the convert command, clock and outputs. The digital output word is positive true logic for bipolar operation and complementary logic for unipolar operation.

The following are some important notes on the ADC803 timing. The times given are typical unless otherwise noted. Nominal maximum and minimum times are also given in Figure 2.

1. When power is first applied, the status of the ADC803 will be undetermined. A CONVERT COMMAND must be applied to initialize the ADC803.
2. The CONVERT COMMAND must be low at least 50nsec prior to the "0" to "1" edge that starts a conversion.
3. The clock runs continuously when the initial CONVERT COMMAND goes high and whenever the CONVERT COMMAND is high thereafter. It does not run when CONVERT COMMAND is low. It may be beneficial to keep CONVERT COMMAND low except during conversions to limit the digital noise induced in the ground and power supply lines.
4. The clock starts 25ns after the "0" to "1" transition of the CONVERT COMMAND.
5. **Parallel Output Data:** The Successive Approximation Register (SAR) is reset 26ns after the leading edge of the first clock period in the conversion cycle. The MSB is set to logic "0" and all other bits are set to logic "1". The bits are determined in succession starting with the MSB, Bit 1, as shown in Figure 2. Each bit will be valid 26ns after its corresponding clock pulse.

   The falling edge of the STATUS signal should not be used to strobe parallel data out of the ADC803



Time Period	Min* (ns)	Max* (ns)
t_{CC}	50	—
t_{CD}	15	40
t_{CP}**	100	125
t_{CW}	17	25
t_{SD}	10	38
t_R	10	38
t_{BD}	10	38
t_{ES}	10	38

*Nominal
**Without external adjustment

FIGURE 2. ADC803 Timing Diagram.

directly. The table in Figure 2 indicates that the falling edge of STATUS may occur prior to bit 12 data becoming valid.

6. STATUS goes high 26ns after the leading edge of the first clock pulse and goes low 18ns after the leading edge of the last clock pulse.
7. Bit 12 will become valid at about the same time STATUS goes low and a new conversion can be initiated at anytime after the output data has been read.
8. The converter may be restarted during a conversion. When CONVERT COMMAND makes a "0" to "1" transition after the minimum set-up time, the SAR will be reset and a new conversion will start regardless of the state of the converter prior to the CONVERT COMMAND being received.

Figures 3, 4, and 5 are photographs of the actual pulse shapes and relationships.

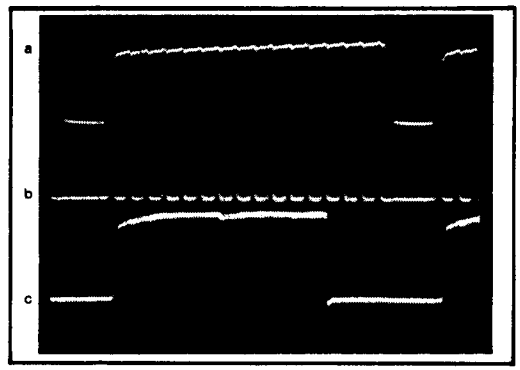


FIGURE 3. Photo of (a) Convert Command, (b) Clock, and (c) Status (200ns/div).

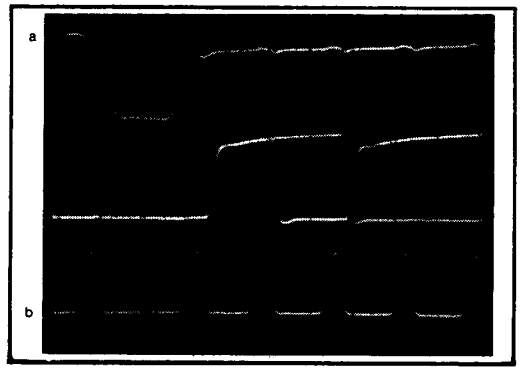


FIGURE 4. Photo of (a) Convert Command, (b) Clock (50ns/div).

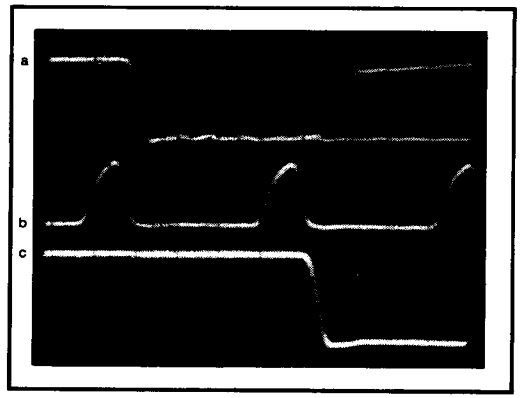


FIGURE 5. Photo of (a) Bit-12 Data (Parallel), (b) Clock, and (c) Status (20ns/div).

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC803 parallel output; they are complementary straight binary (Logic "0" true) for unipolar input signal ranges and bipolar offset binary (Logic "1" true) for bipolar input signal ranges. Binary two's complement may be obtained for bipolar input ranges by inverting the MSB. It should be noted that for unipolar input ranges -10 volts is full scale.

Table I shows the LSB, transition values, and code definitions for each possible analog signal range.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Analog Input Voltage Range	±10V	±5V	0 to -10V
Code Designation	BOB[1] or BTC[2]	BOB or BTC	CSB[3]
One Least Significant Bit (LSB)	4.88mV	2.44mV	2.44mV
Transition Values MSB LSB[4]			
000...000 ↔ 000...001	-10V + 1/2LSB	-5V + 1/2LSB	-10V + 3/2LSB
011...111 ↔ 100...000	-1/2LSB	-1/2LSB	-5V + 1/2LSB
111...110 ↔ 111...111	+10V - 3/2LSB	+5V - 3/2LSB	−1/2LSB

NOTES: 1. BOB = Bipolar Offset Binary.
2. BTC = Binary Two's Complement (obtained by inverting the most significant bit (pin 1)).
3. CSB = Complementary Straight Binary.
4. Voltages given are the nominal value for the transition from the next lower code.

Serial Data (NRZ)

ADC803 serial data operation is not guaranteed. To operate in serial output mode a pin-for-pin replacement ADC806 is recommended.

DISCUSSION OF SPECIFICATIONS

The ADC803 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are Linearity, Drift, Gain and Offset errors, and Conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.05% of FSR at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10, 11, and 12.

ACCURACY VERSUS CONVERSION TIME

In successive approximation A/D converters, the conversion time affects Linearity and Differential Linearity errors. Conversion time and its effect on Linearity and Differential Linearity errors for the ADC803 are shown in Figure 6.

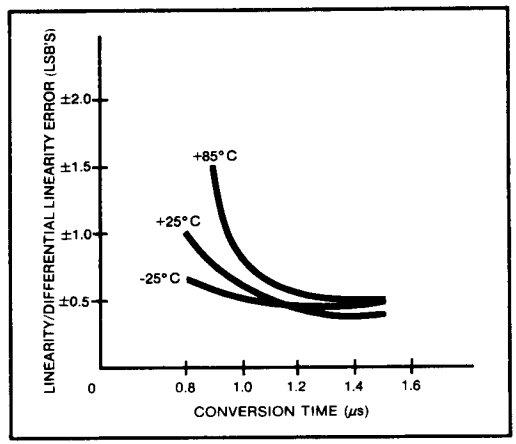


FIGURE 6. Linearity and Differential Linearity Error versus Conversion Time.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

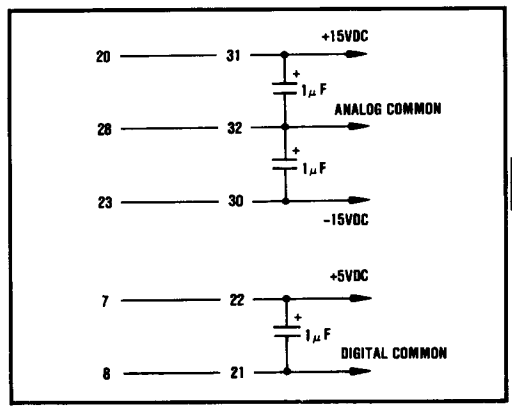


FIGURE 7. Recommended Power Supply Decoupling.

LINEARITY ERROR

Linearity error is not adjustable by the user. Linearity is the deviation of an actual bit transition from the best fit straight line value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity describes the step size between transition values. A Differential Linearity error of

±1/2LSB indicates that the size of any step may not vary from 1LSB by more than ±1/2LSB.

ENVIRONMENTAL SCREENING

Q screening is now available for all models of the ADC803 family. The Q-screened versions have the same specifications as the unscreened versions listed in the Specifications table.

Q Screening

Burr-Brown Q-screened models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those listed below. Burr-Brown's detailed procedures may vary slightly from those of MIL-STD-883.

SCREENING FLOW FOR ADC803Q

Screen	Method Burr-Brown or MIL-STD-883	Condition
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008	B (150°C, 24hr)
Temperature Cycling	1010	B (10cy, −55°C to +125°C)
Constant Acceleration	2001	(2000G, Y1 axis)
Burn-in ADC803BMQ, CMQ ADC803SMQ	1015	D (160 hrs, +85°C) (160 hrs, +125°C)
Electrical Test	Burr-Brown Test Specification	
Hermeticity Fine Leak	1014	A1 or A2 (Helium, 5×10^{-7}cc/s)
Gross Leak	1014	C
Final Electrical	Burr-Brown Test Specification	
External Visual	Burr-Brown QC5150	

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

The ADC803 is a high speed analog-to-digital converter which requires more layout precautions than general purpose products.

The ADC803 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together externally. The connection between the digital supply pins and the connection between the digital common pins must be as short as possible. The analog and digital commons are not connected together internally in the ADC803, but should be connected together externally to a ground plane.

Connecting all commons to a ground plane at the ADC803 is the best method to minimize noise and dissipate heat. Pin 8 (Digital Common) is internally connected to the case.

The ADC803 also has an analog common Sense input (pin 27) for the analog input. This sense pin must be connected to analog common as close to the input signal source as possible or connected to the ground plane. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. Special attention should be taken to ensure that the clock noise on the +5V supply line does not couple into the analog inputs.

The Comparator input (pin 26) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by analog common or ±15VDC supply patterns. The Clock Output (pin 17) is sensitive to stray capacitance; capacitance on this pin could alter the clock wave shape.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF tantalum capacitors as shown in Figure 8 to obtain noise-free operation. These capacitors should be located close to the ADC.

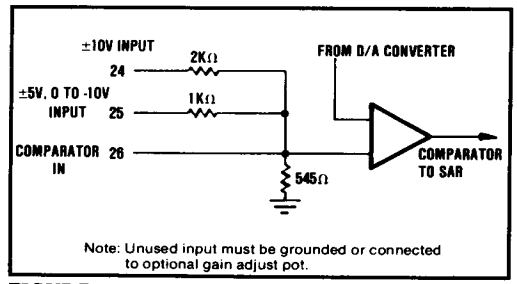


FIGURE 8. Input Scaling Circuit.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signals as shown in Table II. See Figure 8 for circuit details.

OUTPUT DRIVE

All ADC803 outputs except the clock will drive six TTL loads; the clock will drive three TTL loads. If long digital lines must be driven, external logic buffers are required particularly for the clock which is sensitive to capacitive loading.

TABLE II. ADC803 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 29 To	With Gain Adjust	Connect Pin 24 To	Connect Pin 25 To
±10V	BOB or BTC*	26	Yes	40Ω resistor in series with input signal	Gain Adjust Potentiometer
			No	Input Signal	Analog Common
±5V	BOB or BTC*	26	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal
0 to −10V	CSB	Analog Common	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal

*Obtained by inverting MSB (pin 1) externally.

INPUT IMPEDANCE

The source impedance to the ADC803 should be low, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC803.

If this impedance is not low, a buffer amplifier should be added between the input signal and the ADC803 input as shown in Figure 9.

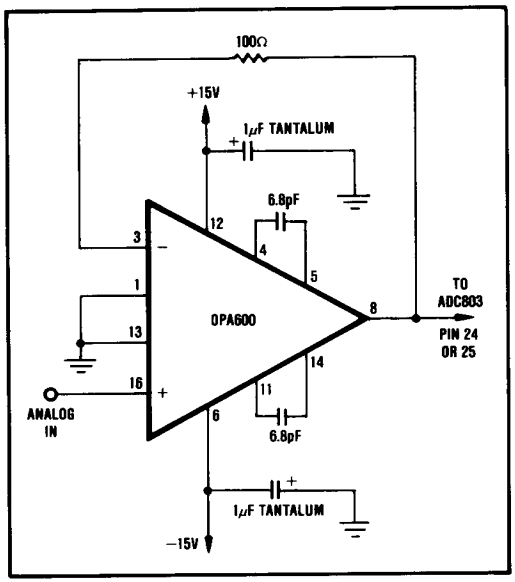


FIGURE 9. Source Impedance Buffering.

A common problem with successive approximation A/D converters is the transients in input current caused by the comparator input being switched back and forth. This requires a fast settling amplifier to drive the input.

The ADC803 comparator is connected in a differential mode (see Figure 8), greatly reducing the size of the input transients. The user, therefore, may use a fast settling wideband operational amplifier to drive the ADC803. The small signal settling time of the amplifier should be less than 100ns.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external trim potentiometers connected to the ADC as shown in Figures 10, 11, and 12. For proper gain adjust range a series resistor must be connected to the analog input pin as specified in Table II and shown in Figures 11 and 12. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. All resistors should be ±1% metal film or better. If the Offset adjust is not used, pin 26 should be left open except for bipolar operation when it is connected to pin 29. If the Gain adjust is not used, the unused input (pin 24 or 25) must be grounded to meet specified gain accuracy.

Adjustment Procedure

Refer to Table I for LSB voltages and transition values.

Unipolar offset - connect the offset potentiometer and resistors as shown in Figure 11, sweep the input through the end point transition voltage, from 111...110 to 111...111. Adjust the Offset potentiometer until the actual end point transition voltage occurs at -1/2LSB.

Bipolar offset - connect the offset potentiometer and resistors as shown in Figure 10. Sweep the input through zero and adjust the offset potentiometer until the transition from 0111 1111 1111 to 1000 0000 0000 occurs at −1/2LSB.

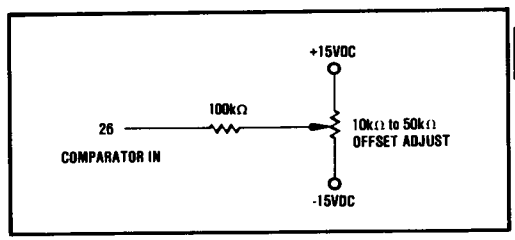


FIGURE 10. Optional Offset Adjust

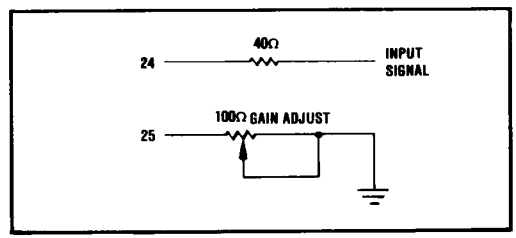


FIGURE 11. Optional Gain Adjust for ±10V Bipolar Operation.

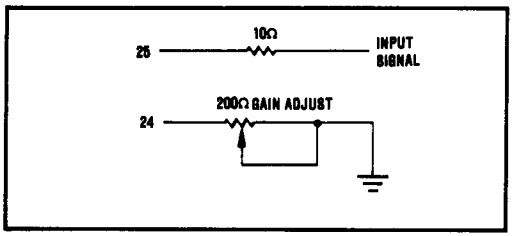


FIGURE 12. Optional Gain Adjust for ±5V Bipolar or 0 to -10V Unipolar Operation.

Gain - connect the Gain potentiometer as shown in Figure 11 or 12. Sweep the input through the end point transition voltage that should cause an output transition from 000...000 to 000...001. Adjust the Gain potentiometer until this transition occurs at the correct end point transition voltage as given in Table I.

OPTIONAL CLOCK RATE CONTROL

The clock is factory-set for a conversion time between 1.3μs and 1.5μs. By use of the optional Clock Rate Control as shown in Figure 13, the Conversion time can be adjusted down to 0.8μs for 12-bit resolution. If the optional Clock Rate Control is not used, pin 19 should be left open. Figure 14 shows Conversion Time versus Clock Rate Control voltage and Figure 6 shows Differential Linearity error versus Conversion time.

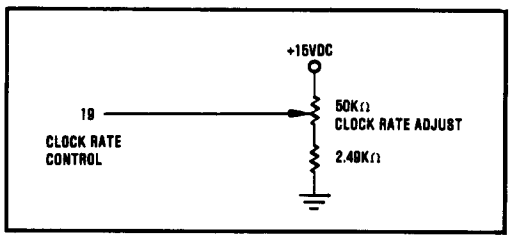


FIGURE 13. Optional Clock Rate Control.

POWER DISSIPATION

The ADC803 dissipates approximately 1.9W (typical) and the package has a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above +85°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 15 for θ_{CA} requirements above +85°C. Improved thermal contact with the PC card copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16-square-inch (minimum) area, this technique will allow operation to +100°C. Forced air plus heat sink is recommended for +125°C operation.

EXTERNAL SHORT CYCLE

If less than 12 bits of resolution is required, the cycle time of the ADC803 can be shortened with the addition of two external components as shown in Figure 16. This circuit will create a shortened status signal directly proportional

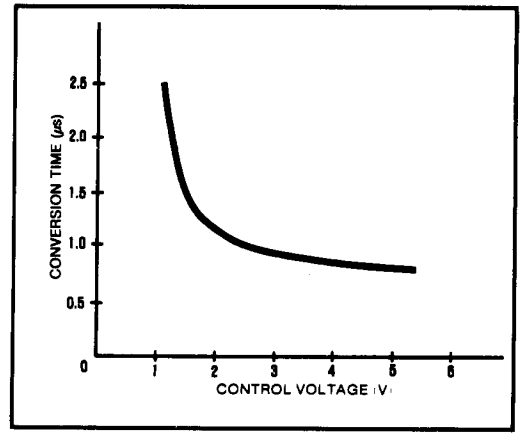


FIGURE 14. Conversion Time versus Clock Rate Control Voltage.

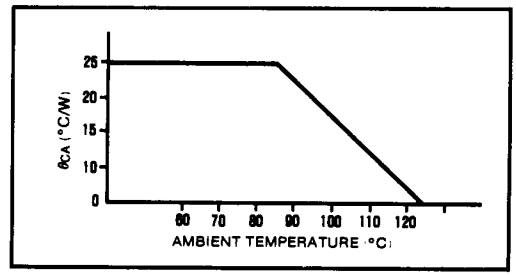


FIGURE 15. θ_{CA} Requirement Above +85°C.

to the reduction of resolution. For n bits of resolution, the n+1 bit is used to create the falling edge of the shortened status signal. It is possible to obtain the equivalent of a 10-bit converter with 670ns conversion time and an 8-bit converter with 500ns conversion time using this short cycle technique and the external clock rate control shown in Figure 13. To begin a new conversion, simply give the converter a new convert command pulse. The SAR will reset and a new conversion will begin.

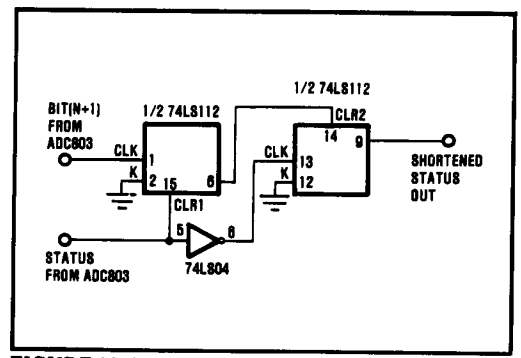


FIGURE 16. External Short Cycle Circuit.

TESTING OF THE ADC803

In order to validate the test results of the ADC803 obtained during final test, the customer must take extreme care in the design and layout of his test fixtures. Proper grounding, correct routing of analog and digital signals and power supply bypassing are crucial in achieving successful results.

ANALOG GROUND, DIGITAL GROUND, SENSE

Figure 17 shows a simplified model of the ADC depicting proper analog and digital grounding. Several analog and digital ground pins have been provided to allow for optimizing the internal layout of the ADC. As will be explained in more detail later, analog and digital grounds should be connected together only at one point by an extremely low resistive and inductive connection (a ground plane is ideal). A special analog ground called "sense" has been provided to eliminate the voltage drop that would otherwise be in the ground return of the R-2R ladder. Measuring the input signal with respect to the sense terminal makes the measurement independent of the impedance that is developed in the connection between the sense terminal and the analog ground, pin 28.

ANALOG-TO-DIGITAL CONVERTER TEST TECHNIQUE

A very effective way of determining the DC performance of an ADC is by using the "servo loop method." The block diagram of this technique is shown in Figure 18. This measurement system automatically locates the analog voltage that causes the digital output to alternate between the desired code and the adjacent code. The

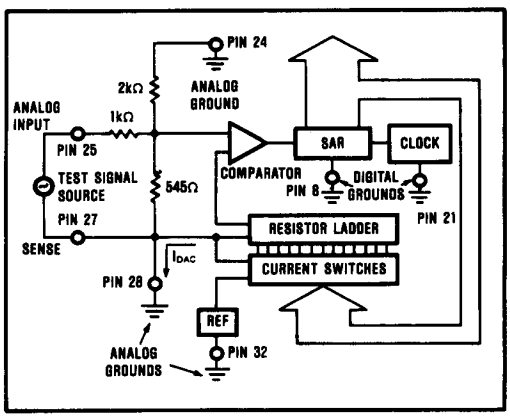


FIGURE 17. Simplified Model of ADC803 Depicting Proper Analog and Digital Ground.

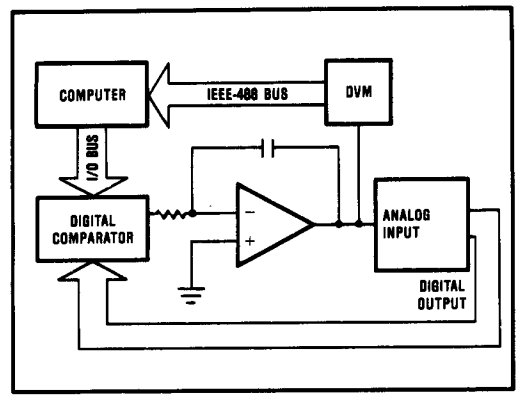


FIGURE 18. Servo Loop Analog-to-Digital Tester.

computer is programmed to place the desired code on the I/O bus which is one set of inputs to the digital comparator. The other set of inputs to this comparator is the digital output of the ADC. Depending upon the result of this comparison, the integrator is directed to change its output until an equilibrium state is achieved. Once in equilibrium, the DVM measures the analog input to the ADC and transmits the information to the computer via the IEEE-488 bus. The test program checks all the desired code combinations, verifying the performance of the ADC. Test time will range from 10 seconds to several minutes depending on the speed of the test program, settling time of the DVM, and number of codes to be checked.

GROUND LOOPS

Figure 19 illustrates the interaction that occurs between the analog and digital grounds when an ADC is connected into a test circuit. This interaction is created by ground loops. The circuit in Figure 19 shows how ground loops are created when the ADC tester combines digital and analog portions of the circuit together—in this case, the test signal generator (analog) and the digital circuitry that detects the ADC code which corresponds to the analog signal (digital). The ground loop exists when the digital ground connection between the ADC and the tester is in parallel with the analog grounds that connect the tester with the ADC. When the connection is made in this manner some of the digital current is diverted into the analog signal return, which creates a code-dependent error signal due to the resistance in the analog signal return. This error distorts the linearity measurement and induces hysterisis. The error can be substantially reduced if the analog and digital grounds are isolated from each other in the ADC tester.

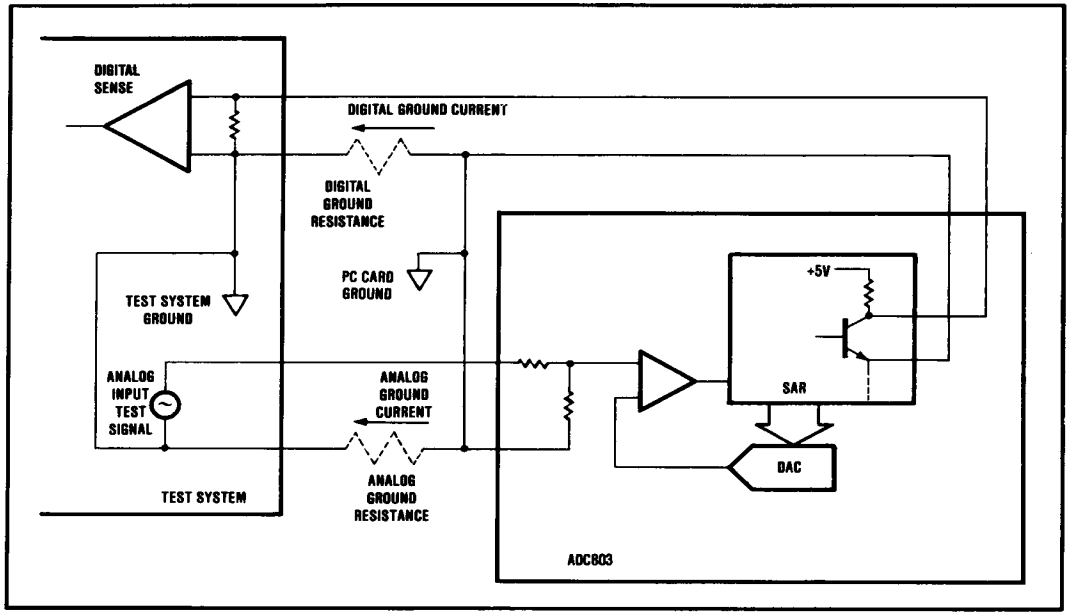


FIGURE 19. Ground Loop Interaction Between Analog and Digital Grounds When ADC Is Connected Into Test Circuit.

BEAT FREQUENCY TEST

A "beat frequency test" applied to an ADC803 with a companion sample/hold illustrates both an effective means of testing the high frequency performance of such a system and demonstrating that the ADC803 with its associated sample/hold is capable of digitizing high frequency signals cleanly. A sample/hold must be used when performing this test to hold the input of the ADC803 constant during the conversion time. Figure 20 is a block diagram of the beat frequency test setup.

The beat frequency test is useful for being able to rapidly determine whether there are any serious problems with the ADC. In this test the input frequency is set at slightly less than one-half the sampling rate. The slight difference is selected to allow the sample point to vary by 1LSB, or less, on successive samples. The data is clocked into a low frequency reconstruction DAC at one-half the sampling rate to enable viewing on an oscilloscope. Figure 21 is a photograph of the response to a full-scale input sine wave centered around the MSB and Figure 22 is a photograph of the response of a small signal sine wave centered around the MSB. For comparison, a photograph (Figure 23) is included which shows the response of the ADC803 to a 125Hz input signal which is the same as the beat frequency.

Figure 24 is the PC card layout that was used for the beat frequency test. This layout demonstrates some of the layout practices that must be followed when using a high speed ADC like the ADC803.

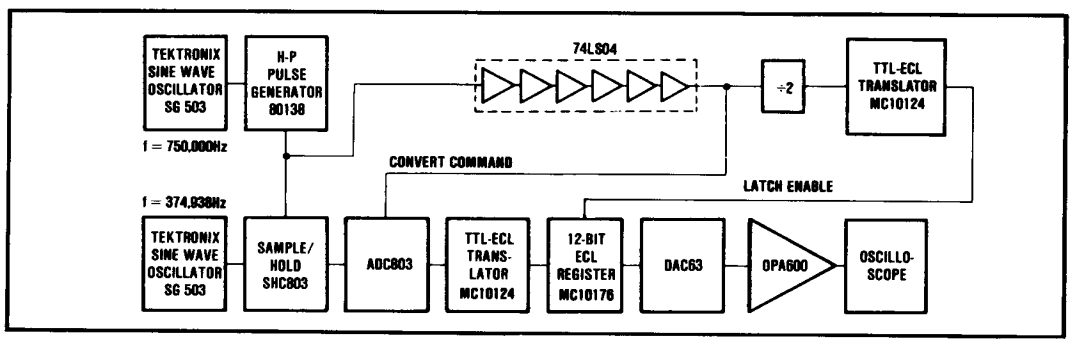


FIGURE 20. Block Diagram of Beat Frequency Test Circuit.

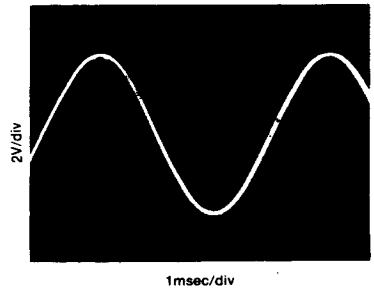


FIGURE 21. Beat Frequency Test Response of Full Scale Sine Wave Input.

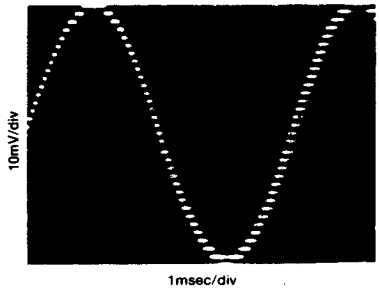


FIGURE 22. Beat Frequency Test Response of Small Signal Sine Wave Input.

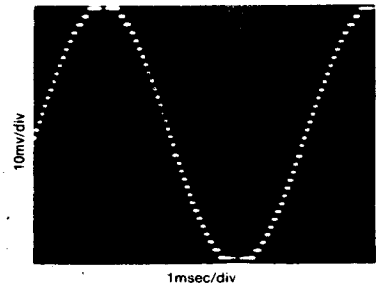


FIGURE 23. Response of Small Signal 125Hz Sine Wave Input.

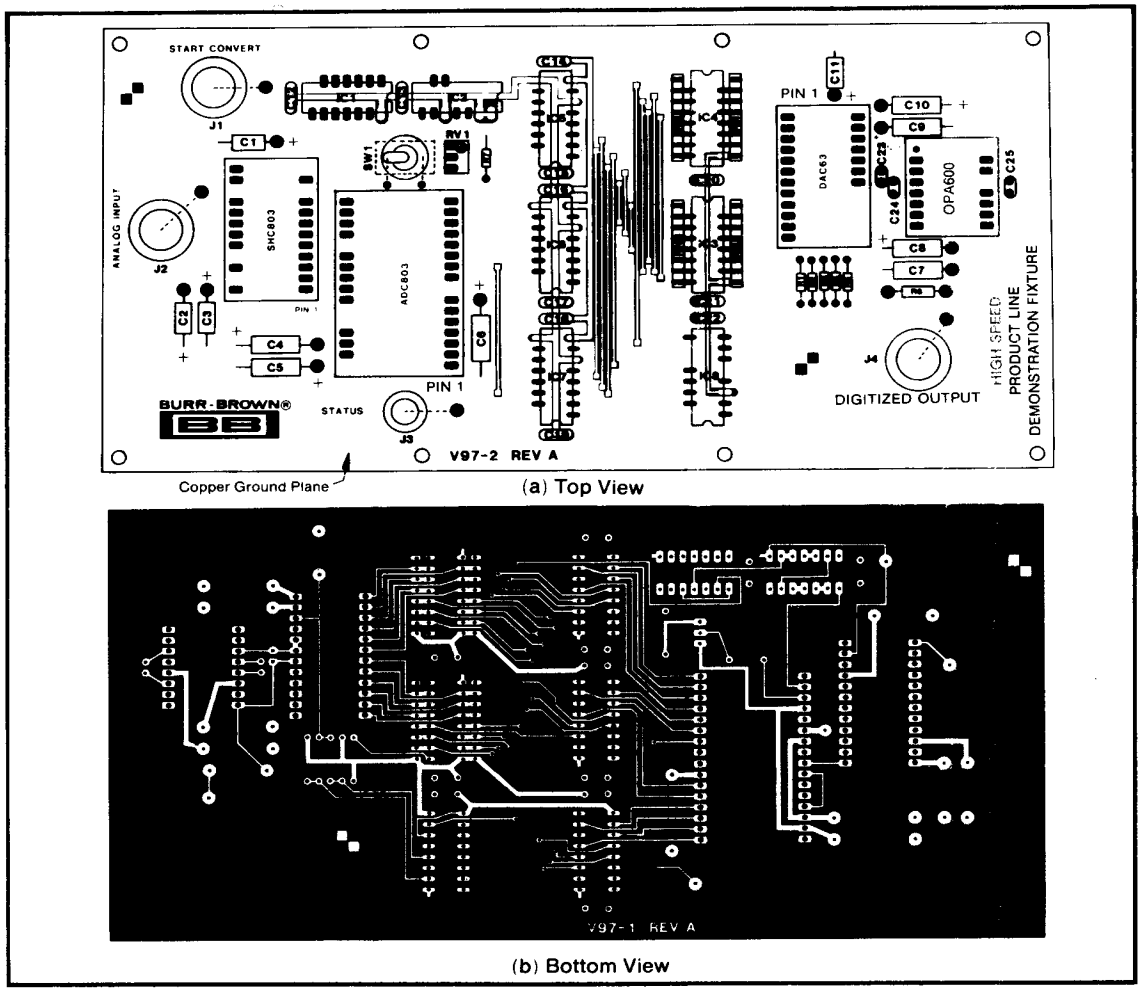


FIGURE 24. PC Board Layout for Beat Frequency Test Fixture.