ABT
Advanced BiCMOS Technology Characterization Information

SCBA008
July 1994

TEXAS INSTRUMENTS

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Introduction

The purpose of this document is to assist the designers of high-performance digital logic systems in using the advanced BiCMOS technology logic family, referred to as ABT.

Detailed electrical characteristics of these bus interface devices are provided and, if available, tables and graphs have been included that compare specific parameters of the ABT family with those of other logic families.

In addition, typical data is provided to give the hardware designer a better understanding of how the ABT devices operate under various conditions.

The major subject areas covered in the report are as follows:

- AC Performance
- Power Considerations
- Input Characteristics
- Output Characteristics
- Signal Integrity
- Advanced Packaging
- Characterization Information

The characterization information provided is typical data and is not intended to be used as minimum or maximum specifications, unless noted as such.

For more information on Texas Instruments ABT logic products, please contact your local TI field sales office or an authorized distributor, or call Texas Instruments at 1-800-336-5236.

AC Performance

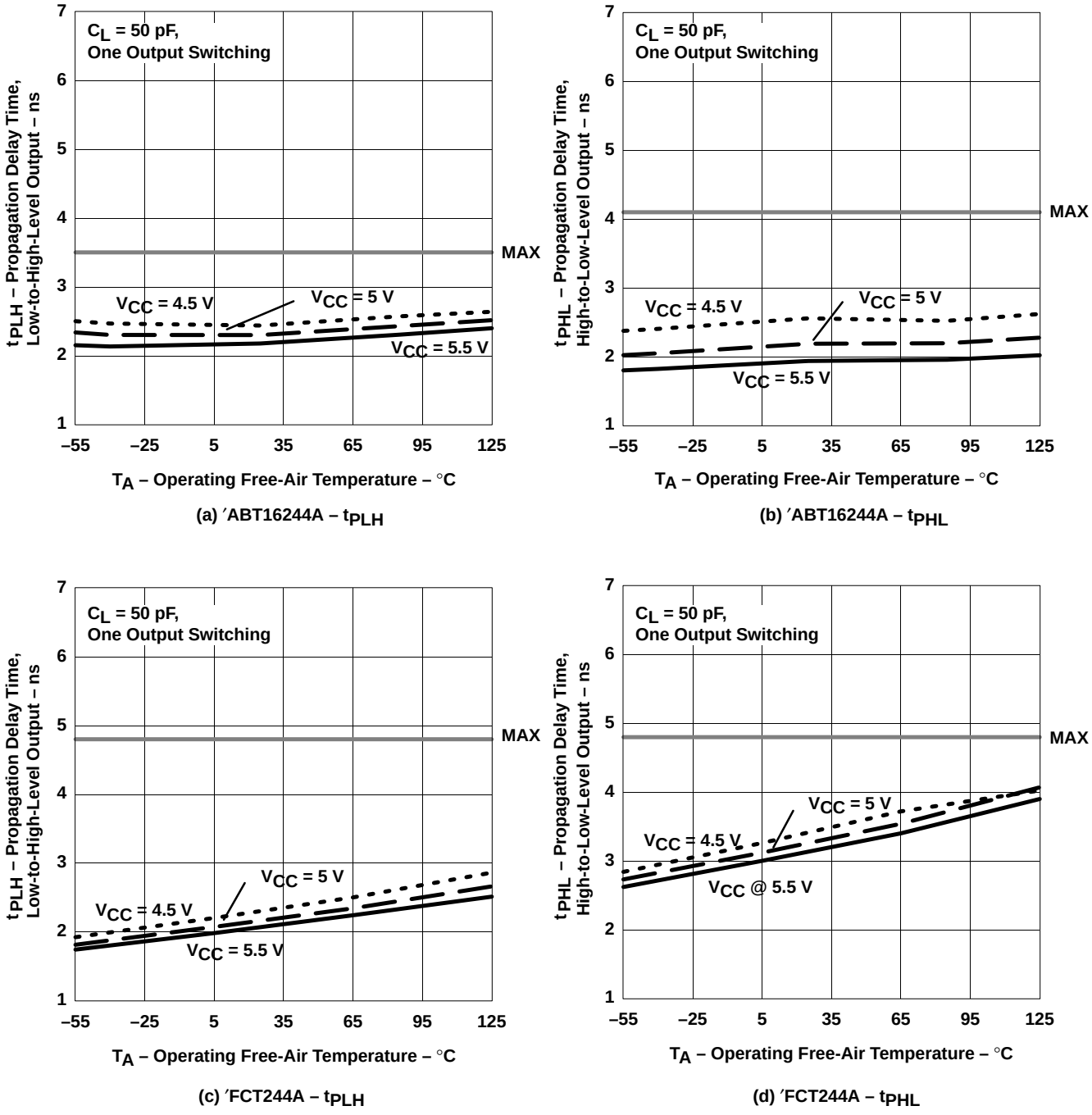
As microprocessor operating frequencies increase, the period of time allotted for operations, such as memory access or arithmetic functions, decreases. With this in mind, Texas Instruments has developed a new family of bus interface devices – ABT, utilizing advanced BiCMOS technology. The goal of the ABT family of devices is to give system designers one bus interface solution which provides high drive capability, good signal integrity, and propagation delays short enough to appear transparent with respect to overall system performance.

Advances in IC process technology including smaller minimum feature size, tighter metal pitch, and shallower junctions, combine to provide stronger drive strengths and smaller parasitic capacitances. As a result, internal propagation delays have become extremely short. With the advent of the 0.8-µm, EPIC-IIB™ BiCMOS process and new circuit innovations, the ABT family offers typical propagation delays as low as 2-3 ns as shown in Figure 1. Maximum specifications are as low as 3-5 ns depending on the device type.

Figure 2 shows the propagation delay versus change in both temperature and supply voltage for an ′ABT16244A, ′FCT244A, and a ′F244 device. The graphs highlight two important aspects of the new ABT logic family. First, ABT interface devices have extremely short propagation delay times. The figures clearly show the improvement in speed of an ABT device over that of a 74F and 74FCTA device. Second, the variance in speed with respect to both temperature and supply voltage is minimal for ABT. At low temperatures, the increase in CMOS performance compensates for the decrease in bipolar device strength. At high temperatures, the reverse occurs. This complementary performance of both CMOS and bipolar devices on a single chip results in a slope which is virtually flat across the entire temperature range of –55°C to 125°C.

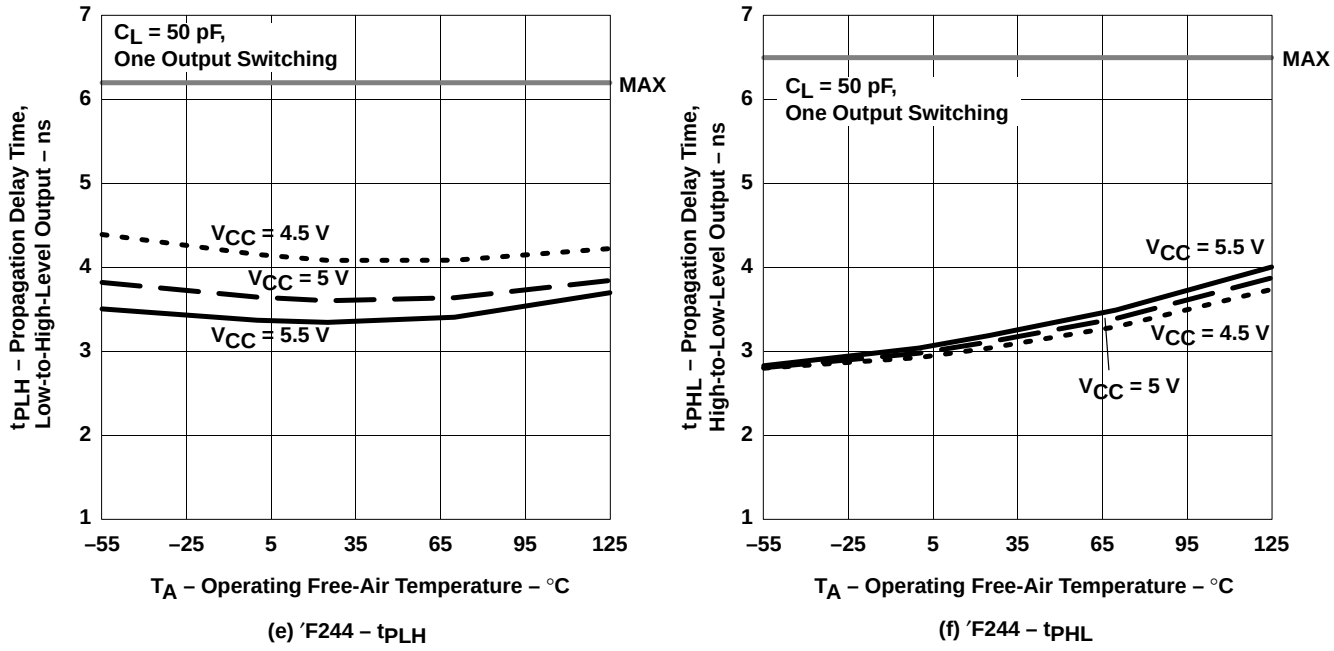
For most applications, the data sheet specifications may not provide all of the information a designer would like to see for a particular device. For instance, a designer might benefit from data such as propagation delay with multiple outputs switching or with various loads. This type of data is extremely difficult to test using automatic test equipment; therefore, it is provided in this document as family characteristics shown in Figure 2 and Figure 3.

In order to get a clear picture of where ABT stands in reference to other logic families, data is shown for a comparable (same function) 74F and 74FCTA device. It is clear that ABT is the designer’s best choice for bus-interface applications which require consistent speed performance over various conditions.



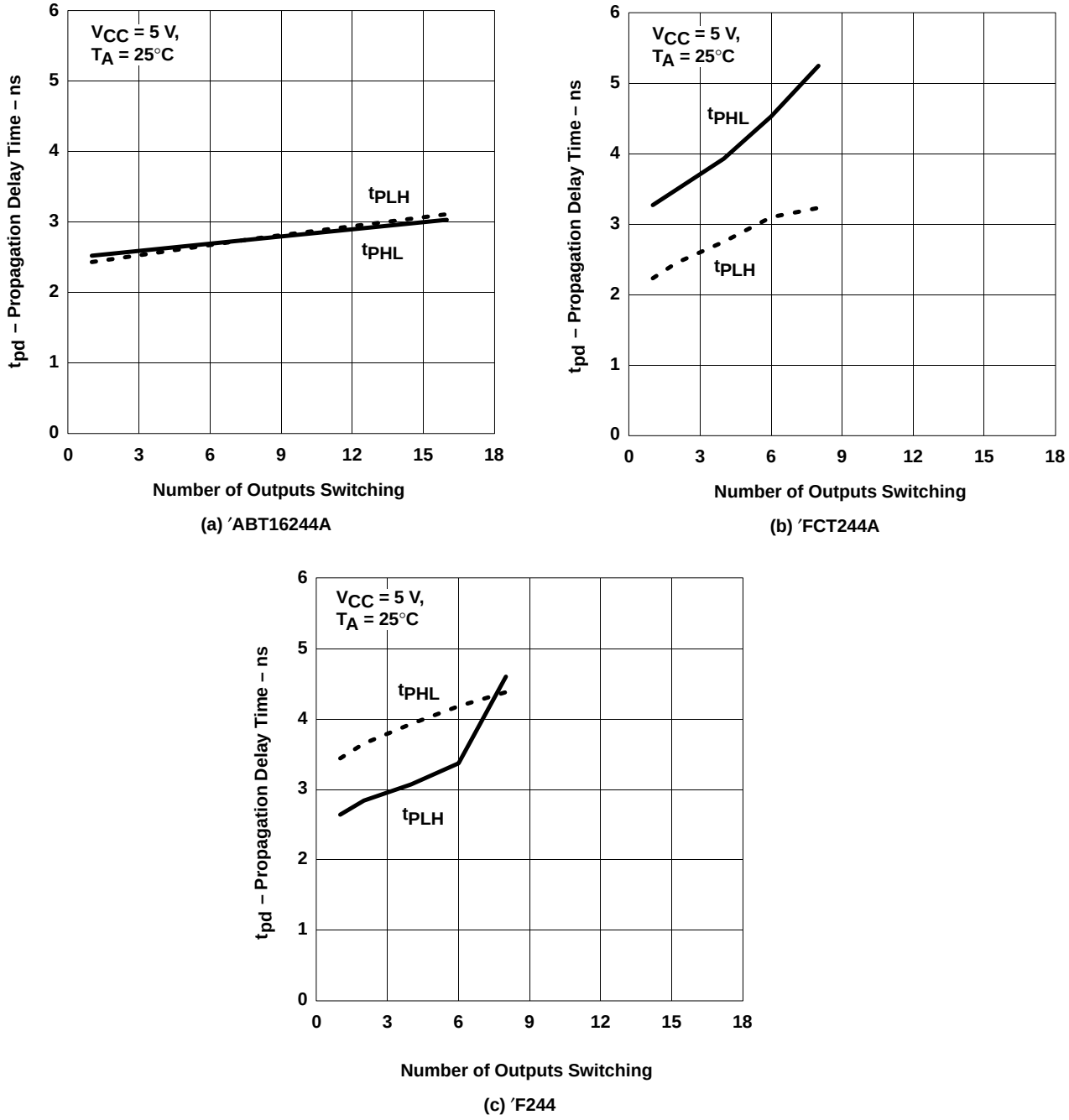
NOTE: MAX is data sheet specification

Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y



NOTE: MAX is data sheet specification

Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y (Continued)

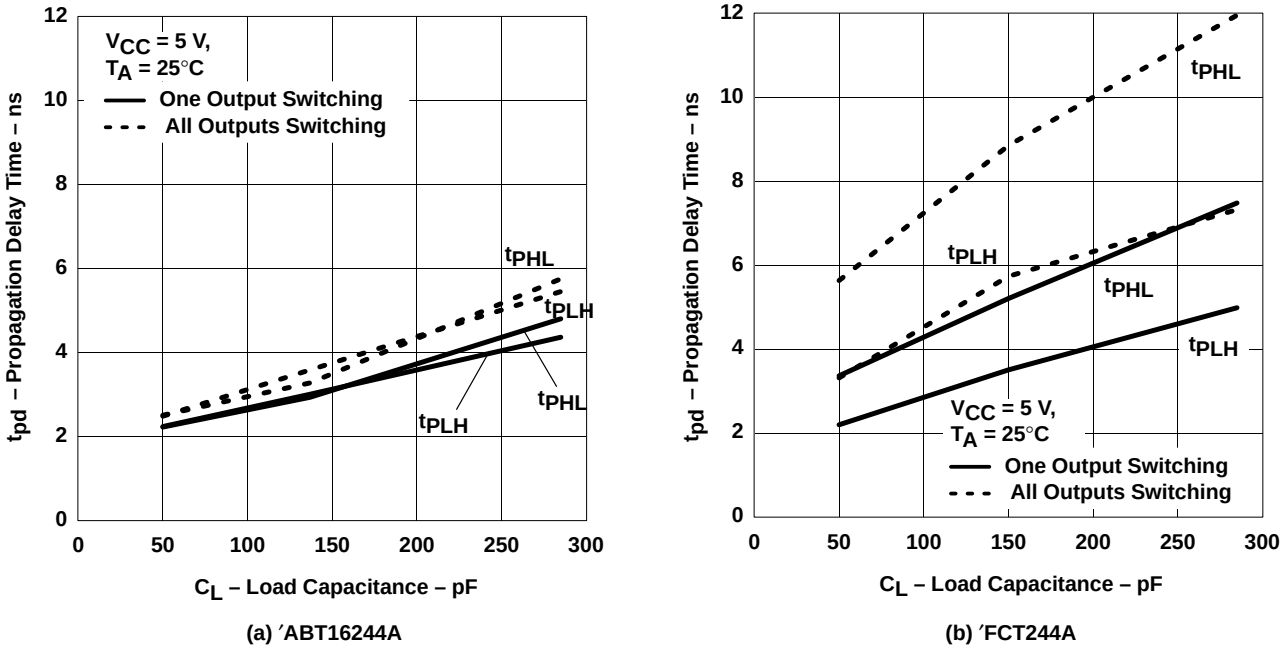


(a) ′ABT16244A

(b) ′FCT244A

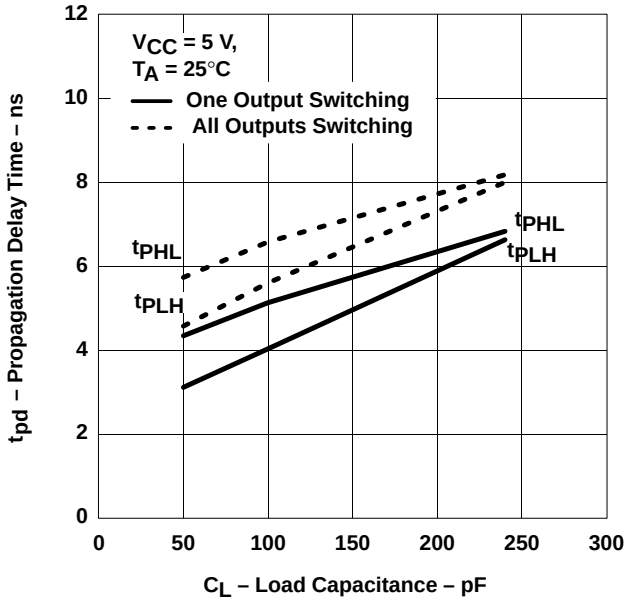
(c) ′F244

Figure 2. Propagation Delay Time vs Number of Outputs Switching



(a) ′ABT16244A

(b) ′FCT244A



(c) ′F244

Figure 3. Propagation Delay vs Capacitive Load

Power Considerations

With the challenge to make systems more dense while improving performance comes the need to replace power-hungry devices without compromising speed. The ABT family of drivers provides a solution with low CMOS power consumption and high-speed bipolar technology together on a single device.

There are two basic things to consider when calculating power consumption, static (dc) power and dynamic power. Static power is calculated using the value of I_{CC} as shown in the data sheet. This is a dc value with no load on the outputs. To understand the relationship between pure CMOS, pure bipolar, and advanced BiCMOS for dc power rating, see Table 1 which shows the various data sheet values. The bipolar device shows the highest I_{CC} values, with little relief regardless of the state of the outputs. This is not the case with ABT octals, which offer the low static power consumption of CMOS while in the high-impedance state, or when the outputs are high (I_{CCZ}, I_{CCH}).

Table 1. Supply Current

PARAMETER	TEST CONDITIONS		′F244		′FCT244		SN74ABT244	
			MIN	MAX	MIN	MAX	MIN	MAX
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		60 mA				250 μA
		Outputs low		90 mA				30 mA
		Outputs disabled		90 mA				250 μA
	V_{CC} = maximum, V ≥ V_{CC} – 0.2 V, V ≤ V_{CC} – 0.2 V					1.5 mA		

Dynamic power involves the charging and discharging of internal capacitances as well as the external load capacitance. It is this dynamic component which makes up the majority of the total power dissipation. Figure 4 shows power as a function of frequency for ABT, FCT and F devices. Although bipolar devices tend to have extremely high static power, there is a point on the frequency curve, commonly referred to as the crossover point, where the CMOS device no longer consumes less power. With ABT devices, the power increase at higher frequencies is less than that of the pure CMOS FCT.

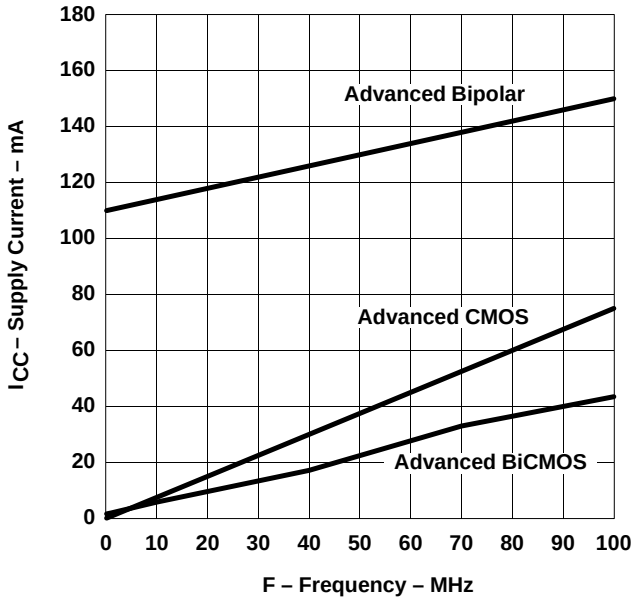


Figure 4. Supply Current vs Frequency

The use of bipolar transistors in the output stage is advantageous in two ways. First, the voltage swing is less than with a CMOS output, reducing the power consumed when charging or discharging the external load. Second, bipolar transistors are capable of turning off more efficiently than CMOS transistors, thus reducing the flow of current from V_{CC} to GND. Combined, these features allow for better power performance at high frequencies.

Input Characteristics

ABT bus interface devices are designed to guarantee TTL-compatible input levels switching between 0.8 V and 2 V (typically 1.5 V). Additionally, these inputs are implemented with CMOS circuitry, resulting in high impedance (low leakage) and low capacitance which reduces overall bus loading. This section is an overview of the circuitry utilized for a typical ABT input, the corresponding electrical characteristics, and guidelines for proper termination of unused inputs.

ABT Input Circuitry

Figure 5 shows a typical ABT input schematic. A pure CMOS-input threshold is normally set at one half of V_{CC}. In order to shift the threshold voltage to be centered around 1.5 V (see Figure 6), the supply voltage of the input stage is dropped by the diode, D1, and the transistor, Q1. Reducing the voltage at the source of Q_p enables it to turn off more efficiently when flow is from V_{CC} to GND (ΔI_{CC}). When the input is in the low state, Q_r raises the voltage of the source of Q_p to V_{CC} to ensure proper operation of the following stage. This feedback circuit provides approximately 100 mV of input hysteresis which increases the noise margin and helps ensure the device will be free from oscillations when operated within specified input ramp rates.

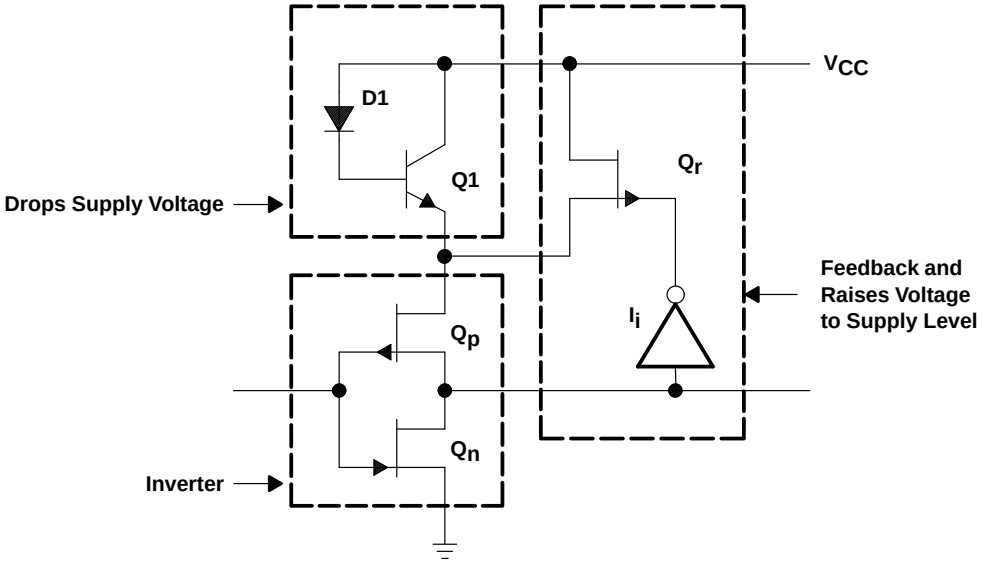


Figure 5. Simplified Input Stage of an ABT Circuit

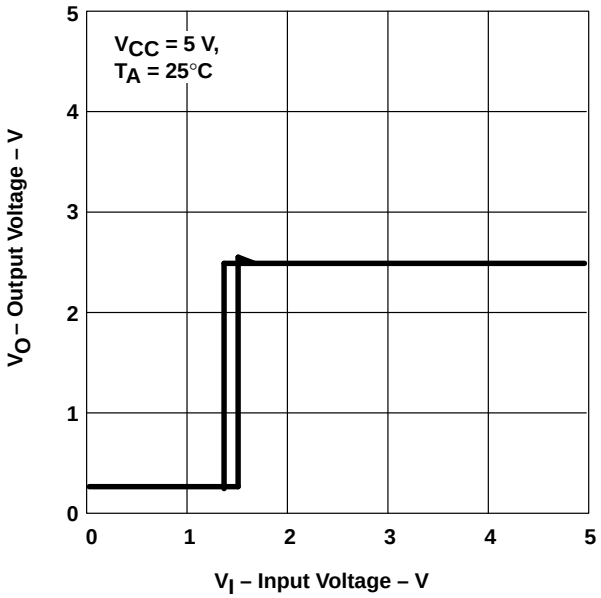


Figure 6. Output Voltage vs Input Voltage

Input Current Loading

The utilization of submicron (0.8-μm) CMOS technology for the input stage of ABT devices causes minimal loading of the system bus due to low leakage currents and low capacitance. The small geometries of the EPIC-IIB™ process have resulted in capacitances as low as 3 pF for inputs and 8 pF for C_{io} of a transceiver. Figure 7 and Table 2 indicate the low input current performance and specifications. Considering this low capacitance along with the negligible input current, it is clear that systems designers will be able to decrease their overall bus loading.

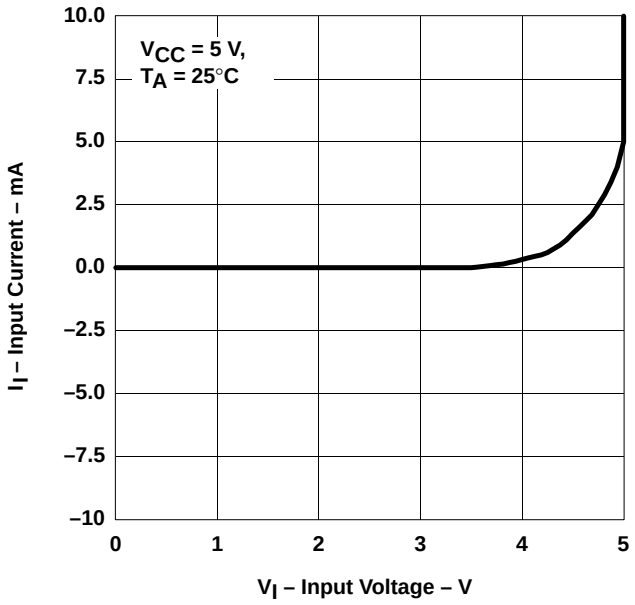


Figure 7. Input Current vs Input Voltage

Table 2. Input Current Specifications

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT245		SN74ABT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZH}†	V_{CC} = 5.5 V,	V_O = 2.7 V			50		50		50	µA
I_{OZL}†	V_{CC} = 5.5 V,	V_O = 0.5 V			−50		−50		−50	µA

† The parameters I_{OZH} and I_{OZL} include the input leakage current.

Supply Current Change (ΔI_{CC})

Because ABT devices utilize a CMOS-input stage but operate in a TTL-level signal environment, there is a current specification unique to this set of conditions known as ΔI_{CC}. Given a CMOS inverter with the input voltage set so that both the p and n channel devices are on, current will flow from V_{CC} to GND. This can occur when the input to an ABT device is at a valid high level (>2 V) which will turn on the n-channel, but not high enough to completely turn off the p-channel device. The current which flows under these conditions is specified in the data sheet (ΔI_{CC}) and is measured one input at a time with the input voltage set at 3.4 V. Figure 8 shows the change in I_{CC} as the input is ramped from 0 V to 5 V. For ABT non-storage devices, a feature is added which turns the input off when the outputs are disabled in order to reduce power consumption (see Table 3 for an example. Refer to individual data sheets for this specification).

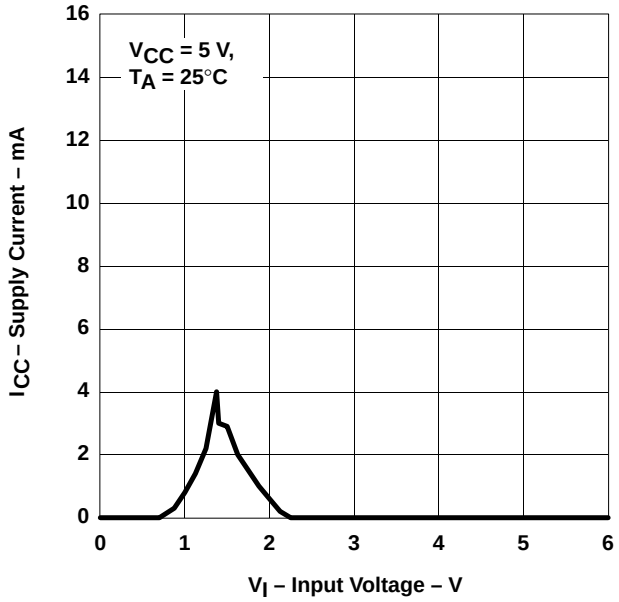


Figure 8. Supply Current vs Input Voltage

Table 3. Supply Current Change (ΔI_{CC})

PARAMETER	TEST CONDITIONS		T_A = 25°C		SN54ABT244		SN74ABT244		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC}†	V_I = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled		1.5		1.5		1.5	mA
		Outputs disabled		50		50		50	µA

† This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Proper Termination of Unused Inputs

With advancements in speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output glitching or, in some cases, oscillations. Similar situations can occur if an unused input is left floating or not being actively held at a valid logic level.

These problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 9). Since the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, the inductive voltage spikes (V_{gnd}) affect the way signals appear to the internal gate structures. For instance, as the voltage at the device's ground node rises, the input signal (V_i') will appear to decrease in magnitude. This undesirable phenomena can erroneously change the output's transition if a threshold violation takes place.

In the case of a slowly rising input edge, if the ground movement is large enough, the apparent signal, V_i', at the device will appear to be driven back through the threshold and the output will start to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents) the slow input edge will be repeatedly driven back through the threshold, resulting in output oscillation.

ABT devices are recommended to have input edge rates faster than 5 ns/V for standard parts, and 10 ns/V for the Widebus™ series of products when the outputs are enabled. A critical area for this edge rate is in the transition region between 1 V and 2 V. It is also recommended to hold inputs or I/O pins at a valid logic high or low when they are not being used or when the part driving them is in the high-impedance state.

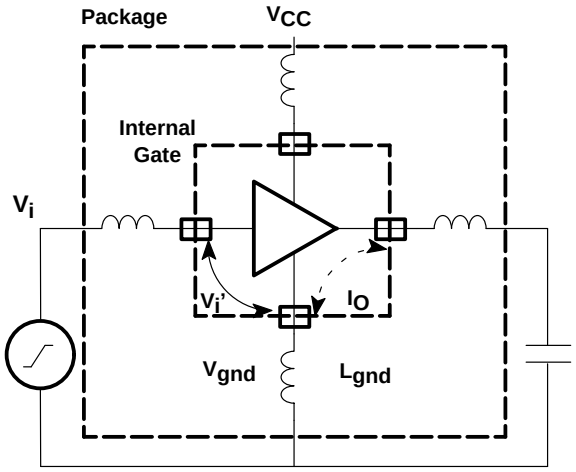


Figure 9. Sample Input/Output Model

Output Characteristics

The current trend is consolidation of the functionality of multiple logic devices into complex, high pin-count ASICs and programmables. There are a number of important advantages for utilizing bus-interface devices in standard high-volume packages. These include the need for high drive capability and good signal integrity. The use of bipolar circuitry in the output stage makes it possible to provide these requirements, along with increased speed, using the ABT family.

Figure 10 shows a simplified schematic of an ABT output stage. Data is transmitted to the gate of M1, which acts as a simple current switch. When M1 is turned on, current flows through R1 and M1 to the base of Q4, turning it on and driving the output low. At the same time, the base of Q2 is pulled low, thus turning off the upper output. For a low-to-high transition, the gate of M1 must be driven low, turning M1 off. Current through R1 will charge the base of Q2, pulling it high and turning on the Darlington pair consisting of Q2 and Q3. Meanwhile, with its supply of base drive cut off, Q4 turns off, and the output switches from low to high. R2 is used to limit output current in the high state, and D1 is a blocking diode used to prevent reverse current flow in specific power-down applications.

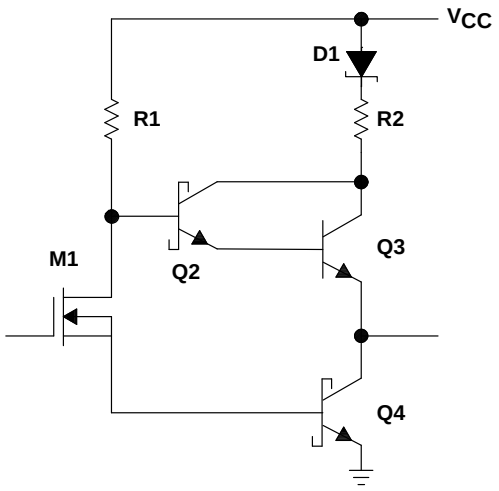


Figure 10. Simplified ABT Output Stage

A clear advantage of using bipolar circuitry in the output stage (as opposed to CMOS) is the reduced voltage swing. This helps to lower ground noise and reduce power consumption. Refer to the sections on Signal Integrity and Power Considerations for further information.

Output Drive

The I_{OH} and I_{OL} curves for a typical ABT output are shown in Figure 11. With a specified I_{OL} of 64 mA and I_{OH} of –32 mA, ABT will accommodate many standard backplane specifications. However, these devices are capable of driving well beyond these limits. This is important when considering switching a low-impedance backplane on the incident wave.

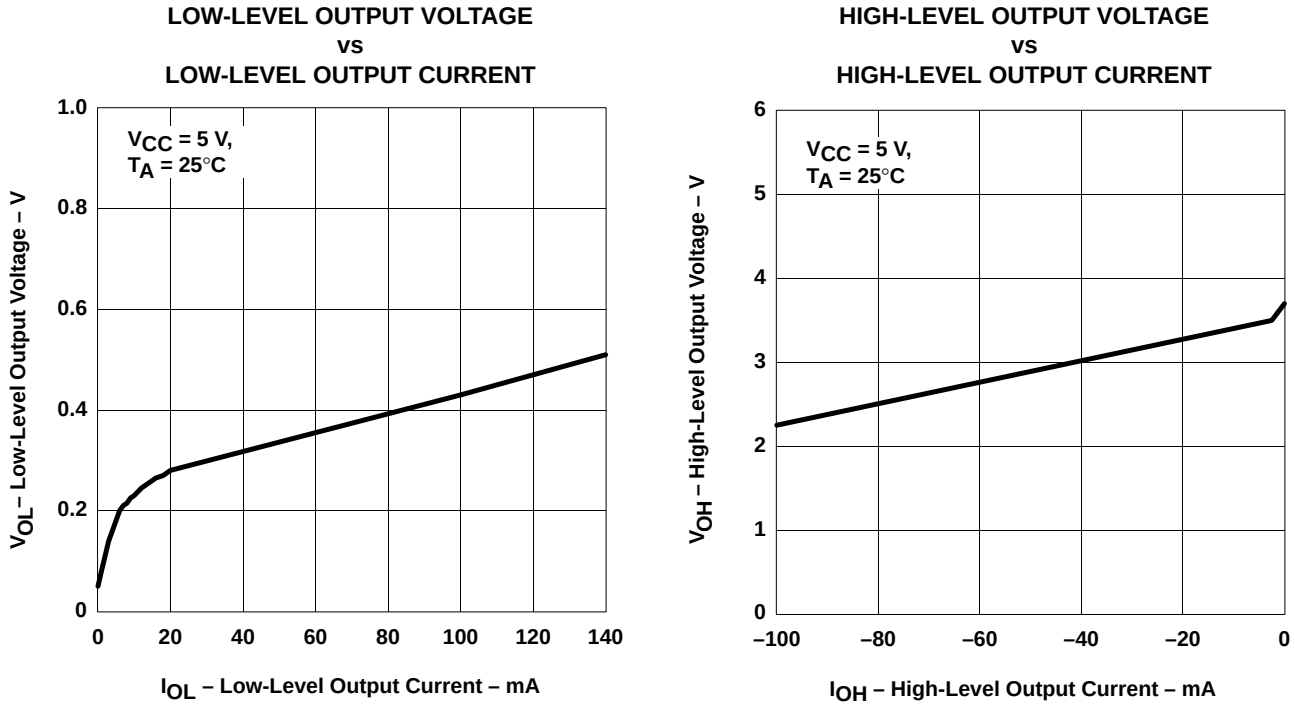


Figure 11. Typical ABT Output Characteristics

Incident-wave switching ensures that for a given transition (either high-to-low or low-to-high) the output will reach a valid V_{IH} or V_{IL} level on the initial wave front (i.e., does not require reflections). Figure 12 shows the possible problems a designer might encounter when a device does not switch on the incident wave. A shelf below $V_{IL(max)}$, signal A, will cause the propagation delay to slow by the amount of time it takes for the signal to reach the receiver and reflect back. Signal B shows the case where there is a shelf in the threshold region. When this happens the input to the receiver is uncertain and could cause several problems associated with slow input edges, depending on the length of time the shelf remains in this region. A signal as seen in example C will not cause a problem because the shelf does not occur until the necessary V_{IH} level has been attained.

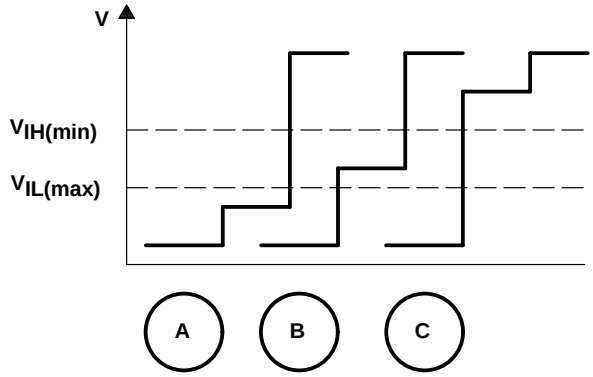


Figure 12. Reflected Wave Switching

Using typical V_{OH} and V_{OL} values along with data points from the curves, ABT devices can typically drive lines in the 25-Ω range on the incident wave.

For a low-to-high transition, (I_{OH} = 85 mA @ V_{OH} = 2.4 V)

$$Z_{LH} = \frac{V_{OH}(min) - V_{OL}(typ)}{I_{OH}} = \frac{2.4\ V - 0.3\ V}{85\ mA} = 25\ \Omega$$

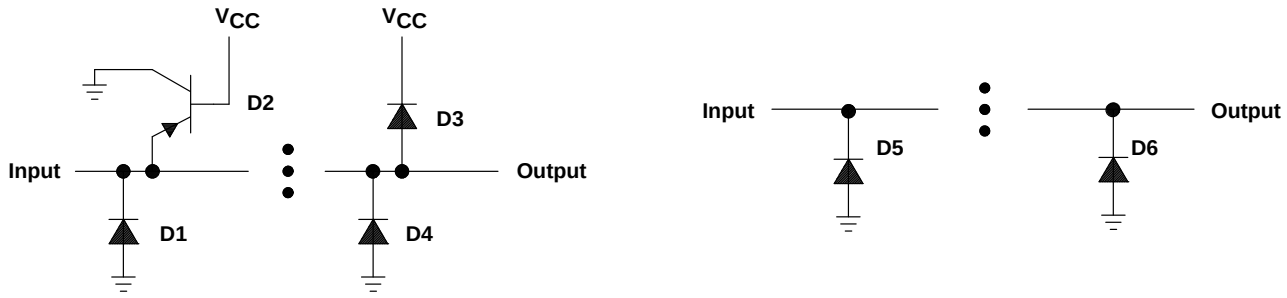
For a high-to-low transition, (I_{OL}= 135 mA @ V_{OL}= 0.5 V)

$$Z_{HL} = \frac{V_{OH}(typ) - V_{OL}(max)}{I_{OL}} = \frac{3.5\ V - 0.5\ V}{135\ mA} = 22\ \Omega$$

Partial Power Down

One application, addressed when designing the ABT family, is partial system power down. When using a standard CMOS device, there is a path from either the input or the output (or both) to V_{CC}. This prevents partial power down for such applications as *hot-card insertion* without adding current limiting components. This is not the case with ABT as these paths have been eliminated with the use of blocking diodes. Figure 13 shows functionally equivalent schematics of the input structures for CMOS and ABT devices.

Consider the situation shown in Figure 14. The driving device is powered with V_{CC} = 5 V while the receiving device is powered down (V_{CC} = 0). If these devices are CMOS, the receiver can be powered up through the diode, D2, when the driver is in a high state. ABT devices do not have a comparable path and are thus immune to this problem, making them more desirable for this application.



(a) CMOS EQUIVALENT INPUT STRUCTURE (b) ABT EQUIVALENT INPUT STRUCTURE

Figure 13. Simplified Input Structures for CMOS and ABT Devices

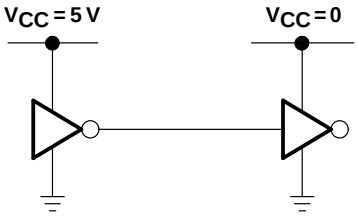


Figure 14. Example of Partial System Power Down

Signal Integrity

A frequent concern system designers have is the performance degradation of ICs when outputs are switched. Texas Instruments priority when designing the ABT bus interface family is to insure signal integrity and eliminate the need for excess settling time of an output waveform. This section addresses the simultaneous switching performance of both the ABT octals and the Widebus™ functions.

Simultaneous-Switching Phenomenon

Figure 15 shows a simple model of an output pin, including the associated capacitance of the output load and the inherent inductance of the ground lead. The voltage drop across the GND inductor, V_L, is determined by the value of the inductance and the rate of change in current across the inductor. When multiple outputs are switched from high to low, the transient current (di/dt) through the GND inductor generates a difference in potential on the chip ground with respect to the system ground. This induced GND variation can be observed indirectly as shown in Figure 16. The voltage output low peak (V_{OLP}) is measured on one quiet output when all others are switched from high to low.

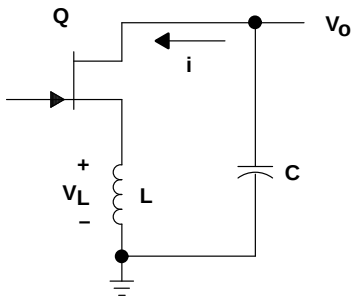
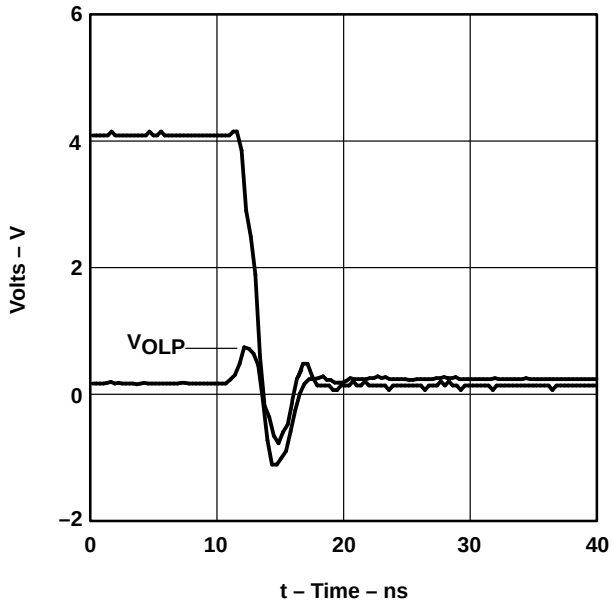


Figure 15. Simultaneous-Switching Output Model



NOTE: V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs

Figure 16. Simultaneous-Switching-Noise Waveform

A similar phenomena occurs with respect to the V_{CC} plane on a low-to-high transition, known as voltage output high valley (V_{OHV}). Most problems are associated with a large V_{OLP} because the range for a logic 0 is much less than the range for a logic 1, as seen in Figure 17. For a comprehensive discussion of simultaneous switching, see the *Simultaneous Switching Evaluation and Testing* application note or the *Advanced CMOS Logic Designer's Handbook* from Texas Instruments.

The impact of these voltage noise spikes on a system can be extreme. The noise can cause loss of stored data, severe speed degradation, false clocking, and/or reduction in system noise immunity. For an overview of how propagation delay is affected by the switching of multiple outputs, please refer to the AC Performance section of this document.

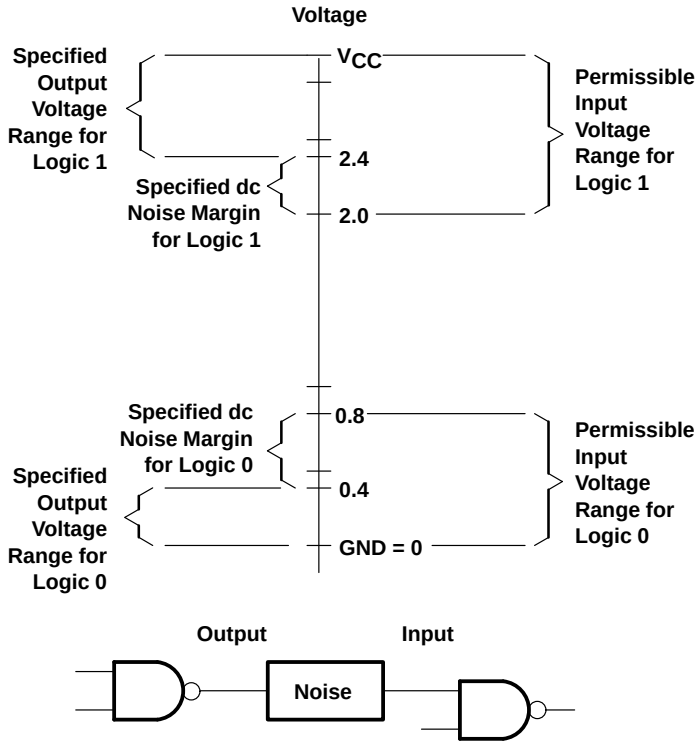


Figure 17. TTL dc Noise Margin

Simultaneous Switching Solutions

Some methods an IC manufacturer can use to reduce the effects of simultaneous switching include: reducing the inductance of the power pins, adding multiple power pins, and controlling the turn on of the output. These techniques are described in depth in the 1988 Texas Instruments *Advanced CMOS Logic (ACL) Designer's Handbook*.

Octal ABT devices employ the standard end-pin GND and V_{CC} configuration while maintaining acceptable simultaneous switching performance, as seen in Figure 18. This is due to the TTL-level output swing (0.3–3 V) and a controlled feedback which limits the base drive to the lower output.

The ABT Widebus™ series (16-, 18-, and 20-bit functions) are offered in an SSOP package (see the Packaging section of this document) which was developed by Texas Instruments to save valuable board space and reduce simultaneous switching effects. One might expect an increase in noise with sixteen outputs switching in a single package; however, the simultaneous switching performance is actually improved. There is a GND pin for every two outputs and a V_{CC} pin for every four. This allows the transient current to be distributed across multiple power pins and decreases the overall d_i/d_t effect. This results in a typical V_{OLP} value on the order of 500 mV for the ABT16500, as shown in Figure 19.

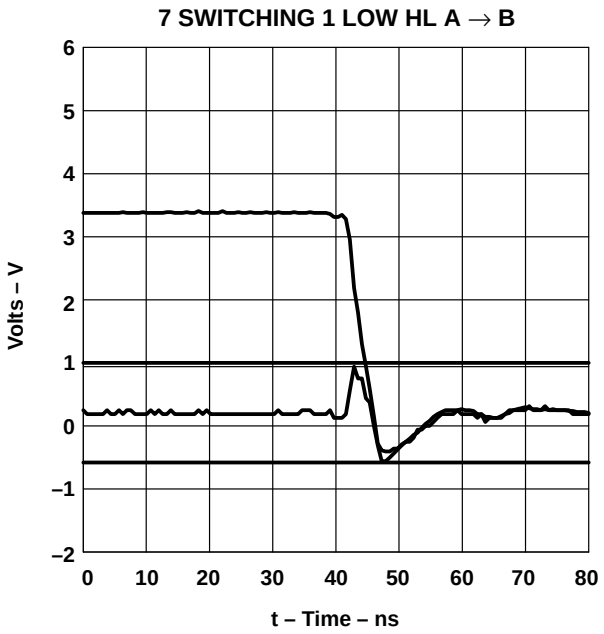


Figure 18. ABT646A Simultaneous-Switching Waveform

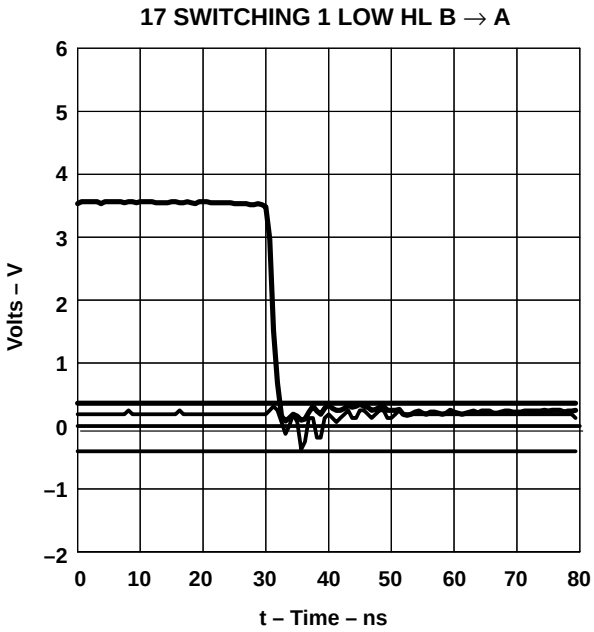


Figure 19. ABT16500A Simultaneous-Switching Waveform

Advanced Packaging

Along with a strong commitment to provide fast, low- power, high-drive integrated circuits, Texas Instruments is the clear-cut leader in logic packaging advancements. The development of the shrink small- outline package (SSOP) in 1989 provided system designers the opportunity to reduce the amount of board space required for bus interface devices by 50%. Several 24-pin solutions including the familiar SOIC, the SSOP, and the TSOP (thin small-outline package) are shown in Figure 20.

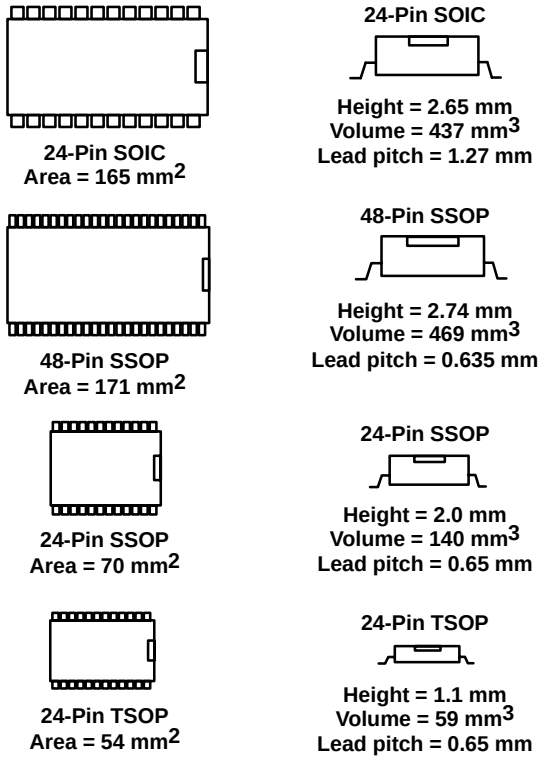


Figure 20. 24-Pin Surface-Mount Comparison

The 48/56-pin SSOP packages allow for twice the functionality (16-, 18-, and 20-bit functions) in approximately the same board area as a standard SOIC. This is accomplished by using a 25-mil (0.635 mm) lead pitch, as opposed to 50-mil (1.27 mm) in SOIC. Figure 21 shows a typical pinout structure for the 48-pin SSOP. The flow-through architecture is standard for all Widebus™ devices, making signal routing easier during board layout. Also note the distributed GND and V_{CC} pins, which improve simultaneous switching effects as discussed in the Signal Integrity section of this document.

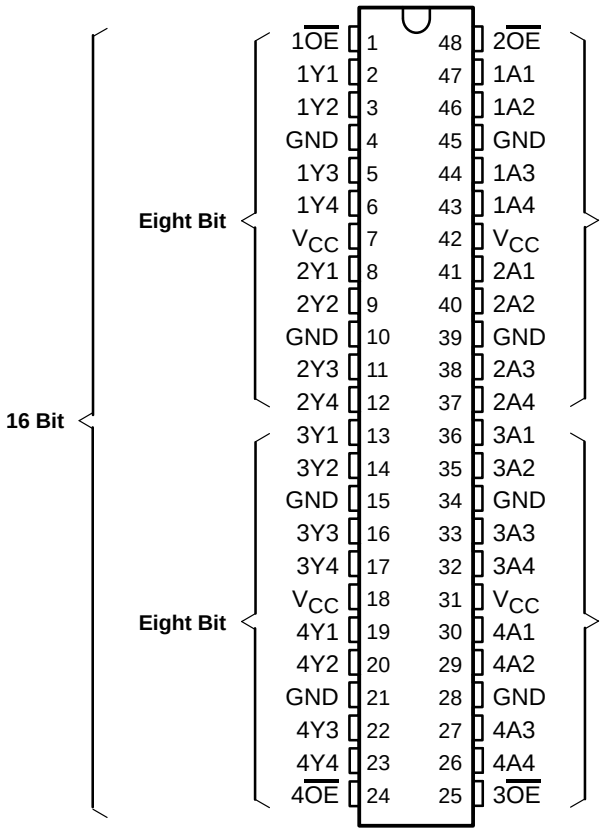


Figure 21. Distributed Pinout of ′ABT16244A

When using the small pin count SSOPs (8-, 9-, and 10-bit functions) the same functionality will occupy less than half the board area of a SOIC (70 mm^2 vs 165 mm^2). There is also a height improvement over the SOIC which is beneficial when the spacing between boards is a consideration. For very dense memory arrays the packaging evolution has been taken one step further with the emerging TSOP. The TSOP thickness of 1.1 mm gives a 58% height improvement over the SOIC.

Table 4 provides a quick reference of the mechanical specifications of the various SSOP packages. If more specific information is required see the *SSOP Designer's Handbook* or the application note Advanced Bus-Interface Solutions Utilizing Fine-Pitch Surface-Mount Packages.

Table 4. SSOP Metric Specifications†

PACKAGE SPECIFICATIONS						PIN SPECIFICATIONS	
PACKAGE TYPE	PINS	INDUSTRY STANDARD	THICKNESS (mm)	BODY WIDTH (mm)	STANDOFF HEIGHT (mm)‡	PIN PITCH (mm)	PIN WIDTH (mm)
SSOP	20	EIAJ	2.00	5.3	0.05	0.650	0.30
SSOP	24	EIAJ	2.00	5.3	0.05	0.650	0.30
SSOP	28	JEDEC	2.59	7.5	0.20	0.635	0.25
SSOP	48	JEDEC	2.59	7.5	0.20	0.635	0.25
SSOP	56	JEDEC	2.59	7.5	0.20	0.635	0.25

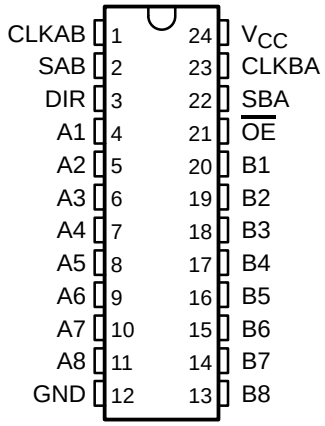
† All values are maximum typical values unless otherwise indicated.
‡ Minimum values

APPENDIX A
′ABT646A

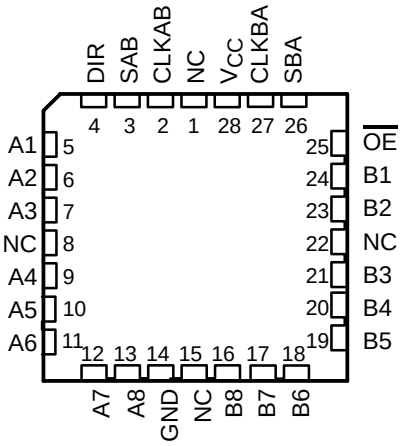
A

- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**

SN54ABT646A . . . JT PACKAGE
SN74ABT646A . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT646A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′ABT646A.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

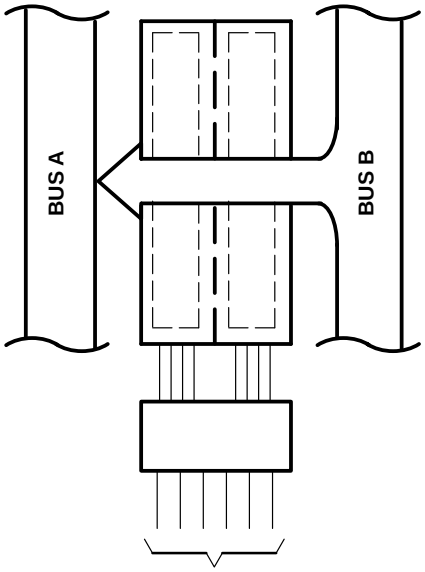
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT646A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

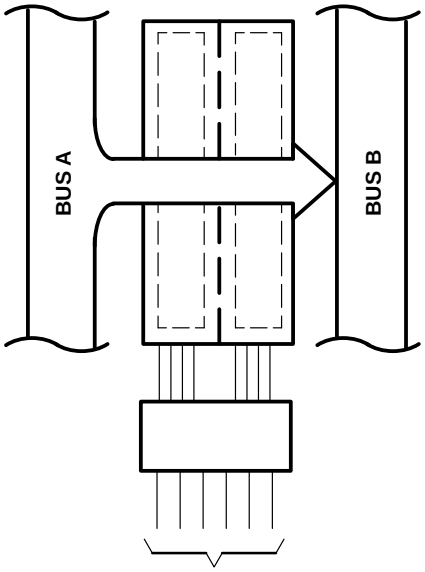
The SN54ABT646A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT646A is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



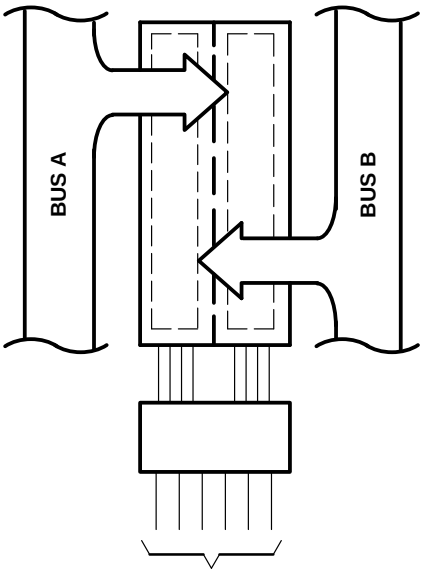
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



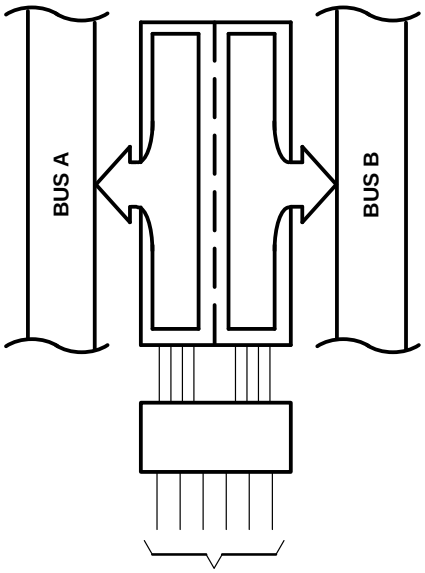
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

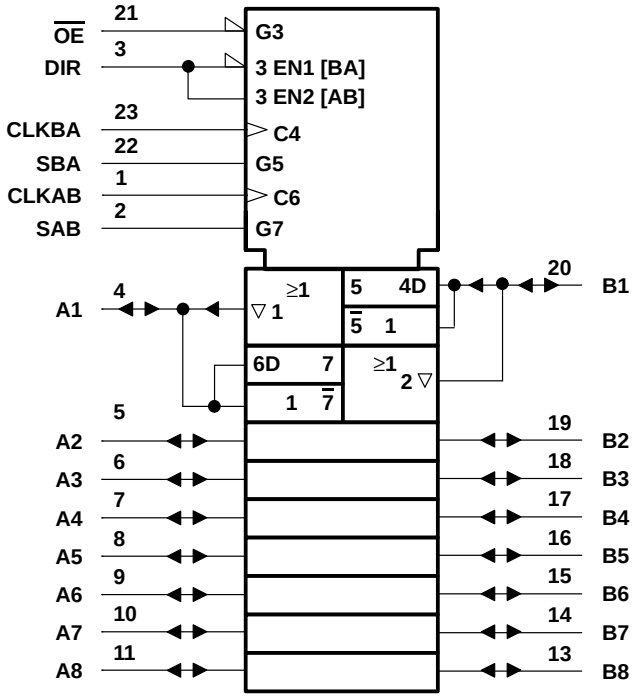
Pin numbers shown are for the DB, DW, JT, and NT packages.

FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

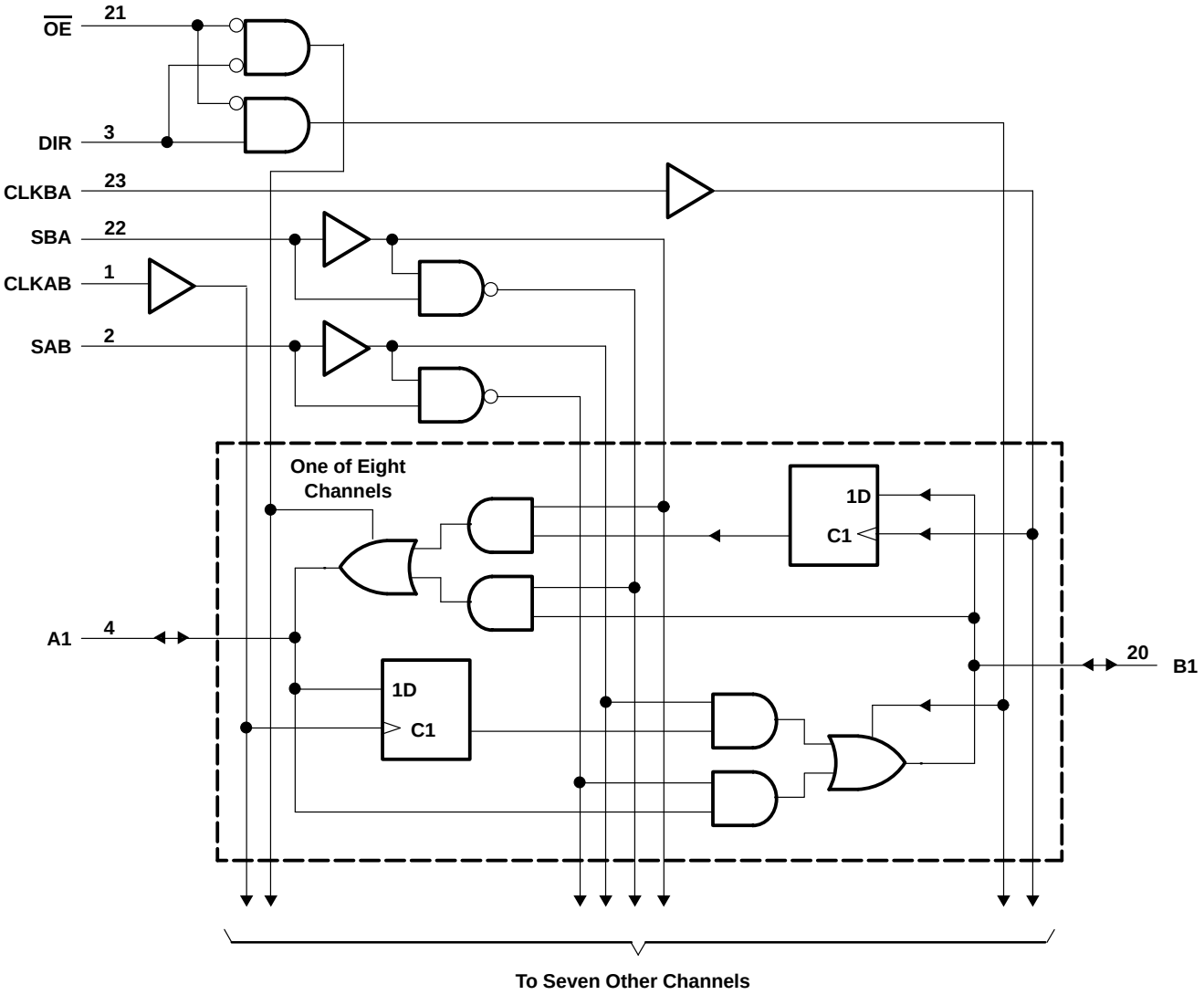
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT646A . . . . . 96 mA
SN74ABT646A . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package . . . . . 0.65 W
DW package . . . . . 1.7 W
NT package . . . . . 1.3 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT646A		SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT646A		SN74ABT646A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA		2			2				
		I_{OH} = –32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				10§		50§		10§	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–10§		–50§		–10§	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			250		250		250	µA
			Outputs low			30		30		30	mA
			Outputs disabled			250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		7						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		12						pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

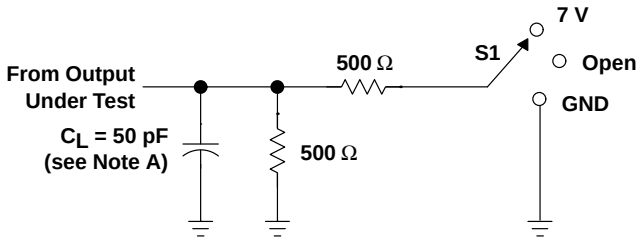
		V_{CC} = 5 V, T_A = 25°C		SN54ABT646A		SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	4		4		4		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		3.5		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		1.5		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT646A		SN74ABT646A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	6.7	2.2	5.6	ns
t_{PHL}			1.7	4	5.1	1.2	6.7	1.7	5.6	
t_{PLH}	A or B	B or A	1.5	3	4.3	1.5	5	1.5	4.8	ns
t_{PHL}			1.5	3.3	4.6	1.5	5.6	1.5	5.4	
t_{PLH}	SAB or SBA†	B or A	1.5	4	5.1	1.5	7.8	1.5	6.5	ns
t_{PHL}			1.5	3.6	4.9	1.5	6.2	1.5	5.9	
t_{PZH}	$\overline{OE}$	A or B	1.5	4.3	5.3	1.5	7	1.5	6.3	ns
t_{PZL}			3	5.8	7.4	3	10.5	3	8.8	
t_{PHZ}	$\overline{OE}$	A or B	1.5	3.5	4.5	1	7.3	1.5	5	ns
t_{PLZ}			1.5	3	4	1.5	5.7	1.5	4.5	
t_{PZH}	DIR	A or B	1.5	4.5	5.7	1.5	7.3	1.5	6.7	ns
t_{PZL}			2.5	6.5	9	2.5	11	2.5	9.5	
t_{PHZ}	DIR	A or B	1.5	3.8	5	1	9	1.5	5.7	ns
t_{PLZ}			1.5	3.8	4.7	1.2	6.7	1.5	6	

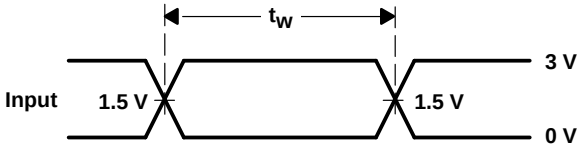
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

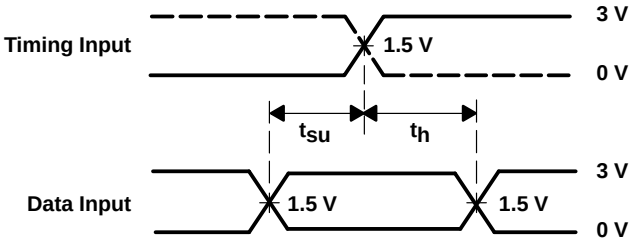


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

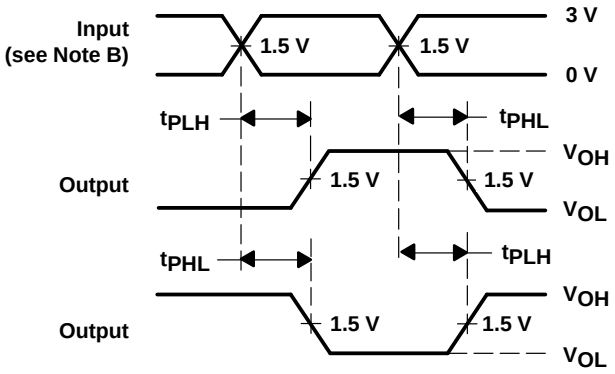
LOAD CIRCUIT FOR OUTPUTS



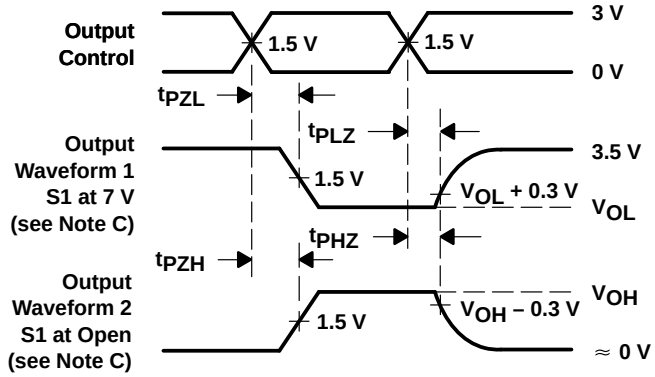
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



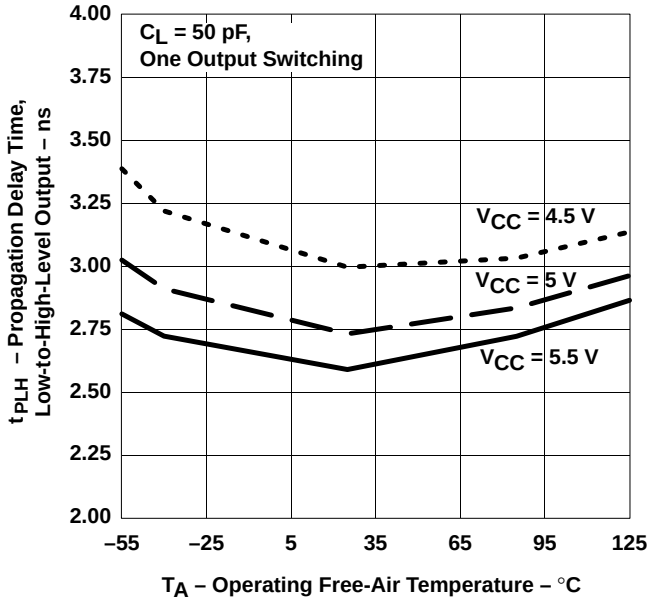
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

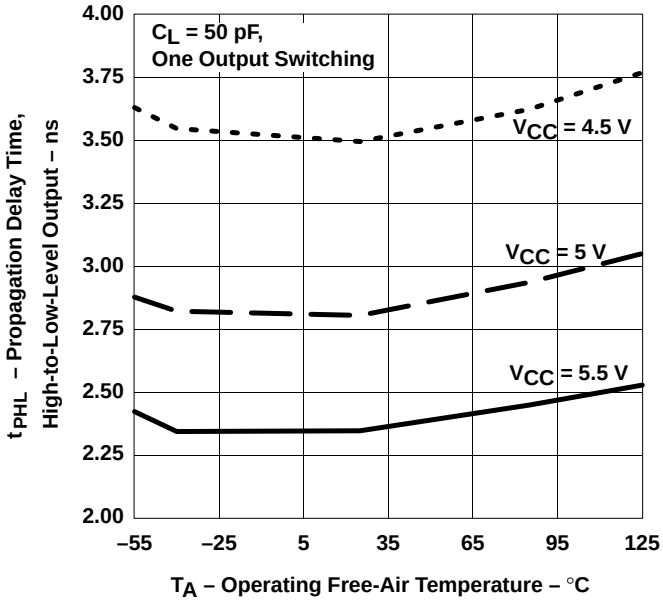
Figure 2. Load Circuit and Voltage Waveforms

Propagation Delay Time vs Temperature

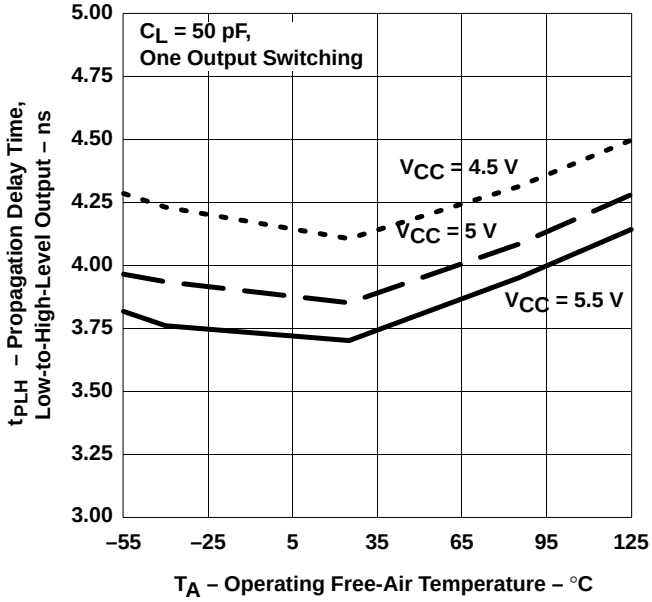
**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



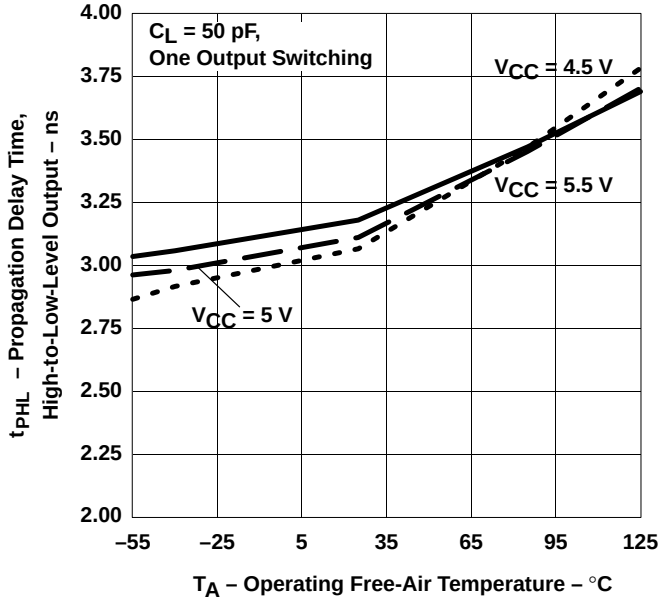
**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
CLKAB to B**

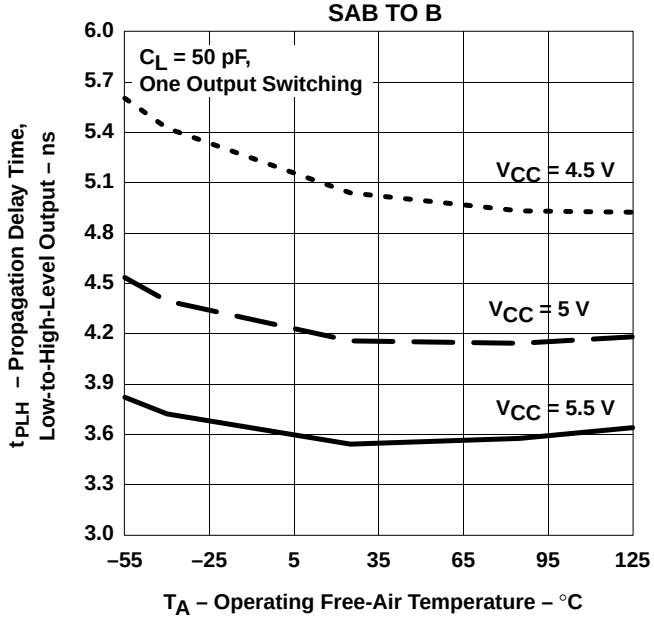


**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
CLKAB TO B**

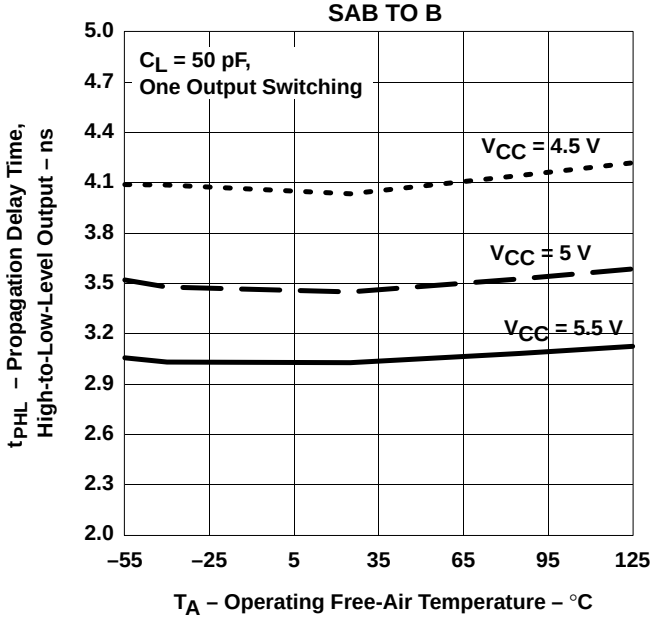


Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
SAB TO B

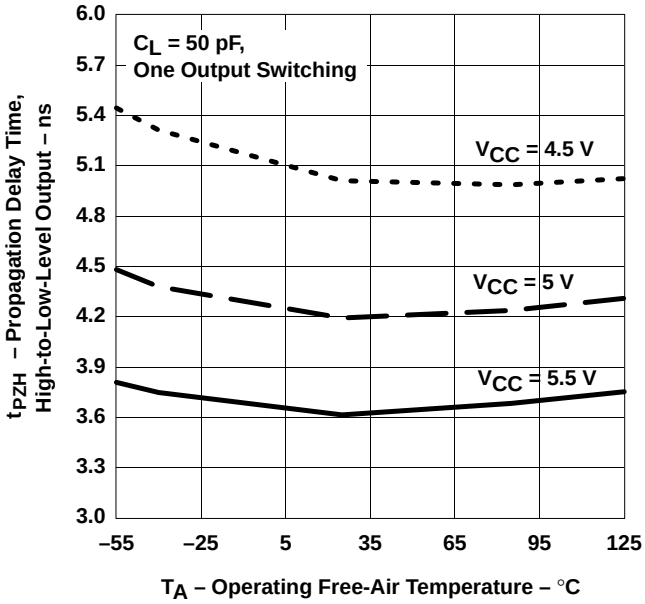


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
SAB TO B

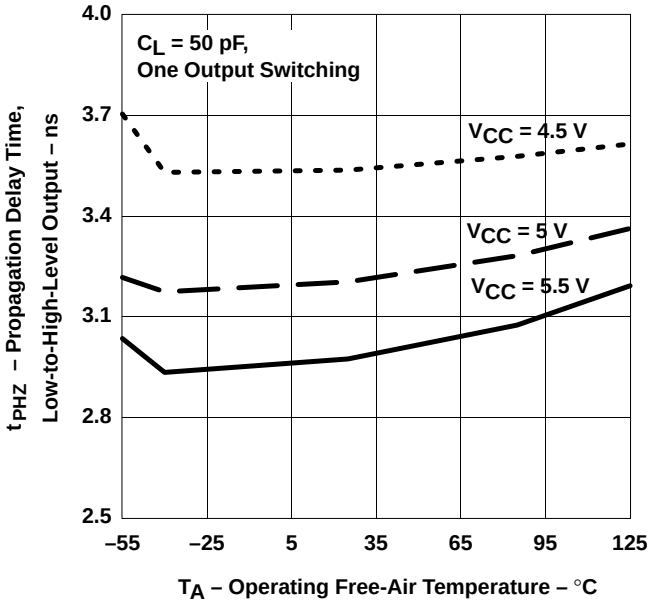


Propagation Delay Time vs Temperature

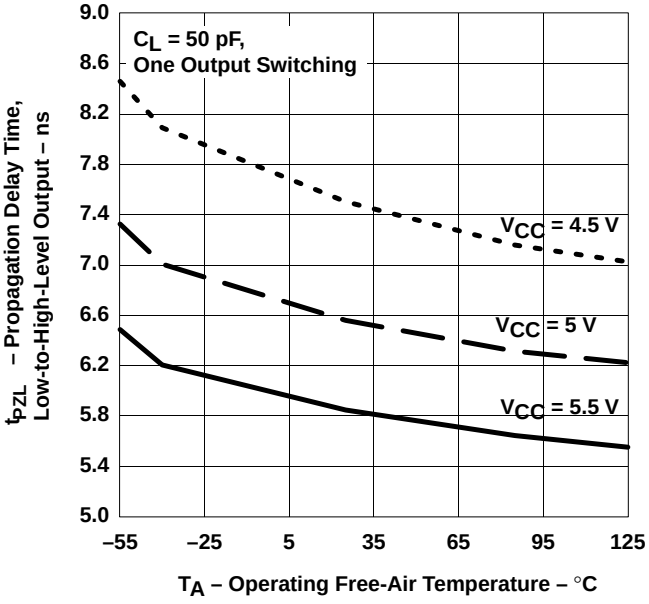
**PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B**



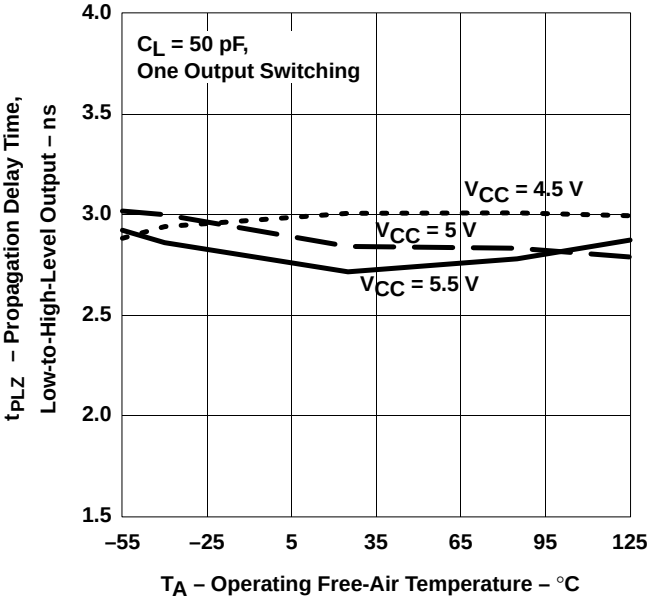
**PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B**



**PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B**

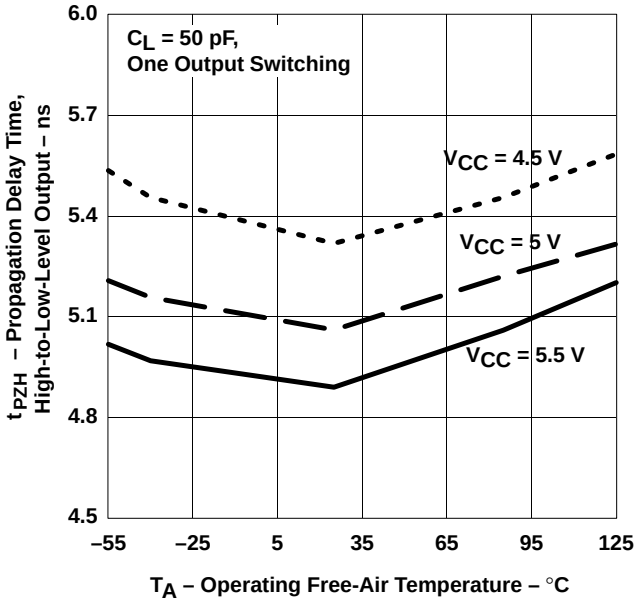


**PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B**

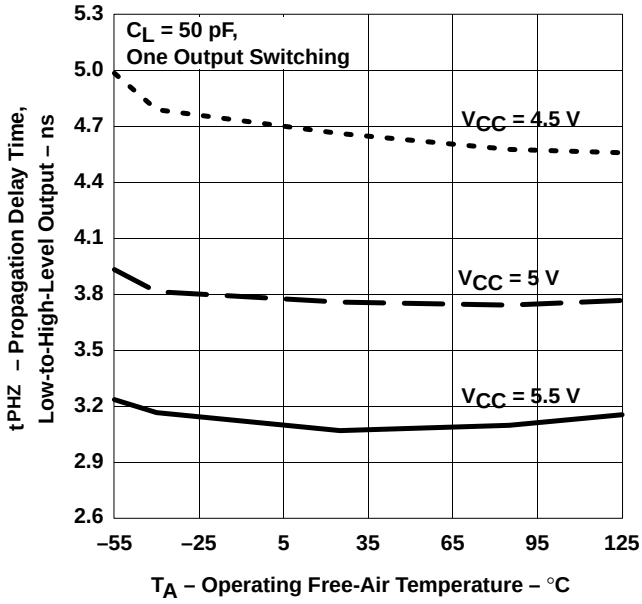


Propagation Delay Time vs Temperature

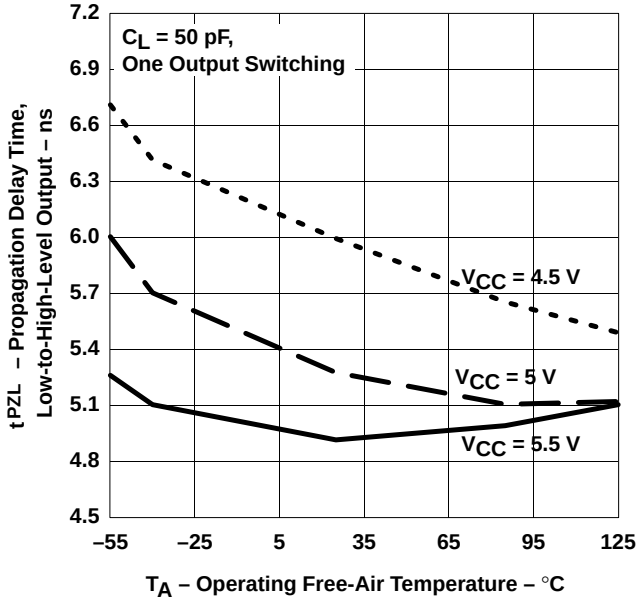
**PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**



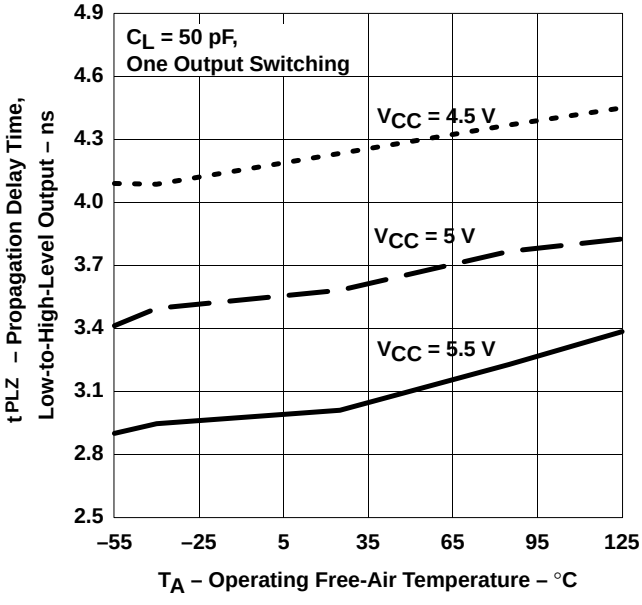
**PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**



**PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**

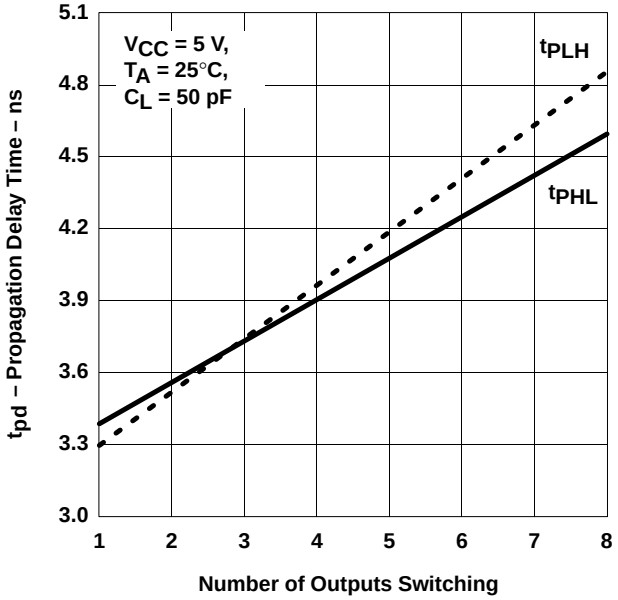


**PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**

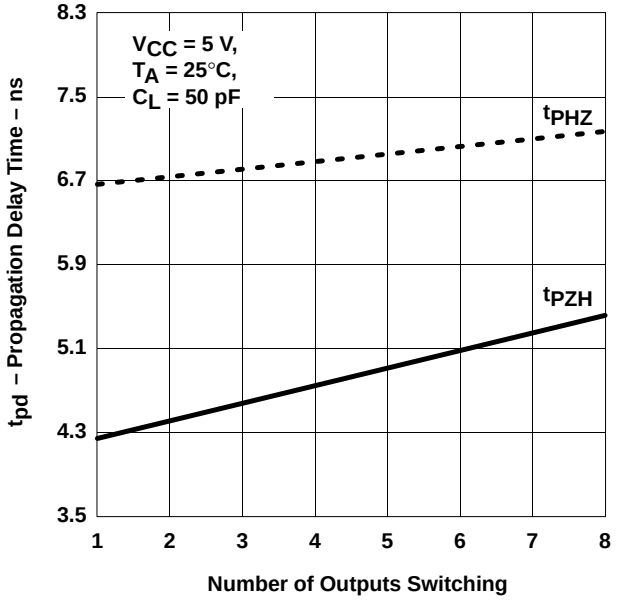


Propagation Delay Time vs Number of Outputs Switching

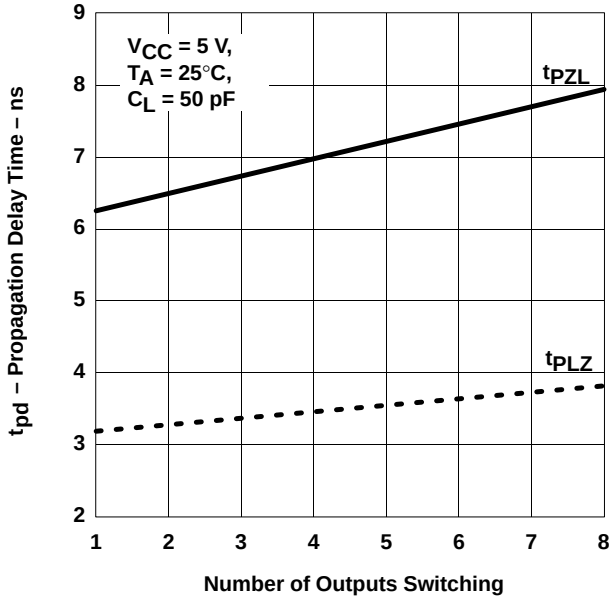
PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A TO B



PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A TO B

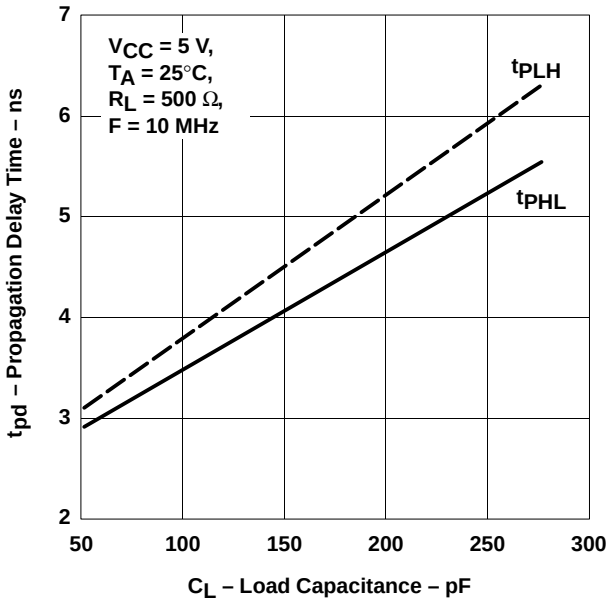


PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A TO B

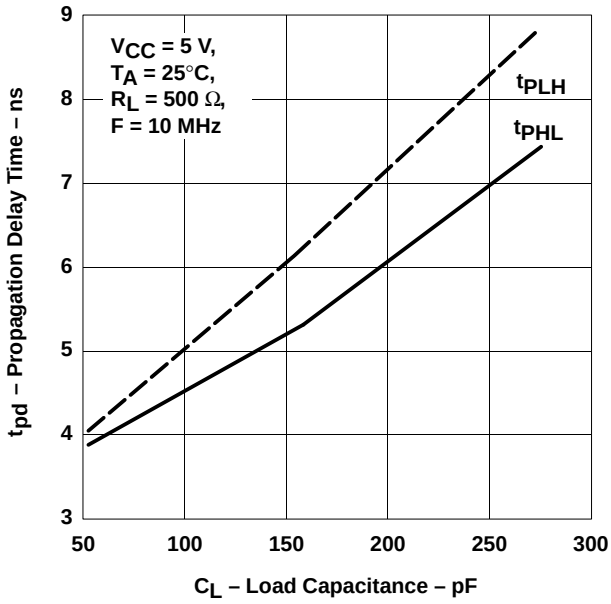


Propagation Delay Time vs Load Capacitance

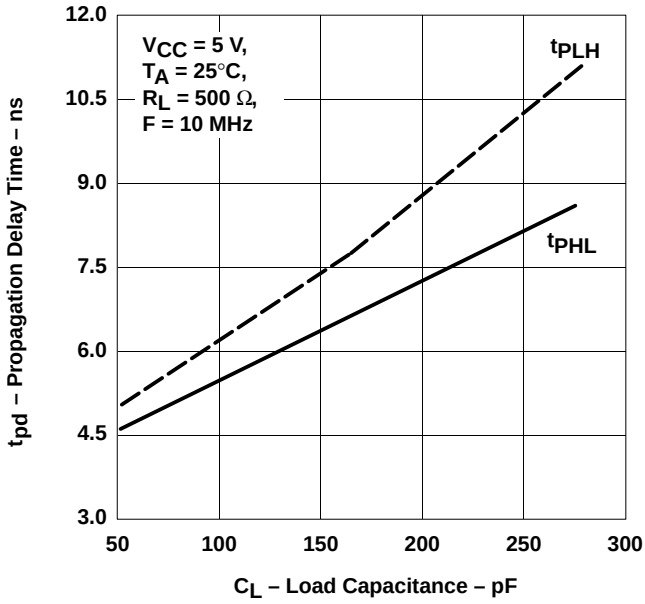
A TO B
ONE OUTPUT SWITCHING



A TO B
FOUR OUTPUTS SWITCHING

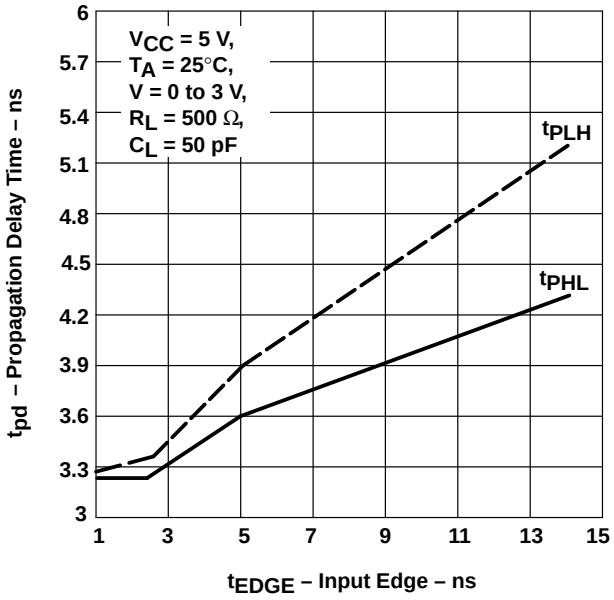


A TO B
EIGHT OUTPUTS SWITCHING

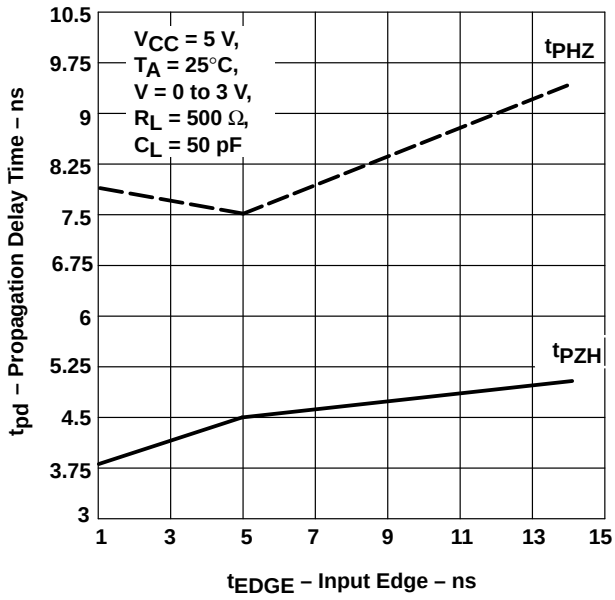


Propagation Delay Time vs Input Edge

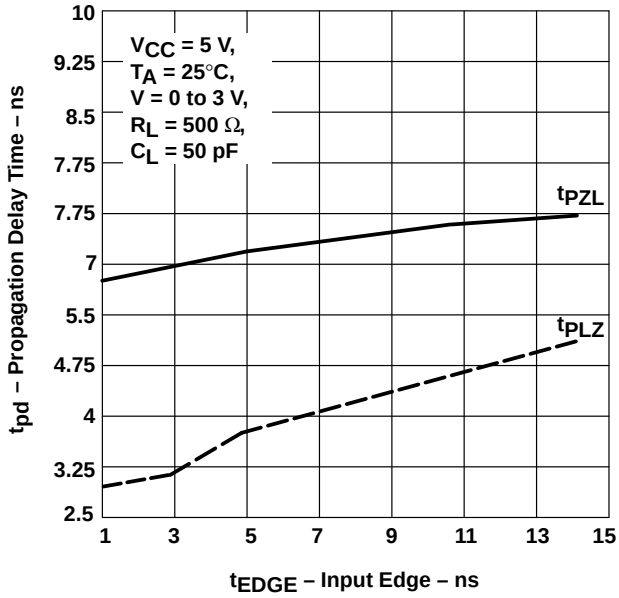
PROPAGATION DELAY TIME
vs
INPUT EDGE
A TO B



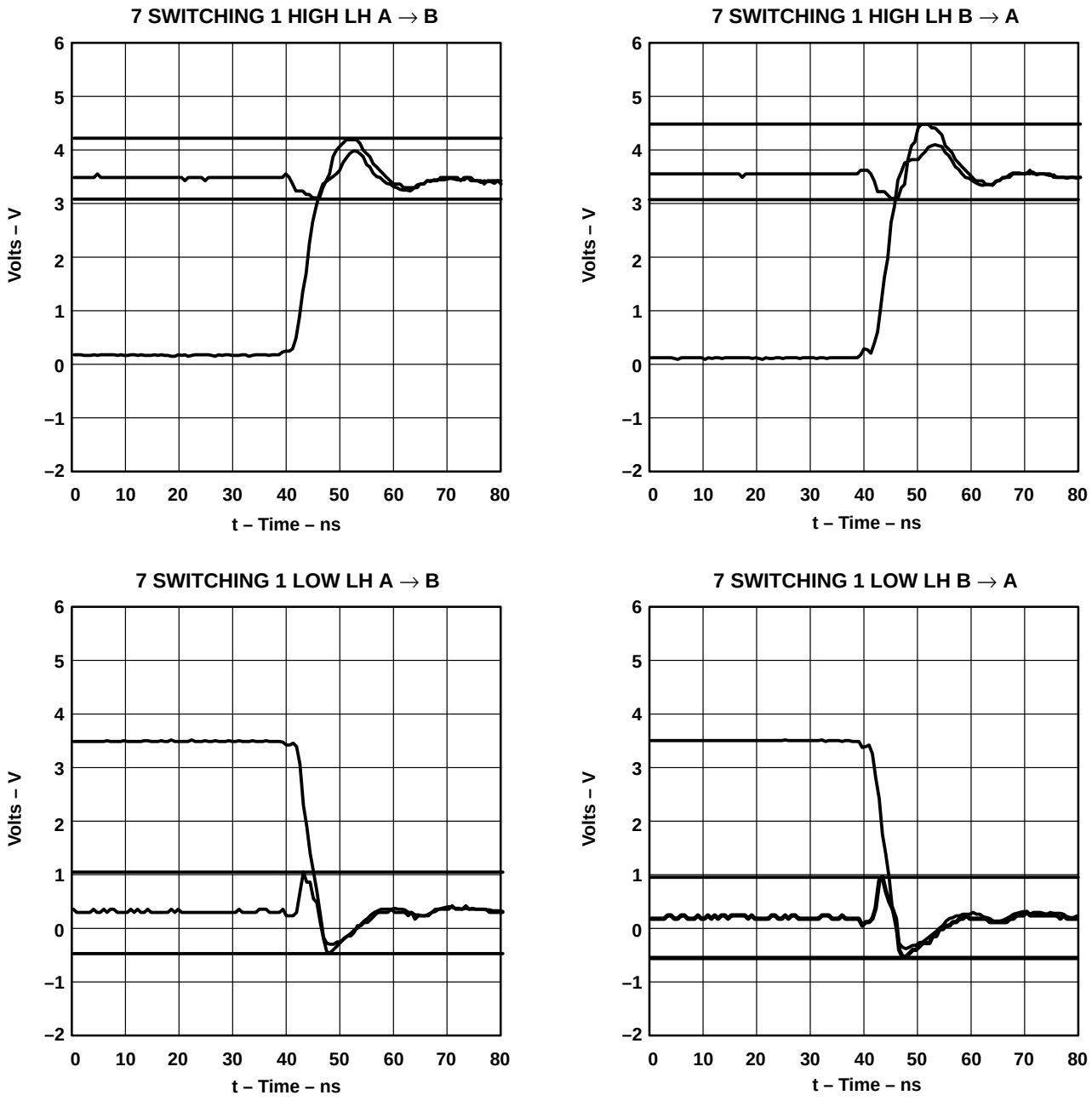
PROPAGATION DELAY TIME
vs
INPUT EDGE
A TO B



PROPAGATION DELAY TIME
vs
INPUT EDGE
A TO B



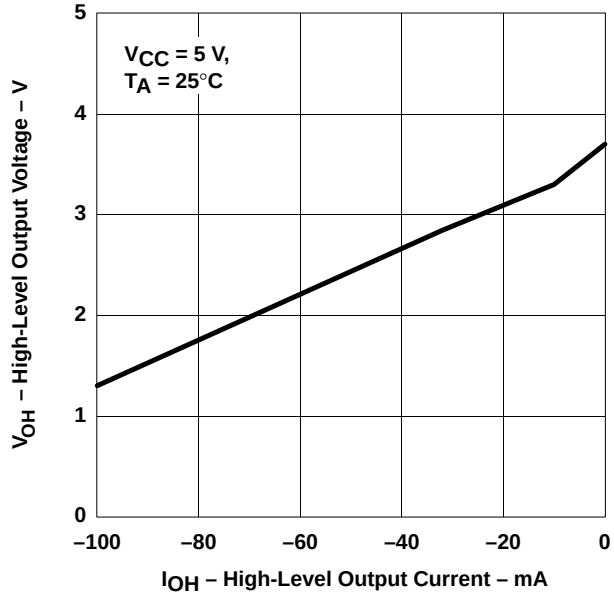
V_{OHV} and V_{OLP}



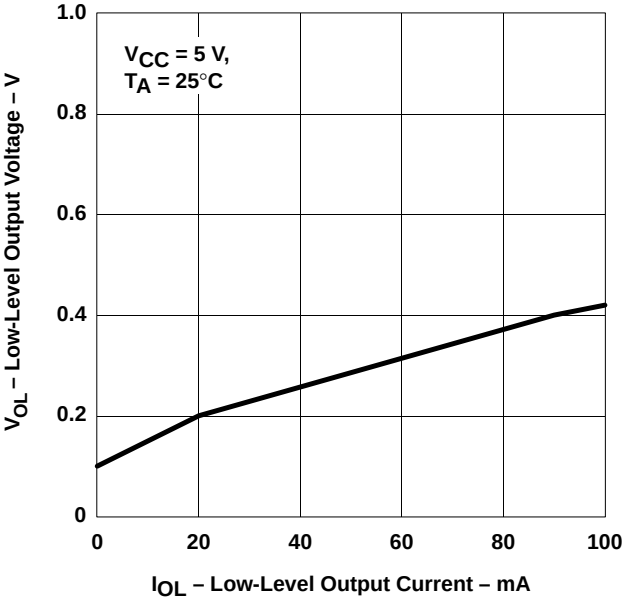
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

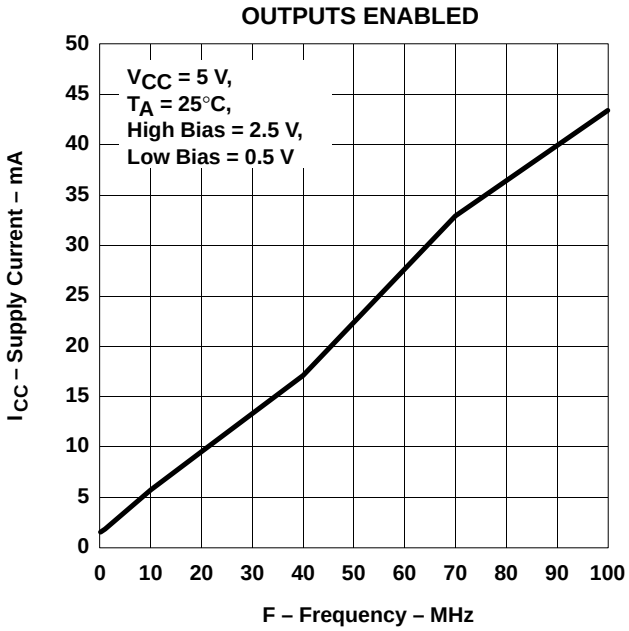
HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

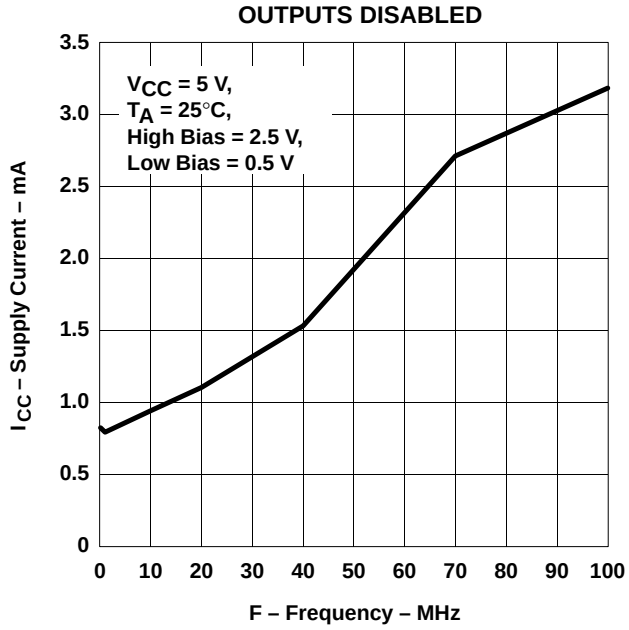


LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT



Supply Current vs Frequency



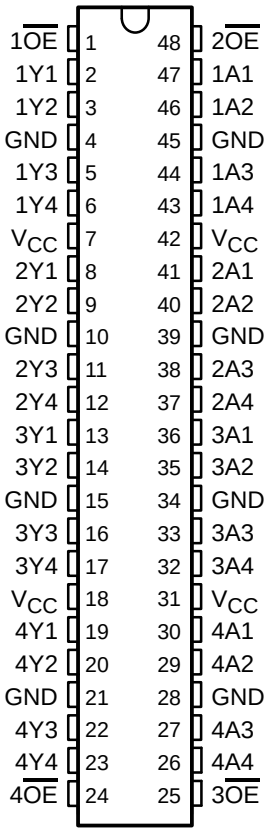


APPENDIX B
SN54ABT16244, SN74ABT16244A

B

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16244 . . . WD PACKAGE
SN74ABT16244A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The SN54ABT16244 and SN74ABT16244A are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16244A is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

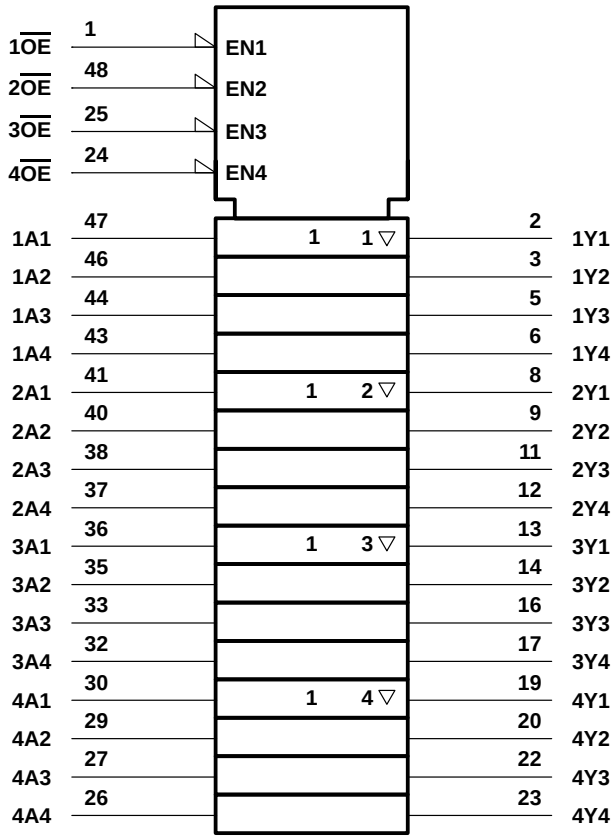
The SN54ABT16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16244A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

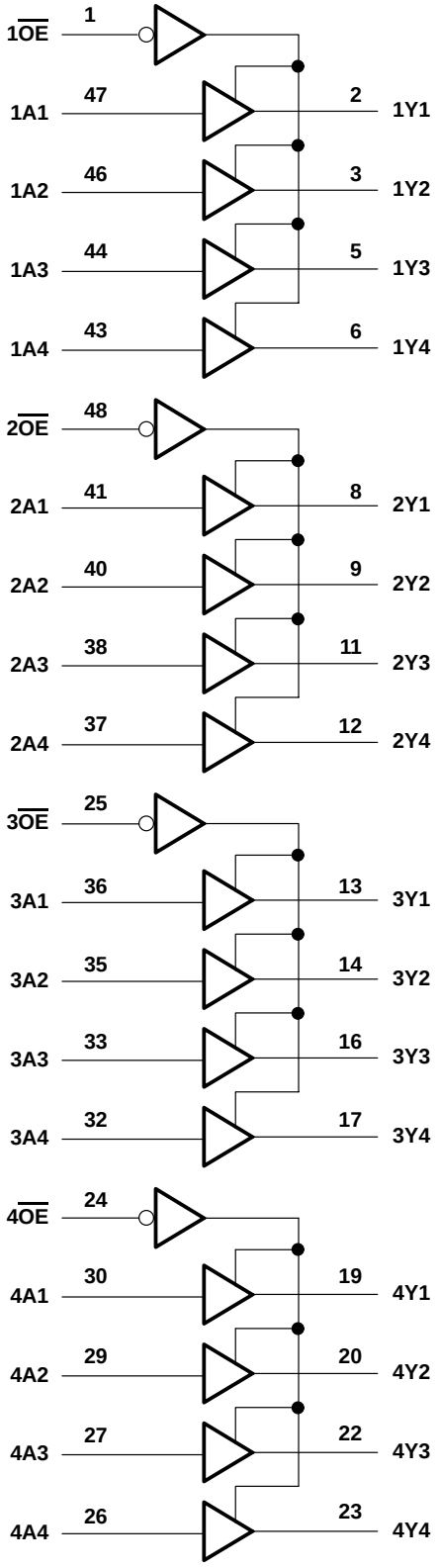
Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16244 . . . . . 96 mA
SN74ABT16244A . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package . . . . . 0.85 W
DL package . . . . . 1.2 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			SN54ABT16244		SN74ABT16244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C†			SN54ABT16244		SN74ABT16244A		UNIT
				MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V	I_{OH} = – 24 mA		2			2				
		I_{OH} = – 32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				10§		10		10§	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–10§		–10		–10§	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			3		2		3	mA
			Outputs low			32		32		32	
			Outputs disabled			3		2		3	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			0.05		1.5		0.05	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				0.05		1.5		0.05	
C_i	V_I = 2.5 V or 0.5 V				3						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

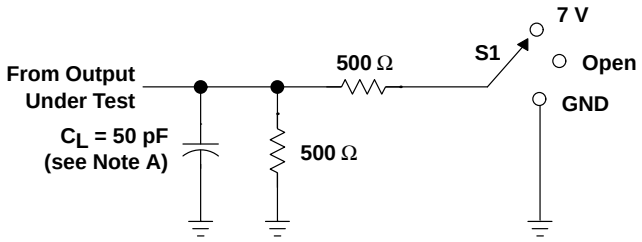
* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† Characteristics for TA = 25°C apply to the SN74ABT16244A only.
‡ All typical values are at V_{CC} = 5 V.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C†			SN54ABT16244		SN74ABT16244A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.3	3.2	0.7	3.7	1	3.5	ns
t_{PHL}			1	2.6	3.7	0.5	4.3	1	4.1	
t_{PZH}	$\overline{OE}$	Y	1	3	3.8	0.7	5	1	4.8	ns
t_{PZL}			1	3.2	4	0.9	5	1	4.8	
t_{PHZ}	$\overline{OE}$	Y	1	3.6	4.4	1	5	1	4.8	ns
t_{PLZ}			1	2.9	3.7	1	4.3	1	4.1	

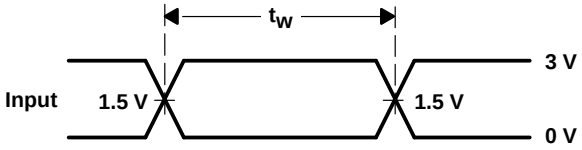
† Characteristics for TA = 25°C apply to the SN74ABT16244A only.

PARAMETER MEASUREMENT INFORMATION

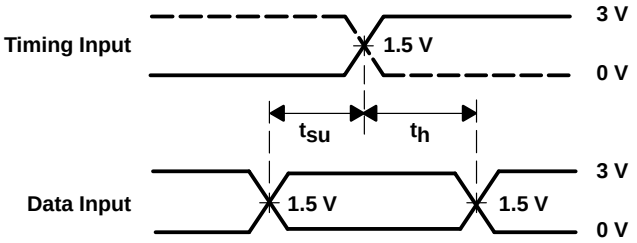


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

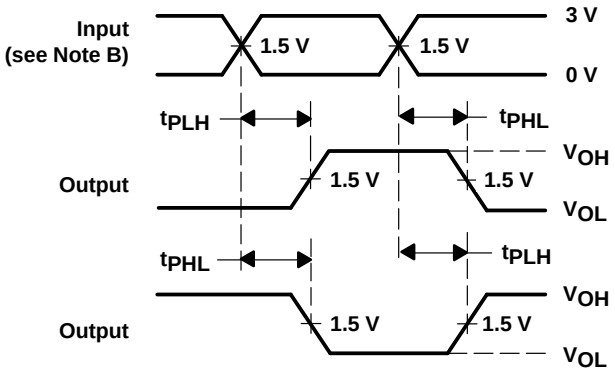
LOAD CIRCUIT FOR OUTPUTS



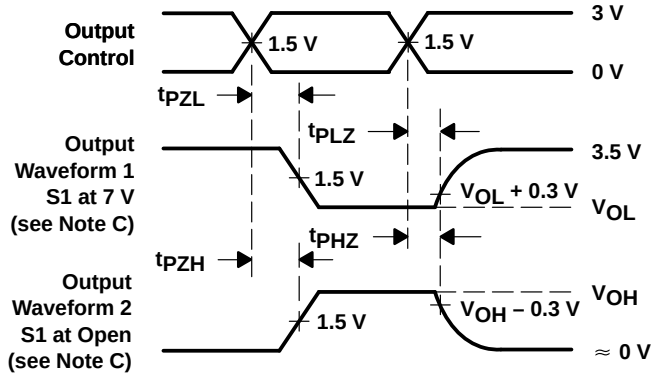
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



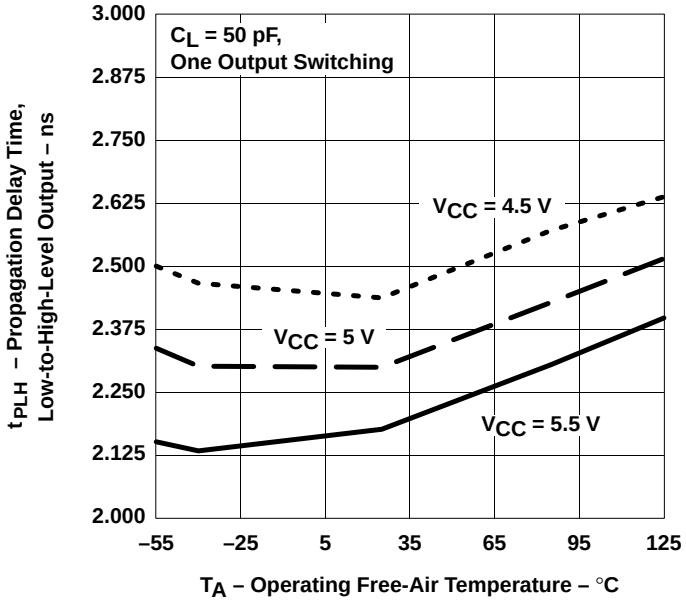
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

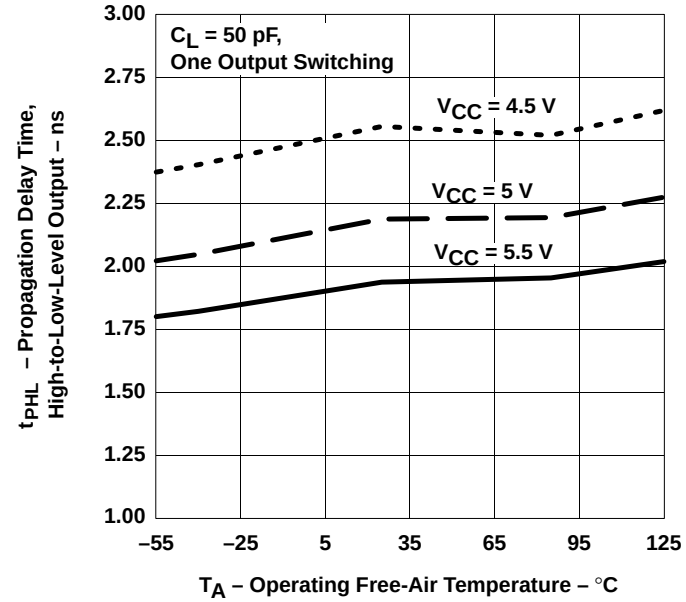
Figure 1. Load Circuit and Voltage Waveforms

Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO Y

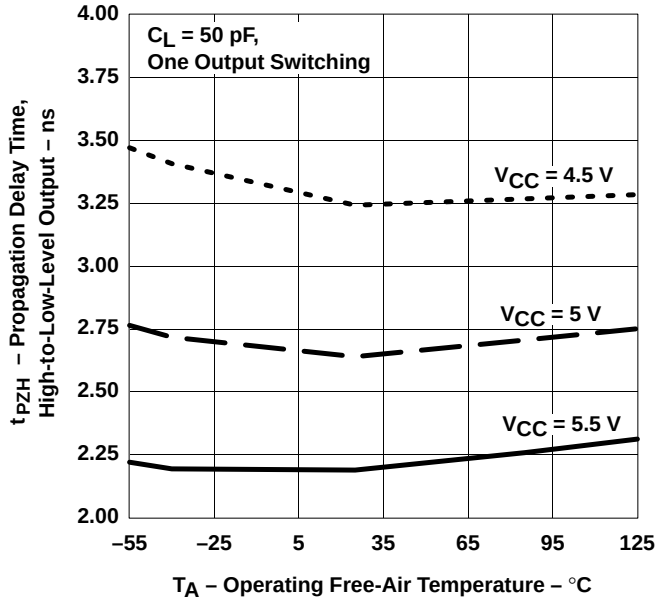


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO Y

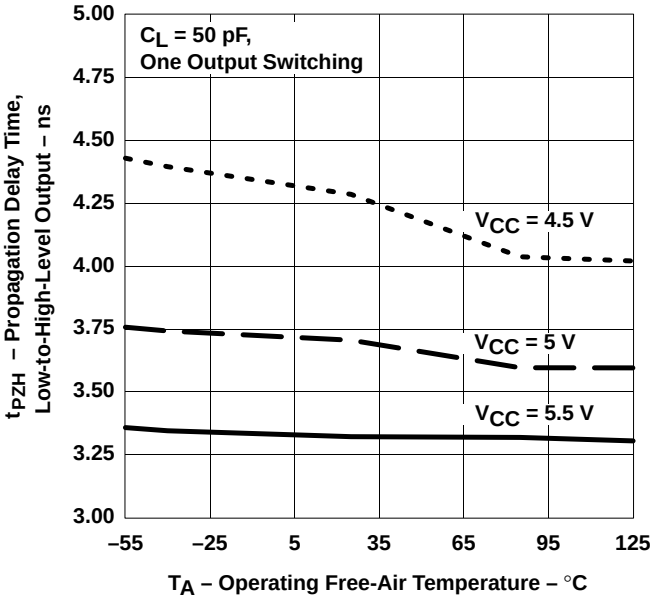


Propagation Delay Time vs Temperature

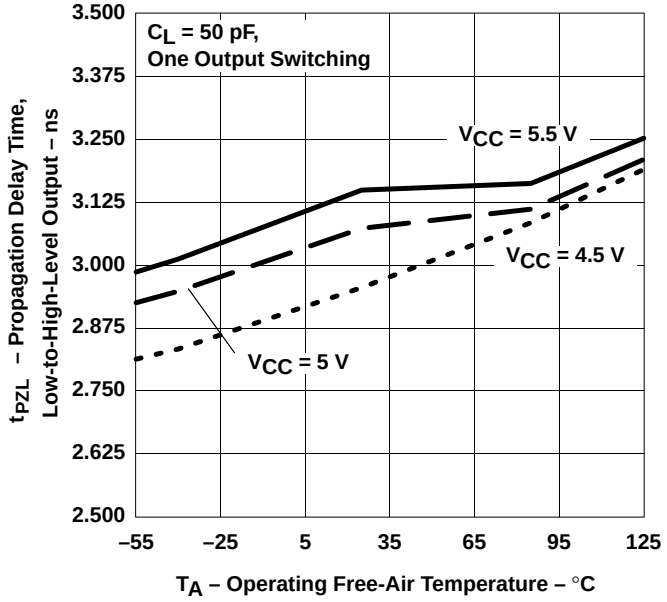
PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO Y



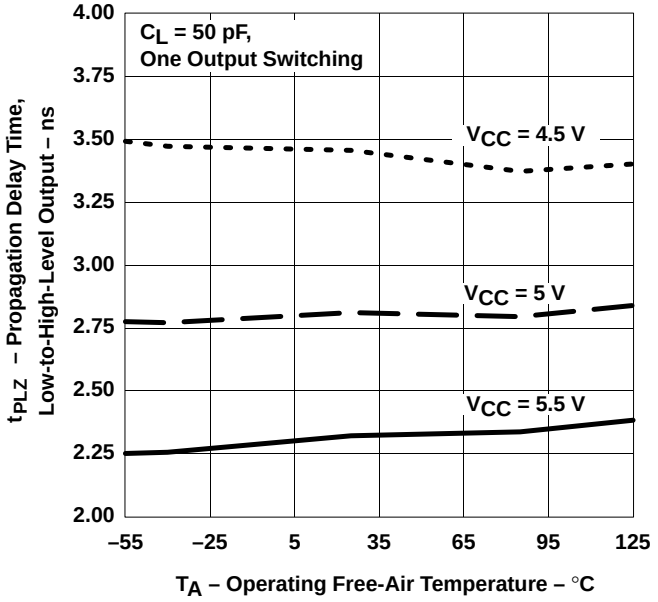
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TOY



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO Y

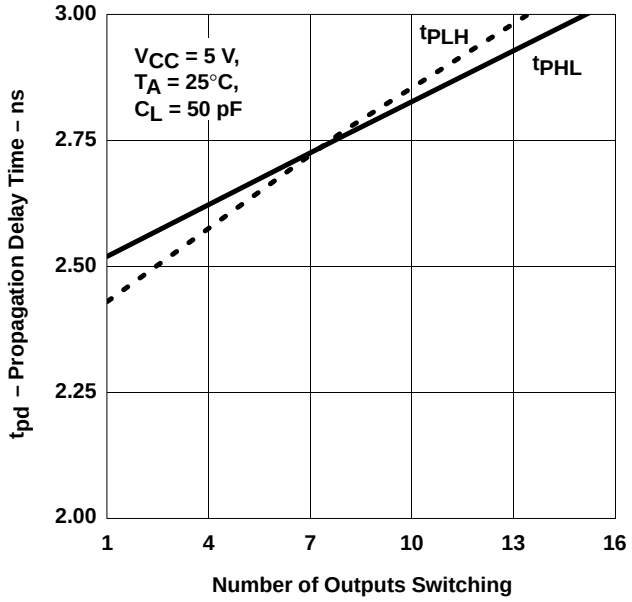


PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO Y

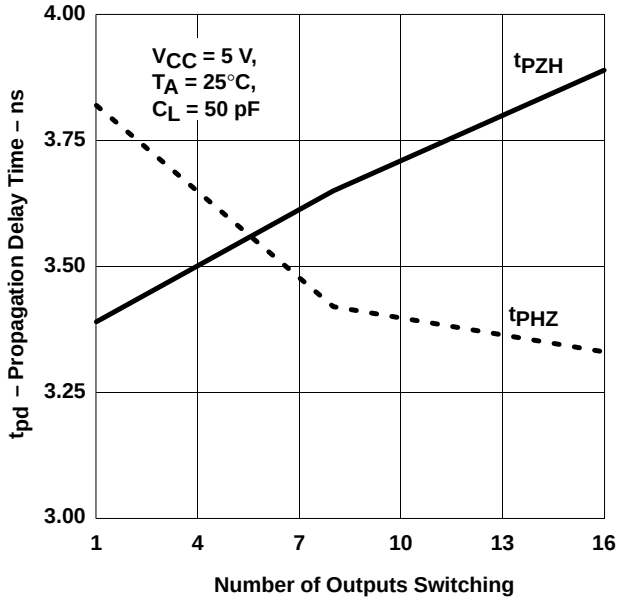


Propagation Delay Time vs Number of Outputs Switching

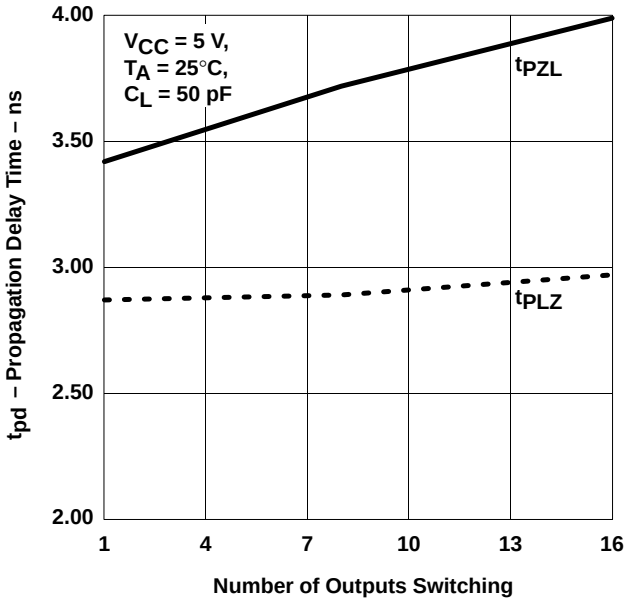
PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A TO Y



PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
$\overline{OE}$ TO Y

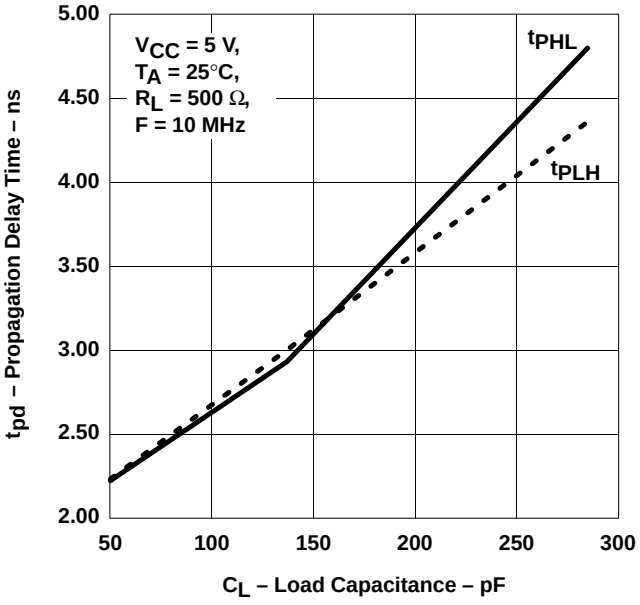


PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
$\overline{OE}$ TO Y

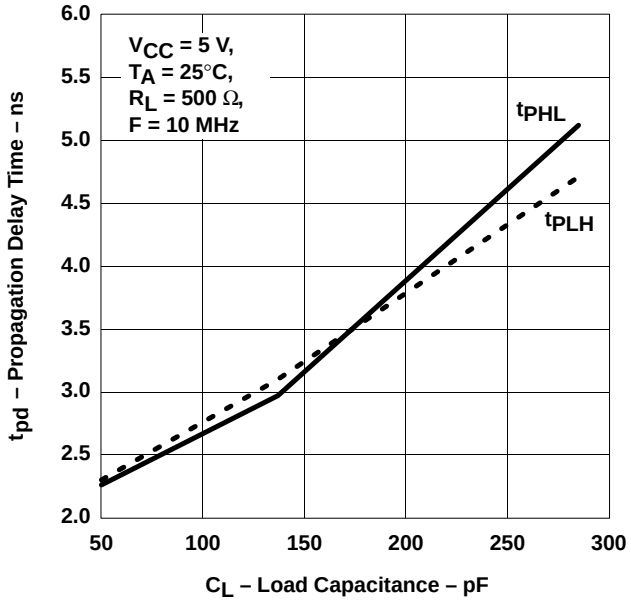


Propagation Delay Time vs Load Capacitance

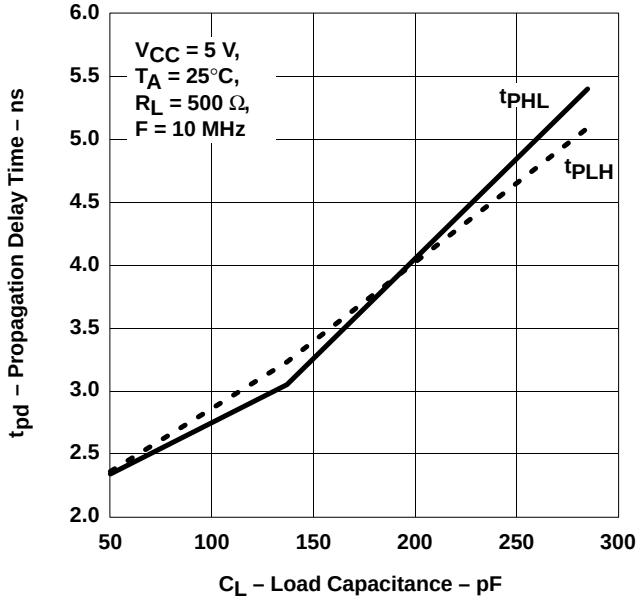
A TO Y
ONE OUTPUT SWITCHING



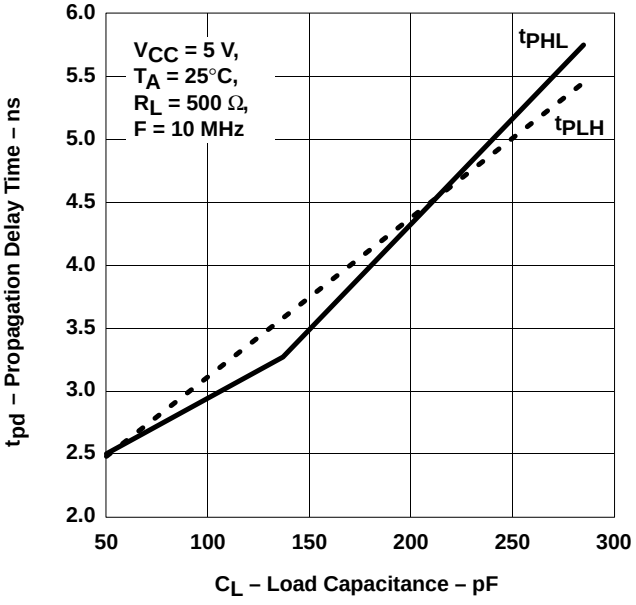
A TO Y
FOUR OUTPUTS SWITCHING



A TO Y
EIGHT OUTPUTS SWITCHING

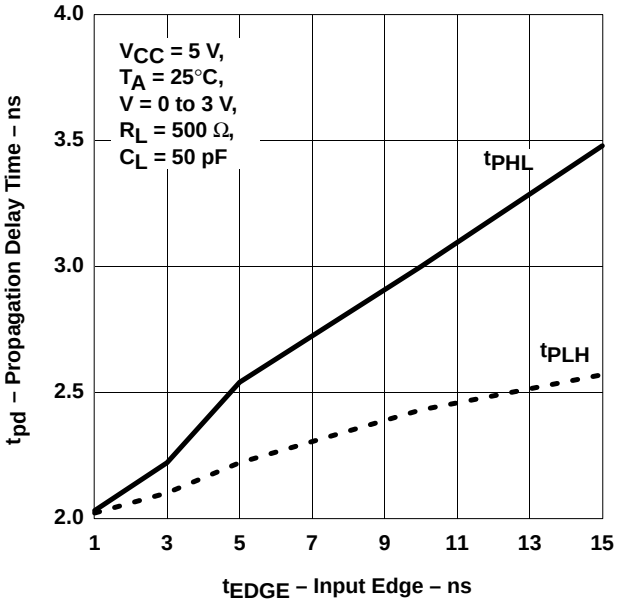


A TO Y
16 OUTPUTS SWITCHING

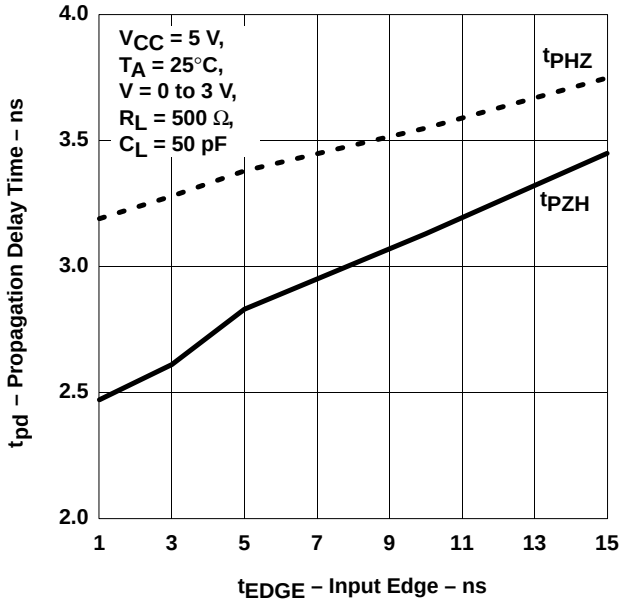


Propagation Delay Time vs Input Edge

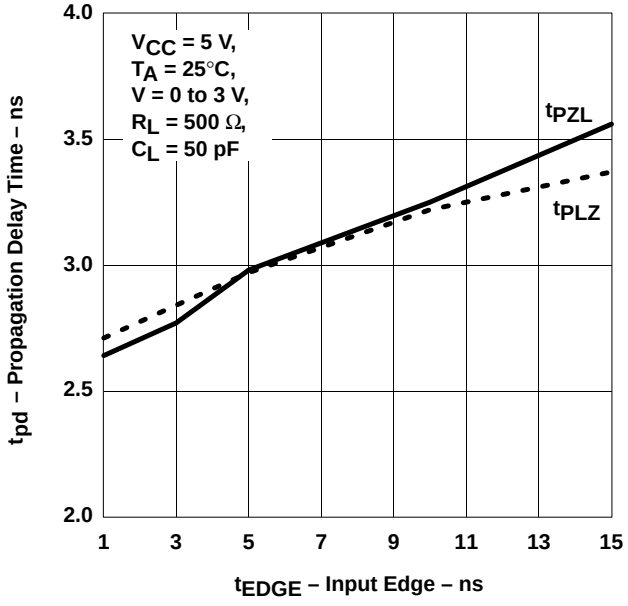
PROPAGATION DELAY TIME vs INPUT EDGE A TO Y



PROPAGATION DELAY TIME vs INPUT EDGE $\overline{OE}$ TO Y

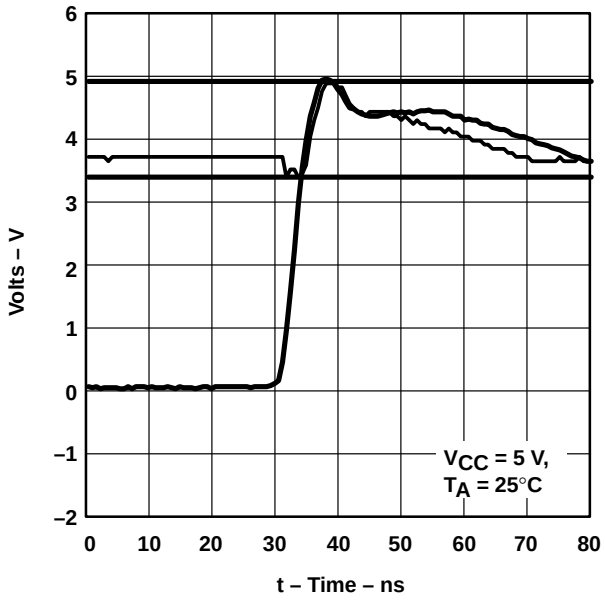


PROPAGATION DELAY TIME vs INPUT EDGE $\overline{OE}$ TO Y

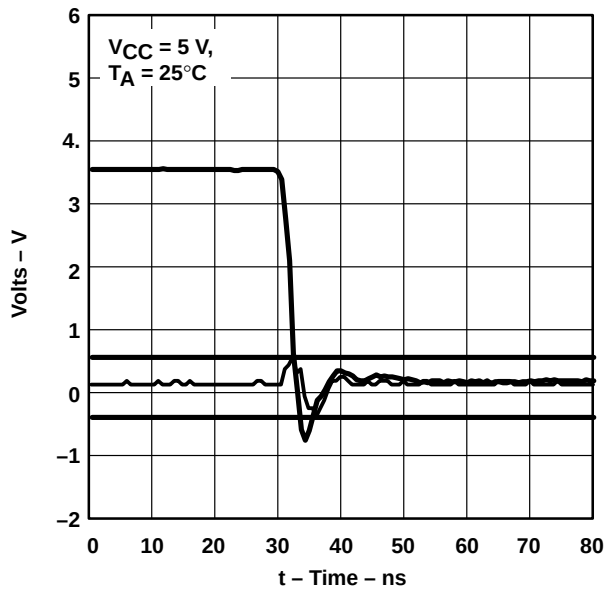


V_{OHV} and V_{OLP}

15 SWITCHING 1 HIGH LH A → Y



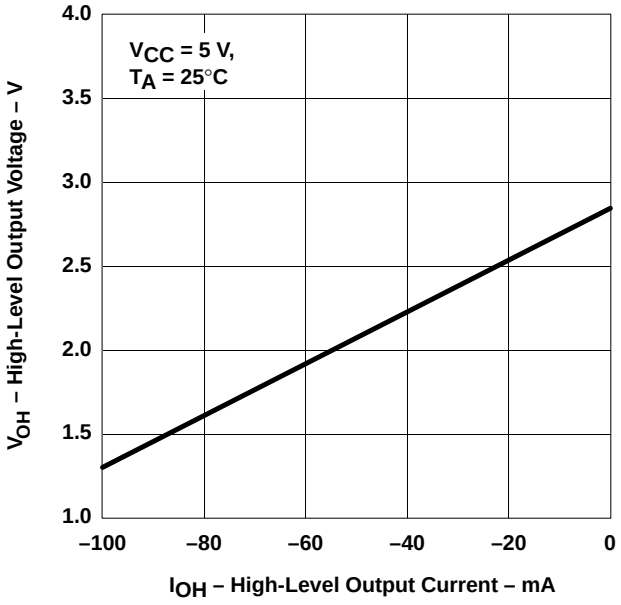
15 SWITCHING 1 LOW HL A → Y



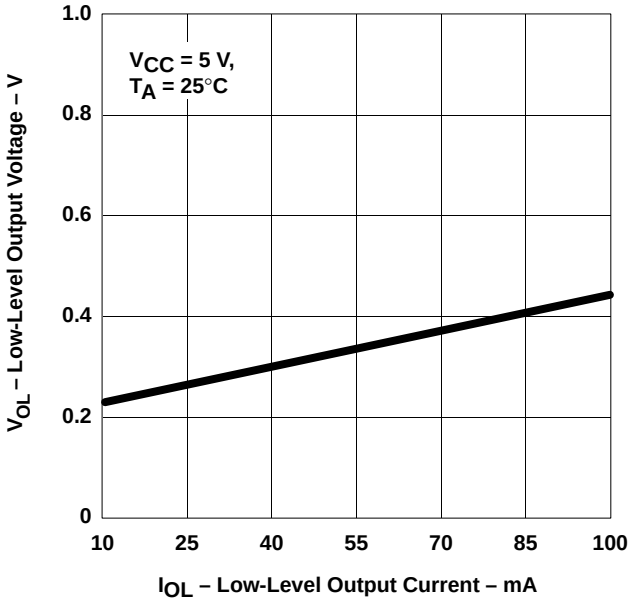
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

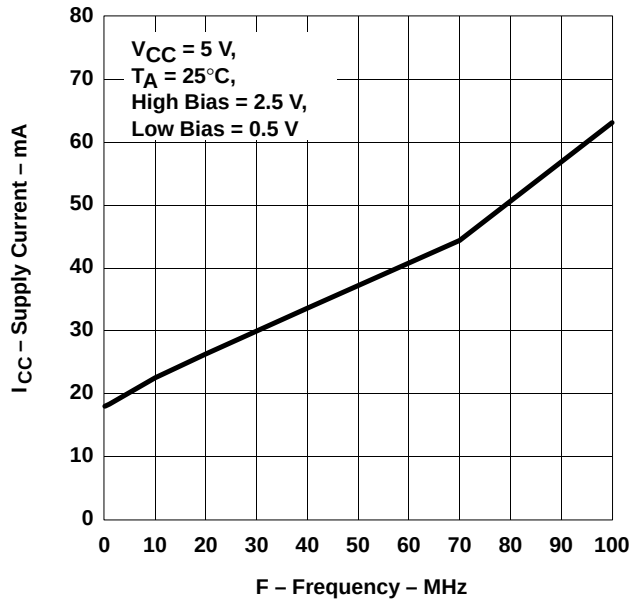


LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

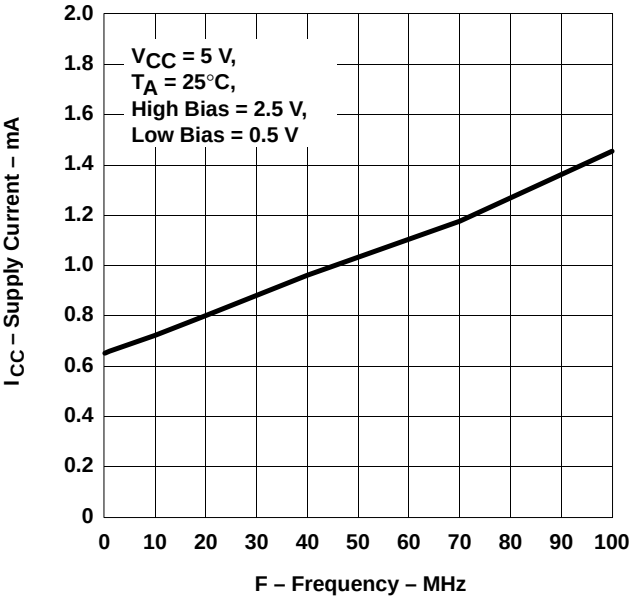


Supply Current vs Frequency

OUTPUTS ENABLED



OUTPUTS DISABLED

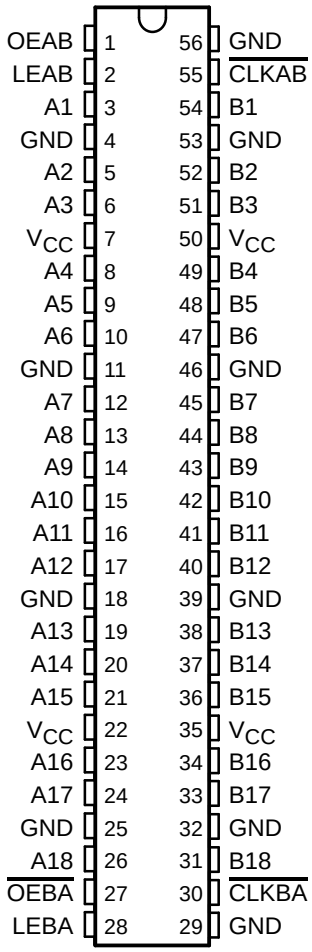


APPENDIX C
′ABT16500B

C

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16500B . . . WD PACKAGE
SN74ABT16500B . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16500B is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16500B is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT16500B is characterized for operation from −40°C to 85°C.

Widebus, EPIC-IIB, and UBT are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

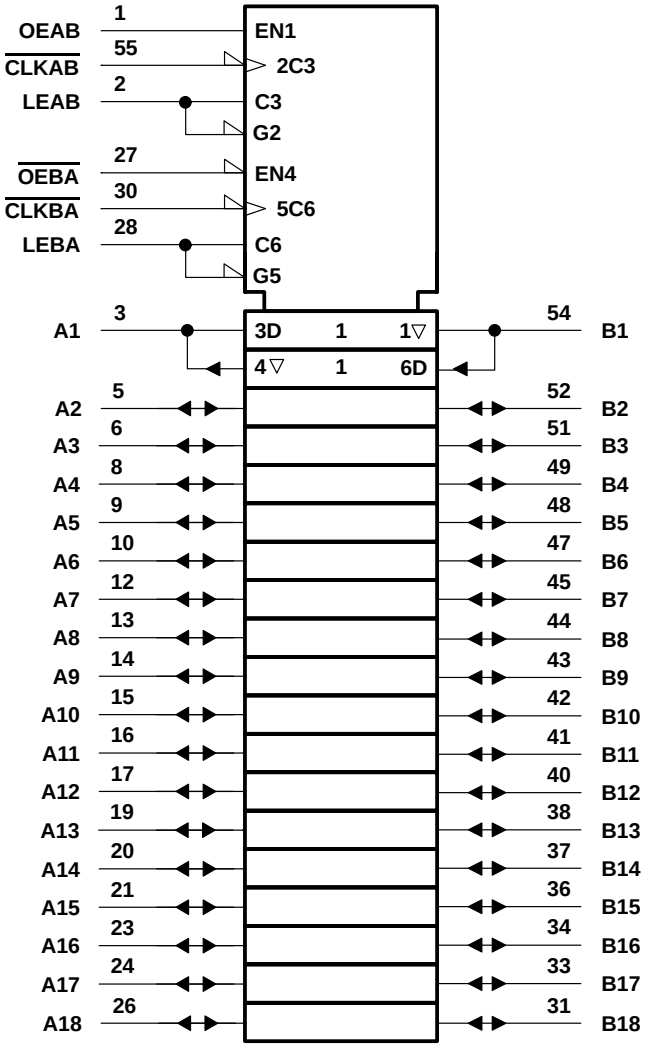
INPUTS				OUTPUT
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

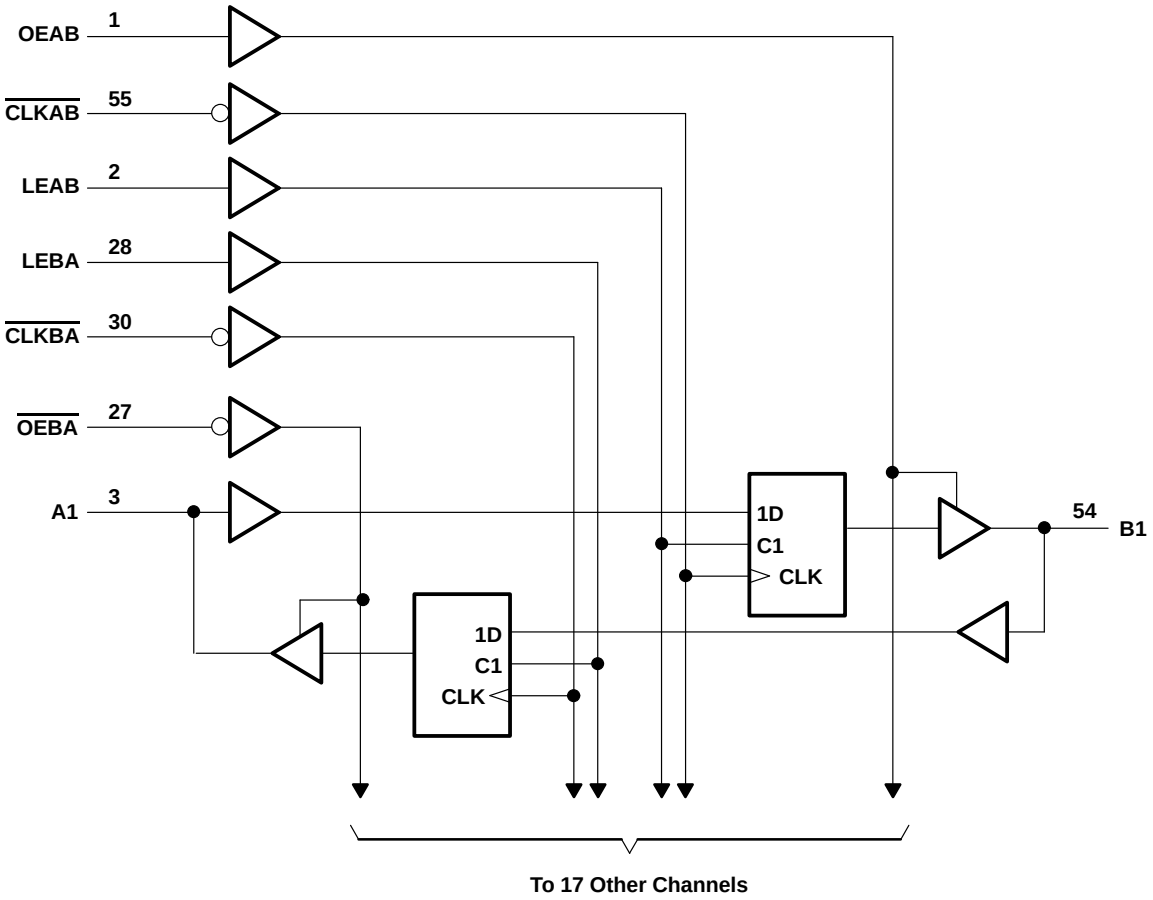
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16500B . . . . . 96 mA
SN74ABT16500B . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT16500B		SN74ABT16500B		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = – 3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = – 24 mA	2			2				
			I_{OH} = – 32 mA	2*					2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55*				0.55	
I_{off}		V_{CC} = 0,	V_I or $V_O \le$ 4.5 V			±100				±100	µA
I_{CEX}	Outputs high	V_{CC} = 5.5 V,	V_O = 5.5 V			50		50		50	µA
I_I	Control inputs	V_{CC} = 0 to 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
	A or B ports	V_{CC} = 2.1 V to 5.5 V, V_I = V_{CC} or GND				±20		±20		±20	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA
I_{OZPU}		V_{CC} = 0 to 2.1 V, V_O = 0.5 to 2.7 V, $\overline{OE}$ or OE= X				±50		±50		±50	µA
I_{OZPD}		V_{CC} = 2.1 V to 0, V_O = 0.5 to 2.7 V, $\overline{OE}$ or OE= X				±50		±50		±50	µA
I_{OZH}§		V_{CC} = 2.1 V to 5.5 V, V_O = 2.7 V, OE ≤ 0.8 V¶	$\overline{OE}$ ≥ 2 V,			10		10		10	µA
I_{OZL}§		V_{CC} = 2.1 V to 5.5 V, V_O = 0.5 V, OE ≤ 0.8 V¶	$\overline{OE}$ ≥ 2 V,			–10		–10		–10	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}#		V_{CC} = 5.5V, Other inputs at V_{CC} or GND	One input at 3.4 V,			50		50		50	µA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9						pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ For V_{CC} between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

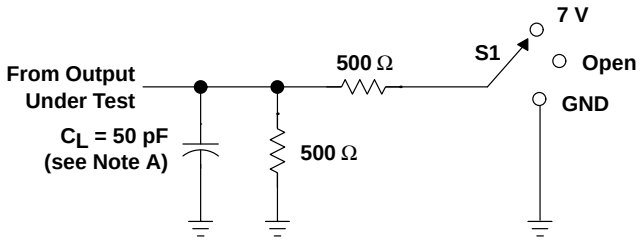
				SN54ABT16500B		SN74ABT16500B		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w†	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low		3		3		
t_{su}	Setup time	A before $\overline{CLKAB}$↓		3		3		ns
		B before $\overline{CLKBA}$↓		3		3		
		A before LEAB↓ or B before LEBA↓	$\overline{CLK}$ high	1		1		
			$\overline{CLK}$ low	2.5		2.5		
t_h	Hold time	A after $\overline{CLKAB}$↓ or B after $\overline{CLKBA}$↓		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		

† This parameter is specified by design but not tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

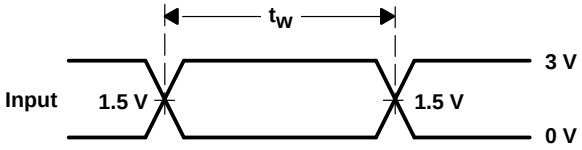
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	A or B	B or A	1	2.5	3.6	1	4.2	1	4	ns
t_{PHL}			1	3.2	4.5	1	5.1	1	4.9	
t_{PLH}	LEAB or LEBA	B or A	1	3.2	4.5	1	5.6	1	5	ns
t_{PHL}			1	3.4	4.5	1	5.4	1	5	
t_{PLH}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A	1	3.5	4.7	1	5.4	1	5.3	ns
t_{PHL}			1	3.5	4.7	1	5.4	1	5.3	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A	1	3.4	4.6	1	5.3	1	5.1	ns
t_{PZL}			1.5	3.8	4.7	1.5	5.6	1.5	5.4	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A	1.5	4.5	5.7	1.5	6.9	1.5	6.5	ns
t_{PLZ}			1.4	3.4	4.7	1.4	5.8	1.4	5.4	

PARAMETER MEASUREMENT INFORMATION

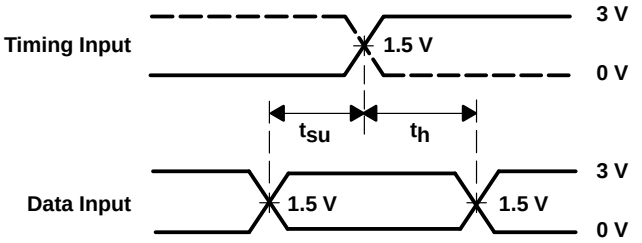


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

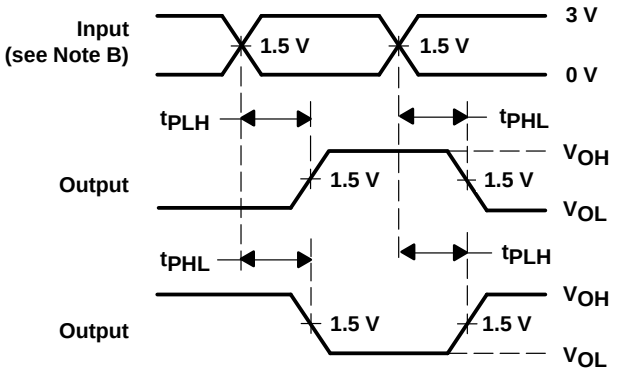
LOAD CIRCUIT FOR OUTPUTS



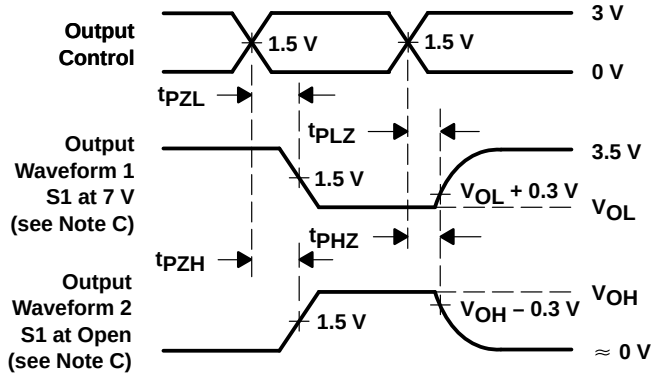
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



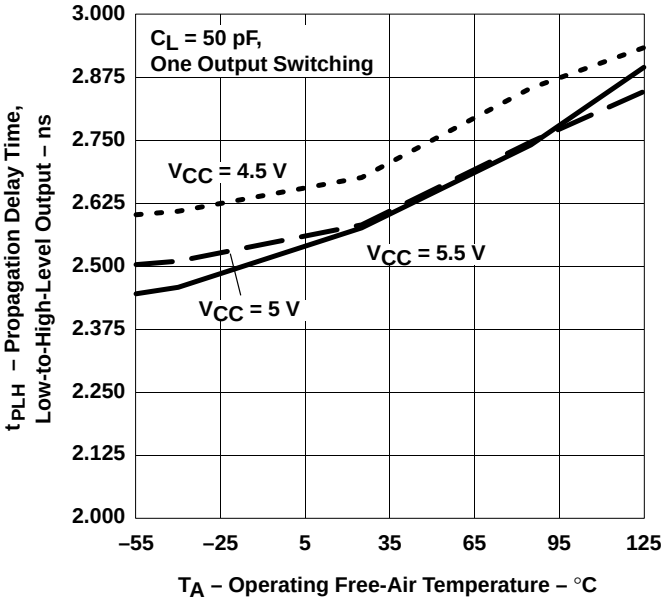
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

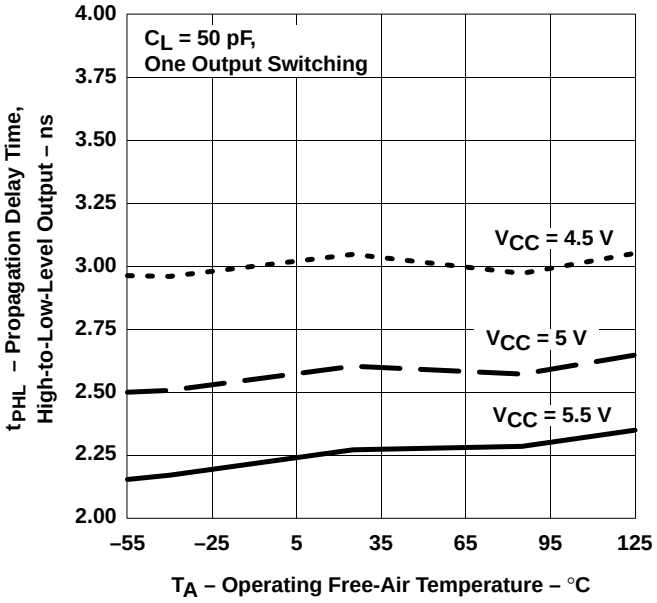
Figure 1. Load Circuit and Voltage Waveforms

Propagation Delay Time vs Temperature

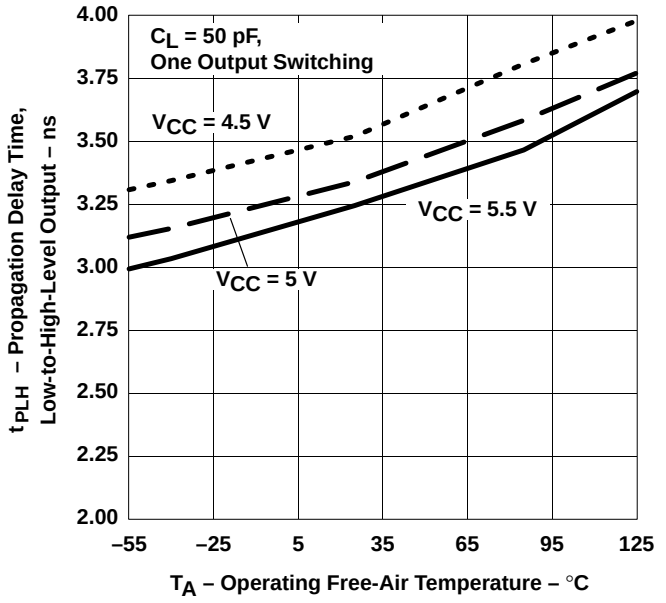
**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



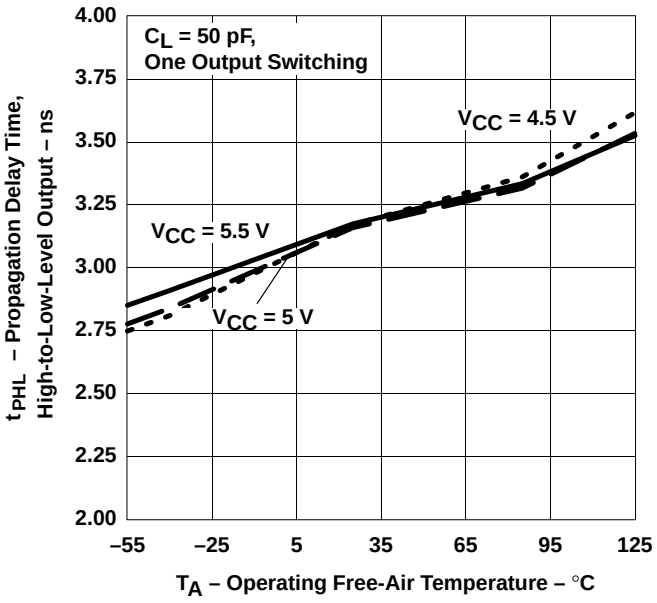
**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
LEAB TO B**

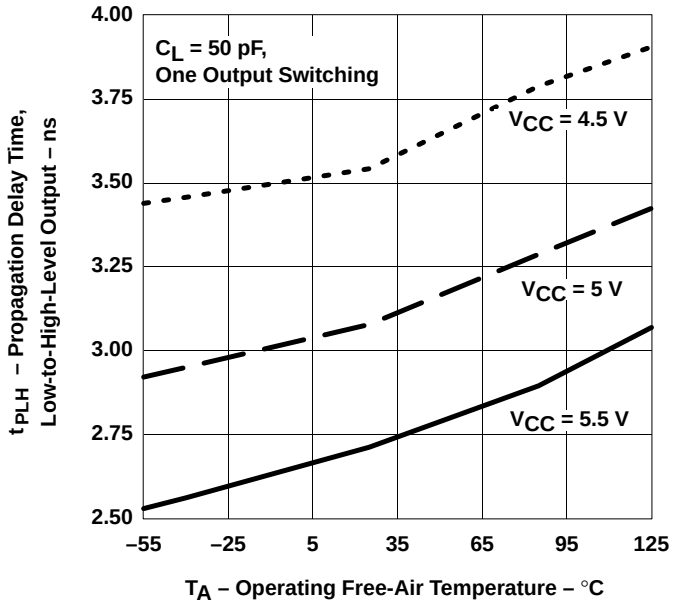


**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
LEAB TO B**

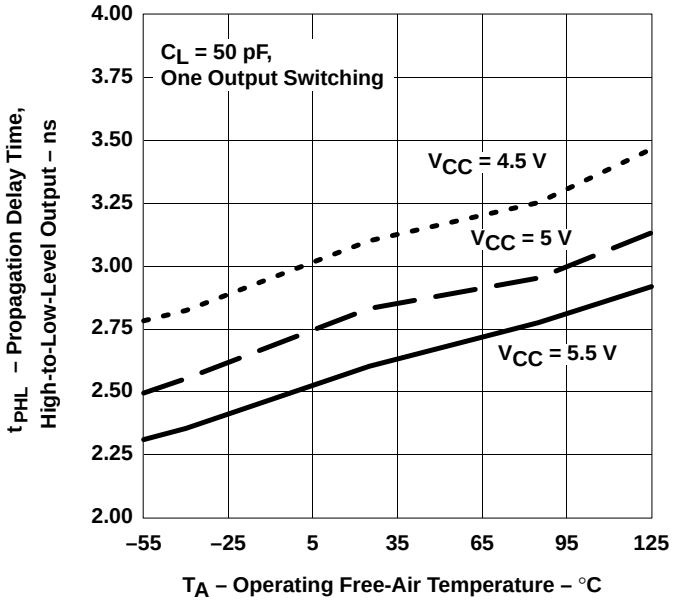


Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{\text{CLKAB}}$ TO B

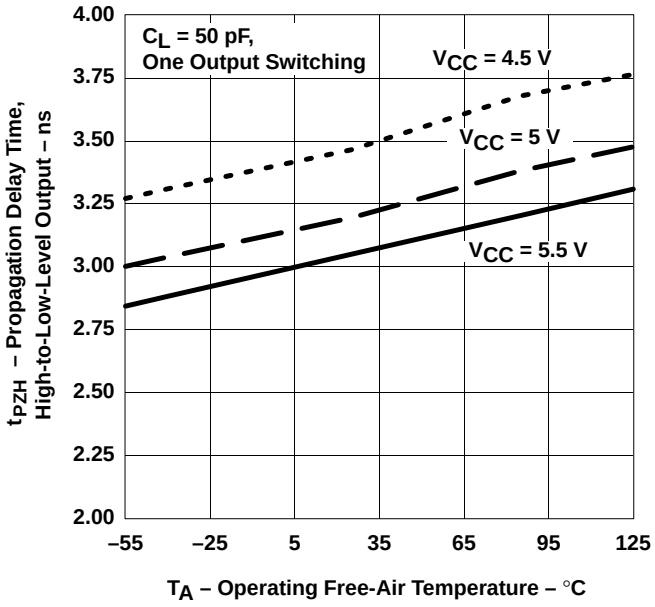


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{\text{CLKAB}}$ TO B

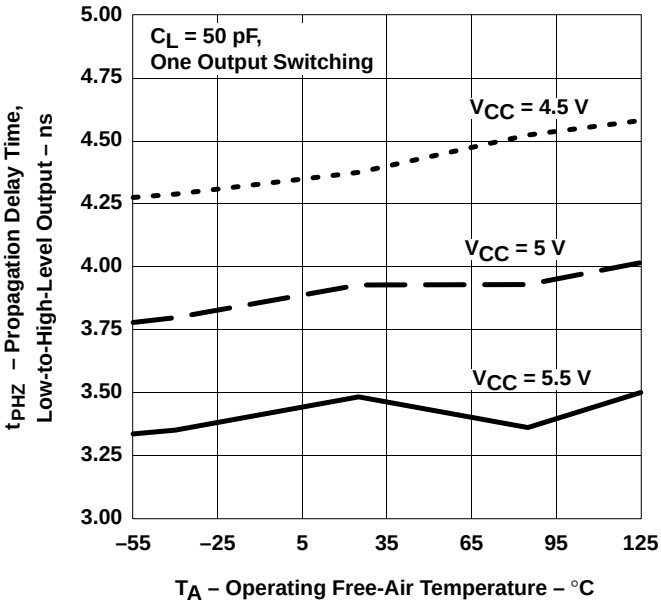


Propagation Delay Time vs Temperature

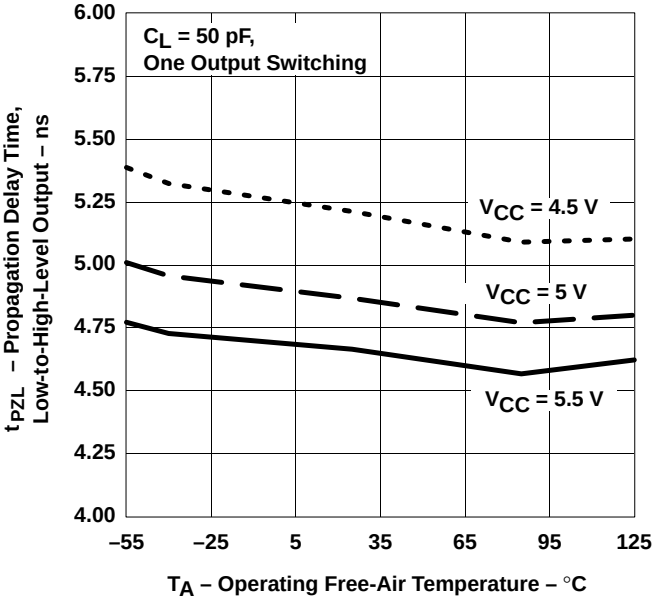
**PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**



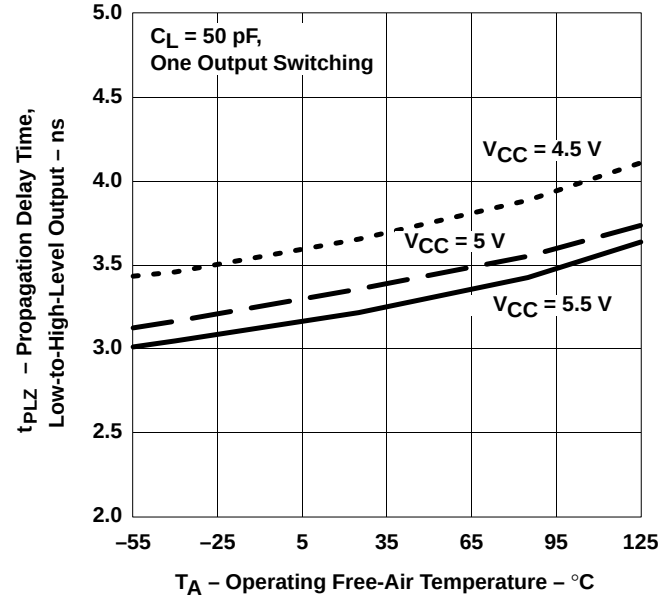
**PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**



**PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**

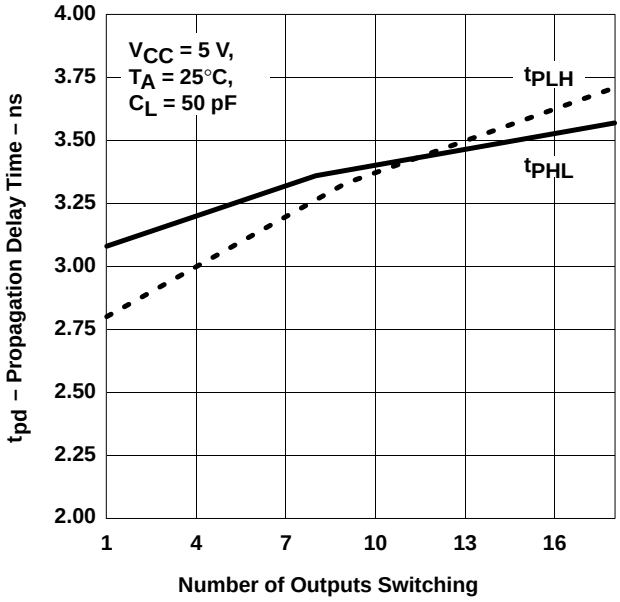


**PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**

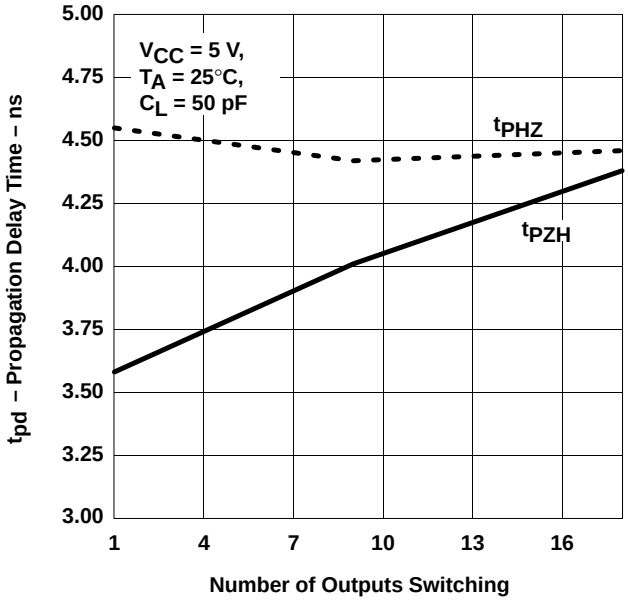


Propagation Delay Time vs Number of Outputs Switching

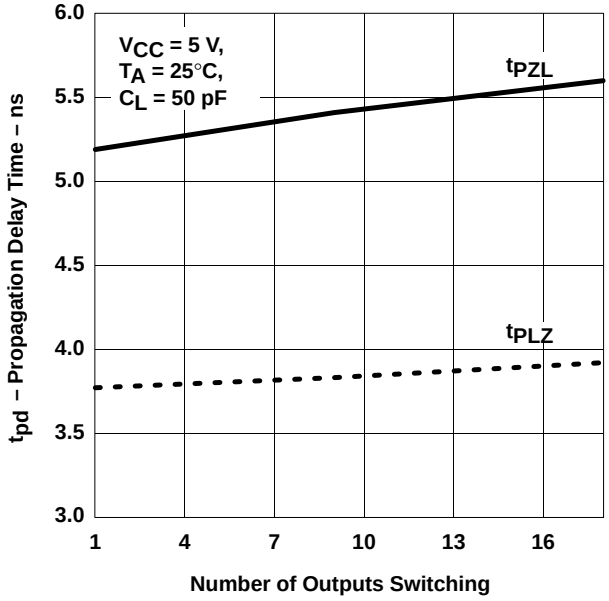
PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A TO B



PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
OEAB TO B

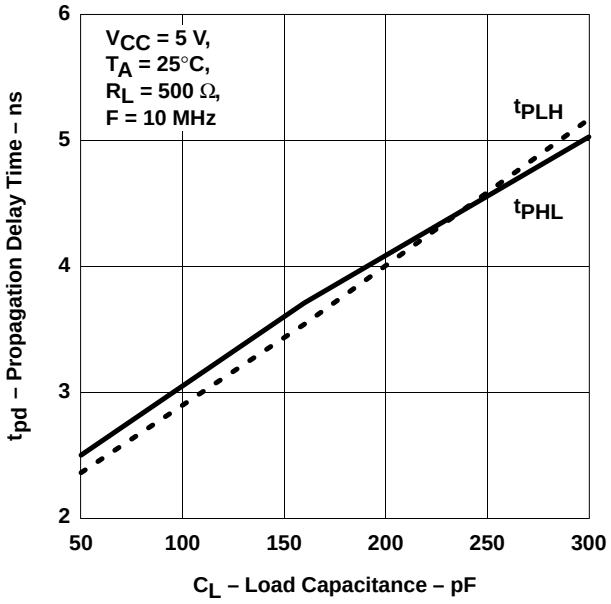


PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
OEAB TO B

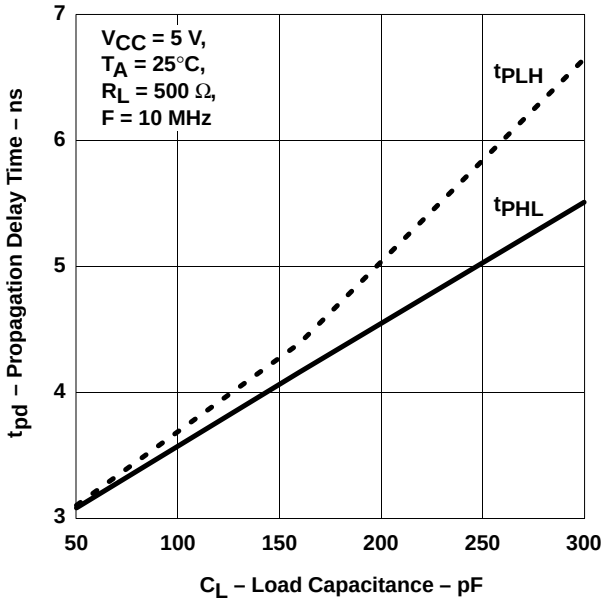


Propagation Delay Time vs Load Capacitance

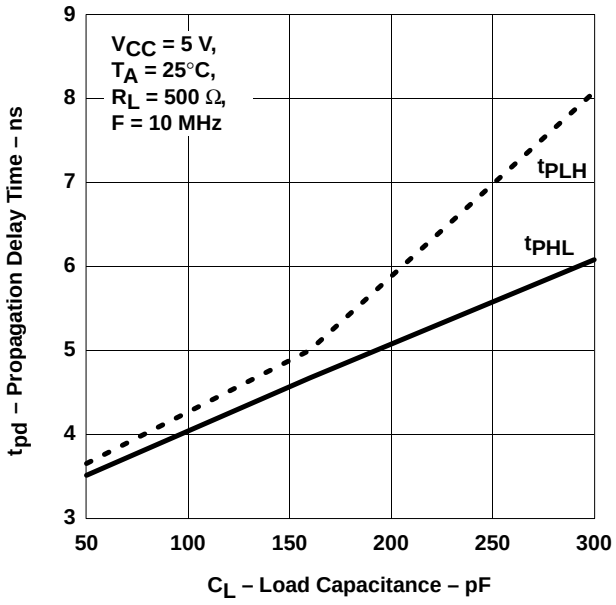
A TO B
ONE OUTPUT SWITCHING



A TO B
NINE OUTPUTS SWITCHING

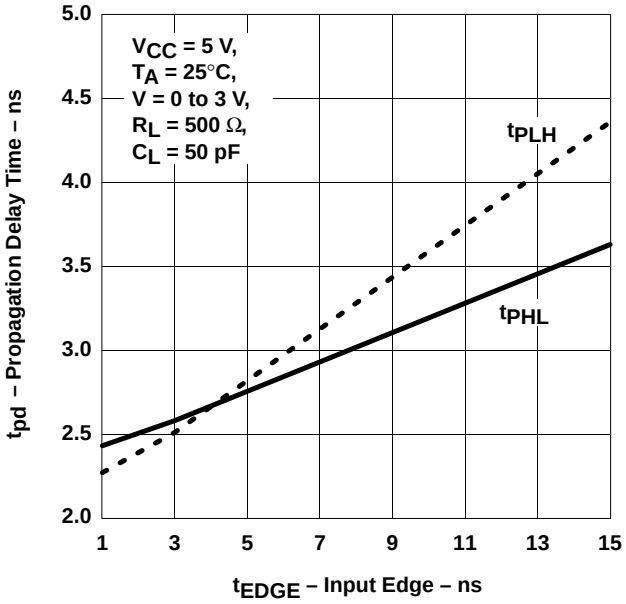


A TO B
18 OUTPUTS SWITCHING

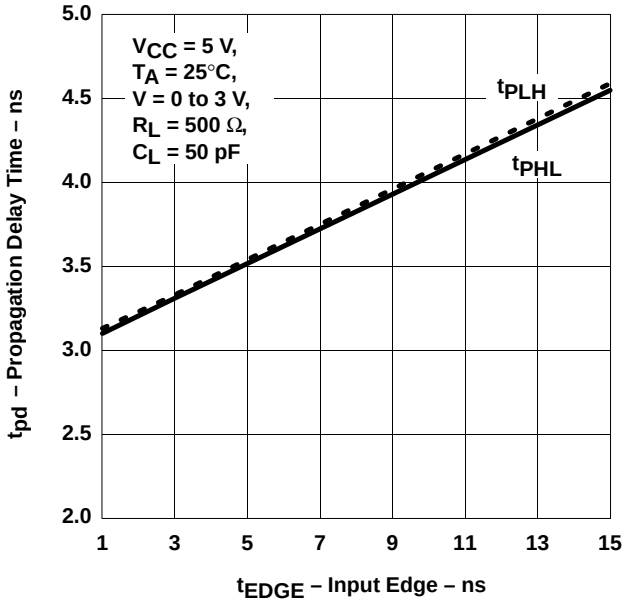


Propagation Delay Time vs Input Edge

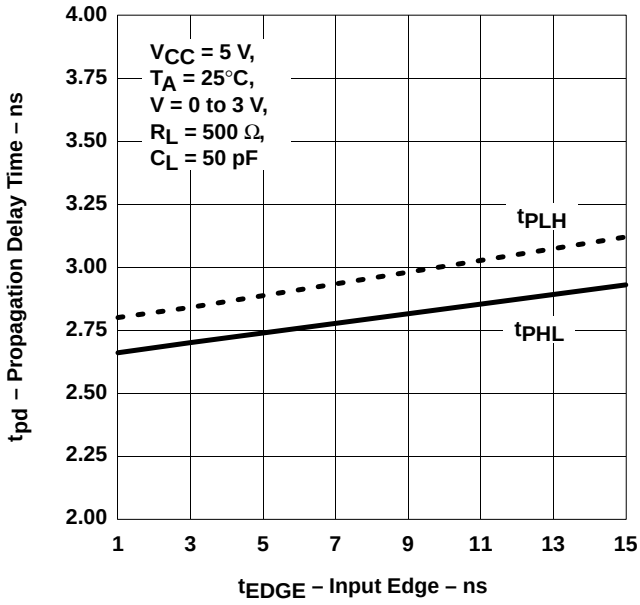
PROPAGATION DELAY TIME vs INPUT EDGE A TO B



PROPAGATION DELAY TIME vs INPUT EDGE LEAB TO B

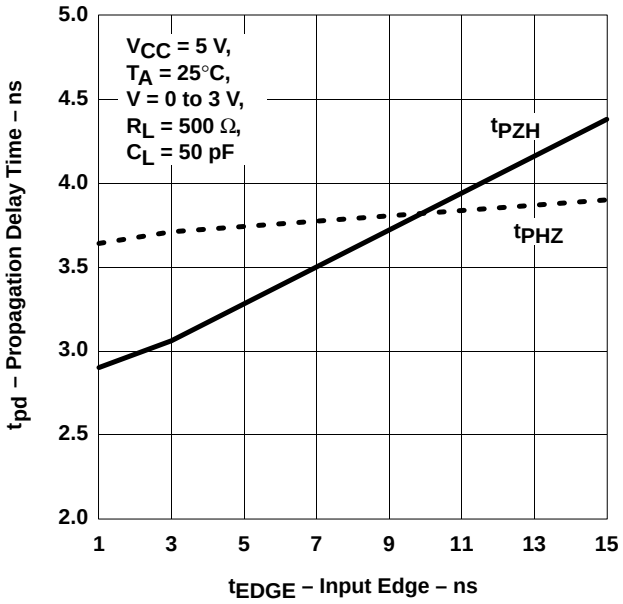


PROPAGATION DELAY TIME vs INPUT EDGE CLKAB TO B

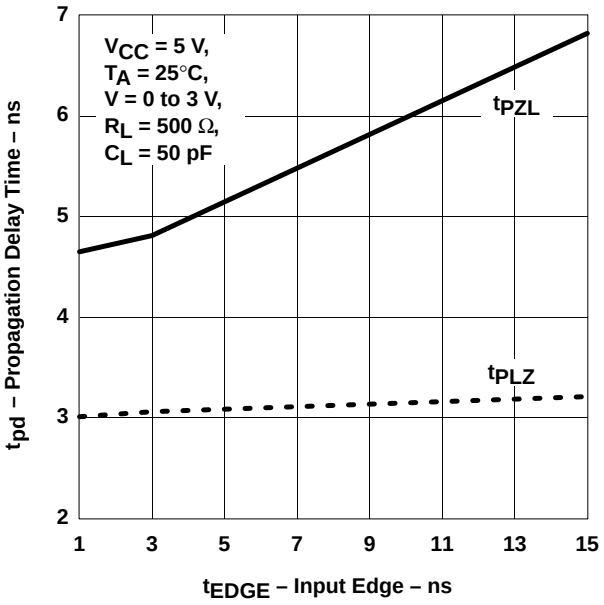


Propagation Delay Time vs Input Edge

PROPAGATION DELAY TIME
vs
INPUT EDGE
OEAB TO B

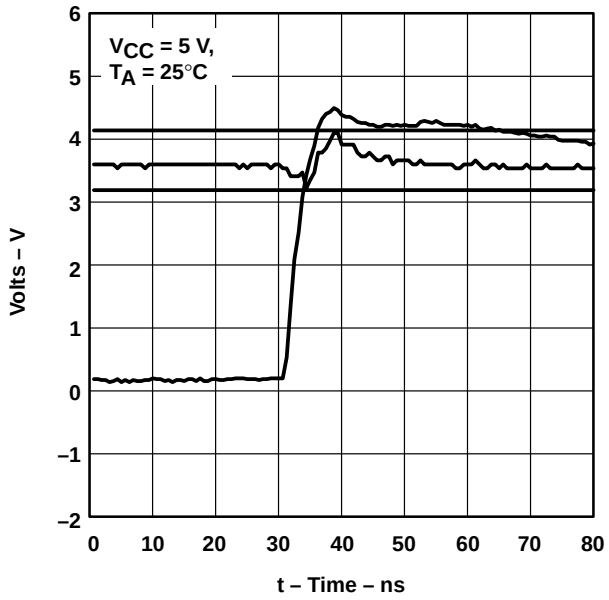


PROPAGATION DELAY TIME
vs
INPUT EDGE
OEAB TO B

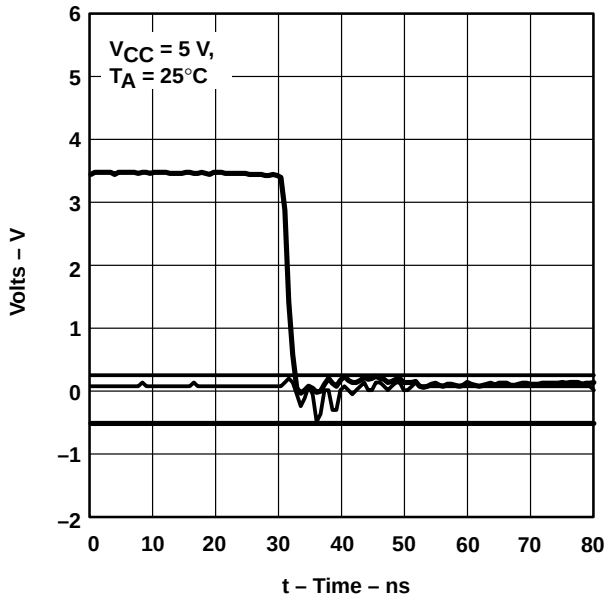


V_{OHV} and V_{OLP}

17 SWITCHING 1 HIGH LH B → A



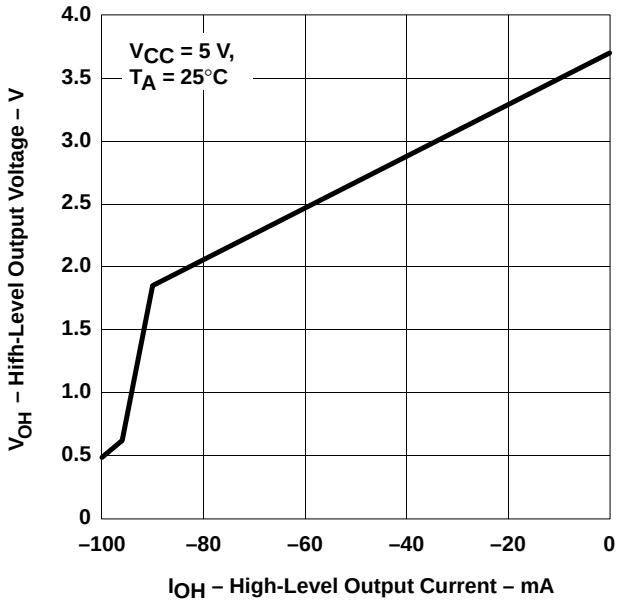
17 SWITCHING 1 LOW HL B → A



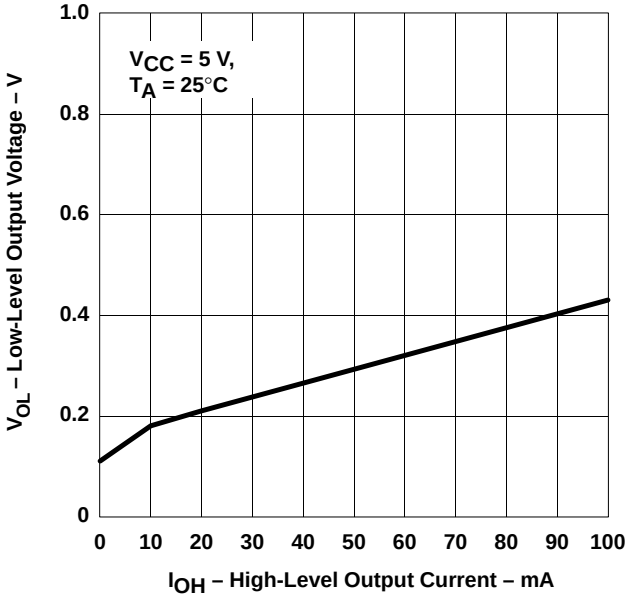
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

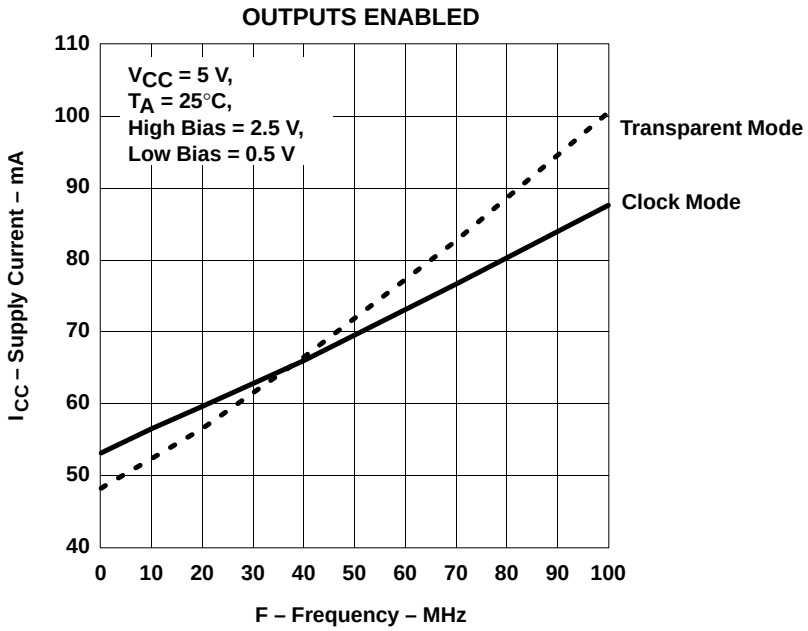
HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

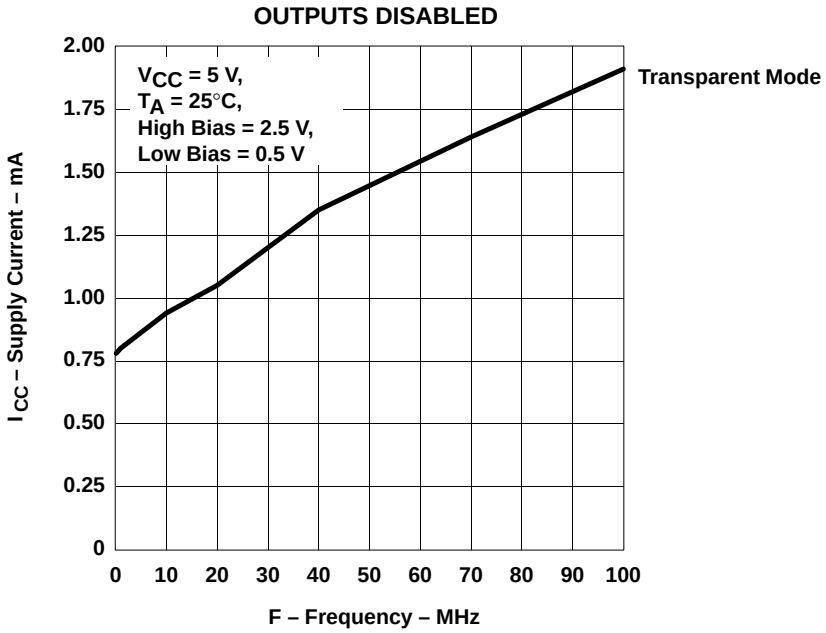


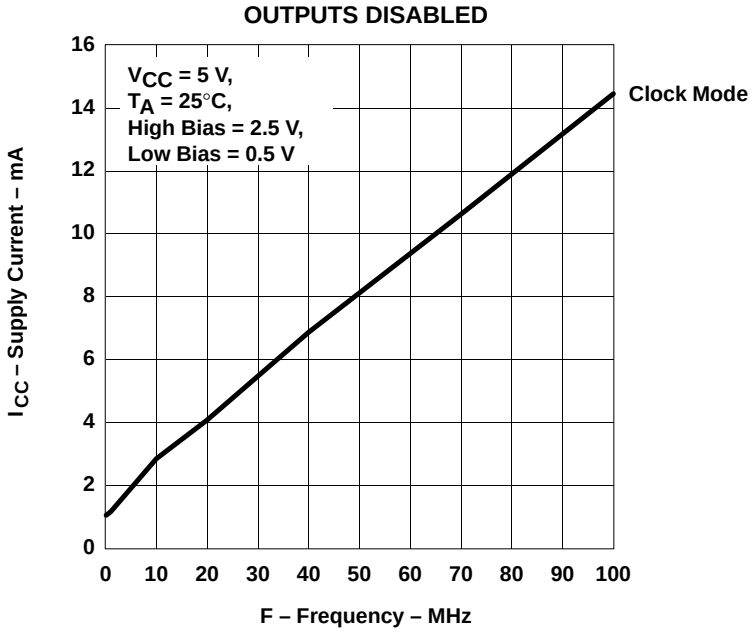
Supply Current vs Frequency



NOTE: Characteristics for latch mode are similar to those when in clock mode.

Supply Current vs Frequency





NOTE: Characteristics for latch mode are similar to those when in clock mode.

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