SN54/74HCT
CMOS Logic Family
Applications and Restrictions

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TEXAS INSTRUMENTS

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Introduction

This report describes applications, features, and system design of the SN54/74HCT high-speed CMOS family. To simplify interfacing of TTL outputs to high-speed CMOS inputs, Texas Instruments (TI) introduced HCT circuits, a subgroup of its HC family. HCT features and functions are identical to HC devices with the exception of modified input circuitry which makes the input threshold voltage compatible with TTL circuits. HCT outputs are similar to the HC family.

The TTL/HC Interface

TTL output voltages and HC input voltages are incompatible, especially between the TTL high-level output voltage (V_{OH}) and the HC high-level input voltage (V_{IH}). This problem can be solved in three different ways. The first way is to use HCT devices with their TTL-compatible input voltages to interface between TTL and HC circuits. Another solution is to provide pullup resistors at the TTL outputs to ensure an adequate high-level TTL output voltage. The third method requires the use of level shifters.

Of the three alternatives mentioned, using HCT circuits to solve the incompatibility problem is the most convenient. Designed to meet the requirements of this application, HCT devices allow the engineer to benefit from the advantages of HC devices (low power consumption) without using discrete components such as pullup resistors.

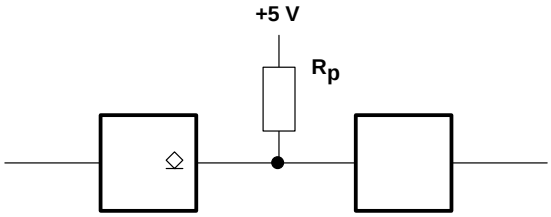

Figure 1. TTL-CMOS Interface With Open-Collector Output and Pullup Resistor

Using pullup resistors to accommodate TTL output signals to interface with HC input circuits (see Figure 1), the design engineer has to choose the resistance that is appropriate for the application. The minimum value of the resistor is determined by the maximum current I_{OL} that a TTL circuit can supply at the low-level output (V_{OL}).

$$R_p\text{min} = \frac{V_{CC}\text{max} - V_{OL}\text{min}}{I_{OL} + n \times I_{IL}} \quad \textbf{(1)}$$

where n is the number of HC inputs to be driven, and I_{IL} is their input current. I_{IL}, having a value of only a few nanoamperes, is negligible in all calculations.

In the case of a SN74ALS03, the following equation defines $R_p$min:

$$R_p\text{min} = \frac{5.5\ \text{V} - 0.4\ \text{V}}{8\ \text{mA}} = 640\ \Omega \quad \textbf{(2)}$$

To calculate the upper limit of this resistor, a sufficient V_{IH} high level must be ensured.

$$R_p\text{max} = \frac{V_{CC} - V_{IH}\text{min}}{n \times I_{IH}} \quad \textbf{(3)}$$

In this situation, the input current of HC devices is negligible and very high values are also obtained.

When calculating the maximum allowable resistance, it is important to ensure that the maximum allowable rise time (t_r = 500 ns) at the HC input is not exceeded. The following equation then applies:

$$V_{IH} = V_{CC}\left(1 - e^{\frac{-t}{R_p \times C}}\right) \quad (4)$$

where C is the total load capacitance in the circuit. C is composed of the output capacitance of the driving gate (≈10 pF), the total input capacitances of gates to be driven (≈5 pF each), and the line capacitance (≈1 pF/cm). The actual value is calculated by solving the equation for R_p:

$$R_p = \frac{-t}{C \times \ln\left(1 - \frac{3.5\ V}{5\ V}\right)} \quad (5)$$

Assuming the total capacitance, C, is 30 pF, the maximum resistor is:

$$R_p = \frac{-500\ ns}{30\ pF \times \ln\left(1 - \frac{3.5\ V}{5\ V}\right)} = 14\ k\Omega \quad (6)$$

Faster rise times result in lower impedance and more power consumption. The previous calculation is based on the assumption that the driving gate has an open collector. Conditions become more satisfactory, however, when a gate with totem-pole output (i.e., SN74ALS00) is used. In that case, the gate output provides the voltage to be brought up to the value V_{OH} = 2.7 V in less than 10 ns (the rise time of the TTL signal). The pullup resistor only has to pull the level to 3.5 V within the desired time. According to the previous formula, and with a required rise time of t_r = 50 ns, the resistor is defined by the following calculation:

$$R_p max = \frac{-50\ ns - 10\ ns}{30\ pF \times \ln\left(1 - \frac{3.5\ V - 2.7\ V}{5\ V - 2.7\ V}\right)} = 3.12\ k\Omega \quad (7)$$

The upper limiting value of the resistor is primarily dictated by the rise time required. The larger the resistance, the longer the rise times and propagation delay times. Reducing the resistance increases speed and power dissipation.

The third method of accommodating TTL signals to HC circuits is accomplished with special level shifters. This solution is not recommended because the level shifter itself has no inherent logic functions and increases component and space requirements.

For design engineers, using HCT circuits to match TTL signal levels with HC devices is the most convenient and efficient way of solving incompatibility problems. HCT devices contain the necessary level shifters and additional logic functions in a single circuit. Furthermore, the designer is not forced to compromise among signal rise time, system speed, and power consumption of the stages.

Operating Voltages of HCT Circuits

HCT circuits feature a limited operating voltage range due to the fact that they have to work with TTL voltage levels. Since internal switching layout is equivalent to HC circuits (with the exception of the input stage), these components could be operated from a 2-V to 6-V range. For HCT circuits operating at less than 4.5 V, the load-level noise margin is reduced and becomes incompatible with TTL thresholds, thus losing one of the primary advantages of the HCT devices.

Noise of HCT Circuits

The noise margin of a logic family is a very important consideration in system design. Composed of low-level and high-level noise margins, each of these components has to be considered separately. The high-level noise margin is the voltage difference between the guaranteed output voltage (V_{OH}) of the driving gate and the guaranteed input voltage (V_{IH}) of the triggered gate. Accordingly, the low-level noise margin can be defined as the voltage difference between the guaranteed output voltage (V_{OL}) and the input voltage, V_{IL} (see Figure 2).

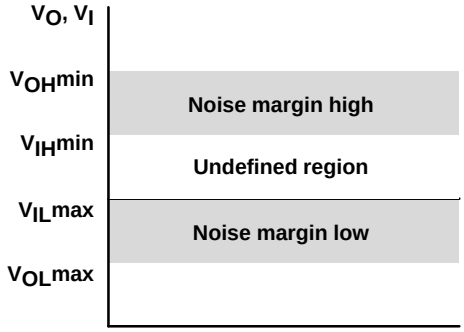

Figure 2. Noise Margin

Regarding magnitude relations, it is desirable to keep both noise margins as large as possible and the undefined range between them as narrow as possible. If the noise margin is not large enough in a certain application, internally or externally sourced interference can modify (i.e., falsify) a signal to fall within the undefined range. Internal noise is caused by inductive or ohmic drops or by inductive and capacitive couplings with other signaling lines. The coupling between signal lines is the more critical aspect in most cases. Figure 3 shows the voltage conditions for HC, HCT and TTL circuits.

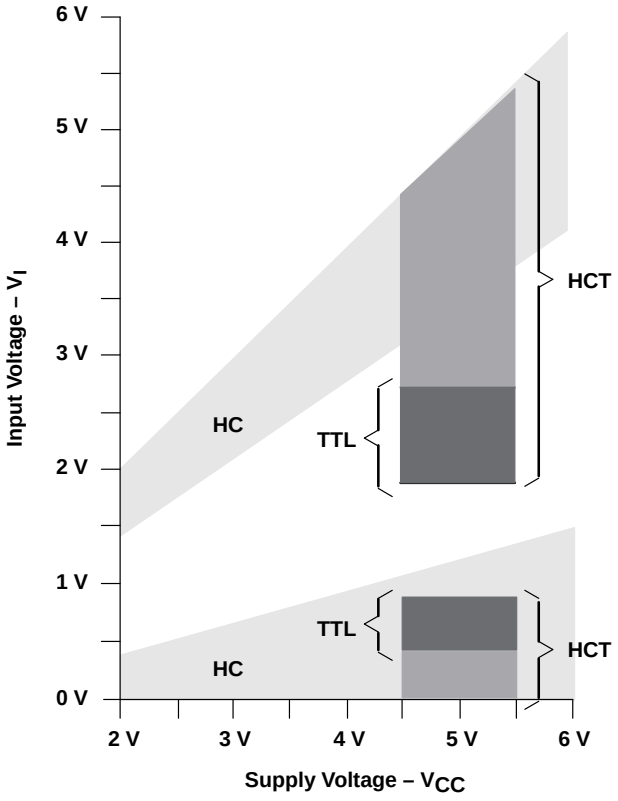

Figure 3. Guaranteed Noise Margins for HC, HCT, and TTL Devices

Since a certain percentage is always transmitted from the noise-emitting line to the interfered line, it is not the absolute noise margin (in volts) that is of consequence, but rather the quotient of the absolute noise margin and the signal-voltage swing. The percentile high- and low-level noise margins (S) would be defined by the following equations:

$$S_H = \frac{V_{OH} - V_{IH}min}{V_{OH} - V_{OL}} \times 100\% \quad (8)$$

$$S_L = \frac{V_{IL}max - V_{OL}}{V_{OH} - V_{OL}} \times 100\% \quad (9)$$

To obtain realistic values, the guaranteed V_{OH}min and V_{OL}max data sheet voltage values must not be used when calculating signal deviation $V_{OH} - V_{OL}$. Data-sheet specifications would indicate a smaller signal deviation and thus a wider noise margin. V_{OH} and V_{OL} values should be based on the low- and high-level voltages supplied by the circuit under normal operating conditions. The following table lists the different voltages for HC, HCT, and TTL circuits, and the resulting noise margins. All calculations use a supply voltage of V_{CC} = 5 V to achieve comparable results.

Table 1. Voltage Levels and Noise Margins

	HC	HCT	TTL	UNIT
V_{OH}typ	4.9	4.9	3.4	V
V_{OL}typ	0.1	0.1	0.3	V
Signal voltage swing V_{OH}typ – V_{OL}typ	4.8	4.8	3.1	V
V_{IH}min	3.5	2.0	2.0	V
V_{IL}max	1.0	0.8	0.8	V
S_H V_{OH}min – V_{IH}min	1.4	2.9	0.7	V
S_L V_{IL}min – V_{OL}min	0.9	0.7	0.4	V
S_H	29.1	60.4	22.5	%
S_L	18.7	14.6	12.9	%

As you see, the low-level noise margin (S_L) is the most critical value for all three logic families, ranging from 18.7% (HC) to 12.9% (TTL). With respect to noise margins, HC devices feature significantly better performance than bipolar logic circuits. In practice, however, the ability of individual circuits to attenuate the noise impressed into a line is the most important. The test setups in Figures 4 and 5 are used to measure the actual noise margin expected in a system. The measured value refers to the crosstalk between two parallel lines. Twenty-five centimeters, usually the maximum length that occurs on a printed circuit board, is regarded as a basic line length.

In Figure 4, the signals are propagating across the line in the same direction. A noise that is induced by line 1 on to line 2 is immediately shorted by the low output impedance of the gate. Signal A in Figure 4 shows the signal on the noise-emitting line, and signals B and C show the noise generated on line 2 at the low and high levels. Both HC and TTL maintain noise values that stay below their allowable limits.

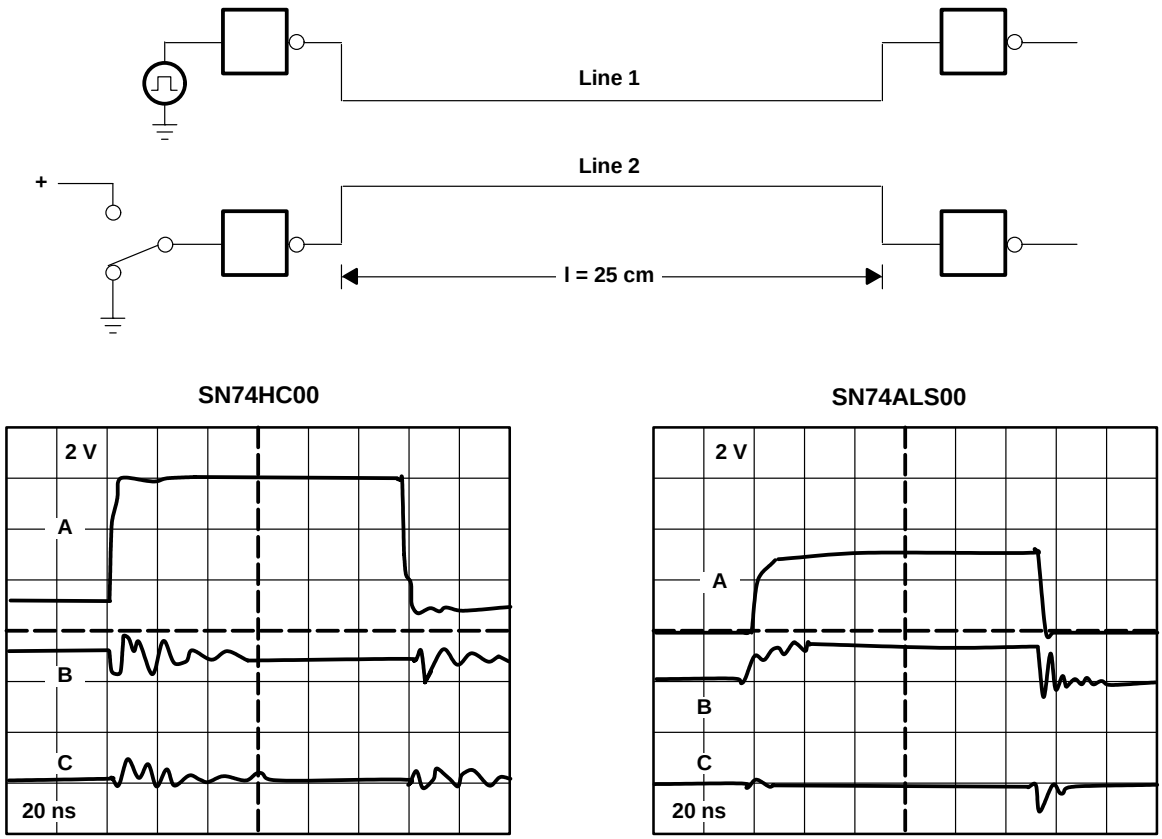

Figure 4. Crosstalk (First Case)

The same configuration is used in the second case, but signals on both lines propagate in opposite directions. A noise impressed on the parallel-running line by the interfering line is not attenuated immediately because at that place the line is terminated by its high-impedance input only. The noise becomes more effective and runs across the line up to the driver output. The low output impedance of the driver output shorts the noise to a large extent. The attenuated interfering signal is reflected at the beginning of the line, and then, after double signal propagation time, the noise is eliminated at the end of the interfered line as well. Due to the larger signal swing (deviation) of HC circuits (4.8 V) as opposed to TTL devices (3.5 V), a larger noise amplitude can be expected. This value does not fully explain the significant amplitude differences in the oscillographs shown in Figure 5. In this case, the output impedance at the low level is significantly lower for TTL circuits (R_i = 10 Ω) as compared to HC devices (R_i = 50 Ω).

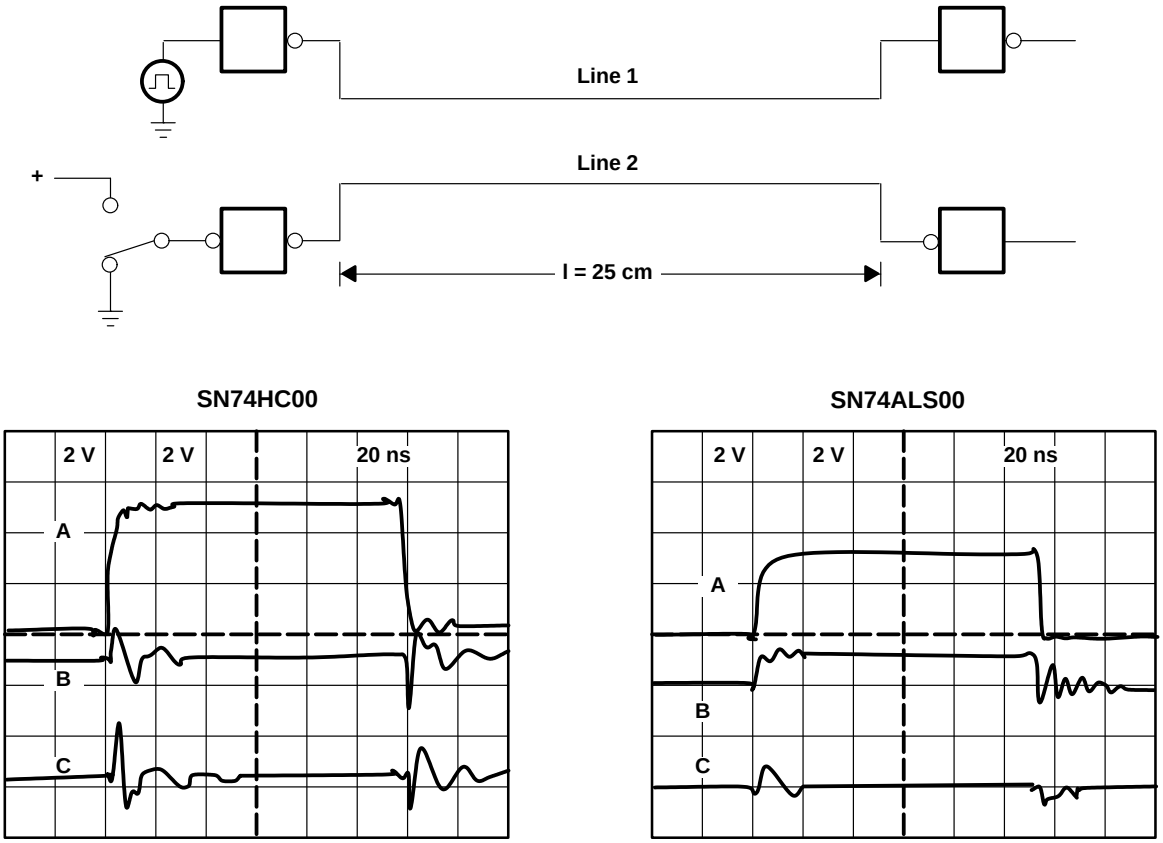

Figure 5. Crosstalk (Second Case)

In addition, the slew rate of the edge (dv/dt), particularly the positive edge of HC circuits, is significantly larger in value compared to TTL circuits. However, HC devices usually operate without interference because the typical threshold voltage at HC circuit inputs amounts to 2.5 V, and this value is not reached in the demonstrated examples. In contrast, the noise amplitude of HCT circuits significantly exceeds the typical threshold voltage of 1.5 V.

To summarize, inherent noise remains below the critical limits within a pure TTL or HC system. When HCT devices are used, the maximum line length should not exceed 10 cm to maintain crosstalk below critical values. Because the logical application of HCT devices is interfacing between HC and TTL circuits, and line lengths are normally shorter, this requirement presents no serious restriction.

Power Consumption of HCT Circuits

The threshold voltage of a CMOS circuit is determined by the geometry of the input transistors. These transistors are designed to sink the same input current at the required threshold voltage. The resulting voltage at the output is equivalent to 50% of the supply voltage V_{CC}. For an HC circuit, the channel width of the p-channel transistor of the input is approximately twice the value of an n-channel transistor. The purpose is to make both transistors have the same current characteristics, thus making the threshold voltage of their input at about 50% of the supply voltage V_{CC}. This circuit area has been modified for HCT devices: the n-channel transistor is about seven times wider than the p-channel transistor (see Figure 6). This shifts the threshold voltage in a way that it amounts to 30% of the supply voltage. At a supply voltage $V_{CC} = 5$ V, the threshold voltage is $V_T = 1.5$ V, similar to the threshold voltage of TTL circuits.

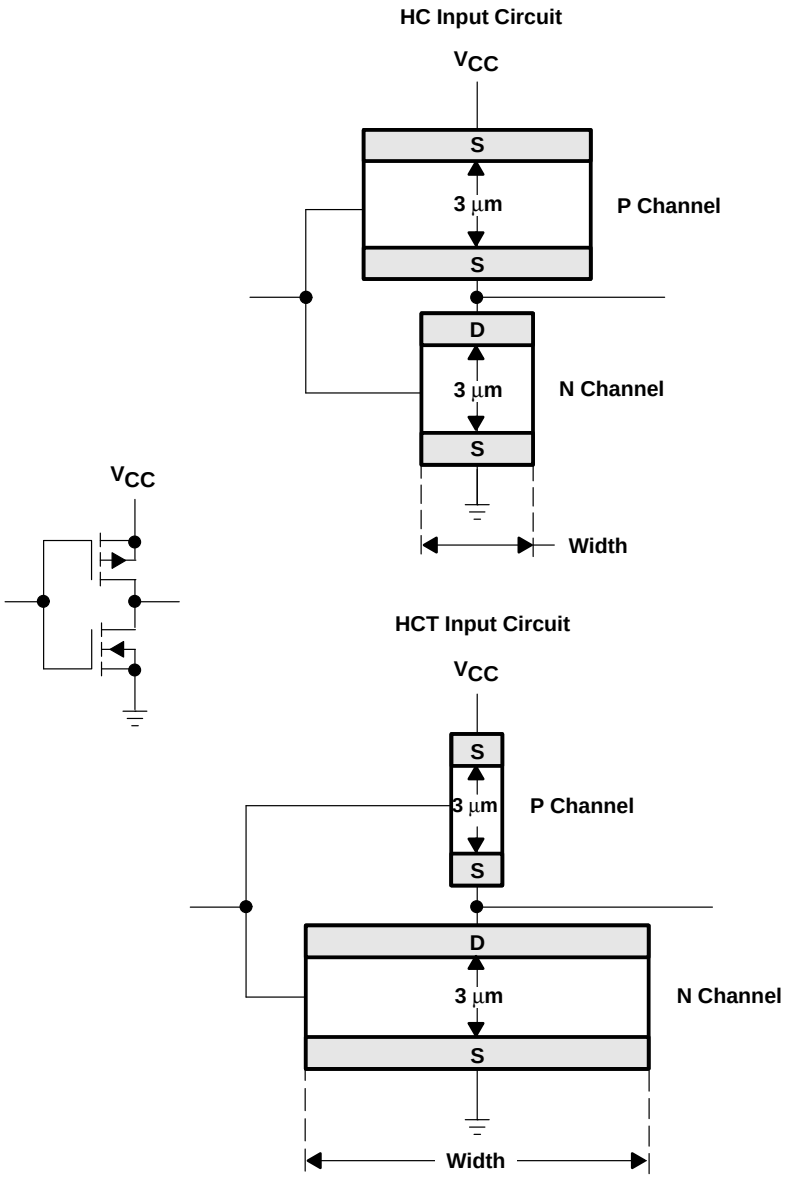

Figure 6. Input-Stage Structure of HC and HCT Circuits

Some compromises are necessary for HCT circuits to reach the parameters required. An unlimited size reduction of the p-channel transistor is impossible without reducing the drain current and thus the whole circuit speed. This is why the n-channel transistor must be enlarged to shift the threshold voltage accordingly. The result is that the supply current of the circuit rises (see Figure 7) if the input voltage is not equal to the supply voltage (p-channel transistor off) or to ground potential (n-channel transistor off). In this case, both transistors are conducting, especially when HCT circuits are triggered by TTL voltage levels. TI includes the parameter ΔI_{CC} for HCT circuits, a value that specifies the increase of the supply current I_{CC} if driven by TTL levels (V_{IL} = 0.4 V, V_{IH} = 2.4 V). This parameter allows the circuit design engineer to calculate the expected power consumption.

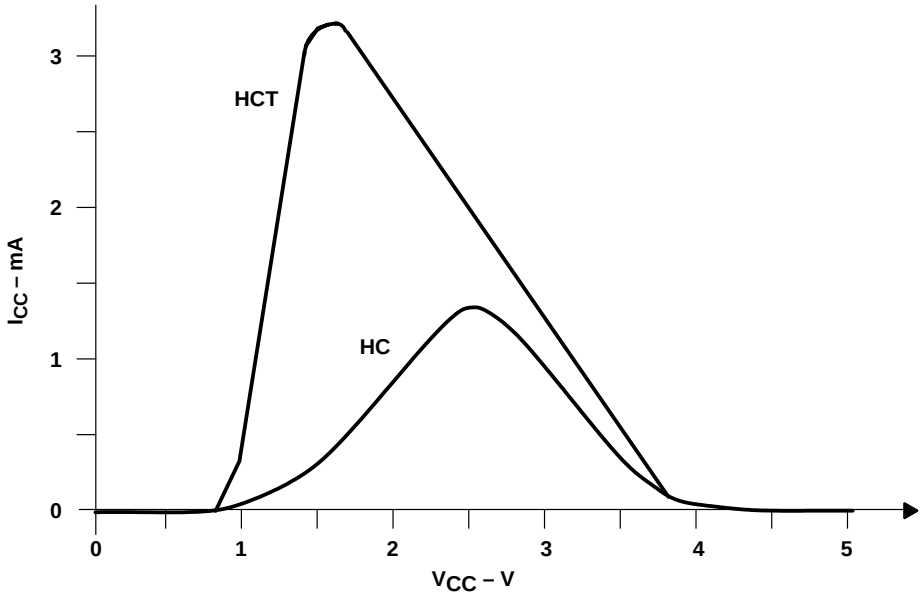

Figure 7. Supply Current as a Function of the Input Voltage

Figure 8 shows the effects of power consumption in a complete system. It shows power consumption of an SN74HCT243 with all four inputs triggered. In one case, the input signal has HC levels (V_{IL} = 0 V, V_{IH} = 5 V); in the other case, TTL levels (V_{IL} = 0.4 V, V_{IH} = 2.4 V). The duty cycle of the input signal is 50%. Each output has a load C_L = 50 pF. As you see, supply current is about 4 mA higher for a device triggered by TTL levels.

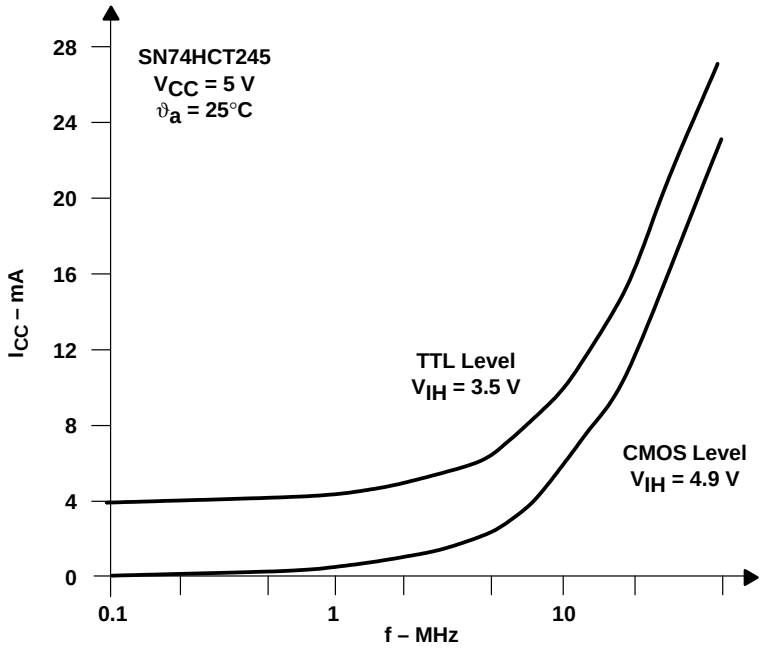

Figure 8. Current Consumption as a Function of Frequency

For frequencies above 5 MHz, this effect is of secondary importance, since current consumption is then determined primarily by the power required for reversing the charge of the load capacitance. Moreover, the increase of current consumption for devices driven by TTL levels is much lower in practice. The reason is that TTL circuits supply a typical voltage swing that is significantly higher than the data sheet value used for the measurement in Figure 8.

Delay Times

Another restriction in the use of HCT circuits results from increased transmission delay times. Although these circuits do not contain more stages than HC devices, the time of reversing charge at the output of the first stage is extended because of the smaller p-channel transistor and the higher capacitance of the n-channel transistor. This prolongs the delay time approximately 1–2 ns for HCT circuits as compared to HC circuits.

Bergeron Analysis

The speed of the ALS and HC logic families and the associated higher slew rate (especially for HC devices) force the system design engineer to carefully evaluate the behavior of electrical waves on the lines. In addition, line reflections have to be considered when the rise and fall times of logic signals are shorter than the propagation time of signals on unterminated lines. Under certain circumstances, these reflections can distort the transferred signals so that the receiver at the other end of the line cannot recognize the signal.

Because digital circuits have no linear input and output characteristics, the equations known for evaluating line reflections are not applicable. A better solution is to use the Bergeron diagram, a graphical method that supplies results with sufficient precision for the examples in question. Figure 9 shows the high- and low-level output characteristics of an SN74ALS245A, as well as the input characteristic of an HC device. Because the input current of these circuits is very low (and negligible), this characteristic coincides with the V axis in the range from 0–5 V. The voltage curve at transmitter and receiver for the positive and negative edges is obtained by drawing the resistance line with slope Z_O and $-Z_O$ onto the graph (see Figure 10). Both cases achieve voltages that fall within the required limits (V_{IL}max = 0.8 V, V_{IH}min = 2.0 V), and the undershoot at the negative edges at the right sides of the pulses is sufficiently damped by the diodes integrated into the input circuitry of HC devices.

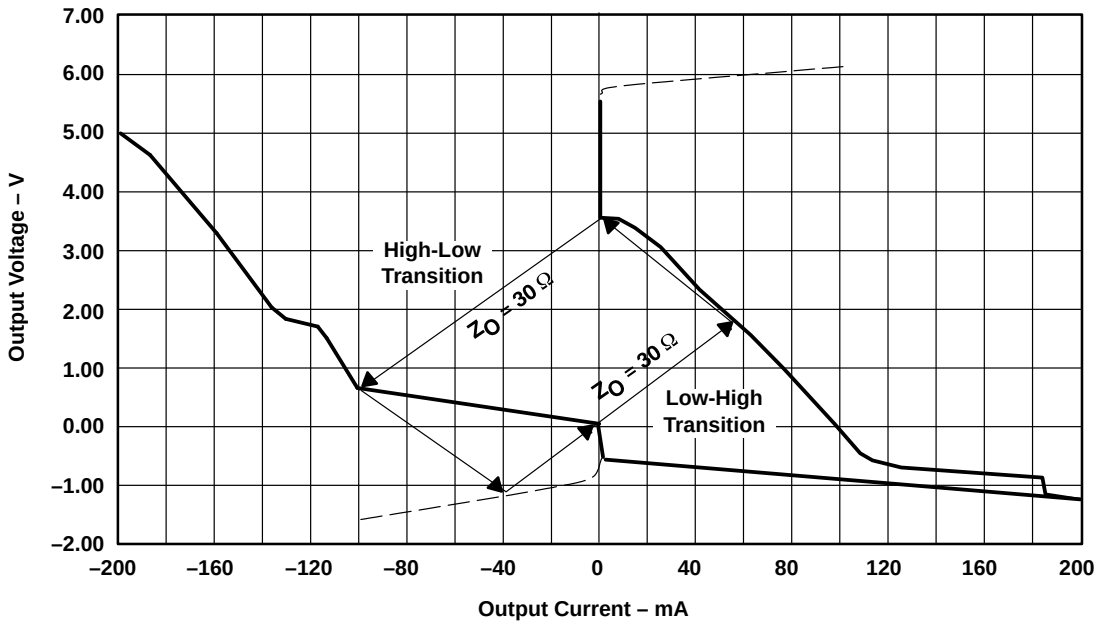

Figure 9. Bergeron Diagram, SN74ALS245 Driver

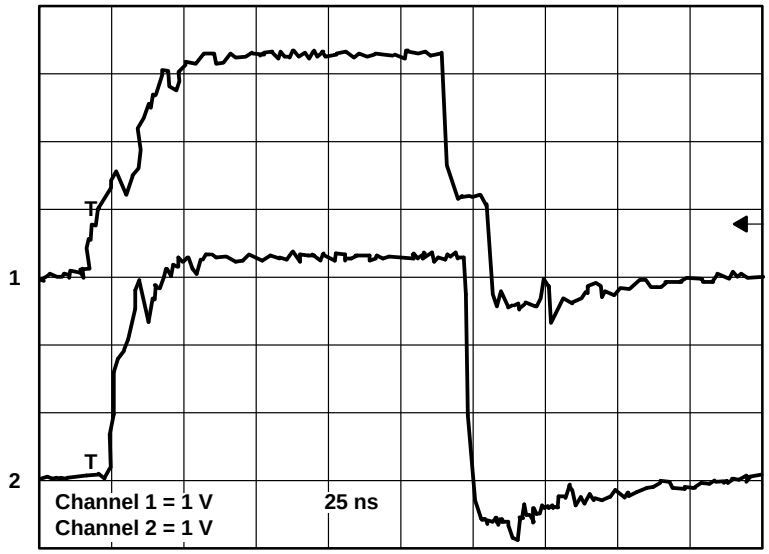

Figure 10. Line Reflections, SN74ALS245 Driver

Figures 11 and 12 show the associated diagrams for an HC or an HCT driver. There is no problem with the positive-going edge. At the line end, a voltage of 3.5 V is applied which is a valid high for both HC and HCT. At the negative edge, the voltage at the line end reaches a level of approximately 1 V. This value is sufficient to drive an HC circuit, but cannot securely drive an HCT device that requires a low-level value below 0.8 V.

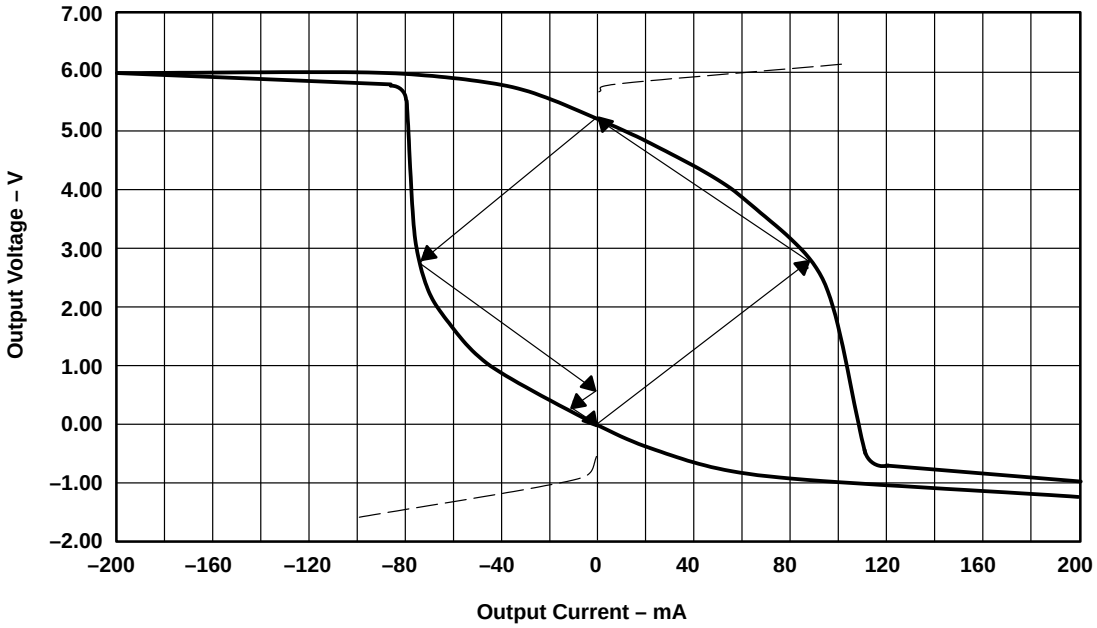

Figure 11. Bergeron Diagram, SN74HC245 Driver

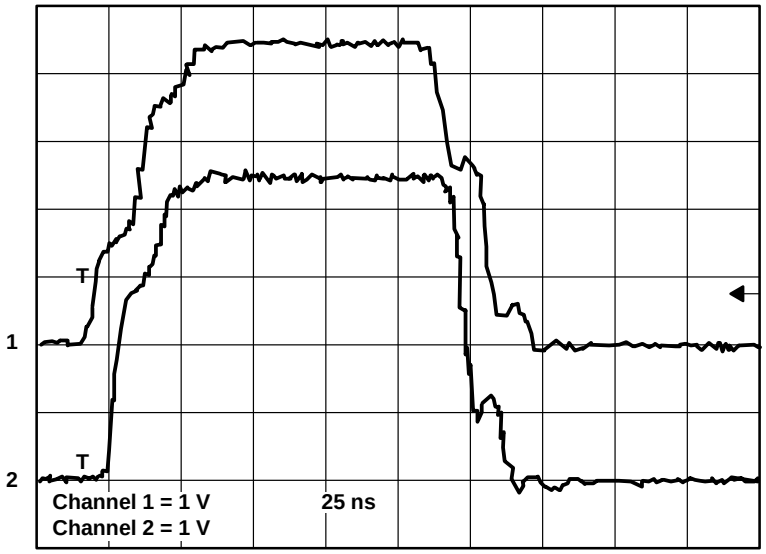

Figure 12. Line Reflections, SN74HC245 Driver

Summary

The SN74HCT circuit family from TI is a subgroup of the SN74HC series. Whereas devices of both families are equivalent in their features and functions, the HCT input circuitry was modified to meet interfacing requirements. These devices can be driven by TTL circuits directly, without the need for additional components. Thus, the HCT family offers an ideal, simple, and cost-effective solution for mixing systems using both TTL and HC devices. However, employing HCT instead of HC devices in pure CMOS systems cannot be recommended. There are several advantages in using HC technology, such as the broad supply-voltage range and the reduction of any adverse effect caused by the lower switching threshold on dynamic behavior. Due to the lower noise margin, there is an increased risk of interference caused by crosstalk, especially when the lines on the printed circuit board exceed a certain length. Moreover, the reduced switching threshold no longer ensures faultless operation of advanced bus systems used in microprocessor applications today.

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