Understanding Operational Amplifier Specifications

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Understanding Operational Amplifier Specifications

Abstract

Selecting the right operational amplifier for a specific application requires you to have your design goals clearly in mind along with a firm understanding of what the published specifications mean. This paper addresses the issue of understanding data sheet specifications.

This paper begins with background information. First, introductory topics on the basic principles of amplifiers are presented, including the ideal op amp model. As an example, two simple amplifier circuits are analyzed using the ideal model. Second, a simplified circuit of an operational amplifier is discussed to show how parameters arise that limit the ideal functioning of the operational amplifier.

The paper then focuses on op amp specifications. Texas Instruments' data book, *Amplifiers, Comparators, and Special Functions*, is the basis for the discussion on op amp specifications. Information is presented about how Texas Instruments defines and tests operational amplifier parameters.

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Introduction

The term operational amplifier, abbreviated op amp, was coined in the 1940s to refer to a special kind of amplifier that, by proper selection of external components, can be configured to perform a variety of mathematical operations. Early op amps were made from vacuum tubes consuming lots of space and energy. Later op amps were made smaller by implementing them with discrete transistors. Today, op amps are monolithic integrated circuits, highly efficient and cost effective.

Amplifier Basics

Before jumping into op amps, lets take a minute to review some amplifier fundamentals. An amplifier has an input port and an output port. In a linear amplifier, output signal = $A \times$ input signal, where A is the amplification factor or gain.

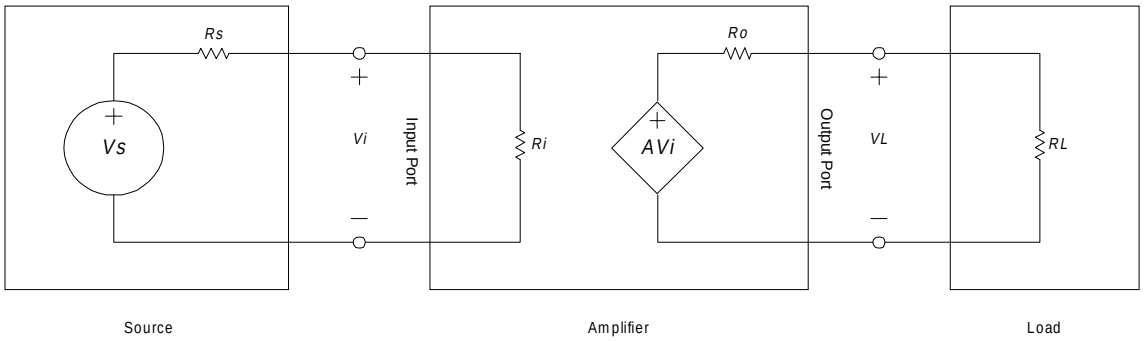
Depending on the nature of input and output signals, we can have four types of amplifier gain:

- Voltage (voltage out/voltage in)
- Current (current out/current in)
- Transresistance (voltage out/current in)
- Transconductance (current out/voltage in)

Since most op amps are voltage amplifiers, we will limit our discussion to voltage amplifiers.

Thevenin's theorem can be used to derive a model of an amplifier, reducing it to the appropriate voltage sources and series resistances. The input port plays a passive role, producing no voltage of its own, and its Thevenin equivalent is a resistive element, R_i. The output port can be modeled by a dependent voltage source, AV_i, with output resistance, R_O. To complete a simple amplifier circuit, we will include an input source and impedance, V_S and R_S, and output load, R_L. Figure 1 shows the Thevenin equivalent of a simple amplifier circuit.

Figure 1. Thevenin Model of Amplifier with Source and Load

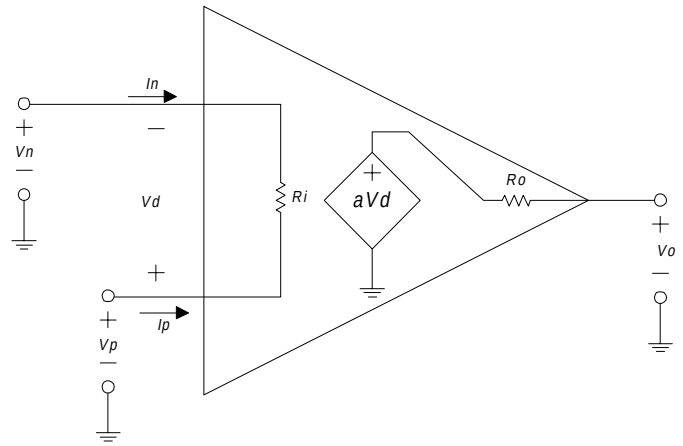


It can be seen that we have voltage divider circuits at both the input port and the output port of the amplifier. This requires us to re-calculate whenever a different source and/or load is used and complicates circuit calculations.

Ideal Op Amp Model

The Thevenin amplifier model shown in Figure 1 is redrawn in Figure 2 showing standard op amp notation. An op amp is a differential to single-ended amplifier. It amplifies the voltage difference, $V_d = V_p - V_n$, on the input port and produces a voltage, V_O, on the output port that is referenced to ground.

Figure 2. Standard Op Amp Notation

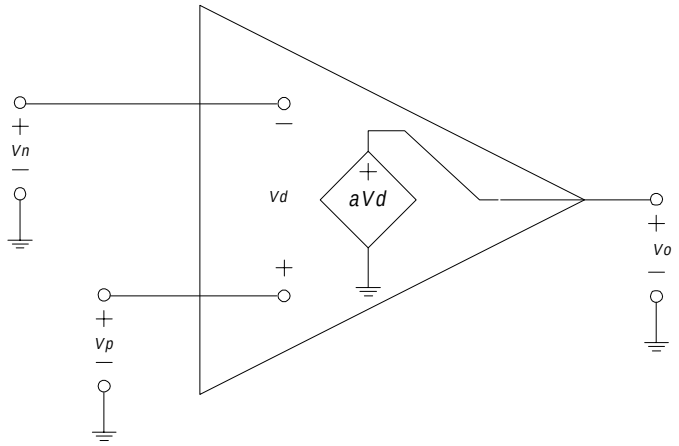


We still have the loading effects at the input and output ports as noted above. The ideal op amp model was derived to simplify circuit calculations and is commonly used by engineers in first-order approximation calculations. The ideal model makes three simplifying assumptions:

- Gain is infinite $a = \infty$ (1)
- Input resistance is infinite $R_i = \infty$ (2)
- Output resistance is zero $R_O = 0$ (3)

Applying these assumptions to Figure 2 results in the ideal op amp model shown in Figure 3.

Figure 3. Ideal Op Amp Model



Other simplifications can be derived using the ideal op amp model:

$\Rightarrow$ **$I_n = I_p = 0$** (4)

Because $R_i = \infty$, we assume $I_n = I_p = 0$. There is no loading effect at the input.

$\Rightarrow$ **$Vo = a\ V_d$** (5)

Because $R_O = 0$ there is no loading effect at the output.

$\Rightarrow$ **$V_d = 0$** (6)

If the op amp is in linear operation, V_O must be a finite voltage. By definition $V_O = V_d \times a$. Rearranging, $V_d = V_O / a$. Since $a = \infty$, $V_d = Vo / \infty = 0$. This is the basis of the virtual short concept.

$\Rightarrow$ **Common mode gain = 0** (7)

The ideal voltage source driving the output port depends only on the voltage difference across its input port. It rejects any voltage common to V_n and V_p.

$\Rightarrow$ **Bandwidth** = ∞ (8)

$\Rightarrow$ **Slew Rate** = ∞ (9)

No frequency dependencies are assumed.

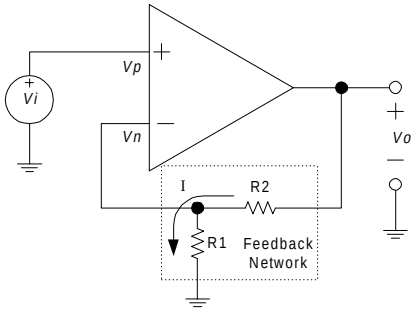
$\Rightarrow$ **Drift = 0** (10)

There are no changes in performance over time, temperature, humidity, power supply variations, etc.

Non-Inverting Amplifier

An ideal op amp by itself is not a very useful device since any finite input signal would result in infinite output. By connecting external components around the ideal op amp, we can construct useful amplifier circuits. Figure 4 shows a basic op amp circuit, the non-inverting amplifier. The triangular gain block symbol is used to represent an ideal op amp. The input terminal marked with a + (Vp) is called the non-inverting input; – (Vn) marks the inverting input.

Figure 4. Non-Inverting Amplifier



To understand this circuit we must derive a relationship between the input voltage, V_i, and the output voltage, V_O.

Remembering that there is no loading at the input,

$$V_p = V_i \tag{11}$$

The voltage at V_n is derived from V_O via the resistor network, R_1 and R_2, so that,

$$V_n = V_o \frac{R_1}{R_1+R_2} = V_o\, b \tag{12}$$

where,

$$b = \frac{R_1}{R_1+R_2} \tag{13}$$

The parameter *b* is called the feedback factor because it represents the portion of the output that is fed back to the input.

Recalling the ideal model,

$$V_O = aV_d = a(V_p - V_n) \tag{14}$$

Substituting,

$$V_O = a(V_i - bV_O) \tag{15}$$

and collecting terms yield,

$$A = \frac{V_o}{V_i} = \left(\frac{1}{b}\right)\left(\frac{1}{1 + \frac{1}{ab}}\right) \tag{16}$$

This result shows that the op amp circuit of Figure 4 is itself an amplifier with gain *A*. Since the polarity of V_i and V_O are the same, it is referred to as a non-inverting amplifier.

A is called the *close loop gain* of the op amp circuit, whereas a is the *open loop gain*. The product ab is called the *loop gain*. This is the gain a signal would see starting at the inverting input and traveling in a clockwise loop through the op amp and the feedback network.

Closed Loop Concepts and Simplifications

Substituting $a = \infty$ (1) into (16) results in,

$$A = \frac{1}{b} = 1 + \frac{R_2}{R_1} \tag{17}$$

Recall that in equation (6) we state that V_d, the voltage difference between V_n and V_p, is equal to zero and therefore, $V_n = V_p$. Still they are not shorted together. Rather there is said to be a *virtual short* between V_n and V_p. The concept of the virtual short further simplifies analysis of the non-inverting op amp circuit in Figure 4.

Using the virtual short concept, we can say that,

$$V_n = V_p = V_i \tag{18}$$

Realizing that finding Vn is now the same resistor divider problem solved in (12) and substituting (18) into it, we get,

$$V_i = V_o \quad \frac{R_1}{R_1 + R_2} = V_o\, b \tag{19}$$

Rearranging and solving for *A*, we get,

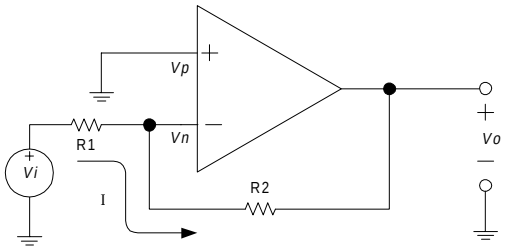
$$A = \left(\frac{1}{b}\right) = 1 + \left(\frac{R2}{R1}\right)$$

The same result is derived in (17). Using the virtual short concept reduced solving the non-inverting amplifier, shown in Figure 4, to solving a resistor divider network.

Inverting Amplifier

Figure 5 shows another useful basic op amp circuit, the inverting amplifier. The triangular gain block symbol is again used to represent an ideal op amp. The input terminal, + (Vp), is called the non-inverting input, whereas – (Vn) marks the inverting input. It is similar to the non-inverting circuit shown in Figure 4 except that now the signal is applied to the inverting terminal via R1 and the non-inverting terminal is grounded.

Figure 5. Inverting Amplifier



To understand this circuit, we must derive a relationship between the input voltage, V_i and the output voltage, V_O.

Since V_p is tied to ground,

$$V_p = 0 \tag{20}$$

Remembering that there is no current into the input, the voltage at V_n can be found using superposition. First let $V_O = 0$,

$$V_n = V_i \left(\frac{R_2}{R_1+R_2}\right) \tag{21}$$

Next let $V_i = 0$,

$$V_n = V_o \left(\frac{R_1}{R_1+R_2}\right) \tag{22}$$

Combining

$$V_n = V_o \left(\frac{R_1}{R_1+R_2}\right) + V_i \left(\frac{R_2}{R_1+R_2}\right) \tag{23}$$

Remembering equation (14), $V_O = aV_d = a(V_p - V_n)$, substituting and rearranging,

$$A = \frac{V_o}{V_i} = 1 - \left(\frac{1}{b}\right)\left(\frac{1}{1 + \frac{1}{ab}}\right) \tag{24}$$

where

$$b = \frac{R_1}{R_1 + R_2}$$

Again we have an amplifier circuit. Because $b \leq 1$, the closed loop gain, A, is negative, and the polarity of V_O will be opposite to V_i. Therefore, this is an inverting amplifier.

Closed Loop Concepts and Simplifications

Substituting $a = \infty$ (1) into (24) results in

$$A = 1 - \frac{1}{b} = -\frac{R_2}{R_1} \tag{25}$$

Recall that in equation (6) we stated that V_d, the voltage difference between V_n and V_p, was equal to zero so that $V_n = V_p$. Still they are not shorted together. Rather there is said to be a *virtual short* between V_n and V_p. The concept of the virtual short further simplifies analysis of the inverting op amp circuit in Figure 5

Using the virtual short concept, we can say that

$$V_n = V_p = 0 \tag{26}$$

In this configuration, the inverting input is a virtual ground.

We can write the node equation at the inverting input as

$$\frac{V_n - V_i}{R_1} + \frac{V_n - V_o}{R_2} = 0 \tag{27}$$

Since $V_n = 0$, rearranging, and solving for A we get

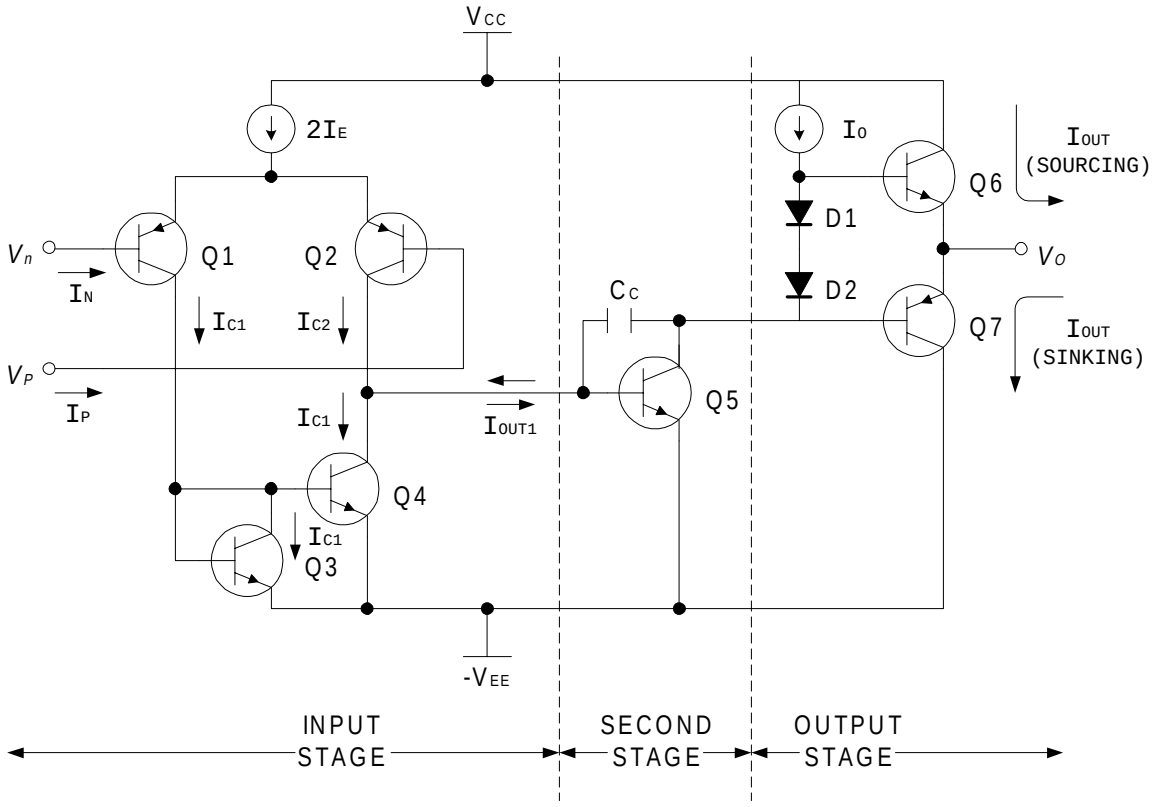
$$A = 1 - \frac{1}{b} = -\frac{R_2}{R_1} \tag{28}$$

The same result is derived more easily than in (24). Using the virtual short (or virtual ground) concept reduced solving the inverting amplifier, shown in Figure 5, to solving a single node equation.

Simplified Op Amp Circuit Diagram

Real op amps are not ideal. They have limitations. To understand and discuss the origins of these limitations, see the simplified op amp circuit diagram shown in Figure 6.

Figure 6. Simplified Op Amp Circuit Diagram



Although simplified, this circuit contains the three basic elements normally found in op amps:

- Input stage
- Second stage
- Output stage

The function of the input stage is to amplify the input difference, V_p - V_n, and convert it to a single-ended signal. The second stage further amplifies the signal and provides frequency compensation. The output stage provides output drive capability.

Input Stage

Symmetry of the input stage is key to its operation. Each transistor pair, Q1-Q2 and Q3-Q4, is matched as closely as possible.

Q3 is diode connected. This forces the collector current in Q3 to equal I_{C1}. The base-emitter junctions of Q3 and Q4 are in parallel so they both see the same V_{BE}. Because Q4 is matched to Q3, its collector current is also equal to I_{C1}. This circuit is called a current mirror.

Current source $2I_E$ is divided between Q1 and Q2. This division depends on the input voltages, V_p and V_n.

When V_p is more positive than V_n, Q1 carries more current than Q2, and I_{C1} is larger than I_{C2}. The current mirror action of Q3-Q4 causes I_{OUT1} to flow into the collector-collector junction of Q2-Q4.

When V_n is more positive than V_P, Q2 carries more current than Q1 and I_{C2} is larger than I_{C1}. The current mirror action of Q3-Q4 causes I_{OUT1} to flow out of the collector-collector junction of Q2-Q4.

I_{OUT1} is the single-ended signal out of the first stage and is proportional to the differential input, $V_p - V_n$. $I_{OUT1} = g_{m_1}(V_p - V_n)$. The term g_{m_1} is called the transconductance of the input stage. The input stage is a transconductance amplifier.

Second Stage

The second stage converts I_{OUT1} into a voltage and provides frequency compensation. If I_{OUT1} flows into the collector-collector junction of Q2-Q4, the second stage output voltage is driven positive. If I_{OUT1} flows out of the collector-collector junction of Q2-Q4, the second stage output voltage is driven negative. The second stage is a transresistance amplifier.

The capacitor, C_C, in the second stage provides internal frequency compensation. It causes the gain to role off as the frequency increases. Without C_C, external compensation is required to prevent the op amp from oscillating in most applications.

Output Stage

The output stage is a typical class AB, push-pull amplifier. The emitter follower configuration of Q6 and Q7 provides current drive for the output load, with unity voltage gain. The output stage is a current amplifier.

Op Amp Specifications

If you have experimented with op amp circuits at moderate gain and frequency, you probably have noted very good agreement between actual performance and ideal performance. As gain and/or frequency are increased, however, certain op amp limitations come into play that effect circuit performance.

In theory, with proper understanding of the internal structures and processes used to fabricate an op amp, we could calculate these effects. Thankfully this is not necessary, as manufacturers provide this information in data sheets. Proper interpretation of data sheet specifications is required when selecting an op amp for an application.

This discussion of op amp parameters is based on Texas Instruments' data sheets. The following definitions (except as noted) are from the "Operational Amplifier Glossary" found in Texas Instruments' data book, *Amplifiers, Comparators, and Special Functions*, pg. 1-37 to pg. 1-40 and pg. 5-37 to pg. 5-40. It defines most of the parameters found in the data sheets.

Operational Amplifier Glossary

α_{IIO} **Average temperature coefficient of input offset current**	The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range. Usually measured in µV/°C.
α_{VIO} †**Average temperature coefficient of input offset voltage**	The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range. Usually measured in µV/°C.
ϕ_m **Phase margin**	The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.
A_m **Gain margin**	The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.
A_V **Large-signal voltage amplification**	The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.
A_{VD} **Differential voltage amplification**	The ratio of the change in the output to the change in differential input voltage producing it with the common-mode input voltage held constant.

† These definitions were misprinted in the data book noted and were corrected by the author**.**

B1 † **Unity gain bandwidth**	The range of frequencies within which the open-loop voltage amplification is greater that unity.
BOM **Maximum-output-swing bandwidth**	The range of frequencies within which the maximum output voltage swing is above a specified value.
Ci **Input capacitance**	The capacitance between the input terminals with either input grounded.
CMRR **Common-mode rejection ratio**	The ratio of differential voltage amplification to common-mode voltage amplification. Note: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.
$\overline{\text{F}}$ †**Average noise figure**	The ratio of (1) the total output noise power within a designated output frequency band when the noise temperature of the input termination(s) is at the reference noise temperature at all frequencies to (2) that part of (1) caused by the noise temperature of the designated signal-input termination within a designated signal-input frequency.
ICC+, ICC- **Supply current**	The current into the V_{CC+} or V_{CC-} terminal of an integrated circuit.
IIB **Input bias current**	The average of the currents into the two input terminals with the output at the specified level.
IIO **Input offset current**	The difference between the currents into the two input terminals with the output at the specified level.
In **Equivalent input noise current**	The current of an ideal current source (having internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.
IOL **Low-level output current**	The current into an output with input conditions applied that according to the product specification will establish a low level at the output.
IOS **Short-circuit output current**	The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point.
kSVS † **Supply voltage sensitivity**	The absolute value of the ratio of the change in input offset voltage to the change in supply voltages. Notes: 1. Unless otherwise noted, both supply voltages are varied symmetrically. 2. This is the reciprocal of supply rejection ratio.

† These definitions were misprinted in the data book noted and were corrected by the author**.**

k_{SVR} **Supply voltage rejection ratio**	The absolute value of the ratio of the change in supply voltages to the change in input offset voltage. Notes: 1. Unless otherwise noted, both supply voltages are varied symmetrically. 2. This is the reciprocal of supply sensitivity.
P_D **Total power dissipation**	The total dc power supplied to the device less any power delivered from the device to a load. Note: At no load: $P_D = V_{CC+} \bullet I$
r_i **Input resistance**	The resistance between the input terminals with either input grounded.
r_{id} **Differential input resistance**	The small-signal resistance between two ungrounded input terminals.
r_o **Output resistance**	The resistance between an output terminal and ground.
SR **Slew rate**	The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.
t_r **†Rise time**	The time required for an output voltage step to change from 10% to 90% of its final value.
t_{tot} **Total response time**	The time between a step-function change of the input signal and the instant at which the magnitude of the output signal reaches, for the last time, a specified level range (±e) containing the final output signal level.
V_I **Input voltage range**	The range of voltage that if exceeded at either input may cause the operational amplifier to cease functioning properly.
V_{IO} **Input offset voltage**	The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.
V_{IC} **Common-mode input voltage**	The average of the two input voltages.
V_{ICR} **Common-mode input voltage range**	The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.
V_n **Equivalent input noise voltage**	The voltage of an ideal voltage source (having internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.
V_{01}/V_{02} **Crosstalk Attenuation**	The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel.

†These definitions were misprinted in the data book noted and were corrected by the author**.**

V_{OH} **High-level output voltage**	The voltage at an output with input conditions applied that according to the product specifications will establish a high level at the output.
V_{OL} **Low-level output voltage**	The voltage at an output with input conditions applied that according to the product specifications will establish a low level at the output.
V_{ID} **Differential input voltage**	The voltage at the non-inverting input with respect to the inverting input.
V_{OM} **Maximum peak output voltage swing**	The maximum positive or negative voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.
$V_{O(PP)}$ **Maximum peak-to-peak output voltage swing**	The maximum peak-to-peak voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.
Z_{ic} **Common-mode input impedance**	The parallel sum of the small-signal impedance between each input terminal and ground.
z_o **Output impedance**	The small-signal impedance between the output terminal and ground.
Overshoot factor	The ratio of the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal to the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.
THD + N [‡] **Total harmonic distortion plus noise**	The ratio of the RMS noise voltage and RMS harmonic voltage of the fundamental signal to the total RMS voltage at the output.
GBW [‡] **Gain bandwidth product**	The product of the open-loop voltage amplification and the frequency at which it is measured.
[‡] **Average long-term drift coefficient of input offset voltage**	The ratio of the change in input offset voltage to the change time. This is an average value for the specified time period. Usually measured in µV/month.

Texas Instruments usually specifies parameters under specific test conditions with some combination of minimum, typical and maximum values at 25° C, and over the full temperature range. What does this mean?

[‡] These definitions where added by the author. They appear commonly in the data sheets.

This means that a parameter measurement circuit is constructed, and the parameter is measured in a large number of devices at various temperatures over the temperature range of the device. Most parameters have a statistically normal distribution. The typical value published in the data sheet is the mean or average value of the distribution, with one exception, offset voltage. The average offset voltage is normally zero (or very close to zero). Therefore, the typical value listed for offset voltage is the 1σ value. This means that in 68% of the devices tested the parameter was found to be $\pm$ the typical value or better. The definition of minimum and maximum values has changed over the years. Texas Instruments currently publishes a conservative 6σ value.

Certain devices are screened for parameters such as offset voltage. These devices are normally given an A suffix. This ensures that the device meets the maximum value specified in the data sheet.

The following discussion uses Figure 6 extensively to explain the origins of the various parameters.

Absolute Maximum Ratings and Recommended Operating Conditions

The following typical parameters are listed in the absolute maximum ratings and the recommended operating conditions for TI op amps. The op amp will perform more closely to the typical values for parameters if operated under the recommended conditions. Stresses beyond the maximums listed will cause unpredictable behavior and may cause permanent damage.

- Absolute Maximums
  - Supply Voltage
  - Differential input voltage
  - Input voltage range
  - Input current
  - Output current
  - Total current into V_{DD+}
  - Total current out of V_{DD-}
  - Duration of short-circuit current (at or below 25°C)
  - Continuous total power dissipation
  - Operating free-air temperature
  - Storage temperature
  - Lead temperature

- Recommended Operating Conditions
  - Supply Voltage
  - Input voltage range
  - Common-mode input voltage
  - Operating free-air temperature

Input Offset Voltage

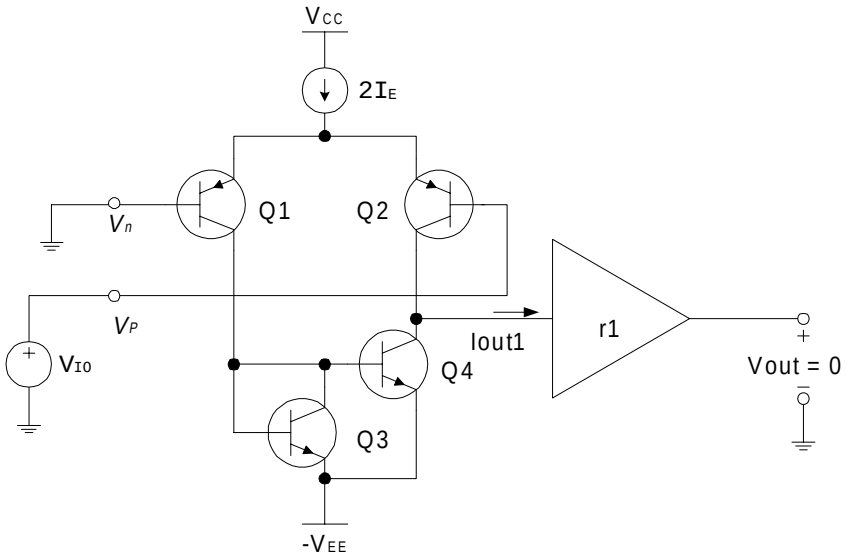
Input offset voltage, V_{IO}, is defined as "the DC voltage that must be applied between the input terminals to force the quiescent DC output voltage to zero or some other level, if specified". If the input stage was perfectly symmetrical and the transistors were perfectly matched, $V_{IO} = 0$. Because of process variations, geometry and doping are never exact to the last detail. All op amps require a small voltage between their inverting and non-inverting inputs to balance the mismatches. V_{IO} is normally depicted as a voltage source driving the non-inverting input, as shown in Figure 7.

TI data sheets show two other parameters related to V_{IO}; the average temperature coefficient of the input offset voltage and the input offset voltage long-term drift.

The average temperature coefficient of input offset voltage, αV_{IO}, specifies the expected input offset drift over temperature. Its units are $\mu V/°C$. V_{IO} is measured at the temperature extremes of the part, and αV_{IO} is computed as $\Delta V_{IO}/\Delta °C$.

Normal aging in semiconductors causes changes in the characteristics of devices. The input offset voltage long-term drift specifies how V_{IO} is expected to change with time. Its units are μV/month.

Figure 7. VIO



Input offset voltage is of concern anytime DC precision is required. Several methods are used to null its effects.

Input Current

Referring to Figure 6, we can see that a certain amount of bias current is required at each input. The input bias current, I_{IB}, is computed as the average of the two inputs,

$I_{IB} = (I_N+I_P)/2$

Input offset current, I_{IO}, is defined as the difference between the bias currents at the inverting and non-inverting inputs,

$I_{IO} = I_N-I_P$

Bias current is of concern when the input source impedance is high. Usually offset currents are an order of magnitude less than bias current so matching the input impedance of the inputs helps to nullify the effect of input bias current on the output voltage.

Input Common Mode Voltage Range

Normally there is a voltage that is common to the inputs of the op amp. If this common mode voltage gets too high or too low, the inputs will shut down and proper operation ceases. The common mode input voltage range, V_{ICR}, specifies the range over which normal operation is guaranteed.

Figure 8 illustrates the positive input voltage limit using the simplified op amp diagram of Figure 6. When V_{IN} is higher than V_{CC} - 0.9V, the input transistors and the current source will begin to shut down.

Figure 8. Positive Common-Mode Voltage Input Limit

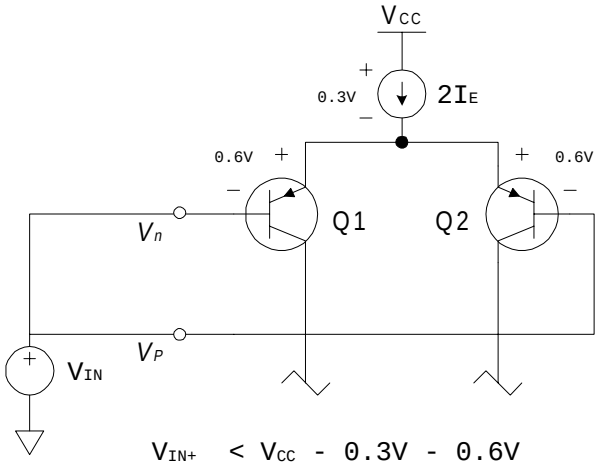
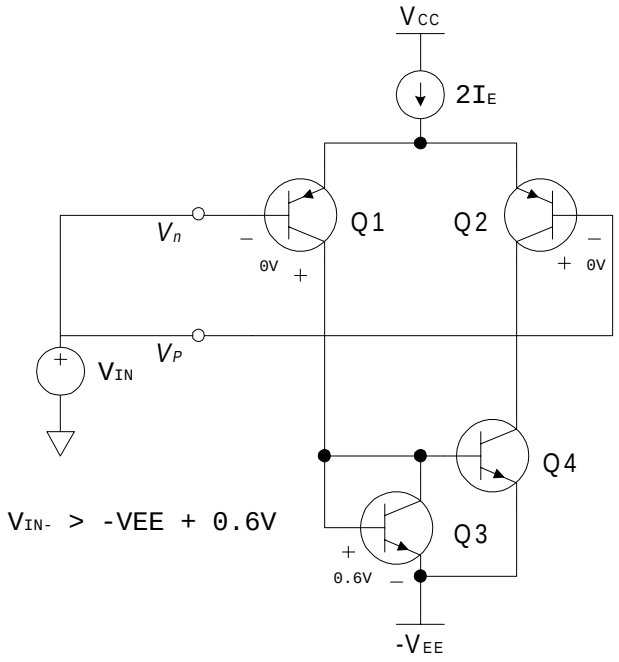


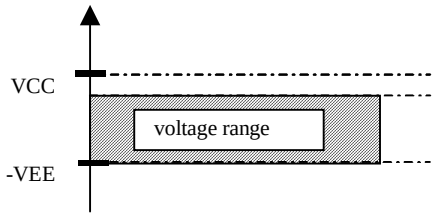
Figure 9 illustrates the negative input voltage limit using the simplified op amp diagram of Figure 6. When VIN is less than -VEE + 0.6V, the current mirror (Q3-Q4) will begin to shut down.

Figure 9. Negative Common-Mode Voltage Input Limit

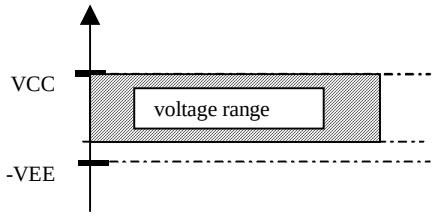


Structures like the one shown in the example above do not allow the common-mode input voltage to include either power supply rail. Other technologies used to construct op amp inputs offer different common-mode input voltage ranges that do include one or both power supply rails. Some examples are as follows (reference schematics can be found in the Texas Instruments' data book, *Amplifiers, Comparators, and Special Functions*):

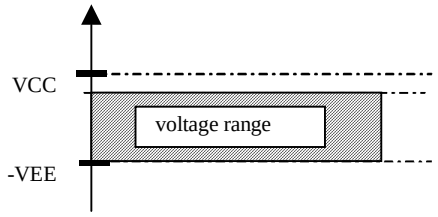
- The LM324 and LM358 use bipolar PNP inputs that have their collectors connected to the negative power rail. Since V_{BC} can equal zero, this allows the common-mode input voltage range to include the negative power rail.



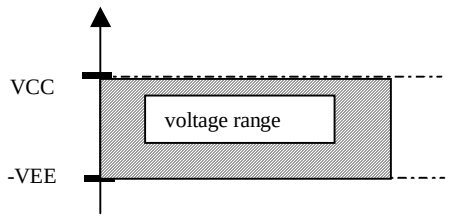
- The TL07X and TLE207X type BiFET op amps use p-channel JFET inputs with the sources tied to the positive power rail via a bipolar current source. Since V_{GS} can equal zero, this structure typically allows the common-mode input voltage range to include the positive power rail.



- TI LinCMOS op amps use p-channel CMOS inputs with the substrate tied to the positive power rail. Therefore a conducting channel is created for $V_G + V_{TH} < V_{DD}$ and this allows the common-mode input voltage range to include the negative power rail.



- Rail-to-rail input op amps use complementary N and P type devices in the differential inputs. When the common-mode input voltage nears either rail at least one of the differential inputs is still active.

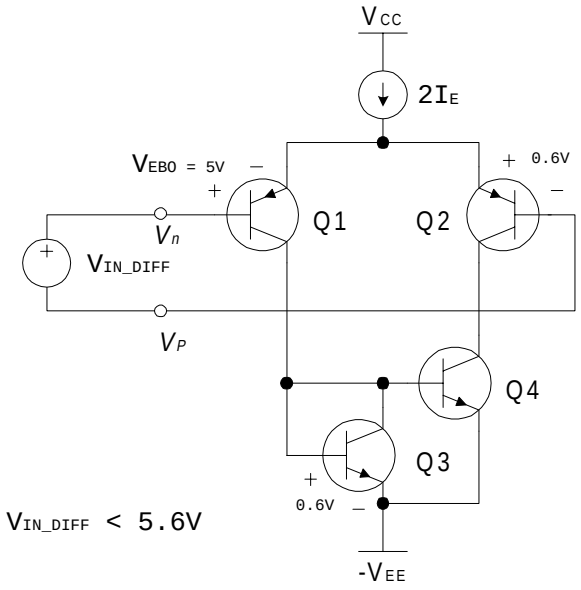


Differential Input Voltage Range

Differential input voltage range is normally specified in data sheets as an absolute maximum. Figure 10 illustrates this.

If the differential input voltage is greater than the base-emitter reverse break down voltage of input transistor Q1 plus the base-emitter forward breakdown voltage of Q2, then Q1's BE junction will act like a zener diode. This is a destructive mode of operation and results in deterioration of Q1's current gain. The same is true if V_{IN_DIFF} is reversed, except Q2 breaks down.

Figure 10. Differential-Mode Voltage Input Limit

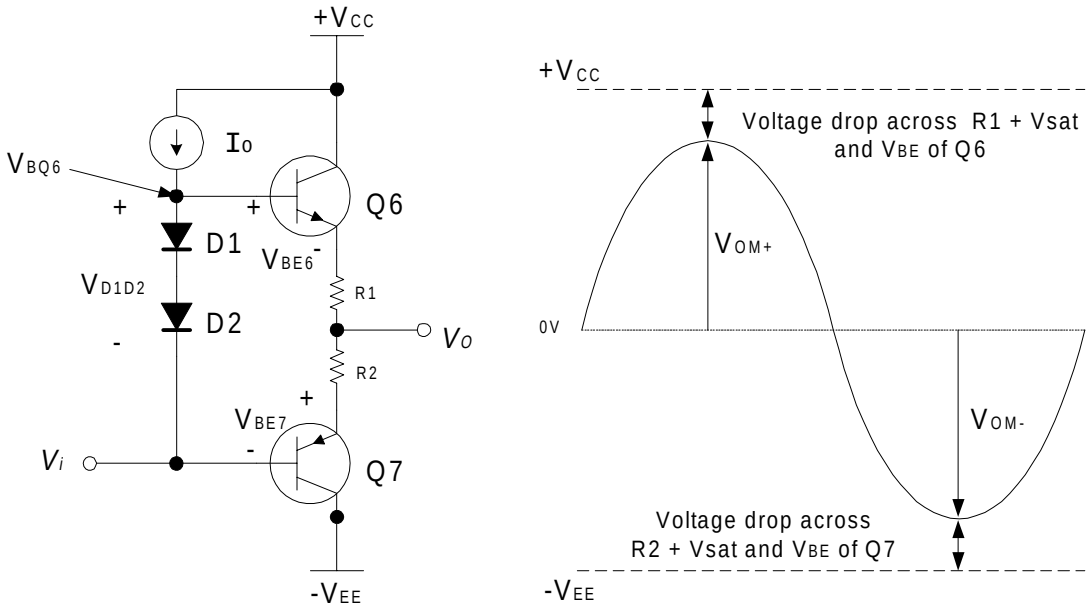


Some devices have protection built into them, and the current into the input needs to be limited. Normally, differential input mode voltage limit is not a design issue.

Maximum Output Voltage Swing

The maximum output voltage, $V_{OM\pm}$, is defined as “the maximum positive or negative peak output voltage that can be obtained without wave form clipping when quiescent DC output voltage is zero”. $V_{OM\pm}$ is limited by the output impedance of the amplifier, the saturation voltage of the output transistors, and the power supply voltages. This is shown in Figure 11. Note that $V_{OM\pm}$ depends on the output load.

Figure 11. $V_{OM\pm}$



The maximum value that V_{BQ6} can be is $+V_{CC}$, therefore $V_O <= +V_{CC} – V_{R1} – V_{BEQ6} – V_{SATQ6}$. The minimum value that Vi can be is $–V_{EE}$, therefore $V_O >= –V_{EE} + V_{R2} + V_{BEQ7} + V_{SATQ7}$.

This emitter follower structure cannot drive the output voltage to either rail. Rail to rail output op amps use a common emitter (bipolar) or common source (CMOS) output stage. With these structures, the output voltage swing is only limited by the saturation voltage (bipolar) or the on resistance (CMOS) of the output transistors, and the load being driven.

Because newer products are focused on single supply operation, more recent data sheets from Texas Instruments use the terminology V_{OH} and V_{OL} to specify the maximum and minimum output voltage.

Maximum and minimum output voltage is usually a design issue when dynamic range is lost if the op amp cannot drive to the rails. This is the case in single supply systems where the op amp is used to drive the input of an analog-to-digital converter, which is configured for full scale input voltage between ground and the positive rail.

Large Signal Differential Voltage Amplification

Large signal differential voltage amplification, A_{VD}, is the ratio of the output voltage change to the input differential voltage change, while holding V_{CM} constant. This parameter is closely related to the open loop gain. The difference is that it is measured with an output load and therefore takes into account loading effects.

The DC value of A_{VD} is published in the data sheet, but A_{VD} is frequency dependent. Figure 18 shows a typical graph of A_{VD} vs. frequency.

A_{VD} is a design issue when precise gain is required. Consider equation (16), where the loop gain of the non-inverting amplifier is given by:

$$A = \frac{V_o}{V_i} = \left(\frac{1}{b}\right)\left(\frac{1}{1 + \frac{1}{ab}}\right)$$

where,

$$b = \frac{R_1}{R_1 + R_2}$$

It is desired to control the gain of the circuit by selecting the appropriate resistors. The term $1/ab$ in the equation is seen as an error term. Unless a, or A_{VD}, is large in comparison with $1/b$, it will have an undesired effect on the gain of the circuit.

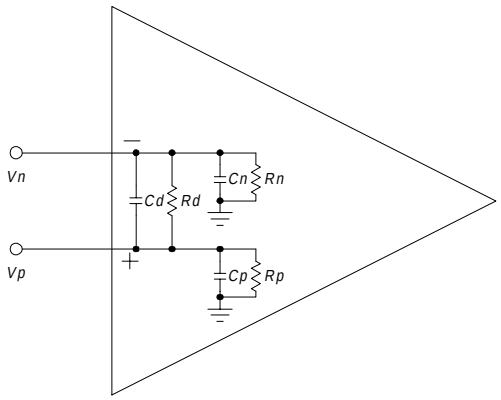
Input Parasitic Elements

Both inputs have parasitic impedance associated with them. Figure 12 shows a model where it is lumped into resistance and capacitance between each input terminal and ground and between the two terminals. There is also parasitic inductance, but the effects are negligible at low frequency.

Input impedance is a design issue when the source impedance is high. The input loads the source.

Also input capacitance will cause extra phase shift in the feedback path. This erodes phase margin and can be a problem when using high value feedback resistors.

Figure 12. Input Parasitic Elements



Input Capacitance

Input capacitance, Ci, is measured between the input terminals with either input grounded. Ci is usually on the order of a few pF. To relate Ci to Figure 12, if you ground Vp, Ci = Cd || Cn.

Sometimes common-mode input capacitance, Cic, is specified. To relate Cic to Figure 12, if you short Vp to Vn, Cic = Cp || Cn, the input capacitance a common mode source would see to ground.

Input Resistance

Two parameters for input resistance, ri and rid, are defined in Texas Instruments' data book, *Amplifiers, Comparators, and Special Functions*, pg. 1-39. Input resistance, ri, is "the resistance between the input terminals and either input grounded." Differential input resistance, rid, is "the small-signal resistance between two ungrounded input terminals."

To relate ri to Figure 12, if you ground Vp, ri = Rd || Rn. Depending on the type of input, values usually run on the order of $10^7\Omega$ to $10^{12}\Omega$.

To relate rid to Figure 12, with both input terminals floating, rid = Rd || (Rn + Rp). Depending on the type of input, values usually run on the order of $10^7\Omega$ to $10^{12}\Omega$.

Sometimes common-mode input resistance, ric, is specified. To relate ric to Figure 12, if you short Vp to Vn, ric = Rp || Rn, the input resistance a common mode source would see to ground.

Output Impedance

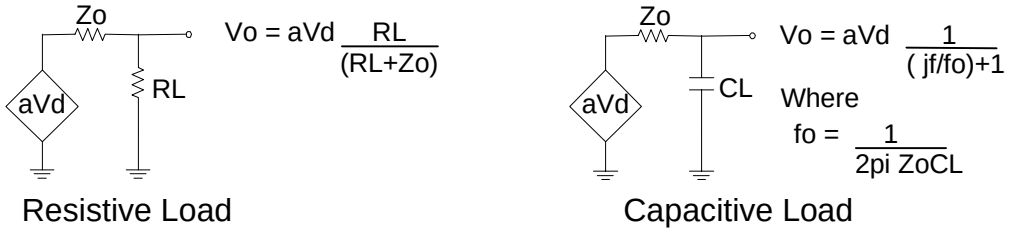
Different data sheets list the output impedance under two different conditions. Some data sheets list *closed-loop* output impedance while others list *open loop* output impedance, both designated by Zo.

Zo is defined as the small signal impedance between the output terminal and ground (see *Amplifiers, Comparators, and Special Functions*, pg. 1-40). Data sheet values run from 50Ω to 200Ω.

Common emitter (bipolar) and common source (CMOS) output stages used in rail-to-rail output op amps have higher output impedance than emitter follower output stages.

Output impedance is a design issue when using rail-to-rail output op amps to drive heavy loads. If the load is mainly resistive, the output impedance will limit how close to the rails the output can go. If the load is capacitive, the extra phase shift will erode phase margin. Figure 13 shows how output impedance affects the output signal assuming Zo is mostly resistive.

Figure 13. Effect of Output Impedance



Common-Mode Rejection Ratio

Common-mode rejection ratio, CMRR, is defined as the ratio of the differential voltage amplification to the common-mode voltage amplification, A_{DIF}/A_{COM}. Ideally this ratio would be infinite with common mode voltages being totally rejected.

The common-mode input voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which, in turn, changes the output voltage. The real mechanism at work is $\Delta V_{OS}/\Delta V_{COM}$.

In a Texas Instrument data sheet, CMRR = $\Delta V_{COM}/\Delta V_{OS}$ (gives a positive number in dB).

CMRR, as published in the data sheet, is a DC parameter. CMRR, when graphed vs. frequency, falls off as the frequency increases.

A common source of common-mode interference voltage is 50 Hz or 60 Hz noise from the AC mains. Care must be used to ensure that the CMRR of the op amp is not degraded by other circuit components.

Supply Voltage Rejection Ratio

Supply voltage rejection ratio, k_{SVR} (AKA power supply rejection ratio, PSRR), is the ratio of power supply voltage change to output voltage change.

The power voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which, in turn, changes the output voltage. The real mechanism at work is $\Delta V_{OS}/\Delta V_{CC\pm}$.

In a Texas Instrument data sheet, for a dual supply op amp, $k_{SVR} = \Delta V_{CC\pm}/\Delta V_{OS}$ (to get a positive number in dB). The term $\Delta V_{CC\pm}$ means that the plus and minus power supplies are changed symmetrically. For a single supply op amp, $k_{SVR} = \Delta V_{DD}/\Delta V_{OS}$ (to get a positive number in dB).

Also note that the mechanism that produces k_{SVR} is the same as for CMRR. Therefore, k_{SVR}, as published in the data sheet, is a DC parameter like CMRR; when k_{SVR} is graphed vs. frequency, it falls off as the frequency increases.

Switching power supplies can have noise on the order of 20 kHz to 200 kHz and higher. K_{SVR} is almost zero at these high frequencies, so that noise on the power supply results in noise on the output of the op amp.

Supply Current

Supply current, I_{DD}, is the quiescent current draw of the op amp(s) with no load. In a Texas Instrument data sheet, this parameter is usually the total quiescent current draw for the whole package. There are exceptions, as with the TL05X, TL06X, and TL07X, where I_{DD} is the quiescent current draw for each amplifier.

In op amps you trade power consumption for noise and speed.

Slew Rate at Unity Gain

Slew rate, SR, is the rate of change in the output voltage caused by a step input. Its units are V/μs or V/ms. Figure 14 shows slew rate graphically.

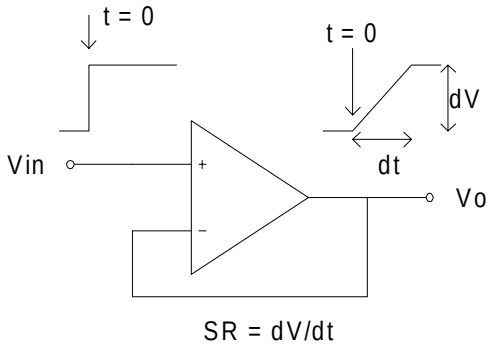
Referring back to Figure 6, voltage change in the second stage is limited by the charging and discharging of capacitor C_C. The maximum rate of change occurs when either side of the differential pair is conducting $2I_E$. This is the major limit to slew rate. Essentially, $SR = 2I_E/C_C$. However, there are op amps that work on different principles where this is not true.

The requirement to have current flowing in or out of the input stage to change the voltage out of the second stage requires an error voltage at the input anytime the output voltage of an op amp is changing. An error voltage on the order of 120 mV is required for an op amp with a bipolar input to realize full slew rate. This can be as high as 1V to 3V for a JFET or MOSFET input.

Capacitor, C_C, is added to make the op amp unity gain stable. Some op amps come in de-compensated versions where the value of C_C is reduced . This increases realizable bandwidth and slew rate, but the engineer must ensure the stability of the circuit by other means.

In op amps you trade power consumption for noise and speed. To increase slew rate, the bias currents within the op amp are increased.

Figure 14. Slew Rate



Equivalent Input Noise

All op amps have associated parasitic noise sources. Noise is measured at the output of an op amp and referenced back to the input; thus, it is called equivalent input noise.

Equivalent input noise specifications are usually given in two ways. One way is to specify the spot noise; that is, the equivalent input noise is given as voltage, V_n, (or current, I_n) per root hertz at a specific frequency. The second way is to specify noise as a peak-to-peak value over a frequency band. A brief review of noise characteristics is necessary to explain these parameters.

The spectral density of noise in op amps has a 1/f and a white noise component. 1/f noise is inversely proportional to frequency and is usually only significant at low frequencies. White noise is spectrally flat. Figure 15 shows a typical graph of op amp equivalent input noise.

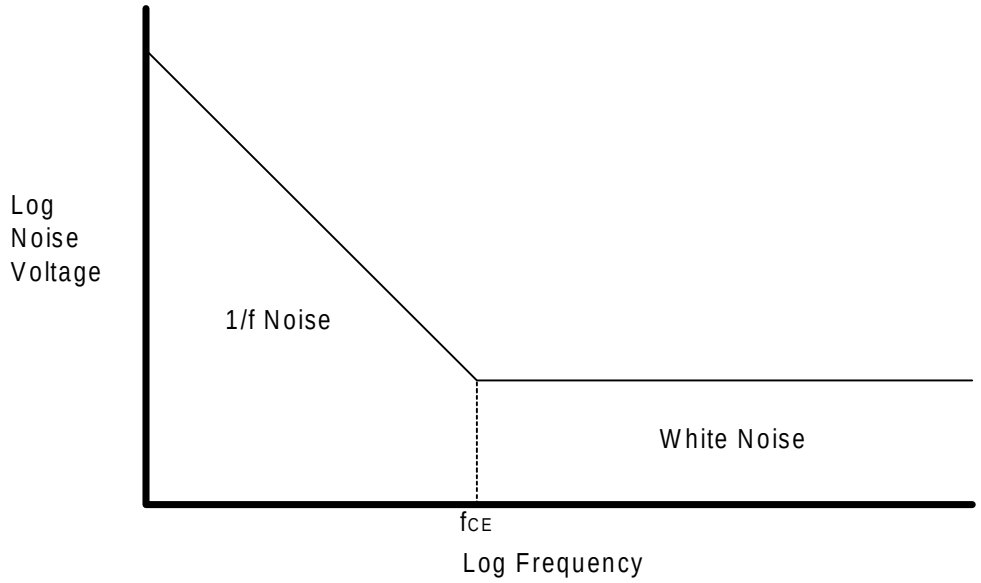
Usually spot noise is specified at two frequencies. The first frequency is usually 10 Hz, where the noise exhibits 1/f spectral density. The second frequency is typically 1 kHz, where the noise is spectrally flat. The units used are normally RMS nV/√Hz (or RMS pA/√Hz for current noise). In Figure 15 the transition between 1/f and white is denoted as the corner frequency, f_{CE}.

A noise specification, such as $V_{N(PP)}$, is the a peak to peak voltage over a specific frequency band, typically 0.1 Hz to 1 Hz or 0.1 Hz to 10 Hz. The units of measurement are typically nV pk-pk. To convert noise voltages given in RMS to pk-pk, a factor around 6 is typically used to account for the high crest factor seen in noise voltages e.g. $V_{N(PP)} = 6 \times V_{N(RMS)}$.

Given the same structure within an op amp, increasing bias currents lowers noise (and increases SR, GBW, and power dissipation).

Also the resistance seen at the input to an op amp adds noise. Balancing the input resistance on the non-inverting input to that seen at the inverting input, while helping with offsets due to input bias current, adds noise to the circuit.

Figure 15. Typical Op Amp Input Noise Spectrum



Total Harmonic Distortion plus Noise

Total harmonic distortion plus noise, THD + N, compares the frequency content of the output signal to the frequency content of the input. Ideally, if the input signal is a pure sine wave, the output signal is a pure sine wave. Because of non-linearity and noise sources within the op amp, the output is never pure.

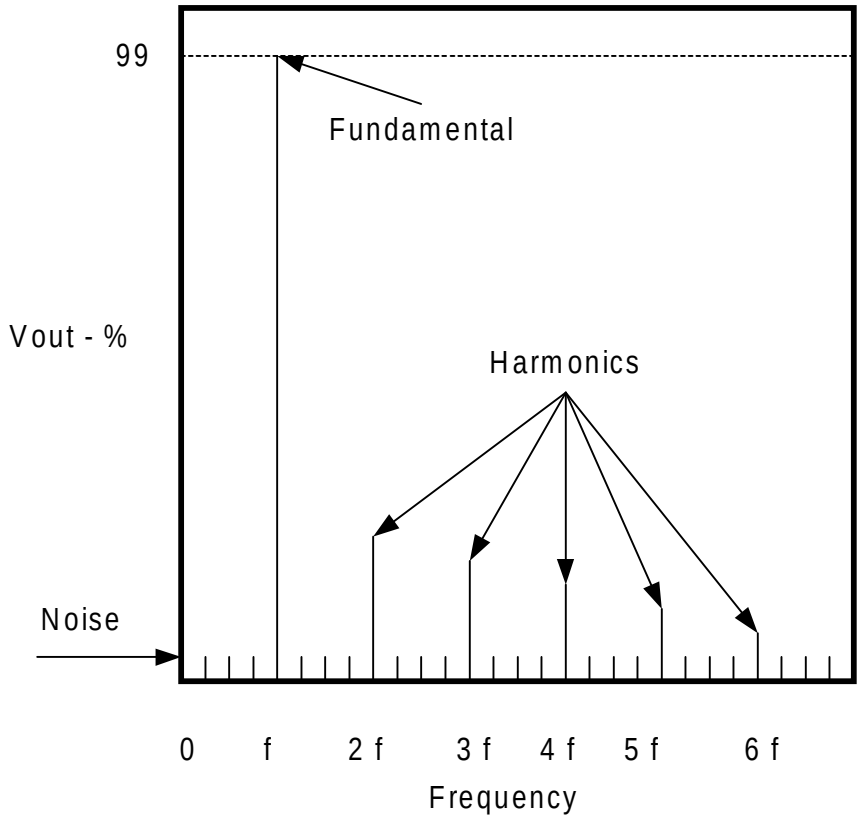
THD + N is the ratio of all other frequency components to the fundamental and is usually specified as a percentage:

$$\text{THD + N} = \frac{\sum (\text{Harmonic voltages + Noise voltages})}{\text{Total output voltage}} \times 100\%$$

Figure 16 shows a hypothetical graph where THD + N = 1%. The fundamental is the same frequency as the input signal and makes up 99% of the output signal. Non-linear behavior of the op amp results in harmonics of the fundamental being produced in the output. The noise in the output is mainly due to the input referenced noise of the op amp. All the harmonics and noise added together make up 1% of the output signal.

Two major reasons for distortion in an op amp are the limit on output voltage swing and slew rate. Typically an op amp must be operated at or below its recommended operating conditions to realize low THD.

Figure 16. Output Spectrum with THD + N = 1%



Unity-Gain Bandwidth and Phase Margin

There are five parameters that relate to the frequency characteristics of the op amp that you will encounter in Texas Instruments' data sheets:

- Unity-gain bandwidth (B_1)
- Gain bandwidth product (GBW)
- Phase margin at unity gain (ϕ_m)
- Gain margin
- Maximum output-swing bandwidth (B_{OM})

Unity-gain bandwidth (B_1) and gain bandwidth product (GBW) are similar. B_1 specifies the frequency at which A_{VD} of the op amp is 1:

$B_1 = f @ A_{VD} = 1$

GBW specifies the gain-bandwidth product of the op amp in an open loop configuration and the output loaded:

GBW = $A_{VD} \times f$

Phase margin at unity gain (ϕ_m) is the difference between the amount of phase shift a signal experiences through the op amp at unity gain and 180°:

ϕ_m = 180° - phase shift @ B_1

Gain margin is the difference between unity gain and the gain at 180° phase shift:

Gain margin = 1 – Gain @ 180° phase shift

Maximum output-swing bandwidth (B_{OM}) specifies the bandwidth over which the output is above a specified value:

$B_{OM} = f_{MAX}$, while $V_O > V_{MIN}$

The limiting factor for B_{OM} is slew rate. As the frequency gets higher and higher the output becomes slew rate limited and can not respond quickly enough to maintain the specified output voltage swing.

To make the op amp stable, capacitor, C_C, is purposely fabricated on chip in the second stage (see Figure 6). This type of frequency compensation is termed dominant pole compensation. The idea is to cause the open-loop gain of the op amp to role off to unity before the output phase shifts by 180°. Remember that Figure 6 is very simplified: there are other frequency shaping elements within a real op amp. Figure 17 shows a typical gain vs. frequency plot for an internally compensated op amp as normally presented in a Texas Instruments data sheet. Figure 18 contains the same information except the phase axis is shifted for clarity.

As noted earlier, it can be seen that A_{VD} falls off with frequency. A_{VD} (and thus B1 or GBW) is a design issue when precise gain is required of a specific frequency band. Consider equation (16), where the loop gain of the non-inverting amplifier is given by:

$$A = \frac{V_o}{V_i} = \left(\frac{1}{b}\right)\left(\frac{1}{1 + \frac{1}{ab}}\right)$$

It is desired to control the gain of the circuit by selecting the appropriate resistors. The term $1/ab$ in the equation is seen as an error term. Unless a, or A_{VD}, is large for all frequencies of interest in comparison with $1/b$, a will have an effect on the gain of the circuit, which is undesired.

Phase margin (ϕ_m) and gain margin are different ways of specifying the stability of the circuit. Since rail-to-rail output op amps have higher output impedance, a significant phase shift is seen when driving capacitive loads. This extra phase shift erodes the phase margin, and for this reason most CMOS op amps with rail-to-rail outputs have limited ability to drive capacitive loads.

Figure 17. Typical Large-Signal Differential Voltage Amplification and Phase Shift vs. Frequency

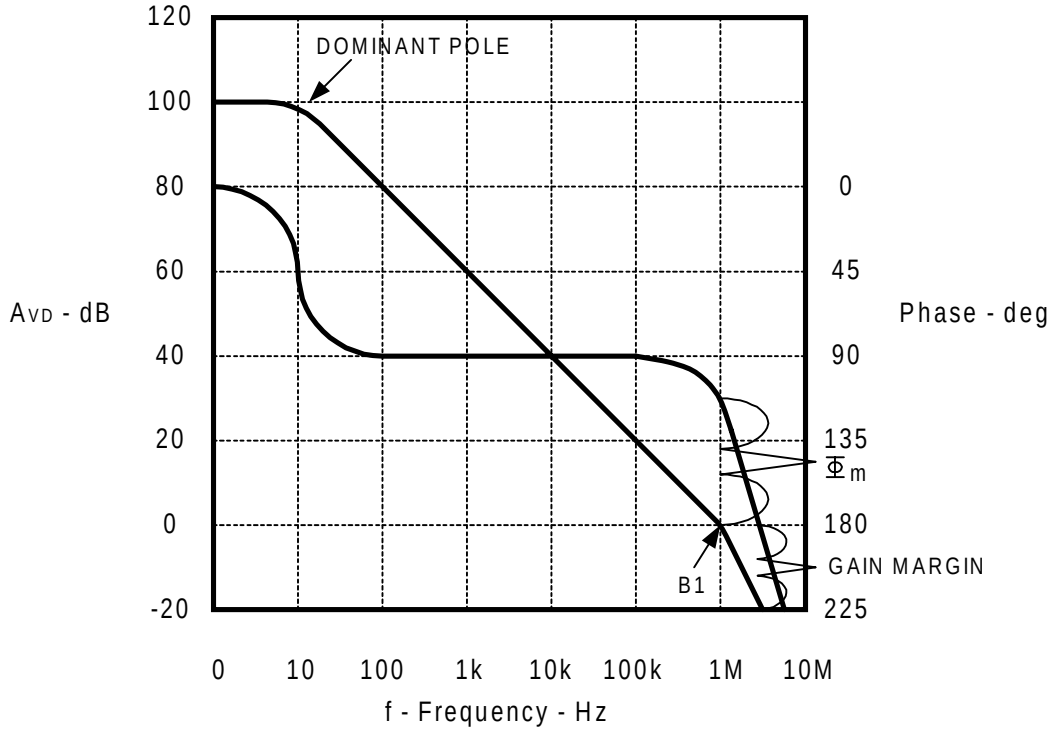
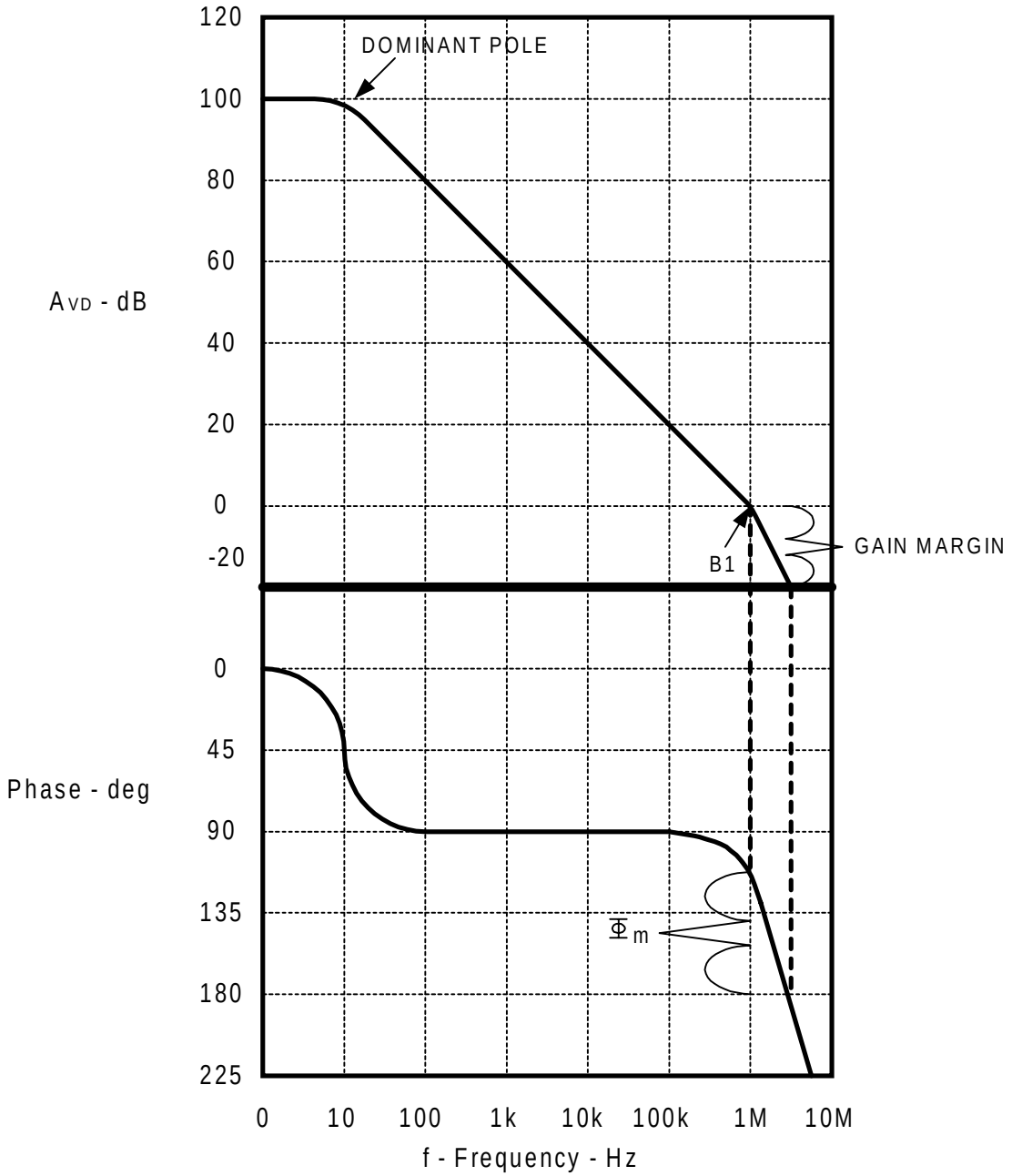


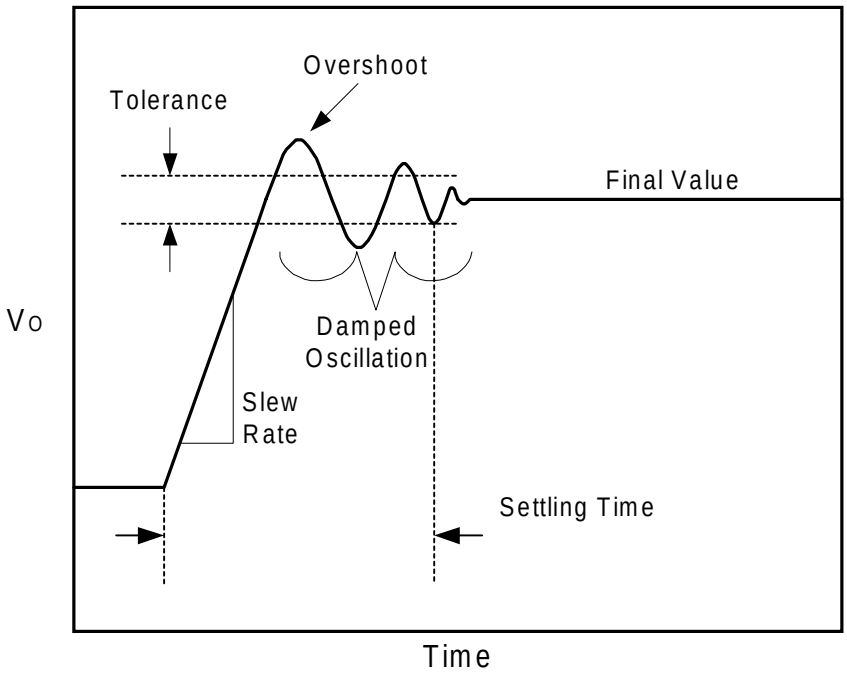
Figure 18. Easier to Read Graph of Voltage Amplification and Phase Shift vs. Frequency



Settling Time

It takes a finite time for a signal to propagate through the internal circuitry of an op amp. Therefore, it takes a certain period of time for the output to react to a step change in the input. Also the output normally overshoots the target value, experiences damped oscillation, and settles to a final value. Settling time, ts, is the time required for the output voltage to settle to within a specified percentage of the final value given a step input. Figure 19 shows this graphically.

Figure 19. Settling Time



Settling time is a design issue in data acquisition circuits when signals are changing rapidly. An example is when using an op amp following a multiplexer to buffer the input to an analog to digital converter. Step changes can occur at the input to the op amp when the multiplexer changes channels. The output of the op amp must settle to within a certain tolerance before the analog to digital converter samples the signal.

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