3-MHz, Low-Power, Low-Noise, RRIO, 1.8-V CMOS Operational Amplifier

Check for Samples: OPA314, OPA2314, OPA4314

FEATURES

- **Low I_Q: 150 µA/ch**
- **Wide Supply Range: 1.8 V to 5.5 V**
- **Low Noise: 14 nV/√Hz at 1 kHz**
- **Gain Bandwidth: 3 MHz**
- **Low Input Bias Current: 0.2 pA**
- **Low Offset Voltage: 0.5 mV**
- **Unity-Gain Stable**
- **Internal RF/EMI Filter**
- **Extended Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Battery-Powered Instruments:**
  - **Consumer, Industrial, Medical**
  - **Notebooks, Portable Media Players**
- **Photodiode Amplifiers**
- **Active Filters**
- **Remote Sensing**
- **Wireless Metering**
- **Handheld Test Equipment**

DESCRIPTION

The OPA314 family of single-, dual-, and quad-channel operational amplifiers represents a new generation of low-power, general-purpose CMOS amplifiers. Rail-to-rail input and output swings, low quiescent current (150 µA typ at 5.0 V_S) combined with a wide bandwidth of 3 MHz, and very low noise (14 nV/√Hz at 1 kHz) make this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance. The low input bias current supports applications with mega-ohm source impedances.

The robust design of the OPA314 devices provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 300 pF, an integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

These devices are optimized for low-voltage operation as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V), and are specified over the full extended temperature range of –40°C to +125°C.

The OPA314 (single) is available in both SC70-5 and SOT23-5 packages. The OPA2314 (dual) is offered in SO-8, MSOP-8, and DFN-8 packages. The quad-channel OPA4314 is offered in a TSSOP-14 package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA314	SC70-5	DCK	SAA
	SOT23-5	DBV	RAZ
OPA2314	SO-8	D	O2314
	MSOP-8	DGK	OCPQ
	DFN-8	DRB	QXY
OPA4314	TSSOP-14	PW	OPA4314

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA314, OPA2314, OPA4314	UNIT
Supply voltage		7	V
Signal input terminals	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output short-circuit(3)		Continuous	mA
Operating temperature, T_A		–40 to +150	°C
Storage temperature, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+150	°C
ESD rating	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V(1)

Boldface limits apply over the specified temperature range: **T_A = –40°C to +125°C**.
At T_A = +25 °C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA314, OPA2314, OPA4314			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = (V_S+) – 1.3 V		0.5	2.5	mV
dV_{OS}/dT	**vs Temperature**			**1**		**µV/°C**
PSRR	vs power supply	V_{CM} = (V_S+) – 1.3 V	78	92		dB
	Over temperature		**74**			**dB**
	Channel separation, dc	At dc		10		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V to 5.5 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V	75	96		dB
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V(2)	66	80		dB
	Over temperature	**V_S = 1.8 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V**	**70**	**86**		**dB**
		V_S = 5.5 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V	**73**	**90**		**dB**
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V(2)	**60**			**dB**
INPUT BIAS CURRENT						
I_B	Input bias current			±0.2	±10	pA
	Over temperature				**±600**	**pA**
I_{OS}	Input offset current			±0.2	±10	pA
	Over temperature				**±600**	**pA**
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		5		μV_{PP}
e_n	Input voltage noise density	f = 10 kHz		13		$nV/\sqrt{Hz}$
		f = 1 kHz		14		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		5		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{IN}	Differential	V_S = 5.0 V		1		pF
	Common-mode	V_S = 5.0 V		5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	90	115		dB
		V_S = 5.5 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	100	128		dB
		V_S = 1.8 V, 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ(2)	90	100		dB
		V_S = 5.5 V, 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ(2)	94	110		dB
	Over temperature	**V_S = 5.5 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ**	**90**	**110**		**dB**
		V_S = 5.5 V, 0.5 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ		**100**		**dB**
	Phase margin	V_S = 5.0 V, G = +1, R_L = 10 kΩ		65		deg

(1) Parameters with minimum or maximum specification limits are 100% production tested at +25ºC, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V[1] (continued)

Boldface limits apply over the specified temperature range: **T_A = –40°C to +125°C**.
At T_A = +25 °C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA314, OPA2314, OPA4314			UNIT
			MIN	TYP	MAX	
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 1.8 V, R_L = 10 kΩ, C_L = 10 pF		2.7		MHz
		V_S = 5.0 V, R_L = 10 kΩ, C_L = 10 pF		3		MHz
SR	Slew rate[3]	V_S = 5.0 V, G = +1		1.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5.0 V, 2-V step , G = +1		2.3		µs
		To 0.01%, V_S = 5.0V, 2-V step , G = +1		3.1		µs
	Overload recovery time	V_S = 5.0 V, V_{IN} × Gain > V_S		5.2		µs
THD+N	Total harmonic distortion + noise[4]	V_S = 5.0 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz, R_L = 10 kΩ		0.001		%
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 1.8 V, R_L = 10 kΩ		5	15	mV
		V_S = 5.5 V, R_L = 10 kΩ		5	20	mV
		V_S = 1.8 V, R_L = 2 kΩ		15	30	mV
		V_S = 5.5 V, R_L = 2 kΩ		22	40	mV
	Over temperature	**V_S = 5.5 V, R_L = 10 kΩ**			**30**	**mV**
		V_S = 5.5 V, R_L = 2 kΩ		**60**		**mV**
I_{SC}	Short-circuit current	V_S = 5.0 V		±20		mA
R_O	Open-loop output impedance	V_S = 5.5 V, f = 100 Hz		570		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	OPA314, OPA2314, OPA4314, V_S = 1.8 V, I_O = 0 mA		130	180	µA
		OPA2314, OPA4314, V_S = 5.0 V, I_O = 0 mA		150	190	µA
		OPA314, V_S = 5.0 V, I_O = 0 mA		150	210	µA
	Over temperature	**V_S = 5.0 V, I_O = 0 mA**			**220**	**µA**
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level		44		µs
TEMPERATURE						
	Specified range		–40		+125	°C
	Operating range		–40		+150	°C
	Storage range		–65		+150	°C

(3) Signifies the slower value of the positive or negative slew rate.
(4) Third-order filter; bandwidth = 80 kHz at –3 dB.

THERMAL INFORMATION: OPA314

THERMAL METRIC(1)		OPA314		UNITS
		DBV (SOT23)	DCK (SC70)	
		5 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	228.5	281.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	99.1	91.6	
θ_{JB}	Junction-to-board thermal resistance	54.6	59.6	
ψ_{JT}	Junction-to-top characterization parameter	7.7	1.5	
ψ_{JB}	Junction-to-board characterization parameter	53.8	58.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL INFORMATION: OPA2314

THERMAL METRIC(1)		OPA2314			UNITS
		D (SO)	DGK (MSOP)	DRB (DFN)	
		8 PINS	8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	138.4	191.2	53.8	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	89.5	61.9	69.2	
θ_{JB}	Junction-to-board thermal resistance	78.6	111.9	20.1	
ψ_{JT}	Junction-to-top characterization parameter	29.9	5.1	3.8	
ψ_{JB}	Junction-to-board characterization parameter	78.1	110.2	20.0	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	11.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

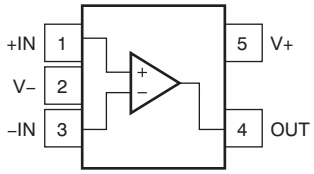
THERMAL INFORMATION: OPA4314

THERMAL METRIC(1)		OPA4314	UNITS
		PW (TSSOP)	
		14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	121.0	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	49.4	
θ_{JB}	Junction-to-board thermal resistance	62.8	
ψ_{JT}	Junction-to-top characterization parameter	5.9	
ψ_{JB}	Junction-to-board characterization parameter	62.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	

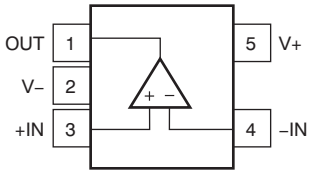
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

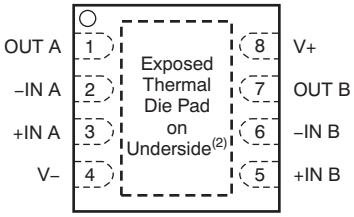
DCK PACKAGE
SC70-5
(TOP VIEW)



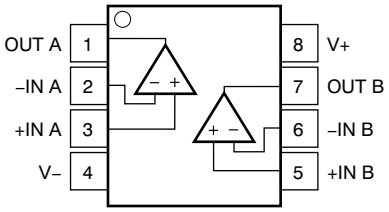
DBV PACKAGE
SOT23-5
(TOP VIEW)



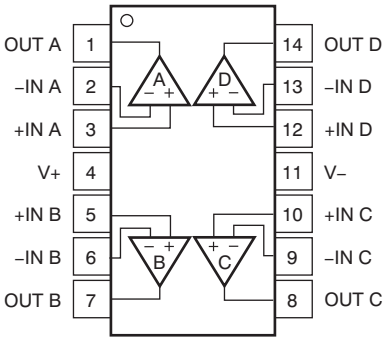
DRB PACKAGE(1)
DFN-8
(TOP VIEW)



D, DGK PACKAGES
SO-8, MSOP-8
(TOP VIEW)



PW PACKAGE
TSSOP-14
(TOP VIEW)



(1) Pitch: 0,65 mm.

(2) Connect thermal pad to V–. Pad size: 1,8 mm × 1,5 mm.

TYPICAL CHARACTERISTICS

Table 1. Characteristic Performance Measurements

TITLE	FIGURE
Open-Loop Gain and Phase vs Frequency	Figure 1
Open-Loop Gain vs Temperature	Figure 2
Quiescent Current vs Supply Voltage	Figure 3
Quiescent Current vs Temperature	Figure 4
Offset Voltage Production Distribution	Figure 5
Offset Voltage Drift Distribution	Figure 6
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	Figure 7
Offset Voltage vs Temperature	Figure 8
CMRR and PSRR vs Frequency (RTI)	Figure 9
CMRR and PSRR vs Temperature	Figure 10
0.1-Hz to 10-Hz Input Voltage Noise (5.5 V)	Figure 11
Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V)	Figure 12
Input Voltage Noise vs Common-Mode Voltage (5.5 V)	Figure 13
Input Bias and Offset Current vs Temperature	Figure 14
Open-Loop Output Impedance vs Frequency	Figure 15
Maximum Output Voltage vs Frequency and Supply Voltage	Figure 16
Output Voltage Swing vs Output Current (over Temperature)	Figure 17
Closed-Loop Gain vs Frequency, G = 1, –1, 10 (1.8 V)	Figure 18
Closed-Loop Gain vs Frequency, G = 1, –1, 10 (5.5 V)	Figure 19
Small-Signal Overshoot vs Load Capacitance	Figure 20
Small-Signal Step Response, Noninverting (1.8 V)	Figure 21
Small-Signal Step Response, Noninverting (5.5 V)	Figure 22
Large-Signal Step Response, Noninverting (1.8 V)	Figure 23
Large-Signal Step Response, Noninverting (5.5 V)	Figure 24
Positive Overload Recovery	Figure 25
Negative Overload Recovery	Figure 26
No Phase Reversal	Figure 27
Channel Separation vs Frequency (Dual)	Figure 28
THD+N vs Amplitude (G = +1, 2 kΩ, 10 kΩ)	Figure 29
THD+N vs Amplitude (G = –1, 2 kΩ, 10 kΩ)	Figure 30
THD+N vs Frequency (0.5 V_{RMS}, G = +1, 2 kΩ, 10 kΩ)	Figure 31
EMIRR	Figure 32

TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

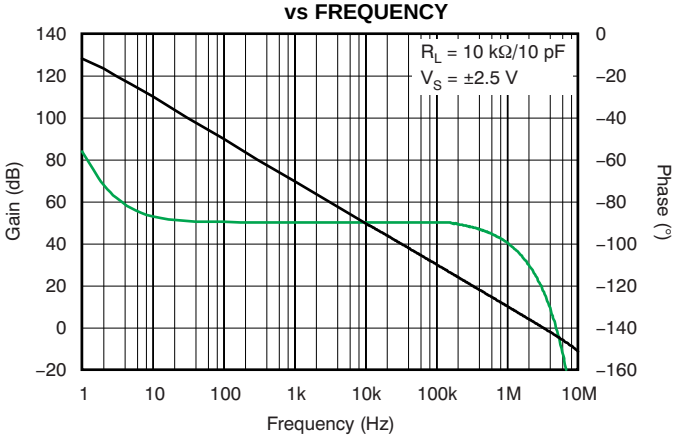


Figure 1.

OPEN-LOOP GAIN vs TEMPERATURE

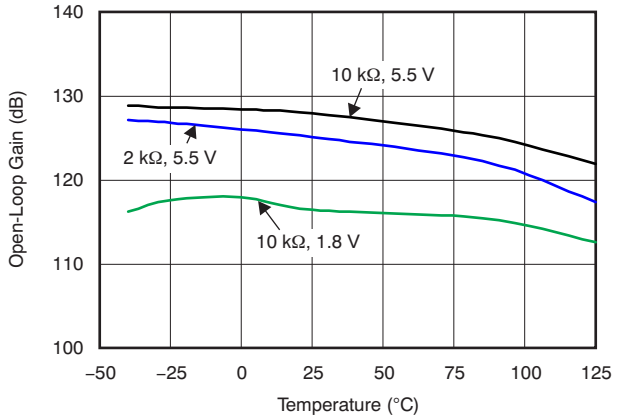


Figure 2.

QUIESCENT CURRENT vs SUPPLY

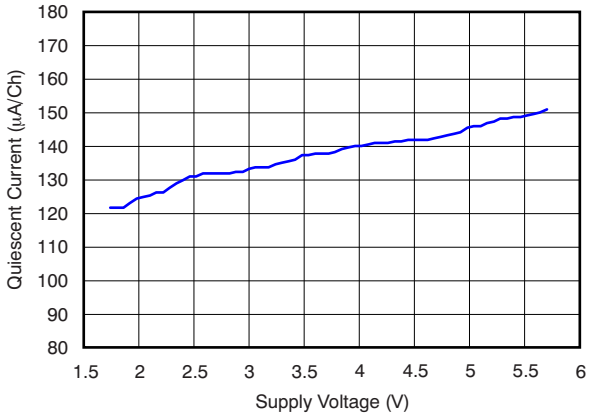


Figure 3.

QUIESCENT CURRENT vs TEMPERATURE

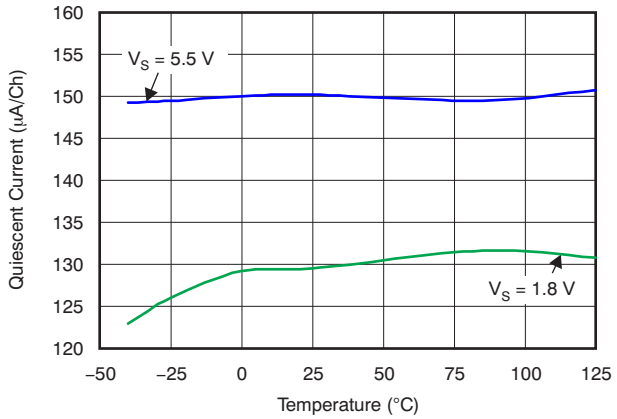


Figure 4.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

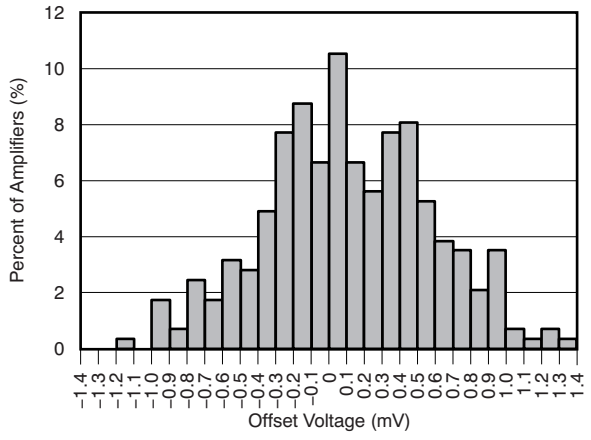


Figure 5.

OFFSET VOLTAGE DRIFT DISTRIBUTION

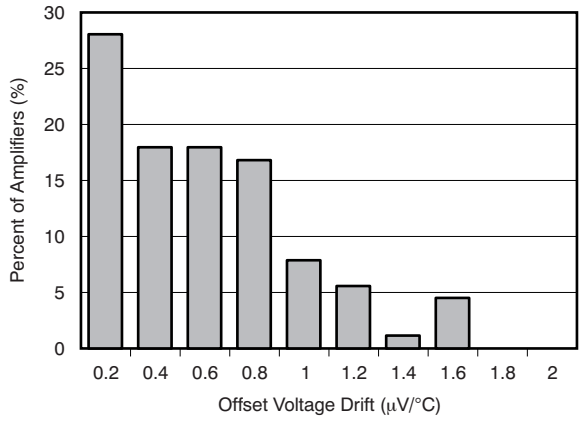


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

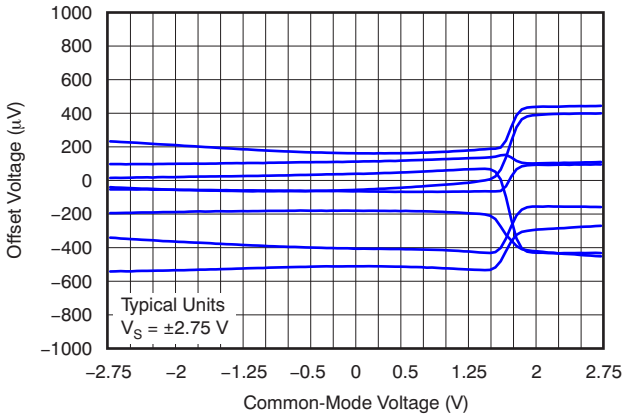


Figure 7.

OFFSET VOLTAGE vs TEMPERATURE

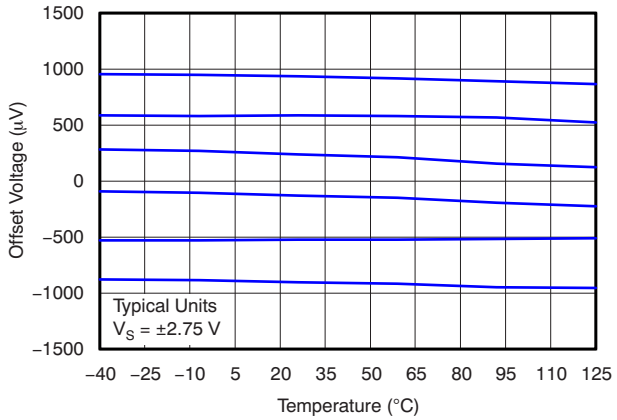


Figure 8.

CMRR AND PSRR vs FREQUENCY (Referred-to-Input)

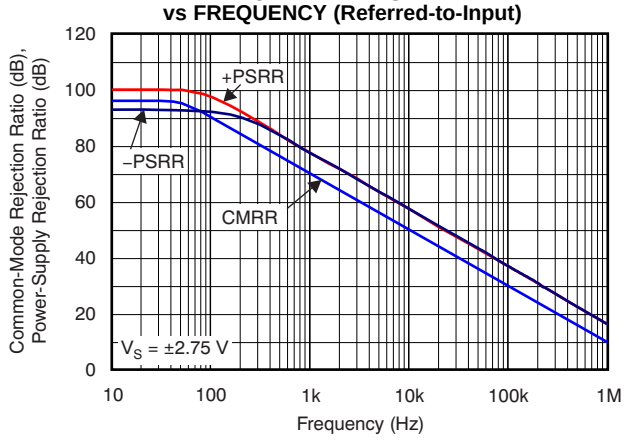


Figure 9.

CMRR AND PSRR vs TEMPERATURE

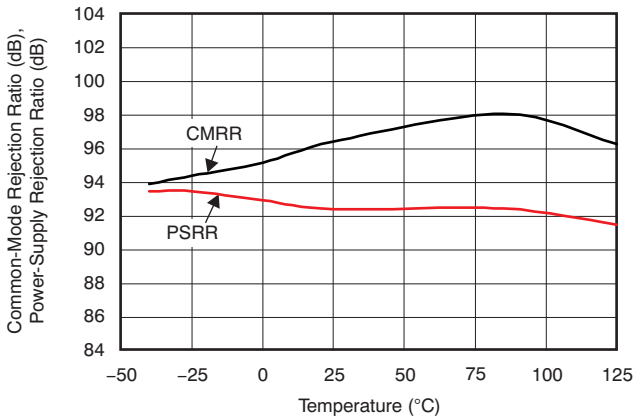


Figure 10.

0.1-Hz to 10-Hz INPUT VOLTAGE NOISE

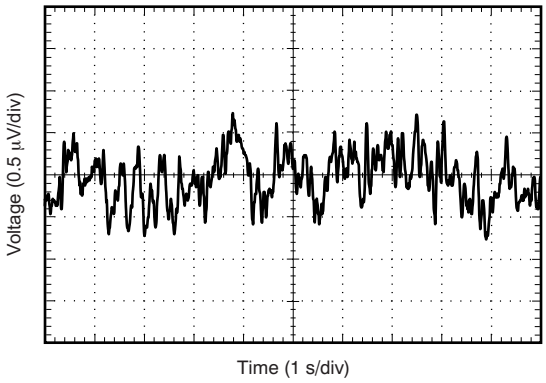


Figure 11.

INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

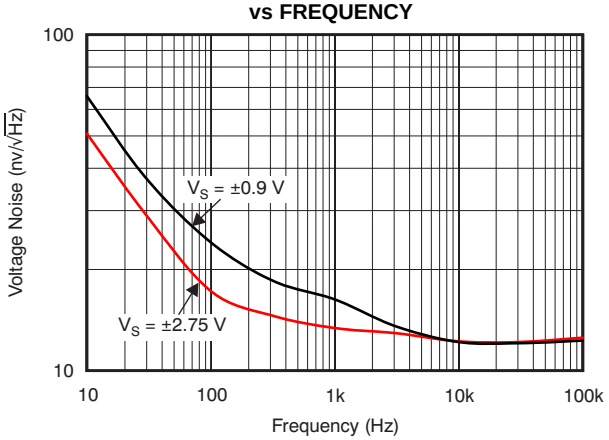


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

VOLTAGE NOISE vs COMMON-MODE VOLTAGE

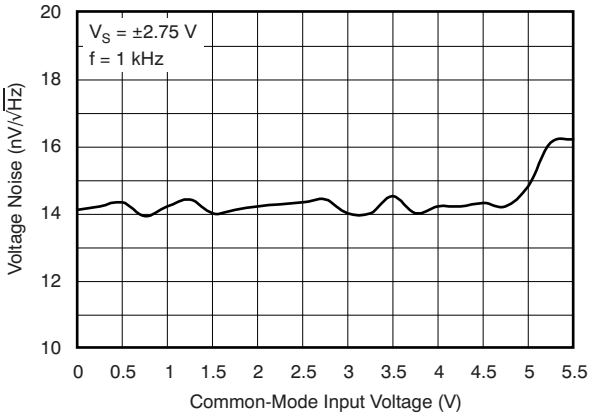


Figure 13.

INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

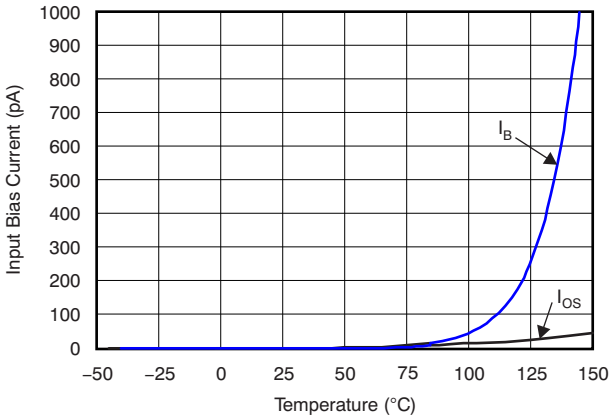


Figure 14.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

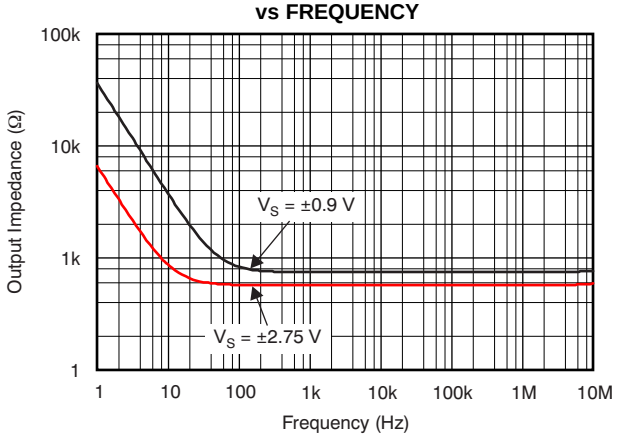


Figure 15.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY AND SUPPLY VOLTAGE

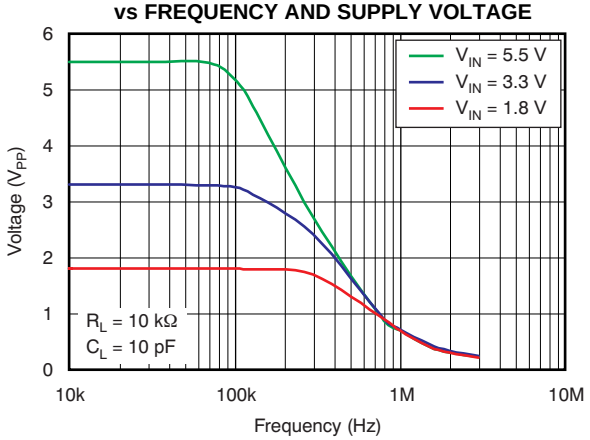


Figure 16.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (Over Temperature)

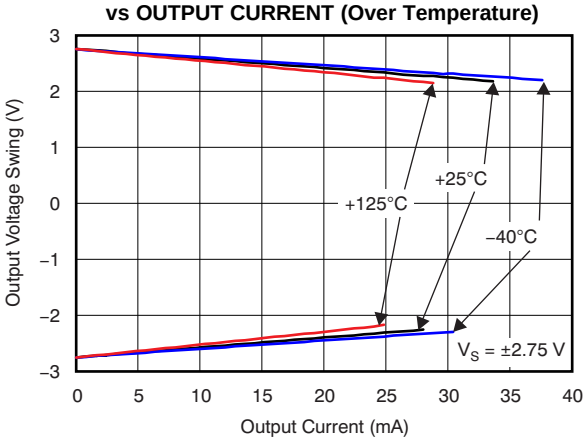


Figure 17.

CLOSED-LOOP GAIN vs FREQUENCY

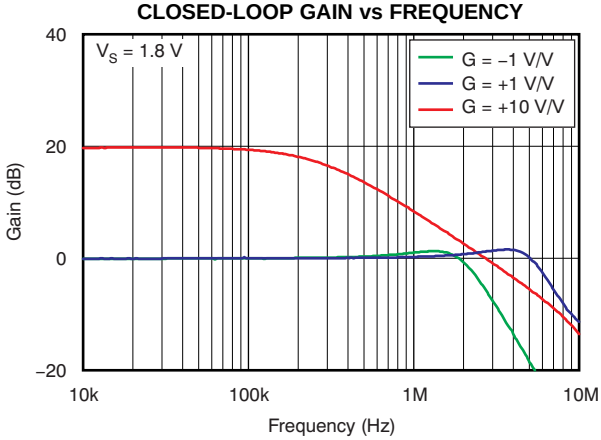


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

CLOSED-LOOP GAIN vs FREQUENCY

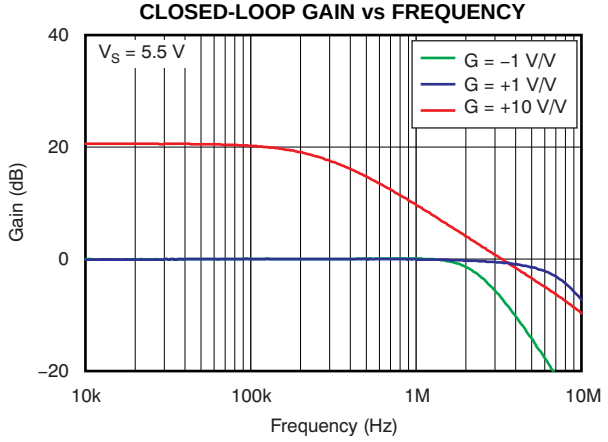


Figure 19.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

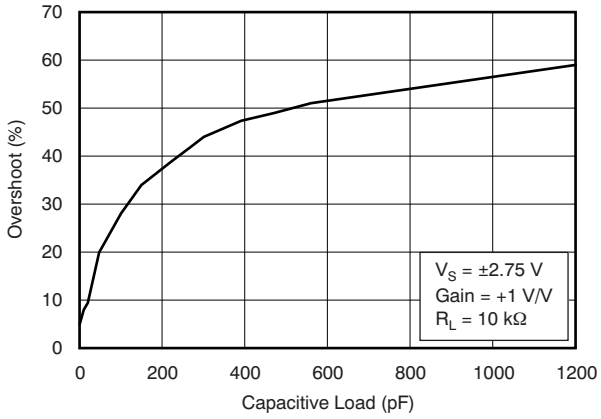


Figure 20.

SMALL-SIGNAL PULSE RESPONSE (Noninverting)

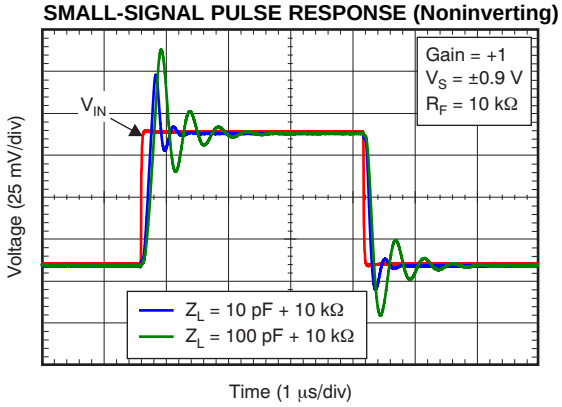


Figure 21.

SMALL-SIGNAL PULSE RESPONSE (Inverting)

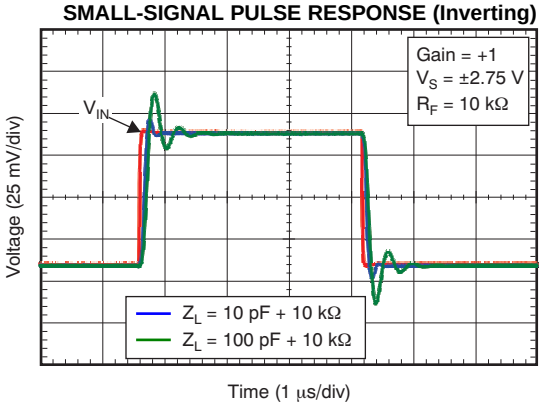


Figure 22.

LARGE-SIGNAL PULSE RESPONSE (Noninverting)

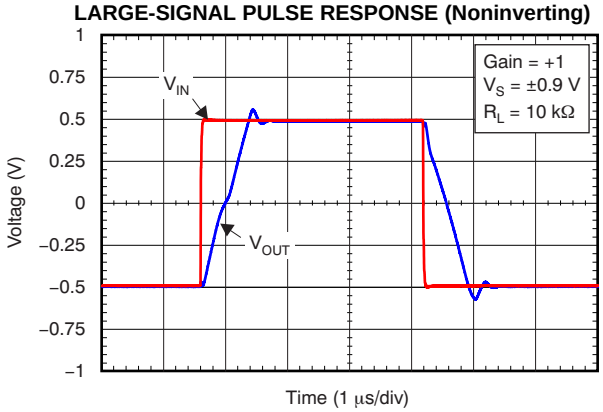


Figure 23.

LARGE-SIGNAL PULSE RESPONSE (Inverting)

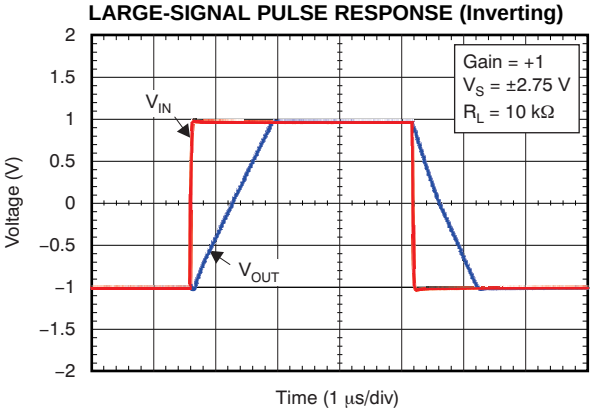


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

POSITIVE OVERLOAD RECOVERY

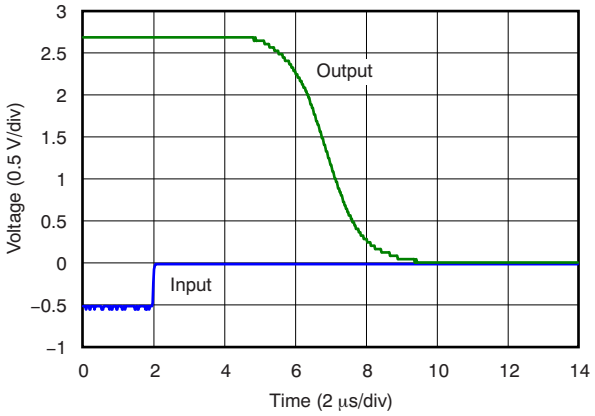


Figure 25.

NEGATIVE OVERLOAD RECOVERY

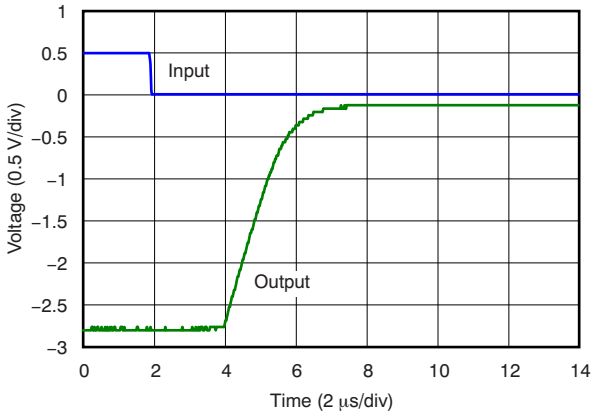


Figure 26.

NO PHASE REVERSAL

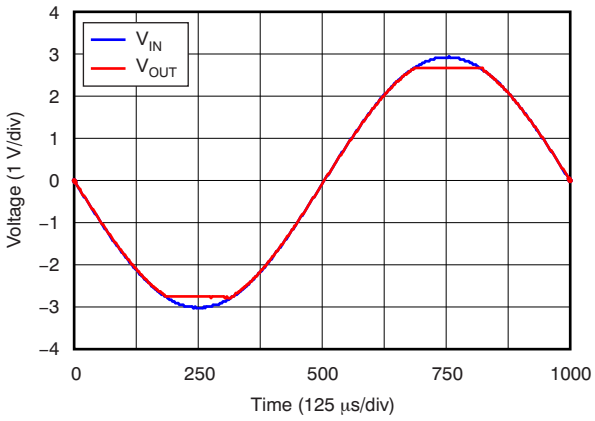


Figure 27.

CHANNEL SEPARATION vs FREQUENCY OPA2314

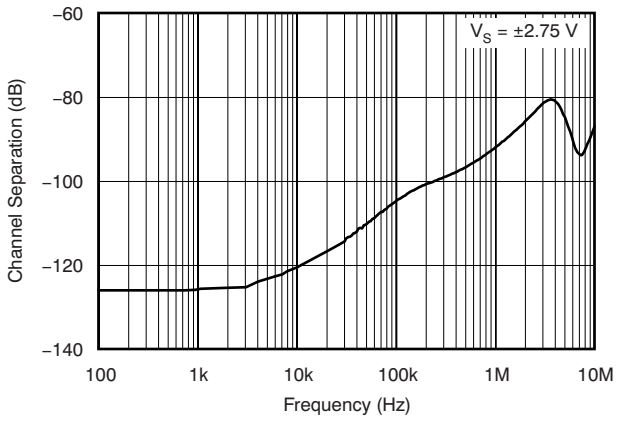


Figure 28.

THD+N vs OUTPUT AMPLITUDE (G = +1 V/V)

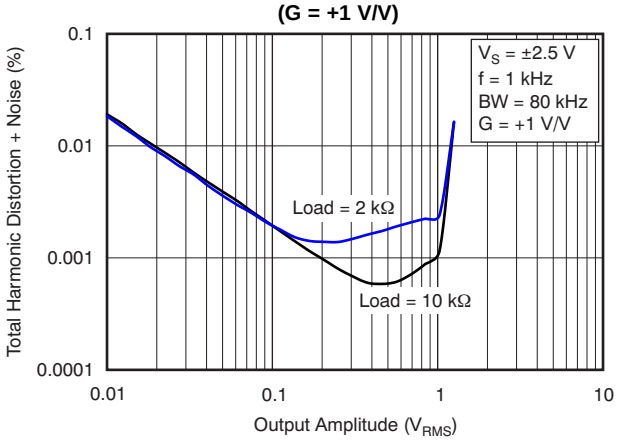


Figure 29.

THD+N vs OUTPUT AMPLITUDE (G = –1 V/V)

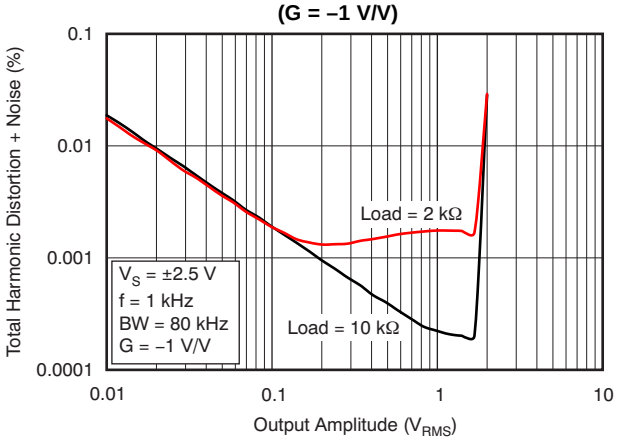


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

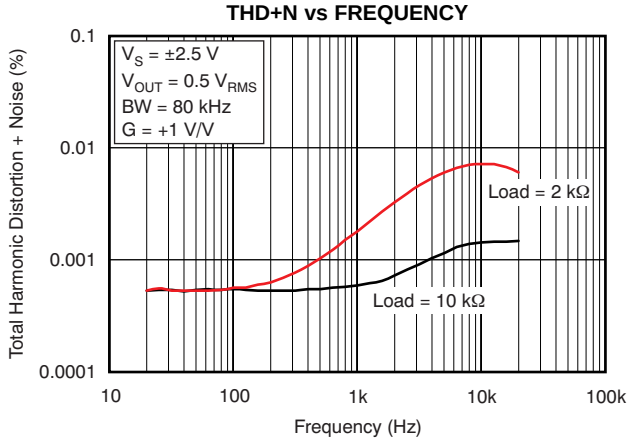


Figure 31.

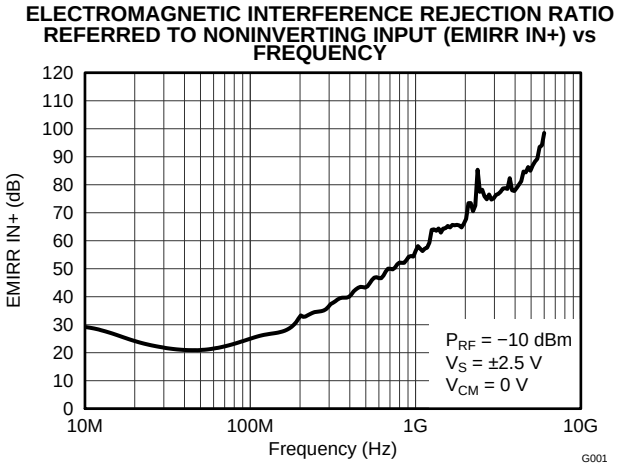


Figure 32.

APPLICATION INFORMATION

The OPA314 is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA314 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The OPA314 features 3-MHz bandwidth and 1.5-V/μs slew rate with only 150-μA supply current per channel, providing good ac performance at very low power consumption. DC applications are also well served with a very low input noise voltage of 14 nV/√Hz at 1 kHz, low input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical).

OPERATING VOLTAGE

The OPA314 series op amps are fully specified and ensured for operation from +1.8 V to +5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics graphs. Power-supply pins should be bypassed with 0.01-μF ceramic capacitors.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA314 series extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 33. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region can vary up to 300 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

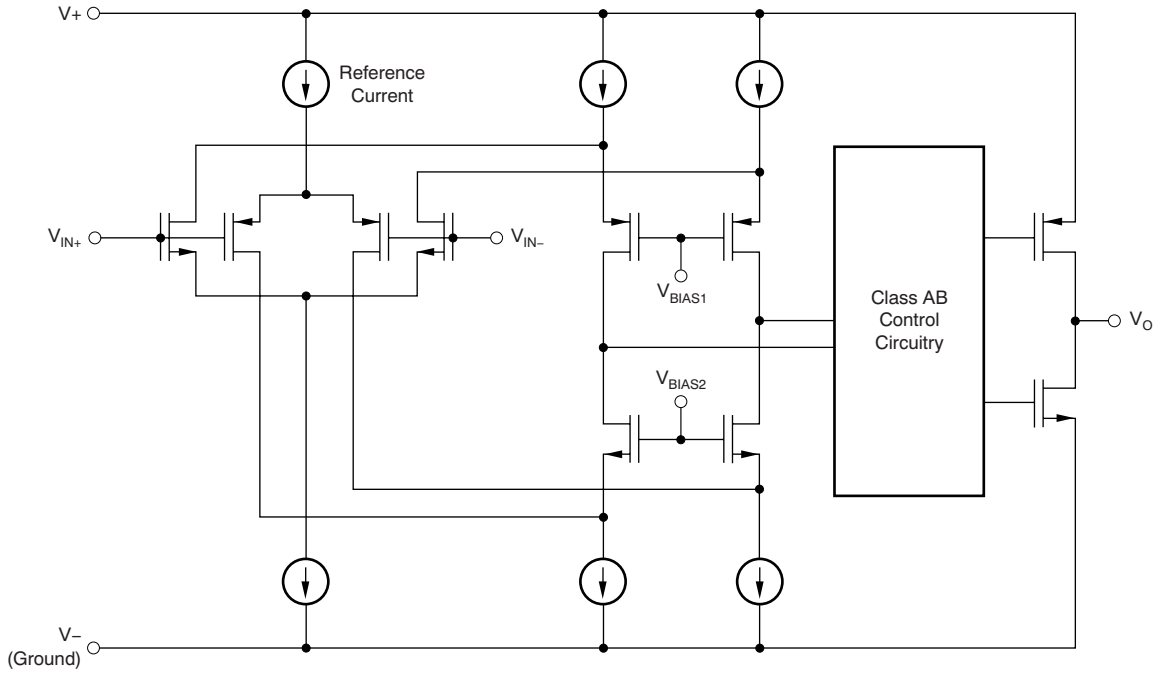


Figure 33. Simplified Schematic

INPUT AND ESD PROTECTION

The OPA314 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings. Figure 34 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

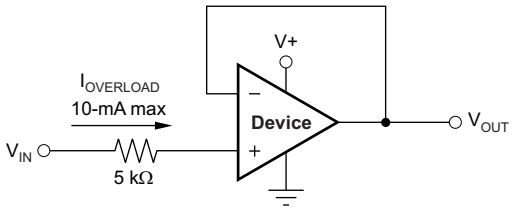


Figure 34. Input Current Protection

COMMON-MODE REJECTION RATIO (CMRR)

CMRR for the OPA314 is specified in several ways so the best match for a given application may be used; see the Electrical Characteristics. First, the CMRR of the device in the common-mode range below the transition region [V_{CM} < (V+) – 1.3 V] is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (V_{CM} = –0.2 V to 5.7 V). This last value includes the variations seen through the transition region (see Figure 7).

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the dc offset observed at the amplifier output may shift from its nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The OPA314 operational amplifier family incorporate an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Figure 32 illustrates the results of this testing on the OPAx314. Detailed information can also be found in the application report, *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

RAIL-TO-RAIL OUTPUT

Designed as a micro-power, low-noise operational amplifier, the OPA314 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; refer to the typical characteristic graph, *Output Voltage Swing vs Output Current*.

CAPACITIVE LOAD AND STABILITY

The OPA314 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA314 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op amp in the unity-gain (+1-V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA314 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the typical characteristic graph, *Small-Signal Overshoot vs. Capacitive Load*.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 35. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

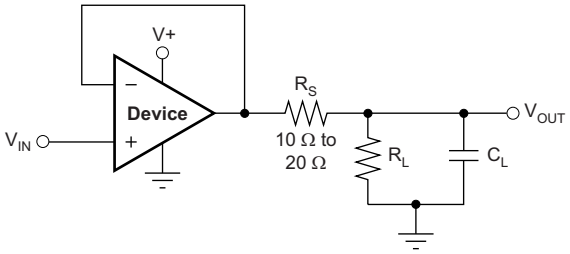


Figure 35. Improving Capacitive Load Drive

DFN PACKAGE

The OPA2314 (dual version) uses the DFN style package (also known as SON); this package is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes printed circuit board (PCB) space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low, 0.9-mm height. DFN packages are physically small, have a smaller routing area, improved thermal performance, reduced electrical parasitics, and use a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can easily be mounted using standard PCB assembly techniques. See Application Note, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download from www.ti.com.

NOTE

The exposed leadframe die pad on the bottom of the DFN package should be connected to the most negative potential (V–).

APPLICATION EXAMPLES

GENERAL CONFIGURATIONS

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as Figure 36 shows.

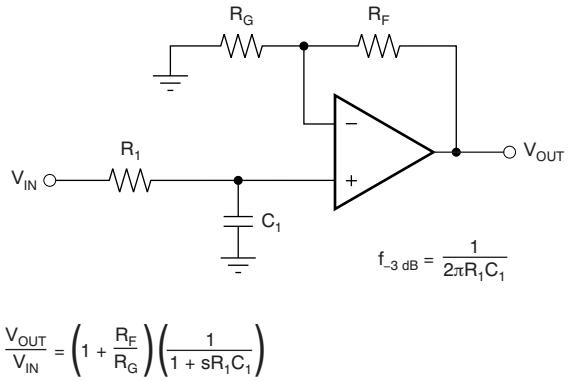


Figure 36. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as Figure 37 shows. For best results, the amplifier should have a bandwidth that is eight to 10 times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

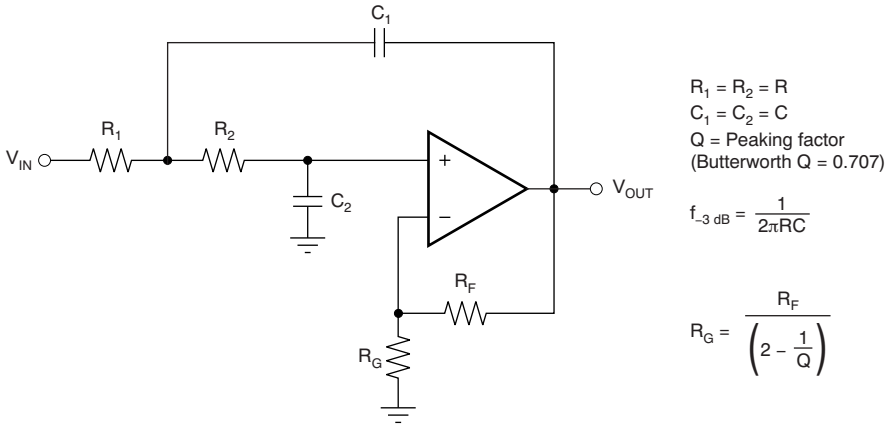


Figure 37. Two-Pole Low-Pass Sallen-Key Filter

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2012) to Revision F — **Page**

- Changed document title (removed "Value Line Series") 1

Changes from Revision D (March 2012) to Revision E — **Page**

- Added "Value Line Series" to title 1

Changes from Revision C (February 2012) to Revision D — **Page**

- Changed product status from mixed status to production data 1
- Deleted shading and footnote 2 from Package Information table 2

Changes from Revision B (December 2011) to Revision C — **Page**

- Changed first Features bullet 1
- Deleted shading from OPA314 SOT23-5 row (DBV package) in Package Information table 2
- Added OPA2314, OPA4314 to first two Power Supply, *Quiescent current per amplifier* parameter rows in Electrical Characteristics table 4
- Added OPA314 Power Supply, *Quiescent current per amplifier* parameter row to Electrical Characteristics table 4

Changes from Revision A (August 2011) to Revision B — **Page**

- Deleted shading from OPA2314 MSOP-8 row in Package Information table 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA2314AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2314	Samples
OPA2314AIDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OCPQ	Samples
OPA2314AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OCPQ	Samples
OPA2314AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2314	Samples
OPA2314AIDRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXY	Samples
OPA2314AIDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXY	Samples
OPA314AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAZ	Samples
OPA314AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAZ	Samples
OPA314AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SAA	Samples
OPA314AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SAA	Samples
OPA4314AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4314	Samples
OPA4314AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4314	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF OPA2314 :

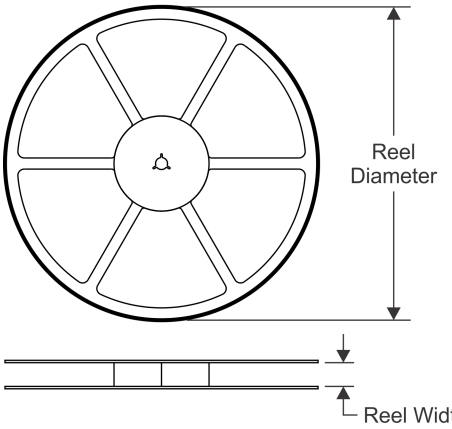
- Enhanced Product: OPA2314-EP

NOTE: Qualified Version Definitions:

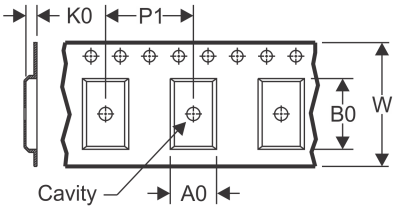
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

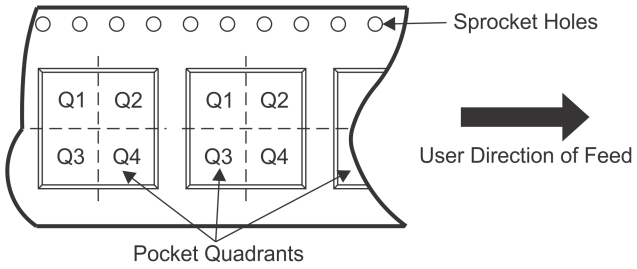


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

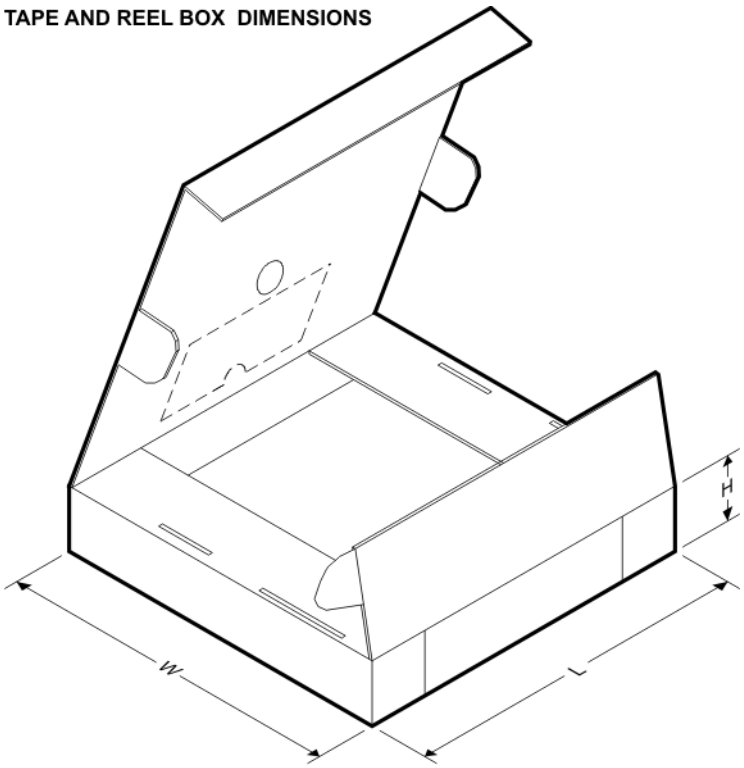
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2314AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2314AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2314AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2314AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA314AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA314AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA314AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA4314AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

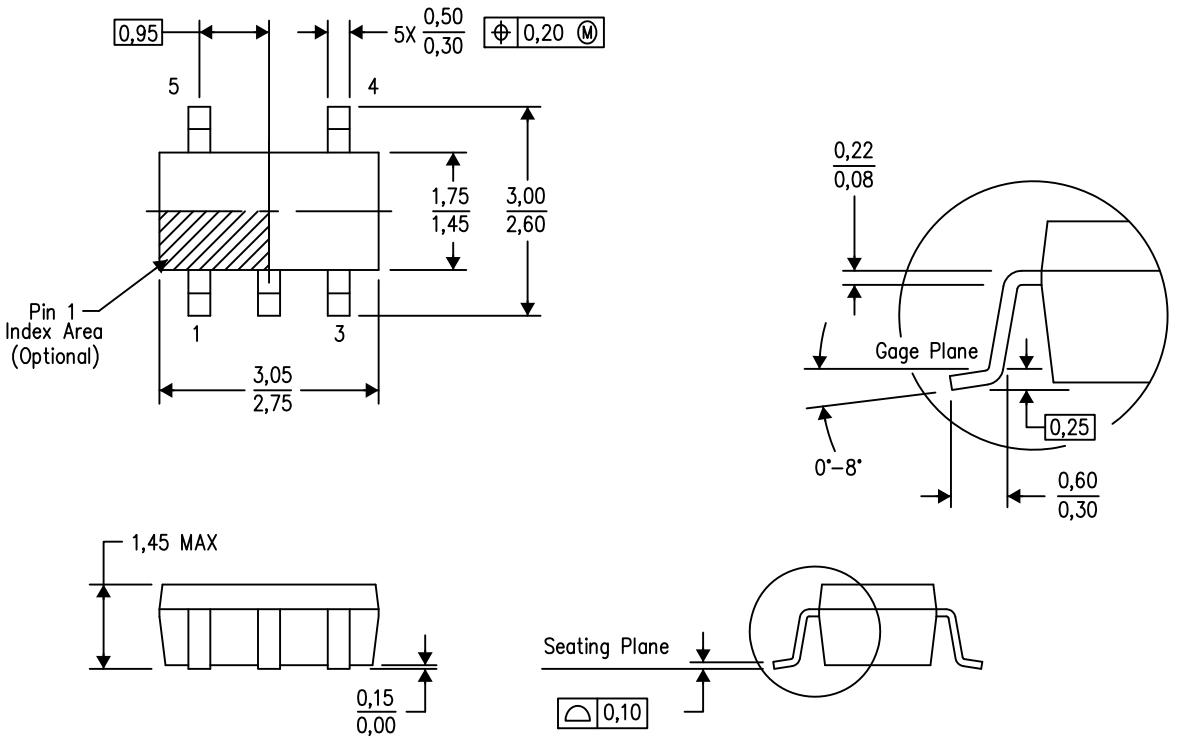
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2314AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2314AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2314AIDRBR	SON	DRB	8	3000	367.0	367.0	35.0
OPA2314AIDRBT	SON	DRB	8	250	210.0	185.0	35.0
OPA314AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA314AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA314AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA4314AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

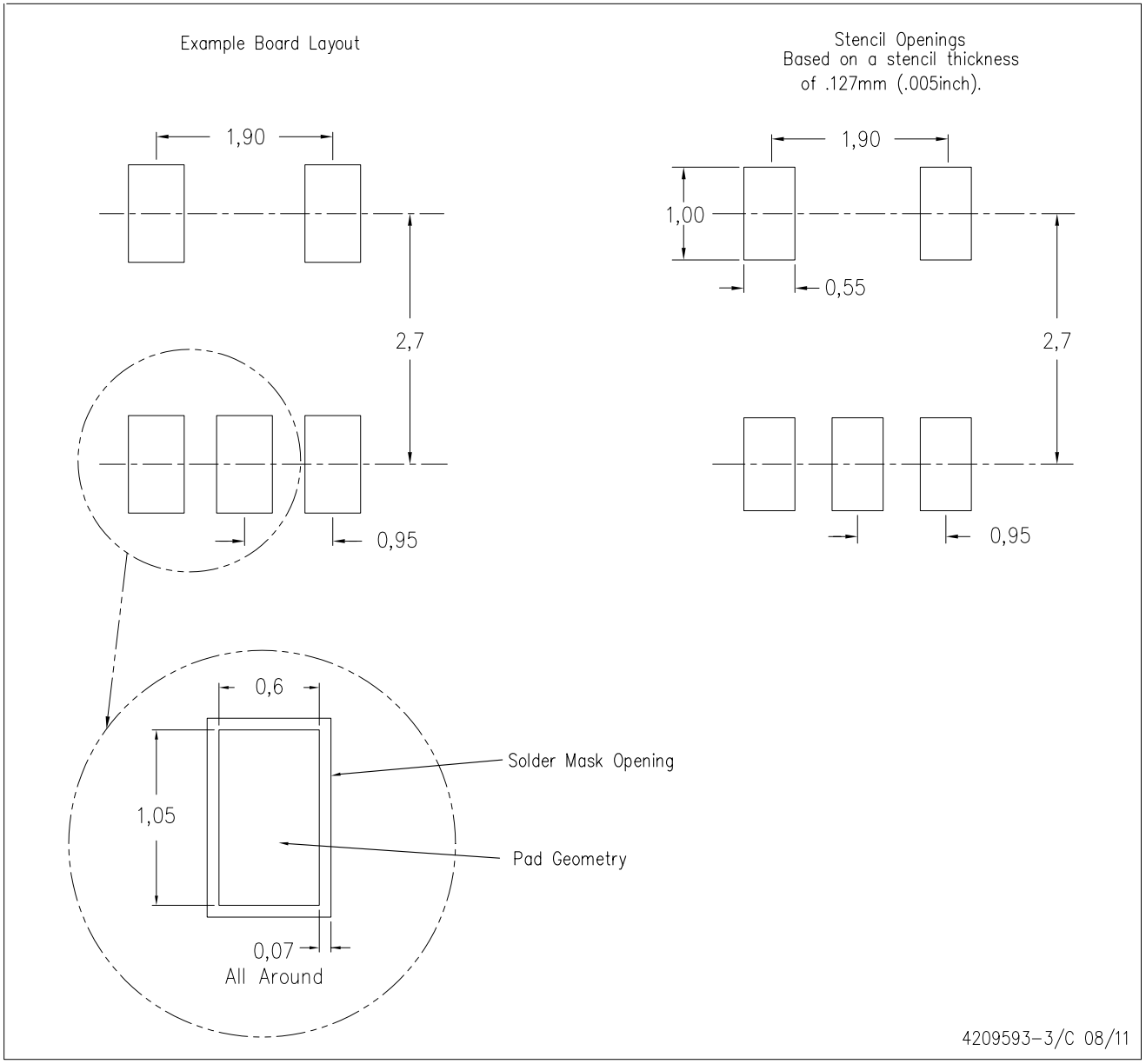
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

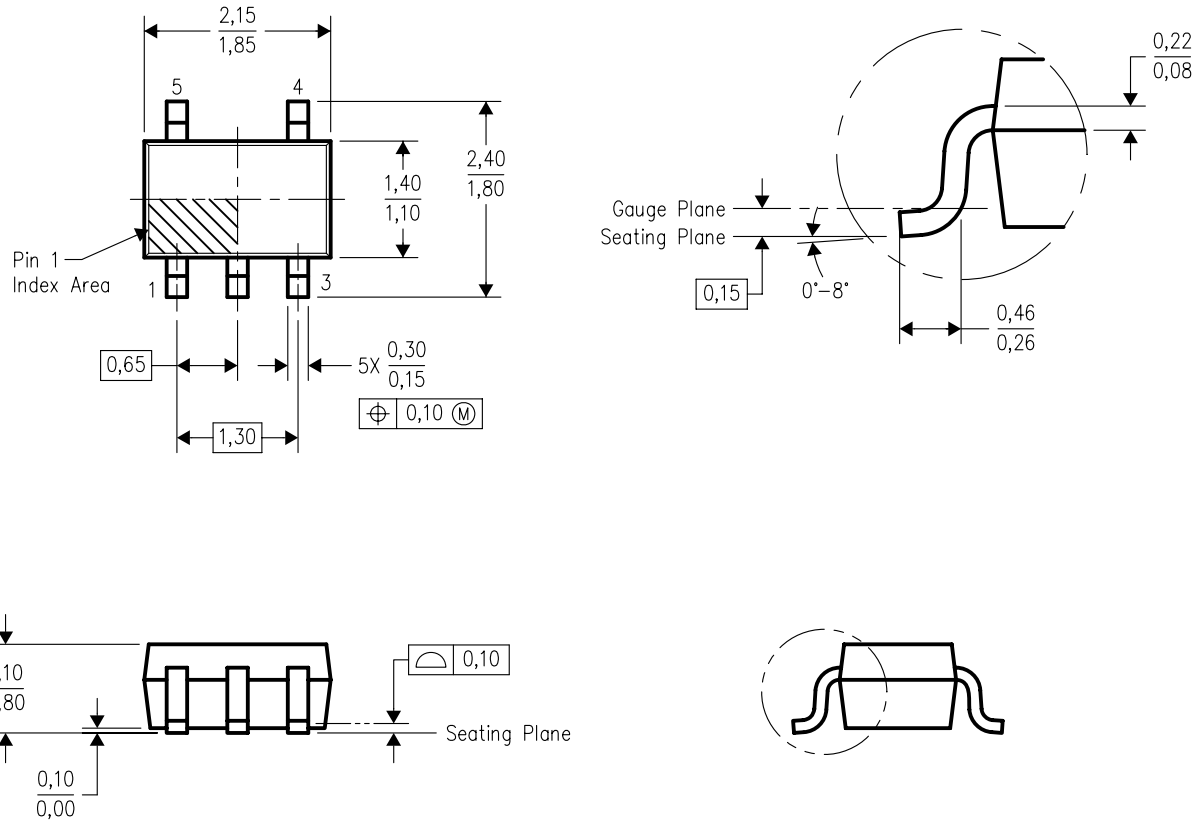
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

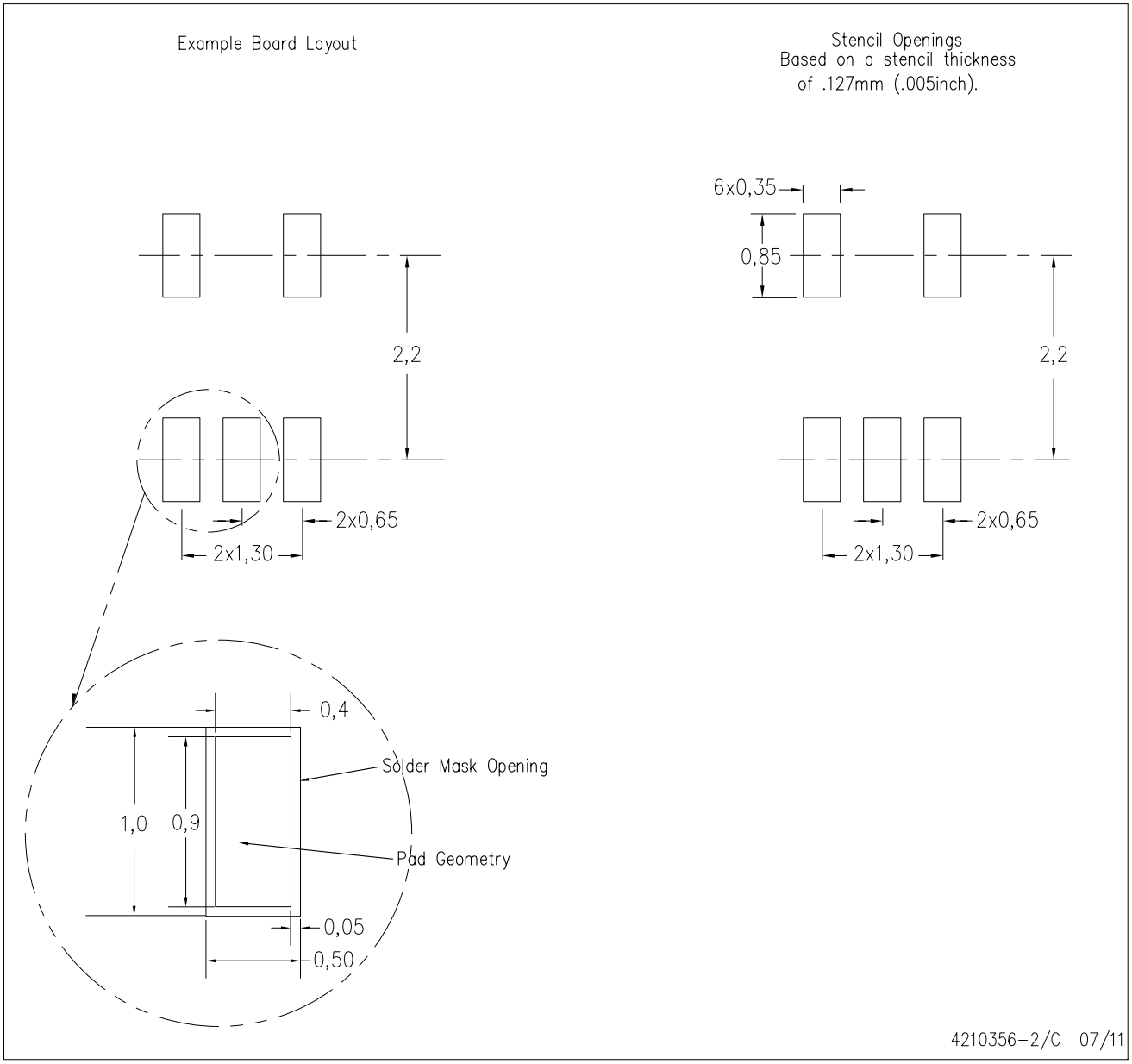
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

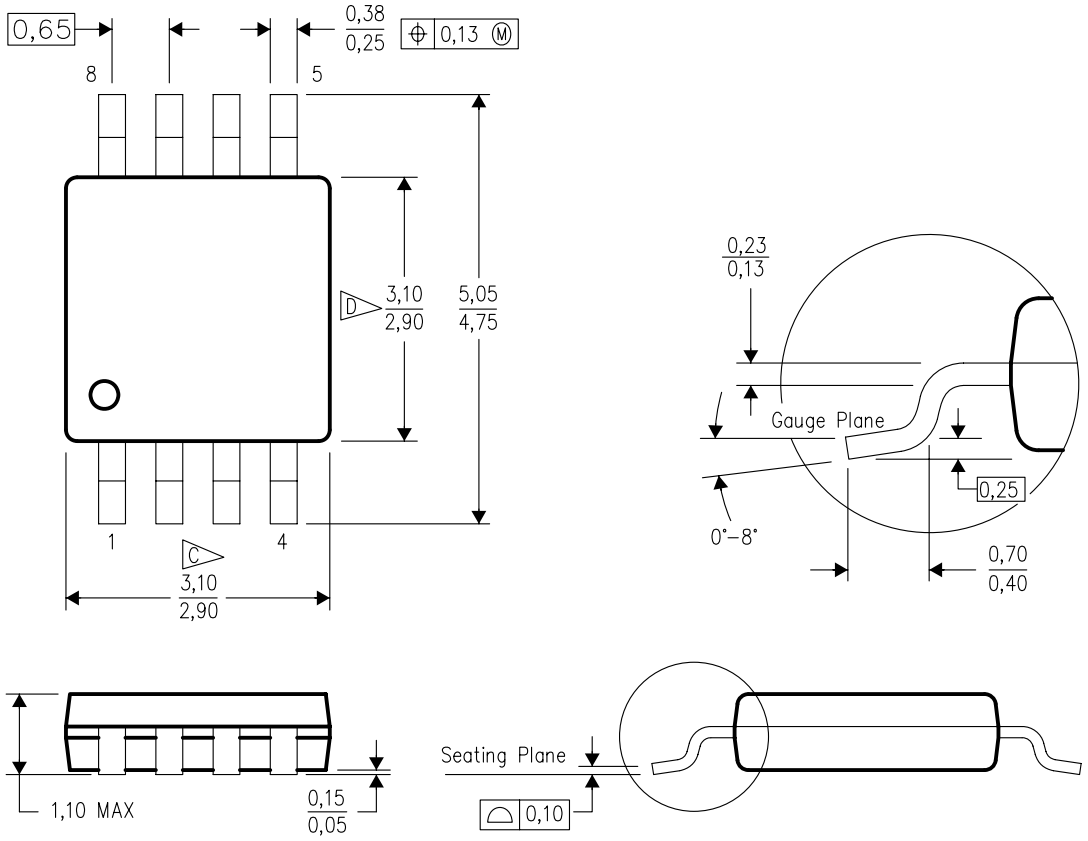
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

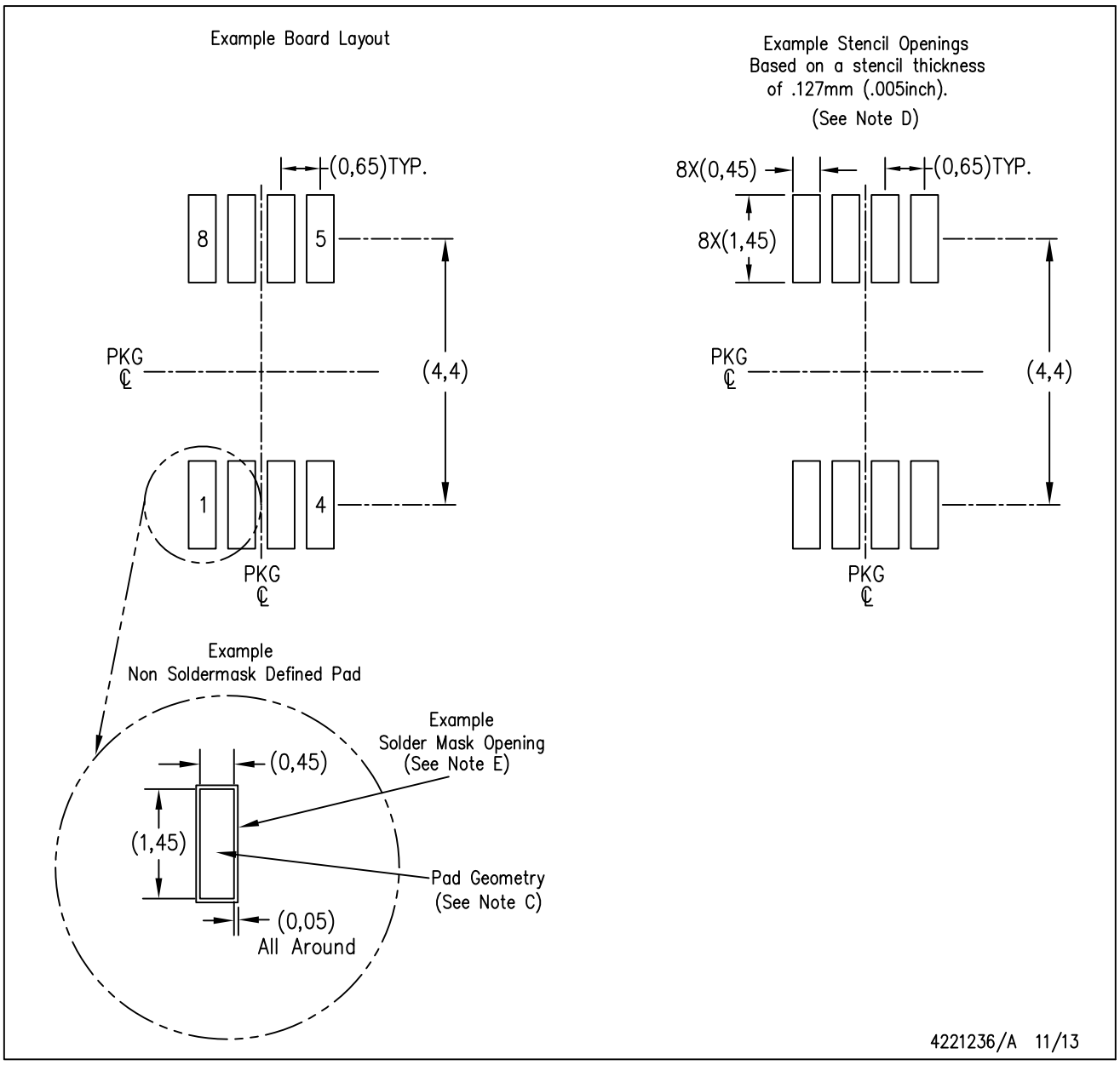
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

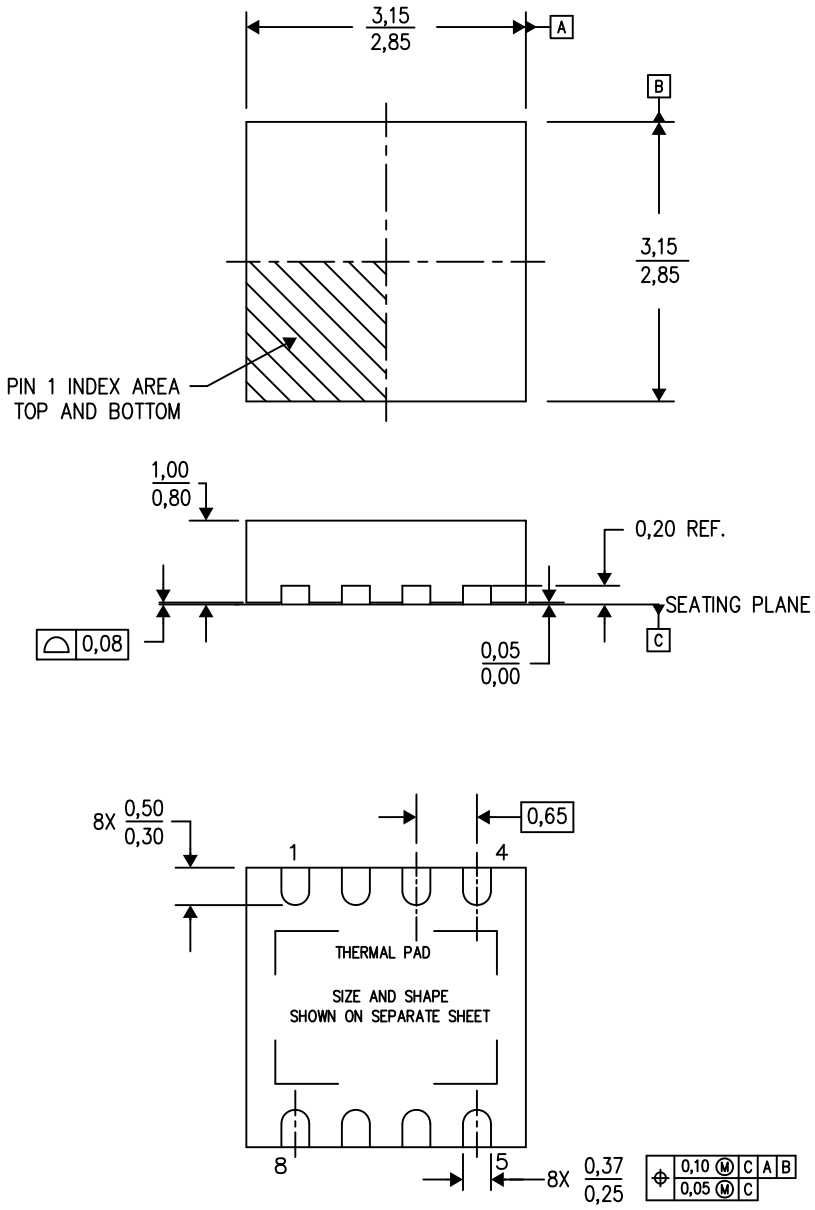
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

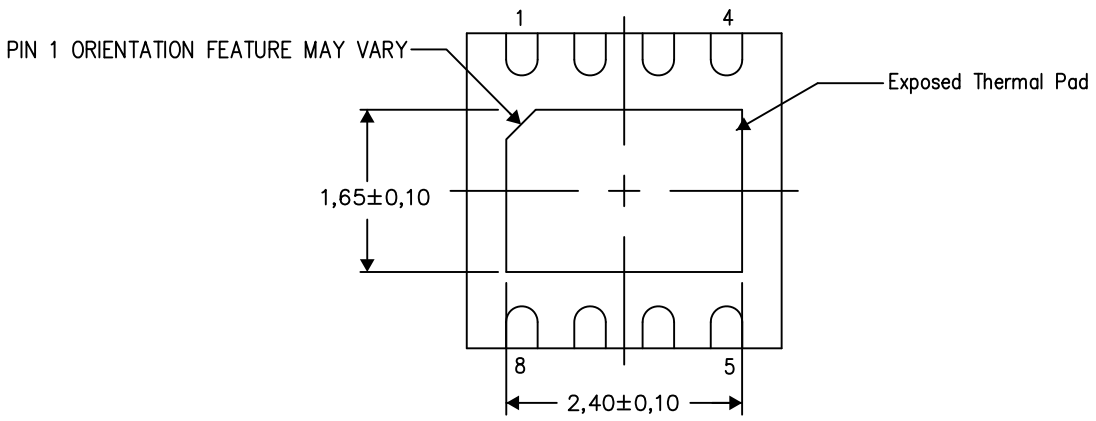
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



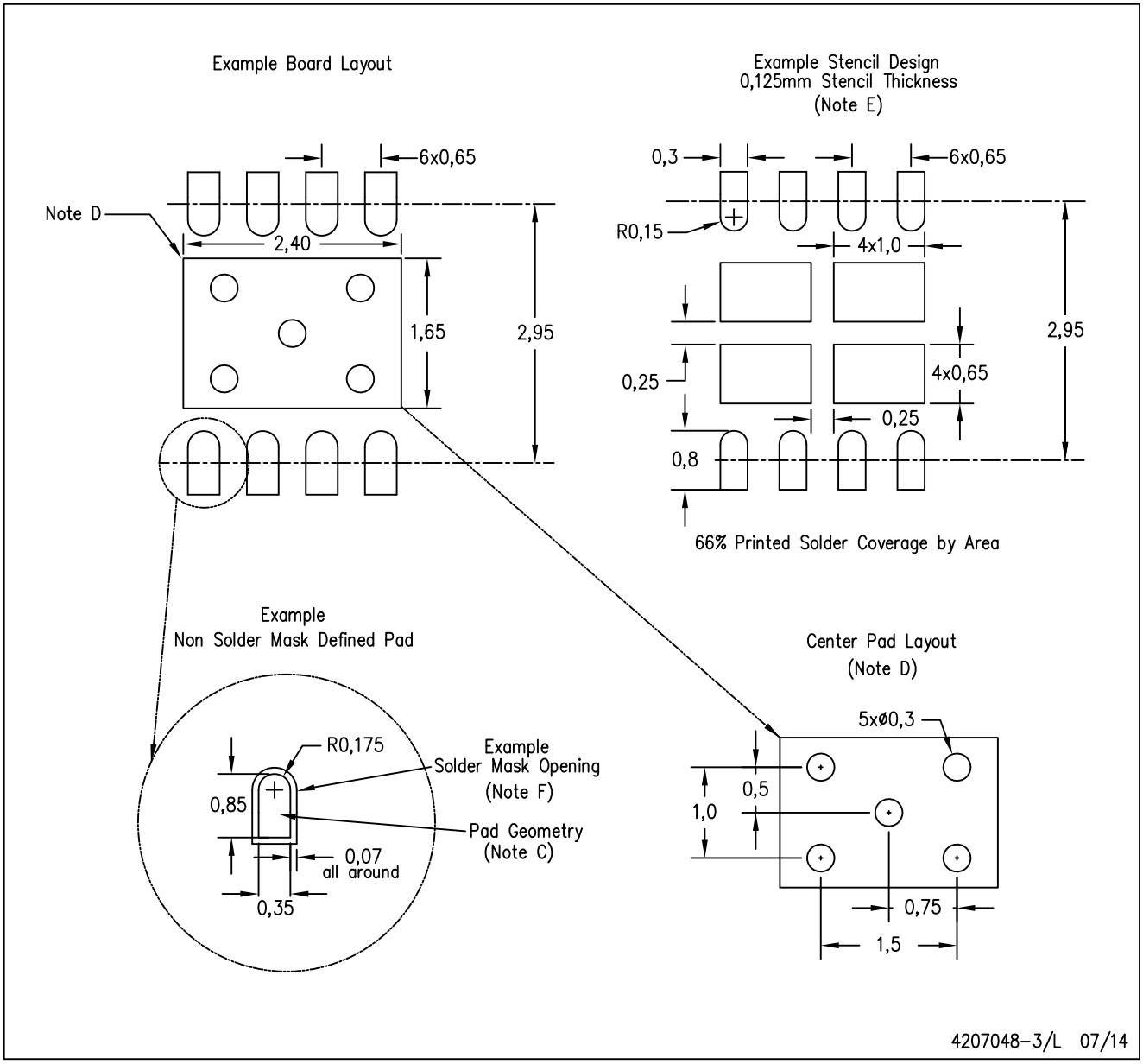
Bottom View

Exposed Thermal Pad Dimensions

4206340–3/P 07/14

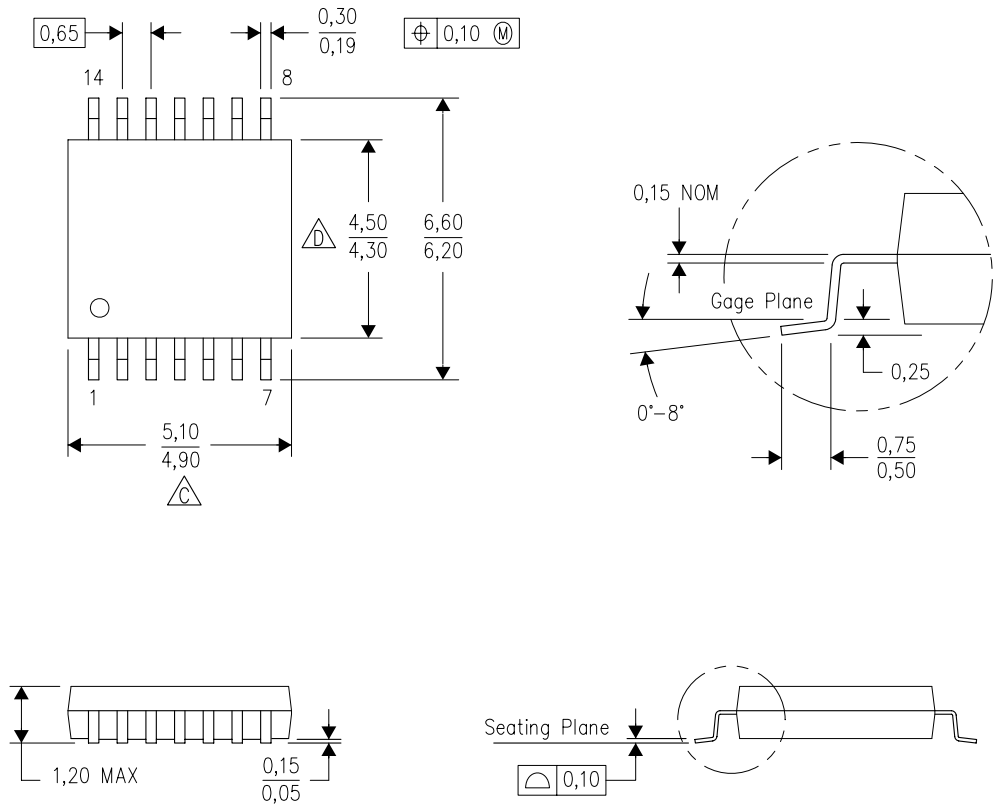
NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

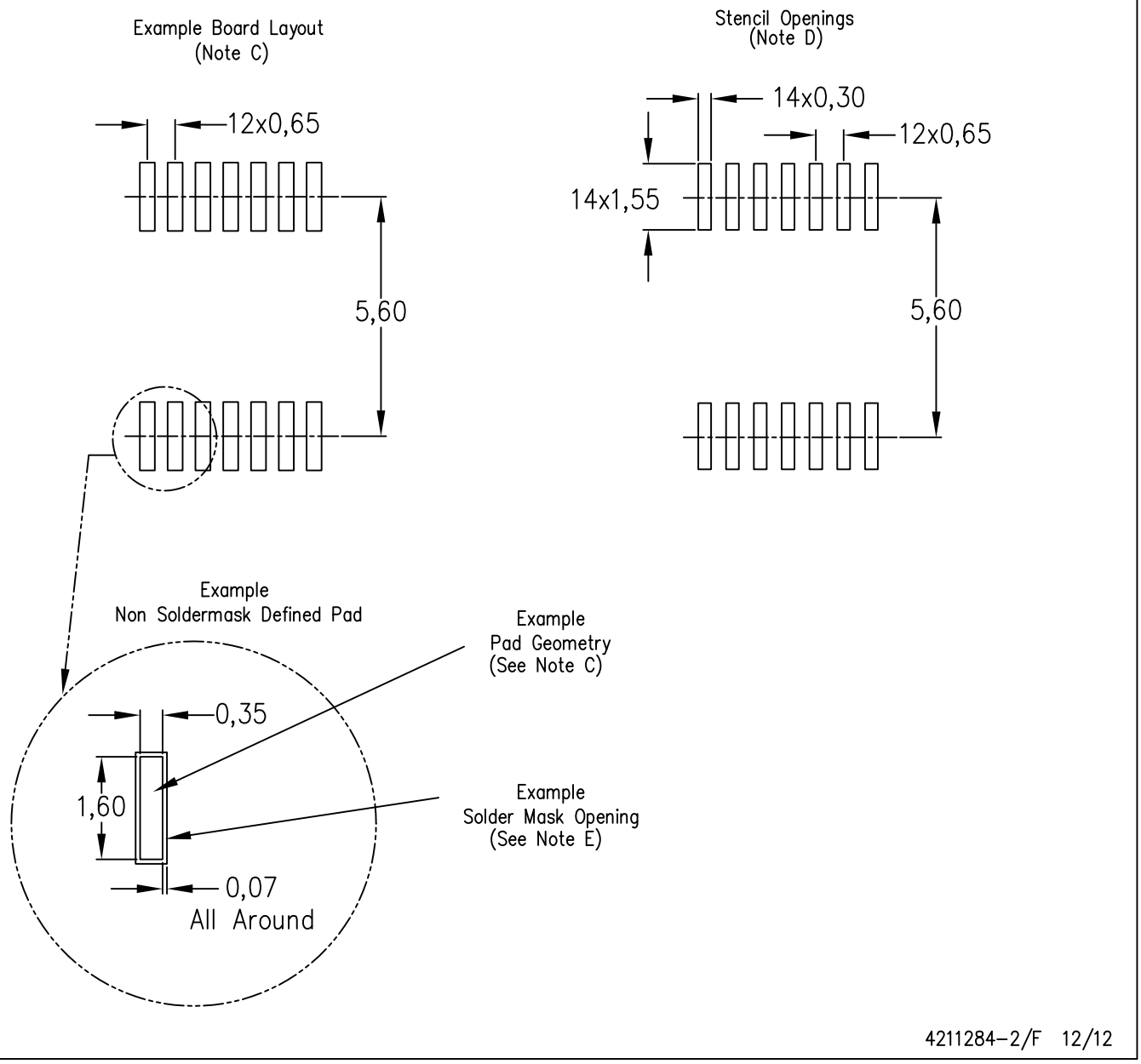
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

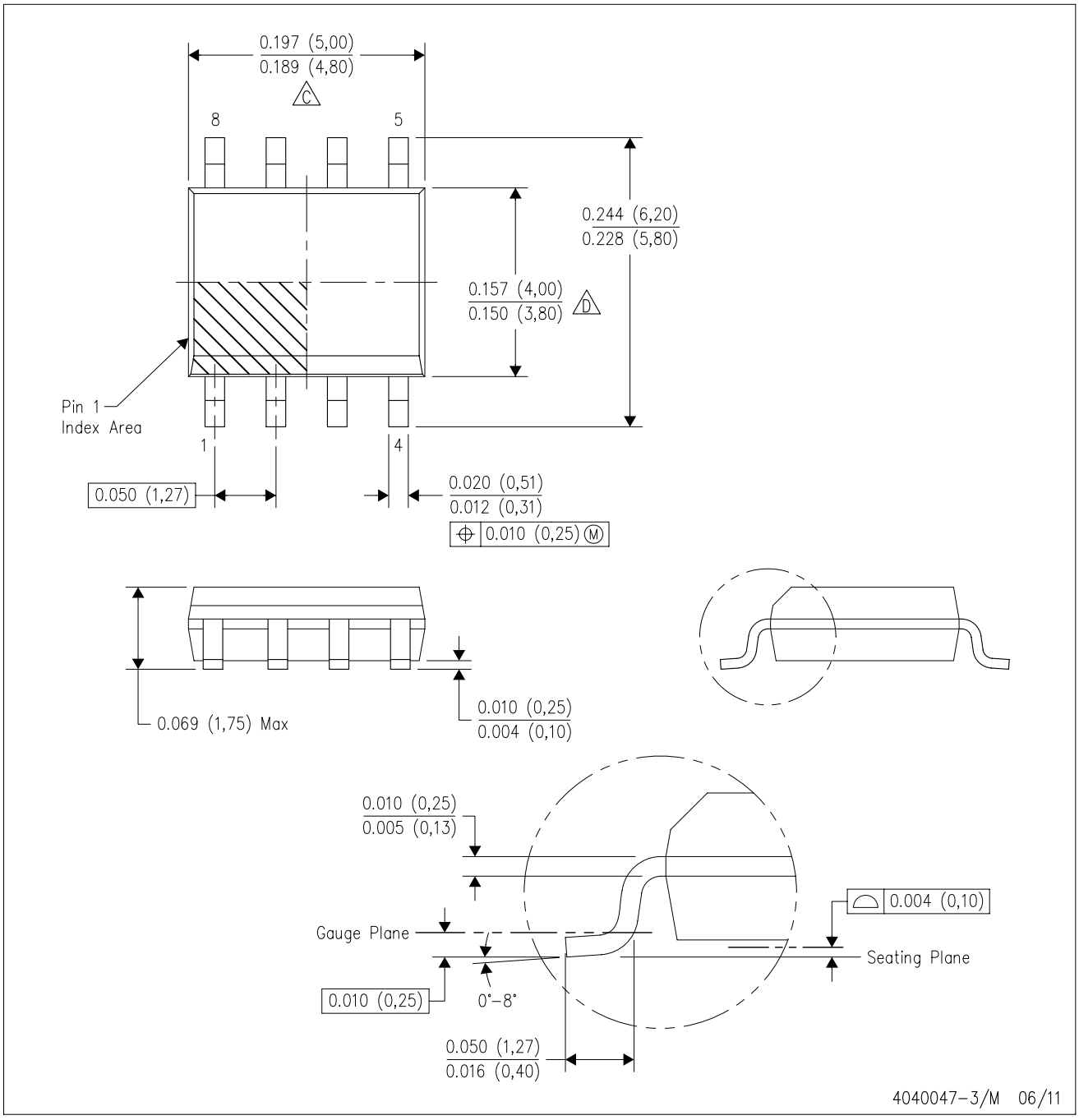
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



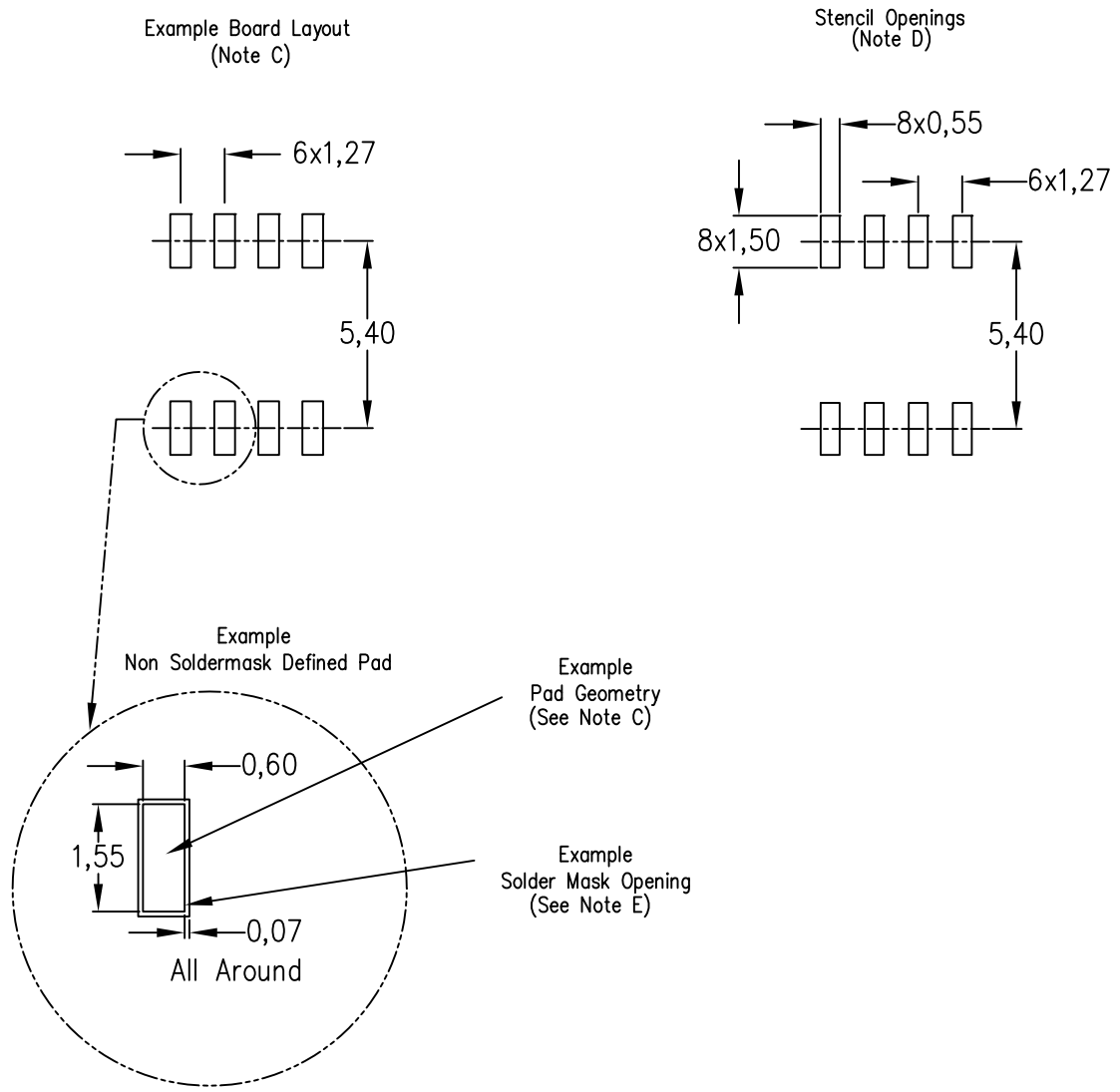
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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