

High-Precision, Low-Noise, Rail-to-Rail Output, 11MHz JFET Op Amp

Check for Samples: [OPA140](#), [OPA2140](#), [OPA4140](#)

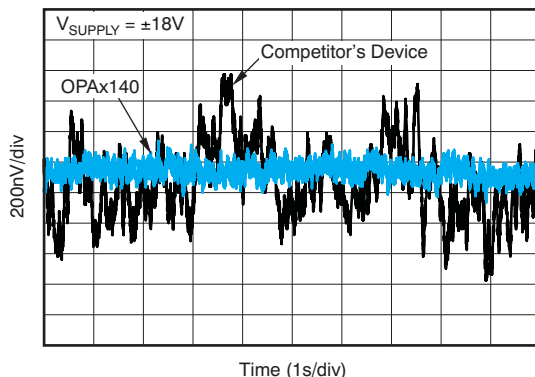
FEATURES

- **Very Low Offset Drift:** $1\mu\text{V}/^\circ\text{C}$ max
- **Very Low Offset:** $120\mu\text{V}$
- **Low Input Bias Current:** 10pA max
- **Very Low 1/f Noise:** 250nV_{PP} , 0.1Hz to 10Hz
- **Low Noise:** $5.1\text{nV}/\sqrt{\text{Hz}}$
- **Slew Rate:** $20\text{V}/\mu\text{s}$
- **Low Supply Current:** 2.0mA max
- **Input Voltage Range Includes V₋ Supply**
- **Single-Supply Operation:** 4.5V to 36V
- **Dual-Supply Operation:** $\pm 2.25\text{V}$ to $\pm 18\text{V}$
- **No Phase Reversal**
- **Industry-Standard SO Packages**
- **MSOP-8, TSSOP, and SOT23 Packages**

APPLICATIONS

- **Battery-Powered Instruments**
- **Industrial Controls**
- **Medical Instrumentation**
- **Photodiode Amplifiers**
- **Active Filters**
- **Data Acquisition Systems**
- **Automatic Test Systems**

0.1Hz to 10Hz NOISE



DESCRIPTION

The OPA140, OPA2140, and OPA4140 op amp family is a series of low-power JFET input amplifiers that feature good drift and low input bias current. The rail-to-rail output swing and input range that includes V₋ allow designers to take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

The OPA140 achieves 11MHz unity-gain bandwidth and $20\text{V}/\mu\text{s}$ slew rate while consuming only 1.8mA (typ) of quiescent current. It runs on a single 4.5 to 36V supply or dual $\pm 2.25\text{V}$ to $\pm 18\text{V}$ supplies.

All versions are fully specified from -40°C to $+125^\circ\text{C}$ for use in the most challenging environments. The OPA140 (single) is available in the SOT23-5, MSOP-8, and SO-8 packages; the OPA2140 (dual) is available in both MSOP-8 and SO-8 packages; and the OPA4140 (quad) is available in the SO-14 and TSSOP-14 packages.

RELATED PRODUCTS

| FEATURES | PRODUCT |
|--|------------------------|
| Low-Power, 10MHz FET Input Industrial Op Amp | OPA141 |
| $2.2\text{nV}/\sqrt{\text{Hz}}$, Low-Power, 36V Operational Amplifier in SOT23 Package | OPA209 |
| Low-Noise, High-Precision, 22MHz , $4\text{nV}/\sqrt{\text{Hz}}$ JFET-Input Operational Amplifier | OPA827 |
| Low-Noise, Low I_Q Precision CMOS Operational Amplifier | OPA376 |
| High-Speed, FET-Input Operational Amplifier | OPA132 |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

| | | VALUE | UNIT |
|---------------------------------------|----------------------------|------------------------|------|
| Supply Voltage | | ±20 | V |
| Signal Input Terminals | Voltage ⁽²⁾ | (V–) –0.5 to (V+) +0.5 | V |
| | Current ⁽²⁾ | ±10 | mA |
| Output Short-Circuit ⁽³⁾ | | Continuous | |
| Operating Temperature, T _A | | –55 to +150 | °C |
| Storage Temperature, T _A | | –65 to +150 | °C |
| Junction Temperature, T _J | | +150 | °C |
| ESD Ratings | Human Body Model (HBM) | 2000 | V |
| | Charged Device Model (CDM) | 500 | V |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to V_S/2 (ground in symmetrical dual-supply setups), one amplifier per package.

PACKAGE INFORMATION⁽¹⁾

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING |
|---------|--------------|--------------------|-----------------|
| OPA140 | SO-8 | D | OPA140 |
| | MSOP-8 | DGK | 140 |
| | SOT23-5 | DBV | O140 |
| OPA2140 | SO-8 | D | O2140A |
| | MSOP-8 | DGK | 2140 |
| OPA4140 | TSSOP-14 | PW | O4140A |
| | SO-14 | D | O4140A |

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ELECTRICAL CHARACTERISTICS: $V_S = +4.5V$ to $+36V$; $\pm 2.25V$ to $\pm 18V$

Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+125^\circ C$.

At $T_A = +25^\circ C$, $R_L = 2k\Omega$ connected to midsupply, $V_{CM} = V_{OUT} =$ midsupply, unless otherwise noted.

| PARAMETER | | CONDITIONS | OPA140, OPA2140, OPA4140 | | | UNIT |
|-----------------------------------|----------------------|--|--------------------------|------------------------|----------|-------------------|
| | | | MIN | TYP | MAX | |
| OFFSET VOLTAGE | | | | | | |
| Offset Voltage, RTI | V _{OS} | V _S = ±18V | | 30 | 120 | μV |
| Over Temperature | | V _S = ±18V | | | 220 | μV |
| Drift | dV _{OS} /dT | V _S = ±18V | | ±0.35 | 1.0 | μV/°C |
| vs Power Supply | PSRR | V _S = ±2.25V to ±18V | | ±0.1 | ±0.5 | μV/V |
| Over Temperature | | V _S = ±2.25V to ±18V | | | ±4 | μV/V |
| INPUT BIAS CURRENT ⁽¹⁾ | | | | | | |
| Input Bias Current | I _B | | | ±0.5 | ±10 | pA |
| Over Temperature | | | | | ±3 | nA |
| Input Offset Current | I _{OS} | | | ±0.5 | ±10 | pA |
| Over Temperature | | | | | ±1 | nA |
| NOISE | | | | | | |
| Input Voltage Noise | | | | | | |
| f = 0.1Hz to 10Hz | | | | 250 | | nV _{PP} |
| f = 0.1Hz to 10Hz | | | | 42 | | nV _{RMS} |
| Input Voltage Noise Density | e _n | | | | | |
| f = 10Hz | | | | 8 | | nV/√Hz |
| f = 100Hz | | | | 5.8 | | nV/√Hz |
| f = 1kHz | | | | 5.1 | | nV/√Hz |
| Input Current Noise Density | I _n | | | | | |
| f = 1kHz | | | | 0.8 | | fA/√Hz |
| INPUT VOLTAGE RANGE | | | | | | |
| Common-Mode Voltage Range | V _{CM} | | (V-) -0.1 | | (V+)-3.5 | V |
| Common-Mode Rejection Ratio | CMRR | V _S = ±18V, V _{CM} = (V-) -0.1V to (V+) - 3.5V | 126 | 140 | | dB |
| Over Temperature | | V _S = ±18V, V _{CM} = (V-) -0.1V to (V+) - 3.5V | 120 | | | dB |
| INPUT IMPEDANCE | | | | | | |
| Differential | | | | 10 ¹³ 10 | | Ω pF |
| Common-Mode | | V _{CM} = (V-) -0.1V to (V+) -3.5V | | 10 ¹³ 7 | | Ω pF |
| OPEN-LOOP GAIN | | | | | | |
| Open-Loop Voltage Gain | A _{OL} | V _O = (V-)+0.35V to (V+)-0.35V, R _L = 10kΩ | 120 | 126 | | dB |
| | | V _O = (V-)+0.35V to (V+)-0.35V, R _L = 2kΩ | 114 | 126 | | dB |
| Over Temperature | | V _O = (V-)+0.35V to (V+)-0.35V, R _L = 2kΩ | 108 | | | dB |
| FREQUENCY RESPONSE | | | | | | |
| Gain Bandwidth Product | BW | | | 11 | | MHz |
| Slew Rate | | | | 20 | | V/μs |
| Settling Time, 12-bit (0.024) | | | | 880 | | ns |
| Settling Time, 16-bit | | | | 1.6 | | μs |
| THD+N | | 1kHz, G = 1, V _O = 3.5V _{RMS} | | 0.00005 | | % |
| Overload Recovery Time | | | | 600 | | ns |

(1) High-speed test, $T_A = T_J$.

ELECTRICAL CHARACTERISTICS: $V_S = +4.5V$ to $+36V$; $\pm 2.25V$ to $\pm 18V$ (continued)

Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+125^\circ C$.

At $T_A = +25^\circ C$, $R_L = 2k\Omega$ connected to midsupply, $V_{CM} = V_{OUT} =$ midsupply, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA140, OPA2140, OPA4140 | | | UNIT | |
|-----------------------------------|-------------------|---|---|------|-----------|------|
| | | MIN | TYP | MAX | | |
| OUTPUT | | | | | | |
| Voltage Output | V _O | R _L = 10kΩ, A _{OL} ≥ 108dB | (V−)+0.2 | | (V+)-0.2 | V |
| | | R _L = 2kΩ, A _{OL} ≥ 108dB | (V−)+0.35 | | (V+)-0.35 | V |
| Short-Circuit Current | I _{SC} | Source | | +36 | | mA |
| | | Sink | | −30 | | mA |
| Capacitive Load Drive | C _{LOAD} | | See Figure 20 and Figure 21 | | | |
| Open-Loop Output Impedance | R _O | f = 1MHz, I _O = 0 (See Figure 19) | | 16 | | Ω |
| POWER SUPPLY | | | | | | |
| Specified Voltage Range | V _S | | ±2.25 | | ±18 | V |
| Quiescent Current (per amplifier) | I _Q | I _O = 0mA | | 1.8 | 2.0 | mA |
| Over Temperature | | | | | 2.7 | mA |
| CHANNEL SEPARATION | | | | | | |
| Channel Separation | | At dc | | 0.02 | | μV/V |
| | | At 100kHz | | 10 | | μV/V |
| TEMPERATURE RANGE | | | | | | |
| Specified Range | | | −40 | | +125 | °C |
| Operating Range | | | −55 | | +150 | °C |

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | OPA140, OPA2140 | OPA140, OPA2140 | OPA140 | UNITS |
|-------------------------------|--|--------------------|--------------------|-------------|--------------|
| | | D (SO) | DGK (MSOP) | DBV (SOT23) | |
| | | 8 | 8 | 5 | |
| θ_{JA} | Junction-to-ambient thermal resistance | 160 | 180 | 210 | $^\circ C/W$ |
| $\theta_{JC(top)}$ | Junction-to-case(top) thermal resistance | 75 | 55 | 200 | |
| θ_{JB} | Junction-to-board thermal resistance | 60 | 130 | 110 | |
| ψ_{JT} | Junction-to-top characterization parameter | 9 | n/a | 40 | |
| ψ_{JB} | Junction-to-board characterization parameter | 50 | 120 | 105 | |
| $\theta_{JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | n/a | n/a | n/a | |

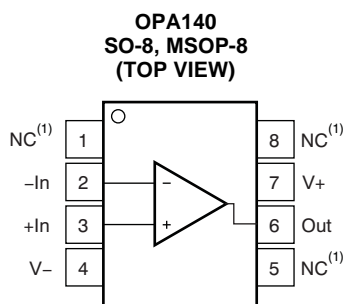
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

THERMAL INFORMATION

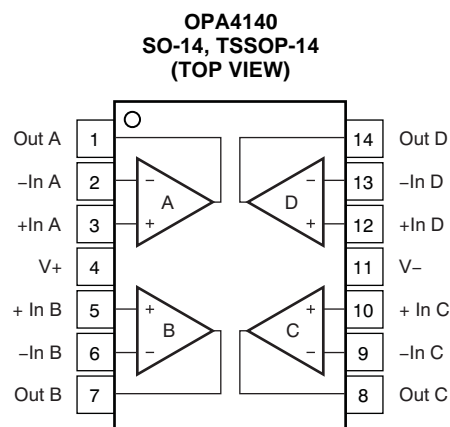
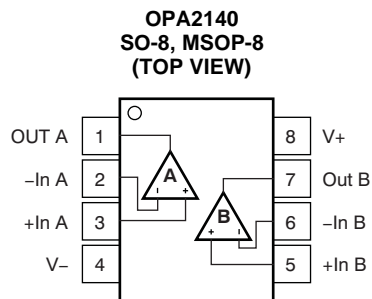
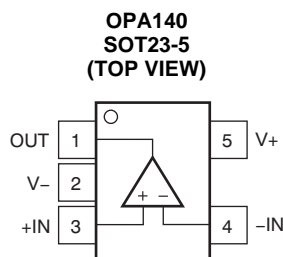
| THERMAL METRIC ⁽¹⁾ | | OPA4140 | OPA4140 | UNITS |
|-------------------------------|--|---------|------------|--------------|
| | | D (SO) | PW (TSSOP) | |
| | | 14 | 14 | |
| θ_{JA} | Junction-to-ambient thermal resistance | 97 | 135 | $^\circ C/W$ |
| $\theta_{JC(top)}$ | Junction-to-case(top) thermal resistance | 56 | 45 | |
| θ_{JB} | Junction-to-board thermal resistance | 53 | 66 | |
| ψ_{JT} | Junction-to-top characterization parameter | 19 | n/a | |
| ψ_{JB} | Junction-to-board characterization parameter | 46 | 60 | |
| $\theta_{JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

PIN ASSIGNMENTS



(1) NC denotes no internal connection.



SIMPLIFIED BLOCK DIAGRAM

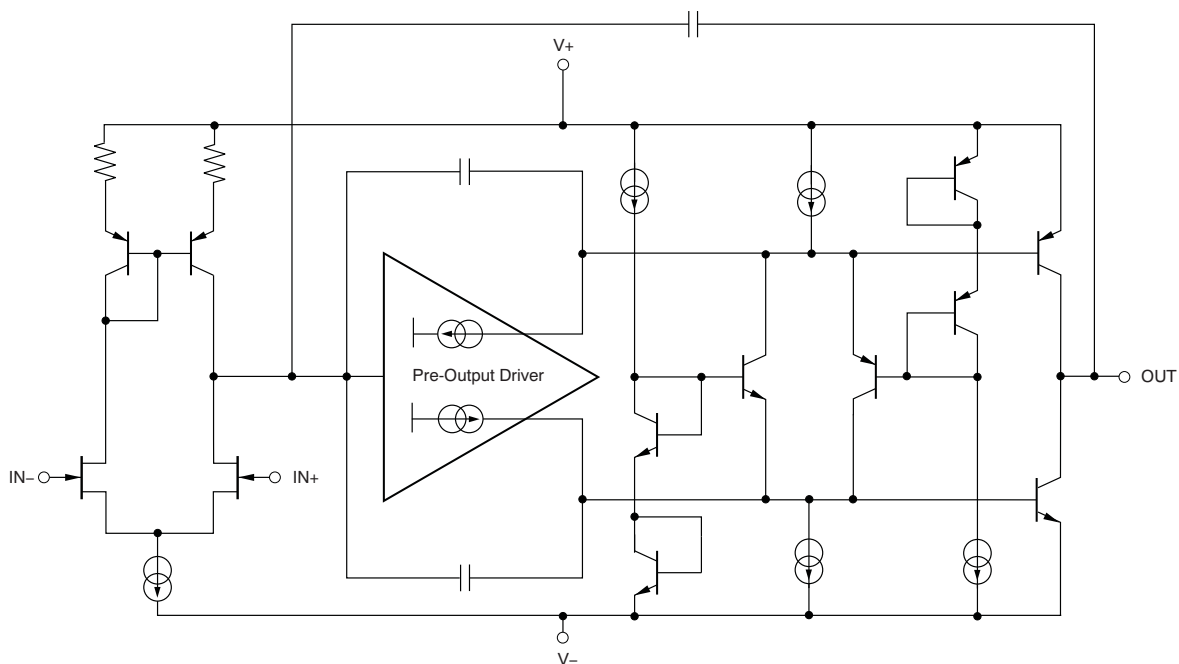


Figure 1.

TYPICAL CHARACTERISTICS SUMMARY

TABLE OF GRAPHS

Table 1. Characteristic Performance Measurements

| DESCRIPTION | FIGURE |
|--|--------------------------------------|
| Offset Voltage Production Distribution | Figure 2 |
| Offset Voltage Drift Distribution | Figure 3 |
| Offset Voltage vs Common-Mode Voltage (Max Supply) | Figure 4 |
| I_B vs Common-Mode Voltage | Figure 6 |
| Input Offset Voltage vs Temperature | Figure 5 |
| Output Voltage Swing vs Output Current | Figure 7 |
| CMRR and PSRR vs Frequency (RTI) | Figure 8 |
| Common-Mode Rejection Ratio vs Temperature | Figure 9 |
| 0.1Hz to 10Hz Noise | Figure 10 |
| Input Voltage Noise Density vs Frequency | Figure 11 |
| THD+N Ratio vs Frequency (80kHz AP Bandwidth) | Figure 12 |
| THD+N Ratio vs Output Amplitude | Figure 13 |
| Quiescent Current vs Temperature | Figure 14 |
| Quiescent Current vs Supply Voltage | Figure 15 |
| Gain and Phase vs Frequency | Figure 16 |
| Closed-Loop Gain vs Frequency | Figure 17 |
| Open-Loop Gain vs Temperature | Figure 18 |
| Open-Loop Output Impedance vs Frequency | Figure 19 |
| Small-Signal Overshoot vs Capacitive Load ($G = +1$) | Figure 20 |
| Small-Signal Overshoot vs Capacitive Load ($G = -1$) | Figure 21 |
| No Phase Reversal | Figure 22 |
| Positive Overload Recovery | Figure 24 |
| Negative Overload Recovery | Figure 25 |
| Large-Signal Positive and Negative Settling Time | Figure 26, Figure 27 |
| Small-Signal Step Response ($G = +1$) | Figure 28 |
| Small-Signal Step Response ($G = -1$) | Figure 29 |
| Large-Signal Step Response ($G = +1$) | Figure 30 |
| Large-Signal Step Response ($G = -1$) | Figure 31 |
| Short-Circuit Current vs Temperature | Figure 32 |
| Maximum Output Voltage vs Frequency | Figure 23 |
| Channel Separation vs Frequency | Figure 33 |

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

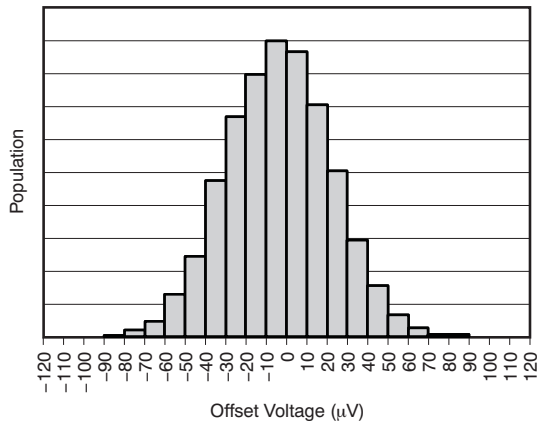


Figure 2.

OFFSET VOLTAGE DRIFT DISTRIBUTION

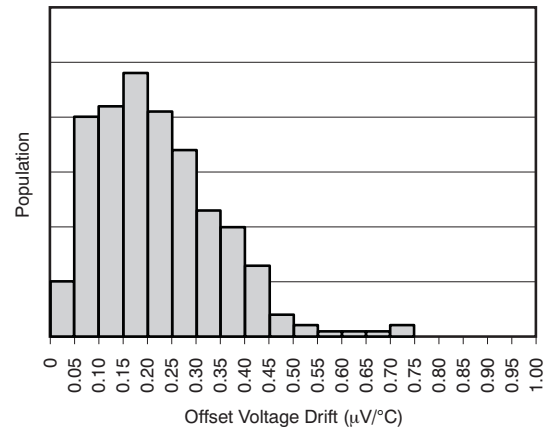


Figure 3.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

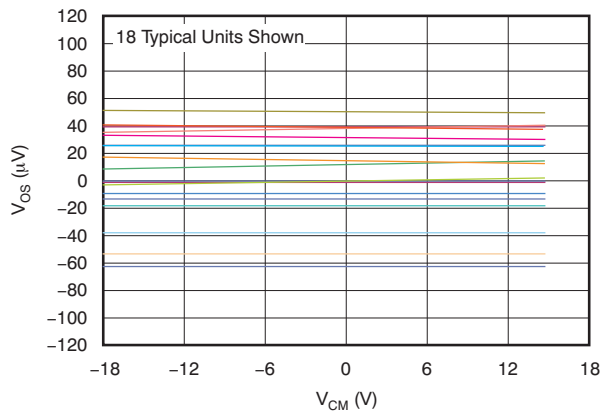


Figure 4.

**INPUT OFFSET VOLTAGE vs TEMPERATURE
(144 Amplifiers)**

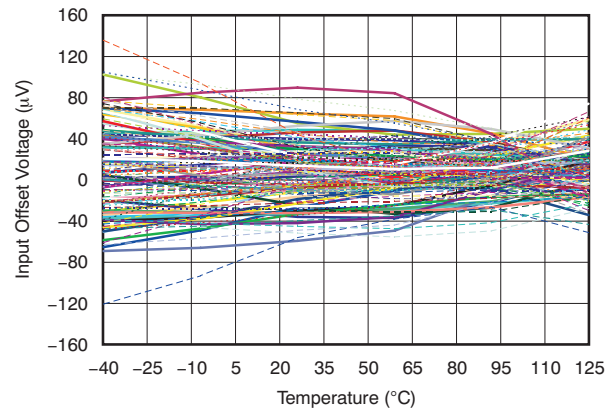


Figure 5.

I_B vs COMMON-MODE VOLTAGE

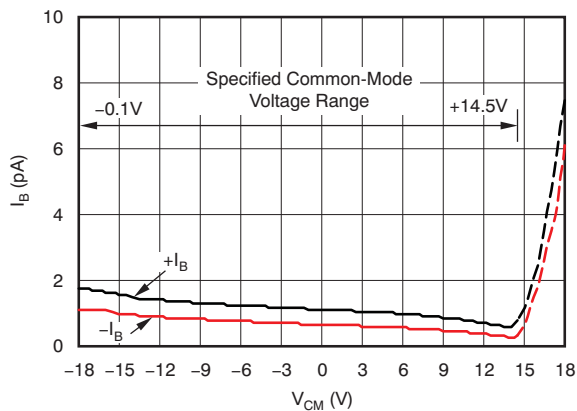


Figure 6.

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT
(MAX SUPPLY)**

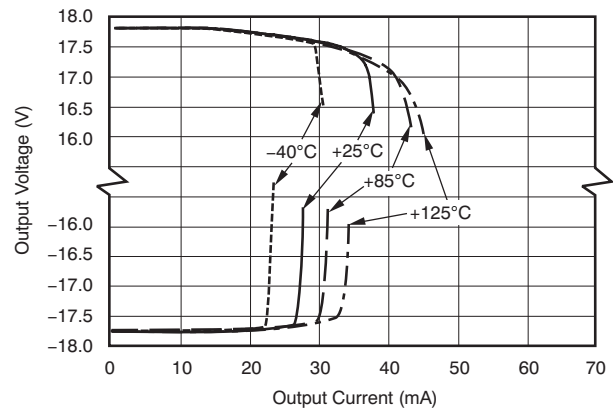


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

CMRR AND PSRR vs FREQUENCY (Referred to Input)

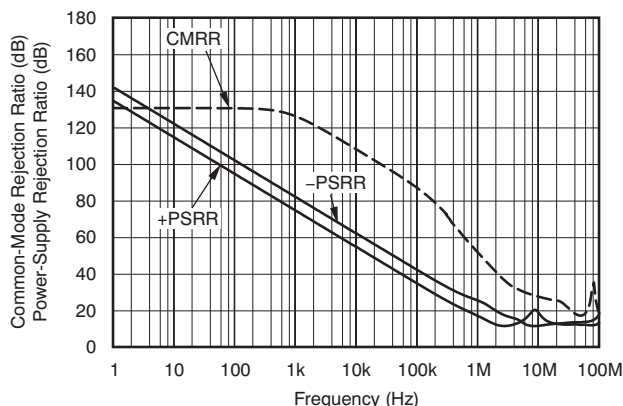


Figure 8.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

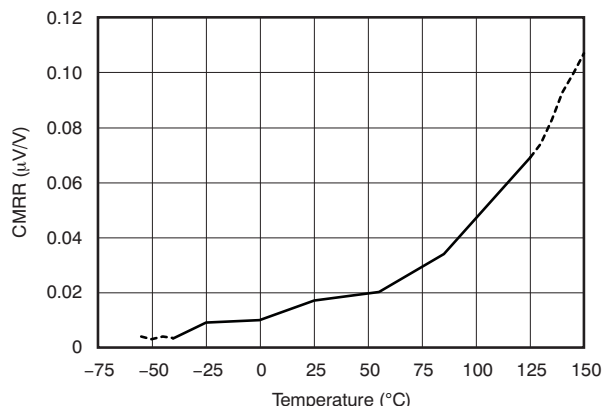


Figure 9.

0.1Hz to 10Hz NOISE

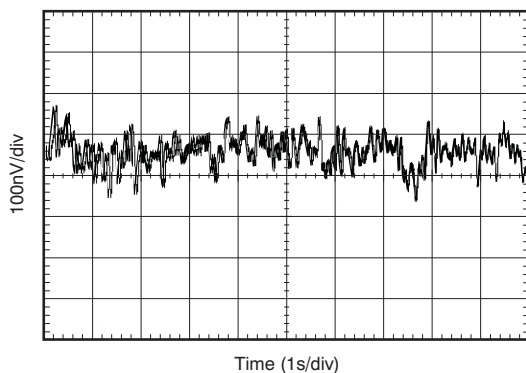


Figure 10.

INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

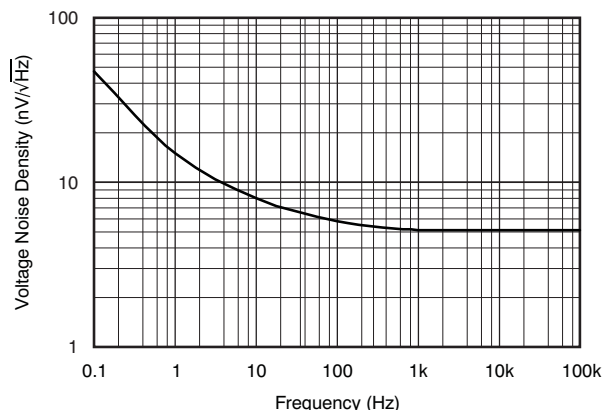


Figure 11.

THD+N RATIO vs FREQUENCY

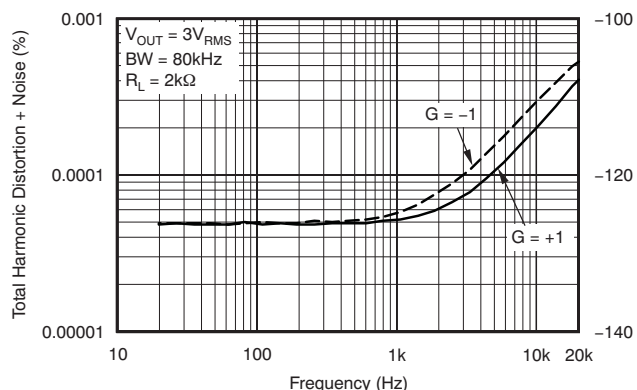


Figure 12.

THD+N RATIO vs OUTPUT AMPLITUDE

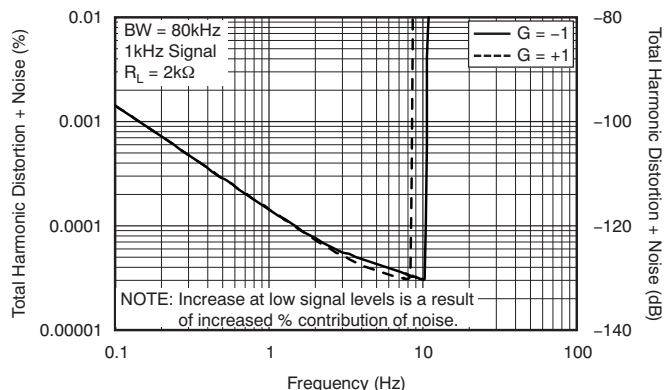


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

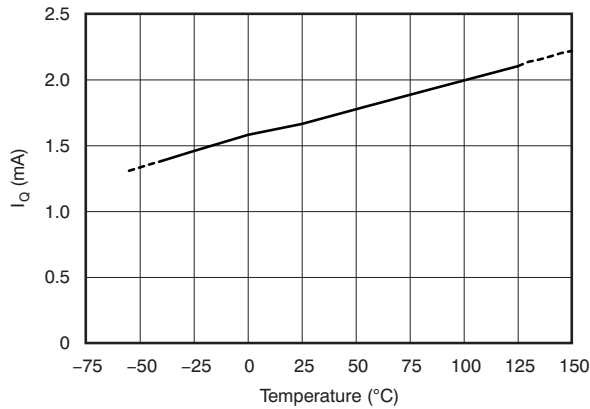


Figure 14.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

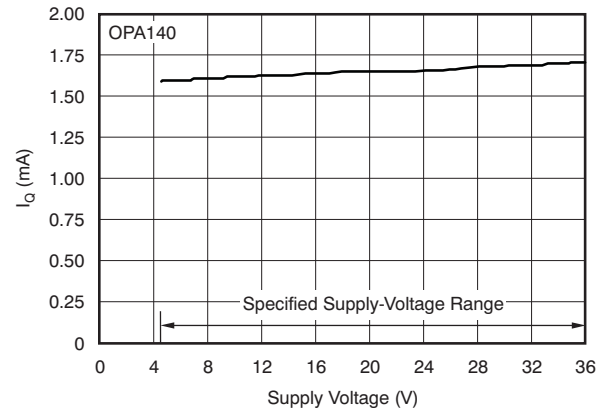


Figure 15.

GAIN AND PHASE vs FREQUENCY

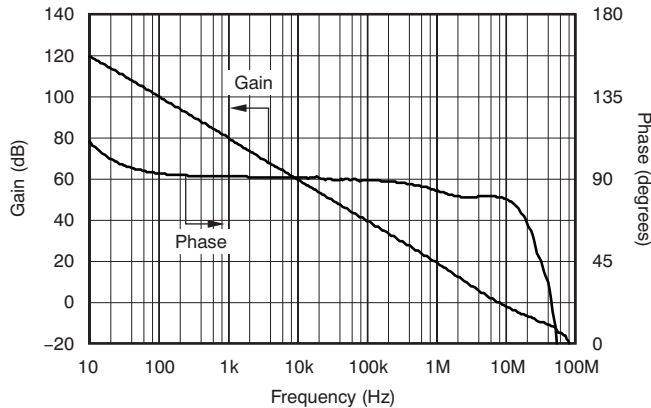


Figure 16.

CLOSED-LOOP GAIN vs FREQUENCY

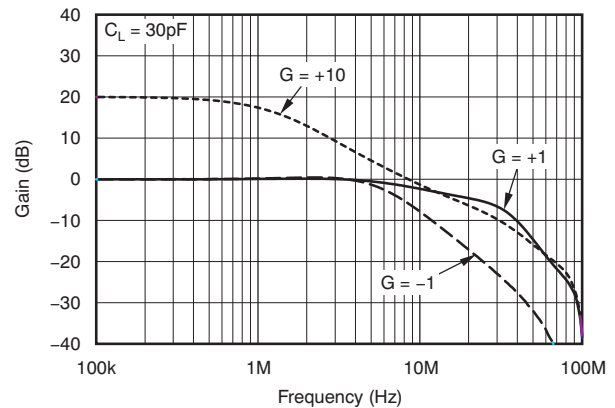


Figure 17.

OPEN-LOOP GAIN vs TEMPERATURE

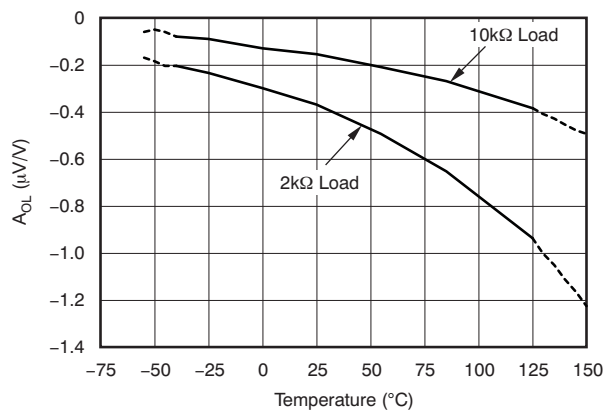


Figure 18.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

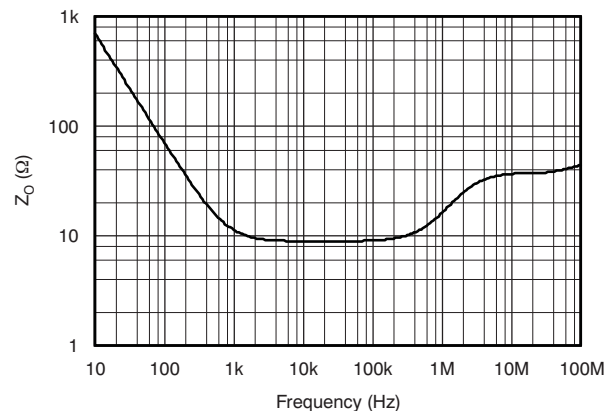


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

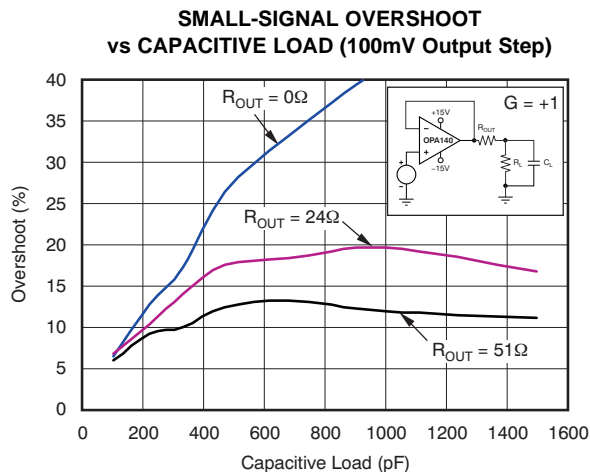


Figure 20.

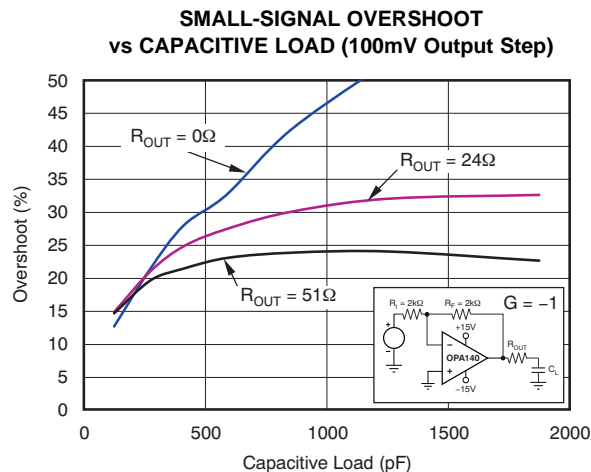


Figure 21.

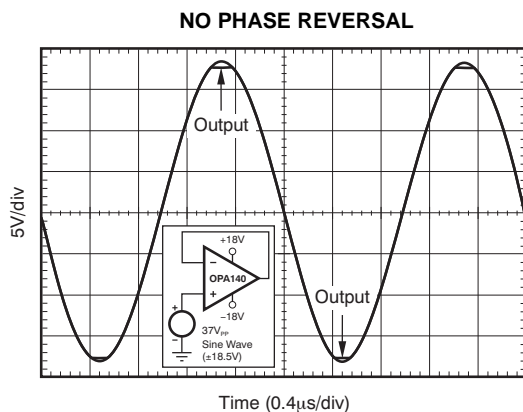


Figure 22.

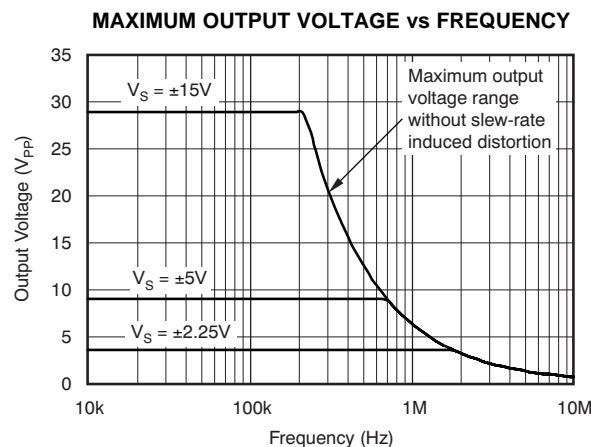


Figure 23.

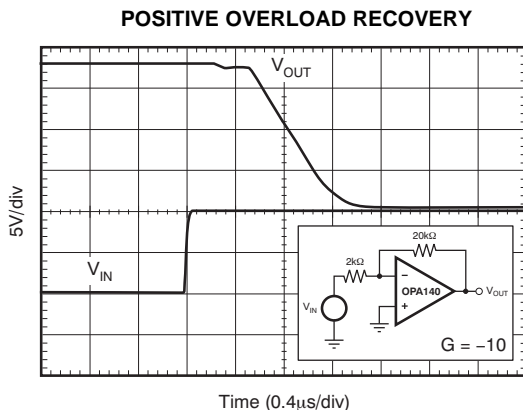


Figure 24.

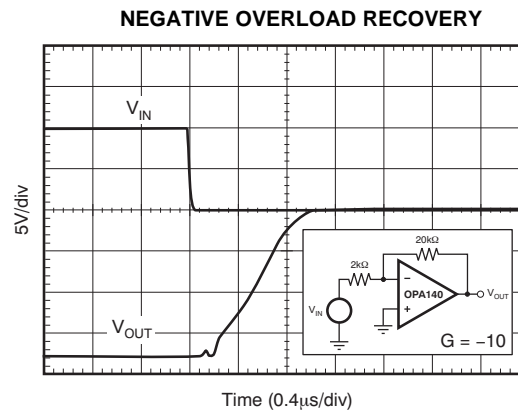


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

**LARGE-SIGNAL POSITIVE SETTLING TIME
(10V Step)**

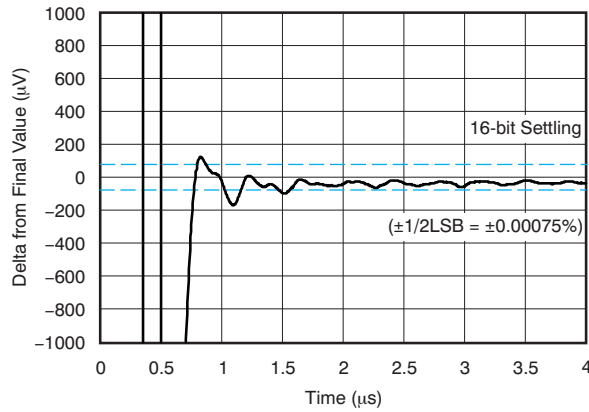


Figure 26.

**LARGE-SIGNAL NEGATIVE SETTLING TIME
(10V Step)**

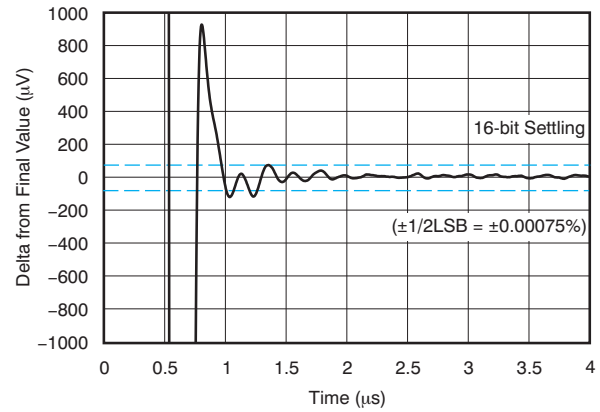


Figure 27.

**SMALL-SIGNAL STEP RESPONSE
(100mV)**

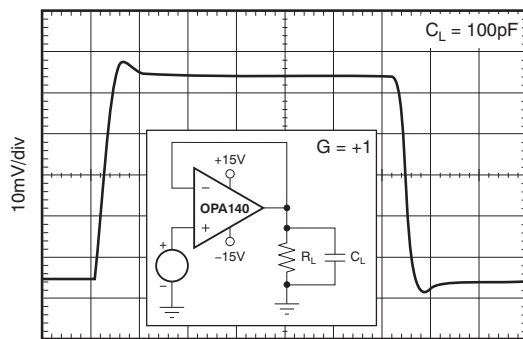


Figure 28.

**SMALL-SIGNAL STEP RESPONSE
(100mV)**

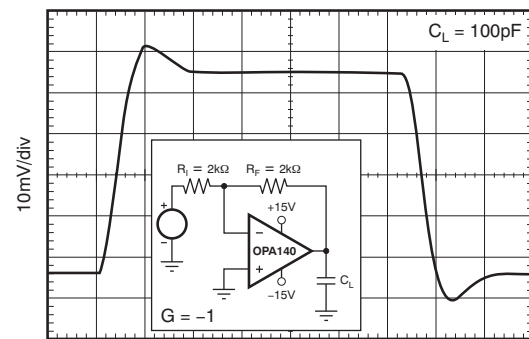


Figure 29.

LARGE-SIGNAL STEP RESPONSE

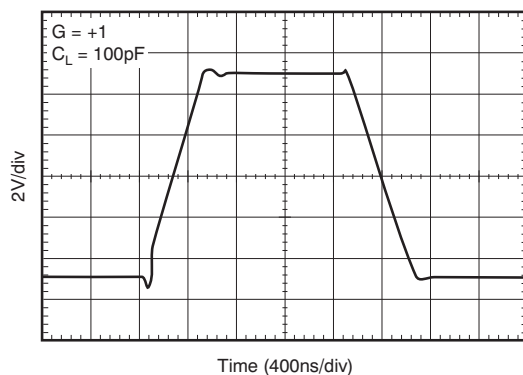


Figure 30.

LARGE-SIGNAL STEP RESPONSE

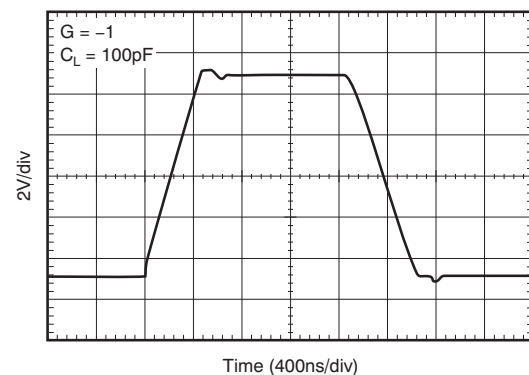


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

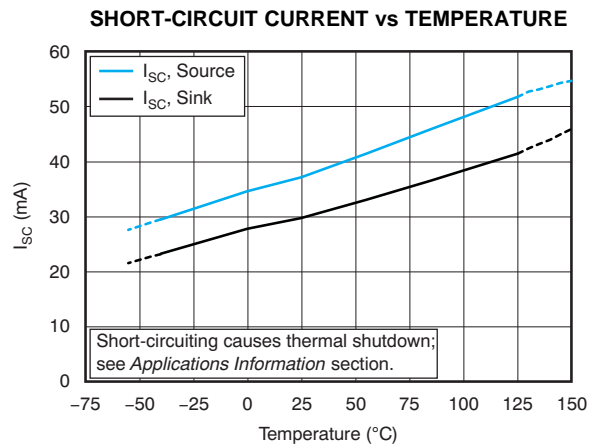


Figure 32.

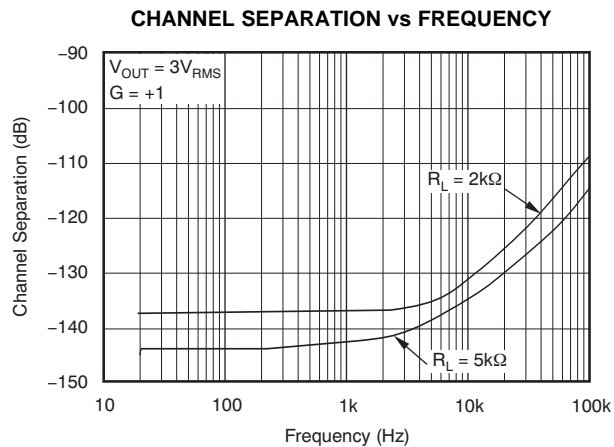


Figure 33.

APPLICATION INFORMATION

The OPA140, OPA2140, and OPA4140 are unity-gain stable, operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1µF capacitors are adequate. [Figure 1](#) shows a simplified schematic of the OPA140.

OPERATING VOLTAGE

The OPA140, OPA2140, and OPA4140 series of op amps can be used with single or dual supplies from an operating range of $V_S = +4.5V (\pm 2.25V)$ and up to $V_S = +36V (\pm 18V)$. These devices do not require symmetrical supplies; they only require a minimum supply voltage of +4.5V ($\pm 2.25V$). For V_S less than $\pm 3.5V$, the common-mode input range does not include midsupply. Supply voltages higher than +40V can permanently damage the device; see the [Absolute Maximum Ratings](#) table. Key parameters are specified over the operating temperature range, $T_A = -40^\circ C$ to $+125^\circ C$. Key parameters that vary over the supply voltage or temperature range are shown in the [Typical Characteristics](#) section of this data sheet.

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPAx140 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50Ω, for example) in series with the output.

[Figure 20](#) and [Figure 21](#) illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT} . Also, refer to [Applications Bulletin AB-028](#) (literature number [SBOA015](#), available for download from the [TI web site](#)) for details of analysis techniques and application circuits.

NOISE PERFORMANCE

[Figure 34](#) shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA140 and OPA211 are shown

with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA140, OPA2140, and OPA4140 family has both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPAx140 series is negligible for any practical source impedance, which makes it the better choice for applications with high source impedance.

The equation in [Figure 34](#) shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in degrees Kelvin (K)

For more details on calculating noise, see the section on [Basic Noise Calculations](#).

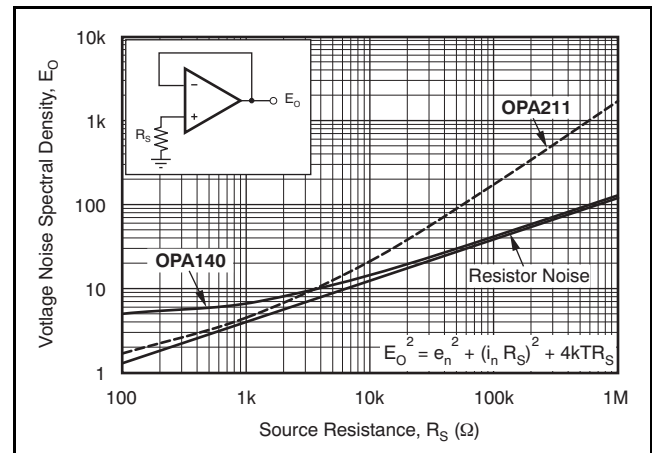


Figure 34. Noise Performance of the OPA140 and OPA211 in Unity-Gain Buffer Configuration

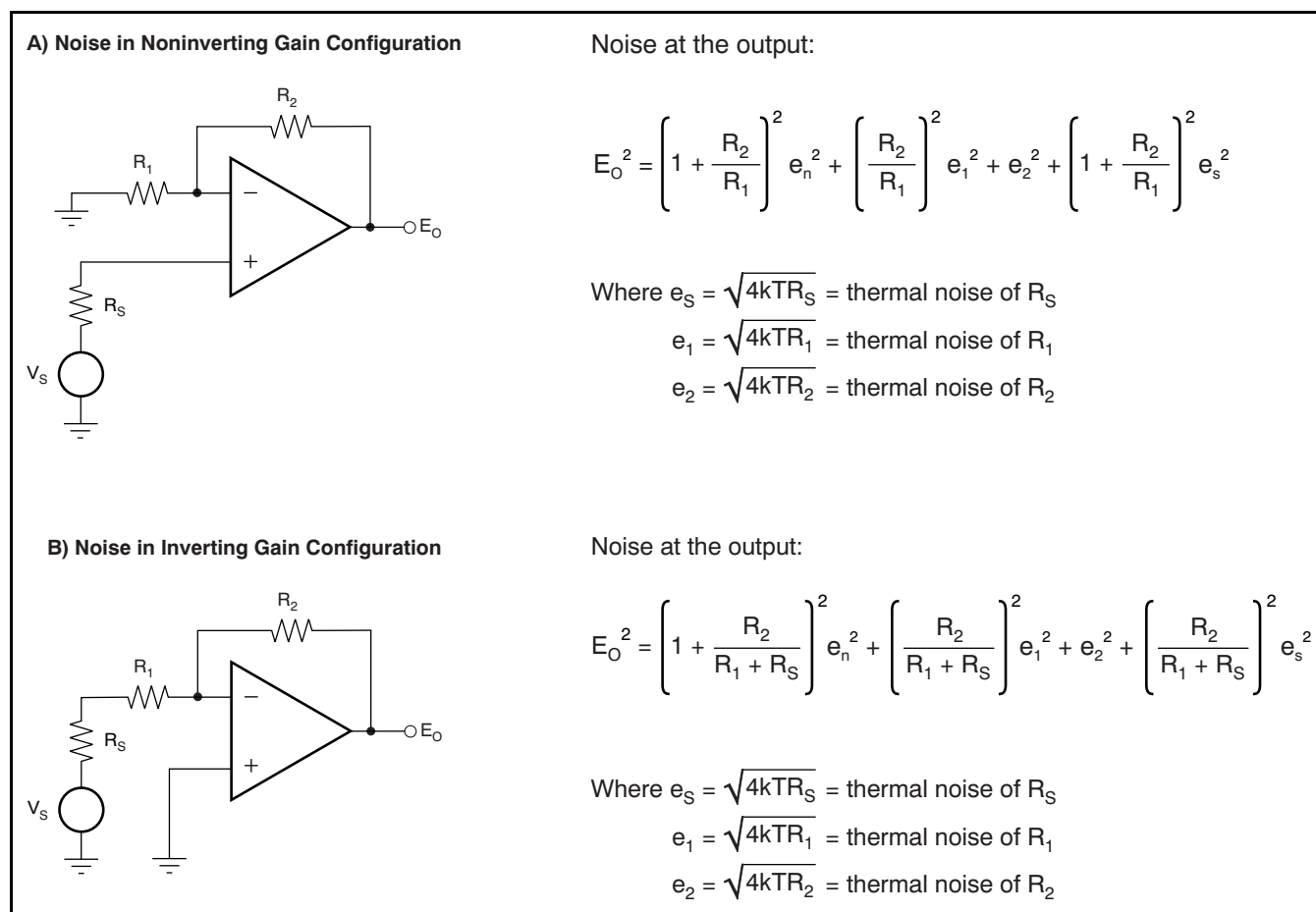
BASIC NOISE CALCULATIONS

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in [Figure 34](#). The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

[Figure 35](#) illustrates both noninverting (A) and inverting (B) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx140 means that its current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.



For the OPAx140 series of operational amplifiers at 1kHz, $e_n = 5.1\text{nV}/\sqrt{\text{Hz}}$.

Figure 35. Noise Calculation in Gain Configurations

PHASE-REVERSAL PROTECTION

The OPA140, OPA2140, and OPA4140 family has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA140, OPA2140, and OPA4140 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see [Figure 22](#)).

OUTPUT CURRENT LIMIT

The output current of the OPAx140 series is limited by internal circuitry to +36mA/–30mA (sourcing/sinking), to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature, as shown in [Figure 32](#).

POWER DISSIPATION AND THERMAL PROTECTION

The OPAx140 series of op amps are capable of driving 2k Ω loads with power-supply voltages of up to ± 18 V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8k Ω at a supply voltage of +36V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance may be used, as long as the output current does not exceed 13mA; otherwise, the device short-circuit current protection circuit may activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA140, OPA2140, and OPA4140 series devices improves heat dissipation compared to conventional materials. Printed circuit board (PCB) layout can also help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by acting as an additional heatsink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to mid-supply, the typical short-circuit current of 36mA leads to an internal power dissipation of over 600mW at a supply of ± 18 V.

In the case of a dual OPA2140 in an MSOP-8 package (thermal resistance $\theta_{JA} = 180^{\circ}\text{C/W}$), such power dissipation would lead the die temperature to be 220°C above ambient temperature, when both channels are shorted. This temperature increase significantly decreases the operating life of the device.

In order to prevent excessive heating, the OPAx140 series has an internal thermal shutdown circuit, which shuts down the device if the die temperature exceeds approximately +180°C. Once this thermal shutdown circuit activates, a built-in hysteresis of 15°C ensures that the die temperature must drop to approximately +165°C before the device switches on again.

Additional consideration should be given to the combination of maximum operating voltage, maximum operating temperature, load, and package type. [Figure 36](#) and [Figure 37](#) show several practical considerations when evaluating the OPA2140 (dual version) and the OPA4140 (quad version).

As an example, the OPA4140 has a maximum total quiescent current of 10.8mA (2.7mA/channel) over temperature. The TSSOP-14 package has a typical thermal resistance of 135°C/W. This parameter means that because the junction temperature should not exceed +150°C in order to ensure reliable operation, either the supply voltage must be reduced, or the ambient temperature should remain low enough so that the junction temperature does not exceed +150°C. This condition is illustrated in [Figure 36](#) for various package types. Moreover, resistive loading of the output causes additional power dissipation and thus self-heating, which also must be considered when establishing the maximum supply voltage or operating temperature. To this end, [Figure 37](#) shows the maximum supply voltage versus temperature for a worst-case dc load resistance of 2k Ω .

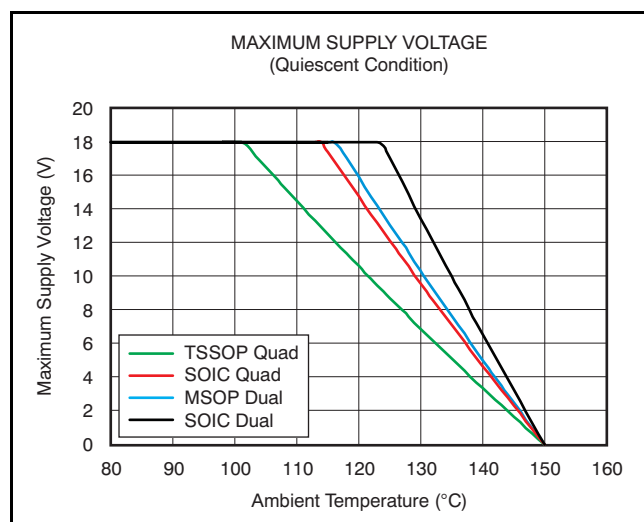


Figure 36. Maximum Supply Voltage vs Temperature (OPA2140 and OPA4140), Quiescent Condition

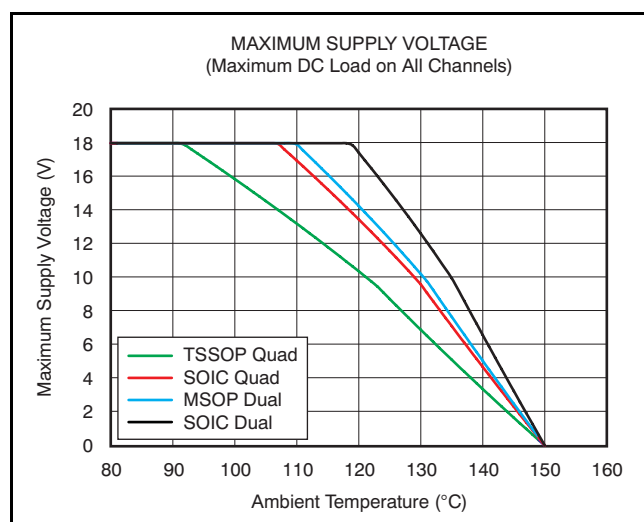


Figure 37. Maximum Supply Voltage vs Temperature (OPA2140 and OPA4140), Maximum DC Load

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the

particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See [Figure 38](#) for an illustration of the ESD circuits contained in the OPAx140 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx140 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one [Figure 38](#) shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 38 depicts a specific example where the input voltage, V_{IN} , exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

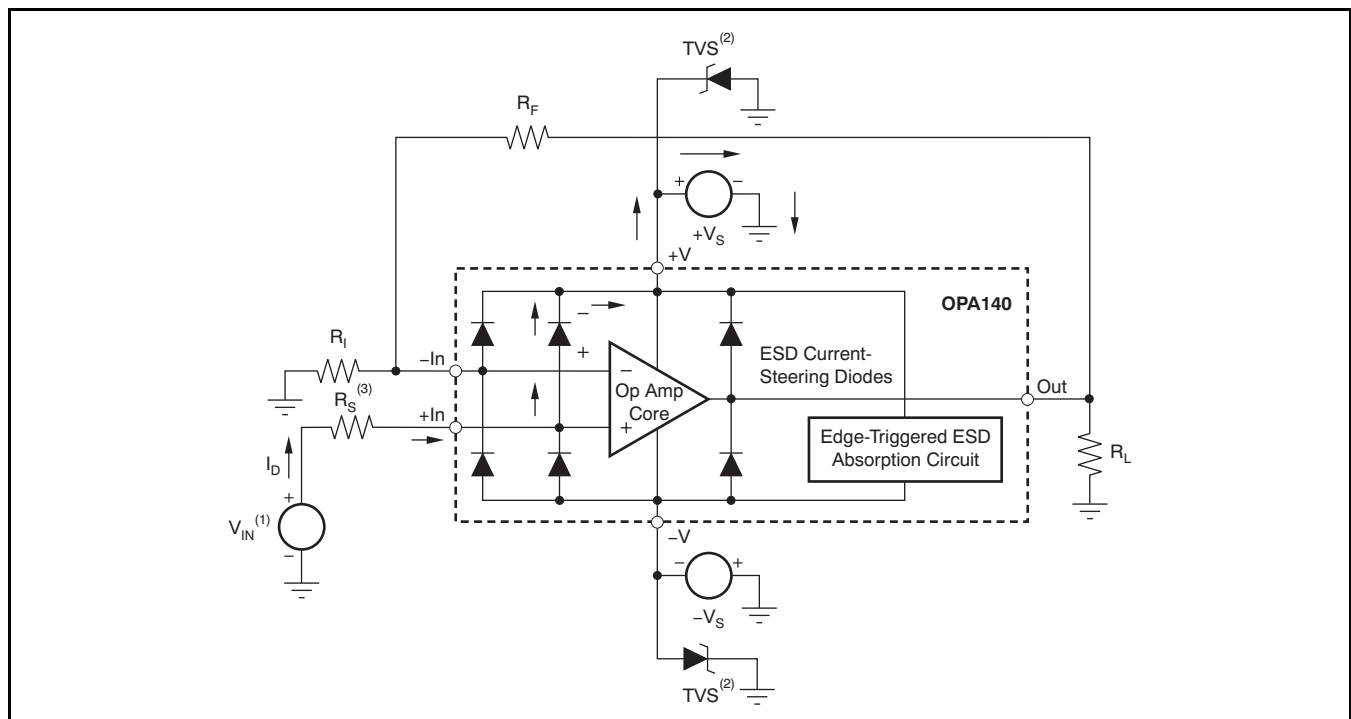
If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $-V_S$ are at 0V.

Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins as shown in Figure 38. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



- (1) $V_{IN} = +V_S + 500\text{mV}$.
- (2) TVS: $+V_{S(\text{max})} > V_{\text{TVSBR (Min)}} > +V_S$
- (3) Suggested value approximately 1kΩ.

Figure 38. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| OPA140AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA140AIDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA140AIDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA140AIDGKR | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA140AIDGKT | ACTIVE | MSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA140AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA2140AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA2140AIDGKR | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA2140AIDGKT | ACTIVE | MSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA2140AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA4140AID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| OPA4140AIDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| OPA4140AIPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| OPA4140AIPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

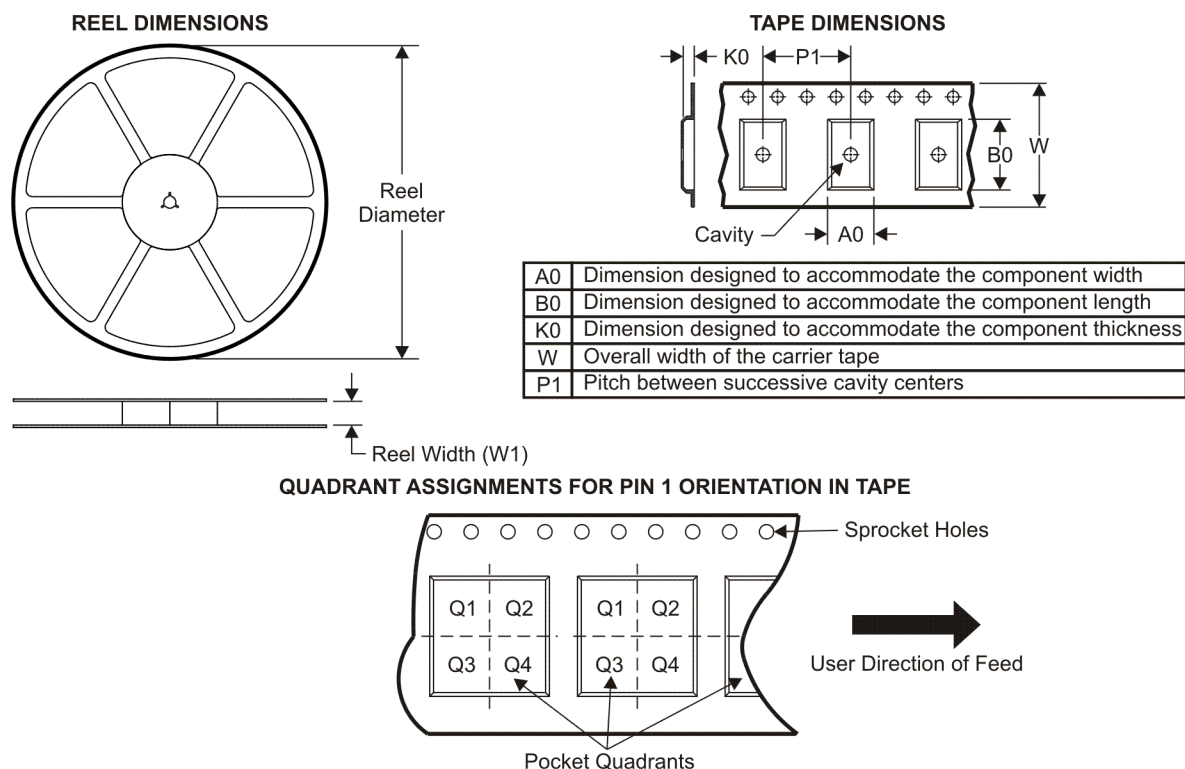
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA140AIDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.1 | 1.39 | 4.0 | 8.0 | Q3 |
| OPA140AIDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.1 | 1.39 | 4.0 | 8.0 | Q3 |
| OPA140AIDGKR | MSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA140AIDGKT | MSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA140AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2140AIDGKR | MSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2140AIDGKT | MSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2140AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA4140AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

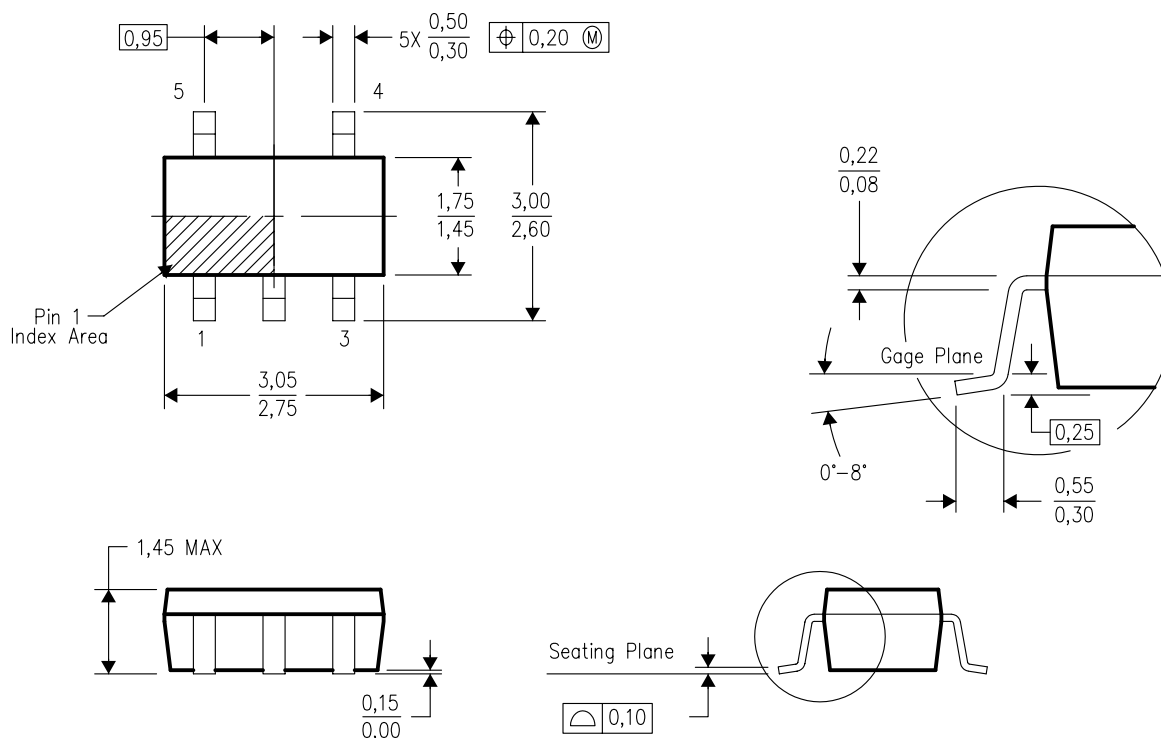


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA140AIDBVR | SOT-23 | DBV | 5 | 3000 | 190.5 | 212.7 | 31.8 |
| OPA140AIDBVT | SOT-23 | DBV | 5 | 250 | 190.5 | 212.7 | 31.8 |
| OPA140AIDGKR | MSOP | DGK | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| OPA140AIDGKT | MSOP | DGK | 8 | 250 | 190.5 | 212.7 | 31.8 |
| OPA140AIDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| OPA2140AIDGKR | MSOP | DGK | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| OPA2140AIDGKT | MSOP | DGK | 8 | 250 | 190.5 | 212.7 | 31.8 |
| OPA2140AIDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| OPA4140AIDR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |

DBV (R-PDSO-G5)

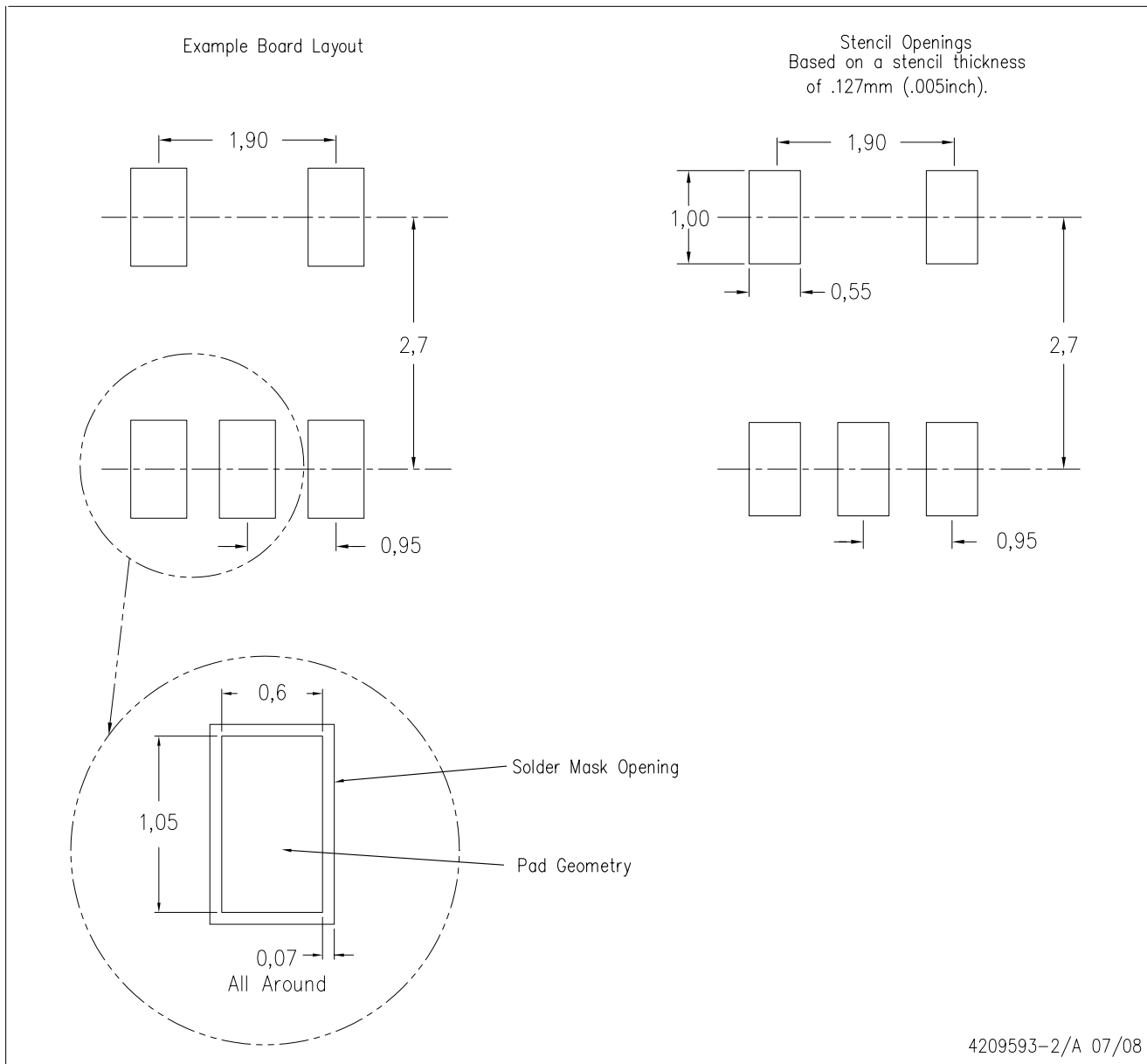
PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

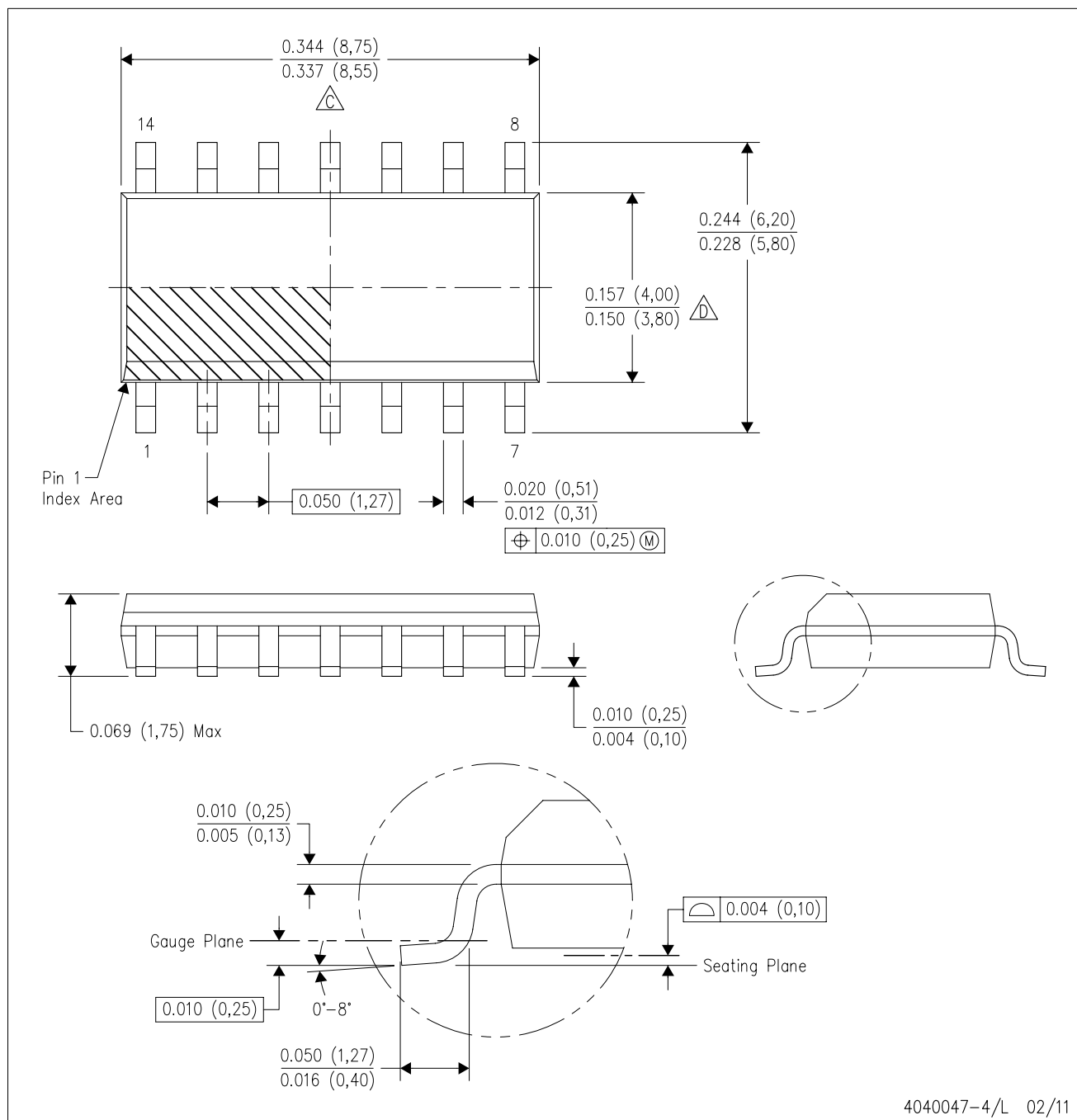
PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



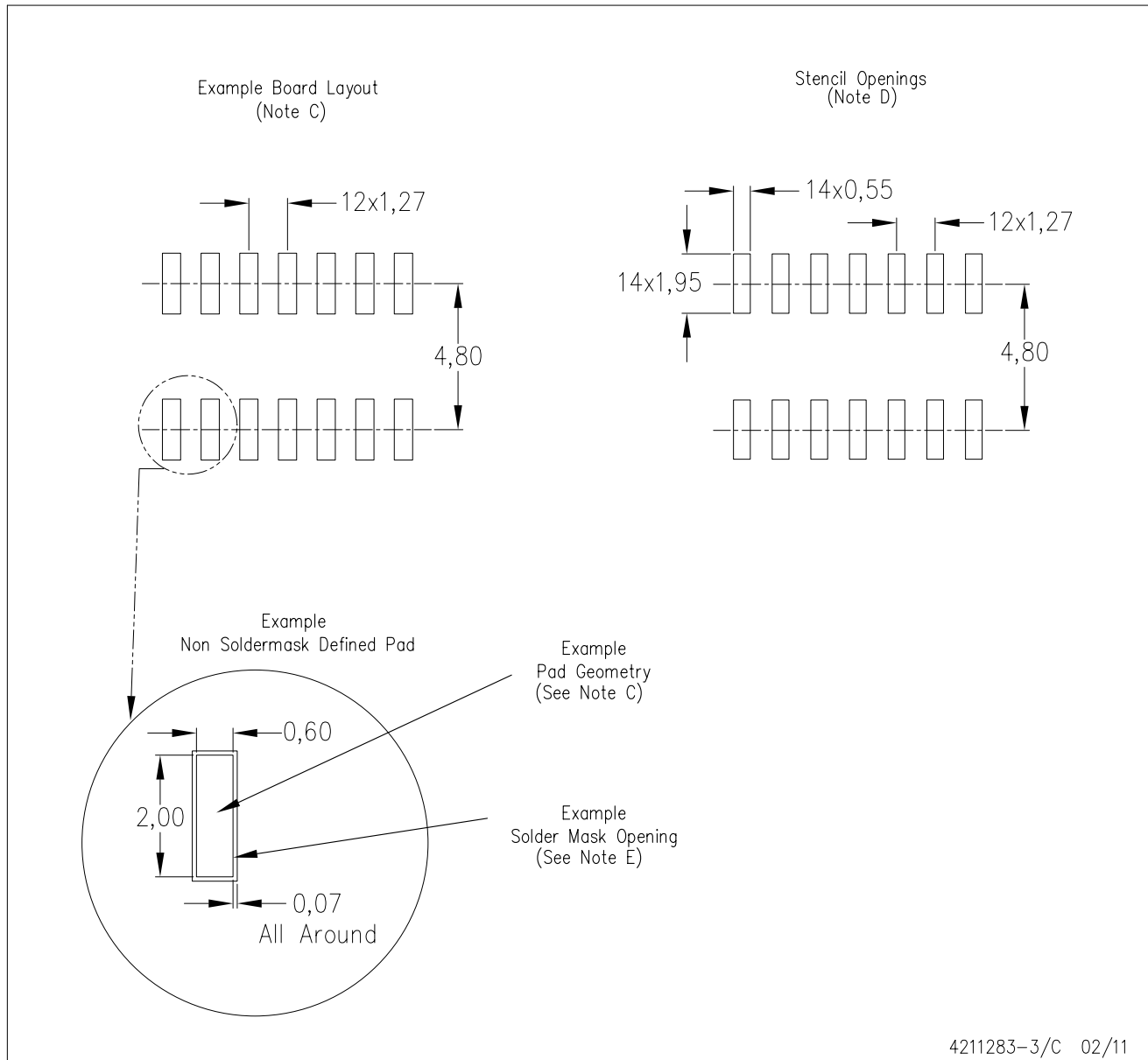
4040047-4/L 02/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

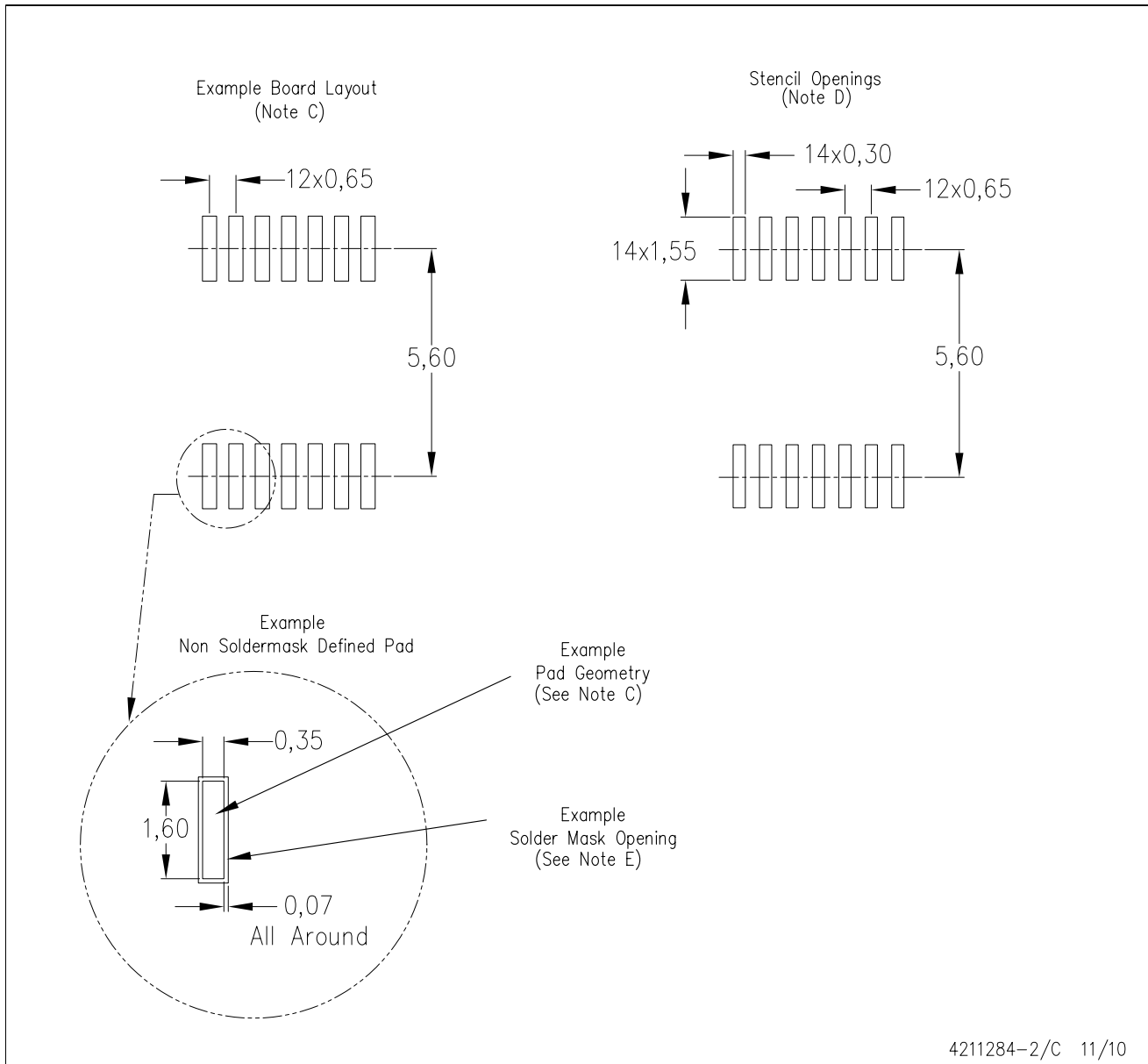


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

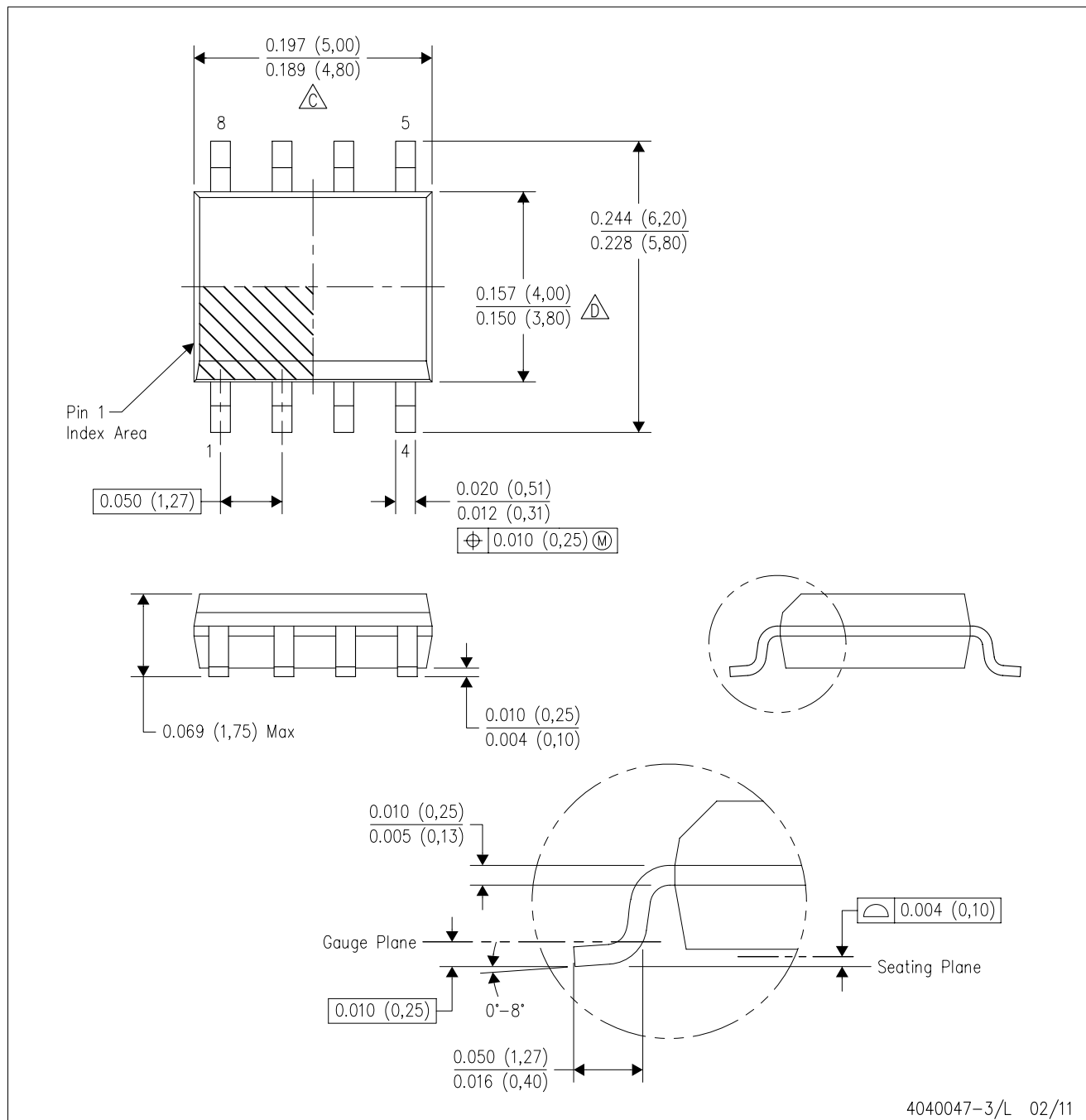
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

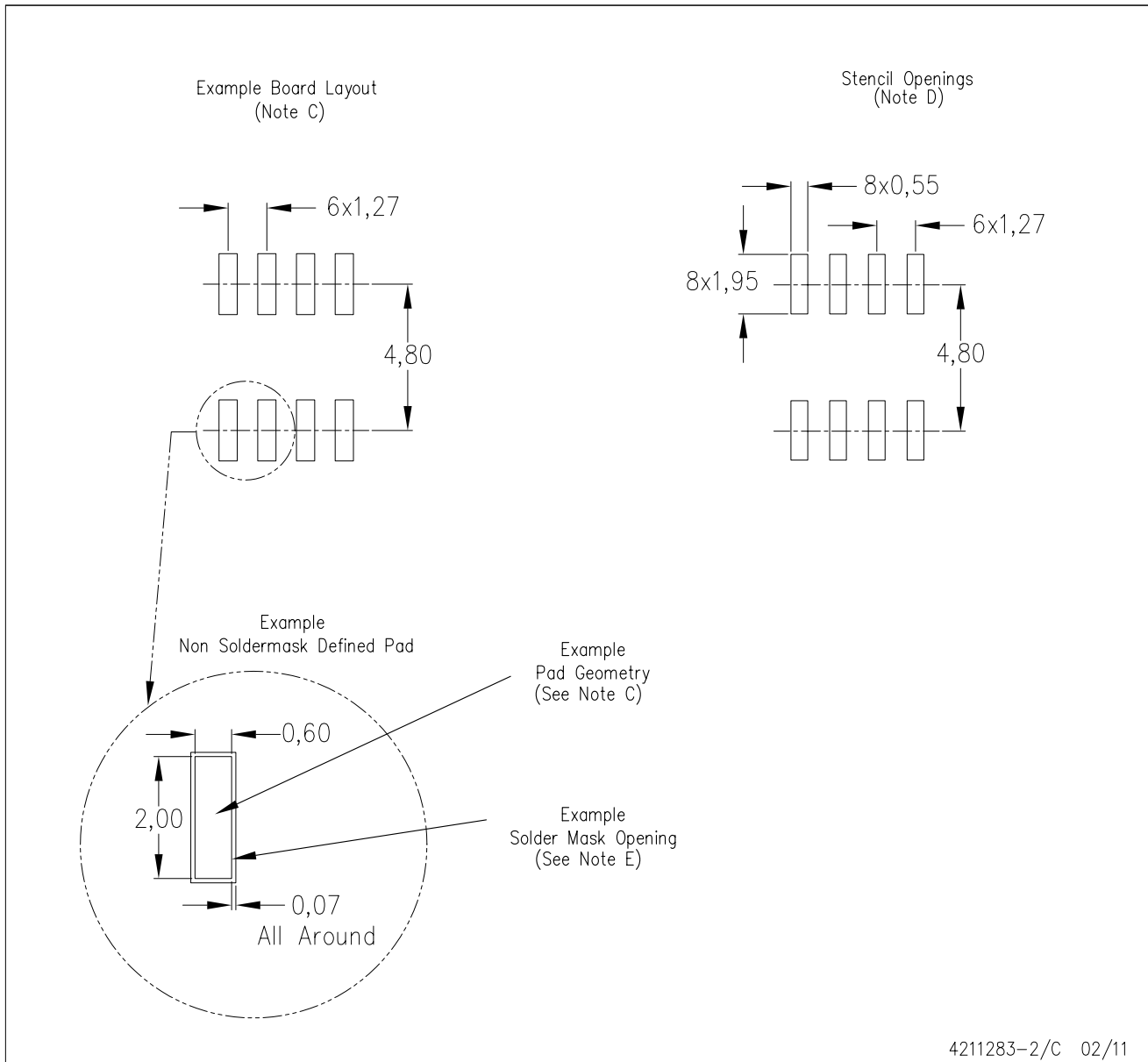
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

| | |
|-----------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf |

Applications

| | |
|-------------------------------|--|
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Transportation and Automotive | www.ti.com/automotive |
| Video and Imaging | www.ti.com/video |
| Wireless | www.ti.com/wireless-apps |

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated