

N-Channel JFETs

J108	SST108
J109	SST109
J110	SST110

PRODUCT SUMMARY				
Part Number	$V_{GS(off)}$ (V)	$r_{DS(on)}$ Max (Ω)	$I_{D(off)}$ Typ (pA)	t_{ON} Typ (ns)
J/SST108	-3 to -10	8	20	4
J/SST109	-2 to -6	12	20	4
J/SST110	-0.5 to -4	18	20	4

FEATURES

- Low On-Resistance: J108 <8 Ω
- Fast Switching— t_{ON} : 4 ns
- Low Leakage: 20 pA
- Low Capacitance: 11 pF
- Low Insertion Loss

BENEFITS

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible “Off-Error” Excellent Accuracy
- Good Frequency Response
- Eliminates Additional Buffering

APPLICATIONS

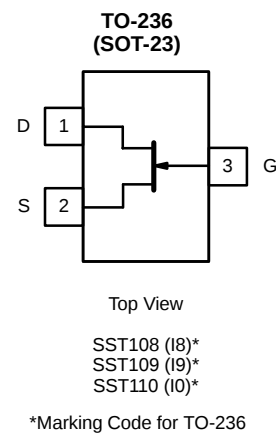
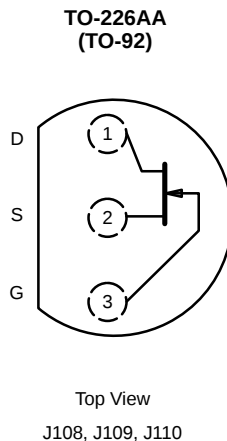
- Analog Switches
- Choppers
- Sample-and-Hold
- Normally “On” Switches
- Current Limiters

DESCRIPTION

The J/SST108 series is designed with high-performance analog switching applications in mind. It features low on-resistance, good off-isolation, and fast switching.

The SST108 series is comprised of surface-mount devices featuring the lowest $r_{DS(on)}$ of any TO-236 (SOT-23) JFET device.

The TO-226AA (TO-92) plastic package provides a low-cost option. Both the J and SST series are available in tape-and-reel for automated assembly (see Packaging Information). For similar products packaged in TO-206AC (TO-52), see the 2N5432/5433/5434 data sheet.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage -25 V
 Gate Current 50 mA
 Lead Temperature ($1/16$ " from case for 10 sec.) 300°C
 Storage Temperature -55 to 150°C

Operating Junction Temperature -55 to 150°C
 Power Dissipation^a 350 mW

Notes

a. Derate 2.8 mW/°C above 25°C

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

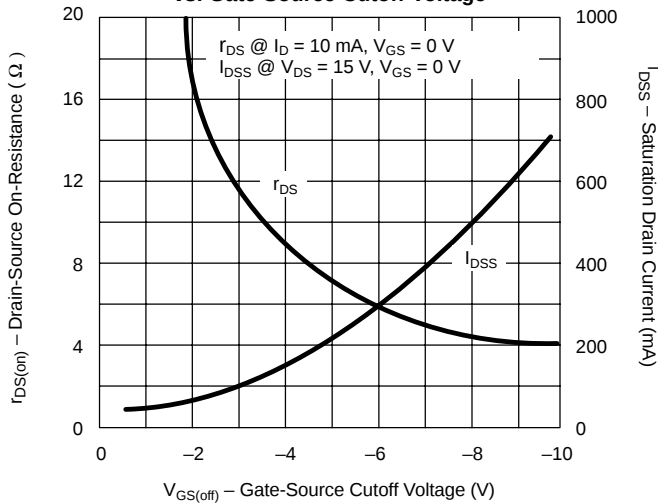
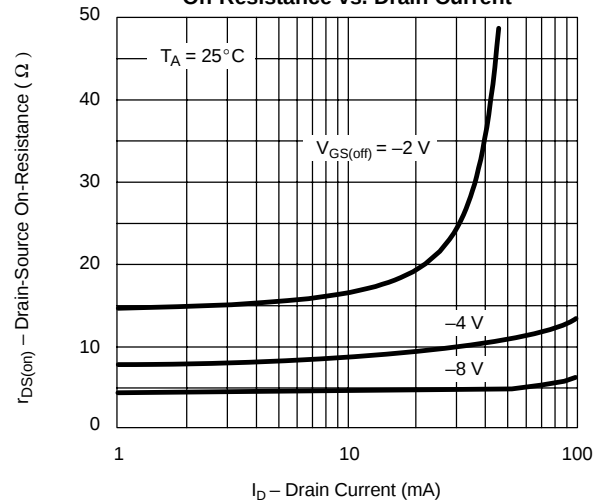
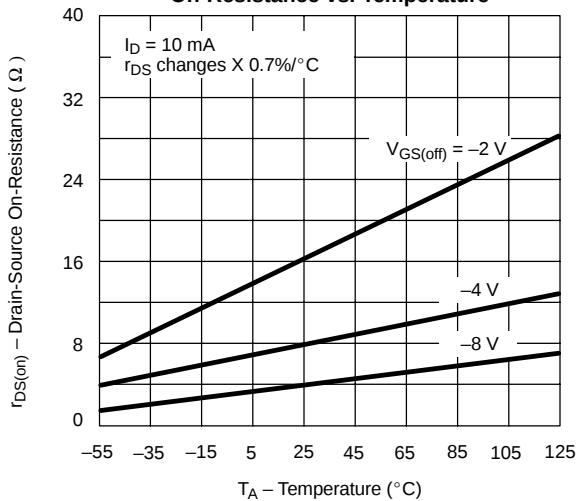
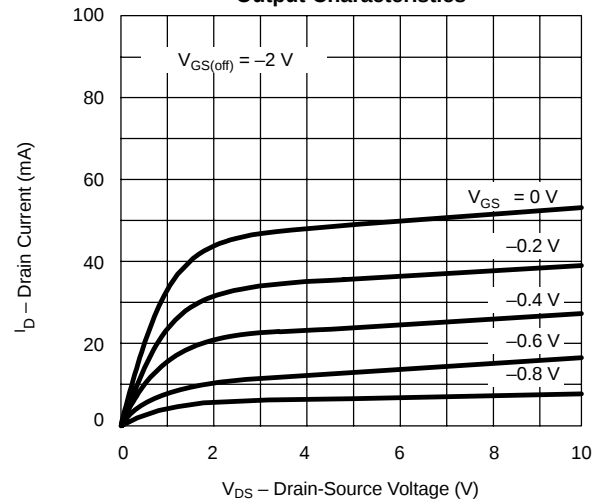
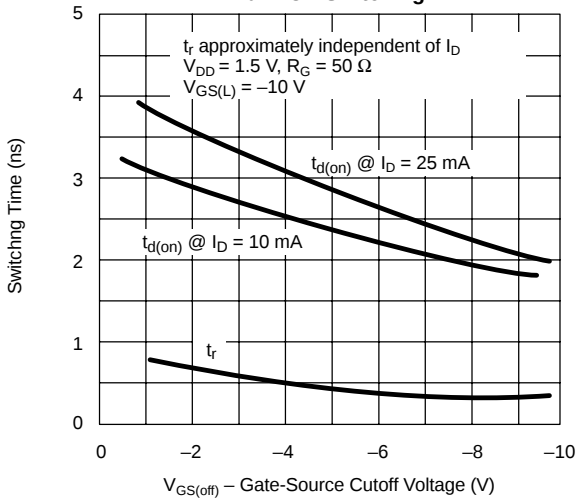
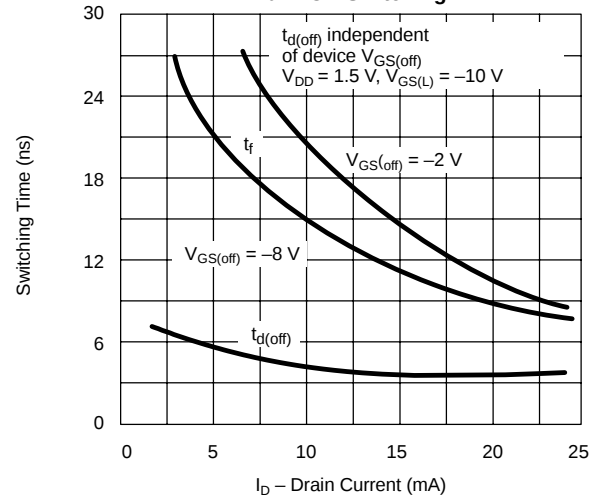
Parameter	Symbol	Test Conditions	Typ ^a	Limits						Unit
				J/SST108		J/SST109		J/SST110		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = −1 μA , V _{DS} = 0 V	−32	−25		−25		−25		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 5 V, I _D = 1 μA		−3	−10	−2	−6	−0.5	−4	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = 15 V, V _{GS} = 0 V		80		40		10		mA
Gate Reverse Current	I _{GSS}	V _{GS} = −15 V, V _{DS} = 0 V	−0.01		−3		−3		−3	nA
		T _A = 125°C	−5							
Gate Operating Current	I _G	V _{DG} = 10 V, I _D = 10 mA	−0.01							
Drain Cutoff Current	I _{D(off)}	V _{DS} = 5 V, V _{GS} = −10 V	0.02		3		3		3	
		T _A = 125°C	1.0							
Drain-Source On-Resistance	r _{DS(on)}	V _{GS} = 0 V, V _{DS} ≤ 0.1 V			8		12		18	Ω
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 1 mA , V _{DS} = 0 V	0.7							V
Dynamic										
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 5 V, I _D = 10 mA, f = 1 kHz	17							mS
Common-Source Output Conductance	g _{os}		0.6							
Drain-Source On-Resistance	r _{ds(on)}	V _{GS} = 0 V, I _D = 0 mA , f = 1 kHz			8		12		18	Ω
Common-Source Input Capacitance	C _{iss}	V _{DS} = 0 V V _{GS} = 0 V f = 1 MHz	SST	60						pF
			J Series	60		85		85		
Common-Source Reverse Transfer Capacitance	C _{rss}	V _{DS} = 0 V V _{GS} = −10 V f = 1 MHz	SST	11						
			J Series	11		15		15		
Equivalent Input Noise Voltage	e _n	V _{DG} = 5 V, I _D = 10 mA f = 1 kHz	3.5							nV/ √Hz
Switching										
Turn-On Time	t _{d(on)}	V _{DD} = 1.5 V, V _{GS(H)} = 0 V See Switching Diagram	3							ns
	t _r		1							
Turn-Off Time	t _{d(off)}		4							
	t _f		18							

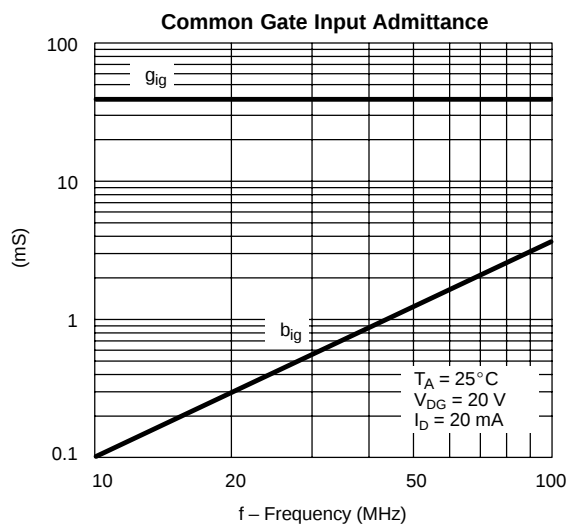
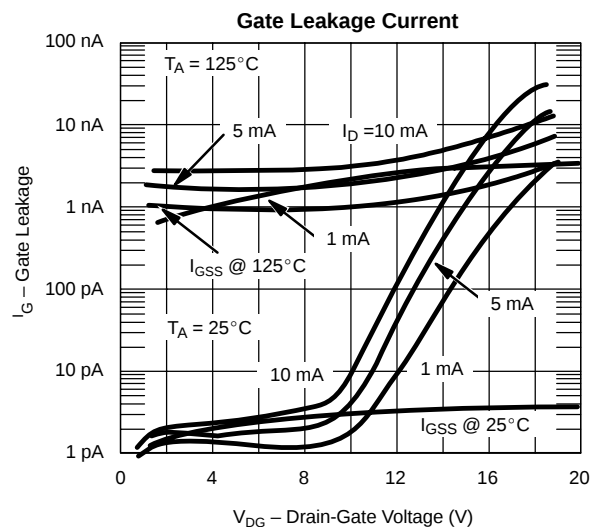
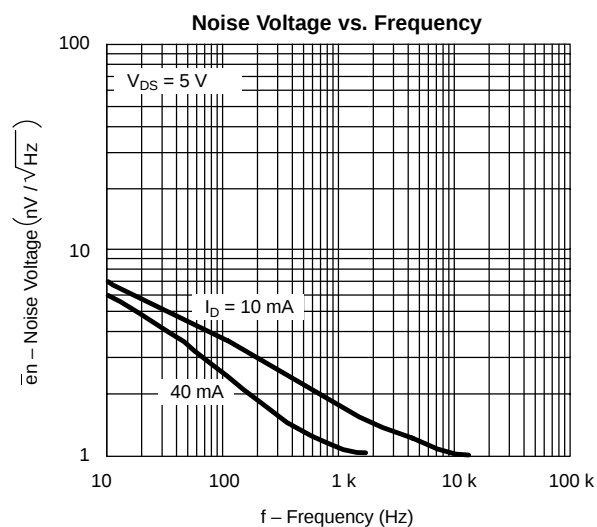
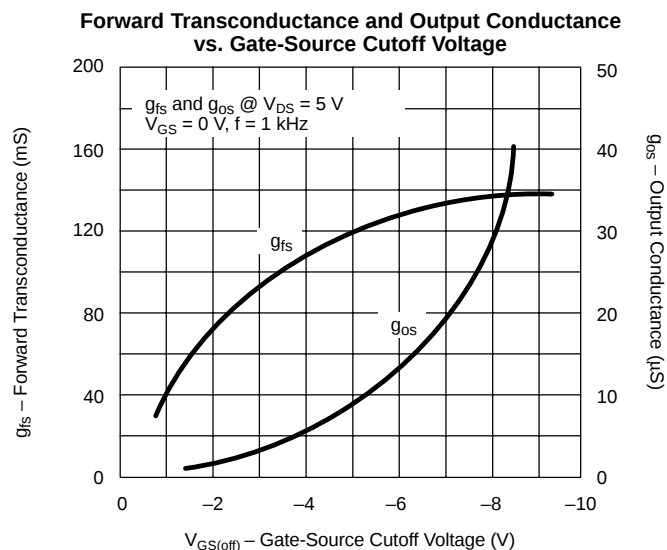
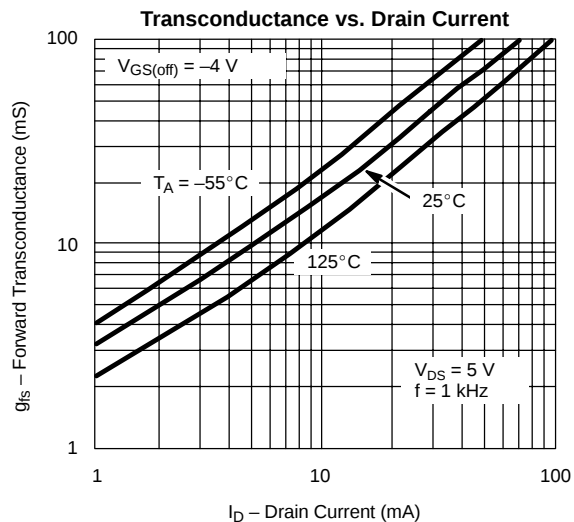
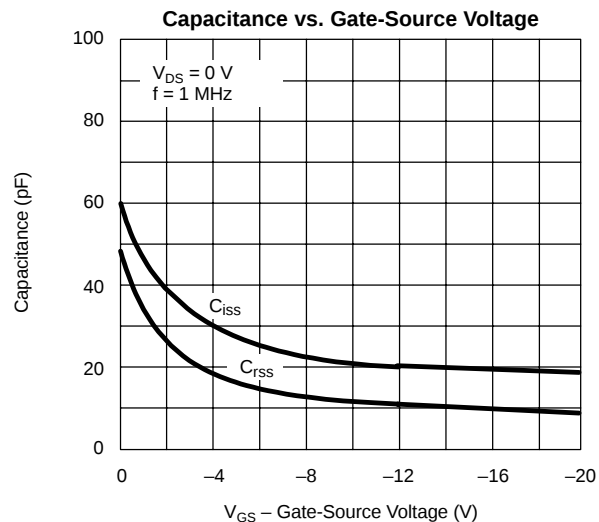
Notes

a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

b. Pulse test: $PW \leq 300\ \mu\text{s}$ duty cycle $\leq 3\%$.

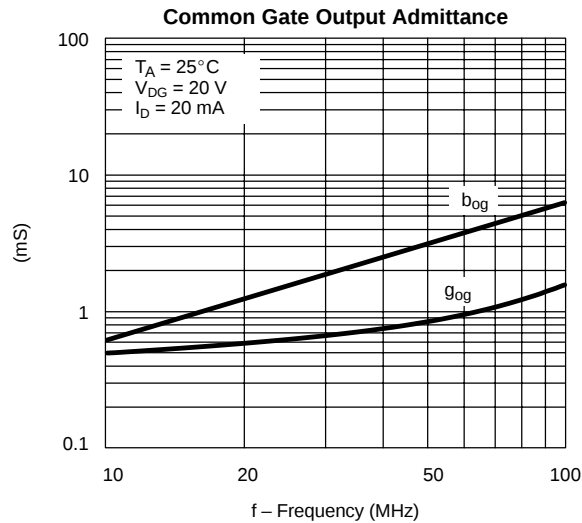
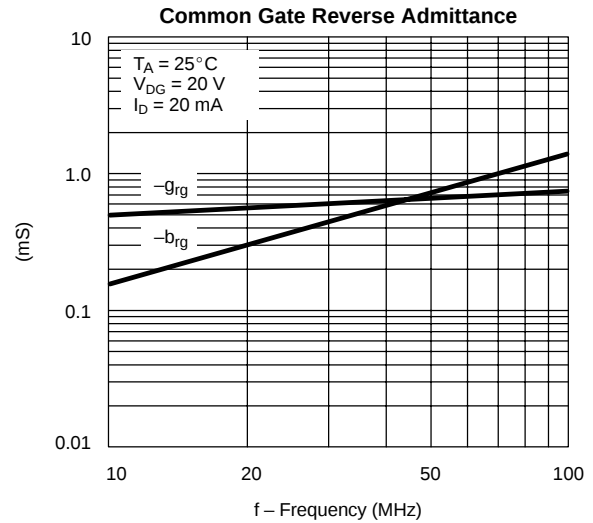
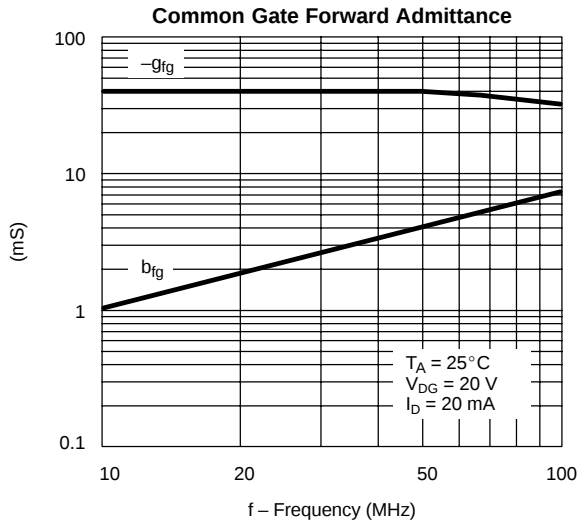
NIP

**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)****On-Resistance and Drain Current vs. Gate-Source Cutoff Voltage****On-Resistance vs. Drain Current****On-Resistance vs. Temperature****Output Characteristics****Turn-On Switching****Turn-Off Switching**

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)




TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



SWITCHING TIME TEST CIRCUIT

	J/SST108	J/SST109	J/SST110
$V_{GS(L)}$	-12 V	-7 V	-5 V
R_L^*	150 Ω	150 Ω	150 Ω
$I_{D(on)}$	10 mA	10 mA	10 mA

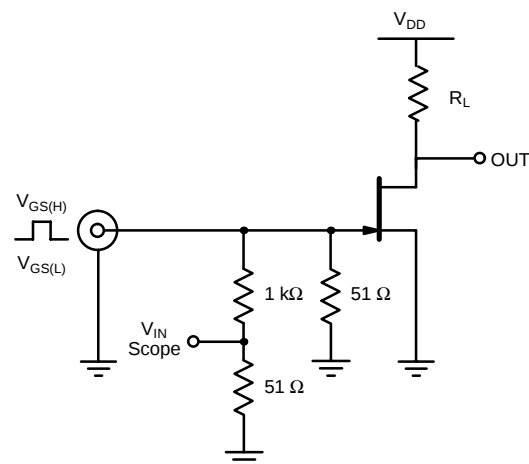
*Non-inductive

INPUT PULSE

Rise Time < 1 ns
Fall Time < 1 ns
Pulse Width 100 ns
PRF 1 MHz

SAMPLING SCOPE

Rise Time 0.4 ns
Input Resistance 10 M Ω
Input Capacitance 1.5 pF





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