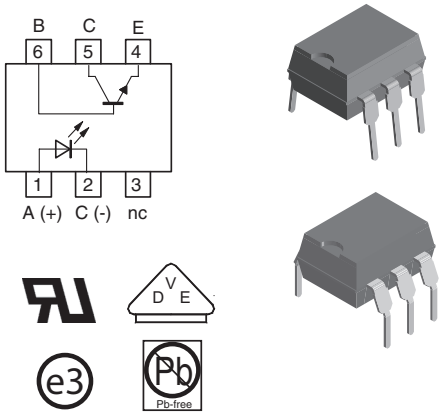
Optocoupler, Phototransistor Output, With Base Connection



Features

- Isolation materials according to UL94-VO
- Pollution degree 2 (DIN/VDE 0110 / resp. IEC 60664)
- Climatic classification 55/100/21 (IEC 60068 part 1)
- Special construction: Therefore, extra low coupling capacity of typical 0.2 pF, high **C**ommon **M**ode **R**ejection
- Low temperature coefficient of CTR
- CTR offered in 3 groups

- Rated isolation voltage (RMS includes DC) V_{IOWM} = 600 V_{RMS} (848 V peak)
- Rated recurring peak voltage (repetitive) V_{IORM} = 600 V_{RMS}
- Creepage current resistance according to VDE 0303/IEC 60112 **C**omparative **T**racking **I**ndex: **CTI** ≥ 275
- Thickness through insulation ≥ 0.75 mm
- Lead-free component
- Component in accordance to RoHS 2002/95/EC and WEEE 2002/96/EC

Agency Approvals

- UL1577, File No. E76222 System Code A, Double Protection
- BSI: BS EN 41003, BS EN 60095 (BS 415), BS EN 60950 (BS 7002), Certificate number 7081 and 7402
- DIN EN 60747-5-2 (VDE0884)
  DIN EN 60747-5-5 pending
- VDE related features:
- Rated impulse voltage (transient overvoltage) V_{IOTM} = 6 kV peak
- Isolation test voltage (partial discharge test voltage) V_{pd} = 1.6 kV
- FIMKO (SETI): EN 60950, Certificate No. 12399

Applications

Circuits for safe protective separation against electrical shock according to safety class II (reinforced isolation):

For appl. class I - IV at mains voltage ≤ 300 V

For appl. class I - III at mains voltage ≤ 600 V according to DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending, table 2, suitable for:

Switch-mode power supplies, line receiver, computer peripheral interface, microprocessor system interface.

Description

The CNY75A/ B/ C/ GA/ GB/ GC consists of a phototransistor optically coupled to a gallium arsenide infrared-emitting diode in a 6-pin plastic dual inline package.

The elements are mounted on one leadframe providing a fixed distance between input and output for highest safety requirements.

VDE Standards

These couplers perform safety functions according to the following equipment standards:

DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending

Optocoupler for electrical safety requirements

IEC 60950/ EN 60950

Office machines (applied for reinforced isolation for mains voltage ≤ 400 VRMS)

VDE 0804

Telecommunication apparatus and data processing

IEC 60065

Safety for mains-operated electronic and related house hold apparatus

Order Information

Part	Remarks
CNY75A	CTR 63 - 125 %, DIP-6
CNY75B	CTR 100 - 200 %, DIP-6
CNY75C	CTR 160 - 320 %, DIP-6
CNY75GA	CTR 63 - 125 %, DIP-6
CNY75GB	CTR 100 - 200 %, DIP-6
CNY75GC	CTR 160 - 320 %, DIP-6

G = Leadform 10.16 mm; G is not marked on the body

For additional information on the available options refer to Option Information.

Absolute Maximum Ratings

T_{amb} = 25 °C, unless otherwise specified

Stresses in excess of the absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute Maximum Rating for extended periods of the time can adversely affect reliability.

Input

Parameter	Test condition	Symbol	Value	Unit
Reverse voltage		V_R	5	V
Forward current		I_F	60	mA
Forward surge current	$t_p \leq 10$ µs	I_{FSM}	3	A
Power dissipation		P_{diss}	100	mW
Junction temperature		T_j	125	°C

Output

Parameter	Test condition	Symbol	Value	Unit
Collector base voltage		V_{CBO}	90	V
Collector emitter voltage		V_{CEO}	90	V
Emitter collector voltage		V_{ECO}	7	V
Collector current		I_C	50	mA
Collector peak current	$t_p/T = 0.5$, $t_p \leq 10$ ms	I_{CM}	100	mA
Power dissipation		P_{diss}	150	mW
Junction temperature		T_j	125	°C

Coupler

Parameter	Test condition	Symbol	Value	Unit
AC isolation test voltage (RMS)	t = 1 min	V_{ISO}	3750	V_{RMS}
Total power dissipation		P_{tot}	250	mW
Ambient temperature range		T_{amb}	- 55 to + 100	°C
Storage temperature range		T_{stg}	- 55 to + 125	°C
Soldering temperature	2 mm from case, t ≤ 10 s	T_{sld}	260	°C

Electrical Characteristics

T_{amb} = 25 °C, unless otherwise specified

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

Input

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Forward voltage	I_F = 50 mA	V_F		1.25	1.6	V
Reverse current	V_R = 6 V	I_R			10	µA
Junction capacitance	V_R = 0, f = 1 MHz	C_j		50		pF

Output

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Collector base voltage	I_C = 100 µA	V_{CBO}	90			V
Collector emitter voltage	I_C = 1 mA	V_{CEO}	90			V
Emitter collector voltage	I_E = 100 µA	V_{ECO}	7			V
Collector-emitter leakage current	V_{CE} = 20 V, I_F = 0	I_{CEO}			150	nA

Coupler

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Collector emitter saturation voltage	I_F = 10 mA, I_C = 1 mA	V_{CEsat}			0.3	V
Cut-off frequency	V_{CE} = 5 V, I_F = 10 mA, R_L = 100 Ω	f_c		110		kHz
Coupling capacitance	f = 1 MHz	C_k		0.3		pF

Current Transfer Ratio

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
I_C/I_F	V_{CE} = 5 V, I_F = 1 mA	CNY75GA	CTR	15			%
		CNY75GB	CTR	30			%
		CNY75GC	CTR	60			%
	V_{CE} = 5 V, I_F = 10 mA	CNY75GA	CTR	63		1.25	%
		CNY75GB	CTR	100		200	%
		CNY75GC	CTR	160		320	%

Switching Characteristics

Parameter	Current	Delay	Rise time	Storage	Fall time	Turn-on time	Turn-off time	Turn-on time	Turn-off time
Test condition	V_{CC} = 5 V, R_L = 100 Ω (see figure 3)							V_{CC} = 5 V, R_L = 1.0 kΩ (see figure 4)	
Symbol	I_F	t_D	t_r	t_S	t_f	t_{on}	t_{off}	t_{on}	t_{off}
Unit	mA	µs	µs	µs	µs	µs	µs	µs	µs
CNY75GA	10	2.0	2.5	0.3	2.7	4.5	3.0	10.0	25.0
CNY75GB	10	2.5	3.0	0.3	3.7	5.5	4.0	16.5	20.0
CNY75GC	10	2.8	4.2	0.3	4.7	7.0	5.0	11.0	37.5

Maximum Safety Ratings

(according to DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending) see figure 1
This optocoupler is suitable for safe electrical isolation only within the safety ratings.
Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Input

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Forward current		I_F			130	mA

Output

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Power dissipation		P_{diss}			265	mW

Coupler

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Rated impulse voltage		V_{IOTM}			6	kV
Safety temperature		T_{si}			150	°C

Insulation Rated Parameters

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Partial discharge test voltage - Routine test	100 %, t_{test} = 1 s	V_{pd}	1.6			kV
Partial discharge test voltage - Lot test (sample test)	t_{Tr} = 60 s, t_{test} = 10 s, (see figure 2)	V_{IOTM}	6			kV
		V_{pd}	1.3			kV
Insulation resistance	V_{IO} = 500 V	R_{IO}	10^{12}			Ω
	V_{IO} = 500 V, $T_{amb} \leq$ 100 °C	R_{IO}	10^{11}			Ω
	V_{IO} = 500 V, $T_{amb} \leq$ 150 °C (construction test only)	R_{IO}	10^{9}			Ω

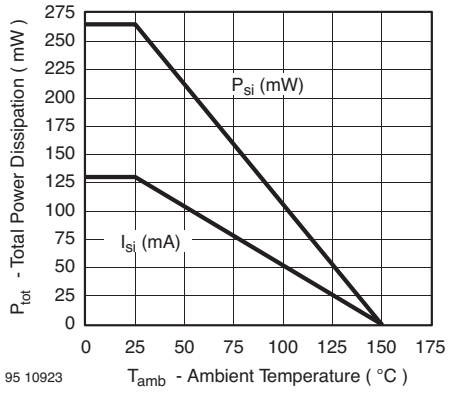


Figure 1. Derating diagram

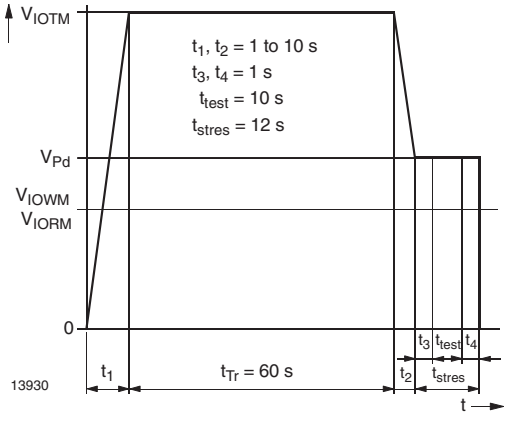


Figure 2. Test pulse diagram for sample test according to DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-; IEC60747

Typical Characteristics (Tamb = 25 °C unless otherwise specified)

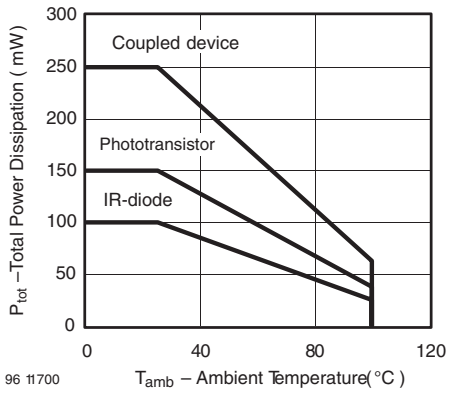


Figure 3. Total Power Dissipation vs. Ambient Temperature

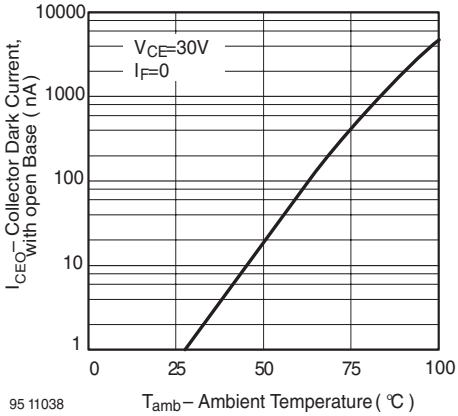


Figure 6. Collector Dark Current vs. Ambient Temperature

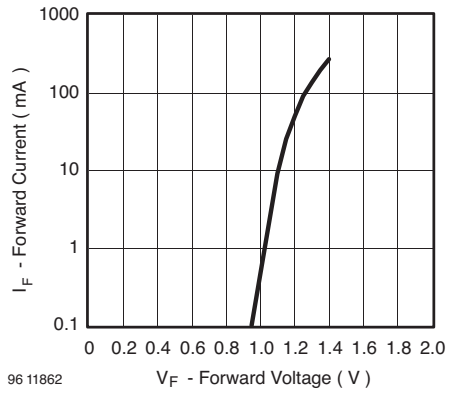


Figure 4. Forward Current vs. Forward Voltage

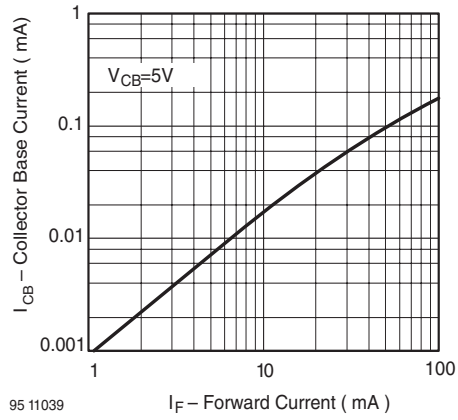


Figure 7. Collector Base Current vs. Forward Current

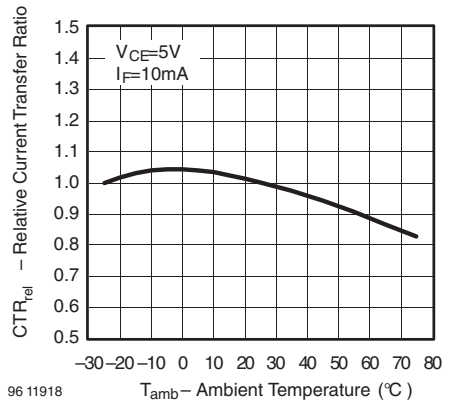


Figure 5. Relative Current Transfer Ratio vs. Ambient Temperature

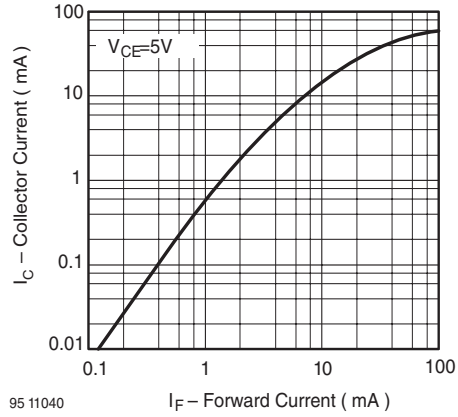


Figure 8. Collector Current vs. Forward Current

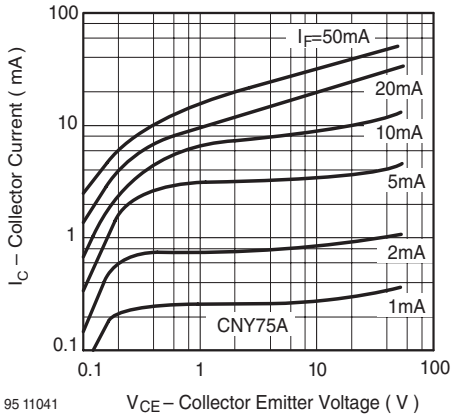


Figure 9. Collector Current vs. Collector Emitter Voltage

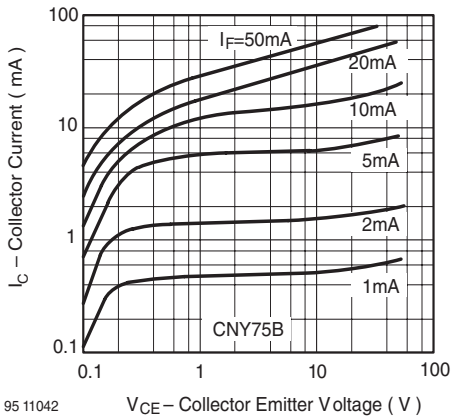


Figure 10. Collector Current vs. Collector Emitter Voltage

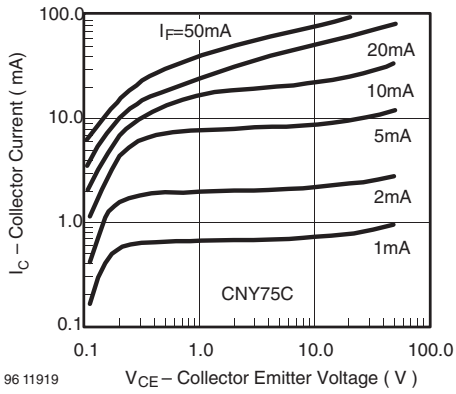


Figure 11. Collector Current vs. Collector Emitter Voltage

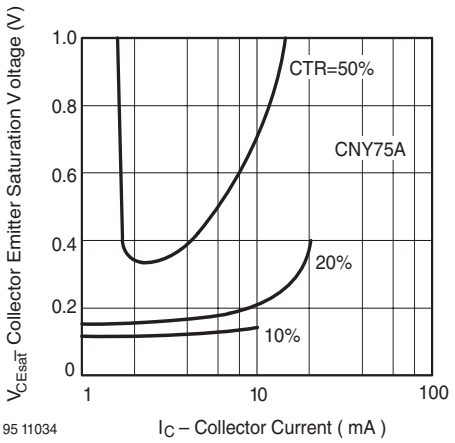


Figure 12. Collector Emitter Saturation Voltage vs. Collector Current

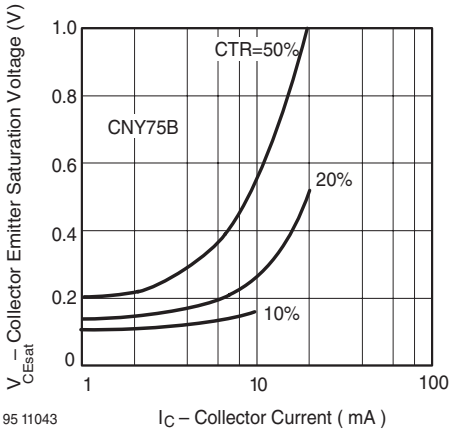


Figure 13. Collector Emitter Saturation Voltage vs. Collector Current

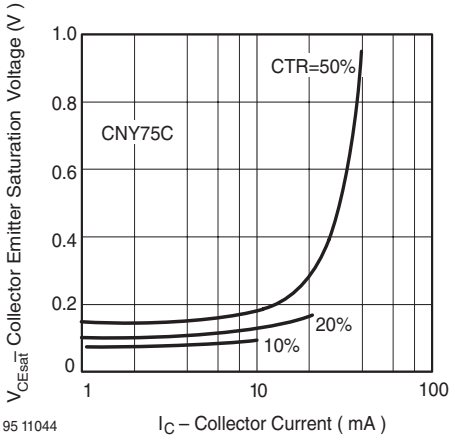


Figure 14. Collector Emitter Saturation Voltage vs. Collector Current

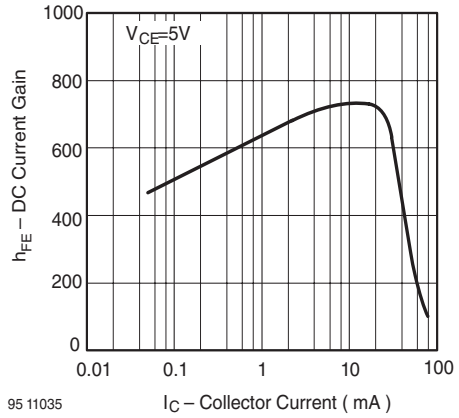


Figure 15. DC Current Gain vs. Collector Current

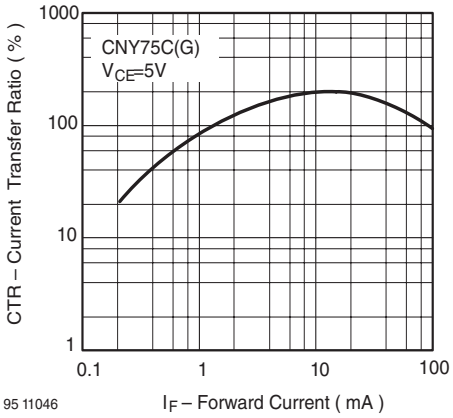


Figure 18. Current Transfer Ratio vs. Forward Current

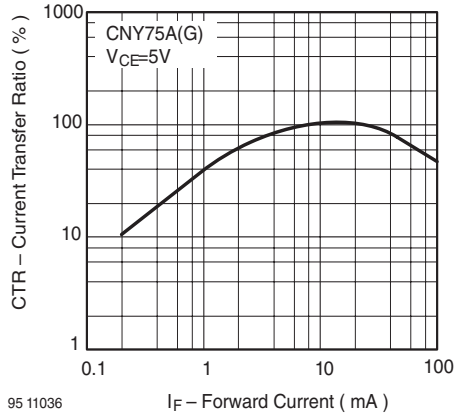


Figure 16. Current Transfer Ratio vs. Forward Current

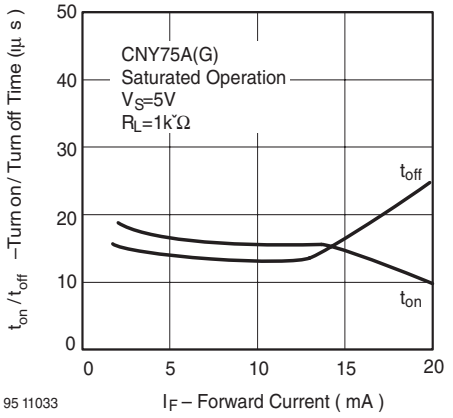


Figure 19. Turn on / off Time vs. Forward Current

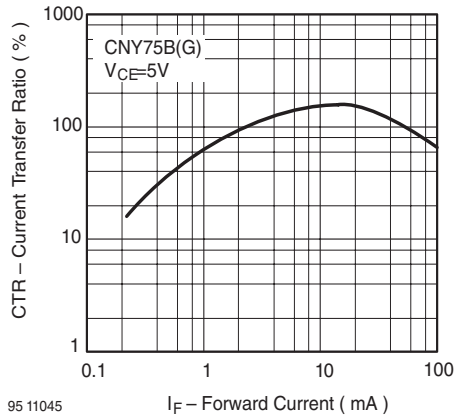


Figure 17. Current Transfer Ratio vs. Forward Current

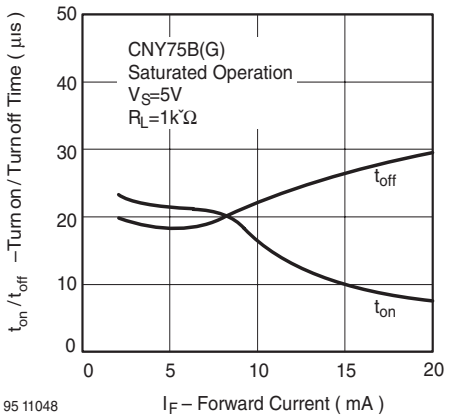


Figure 20. Turn on / off Time vs. Forward Current

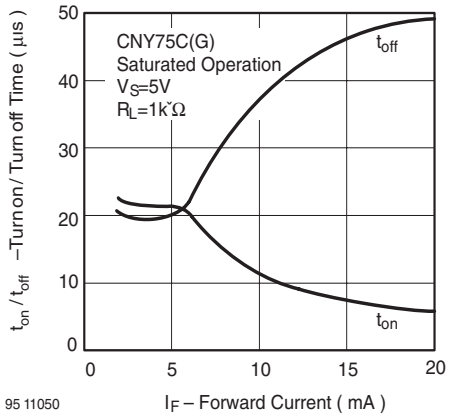


Figure 21. Turn on / off Time vs. Forward Current

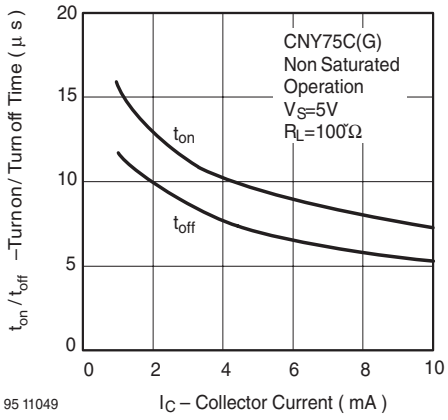


Figure 24. Turn on / off Time vs. Collector Current

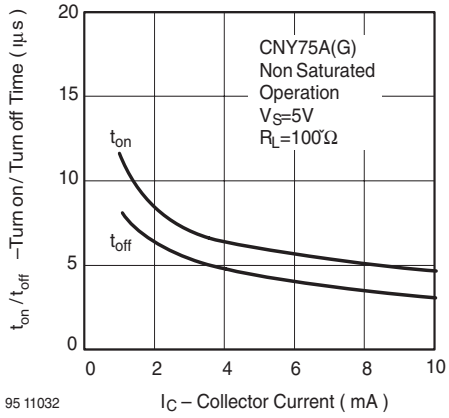


Figure 22. Turn on / off Time vs. Collector Current

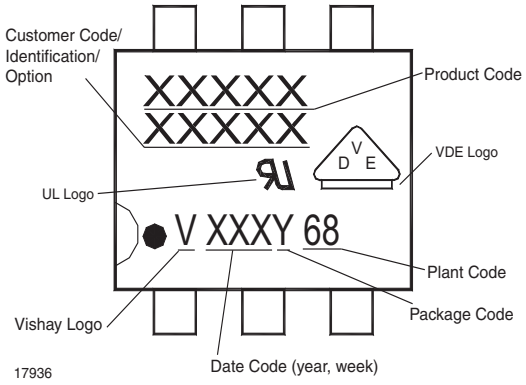


Figure 25. Marking example

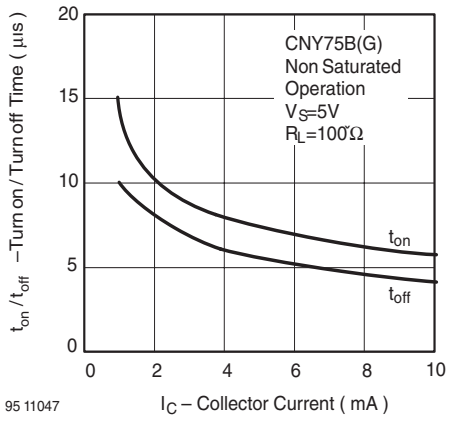
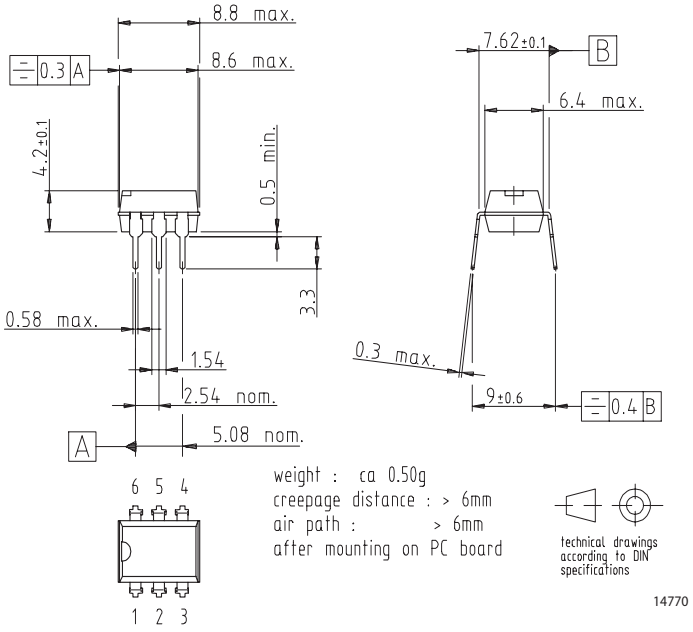
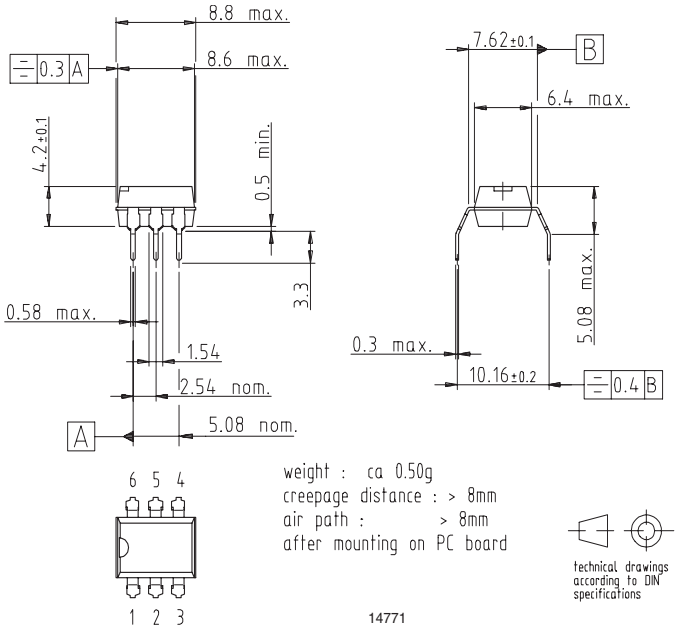


Figure 23. Turn on / off Time vs. Collector Current

Package Dimensions in mm



Package Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operatingsystems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

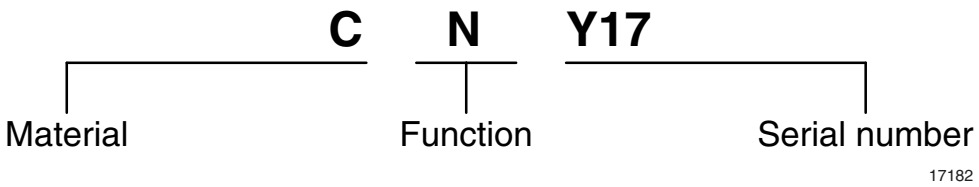
Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423

Conventions Used in Presenting Technical Data

Nomenclature for Semiconductor Devices According to Pro Electron

The type number of semiconductor devices consists of two letters followed by a serial number

For example:



The **first letter** indicates the material used for the active part of the device.

A GERMANIUM
(Materials with a band gap 0.6–1.0 eV) [1)]

B SILICON [2)]
(Materials with a band gap 1.0–1.3 eV) [1)]

C GALLIUM-ARSENIDE 2)
(Materials with a band gap > 1.3 eV) [1)]

R COMPOUND MATERIALS
(For instance Cadmium-Sulfide)

The **second letter** indicates the circuit function:

A DIODE: detection, switching, mixer

B DIODE: variable capacitance

C TRANSISTOR: low power, audio frequency

D TRANSISTOR: power, audio frequency

E DIODE: tunnel

F TRANSISTOR: low power, high frequency

G DIODE: oscillator, miscellaneous

H DIODE: magnetic sensitive

K HALL EFFECT DEVICE: in an open magnetic circuit

L TRANSISTOR: power, high frequency

M HALL EFFECT DEVICE: in a closed magnetic circuit

N PHOTO COUPLER [2)]

P DIODE: radiation sensitive [2)]

Q DIODE: radiation generating

R THYRISTOR: low power

S TRANSISTOR: low power, switching

T THYRISTOR: power

U TRANSISTOR: power, switching

X DIODE: multiplier, e.g. varactor, step recovery

Y DIODE: rectifying, booster

Z DIODE: voltage reference or voltage regulator. transient suppressor diode

The **serial number** consists of:

- Three figures, running from 100 to 999, for devices primarily intended for consumer equipment
- One letter (Z, Y, X, etc.) and two figures, running from 10 to 99, for devices primarily intended for professional equipment

A version letter can be used to indicate a deviation of a single characteristic, either electrically or mechanically.

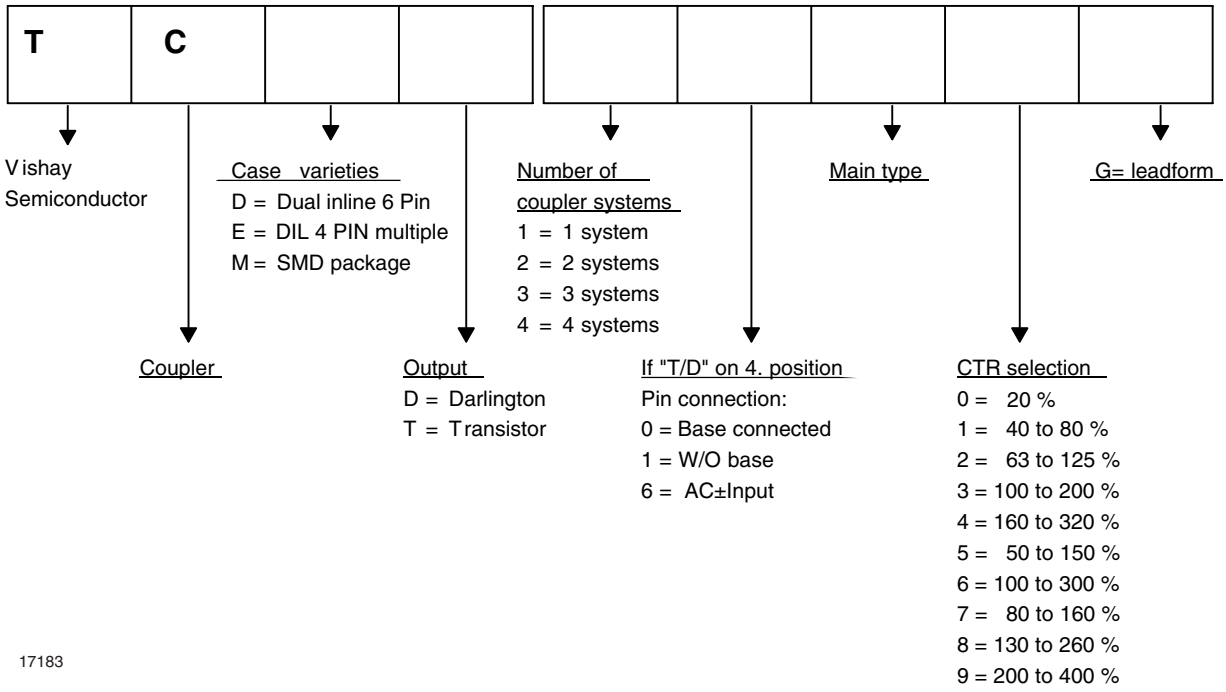
The letter never has a fixed meaning, the only exception being the letter R, indicating reversed voltage, i.e. collector to case.

[1)] The materials mentioned are examples

[2)] Used for Optoelectronic products

Type Designation Code for Optocouplers

Optocouplers



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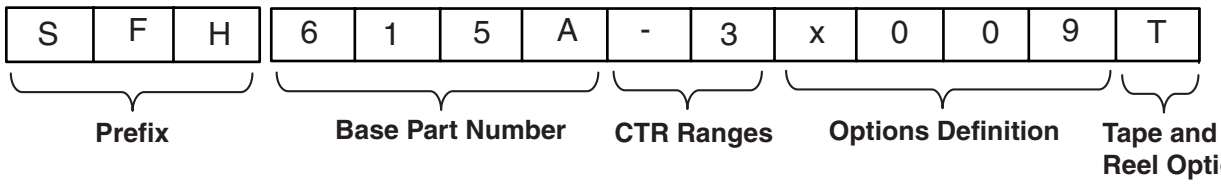
General Optocoupler Nomenclature for BRT, IL and SFH series



BRT
IL
ILD
ILQ
SFH6

1 = 40 % to 80 %
2 = 63 % to 125 %
3 = 100 % to 200 %
4 = 160 % to 320 %
5 = 250 % to 500 %

Option 1 Optocouplers for Safe Electrical Insulation per DIN VDE 0884
Option 6 Optocouplers with 10.16mm (0.4") through hole lead spread.
Option 7 Optocouplers with SMD lead form bend, 0.9 mm maximum standoff height
Option 8 Optocouplers with 10.16mm (0.4") SMD lead form bend
Option 9 Optocouplers with SMD lead form bend, 0.25 mm maximum standoff height

Option 1 may be combined with the other lead forming options.
Option T may only be combined with Options 7, 8, and 9

Examples:
CNY17F-2X017T
4N35-X016
BRT12H-X009T

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General Description

Basic Function

In an electrical circuit, an optocoupler ensures total electric isolation, including potential isolation, as in the case of a transformer, for instance.

In practice, this means that the control circuit is located on one side of the optocoupler, i.e., the emitter side, while the load circuit is located on the other side, i.e., the detector side. Both circuits are electrically isolated by the optocoupler. Signals from the control circuit are transmitted optically to the load circuit. In most cases, this optical transmission is realized with light beams whose wavelengths span the red to infrared range, depending on the requirements applicable to the optocoupler. The bandwidth of the signal to be transmitted ranges from a dc voltage signal to frequencies in the MHz band. An optocoupler is comparable to a transformer or relay. Besides having smaller dimensions in most cases, the advantages of optocouplers are: shorter switching times, no contact bounce, no interference caused by arcs, wear the circuitry*). Optocouplers are suitable for circuits used in microelectronics, data processing and telecommunication systems. Optocouplers are used to an increasing extent as safety tested components, e. g., in switch mode power supplies.

*)Note: See Applications Notes for additional information.

Design

An optocoupler has to fulfill 5 essential requirements:

- Good isolation
- High current transfer ratio (CTR)
- Low degradation
- Low coupling capacitance
- No interference by field strength influences

These factors are essentially dependent on the design, the materials used and the corresponding chips used for the emitter/detector.

Vishay has succeeded in achieving a design with optimized isolation behavior and good transfer characteristics. The basic function of an optocoupler is to isolate the input from the output by means of an insulation material.

The thickness–through–insulation of at least 4 mm provided by Vishay provides better safety and protection against electrical shock (see figure 1 and 2). Vishay builds in additional reliability in these devices to protect the coupler system against ambient light and dust.

The mechanical clearance between the emitter and detector is at least 4 mm and is thus mechanically stable even under thermal overloads, i.e., the possibility of a short circuit caused by material short circuit is minimized. This is important for optocouplers which must meet strict safety requirements (VDE/UL specifications), see DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending Facts and Information. As a result, Vishay couplers have a very low coupling capacitance of 0.2 pF. Couplers with conventional designs have higher coupling capacitance values by a factor of 1.3 - 2. Attention must be paid to the coupling capacitance in digital circuits in which steep pulse edges are produced which superimpose themselves on the control signal. With a low coupling capacitance, the transmission capabilities of these interference spikes are effectively suppressed between the input and output. This capability of suppressing dynamic interferences is commonly known as "common-mode rejection"*).

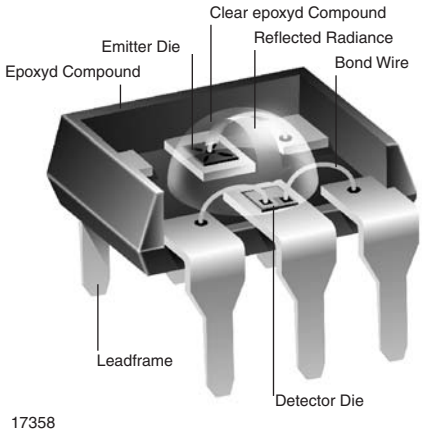


Figure 1.Coplanar Construction Principle

*)Note: See Applications Notes for additional information.

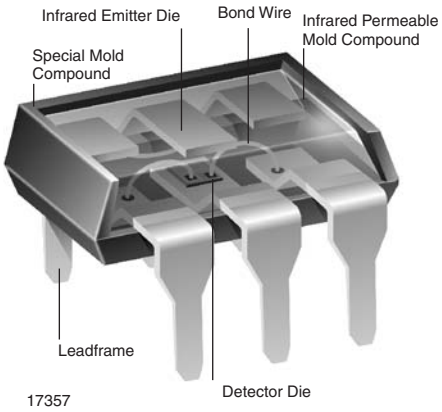


Figure 2.Face to Face Construction Principle

The degradation of an optocoupler, i.e., impairment of its CTR over a finite period, depends on:

1) the emitter element due to its decreasing radiation power while.

2) the degradation of an optocoupler over time results primarily from the emitter chip.

A decrease in the radiation power can be primarily ascribed to thermal stress caused by an external, high ambient temperature and/or high a forward current. In practice, optocouplers are operated with forward current of 1 to 30 mA through the emitting diode. In this range, degradation at an average temperature of 40 °C is less than 5 % after 1000 h. In general, an optocoupler's life time is a period of 100.000 h, i.e, the CTR should not have dropped below 50 % of its value at 0 hours during this time (see figure 4).

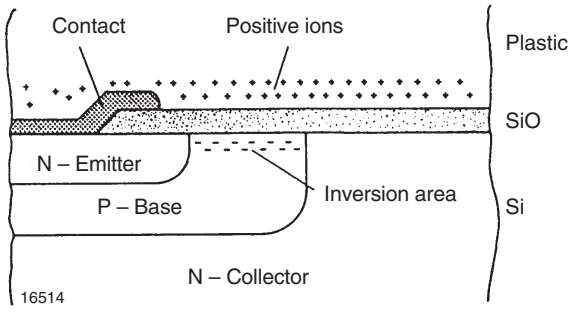


Figure 3.Function of parasitic field effect transistor as a result of failure (latch-up) in the phototransistor of couplers

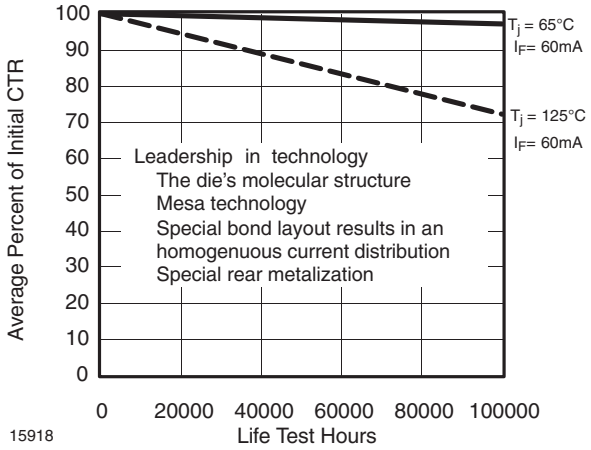


Figure 4.Degradation under typical operating conditions

Technical Description – Assembly

Emitter

Emitters are manufactured using the most modern Liquid Phase Epitaxy (LPE) process. By using this technology, the number of undesirable flaws in the crystal is reduced. This results in a higher quantum efficiency and thus higher radiation power. Distortions in the crystal are prevented by using mesa technology which leads to lower degradation. A further advantage of the mesa technology is that each individual chip can be tested optically and electrically even on the wafer.

Detector

Vishay detectors have been developed so that they match to the emitter. They have low capacitance values, high photosensitivity and are designed for an extremely low saturation voltage. Silicon nitride passivation protects the surface against possible impurities.

Assembly

The components are fitted onto lead frames by fully automatic equipment using conductive epoxy or eutectic adhesive. Contacts are established automatically with digital pattern recognition using the well-proven thermosonic technique. In addition to optical and mechanical check mechanical checks, all couplers are measured at a temperature of 100 °C on short/open test equipment.

Option Information

Optocoupler lead-bend configurations are available as options. In addition, partial discharge testing as per VDE/IEC is also available as an option.

See the Order Information section in the data sheet to determine if and which options are available to a specific product. Contact the Vishay sales office for other option configurations. The options are :

Option 1 VDE Option

Option 6 400 mil (10.16 mm) lead spread DIP configuration

Option 7 Surface mount, gull wing DIP configuration with standoff

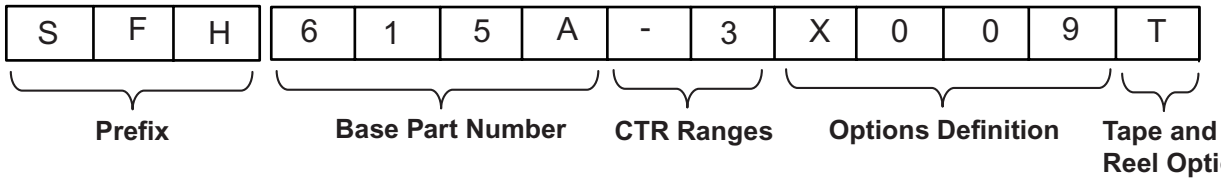
Option 8 Surface mount, gull wing DIP configuration with increased clearance

Option 9 Surface mount, gull wing DIP configuration

Ordering Options

A specific option or combination of options can be ordered by add the options Definition field following the Base Part Number and CTR Range (if applicable) as presented in the following example:

General Optocoupler Nomenclature for BRT, IL and SFH series



BRT
II
ILD
ILQ
SFH6

1 = 40 % to 80 %
2 = 63 % to 125 %
3 = 100 % to 200 %
4 = 160 % to 320 %
5 = 250 % to 500 %

Option 1 Optocouplers for Safe Electrical Insulation per DIN VDE 0884
Option 6 Optocouplers with 10.16mm (0.4") through hole lead spread.
Option 7 Optocouplers with SMD lead form bend, 0.9 mm maximum standoff height
Option 8 Optocouplers with 10.16mm (0.4") SMD lead form bend
Option 9 Optocouplers with SMD lead form bend, 0.25 mm maximum standoff height

Option 1 may be combined with the other lead forming options.
Option T may only be combined with Options 7, 8, and 9

Examples:

CNY17F-2X017T	CNY17F-2, SMD, gull-wing configuration with standoff, VDE approved, on tape and Reel.
4N35-X016	4N35, 400 mil lead spread, VDE approved.
BRT12H-X009T	BRT12H, SMD, gull-wing configuration, on tape and reel
SFH615-3X001	SFH615-3, DIP, VDE approved

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This field is always 4 characters long and commences with the character X. In the case of surface mounted products in Tape and Reel format, the tape and reel option character “T” will follow this field. The possible combinations for these Fields[1] are:

X001, X006, X007, X008, X009, X001T[2], X007T, X008T, X009T, X016, X017, X018, X019, X017T, X018T, X019T

Notes:

[1] Not all options are available for all product types.

[2] The X001T option is only available on products that are available on the following SMD products SFH6106, SFH6156, SFH6186, SFH6206 and SFH6286 series, e.g. SFH6106-3X001T

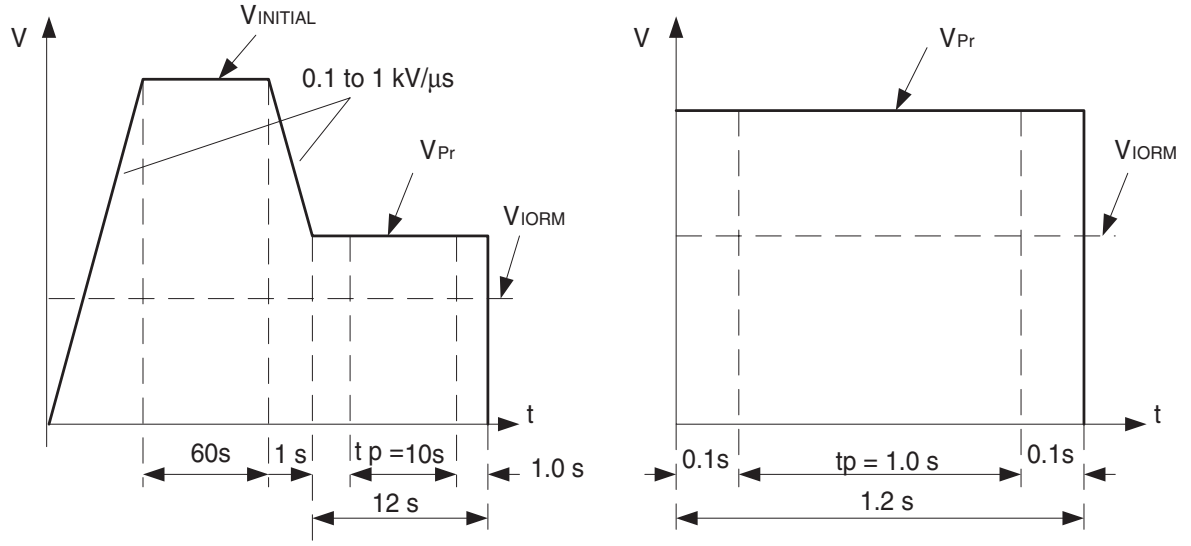
Option 1
Optocouplers for Safe Electrical Insulation per DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending*

The optocoupler listed are suitable for safe electrical insulation only within the safety maximum ratings. Compliance with the safety maximum ratings must be ensured by protective circuits.

The partial discharge measurement ensures that no partial discharge occurs during operation at maximum permissible operating insulation voltage (V_{IORM}). Permanent partial discharge affects the insulating materials and can result in a high voltage breakdown.

It is recommended that tests with the insulation test voltage (V_{ISOL}) should not be made, otherwise partial discharge may occur impairing the insulation characteristics. Thus partial discharges also may occur at the maximum permissible operating insulation voltage.

The insulation test per DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending is carried out after all the other tests.



tp: measuring time for par tial dischage

Procedure a.
Type and sampling tests, destructive tests

tp: measuring time for par tial dischage

Procedure b.
Routine tests, non-destructive tests

17928-1

Figure 1. Time Voltage Diagram per DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending*

* DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending. edition January 2003

Description	Symbol	System 1			Unit
		DIP4	DIP8	DIP16	
		SFH610A-..	ILCT6	ILQ1/2/5/74	
		SFH615A-..	ILD1/2/5/74	ILQ30/31/55	
		SFH615AA-..	ILD30/31/55	ILQ32	
		SFH615AGB-..	ILD32	ILQ66-..	
		SFH615AGR-..	ILD66-..	ILQ615-..	
		SFH617A-..	ILD250/1/2	ILQ620-..	
		SFH618A-..	ILD255	ILQ620GB-..	
		SFH620A-..	ILD621GB-..	ILQ621-..	
		SFH620AA-..	ILD621-..	ILQ621GB-..	
		SFH620AGB-..	ILD621GB-..		
		SFH628A-..	ILD755-..		
		SFH6106-..	ILD766-..		
		SFH6116-..	MCT6		
		SFH6156-..			
		SFH6186-..			
		SFH6206-..			
		SFH6286-..			
Installation Category (DIN VDE 0110)					
for Rated Line Voltages ≤ 300 V_{RMS}		I- IV			
for Rated Line Voltages ≤ 600 V_{RMS}		I- IV			
for Rated Line Voltages ≤ 1000 V_{RMS}		I- III			
IEC Climatic Category (DIN IEC 60068 Part 1/9.80)		55/100/21			
Pollution Degree (DIN VDE 0110 Part 1/1.89)		2			
Maximum Operation Insulating Voltage *)	V_{IORM}	890			V
Test Voltage Input/Output, Procedure b *) V_{Pr} = 1.875 x V_{IORM}, Routine 100 % Test, tp = 1 s, Partial Discharge < 5 pC	V_{Pr}	1669			V
Test Voltage Input/Output, Procedure a *) V_{Pr} = 1.5 x V_{IORM}, Type and Sampling Test tp = 60 s, Partial Discharge < 5 pC	V_{Pr}	1335			V
Maximum Permissible Overvoltage (Transient Overvoltage)	V_{IOTM}	8000			V
Partial Discharge Test Voltage *)	$V_{INITIAL}$	8000			V
Safety Maximum Ratings (Maximum Permissible Ratings in Case of a Fault, also Refer to Diagram) Package Temperature Current (Input Current I_F, P_{Si} = 0, T_A = 25 °C) Derating with Higher Ambient Temp. Power (Output or Total Power Dissipation, T_A = 25 °C) Derating with Higher Ambient Temp.	 T_{si} I_{si} DI_{Si} P_{Si} ΔP_{Si}	 175 275 - 1.83 400 - 2.67			 °C mA mA/K mW mW/K
Insulation Resistance at T_{Si} $V_{I/O}$ = 500 V	R_{IS}	> 10^9			W

Description	Symbol	System 2			Unit
		4N25/26/27/28	IL250	MCT5210	
		4N35/36/37/38/39	IL251	MCT5211	
		4N32/33	IL252	SFH600-..	
		CNY17-..	IL255-..	SFH601-..	
		CNY17F-..	IL400	SFH608-..	
		H11A-..	IL755-..	SFH640-..	
		H11AA1-..	IL755B-..	MOC8050	
		H11B-..	IL766-..	IL56B-..	
		H11B1-..	IL766B-..	MOC8021	
		H11C-..	MCA230/231	MOC8112	
		H11D-..	MCA255	MOC8102/03/ 04/05	
		IL1/2/5/74	MCT2/2E		
		IL2B-..	MCT270/271		
		IL30/31/55	MCT272		
		IL55B-..	MCT273/274		
		IL66-..	MCT275		
		IL66B-..	MCT276/277		
		IL201/202/203			
Installation Category (DIN VDE 0110)					
for Rated Line Voltages ≤ 300 V_{RMS}		I-IV			
for Rated Line Voltages ≤ 600 V_{RMS}		I-IV			
for Rated Line Voltages ≤ 1000 V_{RMS}		I-III			
IEC Climatic Category (DIN IEC 60068 Part 1/9.80)		55/100/21			
Pollution Degree (DIN VDE 0110 Part 1/1.89)		2			
Maximum Operation Insulating Voltage *)	V_{IORM}	890			V
Test Voltage Input/Output, Procedure b *) V_{Pr} = 1.875 x V_{IORM}, Routine 100 % Test, tp = 1 s, Partial Discharge < 5 pC	V_{Pr}	1669			V
Test Voltage Input/Output, Procedure a *) V_{Pr} = 1.5 x V_{IORM}, Type and Sampling Test tp = 60 s, Partial Discharge < 5 pC	V_{Pr}	1335			V
Maximum Permissible Overvoltage (Transient Overvoltage)	V_{IOTM}	8000			V
Partial Discharge Test Voltage *)	$V_{INITIAL}$	8000			V
Safety Maximum Ratings (Maximum Permissible Ratings in Case of a Fault, also Refer to Diagram) Package Temperature Current (Input Current I_F, P_{Si} = 0, T_A = 25 °C) Derating with Higher Ambient Temp. Power (Output or Total Power Dissipation, T_A = 25 °C) Derating with Higher Ambient Temp.	 T_{si} I_{si} DI_{Si} P_{Si} ΔP_{Si}	 175 400 - 2.67 700 - 4.67			 °C mA mA/K mW mW/K
Insulation Resistance at T_{Si} $V_{I/O}$ = 500 V	R_{IS}	> 10^9			W

Description	Symbol	System 4 **)	System 5	System 7	Unit
		IL410	6N135	IL300	
		IL420	6N136	IL300E	
		IL4116	SFH6135	IL300F	
		IL4117	SFH6136	IL300EF	
		IL4118	6N138	IL300DEFG	
		IL4216	SFH6138		
		IL4217	SFH6139		
		IL4218	6N139		
			SFH6345		
Installation Category (DIN VDE 0110)					
for Rated Line Voltages ≤ 300 V_{RMS}		I-IV	I-IV	I-IV	
for Rated Line Voltages ≤ 600 V_{RMS}		I-III	I-IV	I-IV	
for Rated Line Voltages ≤ 1000 V_{RMS}		I-II	I-III	I-III	
IEC Climatic Category (DIN IEC 60068 Part 1/9.80)		55/100/21	55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110 Part 1/1.89)		2	2	2	
Maximum Operation Insulating Voltage *)	V_{IORM}	850	630	890	V
Test Voltage Input/Output, Procedure b *) V_{Pr} = 1.875 x V_{IORM}, Routine 100 % Test, tp = 1 s, Partial Discharge < 5 pC	V_{Pr}	1594	1181	1669	V
Test Voltage Input/Output, Procedure a *) V_{Pr} = 1.5 x V_{IORM}, Type and Sampling Test tp = 60 s, Partial Discharge < 5 pC	V_{Pr}	1275	945	1335	V
Maximum Permissible Overvoltage (Transient Overvoltage)	V_{IOTM}	6000	8000	8000	V
Partial Discharge Test Voltage *)	$V_{INITIAL}$	6000	8000	8000	V
Safety Maximum Ratings (Maximum Permissible Ratings in Case of a Fault, also Refer to Diagram) Package Temperature Current (Input Current I_F, P_{Si} = 0, T_A = 25 °C) Derating with Higher Ambient Temp. Power (Output or Total Power Dissipation, T_A = 25 °C) Derating with Higher Ambient Temp.	 T_{si} I_{si} DI_{Si} P_{Si} ΔP_{Si}	 175 250 - 1.65 500 - 3.33	 175 300 - 2 500 - 3.33	 165 235 - 1.57 465 - 3.1	 °C mA mA/K mW mW/K
Insulation Resistance at T_{Si} $V_{I/O}$ = 500 V	R_{IS}	> 10^9	> 10^9	> 10^9	W

All voltages referred to are peak values except otherwise specified.

*) See time-test voltage diagram
**) In preparation

Testing input/output voltage requires all input pins and all output pins to be shorted.

Option 1: Tested per DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending

Option 6: Wide lead spacing (10.16 mm creepage/clearance distances > 8 mm)

Option 7: Surface mount leads (creepage/clearance distances > 8 mm)

Option 8: Surface mount leads

Option 9: Surface mount leads

See CECC 00802, edition 1, for soldering conditions for SMT devices (option 7 and 9).

"-.." means dash selections.

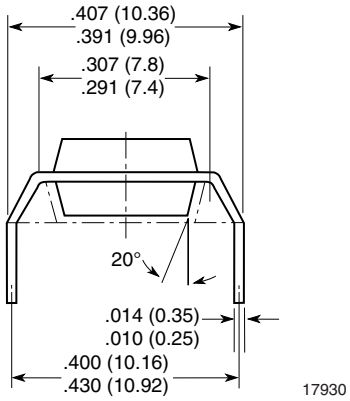
Option 6
DIP Optocouplers with 0.4" (10.16 mm) Lead Spread.

The leads of the optocouplers are bent according to a spacing of 0.4" (10.16 mm). Dimensions deviating from the standard type are:

Lead spacing	10.16 mm (0.4")
Creepage distance	> 8.0 mm
Clearance	> 8.0 mm

This version additionally complies with the following standards:

- IEC 60950 DIN VDE 0805/05 90 (System 2 and 3 only) Reinforced insulation up to an operating voltage of 400 V_{RMS} or DC



Clearance-creepage distance = 8.0 min.
See standard version for pin configuration

Option 7
Lead Bends for Surface Mount Optocouplers

These optocouplers are suitable for surface mounting. Dimensions deviating from the standard type are:

Creepage distance > 8.0 mm

Clearance > 8.0 mm

This version additionally complies with the following standards:

- IEC 60950 DIN VDE 0805/05 90 (System 2 and 3 only) Reinforced insulation up to an operating voltage of 400 V_{RMS} or DC

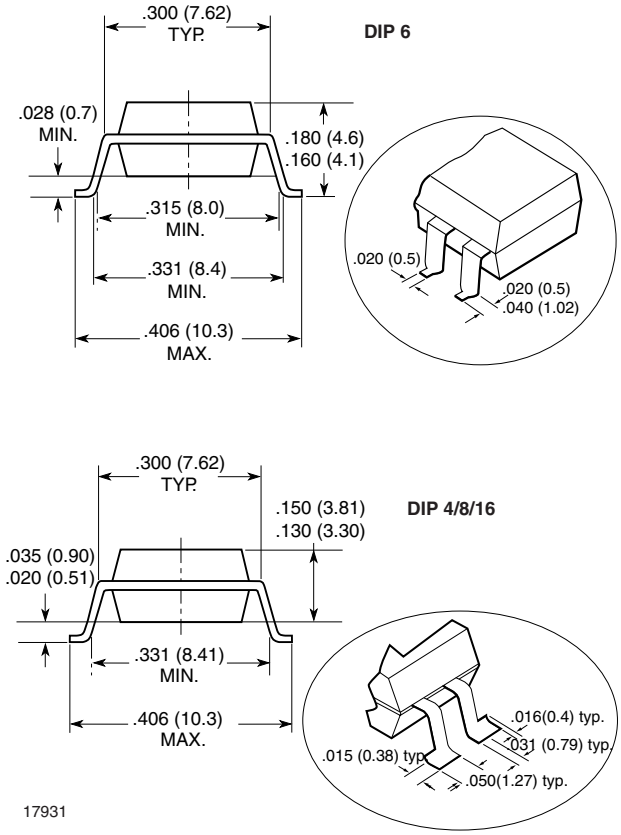
During the soldering process, the package should not be wetted with tin-lead solder to prevent the impairment of the isolation features. Apart from iron soldering, only reflow soldering methods (vapor phase, infrared and hot gas) are permissible.

Permissible soldering conditions:
260 °C at 10 seconds to 215 °C at 30 seconds

The soldering process may be repeated two times at the most. Attention must be paid to the cooling down of the device to 25 °C between the soldering processes.

Clearance and creepage distances must be considered for the solder pad design.

Clearance-creepage distance = 8.0 min.
See standard version for pin configuration.



Option 8
Lead Bends for Surface Mount Optocouplers

These optocouplers are suitable for surface mounting. Dimensions deviating from the standard type are:

Creepage distance > 8.0 mm

Clearance > 8.0 mm

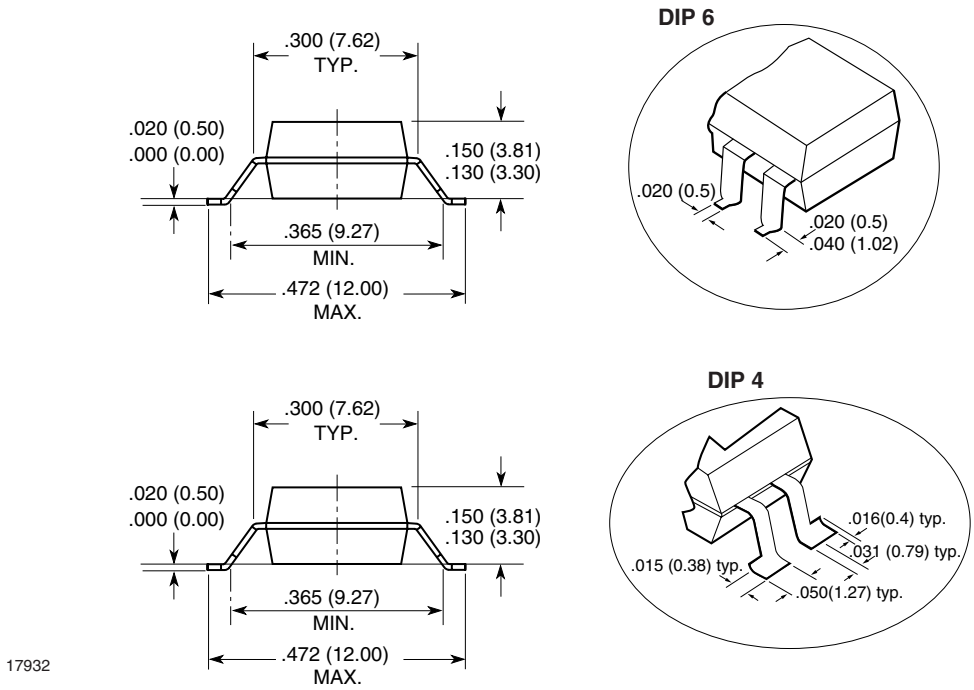
This version additionally complies with the following standards:

- IEC 60950 DIN VDE 0805/05 90 (System 2 and 3 only) Reinforced insulation up to an operating voltage of 400 V_{RMS} or DC

During the soldering process, the package should not be wetted with tin-lead solder to prevent the impairment of the isolation features. Apart from iron soldering, only reflow soldering methods (vapor phase, infrared and hot gas) are permissible.

Permissible soldering conditions:
260 °C at 10 seconds to 215 °C at 30 seconds

The soldering process may be repeated two times at the most. Attention must be paid to the cooling down of the device to 25 °C between the soldering processes.



Clearance and creepage distances must be considered for the solder pad design.

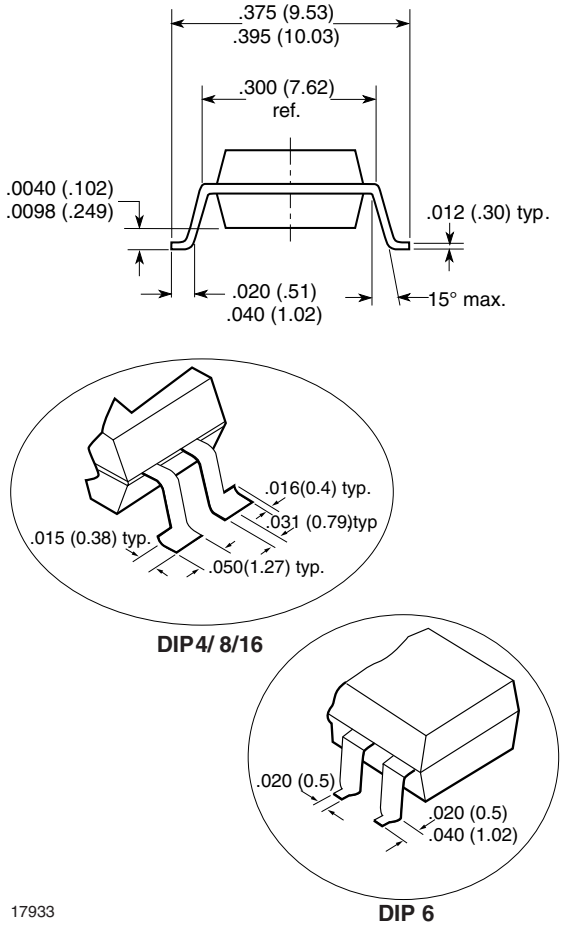
Clearance-creepage distance = 8.0 min.
See standard version for pin configuration.

Option 9
Lead Bends for Surface Mount Optocouplers

During the soldering process, the package should not be wetted with tin-lead solder to prevent the impairment of the isolation features. Apart from iron soldering, only reflow soldering methods (vapor phase, infrared and hot gas) are permissible.

Permissible soldering conditions:
260 °C at 10 seconds to 215 °C at 30 seconds

The soldering process may be repeated two times at the most. Attention must be paid to the cooling down of the device to 25 °C between the soldering processes.



Markings

The following table defines the option information that is marked on the product.

Option type	Marking
X001, X001T	X001
X006	No mark
X007, X007T	X007
X008, X008T	X008
X009, X009T	No Mark
X016	X001
X017, X017T	X017
X018, X018T	X018
X019, X019T	X001

More Speed from Optocouplers (Appnote 5)

Figure 1 shows a typical circuit employing an optocoupler to transmit logic signals between electrically isolated parts of a system. In the circuit shown, the optocoupler must "sink" the current from one T^2L load plus a pull-up resistor to V_{CC}. The resistor in series with the LED half of the optocoupler must supply the worst case load current divided by the "current transfer ratio" or CTR of the optocoupler. If an IL1 optocoupler is used, having a minimum CTR of 0.2, and 80 percent variation in the load is allowed, 8.1 mA is required. This is supplied by the 430 Ω resistor.

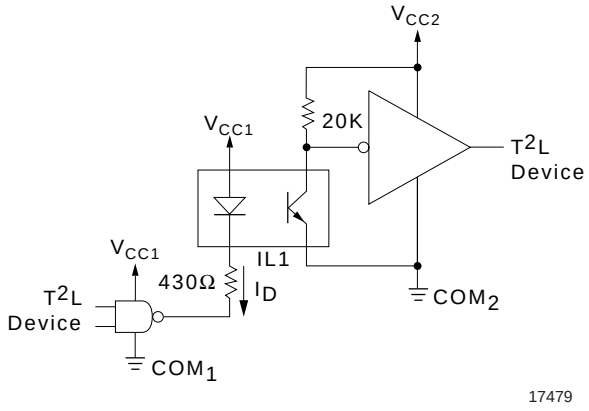


Figure 1.

The maximum repetition rate at which this circuit will operate is only about 8 kHz. The severe speed limitation is due entirely to the characteristics of the phototransistor half of the optocoupler. This device has a large base-collector junction area and a very thick base region in order to make it sensitive to light. C_{ob} is typically 25 pF. This capacitance is, in the circuit of Figure 1, effectively multiplied by a large factor due to the "Miller effect." Also, because the base region volume is large, so is base storage time.

A very simple method of reducing both of these effects is to add a resistor between the base and emitter as shown in Figure 2. This resistor helps by reducing the time constant due to C_{ob} and by removing stored charge from the base region faster than recombination can. When a base-emitter resistor is used, of course, the required LED drive is increased since much of the photo-current generated in the base-collector junction is now deliberately "dumped."

Using this method does not usually result in a large power supply current drain since average repetition rate is low in most applications.

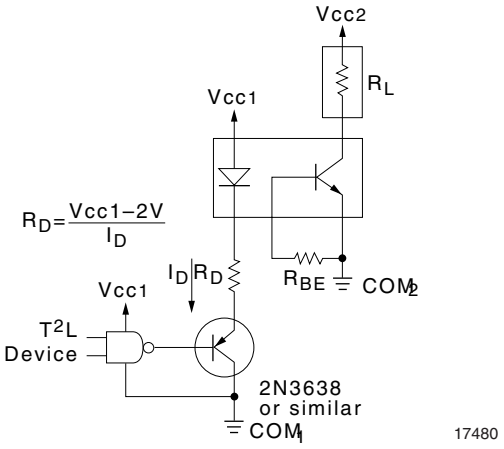


Figure 2.

As drive is increased and R_{BE} reduced, turn-on time and turn-off time both decrease. The total amount of charge stored can also be reduced by decreasing the LED drive pulse duration. Also, as higher drive levels are used, the load resistance, R_L can be reduced to further enhance the speed of the circuit. These parameters are related to each other such that all should be changed together for best results.

One important generalization can be made concerning their interdependence. The LED drive pulse duration, T_{in} output fall time (t_f) output rise time (t_r) and propagation delay (t_p) should occur in a 1.5:1:1:1 ratio, approximately. If this relationship does not occur, the circuit will not operate at as high a repetition rate as it could at the same drive level. T_{out} equals T_{in} at low currents but stretches out at high currents.

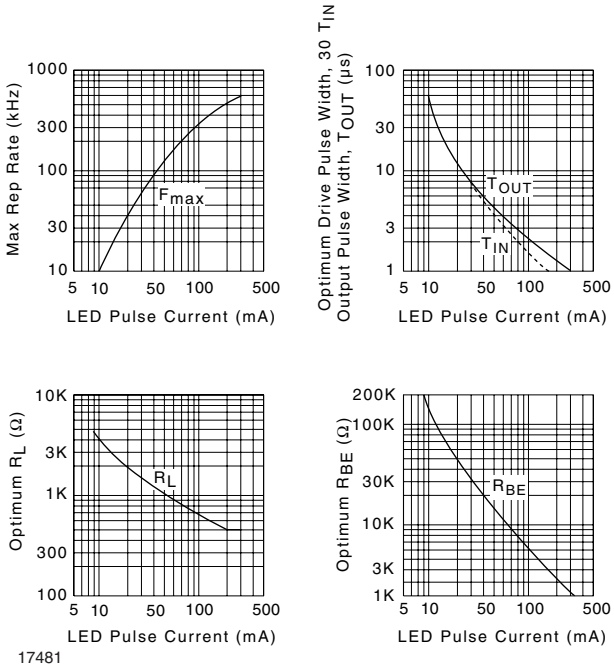


Figure 3. Parameters versus LED pulse current

Figure 3 is a graph relating the important parameters for a typical IL1 whose CTR is 0.25. The optimum values of T_{in}, R_{BE}, and R_L are shown versus LED pulse current as are the resultant output pulse width and maximum full-swing frequency. Rise, fall and propagation time can be read as $^2/_3$ of T_{in}.

Figure 3 shows that increasing drive to 200 mA and using optimum R_{BE} and R_L will increase the maximum repetition rate from 3 kHz to 500 kHz, a 167:1 improvement.

Lower grade optocouplers will behave similarly if the LED drive level is scaled appropriately to allow for a lower CTR.

Another method of increasing speed is to operate the photo-transistor as a photodiode. In this method, bias voltage is supplied between the collector and base terminal, the emitter being unused. Operation to at least 1.0 MHz is possible this way, but the price is the need for external amplification.

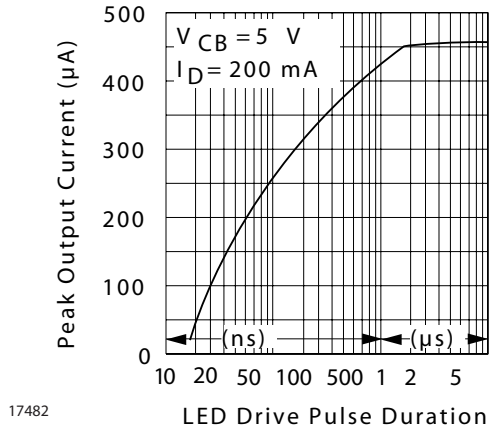


Figure 4. Diode mode output current versus drive pulse duration

Since output current is small, some type of wide bandwidth amplifier must be employed in order to drive T^2L loads.

One simple solution for intermediate speed operation is the use of MOS inverter (1/6 74HC04),

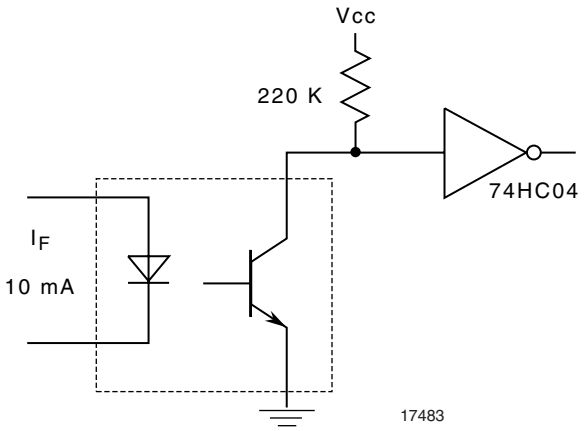


Figure 5.

Another device which will provide a good interface is an integrated comparator amplifier. The phototransistor collector goes to V_{CC}. Its base has a 200 Ω load resistor to ground and goes to one input of the comparator. Also, a resistor goes from this node to the minus supply. This resistor is chosen to supply 50 µA. The other comparator input is grounded. The voltage at the comparator input will switch from –10 mV to + 10 mV or more when the diode turns on and the output will drive the T^2L loads.

Of course discrete component amplifiers could be used and may be best in some applications.

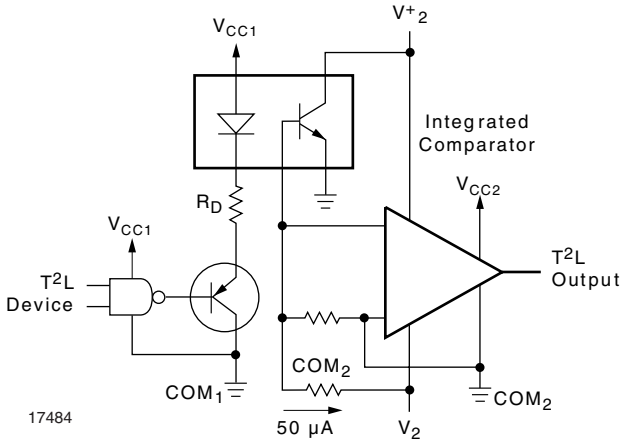


Figure 6.

Conclusion

For operation to 500 kHz, the addition of a base-emitter resistor and a high-current driver is probably the best method of increasing optocoupler speed. Above 500 kHz one must revert to photodiode mode and use an external amplifier to drive most loads, particularly T^2L.

Design Guidelines for Optocoupler Safety Agency Compliance

Introduction to Electrical Safety

Traditionally, electrical isolation from hazardous voltages has been the most common application of optocoupler devices. Other applications for optocouplers include reducing EMI through the elimination of common mode current loops, which are the greatest contributors to radiated emissions in high-speed digital systems. However, isolation is still the predominant role for optocouplers in today's electronics marketplace.

Electrical isolation is important in modern electronics design as a way of minimizing the likelihood of exposing an end-user to injury from hazardous currents. The currents at which harm or even death can occur are far lower than most people think. In certain invasive medical operations, currents as low as 80 µA can be fatal and have an acceptable safety limit of 10 µA. These thresholds are outlined in Figure 1.

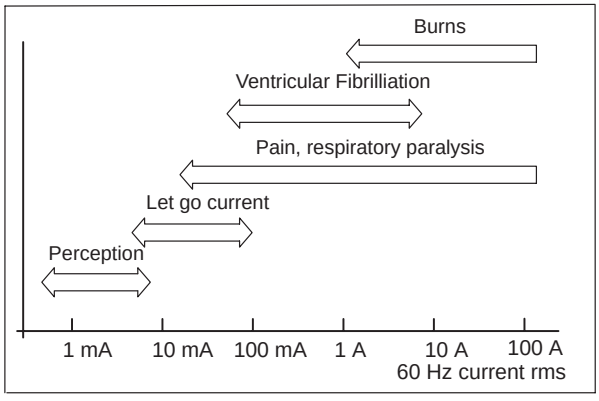


Figure 1. Shock Hazardous Levels

Electrical isolation is typically achieved by one of three methods: magnetic, capacitive, and electro-optical. All three have their pros and cons. Magnetic isolation (using an isolation transformer) is probably the longest-established method of electrical isolation, providing high levels of isolation at high frequencies in a robust package. Among the downsides of this method of isolation are a large device footprint when compared with other methods and suitability only for ac signal coupling. Due to these characteristics, magnetic coupling is for the most part limited to "high-power" ac applications.

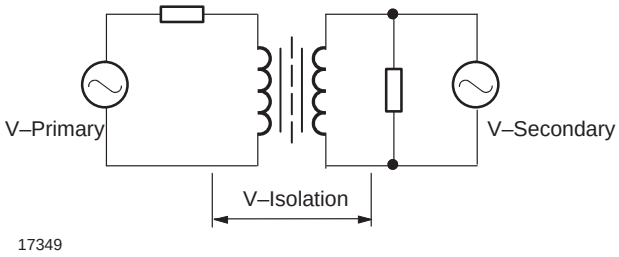


Figure 2. Magnetic Isolation

The second common method of electrical isolation is capacitive coupling. The advantages of capacitive coupling are high switching speeds and a relatively small package footprint, but to eliminate the need for a floating power supply on the secondary side, a large capacitance is required to transfer energy from the primary to the secondary side. Thus, the electrical isolation value of this technique is greatly diminished by the need for efficient energy coupling. Consequently, most capacitive coupling isolation schemes have isolation values in the hundreds of volts rather than the thousands of volts achievable with other methods.

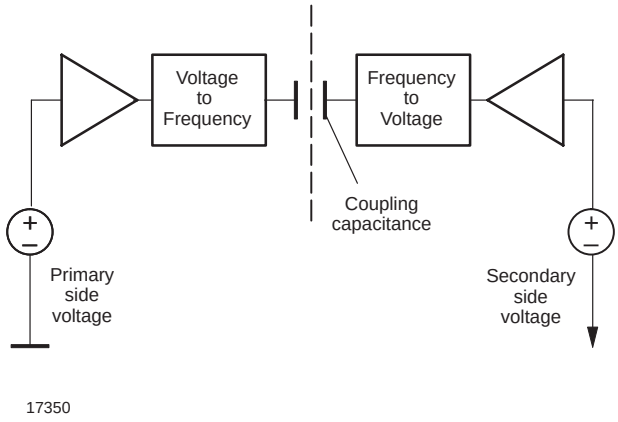


Figure 3. Capacitive Isolation

Another potential isolation method involves the use of magneto resistive sensors. These sensors are able to detect dc as well as ac magnetic fields. However, this is an emerging technology and is susceptible to induced noise from extraneous external magnetic fields.

Optical isolation has many of the best aspects of the former methods without the drawbacks. Mainly, optical isolation offers high electrical isolation values, an effective "line in the sand" barrier that hazardous voltages are incapable of penetrating. In the case of Vishay's couplers, these values are as high as 8000 V the highest level in the industry. This is achieved with low footprint packages and high speed; moreover, it is equally effective with ac or dc signals.

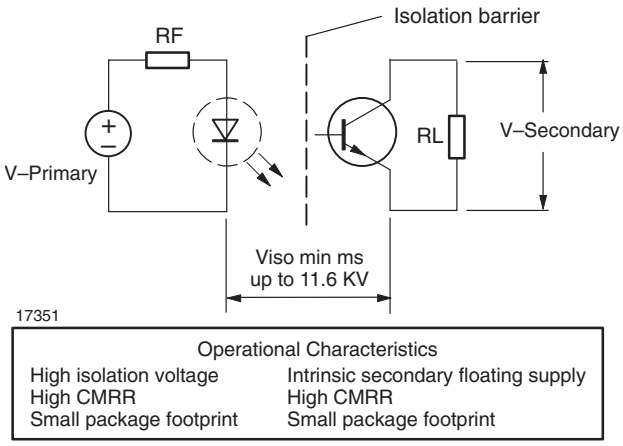


Figure 4. Electro-optical Isolation

Safety Agency Standards Overview

There are several widely accepted industry standards that govern the manufacture and testing of electronic equipment. Probably the most widely known of these in North America is Underwriter's Laboratories (UL). UL has two types of basic approvals: UL Listing and UL Recognition. The difference is simple but often a subject of much confusion. The "UL Recognized" mark, optionally inscribed on the devices themselves, refers to components that have been evaluated to a certain extent by UL and will be "re-reviewed" by UL for proper incorporation into the end-use equipment. A "UL Listed" mark is placed on complete equipment. For example, a computer would be a UL Listed, while the component hard drive would be a UL Recognized part. As seen in the next page, UL was concerned enough about potential confusion between the meanings of these two marks that it intentionally made them distinct from one another.

Figure 5. UL Listed / UL Recognized

UL has safety standards for everything that is or possibly can be manufactured; however, to simplify things, these standards can be divided into two groups: system standards and component standards. The system standards are beyond the scope of this document to address in their entirety. Arguably, the most commonly applicable system standard in the electronics industry is UL60950, which governs the electrical safety requirements for the broad category of information technology equipment (ITE). In addition to information technology, there are also standards that deal with other specialty fields of product electrical safety. Of particular interest to optocoupler design is IEC60601-1, which governs the safety of medical equipment. IEC60601-1 was generated by those in the medical field worldwide, and it is the basis for many countries' national standards, such as UL2601-1 in the United States. Similarly, UL60950 has been based on the internationally generated IEC60950 and adopted with changes due to unique national conditions in the United States, including the National Electrical Code (NEC).

The European Union adopted the IEC-based version as EN60950. As is the case for all components, optocouplers do not necessarily need to meet all particular end-use system standards, such as IEC609050 or IEC60601-1. In trying to meet any of the specific system standards, is important to know which component parameters create design limitations. For safety purposes these parameters include creepage (along a surface) distances, clearance (through air) distances, maximum isolation voltages, and insulation thicknesses. For the most part, this document will deal with standards exclusively dealing with the manufacture and testing of optocouplers. These are covered under two standards, UL1577 and IEC60747-5-1, which incorporate and supersede the earlier DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending. In addition to these standards, which explicitly deal with optocouplers, the latest version IEC60950-1 clauses 2.10.5.1, 2.10.7, 2.10.8 , ANEX P.1, and ANEX P.2

also address issues that deal with optocouplers directly.

UL 1577

The main UL component standard, addressing optocouplers in the United States is UL 1577, which covers the safety specifications that pertain to optocouplers in North America. This document offers an outline of the specification and points out the highlights that deal with electrical safety.

Generally, all tests classified as "type tests" refer to those tests performed to validate a particular design to a standard. They are conducted by qualified testing laboratories, often only once before serial production begins. This is in contrast to routine tests, also known as 100 % production line tests, which are intended to prevent manufacturing defects from ever leaving the factory. In other words, 100 % production line tests are designed to assure that products coming off the line are confirmed to be constructed as those evaluated during the type tests. The first sections of UL1577 deal with package construction issues, materials, cor-rosion protection, spacing, thermal testing, etc.

The section of greatest interest is section 16.2, which specifies "rated dielectric insulation voltage" testing. It specifies a test at the rated dielectric insulation voltage for 60 seconds; however, it gives the manufacturer the option of testing at 120 % of the rated dielectric insulation voltage for only 1 second. For obvious efficiency concerns, the 1-second test is much more desirable. Thus, on a Vishay optocoupler data sheet, a "minimum isolation test voltage" or "isolation voltage for 1 second" is actually 120 % of the rated dielectric insulation voltage. Consequently, the actual rated dielectric insulation voltages are arrived at from Table 1, where they are identified by "System Type" (family of related components).

Opto. Family (System Type)	60 sec test VAC_{RMS}	60 sec test VDC	1 sec VAC_{RMS}	1 sec VDC
A, C, D	1500	2120	1800	2550
B, H, J	4420	6250	5304	7500
E	3748	5300	4498	6360
F	1980	2800	2376	3360
G	3536	5000	4243	6000
S, Y, O	2500	3536	3000	4200
T	3750	5303	4500	6364
I, V	1473	2083	1768	2500
L	1250	1768	1500	2122
U	3125	4419	3750	5303

Table 1: PRODUCTION TESTING CONDITIONS

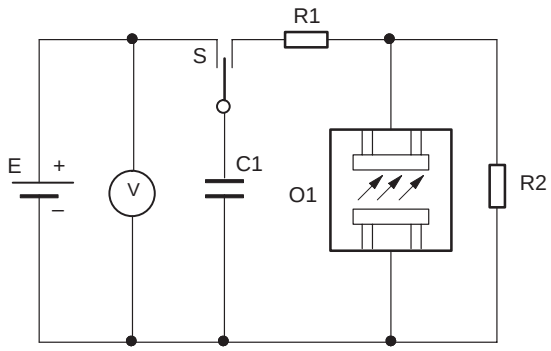
In addition to the general optocoupler standards listed above, there is one additional component classification, that of "double-protection" optical isolators, which is a fairly unique evaluation specific under UL 1577. This is often confused with the more commonly used IEC-based terms of "double insulation" and "reinforced isolation." Both terms, explained in great detail in IEC60950, are briefly defined as follows:

Reinforced insulation: A single, robust level of insulation that meets a high level of constructional and performance requirements at a single point. This can be thought of as a high-integrity component, such as a power transformer with low-voltage outputs or an optocoupler with at least a 0.4-mm minimum insulation thickness to fulfill this requirement. Most of Vishay's optocouplers fulfill this criterion. Those that do will indicate the required 0.4-mm minimum insulation thickness. Vishay's unique over-under double-molded construction inherently provides excellent dielectric insulation characteristics.

Double insulation: An insulation system, equivalent in principle to the above in that it prevents the operator from being exposed to hazardous currents, that consists of the sum of basic insulation and a secondary, independent fault-protection method. Such an insulation system should protect the end-user from any single point of failure of the primary insulation medium. One of the most common methods of providing secondary fault protection is to use a grounded metal chassis, which is designed to trip a fault-protection device should the line fault to the chassis. Another would be to employ a completely independent insulation system such as would be provided by a plastic chassis.

Double protection does not refer to either of the above common IEC defined terms but rather is a performance test, outlined in the UL1577 standard. All of Vishay's system H and J parts have been tested and

conform to the double protection standard. The double protection test basically involves subjecting the part under test to 20-kV pulse discharges and then testing the device using a partial discharge method to verify that no permanent damage has been incurred.The apparatus used to perform the double protection test is described below.



C1	0.0005 σF	O1	Device Under Test	S	Switch
R2	100 MT	R2	100 T	V	DC voltmeter

17352

Figure 6. Circuit Discharge Test

DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending/ IEC60747

The main German standard-writing body, VDE (Verband Deutscher Electrotechniker), has a different approach to optocoupler safety testing and certification than the UL. This approach relies to a much lesser degree on assumptions regarding the viability of insulation thickness.

Rather than assuming that a particular insulation thickness guarantees the electrical dielectric barrier required to maintain a given standard of electrical safety, the VDE method of testing and certification admits the possibility that the insulation could be flawed by voids due to cracks, air bubbles, etc., and compromised over time by voltage transients. This approach allows for a higher degree of confidence in the insulation system, as well as a more flexible approach to meeting a given isolation standard. Using this approach, it is possible to meet an isolation standard with an insulation of lower thickness than would be required by perspective standards that are based strictly on insulation thickness. The consequence of this higher standard of safety confidence is the need for more frequent and accurate testing.

The key to the VDE method of testing is the partial discharge test. As in the case of UL1577, VDE testing methodology includes testing 100 % of the manufactured devices in question to an elevated voltage for 1 second and testing for dielectric breakdown. However, the VDE standard for dielectric failure is extremely tight. It allows for leakage from the "ganged" input to output pins of no greater than 5 pC. Furthermore, this elevated voltage test is done at a lower voltage than the required UL high-pot test, reducing the possibility of component damage during the test. Moreover, in addition to the 100 % partial discharge test on the production line and a type or qualification test during the engineering evaluation phase, VDE requires a destructive sample testing by random sampling tests throughout the manufacturing process. The destructive type and batch sample test is described in Figure 7.

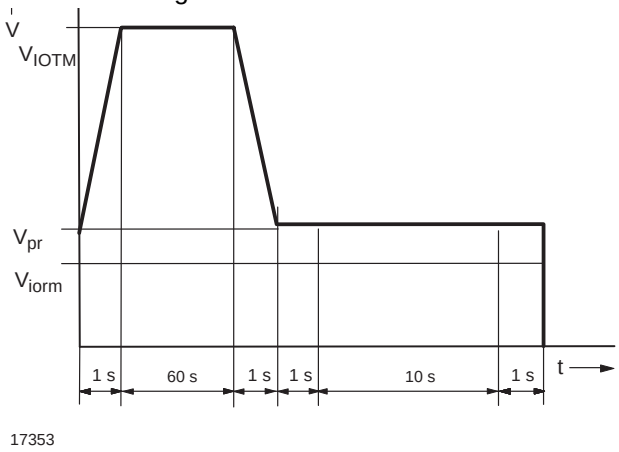


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Figure 7. VDE TYPE and Sampling Destructive Test

V_{IOTM} and V_{IORM} are parameters designated by Vishay and based on the inherent material and construction characteristics of particular parts. These are provided in the Vishay data book for each specific part in question. V_{IOTM} refers to the impulse voltage value of a particular device, and it will be important for determining "usage category," which is described in detail later on in this document. V_{IORM} is the maximum recurring peak voltage, or maximum operation voltage, which is one of the parameters used when determining the maximum continuous operating voltage. V_{PR}, the partial discharge test voltage, is derived from V_{IORM}, being $1.875*V_{IORM}$ for 100% production line testing and 1.5 to $1.2*V_{IORM}$ for various stages of type testing.

In addition to the destructive tests that are performed for type qualification and sample batch testing, VDE requires a partial discharge test to be performed for every single part as a routine test. Moreover, preceding the partial discharge test, Vishay performs an isolation voltage test for 1 second for each and every part coming through production. This test is per-

formed on all Vishay optocoupler parts, whether or not they are required to meet the DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending standard, because it is a test also required for UL 1577. It is described in Figure 8.

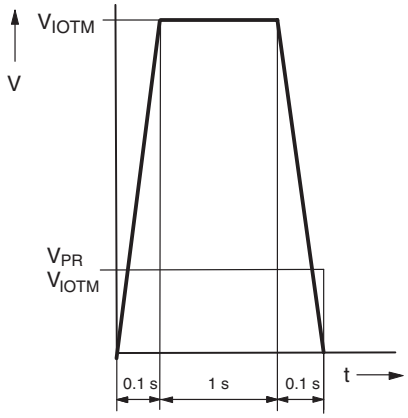

Figure 8. Isolation Voltage Test

For those parts that comply to DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending or IEC 60747, a partial discharge test is conducted subsequent to the isolation test described above. This partial discharge test consists of applying an elevated voltage from the input side to the output side of the optocoupler device under test and measuring the leakage current from primary to secondary. The leakage current allowed is 5 pC. Consequently, this is an excellent test for measuring the insulation integrity of a device, much more so than the use of a prescribed minimum insulation thickness. This test is described in Figure 9.

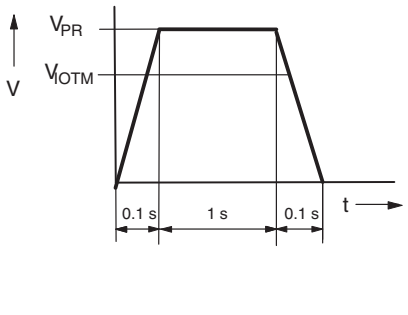

Figure 9. Partial Discharge Test Profile

In addition to the UL and VDE/IEC specs described above, Vishay couplers are also certified by several other regional "competent bodies" such as CSA, which is accredited by the Standards Council of Canada, and notified bodies in the European Union such as BSI and FIMKO. Whether or not a specific part is certified by a specific agency can be determined by looking at the Vishay agency approval table, and if there are any doubts, this may be ascertained by contacting Vishay directly. All of these additional approvals involve the submission of product to various regulatory agencies and notified bodies and do not require any additional production line testing.

INSTALLATION CATEGORY

An additional issue to consider when addressing the electrical safety issues involved with the use of optocouplers is "installation category". Installation category refers to a grouping of equipment based on where the end-user product is located in the power distribution system, and therefore what over voltage transients the circuits would be expected to tolerate. For example, the worst-case installation category IV would be a power meter that is connected directly to the main power feed and does not benefit from the additional transient protection that is enjoyed by systems farther downstream from the main power feed. This would require the highest possible transient withstand voltage, and it would be the highest installation category. The further away equipment is from the main power feed, the lower will be the required transient withstand voltage and installation category. This concept is illustrated below.

In addition to how close to the utility line equipment resides, a second consideration to take into account when determining installation category is utility line voltage.

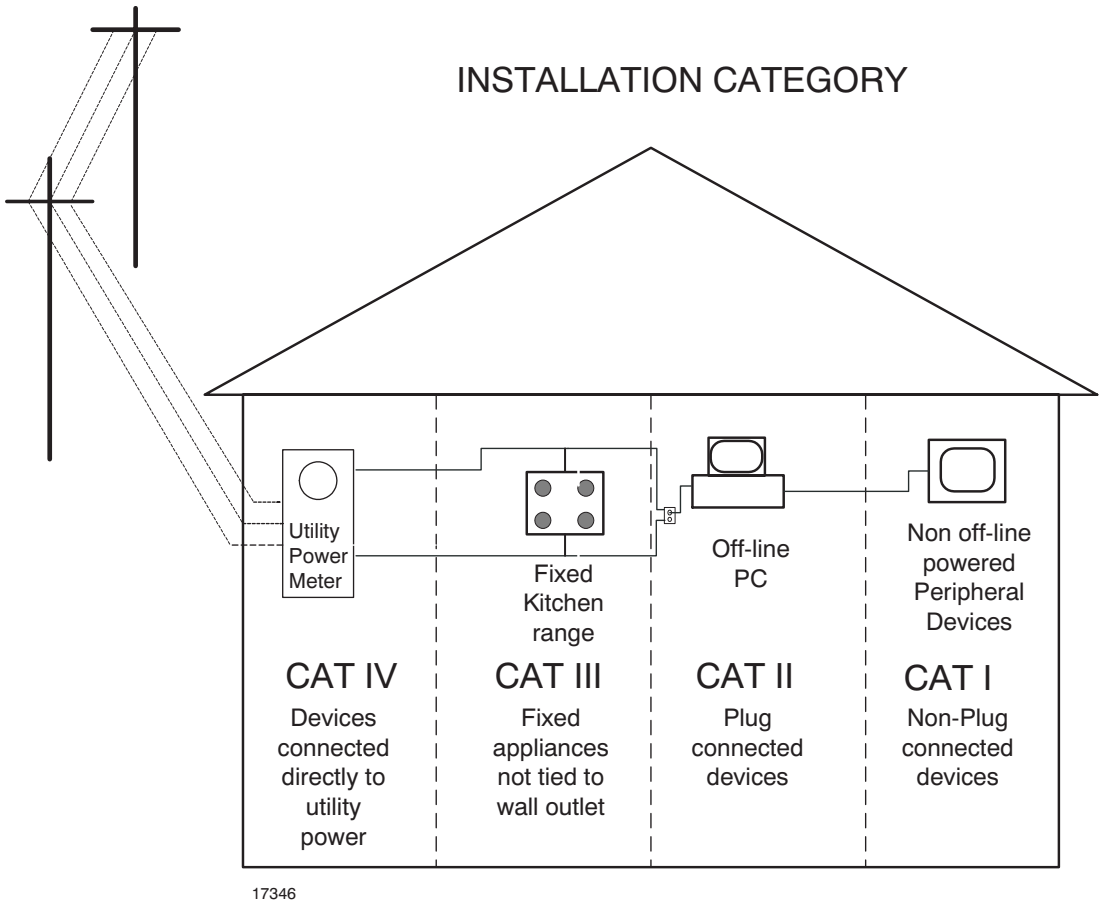

Figure 10. Installation Category

Utility Voltage Phase to earth V_{RMS} or DC	Impulse Withstand Voltages in Volts for Installation Category V_{IOTM} (From VISHAY VDE tables)			
	Installation Category I	Installation Category II	Installation Category III	Installation Category IV
50	330	500	800	1500
100	500	800	1500	2500
150	800	1500	2500	4000
300	1500	2500	4000	6000
600	2500	4000	6000	8000
1000	4000	6000	8000	12000

Table 2: IEC-664 INSTALLATION CATEGORIES

UL60950 for ITE only details spacings with the assumption that the products covered under the standard are category II, so the decision of installation category is essentially made for the manufacturers when they choose to abide by standards such as UL60950.

CREEPAGE AND CLEARANCE

Crucial points of interest when trying to meet any specific system standards are creepage and clearance parameters. Creepage is defined as the shortest distance between two conductors over a material's surface. Clearance is simply the shortest distance between two conductors through air. These two parameters, discussed in great detail in EN60950, and other IEC standards do not apply where insulation is relied upon to isolate circuits, but do apply where there are potential paths "around" the insulation. Both of these parameters are provided in the Vishay product data sheet as they apply to Vishay

optocouplers. They are explained in Figure 11 and 12.

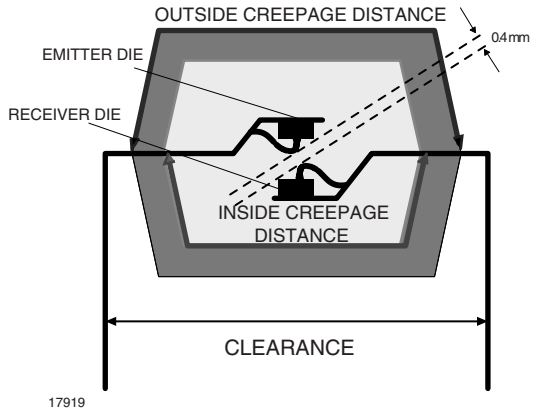

Figure 11. Over - under Double - molded Optocoupler Crossection

In addition to the standard clearance paths, option 6 and option 8 can increase the spacing paths by increasing the lead spread as illustrated in Figure 12.

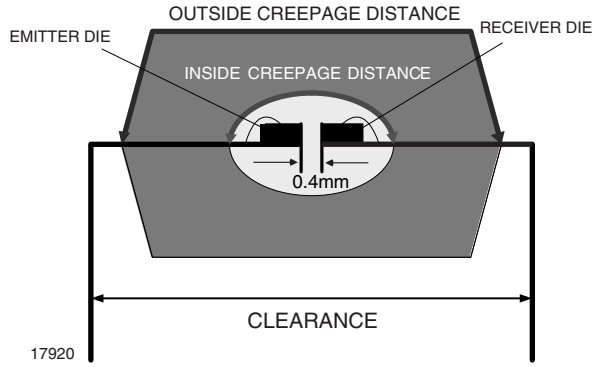

Figure 12. Coplanar Optocoupler Crossection

Designers should note that often it is the pad-to-pad spacing on the circuit boards themselves that is the limiting factor for the allowable spacing requirements. Most printed wiring board manufacturers do not evaluate their boards for Comparative Tracking Index (CTI) ratings, so the worst-case material group IIIb (as defined in IEC-60950) is almost always assumed, with hard-to-control solder-mask not depended upon as a reliable insulating means.

Some manufacturers place 1-mm-wide minimum slots in the board for pollution degree 2 environments to break up the creepage distance requirement and meet only the clearance distance. See Figure 13.

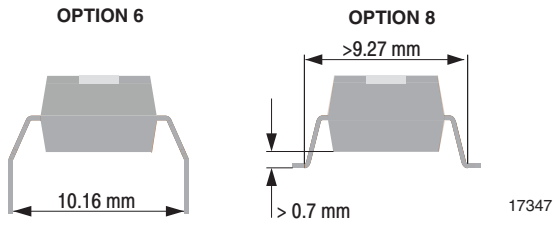

Figure 13. Lead spacings

DESIGN EXAMPLE:

A power supply designer wants to sell an existing ac-to-dc switching power supply, which is agency-approved for the ITE industry under UL60950, to the international (IEC based) industrial control market that normally sits upstream of ITE in the building's branch circuit distribution. That is, the power supply would be used in an installation category III environment instead of II. The product will be used in a 208-V application, Table 2 shows that a 4000-V impulse withstand voltage (or V_{IOTM}) is required. Also, in the supply there is a maximum repetitive peak working voltage of 350-Vpk in the front end of the supply that may appear at the optocoupler, so it should be selected with the minimum repetitive peak working voltage (or V_{IORM}) of 350-V_{pk}. V_{IOTM} and V_{IORM} values are often confused with the isolation test voltage (or dielectric or high-pot rating). The spacings (creepage and clearances) would then need to be checked, with the circuit board's pads usually being the limiting factor. Vishay's spacings are typically shown on the spec sheets.

CONCLUSION

It is important to reemphasize the difference between system-level standards and component-level standards. The procedures and standards discussed in this document refer to component-level standards and must be looked at in that context. If issues arise regarding specific system standards such as IEC-60950, IEC-60601, etc., Vishay applications engineering is able to deal with questions as they may pertain to the optocoupler requirements. Meeting system electrical safety standards is an issue that must be addressed on a final system level, and it cannot be completely addressed by simply choosing the "right" optocoupler.

References:

Webster, G. John, "Medical Instrumentation Application and Design". New York: Wiley, 1998.

Burek, Robert & Linehan, James, "Product Safety for ITE, Telecom, Laboratory, and Test and Measurement Equipment". Compliance Engineering, Foxborough, 1998.

UL 1577 Standard for Safety for Optical Isolators.

IEC 60950 Safety Standard for Information Technology Equipment.

IEC 60747-5-2 Standard for Optoelectronic Devices.

USEFUL WEB Links:

Vishay	http://www.vishay.com
UL	http://www.ul.com/
IEC	http://www.iec.ch/
FIMCO	http://www.sgsfimko.fi/index_en.html
BSI	http://www.bsi-global.com/index.xalter
CSA	http://www.csa-international.org/default.asp?language=english
VDE	http://www.vde.com/VDE/de/

How to Use Optocoupler Normalized Curves (Appnote 45)

An optocoupler provides insulation safety, electrical noise isolation, and signal transfer between its input and output. The insulation and noise rejection characteristics of the optocoupler are provided by the mechanical package design and insulating materials.

A phototransistor optocoupler provides signal transfer between an isolated input and output via an infrared LED and a silicon NPN phototransistor.

When current is forced through the LED diode, infrared light is generated that irradiates the photosensitive base-collector junction of the phototransistor. The base-collector junction converts the optical energy into a photocurrent which is amplified by the current gain (HFE) of the transistor.

The gain of the optocoupler is expressed as a Current Transfer Ratio (CTR), which is the ratio of the phototransistor collector current to the LED forward current. The current gain (HFE) of the transistor is dependent upon the voltage between its collector and emitter. Two separate CTRs are often needed to complete the interface design. The first CTR, the non-saturated or linear operation of the transistor, is the most common specification of a phototransistor optocoupler and has a V_{ce} of 10 V. The second is the saturated or switching CTR of the coupler with a Vce of 0.4 V. Figures 1 and 2 illustrate the Normalized CTR_{CE} for the linear and switching operation of the phototransistor. Figure 1 shows the Normalized Non-Saturated CTR_{CE} operation of the coupler as a function of LED current and ambient temperature when the transistor is operated in the linear mode. Normalized $CTR_{CE(SAT)}$ is illustrated in Figure 2. The saturated gain is lower with LED drive greater than 10 mA.

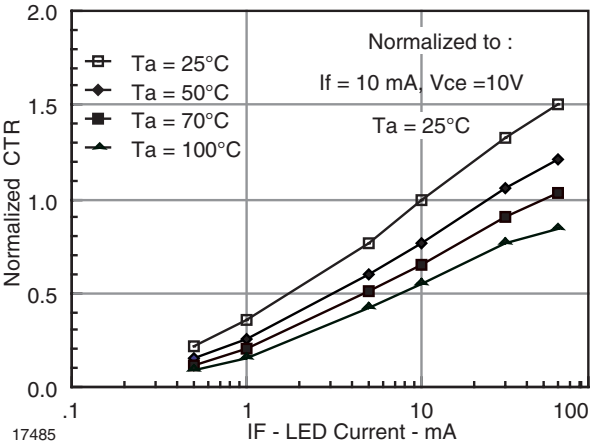

Figure 1. Normalized CTR versus I_F and T_{amb}

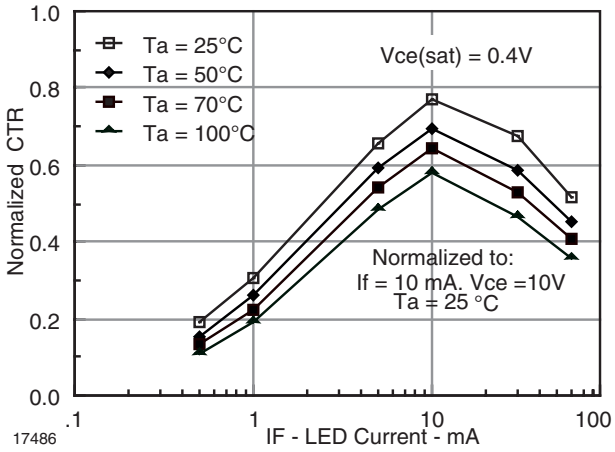

Figure 2. Normalized saturated CTR

The following design example illustrates how normalized curves can be used to calculate the appropriate load resistors.

Problem 1.

Using an IL1 optocoupler in a common emitter amplifier (Figure 3) determine the worst case load resistor under the following operation conditions:

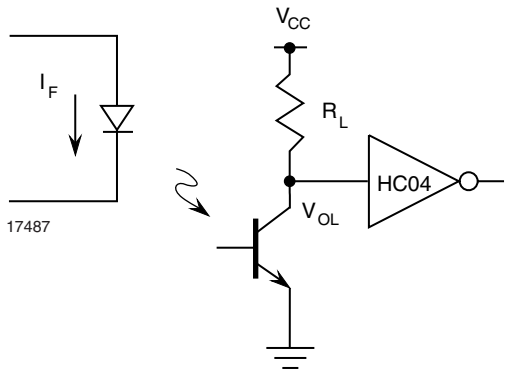

Figure 3. IL1 to 74HC04 interface

T_{amb} = 70 °C, I_F = 2 mA, V_{OL} = 0.4 V,
Logic load = 74 HC04

IL1 Characteristics:

$CTR_{CE(NON\ SAT)}$ = 20 % Min. at T_{amb} = 25 °C,
I_F = 10 mA, V_{CE} =1 0 V

Solution

Step 1. Determine $CTR_{CE(SAT)}$ using the normalization factor ($NF_{CE(SAT)}$) found in Figure 2.

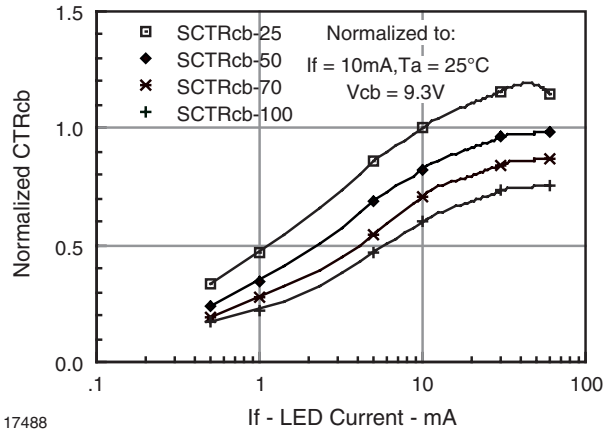

Figure 4. Normalized saturated CTR

$$CTR_{CE(SAT)} = CTR_{CE(NON\ SAT)}\ NF_{CE(SAT)} \quad (1)$$

$CTR_{CE(SAT)}$ = 20 % * 0.36

$CTR_{CE(SAT)}$ = 7.2 %

Step 2. Select the minimum load resistor using the following equation:

$$R_{L(MIN)} = \frac{V_{CC} - V_{OL}}{\frac{CTR_{CE(SAT)} I_F}{100\%} - I_L} \quad (2)$$

$$R_{L(MIN)} = \frac{5V - 0{,}4V}{\frac{(0{,}072)2mA}{100\%} - 50\mu A}$$

$R_{L(MIN)}$ = 48.94 KΩ, select 51 KΩ ± 5 %

The switching speed of the optocoupler can be greatly improved through the use of a resistor between the base and emitter of the output transistor. This is shown in Figure 5. This resistor assists in discharging the charge stored in the base to emitter and collector to base junction capacitances. When such a speed-up technique is used the selection of the collector load resistor and the base-emitter resistor requires the determination of the photocurrent and the HFE of the optocoupler.

The photocurrent generated by the LED is described by the CTR_{CB} of the coupler. This relationship is shown in Equations 3 and 4. Equation 5 shows that CTR_{CE} is the product of the CTR_{CB} and the HFE. The HFE of the transistor is easily determined by evaluating Equation 4, once the $CTR_{CE(SAT)}$ and CTR_{CB} are known. The Normalized CTR_{CB} is shown in Figure 6. Equations 5, 6, and 7 describe the solution for determining the R_{BE} that will permit reliable operation.

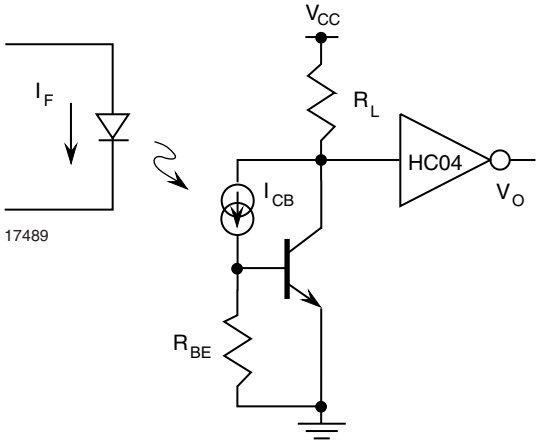

Figure 5. Optocoupler/logic interface with R_{BE} resistor

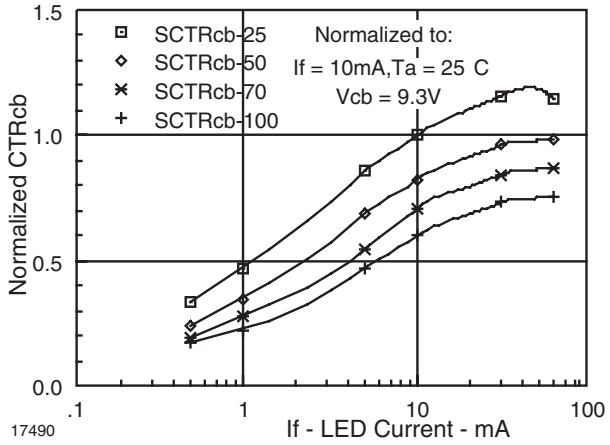

Figure 6. Normalized CTR_{CB} versus LED current

$$CT_{CB} = \frac{I_{CB}}{I_F}100\% \quad (3)$$

$$I_{CB} = I_F\frac{CTR_{CB}}{100\%} \quad (4)$$

$$CTR_{CE(SAT)} = CTR_{CB}\,HFE_{(SAT)} \quad (5)$$

$$HFE_{(SAT)} = \frac{CTR_{CE(SAT)}}{CTR_{CB}} \quad (6)$$

$$R_{BE} = \frac{V_{be}}{I_{CB} - I_{BE}} \quad (7)$$

$$R_{BE} = \frac{V_{BE}HFE_{(SAT)}R_L}{I_{CB}HFE_{(SAT)}R_L - [V_{CC} - V_{CE(SAT)}]} \quad (8)$$

$$R_{BE} = \frac{V_{BE}\dfrac{CTR_{CE}NF_{CE(SAT)}}{CTR_{CB}NF_{CB}}R_L}{\dfrac{I_F CTR_{CE}NF_{CE(SAT)}R_L}{100\%} - [V_{CC} - V_{CE(SAT)}]} \quad (9)$$

Problem 2.

Using an IL2 optocoupler in the circuit shown in Figure 6, determine the value of the collector load and base-emitter resistor, given the following operational conditions:

T_{amb} = 70 °C, I_F = 5 mA, V_{OL} = 0.4 V,
Logic load = 74HC04

IL2 Characteristics:

CTR_{CE} = 100 % at T_{amb} = 25 °C, V_{CE} = 10 V, I_F = 10 mA

CTR_{CB} = 0.24 % at T_{amb} = 25 °C, V_{CB} = 9.3 V, I_F = 10 mA

Solution

Step 1. Determine $CTR_{CE(SAT)}$, and CTR_{CB}.

From Figure 2 the $CTR_{CE(SAT)}$ = 55 %, [$NF_{CE(SAT)}$ = 0.55]

From Figure 6 the CTR_{CB} = 0.132 %, [NF_{CB} = 0.55]

Step 2. Determine R_L.

From Equation 2 R_L = 1.7 KΩ

Select R_L = 3.3 KΩ

Step 3. Determine R_{BE}, using Equation 9.

$$R_{BE} = \frac{0{,}65V\dfrac{(100\%)(0{,}55)}{(0.24\%)(0{,}55)}3{,}3K\Omega}{\dfrac{(5mA)(100\%)(0{,}55)(3{,}3K\Omega)}{100\%} - [5V - 0{,}4V]} \quad (10)$$

R_{BE} = 199 KΩ, select 220 KΩ

Using a 3.3 kΩ collector and a 220 KΩ base-emitter resistor greatly minimize the turn-off propagation delay time and pulse distortion. The following table illustrates the effect the R_{BE} has on the circuit performance.

	I_F = 5 mA, V_{CC} = 5 V	
	R_L = 3.3 KΩ R_{BE} = ∞ Ω	R_L = 3.3 KΩ R_{BE} = 220
t_{delay}	1 µs	2 µs
t_{rise}	4 µs	5 µs
$t_{storage}$	17 µs	10 µs
t_{fall}	5 µs	12 µs
t_{phl}	3.5 µs	7 µs
t_{plh}	22 µs	12 µs
Pulse Distortion 50 µs	37 %	10 %

Not only does this circuit offer less pulse distortion, but it also improves high temperature switching and lower static DC power dissipation and improved common mode transient rejection.

Optocouplers in Switching Power Supplies

The following provide information on how to use optocouplers in designs to protect against electric shock.

Safety standards for optocouplers are intended to prevent injury or damage due to electric shock Two levels of electrical interface are normally used:

- Reinforced, or safe insulation is required in an optocoupler interface between a hazardous voltage circuit (like an ac line) and a touchable **S**afety **E**xtra **L**ow **V**oltage (SELV) circuit.
- Basic insulation is required in an optocoupler interface between a hazardous voltage circuit and a non-touchable **E**xtra **L**ow **V**oltage (ELV) circuit.

The most widely used insulation for optocouplers in switch-mode power supply is reinforced insulation (class II). The following information enables the designer to understand the safety aspects, the basic concept of the DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending and the design requirements for applications.

Facts and Information*)

Optocouplers for line-voltage separation must have several national standards. The most accepted standards are:

- UL for America
- UL/ CSA for Canada
- CQC for China
- BSI for Great Britain
- FIMKO, SEMKO, NEMKO, DEMKO for Nordic countries (Europe)
- VDE for Germany

Today, most manufacturers operate on a global scale. Therefore, it is important to understand and meet those requirements.

The DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending is a major safety standard in the world.

The DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending standard and IEC 60047C/199/CD standards may become part of IEC 60747-5.

If design engineers work with VISHAY optocouplers**,** they will find some terms and definitions in the data sheets which relate to DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending.

Rated isolation voltages:

V_{ISO} is the voltage between the input terminals and the output terminals.

Note: All voltages are peak voltages!

- V_{IOWM} is a maximum rms. voltage value of the optocouplers assigned by VISHAY. This characterizes the long term withstand capability of its insulation.
- V_{IORM} is a maximum recurring peak (repetitive) voltage value of the optocoupler assigned by VISHAY. This characterizes the long-term withstand capability against recurring peak voltages.
- V_{IOTM} is an impulse voltage value of the optocoupler assigned by VISHAY. This characterizes the long-term withstand capability against transient over voltages.

Isolation test voltage for routine tests is at factor 1.875 higher than the specified V_{IOWM}/ $V_{IORM\ (peak)}$.

A partial discharge test is a different test method to the normal isolation voltage test. This method is more sensitive and will not damage the isolation behavior of the optocoupler like other test methods probably do. The DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending therefore does not require a minimum thickness through insulation. The philosophy is that a mechanical distance only does not give you an indica tion of the safety reliability of the coupler. It is recommended that construction together with the assembling performance. The **partial discharge test method** can monitor this more reliably.

The following tests must be done to guarantee this safety requirement.

100 % test (piece by piece) for one second at a voltage level of specified V_{IOWM}/V_{IORM} (peak) multiplied by 1.875*) test criteria is partial discharge less than 5 pico coulomb.

A lotwise test at V_{IOTM} for 10 seconds and at a voltage level of specified V_{IOWM}/ V_{IORM} (peak) multiplied by 1.5 for 1 minute*) test criteria is partial discharge less than 5 pico coulomb.

Design example:

The line ac voltage is 380 V_{RMS}. Your application class is III (DIN/VDE 0110 Part 1/1.89). According to table 1, you must calculate with a maximum line voltage of 600 V and a transient over voltage of 6000 V.

*)See Safety Agency Applications Note for more information.

V_{IOWM}/V_{IORM} up to	Appl. Class I	Appl. Class II	Appl. Class III	Appl. Class IV
50 V	350 V	500 V	800 V	1500 V
100 V	500.V	800 V	1500 V	2500 V
150 V	800 V	1500 V	2500 V	4000 V
300 V	1500 V	2500 V	4000 V	6000 V
600 V	2500 V	4000 V	6000 V	8000 V
1000 V	4000 V	6000 V	8000 V	12000 V

Table 1: Reccomended transient overvoltages related to ac/dc line voltage (peak values)

Now select the TCDT1100 from our VISHAY coupler program. The next voltage step of 380 V is 600 V (V_{IOWM}).The test voltages are 1600 V for the TCDT1100 for the routine test and 6000 V/ 1300 V for the sample test.

The DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending together with the isolation test voltages also require very high isolation resistance, tested at an ambient temperature of 100 °C.

Apart from these tests for the running production, the VDE Testing and Approvals Institute also investigates the total construction of the optocoupler.

The DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending requires life tests in a very special sequence; 5 lots for 5 different subgroups are tested.

The sequence for the main group is as follows:

- Cycle test
- Vibration
- Shock
- Dry heat
- Accelerated damp heat
- Low temperature storage (normally – 55 °C)
- Damp heat steady state
- Final measurements.

Finally there is another chapter concerning the safety ratings. This is described in DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending.

The maximum safety ratings are the electrical, thermal and mechanical conditions that exceed the absolute maximum ratings for normal operations. The philosophy is that optocouplers must withstand a certain exceeding of the input current, output power dissipation, and temperature for at least 72 hours. This is a simulated space of time where failures may occur.

It is the designer's task to create his design inside of the maximum safety ratings.

Optocouplers – approved to the DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending – must consequently pass all tests undertaken. This enables you to go ahead and start your design.

Layout Design Rules

The previous chapter described the important safety requirements for the optocoupler itself; but the knowledge of the creepage distance and clearance path is also important for the design engineer if the coupler is to be mounted onto the circuit board. Although several different creepage distances refer to different safety standards, e.g. IEC 60065 for TV or the IEC 60950 for office equipment, computer, data equipment etc. there is one distance which dominates switching power supplies: This is the 8 mm spacing requirement between the two circuits: The hazardous input voltage (ac 240 power-line voltage) and the safety low voltage.

This 8 mm spacing is related to the 250 V power line and defines the shortest distance between the conductive parts (either from the input to the output leads) along the case of the optocoupler, or across the surface of the print board between the solder eyes of the optocoupler input/ output leads, as shown in figure 1. The normal distance input to output leads of an optocoupler is 0.3". This is too tight for the 8 mm requirement. The designer now has two options: He can provide a slit in the board, but then the airgap is still low or .

Depending on the product, option 1 or the "G" version can be used e.g. SFH619-X001 or TCDT1100G.

"G" stands for a wide-spaced lead form of 0.4" and meets the 8 mm spacing.

The spacing requirements of the 8 mm must also be taken into consideration for the layout of the board.

Figures 2 and 3 provide examples for your layout.

The creepage distance is also related to the resis ance of the tracking creepage current stability. The plastic material of the optocoupler itself and the mate-

rial of the board must provide a specified creepage-current resistance.

The behavior of this resistance is tested with special test methods described in the IEC 112. The term is CTI (**C**omparative **T**racking **I**ndex).

The DIN EN 60747-5-2(VDE0884)/ DIN EN 60747-5-5 pending requires a minimum of a CTI of 175.

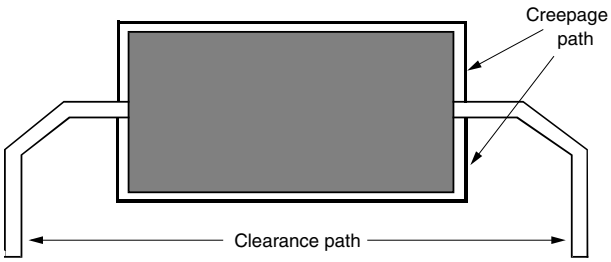

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Figure 1. Isolation creepage/clearance path along the body

(The creepage path is the shortest distance between conductive parts along the surface of the isolation material.

The clearance path is the shortest distance between conductive parts.)

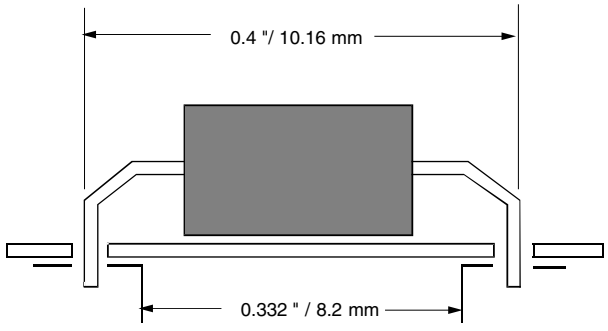

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Figure 2. Isolation creepage/clearance path after mounting on a board (side view)

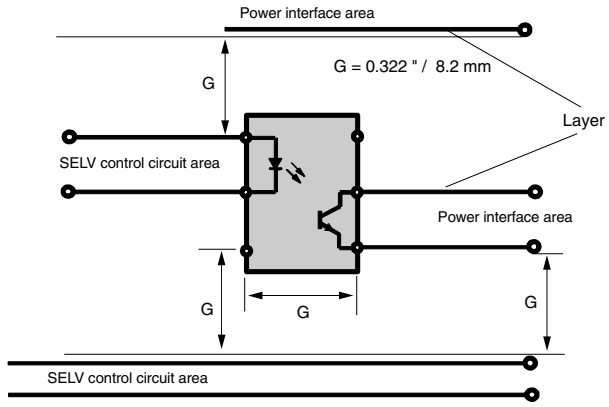

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Figure 3. "Top view of optocoupler mounting on a board" (clearance on PC board: 0.322 / 8.2 mm, creepage path on PC board is 0.322 / 8.2 mm)

Not only the solder eyes of the coupler itself on the board must have the 8 mm distance, but also all layers located between the SELV areas and the power interface areas.

Optocouplers for Safe Electrical Isolation to DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending (Appnote 48)

Because of their high reliability and long life, optocouplers are used in applications requiring safe electrical isolation of two circuits, such as in switched-mode power supplies (SMPS). Optocouplers have to comply with the relevant VDE standards and/or international standards like IEC when used for protecting systems against electrical damage.

Currently the tendency is to incorporate international standards (e.g. IEC) into the German VDE regulations. On the other hand, the goal is to make a national VDE standard (such as one that has proved to increase safety) into an internationally recognized IEC standard. For example, a new VDE standard, DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending, has just been introduced in Germany and also is being reviewed in various international standardization committees.

German VDE standards are divided into three main groups:

- Basic VDE standards, such as VDE 0110 which describes air and creepage path requirements in general
- VDE standards governing components, such as the recently expired VDE 0883 standard for optocouplers
- VDE standards governing systems and equipment, such as VDE 0805/0806 for office machines and EDP systems

Optocouplers used in a switched mode power supply of a computer have to satisfy the requirements of VDE 0883 and VDE 0805/0806.

Thickness of solid insulation between conducting parts, the isolation test voltage and the air and creepage paths are crucial in applications requiring reliable electrical isolation. Depending on the sensitivity of the application, different values are given in the VDE standards.

For example, an electrical control cabinet will probably be opened and operated infrequently and only by skilled staff. However, it's not unusual for a cup of coffee to be spilled accidentally over the keyboard of an electric typewriter. Thus the requirements to be met in the two cases are very different.

The latest findings in high-voltage technology have questioned two parameters thickness of solid insulation and isolation test voltage. Dielectric strength does increase with the thickness of the insulating material, but only when the insulating material is homogeneous and free of impurities or air-pockets. A high-quality thin insulation can be better than a thick layer with impurities or air-bubbles. The trend is clearly towards reducing insulation thickness (about 0.3 to 0.5 mm) for more economical manufacturing and technologically advanced optocoupler functions.

To test the breakdown strength, isolation test voltage normally lasts 60 seconds in qualification tests and up to one second in 100 % inspection (depending on the particular VDE standard). However, no determination is made whether any partial discharge occurs in the insulation material during testing. This requires measurement equipment of extreme sensitivity and has been introduced on the market only recently.

Studies in high-voltage technology have shown that a single partial discharge will probably not be extinguished at low voltages and that permanent partial discharge may degrade and damage the insulating material. So that even under normal operating conditions partial discharge may occur when operating voltage is applied. A high-voltage breakdown is likely to occur after a certain time of operation.

The new standard for optocouplers, DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending, used for safe electrical isolation addresses the two drawbacks mentioned earlier. Suitable dielectric strength is now determined by the presence of partial discharges at a defined test voltage. Partial discharges occur with impurities or air-bubbles in the insulating material or insufficient thickness of solid insulation.

The conventional breakdown test (isolation test voltage) may risk causing initial damage to the optocoupler which is not detectable. This test has been replaced in DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending by the partial discharge test which detects any partial discharge. The absence of partial discharge during the test reliably proves the isolation capability without any undesirable initial damage to the insulation material.

Partial discharge measurement method per VDE 0884

Two measurement methods, as described in DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending, have proved to be reliable and suitable for optocouplers.

- Measurement method A—a destructive test to qualify optocouplers and for sample testing in manufacture.
- Measurement method B—a non-destructive test of every component (100 % inspection).
- Figures 1 and 2 show two typical voltage time curves (AC voltage peak-to-peak values) for Vishay optocoupler testing per DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending.

A destructive test for the qualification of optocouplers and sample testing in manufacture. This time-test voltage diagram can be used with SFH601 and CNY17 couplers.

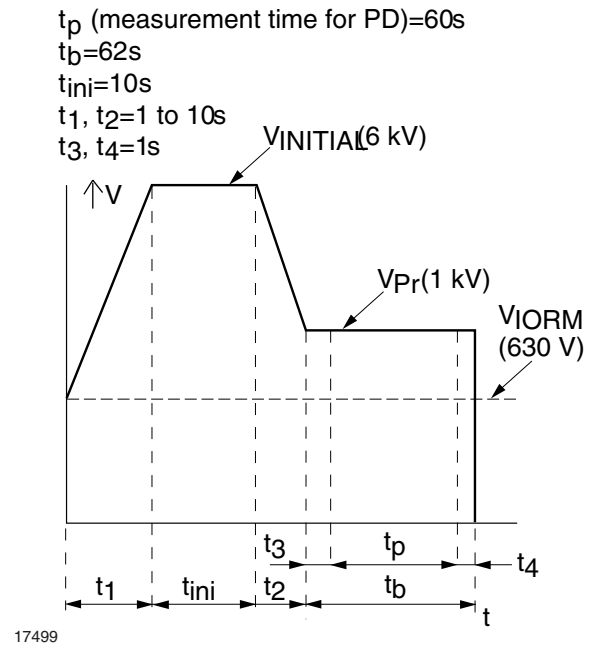


Figure 1. Measurement method A of DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending

A non-destructive test of every component (100 % inspection).

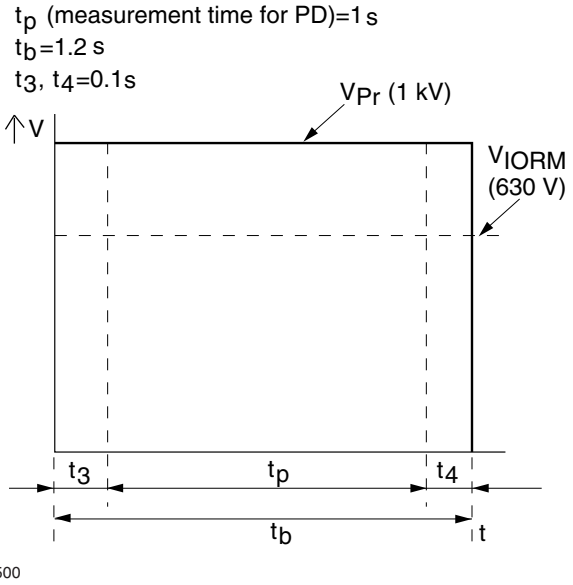


Figure 2. Measurement method B

More DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending test criteria for safe electrical isolation by optocouplers

In addition to the partial discharge test, DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending has further requirements to improve optocoupler reliability. For example, data on reliability limits such as limit current, temperature, and/or power dissipation must be given for every approved and qualified component. Figure 3 shows the reliability limit values for SFH601 and CNY17 optocouplers.

Limit values are generally higher than the maximum ratings. They indicate whether and if additional components are required in the circuit to ensure safe electrical isolation in case of failure in the surrounding circuitry.

In the qualification test (destructive test) the optocoupler is exposed to numerous tests in rough environments such as humidity cycles or temperature shocks. The optocouplers are then stressed to the limit values for 72 hours. Finally, they are tested partial discharge. Absence of partial discharge (PD) currently means a value below 5 picocoulombs.

Importance of DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending standard for the future

Optocouplers used in applications for safe electrical isolation are tested for freedom from partial discharge to give improved reliability and useful information on the long term stability of insulating materials. DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending is only a first step in this direction. Partial discharge measurements probably will become applicable to transformers, capacitors, and other components. VDE 0883 is no longer the standard since December 1988. However, until the end of 1991 approvals to VDE 0883 were accepted in the marketplace.

From 1992 optocouplers must have DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending approval. New designs of PC boards or systems using optocouplers which have to fulfil the requirements of safe electrical isolation, must use only optocouplers with DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending approval.

Vishay already offers the SFH601 and CNY17 optocouplers with DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending approval under option 1. Other types, especially DIP-4 series, have been approved and are available.

For every optocoupler type approved to DIN EN 60747-5-2 (VDE0884)/ DIN EN 60747-5-5 pending, reliability limit values such as limit temperature, current and power dissipation must be given.

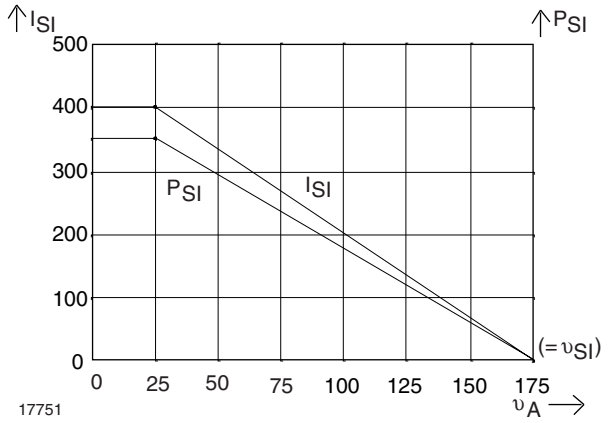


Figure 3. Dependency of reliability maximum ratings on ambient temperature for SFH601, CNY174

Application Examples

Introduction

Optocouplers are used to isolate signals for protection and safety between a safe and a potentially hazardous or electrically noisy environment. The interfacing of the optocoupler between digital or analogue signals need to be designed correctly for proper protection. The following examples help in this area by using DC and AC input phototransistor optocouplers.

Optocouplers in IC Logic Design

To interface with TTL logic circuits, Vishay offers a wide range of 4 pin and 6 pin optocoupler series such as the CNY17x, SFH61xA, TCET110x, or K817P family.

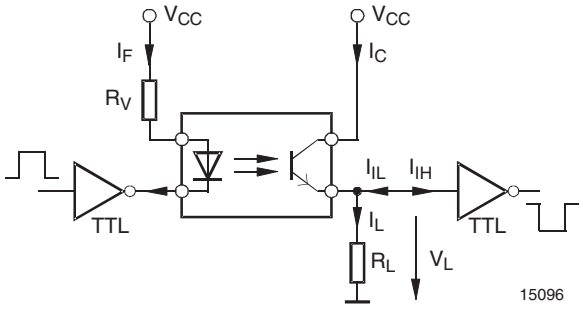
a) Supply voltage: V_{CC} = 5 V

b) Operation temperature range: – 20 °C to + 60 °C

c) Service life of application: 10 years

Example 1

Phototransistor wired to emitter resistor.



For simplicity, a typical CTR value of 100 % at I_F = 10 mA is selected. Within the temperature range of – 20 °C to + 60 °C the CTR undergoes change between + 12 % and – 17 %. The – 17 % reduction is critical as applied to functioning of the circuit.

Assuming a 10-year service life period of the interface circuit, allowance needs to be made for additional CTR reduction of approximately 20 % on account of degradation. Making an additional tolerance allowance of approximately – 25 % for the CTR will result in a safe minimum value of approximately 50 %.

CTR_{min} = 100 % x **(0.83)** x **(0.80)** x **(0.75) = 49.8 %**

For a defined low state at the output of the optocoupler the voltage V_L at R_L must be $V_{IL} \leq 0.8$ V and current I_{IL} (I_{ILmax} = 1.6 mA) must be capable of flowing through R_L from the TTL input.

Owing to the phototransistor in this case being blocked at the output of the optocoupler and I_{CEO} maximum 200 nA (at approximately 60 °C), $I_L - I_{IL}$ setting can proceed practically without any error.

This results in the following maximum value of R_L:

$$R_L < \frac{V_{IL}}{I_{IL}} = \frac{0{,}8\,V}{1.6\ \text{mA}} = 500\Omega$$

A voltage V_L at R_L resistor of $V_{IH} \geq 2$ V is necessary in order to attain a safe high state at the output. This needs to be generated by the collector current I_C of the phototransistor.

In the case of the TTL output at the input of the optocoupler the current should remain $I_{OL} \leq 16$ mA. The CTR value of 50 % results in maximum output current I_C for the optocoupler of 8 mA.

With $I_L = I_C + I_{IH}$ and I_{IH} for standard TTL being maximum 40 µA, $I_L = I_C$ can be assumed without any essential error.

This allows the minimum value to be determined for R_L.

$$R_L > \frac{V_{IH}}{I_L} = \frac{2\,V}{8\,mA} = 250\Omega$$

If for example R_L = 390 Ω is selected and 20 % safety is computed to the minimum V_{IH} in respect of the high state (V_{IH} + V_{IH} x 20 % = 2.4 V), this will then permit

I_C, I_F and the dropping resistor R_V at the input of the optocoupler to be determined,

$$I_C = I_L > \frac{2{,}4\,V}{390\Omega} = 6.15\ \text{mA}$$

$$-> I_F > \frac{6.15\,mA}{CTR} = 12.3\,mA$$

With V_F = 1.2 V, (the forward voltage of the IR diode) and $V_{OL} \leq 0.4$ V for the TTL output follows

$$R_V > \frac{V_{CC} - V_F - V_{OL}}{12.3\text{mA}} = 276\Omega,\ R_V = 270\Omega$$

The TTL interface with the optocoupler is able to transmit signals having a frequency of > 50 kHz or a transmission rate of ≥ 100 kbit/s.

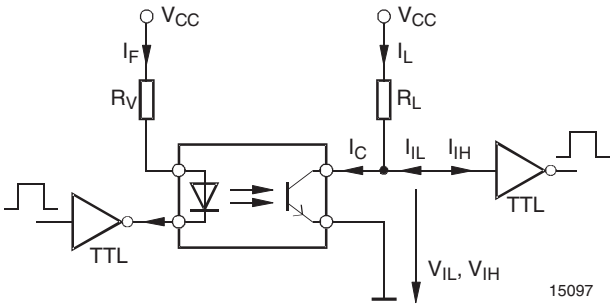
In the same way, the optocoupler can interface with other logic circuits, e.g., LSTTL or HCMOS, HCTMOS components. All that needs to be done is to work the corresponding limit values V_{IH}, V_{OH}, I_{IL}, I_{OL}, etc., into the computation for the relevant

family.

If use is made of LSTTL or HCTMOS components this will also bring about an essential reduction in current consumption.

Example 2:

Phototransistor wired to collector resistor



The CTR is determined applying the same calculation – 50% – as that given in example 1. In this example dimensioning of the interface is launched from the high state at the output of the optocoupler.

In the high state a non–operate current of the I_{IH} – of maximum 40 µA – may flow in the TTL input. If R_L selection is too high, the entire non–operate current = $I_{CEO} + I_{IH}$ may produce such a voltage drop through the R_L that the critical V_{IH} voltage (minimum = 2 V), is not attained.

$$R_L < \frac{V_{CC} - V_{IH}}{I_{CEO} + I_{IH}} = \frac{5\,V - 2\,V}{40{,}2\mu A} = 74{,}6\,k\Omega$$

or if another + 20% safety is added to the V_{IH} voltage,

$$R_L < \frac{V_{CC} - (V_{IH} + V_{IH} \times 20/100)}{I_{CEO} + I_{IH}} = \frac{5\,V - 2{,}4\,V}{40{,}2\mu A} = 64{,}7\,k\Omega$$

For calculating the smallest usable R_L–value I_{Cmax} = 8 mA is assumed as in example 1 and use is made of the low state of the optocoupler output. In this circuit the current I_{IL} of the TTL input flows through the phototransistor in such a way that the following applies: $I_C = I_L + I_{IL}$.

This results in the following:

$$R_L > \frac{V_{CC} - V_{IL}}{I_{Cmax} - I_{IL}} = \frac{5\,V - 0{,}8\,V}{6{,}4\,mA} = 656\Omega$$

To select the value for RL the following should be observed.

Proceeding from the voltage V_{IL} = 0.8 V the phototransistor is on the limits of saturation.

Owing to the voltage V_{CE} being relatively unstable in this state, V_{CE} should be selected in such a way that the phototransistor is in full saturation.

From the diagram V_{CEsat} vs. I_C in any given 4 pin or 6 pin phototransistor data sheet, CTR reduced by 50% and for I_C < 5 mA follows V_{CEsat} < 0.5 V.

I_{Cmax} is now reduced to approximately 4 mA and for the minimum R_L follows,

$$R_L > \frac{V_{CC} - V_{CEsat}}{4mA - 1.6\text{mA}} = \frac{5V - 0{,}5V}{2{,}4mA} = 1875\Omega$$

If a suitable value is selected for the resistor R_L it is possible to determine R_V at the input.
Example for R_L = 5.1 kΩ follows

$$I_L = \frac{V_{CC} - V_{CEsat}}{R_L} = \frac{5{,}5V}{5.1\text{k}\Omega} = 1.08\text{mA}$$

$I_C = I_{IL} + I_L$ = 2.68 mA
and with CTR = 25 % $I_F = I_C$ / CTR = 10.72 mA

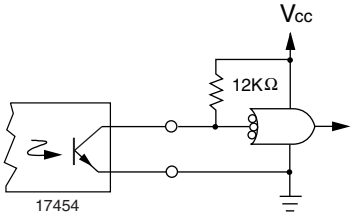
$$R_V = \frac{V_{CC} - V_F - V_{OL}}{10.72\text{mA}} = 317\Omega,\ R_V = 330\Omega$$

This interface circuit can be used for transmission rates of up to about 28 kbit/s The fact that considerably lower transmission rates are possible here compared with the circuit given in example 1 is partly due to the saturation state of the phototransistor and to a large extent to the higher value required for R_L.

Example 3:

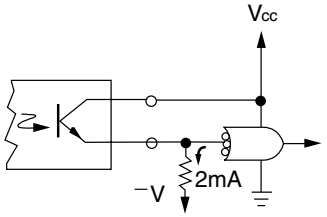
Here are other circuit configurations to interface with TTL circuit, specifically the 7400 family.

TTL Active Level Low (7400)

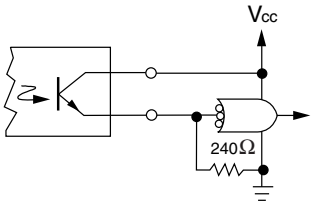


Note: Use smaller pull up resistor for higher speed.

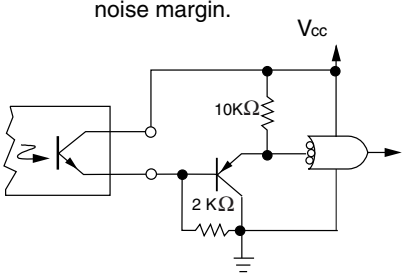
It is more difficult to operate into TTL gates in the active level high configuration. Some possible methods are as follows:



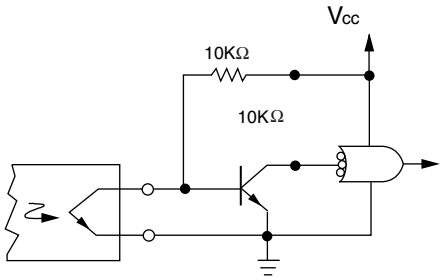
Note: Best method if negative supply is available.



Note: Requires 10 mA from transistor and sacrifices noise margin.

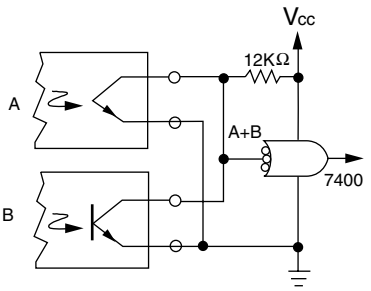


Note: High sensitivity but sacrifices noise margin. Needs extra parts.

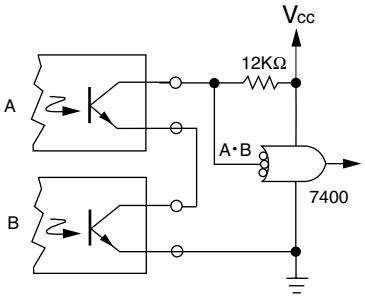


Note: Extra parts cost but high sensitivity.

Obviously, several optocoupler output transistors can be connected to perform logical functions.



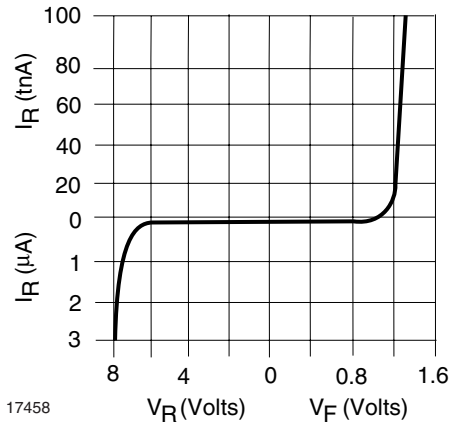
Note: Logical OR connection.



17457 Note: Logical AND connection.

Input Driving Circuits

The input side of the optocoupler has an emitter characteristic as shown.

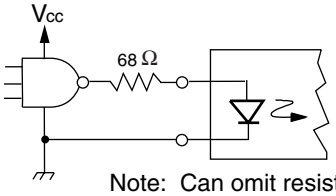


17458

The forward current must be controlled to provide the desired operating condition.

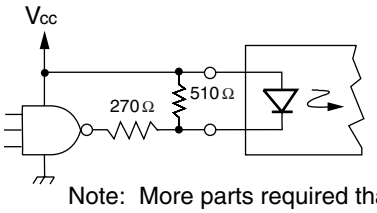
The input can be conveniently driven by integrated circuit logic elements in a number of different ways.

TTL Active Level High (7400 Series)

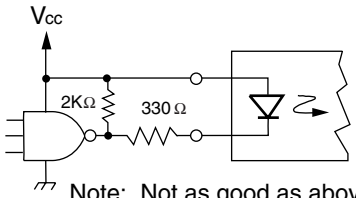


17459 Note: Can omit resistor for about 15 mA into diode.

TTL Active Level Low (7400 Series)



Note: More parts required than above.



17460 Note: Not as good as above circuit. Not recommended.

There are obviously many other ways to drive the device with logic signals, but a majority can be met with the above circuits. All provide 10 mA into the LED giving 2 mA minimum out of the phototransistor. The 1 V diode knee and its high capacitance (typically 100 pF), provides good noise immunity. The rise time and propagation delay can be reduced by biasing the diode on to perhaps 1 mA forward current, but the noise performance will be increased.

AC Input Compatible Optocoupler

Introduction

With the rapid penetration and diversification of electronic systems, demand for optocouplers is strengthening. Most popular are products featuring compact design, low cost, and high added value. To meet the market needs, Vishay is expanding the optocoupler. This application note focuses on optocouplers compatible with AC input, and covers configuration, principles of operation, and application examples.

Configuration (Internal PIN Connection Diagram)

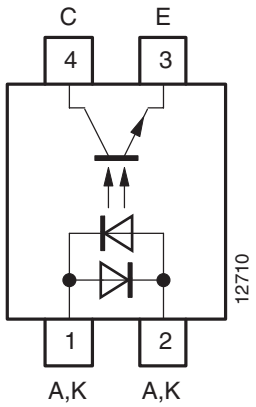


Figure 1. 4-Pin AC Input Optocoupler

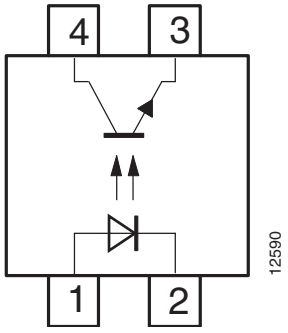


Figure 2. 4-Pin DC Input Optocoupler

Figure 1 shows the internal pin connection of a 4-pin AC input SFH620A-x optocoupler TCET1600, K814P Series, and Figure 2, of a 4-pin DC input optocoupler TCET1100, SFH61xA-x, and K817P Series. The main difference is that the AC input optocouplers incorporates an input circuit with two Emitters connected in reverse parallel. In the DC input optocoupler one Emitter is connected in the input circuit so that the Emitter emits light

to provide a signal when a current flows in one direction(1–>2 in Figure 1) (one–direction input type).

However, in the configuration shown in Figure 2, when a current flows in direction 1 to 2, Emitter1 emits light to send a signal, and when it flows from 2 to 1, Emitter 2 emits light to send a signal (bidirectional input type). Namely, even if the voltage level between 1 and 2 varies, and the positive and negative polarities are changed, either of two Emitters emits light to send a signal. This means that the one–direction input optocoupler permits DC input only, while the bidirectional input type permits AC input as well. The next section describes the status of output signals when V_{ac} power is directly input to an AC input compatible optocoupler via a current limit resistor.

Example 1: AC–DC converter

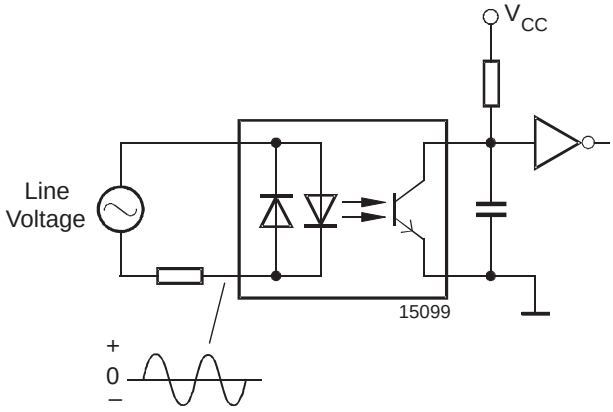


Figure 3. AC input compatible optocoupler (bidirectional input)

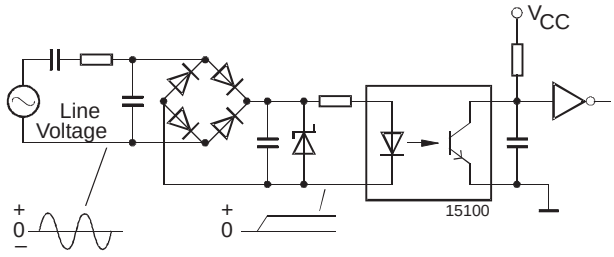


Figure 4. Conventional optocoupler (one-direction input)
(Full-wave rectification by means of diode bridge)

Example 2: Detection of a telephone bell signal

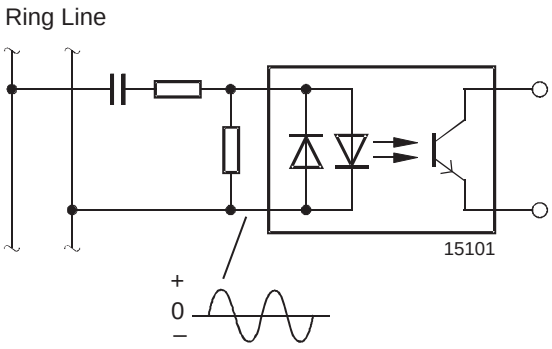


Figure 5.AC input compatible optocoupler (bidirectional input)

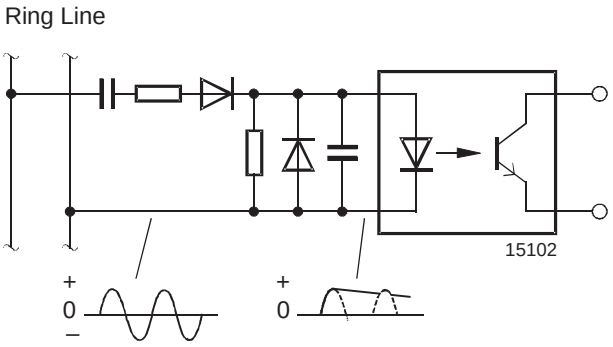


Figure 6. Conventional optocoupler (one-direction input)
(rectified by CR circuit)

Example 3: Sequencer circuit input section

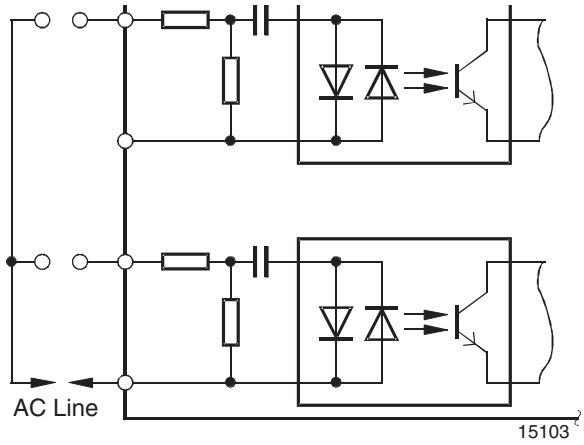


Figure 7. AC input compatible optocoupler (bidirectional input)

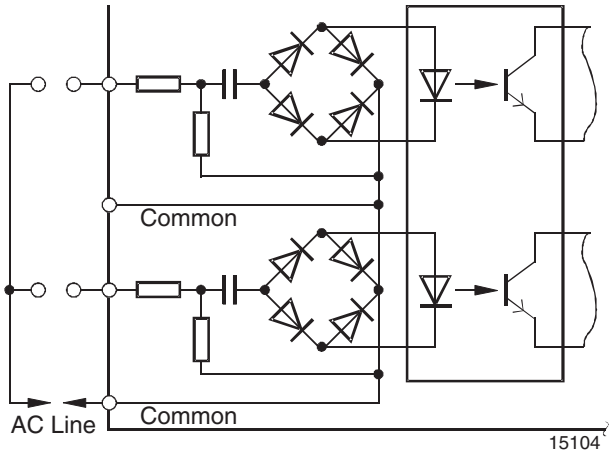
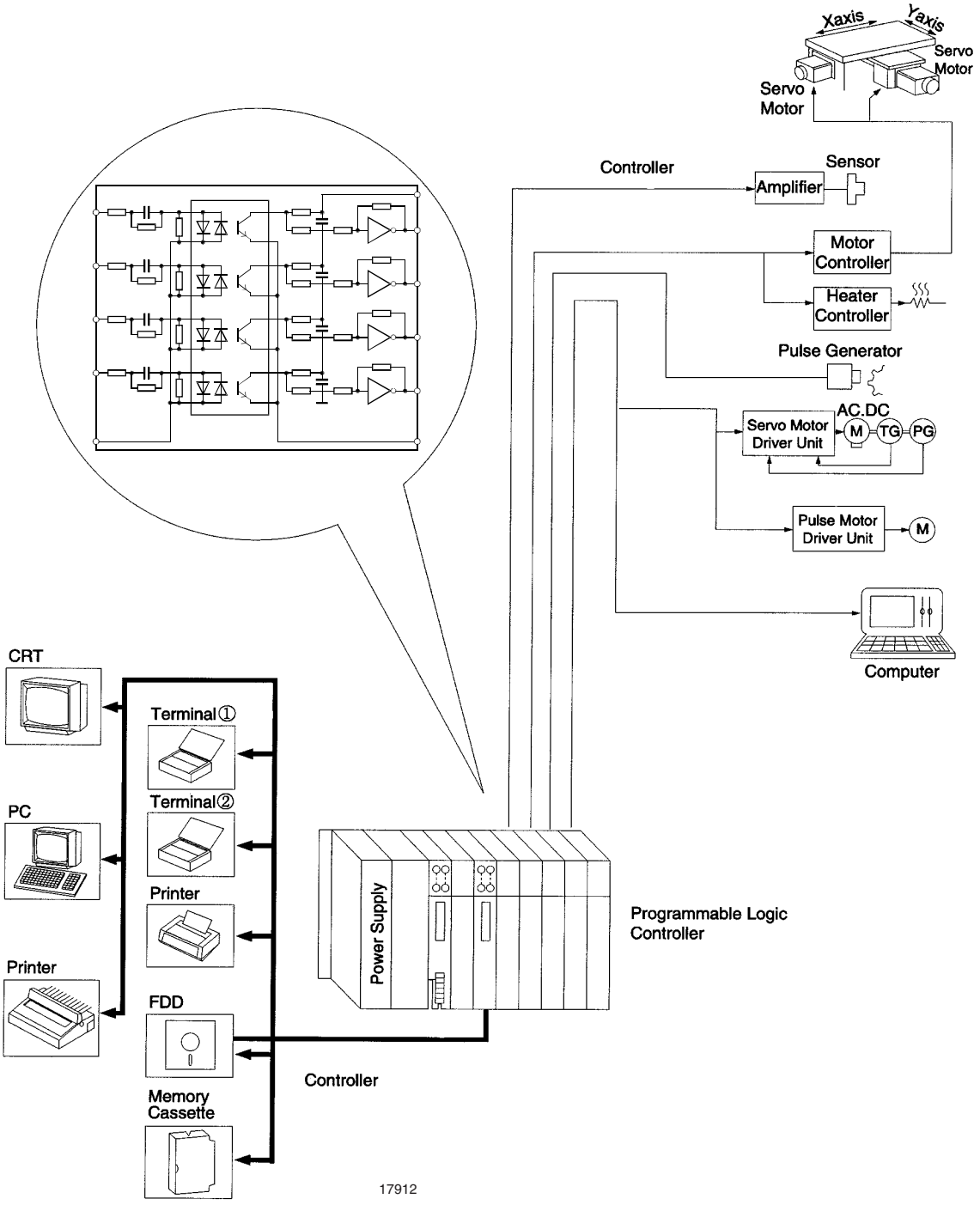


Figure 8. Conventional optocoupler (one-direction input)
(Full-wave rectified by diode bridge)

Programmable Logic Controller Example

Purpose: in–out interface



Driving High-Level Loads With Optocouplers (Appnote 4)

Frequently a load to be driven by an optocoupler requires more current, voltage, or both, than an optocoupler can provide at its output.

Available optocoupler output current is found by multiplying input (LED section) current by the "CTR" or current transfer ratio. For worst-case design, the minimum specified value would be used. The minimum CTR of the IL1 is 20 %. Temperature derating is not usually necessary over the 0 °C to + 60 °C range because the LED light output and transistor beta have approximately compensating coefficients.

Multiplying the minimum CTR by 0.9 would ensure a safe design over this temperature range. Over a wide range, more margin would be required.

The LED source current is limited by its rated power dissipation. Table 1 shows maximum allowable I_F versus maximum ambient temperature.

Values for Table 1 are based on a 1.33 mW/°C derate from the 100 mW at 25 °C power rating.

Maximum Temperature	I_F Maximum
40°C	50 mA
60°C	35 mA
80°C	17 mA

Table 1:

Obviously, one can increase the available output current either by choosing a higher CTR-rated optocoupler or by providing more current, or both. Table 2 shows the minimum available output current for the IL1, at T_A = 60 °C (from Table 1) and a 10 percent margin for temperature effects.

P/N	I_{CE} (min) mA
IL1	6.3

Table 2:

If the IL1 is being operated from logic with 5 V driving transistor and 0.2 V V_{CE} saturation is assumed for the driving transistor; a 75 Ω R_{IF} resistor will provide the 48 mA. The forward voltage of the IR-emitting LED is about 1.2 V. Figures 1 and Figure 2 show two such drive circuits.

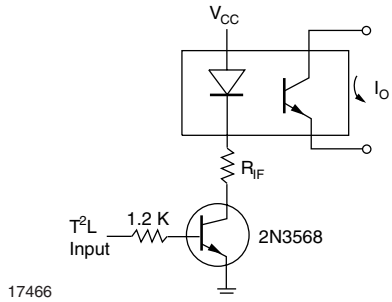


Figure 1. NPN driver

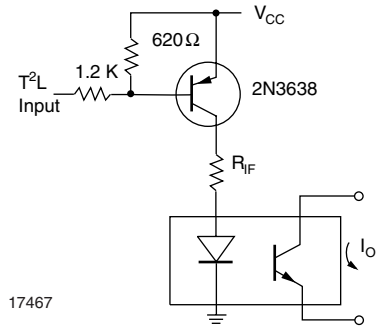


Figure 2. PNP driver

A "buffer-gate," such as the SN7440 provides a very good alternative to discrete transistor drivers. Figure 3 shows how this is done. Note that the gate is used in the "current-sinking" rather than the "current-sourcing" mode. In other words, conventional current flows into the buffer-gate to turn on the LED. This makes use of the fact that a T^2L gate will sink more current than it will source. The SN7440 is specified to drive thirty 1.6 mA loads or 48 mA. Changing R_{IF} from 75 to 68 Ω adjusts for the higher saturation voltage of the monolithic device.

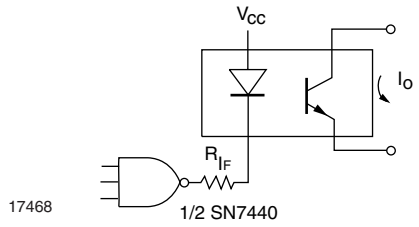


Figure 3. Buffer-gate drive

More Current

For load currents greater than 6.3 mA, a current amplifier is required. Figure 4 and Figure 5 show two simple one-transistor current amplifier circuits.

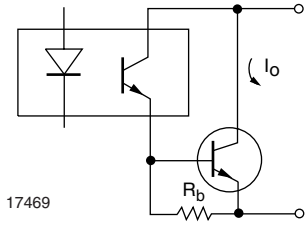


Figure 4. NPN current booster

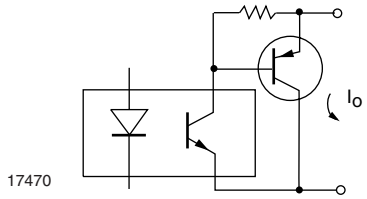


Figure 5. PNP current booster

Since the transistor in the optocoupler is treated as a two-terminal device, no operational difference exists between the NPN and the PNP circuits. R_b provides a return path for I_{CBO} of the output transistor. Its value is: R_b = 400 mV/I_{CBO} (T) where I_{CBO}(T) is found for the highest *junction* temperature expected.

Assume that leakage currents double every ten degrees. Use the maximum dissipated power, the specified maximum junction-to-ambient thermal resistance, and the maximum design ambient temperature in conjunction with the specified maximum 25° I_{CBO} to calculate I_{CBO}(T).As an example, suppose a 2N3568 is used to provide a 100 mA load current. Also assume a maximum steady-state transistor power dissipation of 100 mW and a 60°C maximum ambient. The transistor junction-to-ambient thermal resistance is 333° C/watt, so a maximum junction temperature of 60 + 33 or 93 °C is expected. This is about 7 decades above 25 °C.

Therefore,
I_{CBO}(T) = I_{CBO}(max) x 27 = 50 nA x 128 = 6.5 µA.
A safe value for R_b is 400 mV/6.5 µA = 62 kΩ.

Working backwards, maximum base current under load will be I_O/h_{FE}(min) = 100 mA/100 = 1 mA. Current in R_b is V_{BE}/R_b = 600 mV/60 k = 10 µA, which is negligible. An IL1 with a 9 mA drive would operate effectively.

If the load requires more current than can be obtained with the highest beta transistor available, then more than one transistor must be used in cascade. For example, suppose 3 A load current and 10 W dissipation are needed. A Motorola MJE3055 might be used for the output transistor, driven by a MJE205 as shown in Figure 6. Using a 5 °/W heat sink and the rated MJE3055 junction-to-case thermal resistance of 1.4 °/W, we find that junction temperature rise is 6.4 x 10, or 64 °. Therefore maximum junction temperature is 124 °C. This is 10 decades above 25 °C making $I_{CBO}(T) = 2^{10}\ I_{CBO}(max) = 10^3\ I_{CBO}(max)$ I_{CBO}(max) at 30 V or less is not given, but I_{CEO} is. Using (for safety) a value of 20 for the minimum low current h_{FE} of the device, I_{CBO} could be as large as $I_{CEO}/20$ = 35 µA. Then I_{CBO}(T) is 35 mA and R_{b2} = 400 mV/ 35 mA = 11 Ω. For I_b use I_O/h_{FE} (min. at 4 A) = 3 A/20 = 150 mA.
I_{Rb2} = 600 mV/ 10 Ω = 60 mA, so $I_{e(Q1)}$ = 210 mA

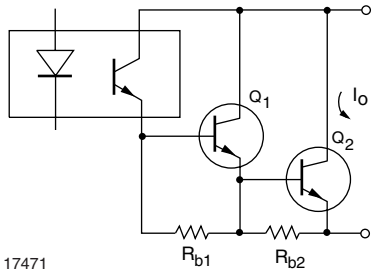


Figure 6. Two NPN current boosters

Maximum power in Q_1 will be about 1/14 the power in Q_2 since its current is lower by that ratio and the two collector-to-emitter voltages are nearly the same. This means Q_1 must dissipate 700 mW.

Assuming a small "flag" heat sink having 50°/W thermal resistance, we find the junction at about 95°C. The 150 °C case temperature I_{CBO} rating for this device is 2 mA, so one can work backwards and

assume about 1/30 of this value, or 70 µA. On the other hand, the 25° rated I_{CBO} is 100 µA. Choosing the larger of these contradictory specifications, R_{b1} = 400 mV/0.1 mA = 4 k ≈ 3.9 k. Q_1 base current is $I_{E(Q1)}/h_{FE(Q1\text{-}mjn)}$ = 210 mA/50* = 4.2 mA. Total current is $I_{b(Q1)}$ + I_{Rb1} = 4.2 + 0.24 = 4.5 mA. Table 2 shows that an IL1 could be used here.

* Minimum h_{FE} is obtained using the specification at I_{CE} = 2 A and the "Normalized DC Current Gain" graph given in Motorola's "Semiconductor Data Book", 5th edition, pp. 7–232 and 7–233.

More Load Voltages

All of the current-gain circuits shown so far have one common feature: load voltage is limited by the 30 V rating of the IL1 not by the voltage or power rating of the transistor(s).

Figure 7 shows a method of overcoming this limitation. This circuit will stand off BV_{CEO} of Q_1. The voltage rating of the phototransistor is irrelevant since its maximum collector-emitter voltage is the base emitter voltage of Q_1 (about 0.7 V).

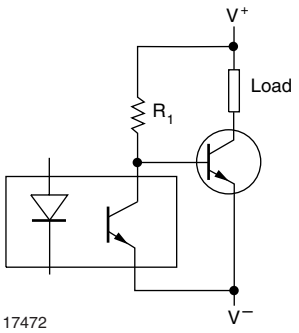


Figure 7. NPN HV booster

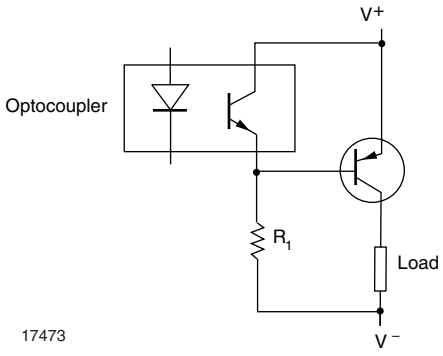


Figure 8. PNP HV booster

Unlike the "Darlington" configurations shown previously, this circuit operates "normally-ON." When no current flows in the LED the phototransistor, being OFF, allows R_2 current to flow into the base of Q_1, turning Q_1 ON. When the optocoupler is energized, its phototransistor "shorts out" the R_2 current turning Q_1 OFF.

The value of R_1 depends only on the load-supply voltage $V^+ - V^-$, and the maximum required Q_1 base current. This is derived from the minimum beta Of Q_1 at minimum temperature and the load current. The required current-drive capability is the same as I_{R1}, since I_{R1} changes negligibly when the circuit goes between its "ON" and "OFF" states.

In some applications either more current gain will be required than one transistor can provide or the power dissipated in R_1 will be objectionable. In these cases, simply use the Darlington high-voltage boosters shown in Figure 9.

If more than one load is being driven and their negative terminals must be in common, use the PNP circuit (Figure 10). Otherwise, the NPN is better because the transistors cost less. Performance characteristics of the NPN and PNP versions are identical if the device parameters are also the same.

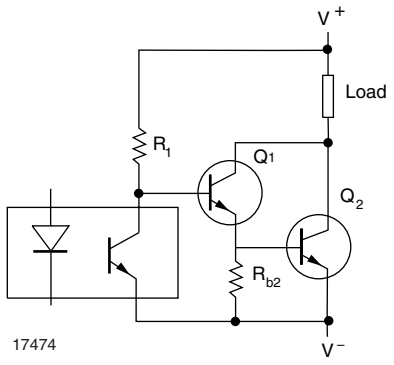


Figure 9. NPN Darlington HV booster

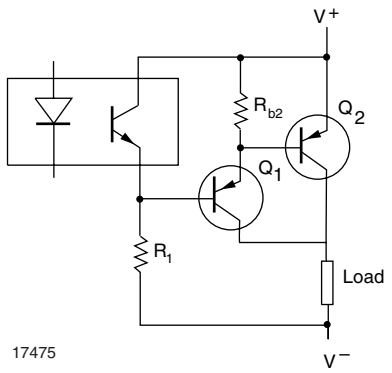


Figure 10. PNP Darlington HV booster

Applications

Optocoupler isolated circuits are useful wherever ground loop problems exist in systems, or where dc voltage level translations are needed. In many systems so-called interpose relays are used between a logic circuit section (which may be a mini-computer) and the devices being controlled. Sometimes *two levels* of interpose relays are used in cascade either because of the load power level or because of extreme difficulties with EMI. Optocouplers aided by booster circuits such as those described can replace many of the relays in these systems.

The reed relays, typically used as the first level of interpose and mounted on the interface logic cards in the electronic part of the system, are almost always replaceable by optocouplers since their load is just the coil of a larger relay. This relay may have a coil power of 1/2 to 5 W and operate on 12, 24 or 48 V dc.

Assuming worst-case design techniques are carefully followed, system reliability should improve in proportion to the number of relays replaced.

Manufacturing and Reliability

The Importance of Optocoupler Reliability

Because of the widespread use of optocouplers as an interface device, optocoupler reliability has been of major importance to circuit designers and components engineers. Published studies of comparative tests have indicated a lack of manufacturing consistency with individual manufacturers as well as from manufacturer to manufacturer. This has resulted in user uncertainty about designing in optocouplers. These devices often offer the better circuit solution.

This is intended to demonstrate Vishay's concern, efforts, and results in addressing these manufacturing issues to assure users of the quality (out-going) and reliability (long term) of our opto-isolated products. First, aspects of optocoupler characteristics are discussed along with the measures Vishay has taken to assure their quality and reliability. Second, the reliability tests used to approximate worst case conditions and the latest results of these tests are described.

Optocoupler Output

There are a variety of outputs available in optocouplers. A standard bipolar phototransistor is the most common. They are available with different ratings to fit most applications, including versions without access to the base of the transistor to reduce noise transmission. Darlington transistor outputs offer high gain with reduced input current requirements, but typically trade off speed. Logic optocouplers provide speed but trade off working voltage range. Logic couplers are normally only used in data transmission applications. Silicon Controlled Rectifier (SCR) devices allow control of much higher voltages and typically are applied to control AC loads. They are also offered in inverse-parallel (anti-parallel) SCR (triac) configurations that both cycles of an AC sinusoid can be switched. In Vishay's manufacturing flow, all these devices are 100 % monitored at a high temperature hot rail (see Figure 1) to eliminate potential failures due to marginal die attaches and lead bends, resulting in a more reliable product. Vishay offers all the above types of products.

In optocouplers, especially the transistor, the slow change over several days in the electrical parameters when voltage is applied, is termed the field effect. This process is extreme particularly at high temperatures (100 °C) and with a high DC voltage (1 kV). Changes in the electrical parameters of the silicon phototransistor can occur due to the release of charge carriers. In this way, a similar effect as takes place in a MOS transistor (inversion at the surface) is caused by the strong electrical field. This may result in changes in the gain, the reverse current, and the reverse voltage. In this case, the direction of the electrical field is a decisive factor.

In Vishay's optocouplers, the pn junctions of the silicon phototransistor are protected by a transparent ion screen from influences of the electrical field. In this way, changes of electrical parameters by the electrical field are limited to an extremely low value or do not occur at all.

Optocoupler Input

The area of greatest concern in optocoupler reliability has been the IR LED. The decrease in LED light output power over current flow time has been the object of considerable attention in order to reduce its effects. (Circuit designs which have not included allowances for parametric changes with temperature, input current, phototransistor bias, etc. have been attributed to LED degradation. To insure reliable system operation over time, the variation of circuit from data sheet conditions must be considered.)

Vishay has focused on the infrared LED to improve CTR degradation and consequently achieved a significant improvement in coupler reliability. The improvements have included die geometry to improve coupling efficiency metallization techniques to increase die shear strength and to increase yields while reducing user cost, and junction coating techniques to protect against mechanical stresses, thus stabilizing long term output.

Current Transfer Ratio

The Current Transfer Ratio (CTR) is the amount of output current derived from the amount of input current. CTR is normally expressed as a percent. For example, if 10 mA of input current is applied to the input (LED) and 10 mA of collector current is obtained, then the CTR is 100 or 100 %. CTR is affected by a variety of influences: LED output power, h_{fe} of the transistor, temperature, diode current, and device geometry. If all these factors remain constant, the principle cause of CTR degradation is the degradation of the input LED.

As mentioned earlier, Vishay has made tremendous progress in manufacturing techniques to reduce CTR degradation. Vishay's manufacturing techniques

maximize coupling efficiency which realize high transfer ratios and low input current requirements. Additionally this allows a large variety of standard CTR values, and the capability of special selection in production volumes.

Isolation Breakdown Voltage

Isolation voltage is the maximum voltage which may be applied across the input and output of the device without breaking down. This breakdown will not normally occur inside the package between the LED and the transistor, but rather on the boundary surfaces across which partial discharges can occur. Vishay uses a double mold manufacturing technique where the LED and transistor are encapsulated in an infrared transparent inner mold. The next step in the process is an epoxy over mold. The double mold technique lengthens the leakage path for high voltages discharges appreciably, allowing the device to achieve very high isolation voltages. All of Vishay's optocouplers are built using U.L. approved process. A standard line of VDE approved optocouplers is also available in Agency Table section.

Collector to Emitter Breakdown Voltage

Collector to emitter breakdown voltage (BV_{CEO}) can be thought of as a transistor's working voltage. When considering the application, the selection should be made to include a safety margin to insure the device is off when it is supposed to be off. Vishay transistor technology in wafer processing offers a variety of BV_{CEO} devices. Each is parametrically tested to insure proper operation (see Figure 1).

Blocking Voltage

Blocking voltage (V_{DRM}, expressed in peak value) is used when describing the working voltage for SCR or triac type devices. Vishay offers products through 800 V of blocking capability.

DV/DT Rating

DV/DT, an important safety specification, describes a triac type device's capability to withstand a rapidly rising voltage without turning on or false firing. Vishay's triac type devices have the highest available DV/DT rating offered on the market. Vishay's manufacturing process yields a 10,000 V/µs DV/DT rating. This rating eliminates the need for snubber (RC) networks which negatively affect loads sensitive to leakage currents, while reducing component count for circuit implementation and cost. An example of such a load would be neon indicator lamps. Vishay's triac type devices also carry a load current rating three times the industry standard. This 300 mA current capability allows the device to drive most AC loads without the need for a follow-on triac or interposing an electromechanical relay. Vishay manufactures this device with or without zero crossing detector logic.

Test	MIL-STD-883 Reference	Test Condition
Pre-condition	—	Baking 150°C, 16 hours, RTSH
Thermal Climatic	1010 1004	TC – 55 °C to + 150 °C, 100 Cycles MC 25 °C/ 95 % RH, 12 hours 85 °C/ 95 % RH, 12 hours V_{LED} = 0.8 V_R Max. V_{DET} = 0.8 V_{CE} Max. 14 Cycles ALT Max. power at 25 °C, 168 hours
Solderability	2003	260 °C, 5 Seconds

Table 1: Reliability Requirements for Optocouplers Environmental Tests

Tests	Test Conditions			
	Temp (°C)	RH (%)	Bias	Hours
Ambient Life Test	25	ð60%	Max Rating	1000
Elevated Life Test	70	ð60%	Derated Max Rating	1000
High Temp Life Test Low Temp Life Test Temp/Humidity Life Intermittent Operating Life	150 – 55 85 25	ð60% ð60% 85% ð60%	0 0 0 Max Rating	1000 1000 1000 1000
High Temperature Reverse Bias	125	ð60%	80 % of Max Voltage Rating	1000

Table 2: Life Tests

Quality and Reliability Tests

The tests in Figure 1 were performed on Vishay optocouplers. The tests allow early detection of weak points and provide information regarding the reliability characteristics of the component.

From the Life Test information assumptions of useful life expectancy can be obtained. All quality and reliability tests are performed in conditions that either exceed or are equivalent to the limits defined in our data sheets. International standards are also considered. Assuming that no additional failure mechanisms are created by the stress conditions, the results of the stress test will correlate to conditions in the field and

can be used to estimate useful lifetime. The environmental stress tests ensure Vishay's manufacturing capabilities will provide package integrity in the most rigorous conditions The Life Test results highlight our ability in packaging and electrical performance to achieve MTBF hours which meet exceed the highest industry standards for the semiconductor.

Package Integrity

Although packaged in standard IC configurations, optocouplers have some unique package considerations. The use of two chip and internal light transfer medium require careful selection of materials to insure compatibility under a variety of operating conditions. In addition to the high isolation voltages achieved by Vishay optocouplers, our devices are tested to assure high levels of mechanical integrity and moisture resistance. For example, a ninety-six hour pressure pot test has been implemented to more stringently verify moisture resistance.

Package Density

Board space has become increasingly important in the electronic industry. Vishay uses a plate molding technique to achieve reduction in cost, allowing us to offer a wide selection of packages. These consist of single channel optocouplers in 4, 6, 8, and 16 pin packages, dual channel devices in 8 pin DIP or SMD packages, and quad channel devices in 16 pin DIP packages. The above devices are available in two surface mount lead configurations, as well as the standard through-hole lead. Vishay has also a standard single and dual channel optocoupler in a SOIC-8 package. The dual SOIC-8 package has the highest packaging density of any high volume standard optocoupler available. All of these packages have been designed and tested to meet the highest quality and reliability expectations of the semiconductor industry.

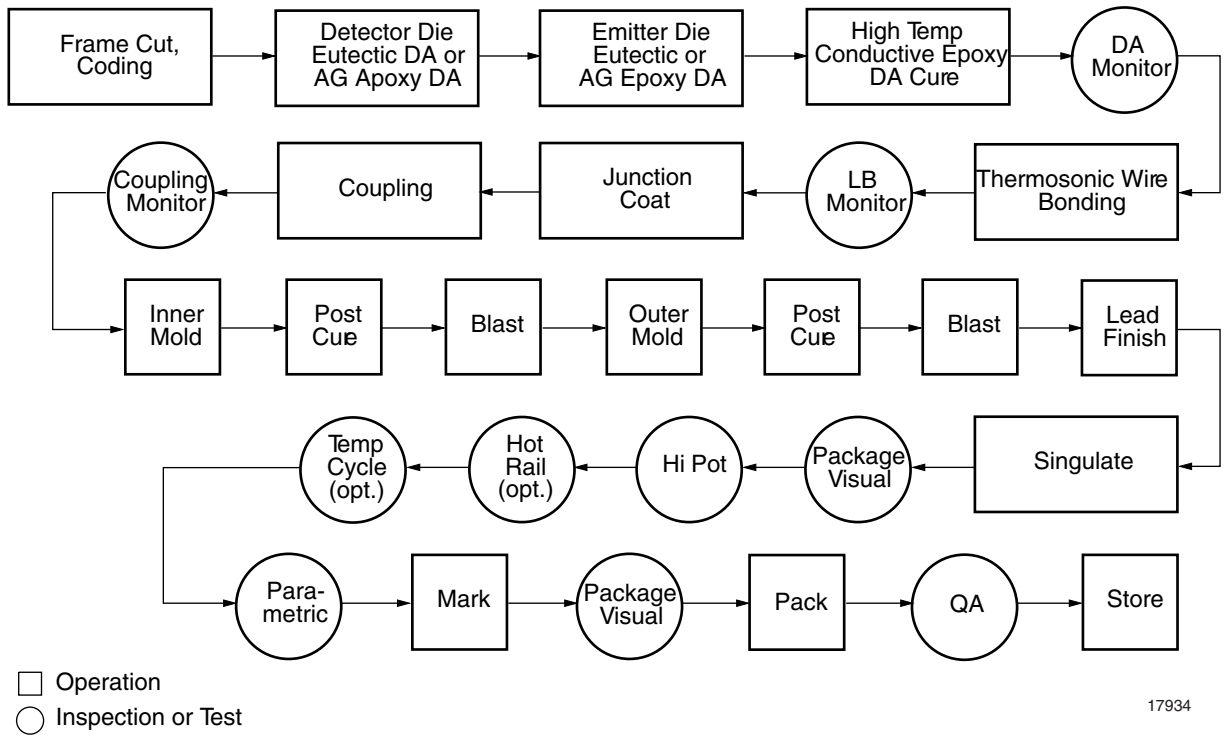


Figure 1. Coupler Process Flow and Inspections

Footprints

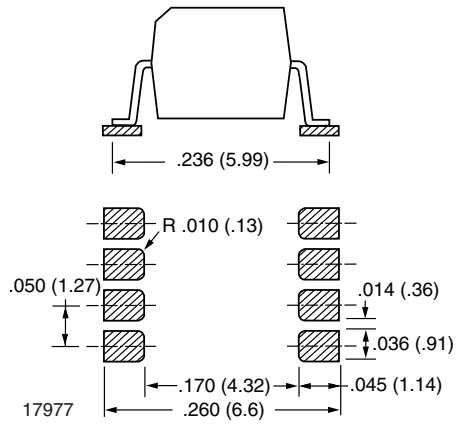


Figure 1. SO8A and DSO8A SMD

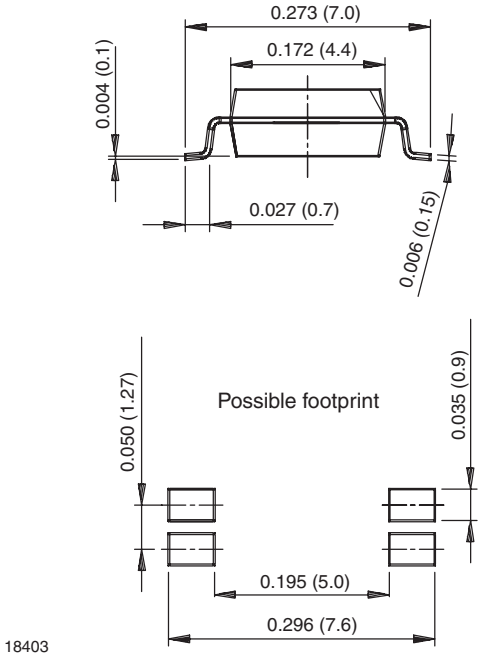


Figure 2. SOP-4, Miniflat

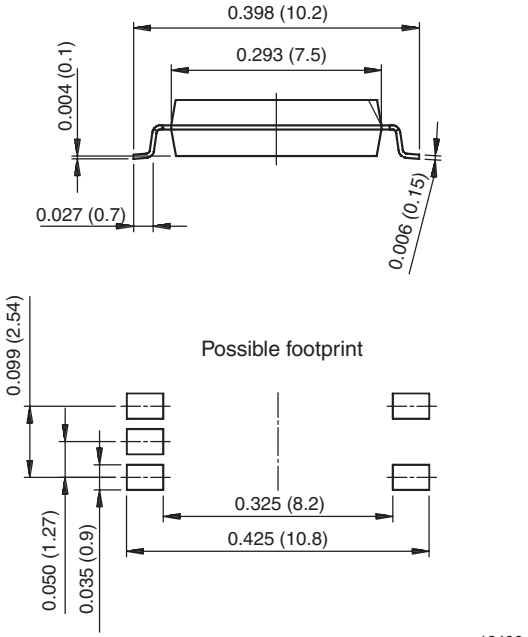


Figure 3. SOP-6, 5-pin wide body

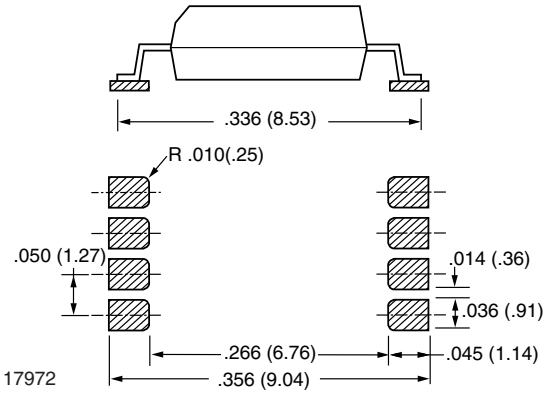


Figure 4. 8-pin PCMCIA

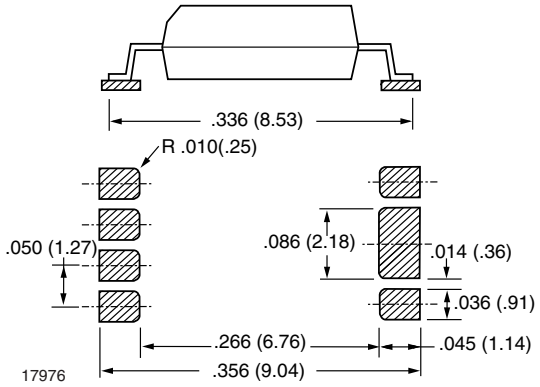


Figure 5. 8-pin PCMCIA, heat sink

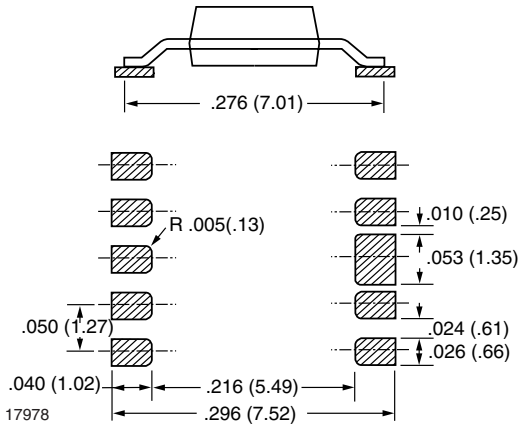


Figure 6. Mini coupler

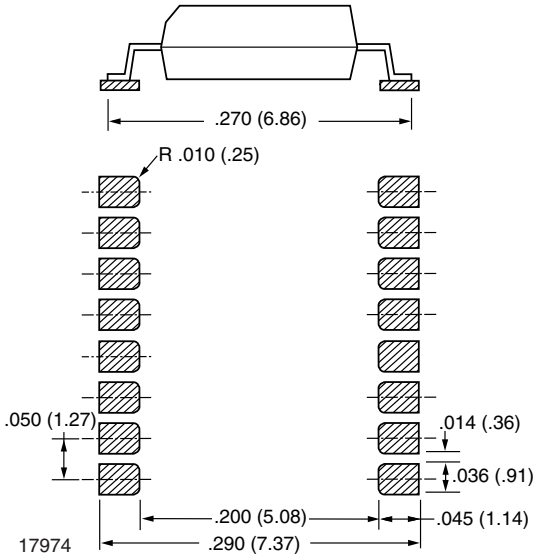


Figure 7. SOP-16

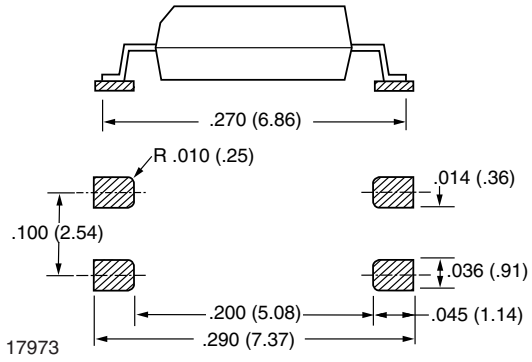


Figure 8. 4-pin MINI-FLAT

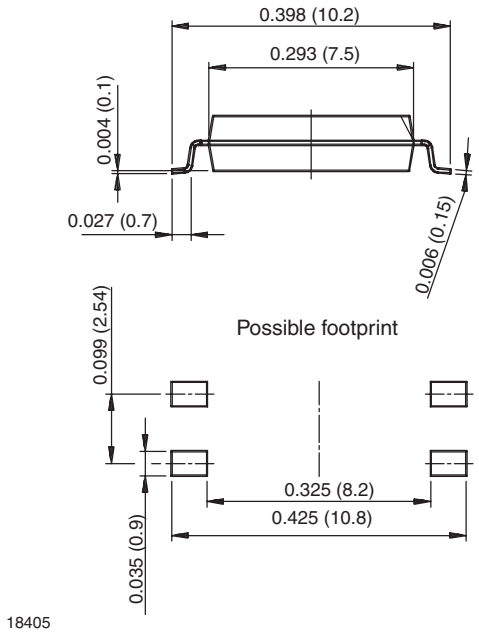


Figure 9. SOP-6, 4-pin wide body

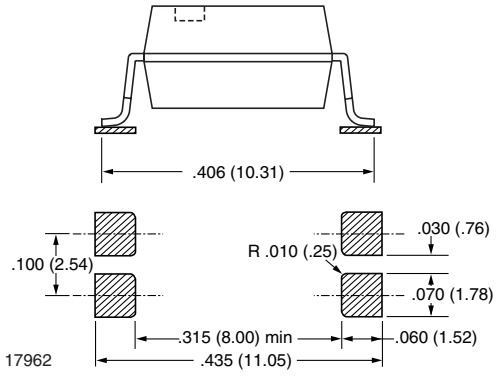


Figure 10. 4-pin SMD option 7

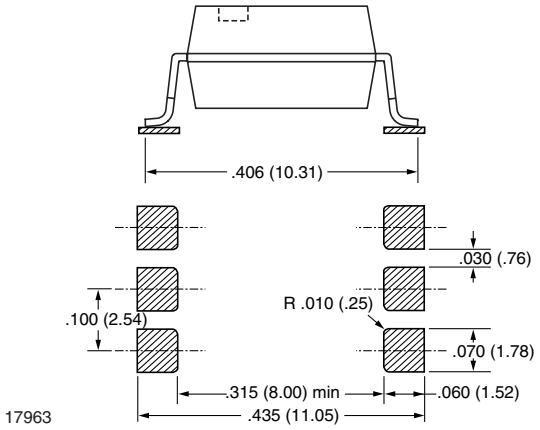


Figure 11. 6-pin SMD option 7

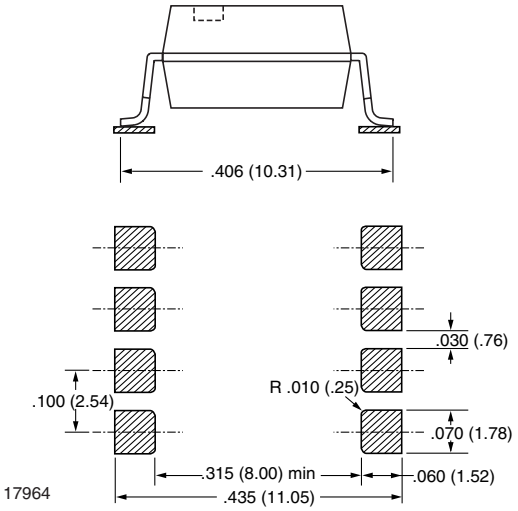


Figure 12. 8-pin SMD option 7

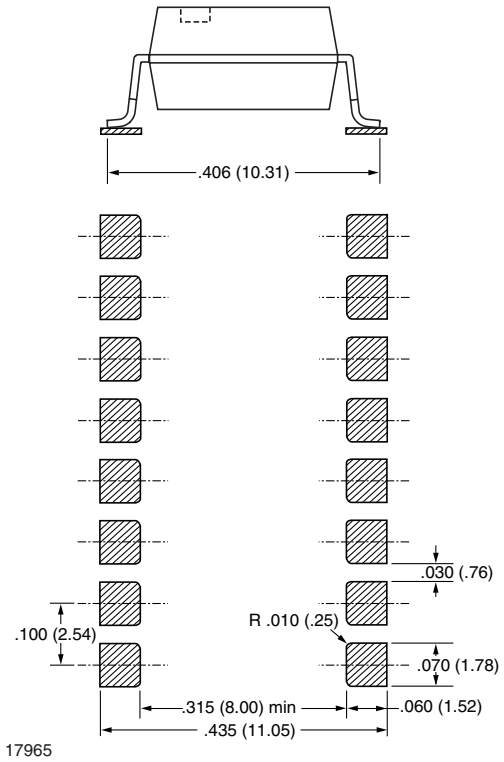


Figure 13. 16-pin SMD option 7

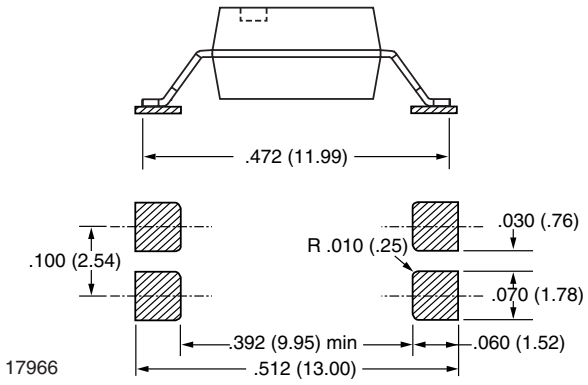


Figure 14. 4-pin SMD option 8

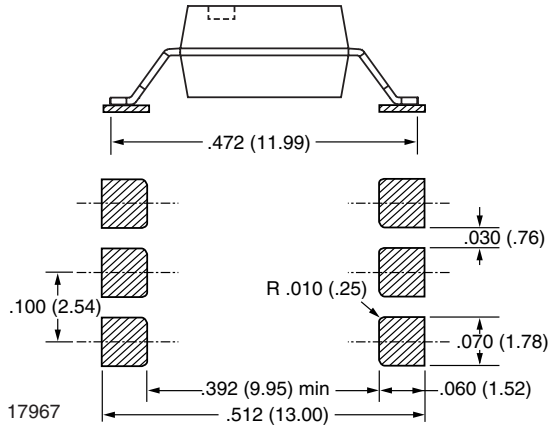


Figure 15. 6-pin SMD option 8

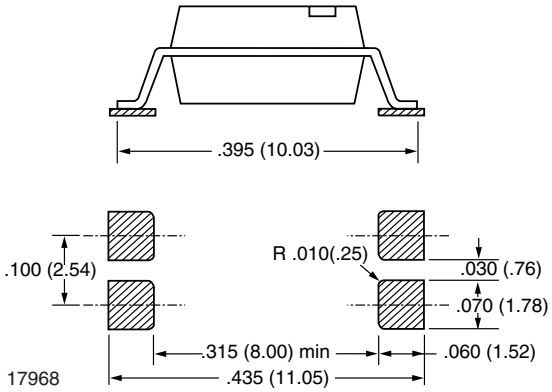


Figure 16. 4-pin SMD option 9

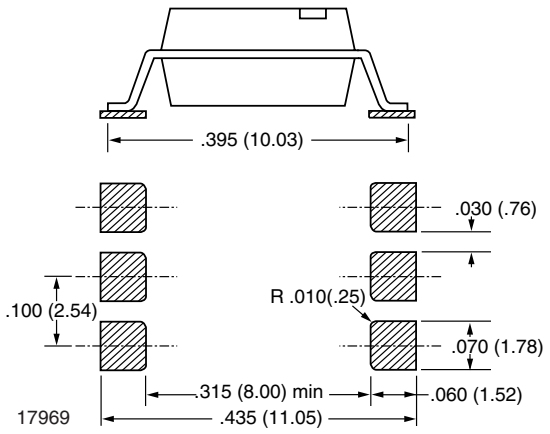


Figure 17. 6-pin SMD option 9

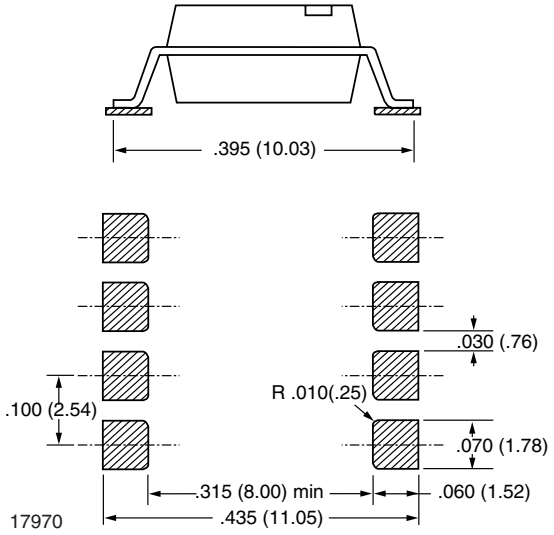


Figure 18. 8-pin SMD option 9

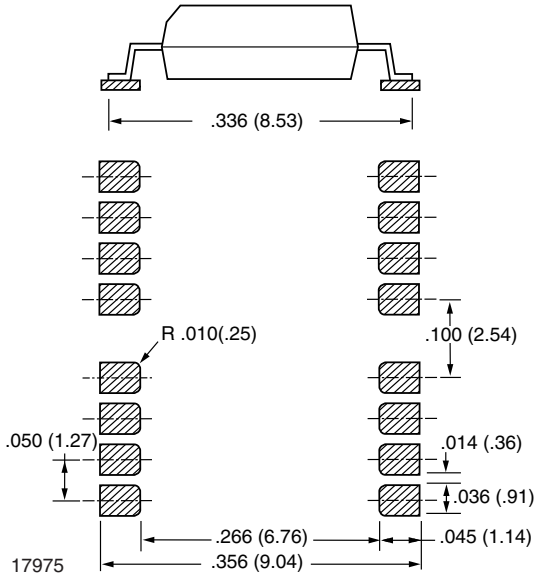


Figure 20. 16-pin PCMCIA

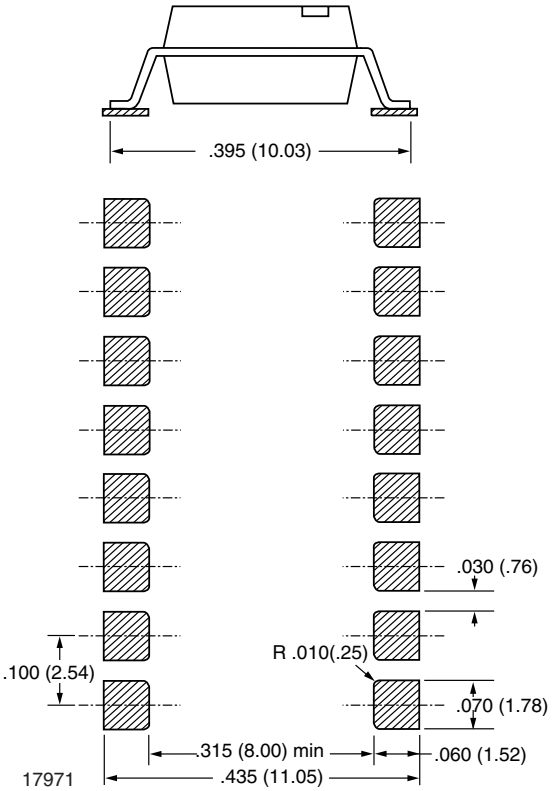
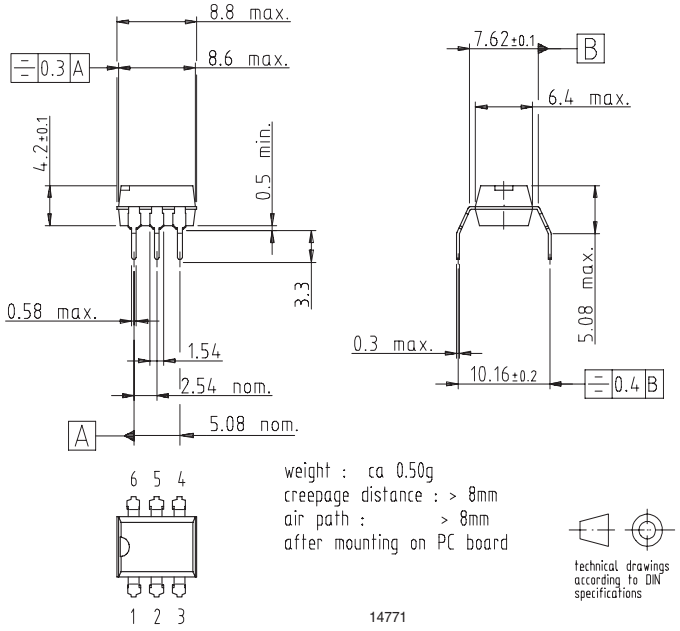


Figure 19. 16-pin SMD option 9

DIL400-6

Package Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operatingsystems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

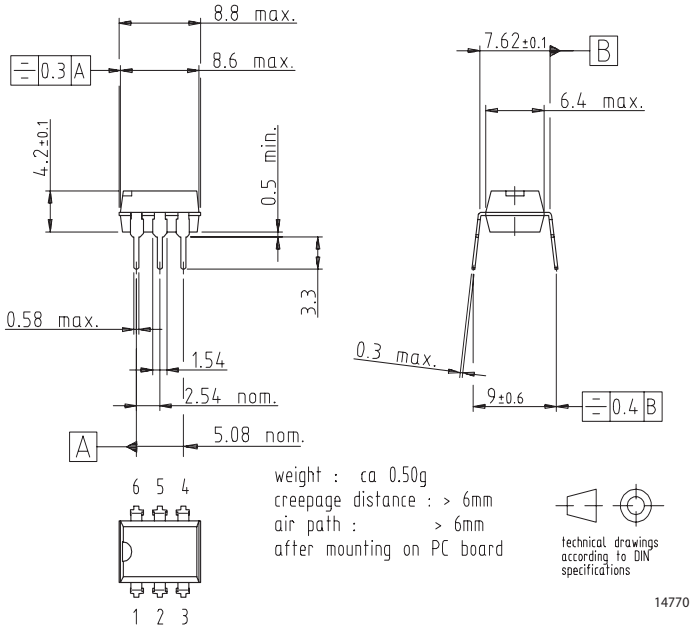
1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423

DIL300-6

Package Dimensions in mm



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Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423

Standard Marking on Optocouplers

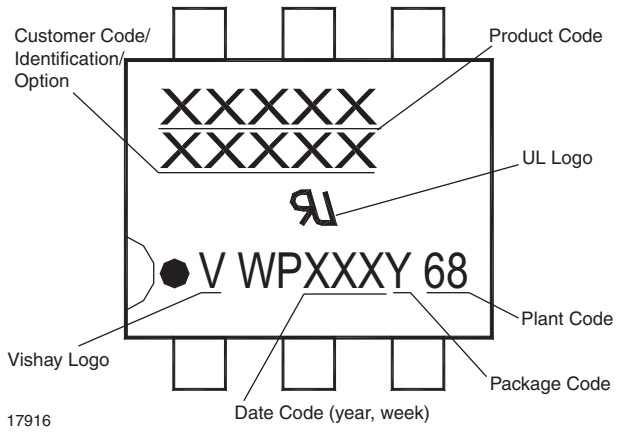

Figure 1. 6-pin

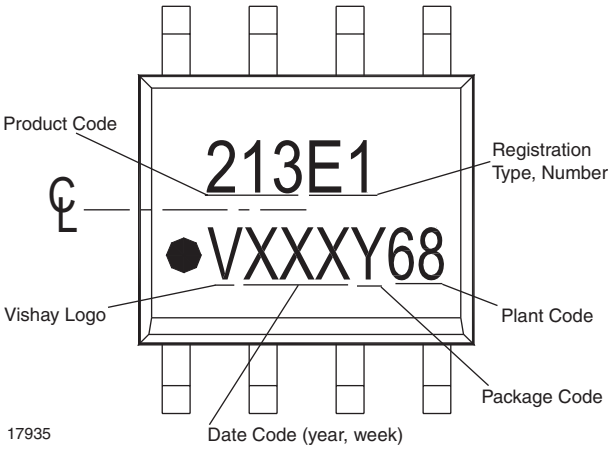

Figure 2. Single and Dual SO-8

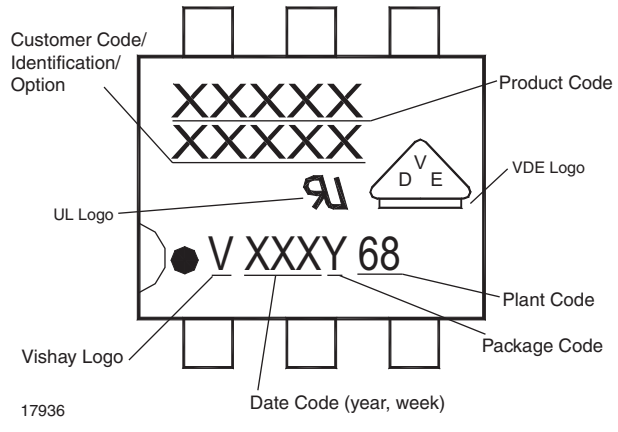

Figure 3. DIP-6 Products

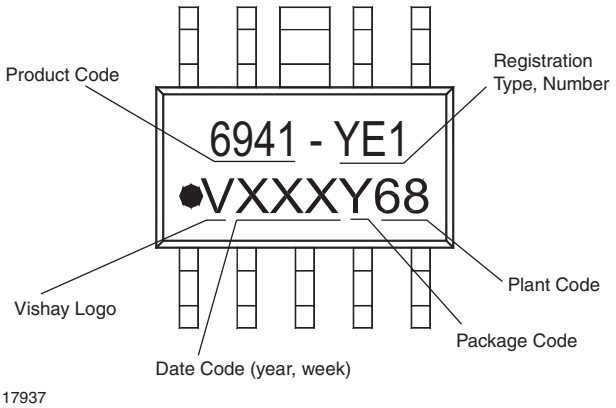

Figure 4. Minicoupler

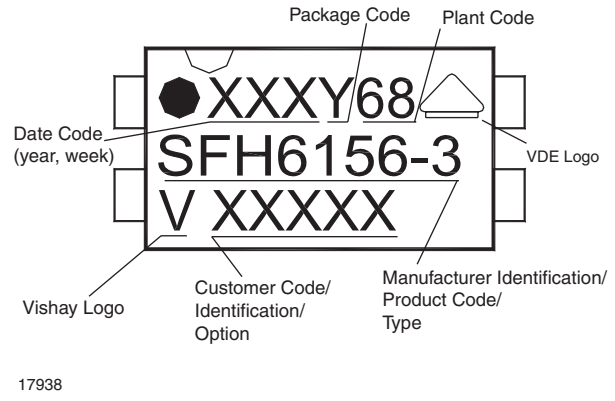

Figure 5. DIP-4 Products

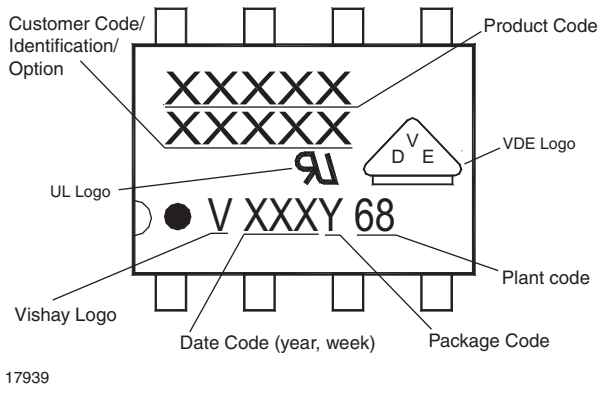

Figure 6. DIP-8 Products

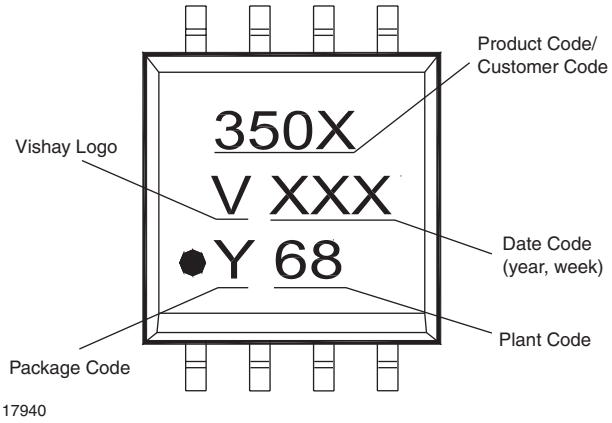

Figure 7. PCMCIA Products

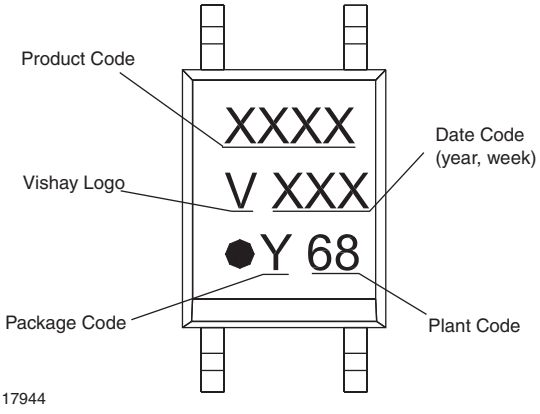

Figure 8. Pin Miniflat/ 4 Pin Flatpack

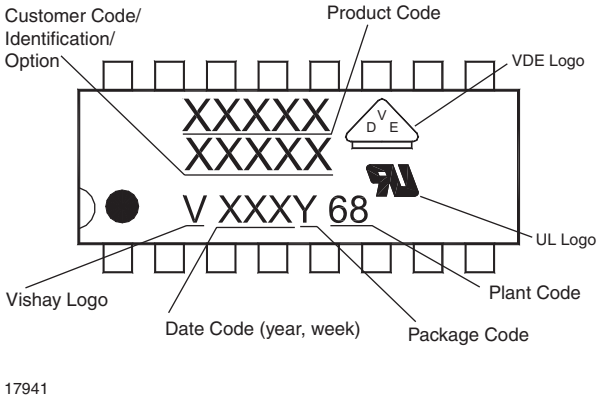

Figure 9. DIP-16 Products

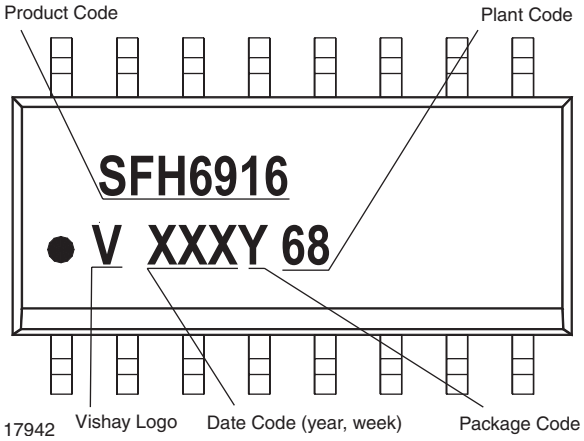

Figure 10. 16 Pin Miniflat

Markings

The following table defines the option information that is marked on the product.

Option type	Marking	Definition
X001, X001T	X001	Partial discharge test per DIN EN 60747-5-2 (VDE0884)
X006	No mark	10.16 mm (400 mil) through hole lead spread
X007, X007T	X007	SMD lead form bend, 0.9 mm maximum standoff height
X008, X008T	X008	SMD lead form bend, 9.3 mm lead spread
X009, X009T	No Mark	SMD lead form bend, 0.25 mm maximum standoff height
X016	X001	Partial discharge test and 400 mil through hole lead spread
X017, X017T	X017	Partial discharge test and SMD lead form bend, 0.9 mm standoff
X018, X018T	X018	Partial discharge test and SMD lead form bend, 9.3 mm lead spread
X019, X019T	X001	Partial discharge test and SMD lead form bend, 0.25 mm standoff

Options are added to optocouplers in DIP package. For SOIC-8 packages, only option 1 can be added. Please contact your local Vishay sales office for availability of option combinations.

Quality Information

Corporate Quality Policy

Our goal is to exceed the quality expectations of our customers. This commitment starts with top management and extends through the entire organization. It is achieved through innovation, technical excellence and continuous improvement.

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Figure 1. VISHAY quality policy

VISHAY INTERTECHNOLOGY; INC.
ENVIRONMENTAL, HEALTH AND SAFETY POLICY

VISHAY INTERTECHNOLOGY, INC. is committed to conducting its worldwide operations in a socially responsible and ethical manner to protect the environment, and ensure the safety and health of our employees to conduct their daily activities in an environmentally responsible manner.

Protection of the Environment: Conduct our business operation in a manner that protects the environmental quality of the communities in which our facilities are located. Reduce risks involved with storage and use of hazardous materials. The company is also committed to continual improvement of its environmental performance.

Compliance with Environmental, Health and Safety Laws and Regulations:
Comply with all relevant environmental, health and safety laws and regulations in every location.
Maintain a system that provides timely updates of regulatory change.
Cooperate fully with governmental agencies in meeting applicable requirements.

Energy, Resource Conservation and Pollution Control: Strive to minimize energy and material consumption in the design of products and processes, and in the operation of our facilities. Promote the recycling of materials, including hazardous wastes, whenever possible. Minimize the generation of hazardous and non-hazardous wastes at our facilities to prevent or eliminate pollution. Manage and dispose of wastes safely and responsibly.

Figure 2. VISHAY Quality road map

Quality System

Quality Program

At the heart of the quality process is the VISHAY worldwide quality program. This program, which has been in place since the early 90's, is specifically designed to meet rapidly increasing customer quality demands now and in the future.

Vishay Corporate Quality implements the Quality Policy and translates its requirements for use throughout the worldwide organization.

VISHAY Quality has defined a roadmap with specific targets along the way. The major target is to achieve world-class excellence throughout VISHAY worldwide by 2006.

VISHAY Corporate Quality

The VISHAY Corporate Quality defines and implements the VISHAY quality policy at a corporate level. It acts to harmonize the quality systems of the constituent divisions and to implement Total Quality Management throughout the company worldwide.

Vishay Zero Defect Program

- Exceeding quality expectations of our customers
- Commitment from top management through entire organization
- Newest and most effective procedures and tools
  - design, manufacturing and testing
  - management procedures (eg. SPC, TQM)
- Continuous decreasing numbers for AOQ and Failure Rate
- Detailed failure analysis using 8D methodology
- Continuous improvement of quality performance of parts and technology

Quality Goals and Methods

The goals are straightforward: Customer satisfaction through continuous improvement towards zero defects in every area of our operation. We are committed to meet our customers' requirements in terms of quality and service. In order to achieve this, we build excellence into our product from concept to delivery and beyond.

- **Design-in Quality**

Quality must be designed into products. VISHAY uses optimized design rules based on statistical information. This is refined using electrical, thermal and mechanical simulation together with techniques such as FMEA, QFD and DOE.

- **Built-in Quality**

Quality is built into all VISHAY products by using qualified materials, suppliers and processes. Fundamental to this is the use of SPC techniques by both VISHAY and its suppliers. The use of these techniques, as well as tracking critical processes, reduces variability, optimizing the process with respect to the specification. The target is defect prevention and continuous improvement.

- **Qualification**

All new products are qualified before release by submitting them to a series of mechanical, electrical and environmental tests. The same procedure is used for new or changed processes or packages.

- **Monitoring**

A selection of the same or similar tests used for qualification is also used to monitor the short- and long-term reliability of the product.

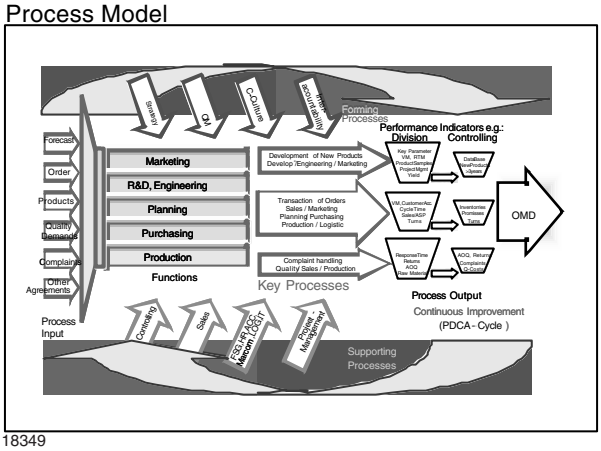
- **SPC (Statistical Process Control)**

SPC is an essential part of all VISHAY process control. It has been established for many years and is used as a tool for the continuous improvement of processes by measuring, controlling and reducing variability.

- **VISHAY Quality System**

All VISHAY's facilities worldwide are approved to ISO 9000. In addition, depending on their activities, some VISHAY companies are approved to recognized international and industry standards such as VDA 6.1 and QS 9000. Each subsidiary goal is to fulfill the particular requirements of customers. The Opto Divisions of Vishay Semiconductor GmbH are certified according to ISO 9001:2000, QS 9000 and VDA 6.1.

Process Model



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The procedures used are based upon these standards and laid down in an approved and controlled Quality Manual.

Total Quality Management

Total Quality Management is a management system combining the resources of all employees, customers and suppliers in order to achieve total customer satisfaction. The fundamental elements of this system are:

- Management commitment
- European Foundation for Quality Management (EFQM assessment methodology)
- Empowered Improvement Teams (EITs)
- Supplier development and partnership
- Quality tools
- Training
- Quality System

All VISHAY employees from the senior management downwards are trained in understanding and use of TQM. Every employee plays a part in the continuous improvement process which is fundamental to TQM and our corporate commitment to exceed customers' expectations in all areas including design, technology, manufacturing, human resources, marketing, and finance. Everyone is involved in fulfilling this goal. The management believes that this can only be achieved by employee empowerment.

The VISHAY corporate core values

- Leadership by example
- Employee empowerment
- Continuous improvement
- Total customer satisfaction
- Business excellence

are the very essence of the VISHAY Quality Movement process.

- **Training**

VISHAY maintains that it can only realize its aims if employees are well trained. It therefore invests heavily in courses to provide all employees with the knowledge they need to facilitate continuous improvement. A training profile has been established for all employees with emphasis being placed on Total Quality Leadership. Our long-term aim is to continuously improve our training so as to keep ahead of projected changes in business and technology.

- **EFQM Assessment Methodology**

VISHAY has the EFQM (European Foundation for Quality Management) methodology for structuring its Total Quality Management approach since 1995. This methodology, similar to the Malcolm Baldrige process, consists in self-assessing the various VISHAY divisions and facilities according to nine business criteria:

- Leadership
- People
- Policy & Strategy
- Partnership & Resources
- Processes
- People Results
- Customer Results
- Society Results
- Key Performance Results

(See figure 3)

The assessments are conducted on a yearly basis by trained and empowered, internal VISHAY assessors. This permits the identification of key improvement projects and the measurement of the progress accomplished.

The EFQM methodology helps VISHAY to achieve world-class business excellence.

- **Empowered Improvement Teams (EITs)**

At VISHAY we believe that every person in the company has a contribution to make in meeting our target of customer satisfaction. Management therefore empowers employees to higher and higher levels of motivation, thus achieving higher levels of effectiveness and productivity. Empowered improvement teams, which are both functional and cross functional, combine the varied talents from across the breadth of the company. By taking part in training, these teams are continually searching for ways to improve their jobs, achieving satisfaction for themselves, the company and most important of all the customer.

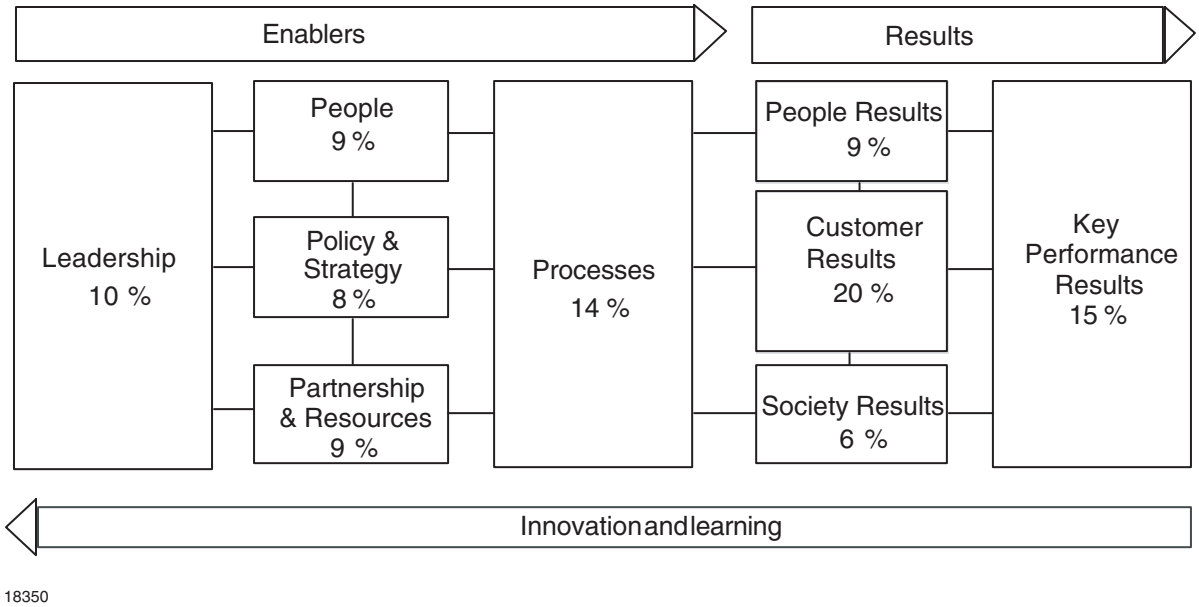

Figure 3. EFQM criteria for self-assessment

TQM Tools

As part of its search for excellence, VISHAY employs many different techniques and tools. The most important of them are:

- **Auditing**

In addition to third party auditing employed for approval by ISO 9000 and customers, VISHAY carries out its own internal and external auditing. There is a common auditing procedure for suppliers and sub-contractors between the VISHAY entities. This procedure is also used for inter-company auditing between the facilities within VISHAY. It is based on the "Continuous Improvement" concept with heavy emphasis on the use of SPC and other statistical tools for the control and reduction of variability.

Internal audits are carried out on a routine basis. They include audits of satellite facilities (i.e., sales offices, warehousing etc.). Audits are also used widely to determine attitudes and expectations both within and outside the company.

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- **Failure Mode and Effect Analysis (FMEA)**

FMEA is a technique for analyzing the possible methods of failure and their effect upon the performance/ reliability of the product/process. Process-FMEAs are performed for all processes. In addition, product FMEAs are performed on all critical or customer products.

- **Design of Experiments (DOE)**

There is a series of tools that may be used for the statistical design of experiments. It consists of a formalized procedure for optimizing and analyzing experiments in a controlled manner. Taguchi and factorial experiment design are included in this. They provide a major advantage in determining the most important input parameters, making the experiment more efficient and promoting common understanding among team members of the methods and principles used.

- **Gauge Repeatability and Reproducibility (GR&R)**

This technique is used to determine equipment's suitability for purpose. It is used to make certain that all equipment is capable of functioning to the required accuracy and repeatability. All new equipment is approved before use by this technique.

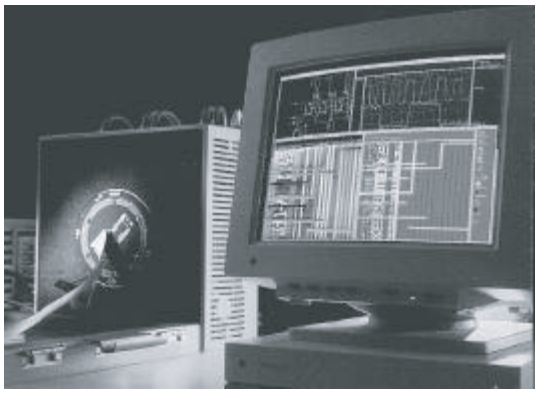
- **Quality Function Deployment (QFD)**

QFD is a method for translating customer requirements into recognizable requirements for VISHAY's marketing, design, research, manufacturing and sales (including after-sales). QFD is a process, which brings together the life cycle of a product from its conception, through design, manufacture, distribution and use until it has served its expected life.

Quality Service

VISHAY believes that quality of service is equally as important as the technical ability of its products to meet their required performance and reliability.

- Our objectives therefore include:
- On-time delivery
- Short response time to customers' requests
- Rapid and informed technical support
- Fast handling of complaints
- A partnership with our customers



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- **Customer Complaints**

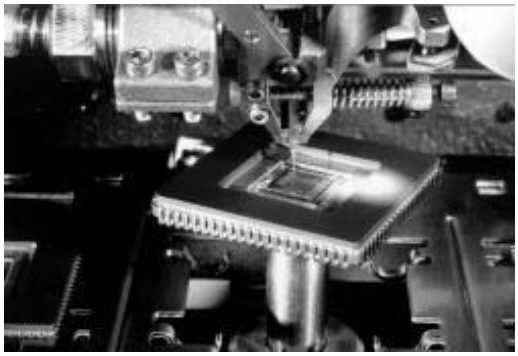
Complaints fall mainly into two categories:

- Logistical
- Technical

VISHAY has a procedure detailing the handling of complaints. Initially complaints are forwarded to the appropriate sales office where in-depth information describing the problem, using the VISHAY **P**roduct **A**nalysis **R**equest and **R**eturn **F**orm (PARRF), is of

considerable help in assists in providing fast response a fast and accurate response. If it is necessary to send back the product for logistical reasons, the Sales Office issues a Returned Material Authorization (RMA) number. On receipt of the goods in good condition, credit is automatically issued. If there is a technical reason for complaint, sample together with the **PARRF** is sent to the Sales Office for forwarding to the Failure Analysis Department of the supplying facility. The device's receipt will be acknowledged and a report issued on completion of the analysis. The cycle time is constantly monitored in order to improve the response time. Failure analysis normally consists of electrical testing, functional testing, mechanical analysis (including X-ray), decapsulation, visual analysis and electrical probing. Other specialized techniques (i.e. LCD, thermal imaging, SEM, acoustic microscopy) may be used if necessary.

If the analysis uncovers a quality problem, Corrective Action Report (CAR) in 8D format will be issued. Any subsequent returns are handled through the RMA procedure.



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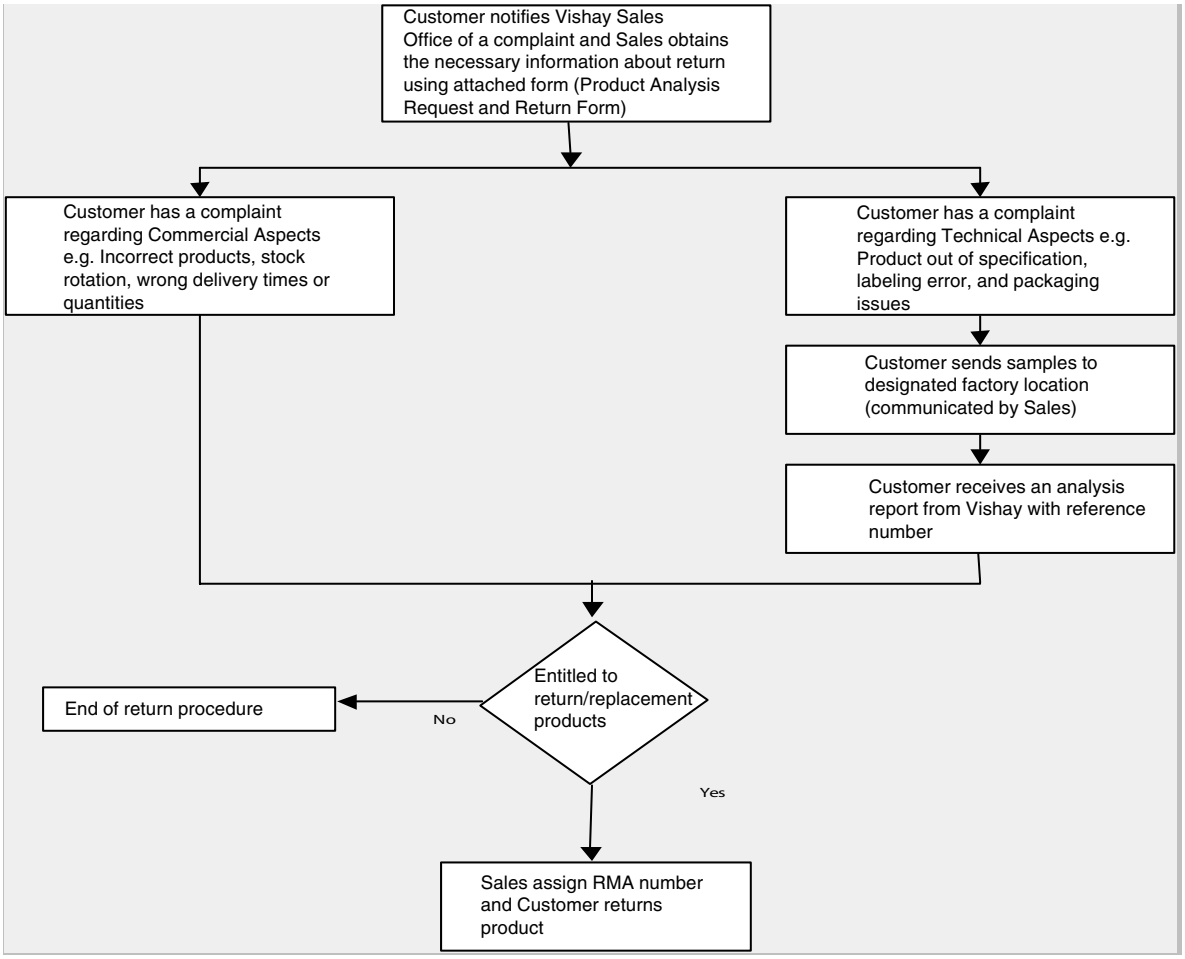

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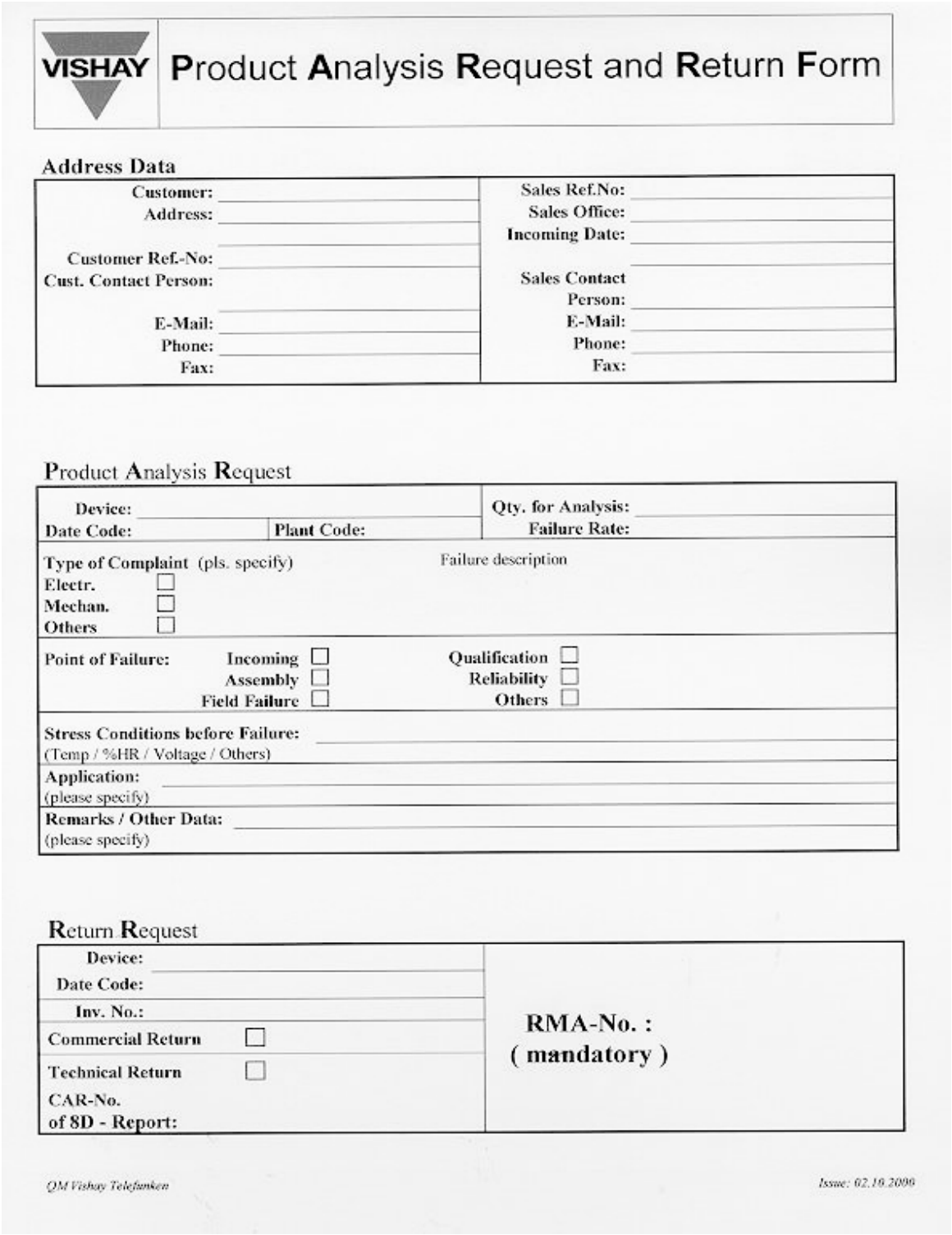
Complaint and Return Procedure



VISHAY Product Analysis Request and Return Form

Address Data

Customer:	Sales Ref.No:
Address:	Sales Office:
	Incoming Date:
Customer Ref.-No:	
Cust. Contact Person:	Sales Contact Person:
E-Mail:	E-Mail:
Phone:	Phone:
Fax:	Fax:

Product Analysis Request

Device:	Qty. for Analysis:
Date Code: / Plant Code:	Failure Rate:
Type of Complaint (pls. specify) / Failure description	
Electr. ☐	
Mechan. ☐	
Others ☐	
Point of Failure: Incoming ☐ Assembly ☐ Field Failure ☐	Qualification ☐ Reliability ☐ Others ☐
Stress Conditions before Failure: (Temp / %HR / Voltage / Others)	
Application: (please specify)	
Remarks / Other Data: (please specify)	

Return Request

Device:	RMA-No. : (mandatory)
Date Code:	
Inv. No.:	
Commercial Return ☐	
Technical Return ☐	
CAR-No. of 8D - Report:	

QM Vishay Telefunken Issue: 02.10.2000

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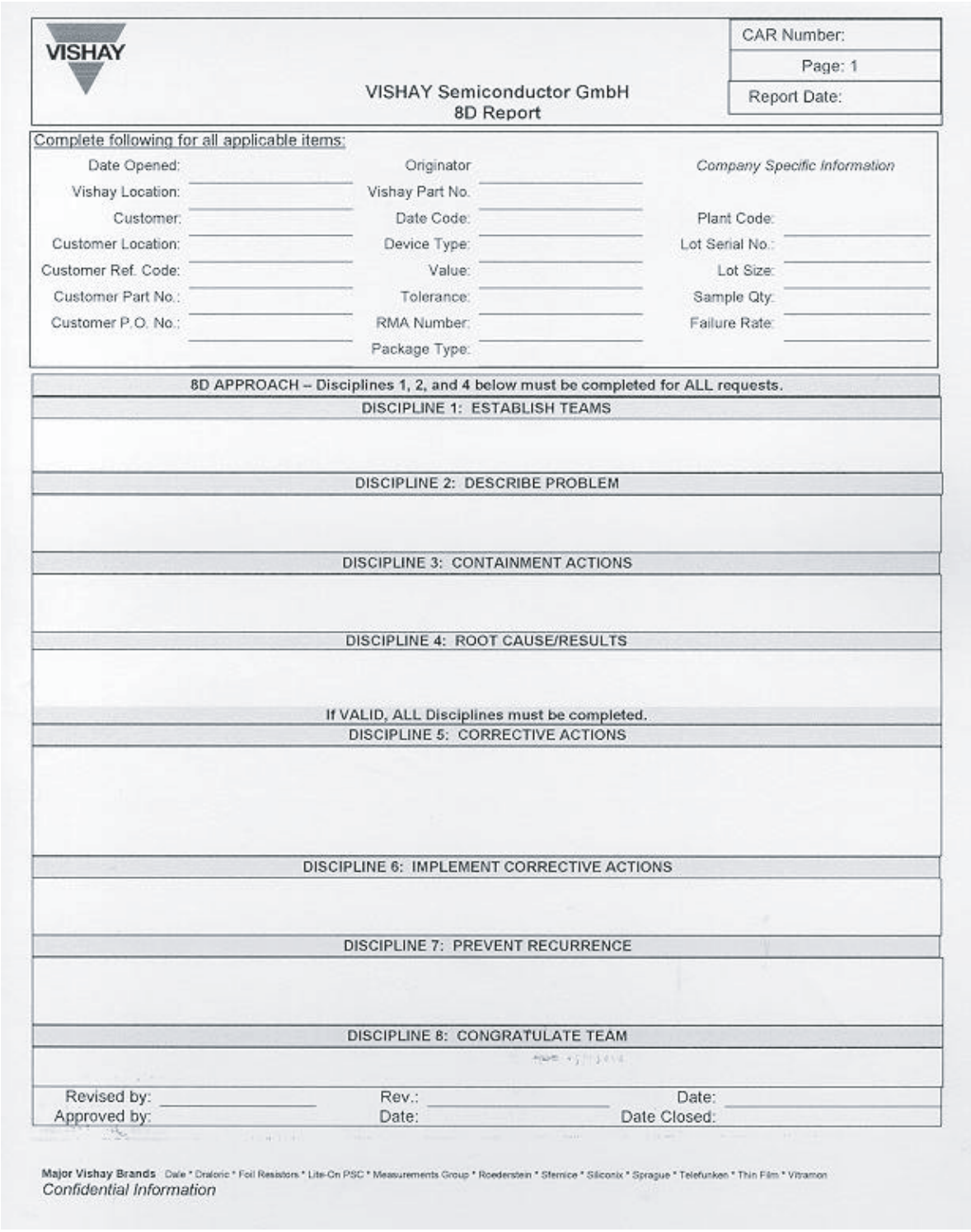
Product **A**nalysis **R**equest and **R**eturn **F**orm (PARRF)



VISHAY

VISHAY Semiconductor GmbH
8D Report

CAR Number:
Page: 1
Report Date:

Complete following for all applicable items:

Date Opened:		Originator		*Company Specific Information*	
Vishay Location:		Vishay Part No.			
Customer:		Date Code:		Plant Code:	
Customer Location:		Device Type:		Lot Serial No.:	
Customer Ref. Code:		Value:		Lot Size:	
Customer Part No.:		Tolerance:		Sample Qty:	
Customer P.O. No.:		RMA Number:		Failure Rate:	
		Package Type:			

8D APPROACH – Disciplines 1, 2, and 4 below must be completed for ALL requests.

DISCIPLINE 1: ESTABLISH TEAMS

DISCIPLINE 2: DESCRIBE PROBLEM

DISCIPLINE 3: CONTAINMENT ACTIONS

DISCIPLINE 4: ROOT CAUSE/RESULTS

If VALID, ALL Disciplines must be completed.

DISCIPLINE 5: CORRECTIVE ACTIONS

DISCIPLINE 6: IMPLEMENT CORRECTIVE ACTIONS

DISCIPLINE 7: PREVENT RECURRENCE

DISCIPLINE 8: CONGRATULATE TEAM

Revised by: _____ Rev.: _____ Date: _____
Approved by: Date: Date Closed:

Major Vishay Brands Dale * Draloric * Foil Resistors * Lite-On PSC * Measurements Group * Roederstein * Sfernice * Siliconix * Sprague * Telefunken * Thin Film * Vitramon
Confidential Information

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VISHAY 8D form

- **Change Notification**

All product and process changes are controlled and released via ECN (Engineering Change Notification). This requires the approval of the relevant departments. In the case of a major change, the change is forwarded to customers via Sales/ Marketing before implementation. Where specific agreements are in place, the change will not be implemented unless approved by the customer.

- **Ship-to-Stock/Ship-to-Line (STS/STL)**

Many customers now require devices to be shipped direct to stock or to the production line by omitting any internal inspection. VISHAY welcomes such agreements as part of its customer partnership program, which promises an open approach in every aspect of its business. A product will only be supplied as STS or STL if there is a valid agreement in place between the two companies. Such an agreement details the quality level targets agreed upon between the companies and the methods to be used in case of problems.

Quality and Reliability

Assurance Program

Though both quality and reliability are designed into all VISHAY products, three basic programs must assure them:

- Average Outgoing Quality (AOQ) –
  100 % testing is followed by sample testing to measure the defect level of the shipped product. This defect level (AOQ) is measured in ppm (parts per million).
- Reliability qualification program –
  to assure that the design, process or change is reliable.
- Reliability monitoring program –
  to measure and assure that there is no decrease in the reliability of the product.

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AOQ Program

Before leaving the factory, all products are sampled after 100% testing to ensure that they meet a minimum quality level and to measure the level of defects. The results are accumulated and expressed in ppm (parts per million). They are the measure of the average number of potentially failed parts in deliveries over a period of time. The sample size used is determined by AQL or LTPD tables depending upon the product. No rejects are allowed in the sample.

The AOQ value is calculated monthly using the method defined in standard JEDEC 16:

$$AOQ = p \cdot LAR \cdot 10^6 (ppm)$$

where:

$$p = \frac{\text{number of devices rejected}}{\text{total number of devices tested}}$$

LAR = lot acceptance rate:

$$LAR = 1 - \frac{\text{number of lots rejected}}{\text{total number of lots tested}}$$

The AOQ values are recorded separately with regard to electrical and mechanical (visual) rejects by product type and package.

The actual qualification procedure depends on which of these (or combinations of these) are to be qualified. Normally there are three categories of qualification in order of degree of qualification and testing required:

- New technology or process (this includes a new design on a new process)
- New product or re-designed product using a qualified process

New package including piece-part or material change
New manufacturing location

- Minor change of process, assembly or package

Accelerated testing is normally used in order to produce results fast. The stress level employed depends upon the failure mode investigated. The stress test is set so that the level used gives the maximum acceleration without introducing any new or untypical failure mode.

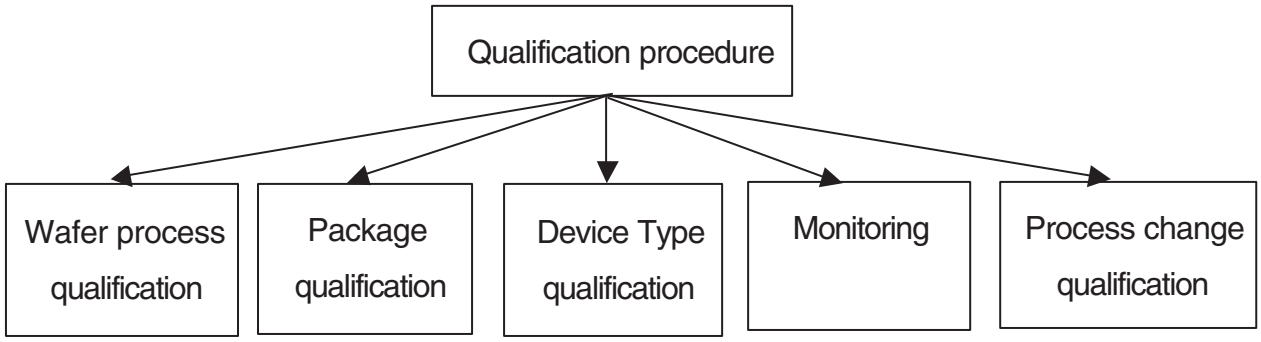
The tests used consist of a set of the following:

- High temperature life test (static)
- High temperature life test (dynamic)
- HTRB (High Temperature Reverse Bias)
- Humidity 85/85 (with or without bias)
- HAST (Highly Accelerated Stress Test)
- Temperature cycling
- High-temperature storage
- Low-temperature storage
- Marking permanency
- Lead integrity
- Solderability
- Resistance to solder heat
- Mechanical shock (not plastic packages)
- Vibration (not plastic packages)
- ESD characterization

SMD devices only are subjected to preconditioning to simulate board assembly techniques using the methods defined in standard JSTD 020A before being subjected to stresses.

Normally, the endpoint tests are related to the data sheet or to specified parameters. Additionally, they may include:

- Destructive physical analysis
- X-ray
- Delamination testing using scanning acoustic microscope
- Thermal imaging
- Thermal and electrical resistance analysis



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Example of the QualPack

Reliability Monitoring & Wear Out

The monitoring program consists of short-term monitoring to provide fast feedback on a regular basis in case of a reduction in reliability and to measure the Early-life Failure Rate (EFR). At the same time, Long-term monitoring is used to determinate the Long-term steady-state Failure Rate (LFR). The tests used are a subset from those used for qualification and consist of:

- Life tests
- Humidity tests
- Temperature-cycling tests
- Solderability tests
- Resistance-to-solder-heat test

The actual tests used depend on the product tested.

Depending on the assembly volume a yearly monitoring and wear out test plan is created.

Wear Out data are very important in Opto electronic device. Out of that data degradation curves can be made. These curves show the long time behavior of the different devices.

Some typical curves are attached in this report.

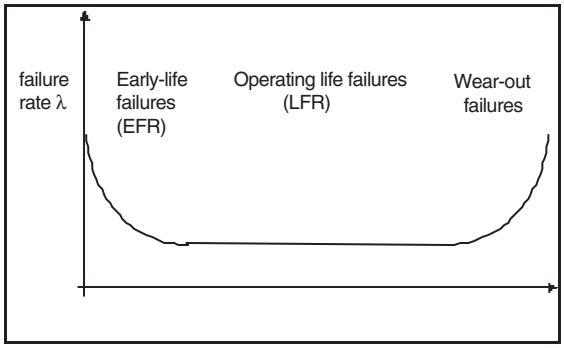

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Figure 4. Bathtub curve

Reliability Principles

Reliability is the probability of survival as a function of time and stress, and is usually expressed in terms of FITs (failures in 10 to 9th power device hours). It is expressed as:

$$F(t) + R(t) = 1 \quad \text{or} \quad R(t) = 1 - F(t)$$

where:

R(t) = probability of survival

F(t) = probability of failure

$F(t) = 1\text{-}e^{-\lambda t}$

where

λ = instantaneous failure rate

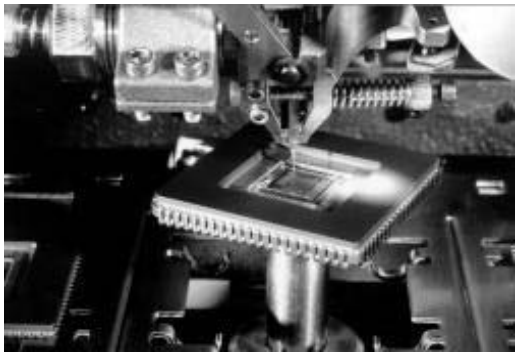
t = time

thus,

$$R(t) = e^{-\lambda t}$$

The lifetime distribution or hazard rate curve is shown on figure 4. This curve is also known as the 'bath-tub curve' because of its shape. There are three basic sections:

- Early-life failures (infant mortality)
- Operating-life failures (random failures)
- Wear-out failures



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The failure rate (l) during the constant (random) failure period is determined from life-test data. The failure rate is calculated from the formula:

$$\lambda = \frac{r}{\Sigma(Fi \cdot ti) + (N \cdot t)} = \frac{r}{C}$$

where

λ = failure rate (hours^{-1})
r = number of observed failures
f_i = failure number
t_i = time to defect
N = good sample size
t = entire operating time
C = number of Components X hours

The result is expressed in either

a) % per 1000 component hours by multiplying by 10^5

or in

b) FITs by multiplying by 10^9 (1 FIT = 10^{-9} hours $^{-1}$)

Example 1: Determination of failure rate λ 500 devices were operated over a period of 2000 hours (t) with:
1 failure (f1) after 1000 hours (t1) and
1 failure (f2) after 1500 hours (t2).
The failure rate of the given example can be calculated as follows:

$$\lambda = \frac{2}{(1 \cdot 1000h) + (1 \cdot 1500h) + (498 \cdot 2000h)}$$

$$\lambda = 2 \cdot 10^{-6} \text{hours}^{-1}$$

That means that this sample has an average failure rate of **0.2 %/1000 hours or 2000 FIT**

Observed failure rates as measured above are for the specific lot of devices tested. If the predicted failure rate for the total population is required, statistical confidence factors have to be applied.

The confidence factors can be obtained from "chi square" (χ^2) charts. Normally, these charts show the value of (χ^2/2) rather than χ^2. The failure rate is calculated by dividing the χ^2/2 factor by the number of component hours.

$$\lambda_{pop} = \frac{(\chi^2/2)}{C}$$

The values for χ^2/2 are given in table 1

Number of Failures	Confidence Level	
	60 %	90 %
0	0.92	2.31
1	2.02	3.89
2	3.08	5.30
3	4.17	6.70
4	5.24	8.00
5	6.25	9.25
6	7.27	10.55

Table 1: χ^2/2 chart

Example 2: The failure rate of the population
Using example 1 with a failure rate of 2000 FIT and 2 failures:
χ^2/2 at 60 % confidence is 3.08

$$\lambda_{pop} = \frac{3.08}{9.985 \cdot 10^5} = 3085 \text{ FIT}$$

This means that the failure rate of the population will not exceed 3085 FIT with a probability of 60 %

- **Accelerated Stress Testing**

In order to be able to assure long operating life with a reasonable confidence, VISHAY carries out accelerated testing on all its products. The normal accelerating factor is the temperature of operation. Most failure mechanisms of semiconductors are dependent upon temperature. This temperature dependence is best described by the Arrhenius equation.

$$\lambda_{T2} = \lambda_{T1} \times e^{\left[\frac{E_A}{k} \times \left(\frac{1}{T1} - \frac{1}{T2}\right)\right]}$$

where

k = Boltzmann's constant 8.63 x 10^{-5} eV/K
E_A = Activation energy (eV)
T_1 = Operation temperature (K)
T_2 = Stress temperature (K)
λ_{T1} = Operation failure rate
λ_{T2} = Stress-test failure rate

Using this equation, it is possible from the stress test results to predict what would happen in use at the normal temperature of operation.

- **Activation Energy**

Provided the stress testing does not introduce a failure mode, which would not occur in practice, this method gives an acceptable method for predicting reliability using short test periods compared to the life of the device. It is necessary to know the activation energy of the failure mode occurring during the accelerated testing. This can be determined by experi-

ment. In practice, it is unusual to find a failure or if there is, it is a random failure mode. For this reason an average activation energy is normally used for this calculation. Though activation energies can vary between 0.3 and 2.2 eV, under the conditions of use, activation energies of between 0.6 and 0.9 eV are used depending upon the technology.

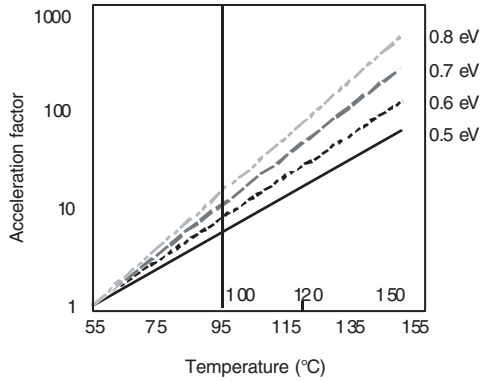

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Figure 5. Acceleration factor for different activation energies normalized to T = 55 °C

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Activation Energies for common failure mechanisms

The activation energies for some of the major semiconductor failure mechanisms are given in the table below. These are estimates taken from published literature.

Failure mechanism	Activation Energy
Mechanical wire shorts	0.3 – 0.4
Diffusion and bulk defects	0.3 – 0.4
Oxide defects	0.3 – 0.4
Top-to-bottom metal short	0.5
Electro migration	0.4 – 1.2
Electrolytic corrosion	0.8 – 1.0
Gold-aluminum intermetallics	0.8 – 2.0
Gold-aluminum bond degradation	1.0 – 2.2
Ionic contamination	1.02
Alloy pitting	1.77

Table 2: Activation energies for common failure mechanism

Failure rates are quoted at an operating temperature of 55 °C and 60 % confidence using an activation energy (E_A) of 0.8 eV for optoelectronic devices.

Example 3: Conversion to 55 °C

In Example 2, the life test was out at 150 °C so to transform to an operating temperature of 55 °C.

T1 = 273 + 55 = 328K

T1 = 273 + 150 = 423K

Acceleration factor =

$$\frac{\lambda_{(T2)}}{\lambda_{(T1)}} = \frac{\lambda_{(423K)}}{\lambda_{(328K)}} = 258$$

$$\lambda_{(328K)} = \frac{\lambda_{(423K)}}{258} = \frac{3080}{258}$$

= 12 FIT

(at 55 °C with a confidence of 60 %)

This figure can be re-calculated for any operating/junction temperature using this method.

- EFR (Early Life Failure Rate)

This is defined as the proportion of failures, which will occur during the warranty period of the system for which they were designed. In order to standardize this period, VISHAY uses 1000 operation hours as the reference period. This is the figure also used by the automotive industry; it equates to one year in the life of an automobile. In order to estimate this figure, VISHAY normally operates a sample of devices for 48 or 168 hours under the accelerated conditions detailed above. The Arrhenius law is then used as before to calculate the failure rate at 55 °C with a con-

fidence level of 60 %. This figure is multiplied by 1000 to give the failures in 1000 hours and by 10^6 to give a failure in ppm. All EFR figures are quoted in ppm (parts per million).

- **Climatic Tests Models**

Temperature cycling failure rate The inverse power law is used to model fatigue failures of materials that are subjected to thermal cycling. For the purpose of accelerated testing, this model relationship is called Coffin-Manson relationship, and can be expressed as follows:

$$A_F = \left(\frac{\Delta T_{stress}}{\Delta T_{use}}\right)^M$$

where:

A_F = Acceleration factor
DT_{use} = temp. range under normal operation
DT_{stress} = temp. range under stress operation
M = constant characteristic of the failure mechanism.

Failure mechanism	Coffin–Manson exponent M
Al wire bond failure	3.5
Intermetallic bond fracture	4.0
Au wire bond heel crack	5.1
Chip-out bond failure	7.1

Table 3: Coffin - Manson exponent M

For instance:

ΔT_{use} = 15 °C/ 60 °C= 45 °C

ΔT_{stress} = –25 °C/ 60 °C= 125 °C

$$A_F = \left(\frac{125\ °C}{45\ °C}\right)^3 \approx 21$$

Relative Humidity failure rate

Moisture effect modeling is based upon the Howard-Pecht-Peck model using the acceleration factor of the equation shown below:

$$A_F = \left(\frac{RH_{stress}}{RH_{use}}\right)^C \cdot e^{\left[\frac{E_A}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]}$$

where:

RH_{stress} = relative humidity during test
RH_{use} = relative humidity during operation
T_{stress} = temperature during test
T_{use} = temperature during operation
E_A = activation energy
k = Boltzmann constant
C = Material constant

For instance:

RH_{stress} = 85 % RH_{use} = 92 %
T_{stress} = 358 K T_{use} = 313 K

$$A_F = \left(\frac{85\ \%\ RH}{92\ \%\ RH}\right)^3 \cdot e^{\left[\frac{0,8}{8,617\ Þ\ 10^{-5}}\left(\frac{1}{313} - \frac{1}{358}\right)\right]}$$

$$A_F \approx 33$$

This example shows how to transform test conditions into environmental or into another test conditions. This equation is applicable for devices subjected to temperature humidity bias (THB) testing.

Using these acceleration factors the useful lifetime can be calculated. Applying the acceleration factor once more, useful lifetime for the moisture effect

model for parts subjected to THB can be estimated by the following equation:

$$\text{Useful life}_{\text{Years}} = \frac{A_F \cdot \text{test hours}}{\text{hours per year}}$$

with:

Test hours = 1000

hours per year = 8760

$A_F \approx 118$ (40 °C / 60 % RH)

$$\text{Useful life}_{\text{Years}} = \frac{118 \cdot 1000}{8760} \approx 13{,}5 \text{ years}$$

This means that operation in 40 °C / 60 % RH environment is good for around 13 years, calculated out of the 85 °C/ 85 % RH 1000h humidity stress test.

18370

Wafer Level Reliability Testing

Due to the increasing demand for complex devices with reduced geometry, VISHAY is committed to enhancing and improving process and product quality through the use of Wafer Level Testing (WLT). Through the use of custom-designed and standard test devices and structures, the on-going design as well as the process quality and reliability are monitored both at the wafer and package level. When implemented in the manufacturing process, they provide a rapid means of monitoring metal integrity and parameter stability.

The main tests are:

- Electro-migration

Commonly known as SWEAT (Standard Wafer- Level Electro-migration Test), this test is used as a metallization process quality monitor.

- Mobile ion instability

Special sensitive transistors are used together with built-in heaters to measure the effect of the movement of mobile ions at the interface region.

Handling for Quality

- **Electrostatic Discharge (ESD) Precautions**

Electrostatic discharge is defined as the high voltage, which is generated when two dissimilar materials move in contact with one another. This may be by rubbing (i.e. walking on a carpet) or by hot air or gas passing over an insulated object. Sometimes, ESD is easily detectable as when a person is discharged to ground (shock).

Electronic devices may be irreversibly damaged when subjected to this discharge. They can also be damaged if they are charged to a high voltage and then discharged to ground.

Damage due to ESD may occur at any point in the process of manufacture and use of the device. ESD is a particular problem if the humidity is low (< 40 %) which is very common in non-humidified but air-conditioned buildings. ESD is not just generated by the human body but can also occur with un-grounded machinery.

ESD may cause a device to fail immediately or damage a device so that it will fail later. Whether this happens or not, usually depends on the energy available in the ESD pulse.

All ESD-sensitive VISHAY products are protected by means of

- Protection structures on chip
- ESD protection measures during handling and shipping

VISHAY has defined procedures, which detail the methods to be used for protection against ESD. These measures meet or exceed those of CECC

00015 or MIL-STD-1686, the standards for ESD-protective and preventative measures.

These include the use of:

- Grounded wrist straps
- Grounded benches
- Conductive floors
- Protective clothing
- Controlled humidity

It also defined the methods for routinely checking these and other items such as the grounded of machines.

A semiconductor device is only completely protected when enclosed in a «Faraday Cage». This is a completely closed conductive container (i.e., sealed conductive bag or box).

Most packaging material (i.e. tubes) used for semiconductors is now manufactured from antistatic material or anti-static-coated material. This does not mean that the devices are completely protected from ESD, only that the packing will not generate ESD. Devices are completely protected only when surrounded on all sides by a conductive package.

It should also be remembered that devices can equally as easily be damaged by discharge from a high voltage to ground as vice-versa.

Testing for ESD resistance is part of the qualification procedure. The methods used are detailed in MIL-STD-883 Method 3015.7 (Human Body Model) and EOS/ESD-S5.1-1993 (Machine Model) specification.

- **Latch-up**

The latch-up effect is a state in which a low impedance path results and persists following an input, output or the latch-up effect is a state in which a low impedance path supply over voltage that triggers a parasitic Thyristor.

Due to this effect an over current occurs in the IC, which can destroy the IC. At least the supply voltage of the IC must be cut off to get back the IC in a defined state.

Normally, the latch-up test is carried out on CMOS ICs. This CMOS latch-up test is according to the JEDEC 17 standard. For Bipolar ICs, there is no standard available so far.

- **Soldering**

All products are tested to ascertain their ability to withstand the industry standard soldering conditions after storage. In general, these conditions are as follows.

- Hand soldering: 260 °C, 2 mm from the device body for 10 s.
- Wave soldering: Double-wave soldering according to CECC 00802 maximum 2 x total restricted to 3 soldering operations
- Reflow soldering: convection soldering according to CECC 00802 with a maximum temperature of 260 °C, maximum 2 x with the total restricted to 3 soldering operations, IR soldering to CECC 00802 with a maximum temperature of 245 °C maximum 2 x with the total restricted to 3 soldering operations

Note: certain components may have limitations

due to their construction.

- **Dry pack**

When being stored, certain types of device packages can absorb moisture, which is released during the soldering operations, thus causing damage to the device. The so-called «popcorn» effect is such an example. To prevent this, Surface Mount Devices (SMD) are evaluated during qualification, using a test consisting of moisture followed by soldering simulation (pre-conditioning) and then subjected to various stress tests. The MSL for optocouplers is 1. In table Number 3 - Moisture Sensitivity Levels – the six different levels, the floor life conditions as well as the soak requirements belonging to these levels are described. Any device, which is found to deteriorate under these conditions, is packaged in «dry pack».

The dry-packed devices are packed generally according to EIA-583 «Packaging Material Standards for Moisture Sensitive Items», IPC-SM-786 «Recommended Procedures for Handling of Moisture Sensitive Plastic IC Packages».

The following are general recommendations:

- Shelf life in the packaging at < 40 °C and 90 % RH is 12 months.
- After opening, the devices should be handled according to the specifications mentioned on the dry-pack label.
- If the exposure or storage time is exceeded, the devices should be baked:
- Low-temperature baking - 192 hours at 40 °C and 5 % RH
- High-temperature backing - 24 hours at 125 °C.

	Floor	Life	Soak Requirements			
Level	Conditions	Time	Time (hours)			Conditions
1	≤ 30 °C / 90 % RH	Unlimited	168			85 °C / 85 % RH
2	≤ 30 °C / 60 % RH	1 year	168			85 °C / 60 % RH
2a	≤ 30 °C / 60 % RH	4 Weeks	696			30 °C / 60 % RH
			X	Y	Z	
3	≤ 30 °C / 60 % RH	168 h.	24	168	192	30 °C / 60 % RH
4	≤ 30 °C / 60 % RH	72 h.	24	72	96	30 °C /
5	≤ 30 °C / 60 % RH	24 / 48 h.	24	24 / 48	48 / 72	30 °C / 60 % RH
6	≤ 30 °C / 60 % RH	6 h.	0	6	6	30 °C / 60 % RH

Table 4: Moisture Sensitivity Levels

X = Default value of semiconductor manufacturer's exposure time (MET) between bake and bag plus the maximum time allowed out of the bag at the distributor's facility. The actual times may be used rather than the default times, but they must be used if they exceed the default times.

Y = Floor life of package after it is removed from dry pack bag (level 8 after completion of bake).

Z = Total soak time for evaluation (X + Y).

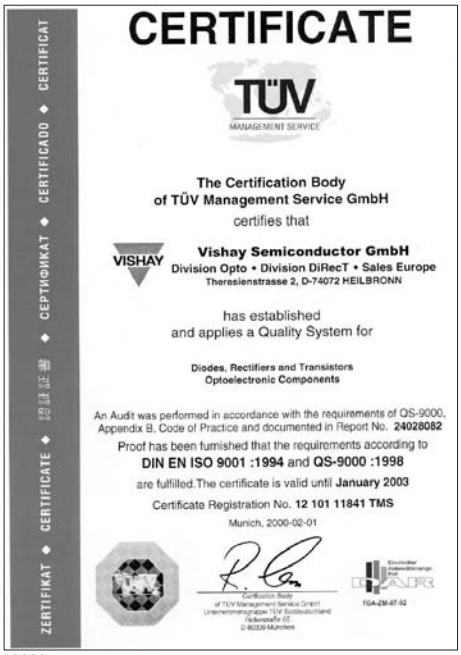
Note: There are two possible floor lives and soak times in Level 5. The correct floor life will be determined by the manufacturer and will be noted on the dry pack bag label per JEP 113.«Symbol and Labels for Moisture Sensitive Devices».

Environmental and Quality System Certificates

Overview

Location	ISO 900x ff	QS 9000	VDA 6.1	ISO 14001
Vishay Semiconductor GmbH Heilbronn, Germany	X	X	X	X
Vishay Semiconductor Ges.m.b.H. Vöcklabruck, Austria	X	X	X	X
Shanghai Vishay Semiconductor Shanghai, China	X	X	X	X
Vishay Hungary Electronic Co. Ltd Budapest, Hungary [1)]	X	X	X	X
Vishay Hungary Electronic Co. Ltd Gyöngyös, Hungary [1)]	X	X	X	X
Vishay (Phils.) Inc. Manila, Philippines	X	X	X	X
Vishay Semiconductor SDN. BHD. Krubong, Malaysia	X	X		X

[1)] ISO / TS16946 certified



CERTIFICATE

TÜV MANAGEMENT SERVICE

The Certification Body
of TÜV Management Service GmbH
certifies that

VISHAY **Vishay Semiconductor GmbH**
Division Opto • Division DiRecT • Sales Europe
Theresienstrasse 2, D-74072 HEILBRONN

has established
and applies a Quality System for

Diodes, Rectifiers and Transistors
Optoelectronic Components

An Audit was performed in accordance with the requirements of QS-9000, Appendix B, Code of Practice and documented in Report No. **24028082**
Proof has been furnished that the requirements according to
DIN EN ISO 9001 :1994 and **QS-9000 :1998**
are fulfilled. The certificate is valid until **January 2003**
Certificate Registration No. **12 101 11841 TMS**
Munich, 2000-02-01

ZERTIFIKAT ◆ CERTIFICATE ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

18389

CERTIFICATE

TÜV MANAGEMENT SERVICE

The Certification Body
of TÜV Management Service GmbH
certifies that

VISHAY (PHILS.) INC.
BAGSAKAN ROAD, FTI ESTATE,
1630 TAGUIG, METRO MANILA,
PHILIPPINES

has established
and applies a Quality System for

MANUFACTURING OF
OPTOELECTRONIC SEMICONDUCTORS

An audit was performed in accordance with the requirements of QS-9000, Appendix B „Code of Practice" and documented in Report No. **70012320.**
Above mentioned company has been registered to
QS-9000 :1998
(Based on and including DIN EN ISO 9001 :1994)
The certificate is valid until **December 2005**
Certificate Registration No. **12 101 11237 TMS**
Munich, 2002-12-13

ZERTIFIKAT ◆ CERTIFICATE ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

18391

TÜV CERT

CERTIFICATE

The TÜV CERT Certification Body
of TÜV Anlagentechnik GmbH
Unternehmensgruppe TÜV Rheinland/Berlin-Brandenburg
certifies in accordance with
TÜV CERT procedures that

VISHAY Shanghai Vishay Semiconductor Co., Ltd.
Shanghai Vishay Semiconductor Opto Co., Ltd.
501 West Jiang Chang Road, Shanghai 200436, P.R. China

has established and applies a quality system for

Manufacturing of Diodes, Opto Couplers,
LED´s and IR-Emitters

An audit was performed in accordance with the requirements of QS-9000, Appendix B, Code of Practice and documented in Report No. **99463**
Proof has been furnished that the requirements according to
DIN EN ISO 9002:1994 and **QS-9000:1998**
are fulfilled.
The certificate is valid until **April 2003**
Certificate Registration No. **09 101 99463**

TÜV Rheinland/Berlin-Brandenburg TÜV

18390

AIB-VINÇOTTE International Ltd.
Brussels, Belgium

Quality Management System Certificate

ISO/TS 16949 : 2002
Particular requirements for the application of
ISO 9001 : 2000
for automotive production and relevant service part organization

This is to certify that ***VISHAY HUNGARY ELEKTRONIKAI Kft***
Opto Division Group

located at ***Fóti út 56***
1047 BUDAPEST (HUNGARY)

has established and is maintaining a Quality Management System which is in accordance with the requirements of ISO/TS 16949 : 2002 and having been audited in accordance with the "Rules for the registration scheme for ISO/TS 16949 : 2002 – First edition" for :

Production of optosensors, Chip on Board and packaged optoelectronic devices

This Certificate is based on the result of an audit documented in report no. ***REP-2-C-080A, 081A/TS.***
This Certificate is granted subject to AIB-VINÇOTTE International's General Regulations on Management Systems Certification.

In appendix (page 2/2): *- list of customer specific requirements*

Certificate number : ***00 1451a***
Date of issue : ***December 9, 2002***
This certificate expires on : ***December 8, 2005***
Signed for the certification body :

Ir. P. OLIVIER
Chairman Certification Committee

AV AIB-VINÇOTTE INTERNATIONAL IQNet

18392

TÜV Rheinland/
Berlin-Brandenburg

TÜV

CERTIFICATE

The Certification Body for Environmental Management Systems
of TÜV Anlagentechnik GmbH
hereby certifies that the enterprise

Shanghai Vishay Semiconductor Opto Co., Ltd.
Shanghai Vishay Semiconductor Co., Ltd.
501 West Jiangchang Road, Shanghai 200436, P. R. China

has established and applies an environmental management system for

Manufacturing of Diodes, Optocoupler, LED and IR-Emitter

The audit was performed,
Report No. **000495**
Proof has been furnished, that the requirements according to
ISO 14001
(edition 1996) are fulfilled.
The certificate is valid until **2004 January**
Certification Registration No. **01 104 000495**

Andreas Gehrmann

Cologne, 2001-01-05
Certification Body for Environmental Management Systems
TÜV Anlagentechnik GmbH

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CERTIFICATE

ZERTIFIKAT ◆ CERTIFICATE ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

TÜV
MANAGEMENT SERVICE

The Certification Body
of TÜV Management Service GmbH
certifies that

Vishay (Phils.), Inc.
Bagsakan Road, FTI Estate,
1630 Taguig, Metro Manila, Philippines

has established and applies an
Environmental Management System for

Manufacturing of OPTOELECTRONIC SEMICONDUCTORS

An Audit was performed, Report No. **24029217**
Proof has been furnished that the requirements according to
DIN EN ISO 14001 :1996
are fulfilled. The certificate is valid until **May 2003**
Certificate Registration No. **12 104 12294 TMS**
Munich, 2000-05-11

18395

ZERTIFIKAT

ZERTIFIKAT ◆ CERTIFICATE ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

TÜV
MANAGEMENT SERVICE

Die Zertifizierungsstelle
der TÜV Management Service GmbH
bescheinigt,
dass das Unternehmen

VISHAY

Vishay Semiconductor GmbH
Division Opto • Division DiRecT • Sales Europe
Theresienstrasse 2, D-74072 HEILBRONN

für den Geltungsbereich

Dioden, Rectifier und Transistoren
Optoelektronischen Bauteile

ein Umweltmanagementsystem eingeführt hat
und anwendet.

Durch ein Audit, Bericht-Nr. **70007368**
wurde der Nachweis erbracht, dass die Forderungen der
DIN EN ISO 14001:1996
erfüllt sind. Dieses Zertifikat ist gültig bis **Dezember 2004**
Zertifikat-Registrier-Nr. **70104105**
Mannheim, 28. Januar 2002

18394

VDA

TÜV
MANAGEMENT SERVICE

SUPPLEMENT TO CERTIFICATE

The TÜV Management Service GmbH
VERBAND DER AUTOMOBILINDUSTRIE E.V. / VDA / CERT. No. 10/97
certifies
that the company

VISHAY

Vishay Semiconductor GmbH
Division Opto • Division DiRecT • Sales Europe
Theresienstrasse 2, D-74072 HEILBRONN

Site: D-74072 HEILBRONN

Diodes, Rectifiers and Transistors
Optoelectronic Components
incl. product development

applies a
Quality system according to VDA 6, Part 1
- material products -

This supplement to certificate is only valid in conjunction with the ISO 9001 certificate
Registration No. 12 101 11841 TMS.
It confirms that the quality system is additionally qualified to the ISO 9001 standard
by fulfilling the VDA 6, Part 1 requirements.
Evidence was present as a part of the certification audit, report no. 24028082.
This certificate is valid until: January 2003
Munich, February 01, 2000

Certification Body
of TÜV Management Service GmbH
Unternehmensgruppe TÜV Süddeutschland
Ridlerstraße 65
D-80339 München

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Reliability & Statistics Glossary

Definitions

Accelerated Life Test: A life test under conditions those are more severe than usual operating conditions. It is helpful, but not necessary, that a relationship between test severity and the probability distribution of life be ascertainable.

Acceleration Factor: Notation: f(t) = the time transformation from more severe test conditions to the usual conditions. The acceleration factor is f(t)/t. The differential acceleration factor is df(t)/dt.

Acceptance number: The largest numbers of defects that can occur in an acceptance sampling plan and still have the lot accepted.

Acceptance Sampling Plan: An accept/reject test the purpose of which is to accept or reject a lot of items or material based on random samples from the lot.

Assessment: A critical appraisal including qualitative judgements about an item, such as importance of analysis results, design criticality, and failure effect.

Attribute (Inspection By): A term used to designate a method of measurement whereby units are examined by noting the presence (or absence) of some characteristic or attribute in each of the units in the group under consideration and by counting how many units do (or do not) possess it. Inspection by attributes can be two kinds: either the unit of product is classified simply as defective or no defective or the number of defects in the unit of product is counted with respect to a given requirement or set of requirements.

Attribute Testing: Testing to evaluate whether or not an item possesses a specified attribute.

Auger Electron Spectrometer: An instrument, which identifies elements on the surface of a sample. It excites the area of interest with an electron beam and observes the resultant emitted Auger electrons.

These electrons have the specific characteristics of the near surface elements. It is usually used to identify very thin films, often surface contaminants.

Availability (Operational Readiness): The probability that at any point in time the system is either operating satisfactorily or ready to be placed in operation on demand when used under stated conditions.

Average Outgoing Quality (AOQ): The average quality of outgoing product after 100 % inspection of rejected lot, with replacement by good units of all defective units found in in- spection.

Bathtub Curve: A plot of failure rate of an item (whether repairable or not) vs. time. The failure rate initially decreases, then stays reasonably constant, then begins to rise rather rapidly. It has the shape of bathtub. Not all items have this behaviour.

Bias: (1) The difference between the s-expected value of an estimator and the value of the true parameter; (2) Applied voltage.

Burn-in: The initial operation of an item to stabilize its characteristics and to minimize infant mortality in the field.

Confidence Interval: The interval within which it is asserted that the parameters of a probability distribution lies.

Confidence Level:
Equals 1 - α where α = the risk (%).

Corrective Action: A documented design, process, procedure, or materials change to correct the true cause of a failure. Part replacement with a like item does not constitute appropriate corrective action. Rather, the action should make it impossible for that failure to happen again.

Cumulative Distribution Function (CDF): The probability that the random variable takes on any value less than or equal to a value x, e.g.
$F(x) = CDF(x) = Pr(x \leq X)$.

Defect: A deviation of an item from some ideal state. The ideal state usually is given in a formal specification.

Degradation: A gradual deterioration in performance as a function of time.

Derating: The intentional reduction of stress / strength ratio in the application of an item, usually for the purpose of reducing the occurrence of stress-related failures.

Duty Cycle: A specified operating time of an item, followed by a specified time of no operation.

Early Failure Period: That period of life, after final assembly, in which failures occur at an initially high rate because of the presence of defective parts and workmanship. This definition applies to the first part of the bathtub curve for failure rate (infant mortality).

EDX Spectrometer: Generally used with a scanning electron microscope (SEM) to provide elemental analysis of X-rays generated on the region being hit by the primary electron beam.

Effectiveness: The capability of the system or device to perform its function.

EOS – Electrical Overstress: The electrical stressing of electronic components beyond specifications. May be caused by ESD.

ESD – Electrostatic Discharge: The transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced

by an electrostatic field. Many electronic components are sensitive to ESD and will be degraded or fail.

Expected Value: A statistical term. If x is a random variable and F (x) it its CDF, the E (x) = xdF (x), where the integration is over all x. For continuous variables with a pdf, this reduces to E (x) = $\int$ x pdf (x) dx. For discrete random variables with a pdf, this reduces to E (x) = $\Sigma x_n p (x_n)$ where the sum is over all n.

Exponential Distribution: A 1-parameter distribution ($\lambda > 0$, $t \leq 0$) with: pdf (t) = lexp ($-\lambda t$);
Cdf (t) 0 1 – exp ($-\lambda t$); Sf (t) = exp ($-\lambda t$) ;
failure rate = λ; mean time-to-failure = $1/\lambda$. This is the constant failure-rate-distribution.

Failure: The termination of the ability of an item to perform its required function.

Failure Analysis: The identification of the failure mode, the failure mechanism, and the cause (i.e., defective soldering, design weakness, contamination, assembly techniques, etc.). Often includes physical dissection.

Failure, Catastrophic: A sudden change in the operating characteristics of an item resulting in a complete loss of useful performance of the item.

Failure, Degradation: A failure that occurs as a result of a gradual or partial change in the operating characteristics of an item.

Failure, Initial: The first failure to occur in use.

Failure, Latent: A malfunction that occurs as a result of a previous exposure to a condition that did not result in an immediately detectable failure. Example: Latent ESD failure.

Failure Mechanism: The mechanical, chemical, or other process that results in a failure.

Failure Mode: The effect by which a failure is observed. Generally, describes the way the failure occurs and tells "how" with respect to operation.

Failure Rate: (A) The conditional probability density that the item will fail just after time t, given the item has not failed up to time t; (B) The number of failures of an item per unit measure of life (cycles, time, miles, events, etc.) as applicable for the item.

Failure, Wearout: Any failure for which time of occurrence is governed by rapidly increasing failure rate.

FIT: Failure Unit; (also, Failures In Time) Failures per 109 hours.

Functional Failure: A failure whereby a device does not perform its intended function when the inputs or controls are correct.

Gaussian Distribution: A 2-parameter distribution with:

$$\text{pdf (x)} = \frac{1}{\sigma\sqrt{2\pi}} \cdot e^{\frac{1}{2}\left(\frac{x-u}{\sigma}\right)^2}$$

Cdf (x) = guaf (x). SF (x) = gaufc (x). "Mean value of x" u, "standard deviation of x" = σ

Hazard Rate: Instantaneous failure rate.

Hypothesis, Null: A hypothesis stating that there is no difference between some characteristics of the parent populations of several different samples, i.e., that the samples came from similar populations.

Infant Mortality: Premature catastrophic failures occurring at a much greater rate than during the period of useful life prior to the onset of substantial wear out.

Inspection: The examination and testing of supplies and services (including when appropriate, raw materials, components, and intermediate assemblies) to determine whether they conform to specified requirements.

Inspection by Attributes: Inspection whereby either the unit of product or characteristics thereof is classified simply as defective or no defective or the number of defects in the unit of product is counted with respect to a given requirement.

Life Test: A test, usually of several items, made for the purpose of estimating some characteristic(s) of the probability distribution of life.

Lot: A group of units from a particular device type submitted each time for inspection and / or testing is called the lot.

Lot Reject Rate (LRR): The lot reject rate is the percentage of lots rejected form the lots evaluated.

Lot Tolerance Percent Defective (LTPD): The percent defective, which is to be, accepted a minimum or arbitrary fraction of the time, or that percent defective whose probability of rejection is designated by **b**.

Mean: (A) The arithmetic mean, the expected value; (B) As specifically modified and defined, e.g., harmonic mean (reciprocals), geometric mean (a product), logarithmic mean (logs).

Mean Life: R(t)dt; where R(t) = the s-reliability of the item; t = the interval over which the mean life is desired, usually the useful life (longevity).

Mean-Life-Between-Failures: The concept is the same as mean life except that it is for repaired items and is the mean up-time of the item. The formula is the same as for mean life except that R(t) is inter-

preted as the distribution of up-times. Mean-Time-Between-Failures (MTBF): For a particular interval, the total functioning life of a population of an item divided by the total number of failures within the population during the measurement interval. The definition holds for time, cycles, miles, events, or other measure of life units.

Mean-Time-To-Failure (MTTF): See "Mean Life".

Mean-Time-To-Repair (MTTR): The total corrective maintenance time divided by the total number of corrective maintenance actions during a given period of time.

MTTR: = G(t)dt; where G(t) = Cdf of repair time;
T – maximum allowed repair time, i.e., item is treated as no repairable at this echelon and is discarded or sent to a higher echelon for repair.

Operating Characteristic (OC) Curve: A curve showing the relation between the probability of acceptance and either lot quality or process quality, whichever is applicable.

Part Per Million (PPM): PPM is arrived at by multiplying the percentage defective by 10,000.

Example: 0.1 % = 1,000 PPM.

Population: The totality of the set of items, units, measurements, etc., real or conceptual that is under consideration.

Probability Distribution: A mathematical function with specific properties, which describes the probability that a random variable will take on a value or set of values. If the random variable is continuous and well behaved enough, there will be a pdf. If the random variable is discrete, there will be a pmf.

Qualification: The entire process by which products are obtained from manufacturers or distributors, examined and tested, and then identified on a Qualified Product List.

Quality: A property, which refers to, the tendency of an item to be made to specific specifications and / or the customer's express needs. See current publications by Juran, Deming, Crosby, et al.

Quality Assurance: A system of activities that provides assurance that the overall quality control job is, in fact, being done effectively. The system involves a continuing evaluation of the adequacy and effectiveness of the overall quality control program with a view to having corrective measures initiated where necessary. For a specific product or service, this involves verifications, audits, and the evaluation of the quality factors that affect the specification, production inspection, and use of the product or service.

Quality Characteristics: Those properties of an item or process, which can be measured, reviewed, or observed and which are identified in the drawings, specifications, or contractual requirements. Reliability becomes a quality characteristic when so defined.

Quality Control (QC): The overall system of activities that provides a quality of product or service, which meets the needs of users; also, the use of such a system.

Random Samples: As commonly used in acceptance sampling theory, the process of selecting sample units in such a manner that all units under consideration have the same probability of being selected.

Reliability: The probability that a device will function without failure over a specified time period or amount of usage at stated conditions.

Reliability Growth: Reliability growth is the effort, the resource commitment, to improve design, purchasing, production, and inspection procedures to improve the reliability of a design.

Risk: α : The probability of rejecting the null hypothesis falsely.

Scanning Electron Microscope (SEM): An instrument, which provides a visual image of the surface features of an item. It scans an electron beam over the surface of a sample while held in a vacuum and collects any of several resultant particles or energies. The SEM provides depth of field and resolution significantly exceeding light microscopy and may be used at magnifications exceeding 50,000 times.

Screening Test: A test or combination of tests intended to remove unsatisfactory items or those likely to exhibit early failures.

Significance: Results that show deviations between hypothesis and the observations used as a test of the hypothesis, greater than can be explained by random variation or chance alone, are called statistically significant.

Significance Level: The probability that, if the hypothesis under test were true, a sample test statistic would be as bad as or worse than the observed test statistic.

SPC: Statistical Process Control.

Storage Life (Shelf Life): The length of time an item can be stored under specified conditions and still meet specified requirements.

Stress: A general and ambiguous term used as an extension of its meaning in mechanics as that which could cause failure. It does not distinguish between those things which cause permanent damage (deteri-

oration) and those things, which do not (in the absence of failure).

Variance: The average of the squares of the deviations of individual measurements from their average. It is a measure of dispersion of a random variable or of data.

Wearout: The process of attribution which results in an increase of hazard rate with increasing age (cycles, time, miles, events, etc.) as applicable for the item.

Abbreviations

AQL	Acceptable Quality Level
CAR	Corrective Action Report / Request
DIP	Dual In-Line Package
ECAP	Electronic Circuit Analysis Program
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
EOS	Electrical Overstress
ESD	Electrostatic Discharge
FAR	Failure Analysis Report / Request
FIT	(Failure In Time) Failure Unit; Failures / 109 hours
FMEA	Failure Mode and Effects Analysis
FTA	Fault Tree Analysis
h (t)	Hazard Rate
LTPD	Lot Tolerance Percent Defective
MOS	Metal Oxide Semiconductor
MRB	Material Review Board
MTBF	Mean-Time-Between-Failures
MTTF	Mean-Time-To-Failure
MTTR	Mean-Time-To-Repair
PPM	Parts Per Million
PRST	Probability Ratio Sequential Test
QA	Quality Assurance
QC	Quality Control
QPL	Qualified Products List
RPM	Reliability Planning and Management
SCA	Sneak Circuit Analysis
SEM	Scanning Electron Microscope
TW	Wearout Time
Z (t)	Hazard Rate
λ	Failure Rate (Lambda)

Assembly Instructions

General

Vishay offers a wide product selection of optocouplers and solid state relays in a variety of packages. This document provides instructions on mounting for the different types of packages, specifically on the different methods of soldering. For DIP packages, they can be mounted in DIP sockets or directly on a predesigned PCB with holes.

If the device is to be mounted near heat-generating components, consideration must be given to the resultant increase in ambient temperature.

Soldering Instructions

Protection against overheating is essential when a device is being soldered. Therefore, the connection wires or PCB traces should be left as long as possible. The maximum permissible soldering temperature is governed by the maximum permissible heat that may be applied to the package.

The maximum soldering iron (or solder bath) temperatures are given in the individual Datasheets. During soldering, no forces must be transmitted from the pins to the case (e.g., by spreading the pins).

Soldering Methods

There are several methods for soldering devices onto the substrate. The following list is not complete.

(a) Soldering in the vapor phase

Soldering in saturated vapor is also known as condensation soldering. This soldering process is used as a batch system (dual vapor system) or as a continuous single vapor system. Both systems may also include a pre-heating of the assemblies to prevent high temperature shock and other undesired effects.

(b) Infrared soldering

By using infrared (IR) reflow soldering, the heating is contact-free and the energy for heating the assembly is derived from direct infrared radiation and from convection (Refer to CECC00802).

The heating rate in an IR furnace depends on the absorption coefficients of the material surfaces and on the ratio of component's mass to an As-irradiated surface.

The temperature of parts in an IR furnace, with a mixture of radiation and convection, cannot be determined in advance. Temperature measurement may be performed by measuring the temperature of a certain component while it is being transported through the furnace.

The temperatures of small components, soldered together with larger ones, may rise up to 280 °C.

Influencing parameters on the internal temperature of the component are as follows:

- Time and power
- Mass of the component
- Size of the component
- Size of the printed circuit board
- Absorption coefficient of the surfaces
- Packing density
- Wavelength spectrum of the radiation source
- Ratio of radiated and convected energy

As a general rule of thumb, maximum temperature should be reached within 360 seconds and time above solder liquids temperature should be reached in less than 180 seconds.

Temperature/time profiles of the entire process and the influencing parameters are given. The IR reflow profile is shown in Figure 2.

(c) Wave soldering

In wave soldering one or more continuously replenished waves of molten solder are generated, while the substrates to be soldered are moved in one direction across the crest of the wave. Maximum soldering temperature is 260 °C for 10 seconds.

Temperature/time profiles of the entire process are given in figure 2.

(d) Iron soldering

This process cannot be carried out in a controlled situation. It should therefore not be used in applications where reliability is important. There is no SMD classification for this process.

(e) Laser soldering

This is an excess heating soldering method. The energy absorbed may heat the device to a much higher temperature than desired. There is no SMD classification for this process at the moment.

(f) Resistance soldering

This is a soldering method which uses temperature-controlled tools (thermodes) for making solder joints. There is no SMD classification for this process at the moment.

Temperature - Time Profiles

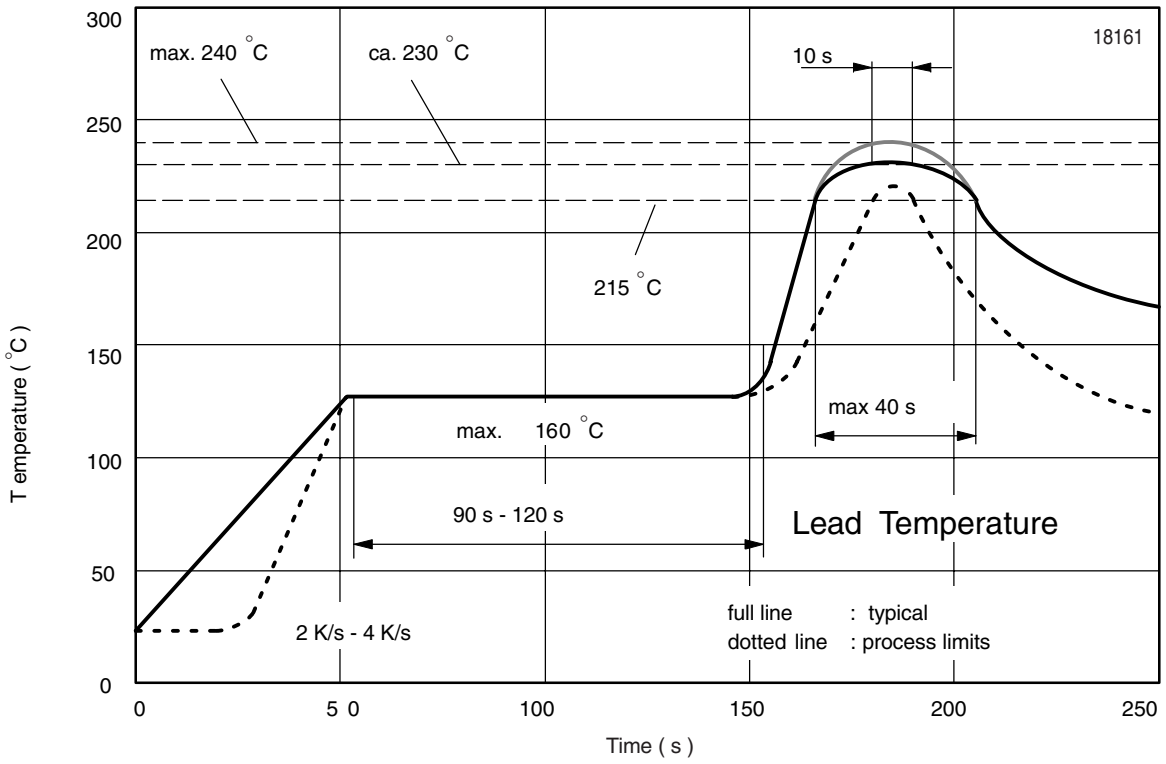


Figure 1. Infrared reflow soldering optodevices (SMD package)

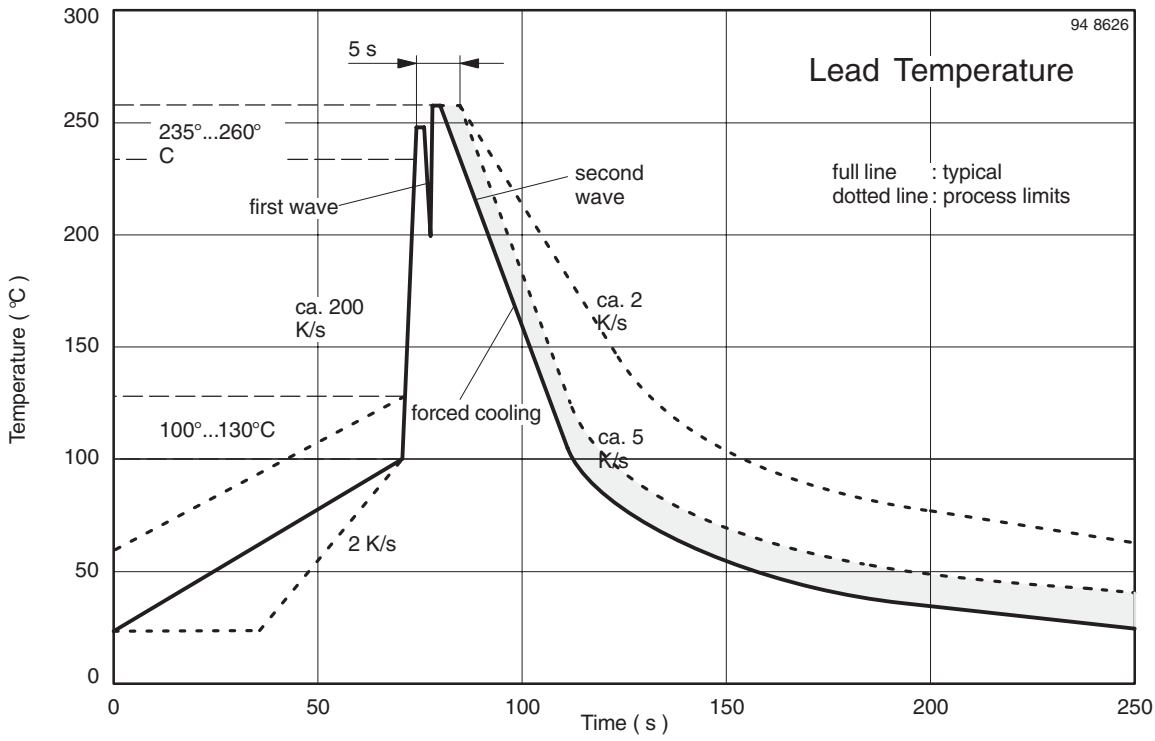


Figure 2. Wave soldering double wave optodevices

Heat Removal

The heat generated in the semiconductor junction(s) must be moved to the ambient. In the case of low-power devices, the natural heat conductive path between case and surrounding air is usually adequate for this purpose.

In the case of medium-power devices, however, heat conduction may have to be improved by the use of star- or flag-shaped heat dissipators which increase the heat radiating surface.

The heat generated in the junction is conveyed to the case or header by conduction rather than convection; a measure of the effectiveness of heat conduction is the inner thermal resistance or thermal resistance junction case, R_{thJC}, whose value is given by the construction of the device.

Any heat transfer from the case to the surrounding air involves radiation convection and conduction, the effectiveness of transfer being expressed in terms of an R_{thCA} value, i.e., the case ambient thermal resistance. The total thermal resistance, junction ambient is therefore:

$R_{thJA} = R_{thJC} + R_{thCA}$

The total maximum power dissipation, P_{totmax}, of a semiconductor device can be expressed as follows:

$$P_{totmax} = \frac{T_{jmax} - T_{amb}}{R_{thJA}} = \frac{T_{jmax} - T_{amb}}{R_{thJC} + R_{thCA}}$$

where:

T_{jmax} the maximum allowable junction temperature

T_{amb} the highest ambient temperature likely to be reached under the most unfavorable conditions

R_{thJC} the thermal resistance, junction case

R_{thJA} the thermal resistance, junction ambient

R_{thCA} the thermal resistance, case ambient, depends on cooling conditions. If a heat dissipator or sink is used, then R_{thCA} depends on the thermal contact between case and heat sink, heat propagation conditions in the sink and the rate at which heat is transferred to the surrounding air.

Therefore, the maximum allowable total power dissipation for a given semiconductor device can be influenced only by changing T_{amb} and R_{thCA}. The value of R_{thCA} could be obtained either from the data of heat sink suppliers or through direct measurements.

In the case of cooling plates as heat sinks, the approach outlines in figures 3 and 4 can be used as guidelines. The curves shown in both figures 3 and 4 give the thermal resistance R_{thCA} of square plates of aluminium with edge length, a, and with different thicknesses. The case of the device should be mounted directly onto the cooling plate.

The edge length, α, derived from figures 3 and 4 in order to obtain a given R_{thCA} value, must be multiplied with α and β:

$\alpha' = \alpha \cdot \beta \cdot \alpha$

where

$\alpha = 1.00$ for vertical arrangement

$\alpha = 1.15$ for horizontal arrangement

$\beta = 1.00$ for bright surface

$\beta = 0.85$ for dull black surface

Example

For an IR emitter with T_{jmax} = 100 °C and R_{thJC} = 100 K/W, calculate the edge length for a 2 mm thick aluminium square sheet having a dull black surface ($\beta = 0.85$) and vertical arrangement ($\alpha = 1$), T_{amb} = 70 °C and $P_{tot\,max}$ = 200 mW.

$$P_{totmax} = \frac{T_{jmax} - T_{amb}}{R_{thJC} + R_{thCA}}$$

$$R_{thCA} = \frac{T_{jmax} - T_{amb}}{P_{totmax}} - R_{thJC}$$

$$R_{thCA} = \frac{100\,°C - 70\,°C}{0.2\ \text{W}} - 100\ \text{K/W}$$

$$R_{thCA} = \frac{30}{0.2} - 100\ \text{K/W}$$

$$R_{thCA} = 50\ \text{K/W}$$

$\Delta T = T_{case} - T_{amb}$

can be calculated from the relationship:

$$P_{totmax} = \frac{T_{jmax} - T_{amb}}{R_{thJC} + R_{thCA}} = \frac{T_{case} - T_{amb}}{R_{thCA}}$$

$$\Delta T = T_{case} - T_{amb} = \frac{R_{thCA} \cdot (T_{jmax} - T_{amb})}{R_{thJC} + R_{thCA}}$$

$$\Delta T = \frac{50\ \text{K/W} \cdot 100\ °\text{C} - 70\ °\text{C}}{150\ \text{K/W}}$$

$$\Delta T = \frac{50\ \text{K/W} \cdot 30\ °\text{C}}{150\ \text{K/W}}$$

$$\Delta T = 10\ °\text{C} = 10\ \text{K}$$

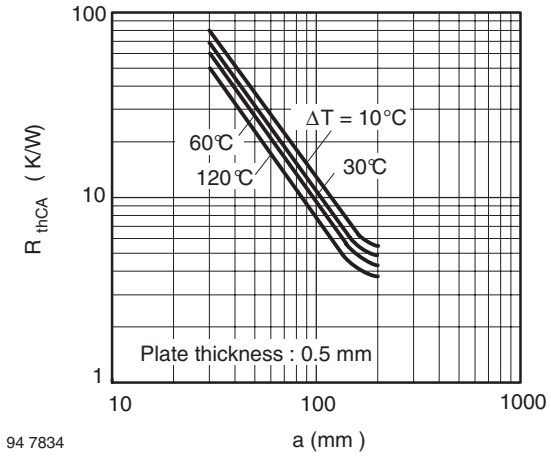


Figure 3.

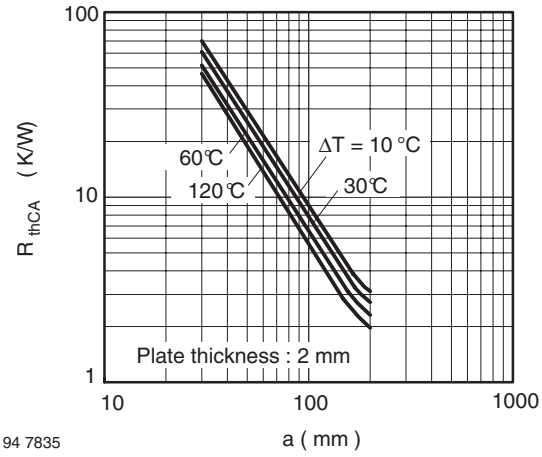


Figure 4.

With R_{thCA} = 50 k/W and ΔT = 10 °C, a plate of 2 mm thickness has an edge length $\alpha = 28\ \mu$.

However, equipment life and reliability have to be taken into consideration and therefore a larger sink would normally be used to avoid operating the devices continuously at their maximum permissible junction temperature.

Handling Instructions

Protection against Electrostatic Damage

Although electrostatic breakdown is most often associated with IC semiconductor devices, optoelectronic devices are also prone to electrostatic damage. Miniaturized and highly integrated components are particularly sensitive.

Sensitivity

Breakdown Voltages

Typical electrostatic discharge in the working environment can easily reach several thousand volts, well above the level required to cause a breakdown. As market requirements are moving towards greater miniaturization, lower power consumption, and higher speeds, optoelectronic devices are becoming more integrated and delicate. This means that they are becoming increasingly sensitive to electrostatic effects.

Device Breakdown

Electrostatic discharge events are often imperceptible. However, some of the the following problems may occur.

Delay Failure

Electrostatic discharge may damage the device or change its characteristics without causing immediate failure. The device may pass inspection, move into the market, then fail during its initial period of use.

Difficulty in Identifying Discharge Site

Human beings generally cannot perceive electrostatic discharges of less than 3000 V, while semiconductor devices can sustain damage from electrostatic voltages as low as 100 V. It is often very difficult to locate the process at which electrostatic problems occur.

Basic Countermeasures

Optoelectronic devices should be protected from static electricity at all stages of processing. Each device must be protected from the time it is received until the time it has been incorporated into a finished assembly. Each processing stage should incorporate the following measures.

Suppression of Electrostatic Generation

Keep relative humidity at 50 to 70 % (if humidity is above 70 %, morning dew may cause condensation). Remove materials which might cause electrostatic generation (such as synthetic resins) from your workplace. Check the appropriateness of floor mats, clothing (uniforms, sweaters, shoes), parts trays, etc. Use electrostatically safe equipment and machinery.

Removal of Electrostatic Charges

Connect conductors (metals, etc.) to ground, using dedicated grounding lines. To prevent dangerous shocks and damaging discharge surges, insert a resistance of 800 kΩ between conductor and grounding line.

Connect conveyors, solder baths, measuring machines, and other equipment to ground, using dedicated, grounding lines.

Use ionic blowers to neutralize electrostatic charges on insulators. Blowers pass charged air over the targeted object, neutralizing the existing charge. They are useful for discharging insulators or other objects that cannot be effectively grounded.

Human Electrostatic

The human body readily picks up electrostatic charges, and there is always some risk that human operators may cause electrostatic damages to the semiconductor devices they handle. The following measures are essential.

Anti-Static Wrist Straps

All people who come into direct contact with semiconductors should wear anti-static wrist straps, i.e., those in charges of parts supply and people involved in mounting, board assembly and repair.

Be sure to insert a resistance of 800 kW to 1 MW into the straps. The resistance protects against electrical shocks and prevents instantaneous and potentially damaging discharges from charged semiconductor devices.

The straps should be placed next to the skin, placing them over gloves, uniforms or other clothing reduces their effectiveness.

Antistatic Mats, Uniforms and Shoes

The use of anti-static mats and shoes is effective in places where use of a wrist strap is inconvenient (for example, when placing boards into returnable boxes). To prevent static caused by friction with clothing, personnel should wear anti-static uniforms, gloves, sleeves aprons, finger covers, or cotton apparel.

Protection during Inspection, Mounting and Assembly

Each individual must ensure that hands do not come into direct contact with leads. Avoid non-conductive finger covers. Cover the work desk with grounded anti-static mats.

Storage and Transport

Always use conductive foams, tubes, bags, reels or trays when storing or transporting semiconductor devices.

Mounting Precautions

Installation

Installation on PWB

When mounting a device on PWB whose pin-hole pitch does not match the lead pin pitch of the device, reform the device pins appropriately so that the internal chip is not subjected to physical stress.

Installation Using a Device Holder

Emitters and detectors are often mounted using a holder. When using this method, make sure that there is no gap between the holder and device.

Installation Using Screws

When lead soldering is not adequate to securely retain a photo interrupter, it may be retained with screws.

The tightening torque should not exceed 6 kg/cm^3. An excessive tightening torque may deform the holder, which results in poor alignment of the optical axes and degrades performance.

Lead Forming

Lead pins should be formed before soldering. Do not apply forming stress to lead pins during or after soldering. For light emitters or detectors with lead frames, lead pins should be formed just beneath the stand-off cut section. For optocouplers or opto sensors using dual-in-line packages, lead pins should beformed below the bent section so that forming stress does not affect the inside of the device. Stress to the resin may result in disconnection.

When forming lead pins, do not bend the same portion repeatedly, otherwise the pins may break.

Cleaning

General

Optoelectronic devices are particularly sensitive with regard to cleaning solvents. The Montreal Protocol for environmental protection calls for a complete ban on the use of chlorofluorocarbons. Therefore, the most harmless chemicals for optoelectronic devices should be used for environmental reasons. The best solution is to use a modem reflow paste or solder composition which does not require a cleaning procedure. No cleaning is required when the fluxes are guaranteed to be non-corrosive and of high, stable resistivity.

Cleaning Procedures

Certain kinds of cleaning solvents can dissolve or penetrate the transparent resins which are used in some types of sensors. Even black molding components used in standard isolators are frequently penetrated between the mold compound and lead frame. Inappropriate solvents may also remove the marking printed on a device. It is therefore essential to take care when choosing solvents to remove flux.

Cleaning is not required if the flux in the solder material is non-aggressive and any residues are guaranteed to be non corrosive an long-term stable of high resistivity. In cleaning procedures using wet solvents only high purity Ethyl and Isopropyl alcohol are recommended.

In each case, the devices are immersed in the liquid for typically 3 minutes and afterwards immediately dried for at least 15 minutes at 50 °C in dry air.

In table 1, appropriate cleaning procedures for various product lines are summarized.

Cleaning Procedure		Product Lines		
Solvent	Procedure	Dil-Coupler		High Voltage Couplers
		System “A“	System “U“	
-	No cleaning of solder materials	O	O	O
Ethyl alcohol	Immersion + drying	O	O	O
Isopropyl alcohol	Immersion + drying	O	O	O
Water	Immersion + drying	-[1)]	O	-

Table 1:

O acceptable

- not acceptable

1) acceptable only if transistor base is not connected to the outside

Precautions

Intensified cleaning methods such as ultrasonic cleaning, steam cleaning, and brushing can cause damage to optoelectronic devices. They are generally not recommended.

Ultrasonic cleaning (unless well controlled) can damage the devices due to mechanical vibrations.

Using high-intensity ultrasonic cleaning, the process might:

a. Promote dissolution or crack the package surface and thus affect the performance of e.g., the sensors

b. Promote separation of the lead frame and resin and thus reduce humidity resistance.

c. Promote the breakage of band wires

This method should only be used after extensive trials have been run to ensure that problems do not occur. Brushing can scratch package surfaces. Moreover, it can remove printed markings.

Special care should be taken to use only high purity or chemically well-controlled solvents. Chloride ions, from flux or solvents that remain in the package are a high risk for the long-time stability of any electronic device. These as well as other promote corrosion on the chip which can interrupt all bond connections to the outside leads.

Packaging, Tape and Reel Information

Description

Optocouplers are available in plastic dual-in-line packages (DIP), SOP packages, and in a surface-mount, gull-wing, lead bend configuration. Optocouplers purchased in the DIP configuration are shipped in tubes. Optocouplers purchased in a gull-wing configuration can be shipped in tubes or on carrier tape. This section provides stick specifications, tape and reel specifications, and component information.

Tube Specifications

Figure 1 shows the physical dimensions of transparent, antistatic, plastic shipping tubes. Figure 2 shows tube safety agency labeling and orientation information.

The following table lists the number of parts per tube.

Devices per Tube

Package	Quantity
4-pin DIP	90
6-pin DIP	50
6-pin gull wing	50
8-pin DIP	50
8-pin gull wing	50
8-pin SOP	90
16-pin DIP	20
16-pin SOP	40

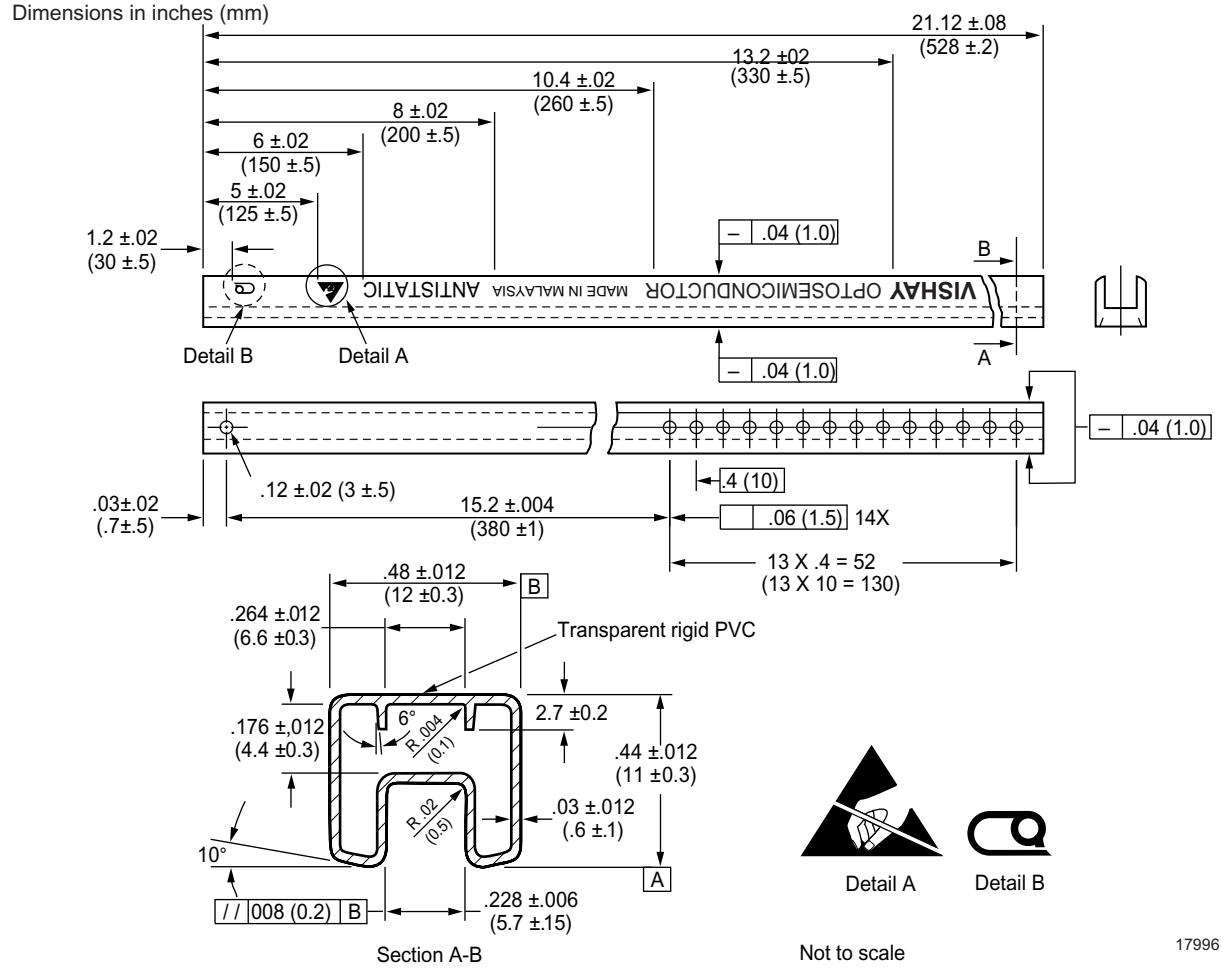


Figure 1. Shipping Tube Specifications for DIP Packages

Dimensions in inches (mm)

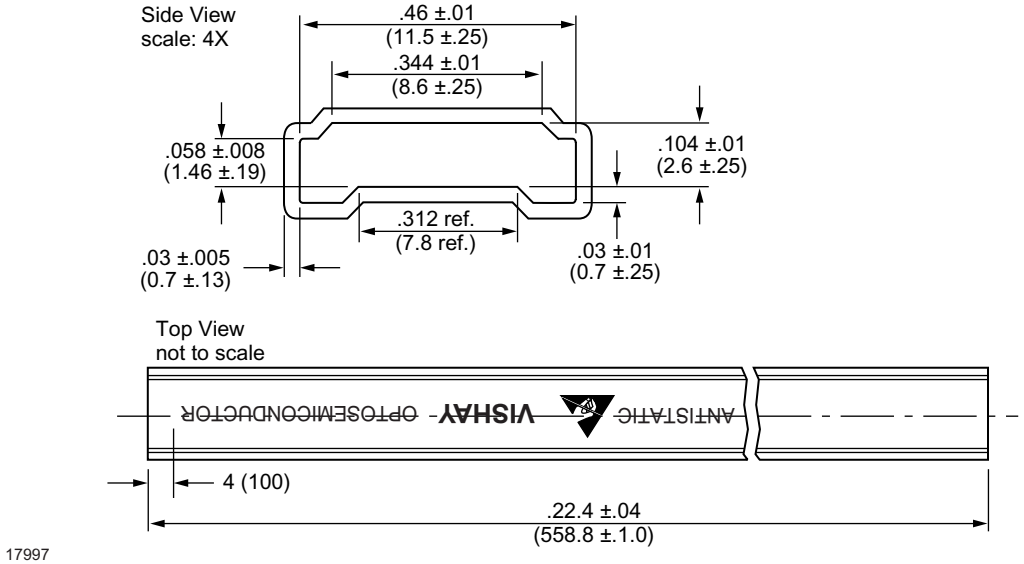


Figure 2. Shipping Tube Specifications for SOP Packages

Tube Specifications for DIP and High Isolation Voltage Packages

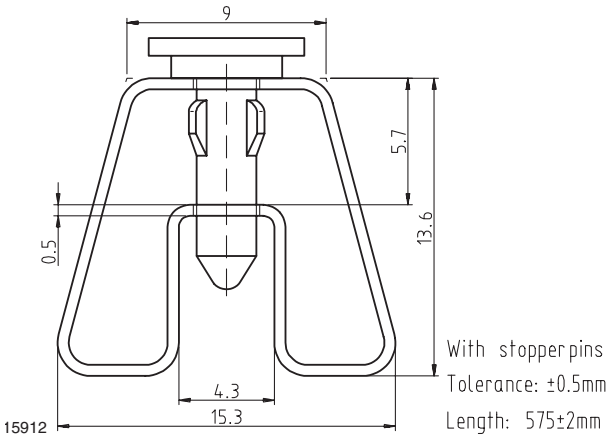


Figure 3. DIP-6 N, G

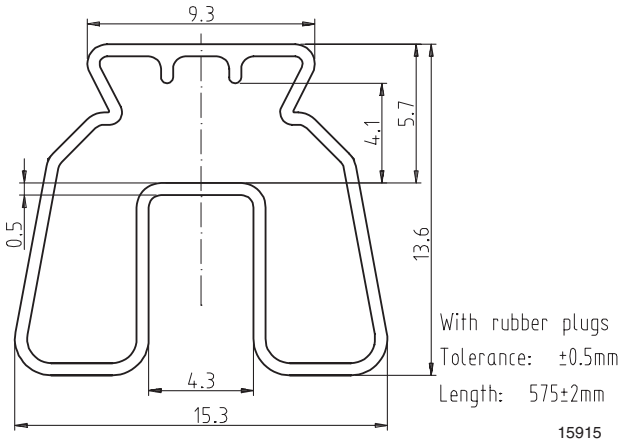


Figure 4. DIP-4, -2, -16 N, G

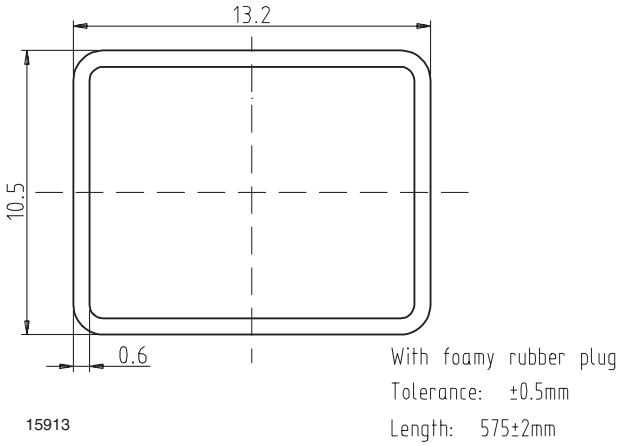


Figure 5. CNY64

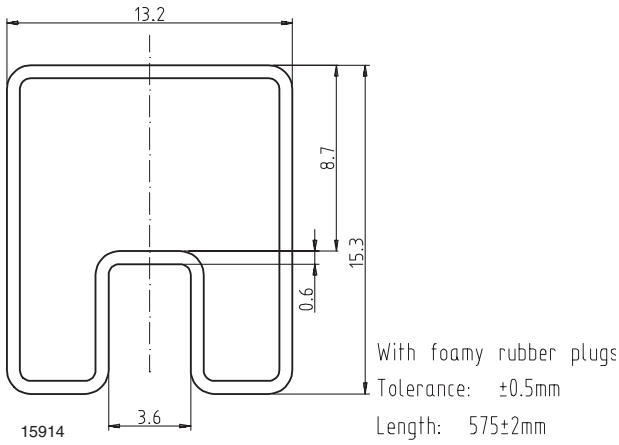


Figure 6. CNY65, 66

Tape and Reel Specifications

Surface-mounted devices are packaged in embossed tape and wound onto 13-inch molded plastic reels for shipment, to comply with Electronics Industries Association Standard EIA-481, revision A.

Leaders and Trailers

The carrier tape and cover tape are not spliced. Both tapes are one single uninterrupted piece from end to end, as shown in Figure 2. Both ends of the tape have empty pockets meeting these requirements.

- Trailer end (inside hub of reel) is 200 mm minimum.
- Leader end (outside of reel) is 400 mm minimum and 560 mm maximum.
- Unfilled leader and trailer pockets are sealed.
- Leaders and trailers are taped to tape and hub, respectively, with masking tape.
- All materials are static-dissipative

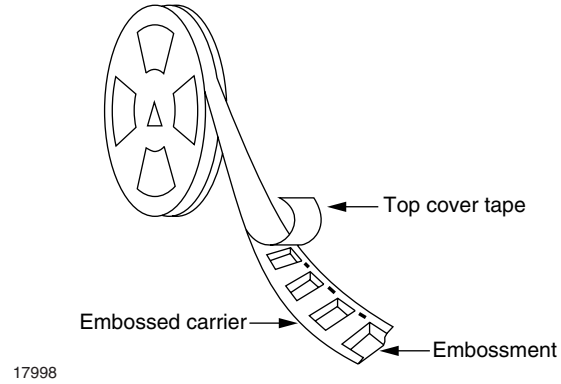


Figure 7. Tape and Reel Shipping Medium

Reels

- As shown in Figure 4, all reels contain standard areas for the placement of ESD stickers and labels. Each reel also has a tape slot in its core. The overall reel dimension is 13 inches. Reels contain 1000 6- or 8-pin gull-wing parts and could have up to three inspection lots.

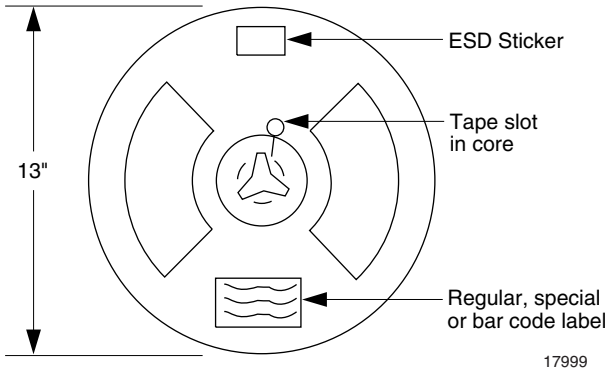
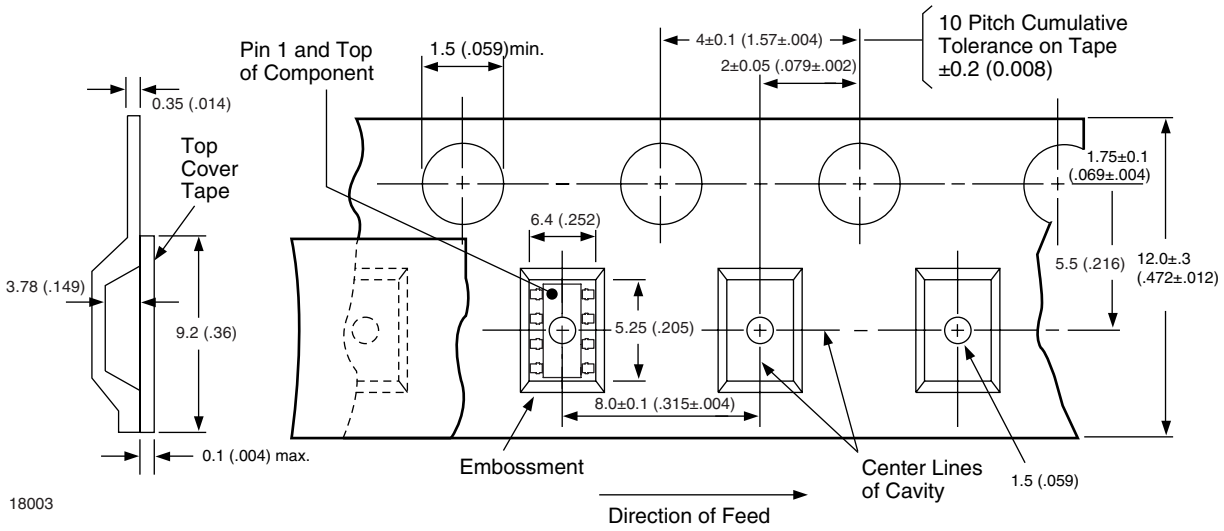


Figure 8.

Tape and Reel Packaging for Single Channel SOIC8 Optocouplers

Selected SOIC8 optocouplers are available in tape and reel format. To order surface mount IL2XXA optocoupler on tape and reel, add a suffix "T" after the part number, i.e., IL207AT.

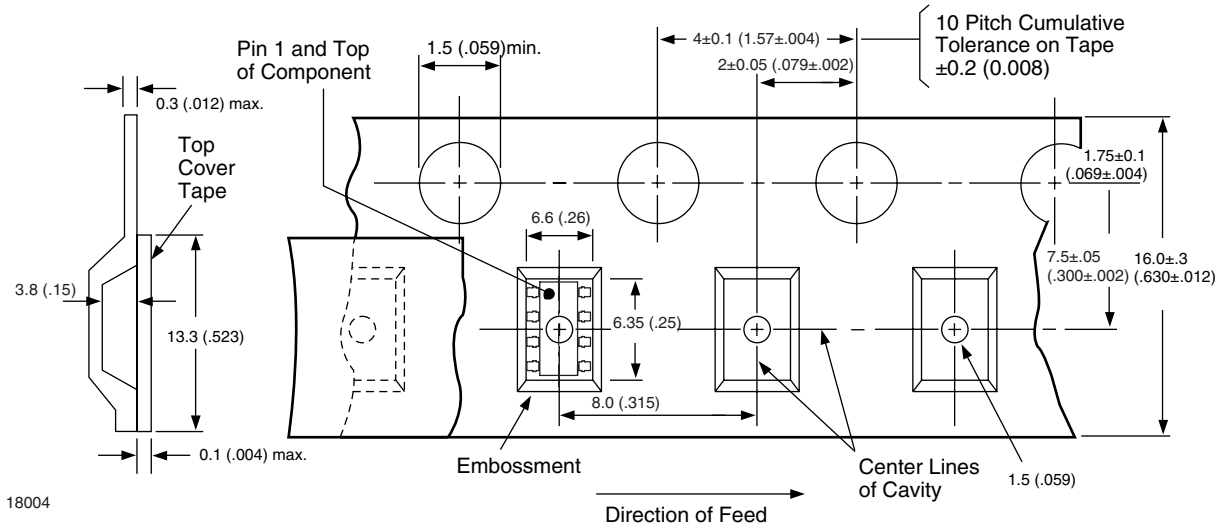
The tape is 12 mm wide on a 33 cm reel. There are 200 parts per reel. Taped and reeled SOIC8-A optocouplers conform to EIA-481-2.



Tape and Reel Packaging for Dual Channel SOIC8 Optocouplers

Selected dual SOIC8 optocouplers are available in tape and reel format. To order surface mount ILD2XX optocoupler on tape and reel, add a suffix "T" after the part number, i.e., ILD207T.

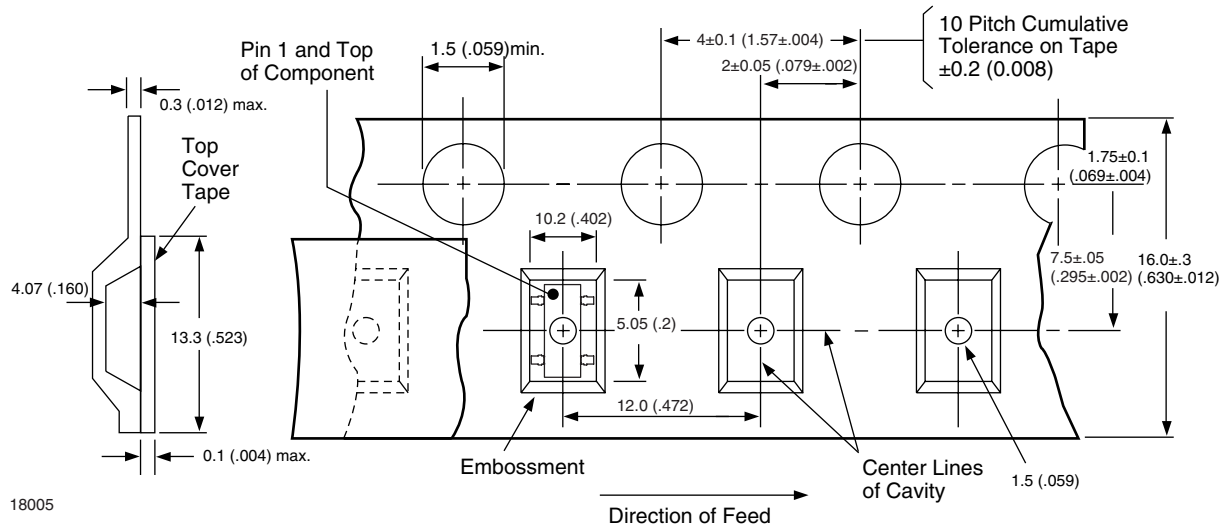
The tape is 16 mm and is wound on a 33 cm reel. There are 2000 parts per reel. Taped and reeled dual SOIC8 optocouplers conform to EIA-481-2.



Tape and Reel Packaging for DIP-4 Optocouplers with Option 9

Selected 4-pin optocouplers are available in tape and reel format. To order any SFH6XX6 optocoupler on tape and reel, add a suffix "T" after the part number, i.e., SFH6156-3T.

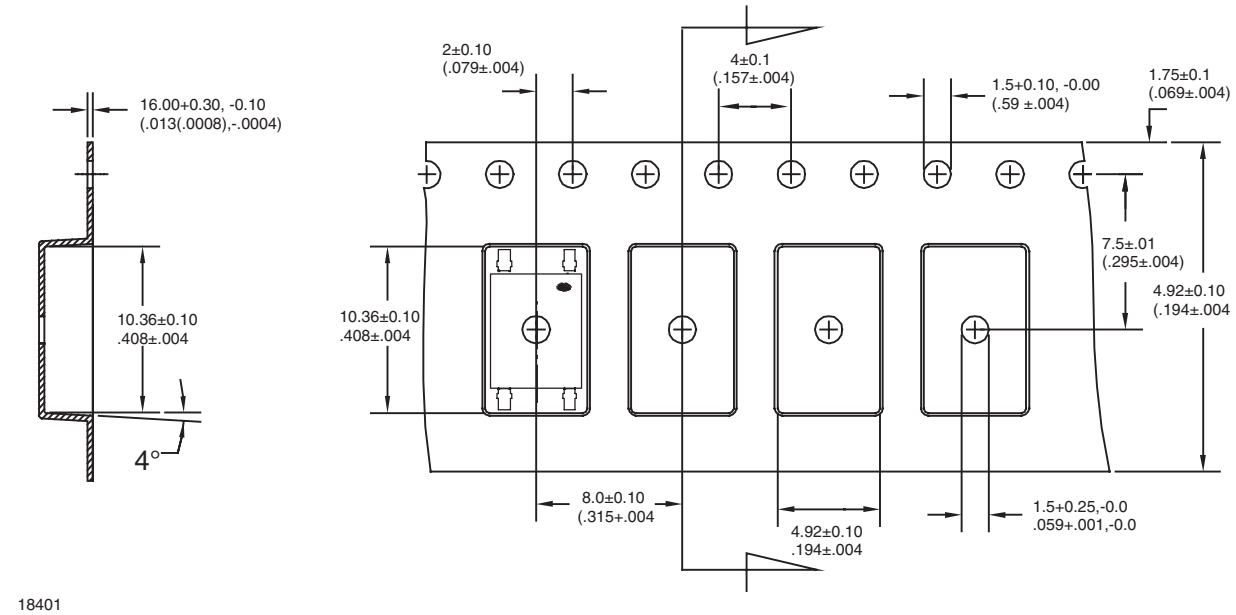
The tape is 16 mm and is wound on a 33 cm reel. There are 1000 parts per reel. Taped and reeled 4-pin optocouplers conform to EIA-481-2.



Tape and Reel Packaging for DIP-4 Optocouplers with Option 9, 90 ° Rotation

Selected 4-pin optocouplers are available in tape and reel format.

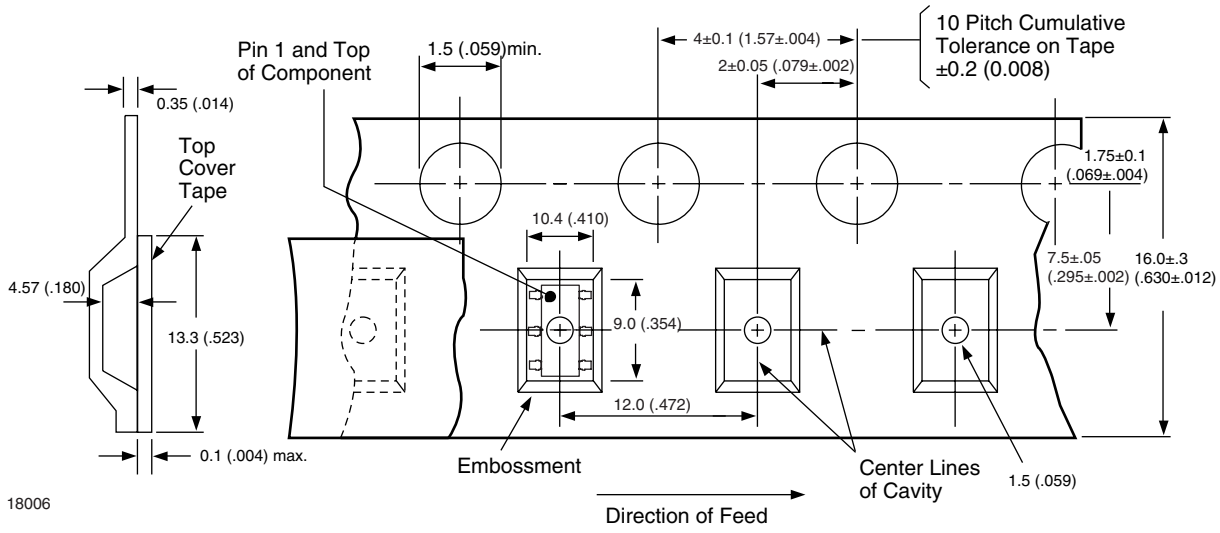
The tape is 16 mm and is wound on a 33 cm reel. There are 2000 parts per reel. Taped and reeled 4-pin optocouplers conform to EIA-481-2.



Tape and Reel Packaging for DIP-6 Optocouplers with Option 7

Selected 6-pin optocouplers with Option 7 are available in tape and reel format. To order 6-pin optocoupler with Option 7 on tape and reel, add a suffix "T" after the option, i.e., CNY17-3X007T.

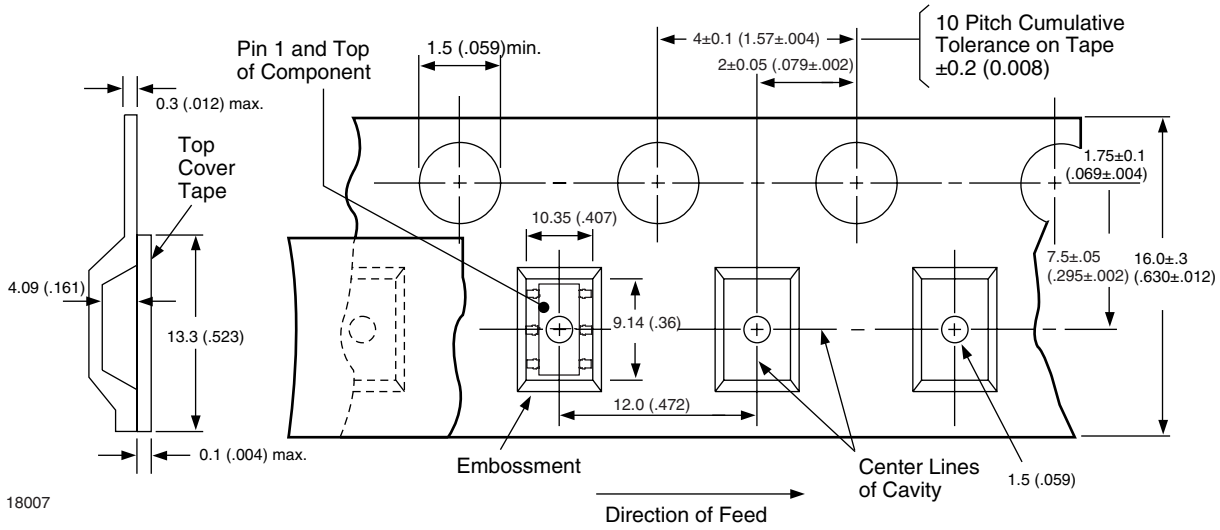
The tape is 16 mm and is wound on a 33 cm reel. There are 1000 parts per reel. Taped and reeled 6-pin optocouplers conform to EIA-481-2.



Tape and Reel Packaging for DIP-6 Optocouplers with Option 9

Selected 6-pin optocouplers with Option 9 are available in tape and reel format. To order 6-pin optocoupler with Option 9 on tape and reel, add a suffix "T" after the option, i.e., CNY17-3X009T.

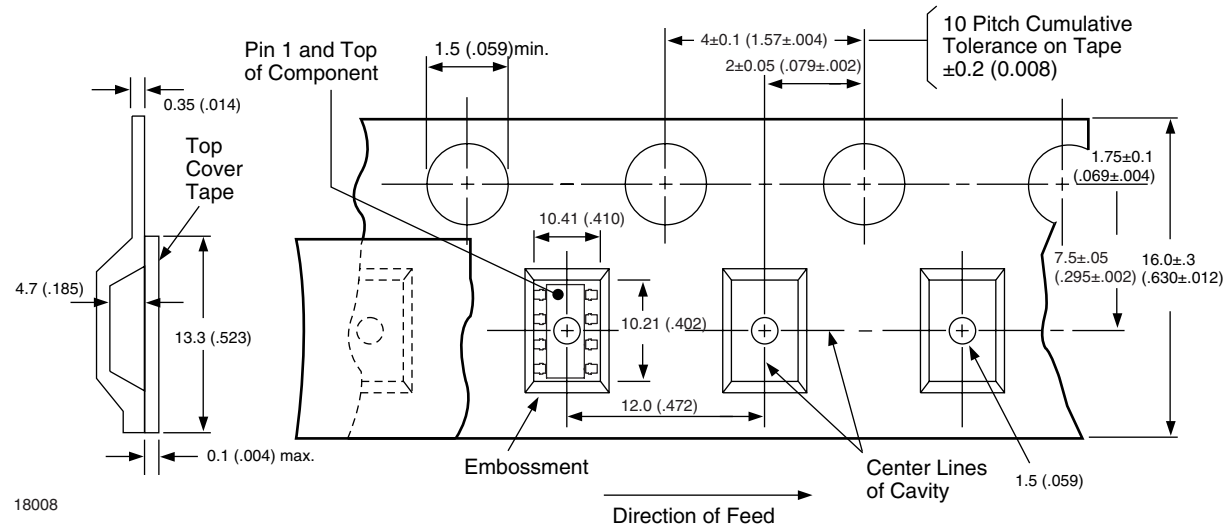
The tape is 16 mm and is wound on a 33 cm reel. There are 1000 parts per reel. Taped and reeled 6-pin optocouplers conform to EIA-481-2.



Tape and Reel Packaging for DIP-8 Optocouplers with Option 7

Selected 8-pin optocouplers with Option 9 are available in tape and reel format. To order 8-pin optocoupler with Option 7 on tape and reel, add a suffix "T" after the option, i.e., ILCT6-X007T.

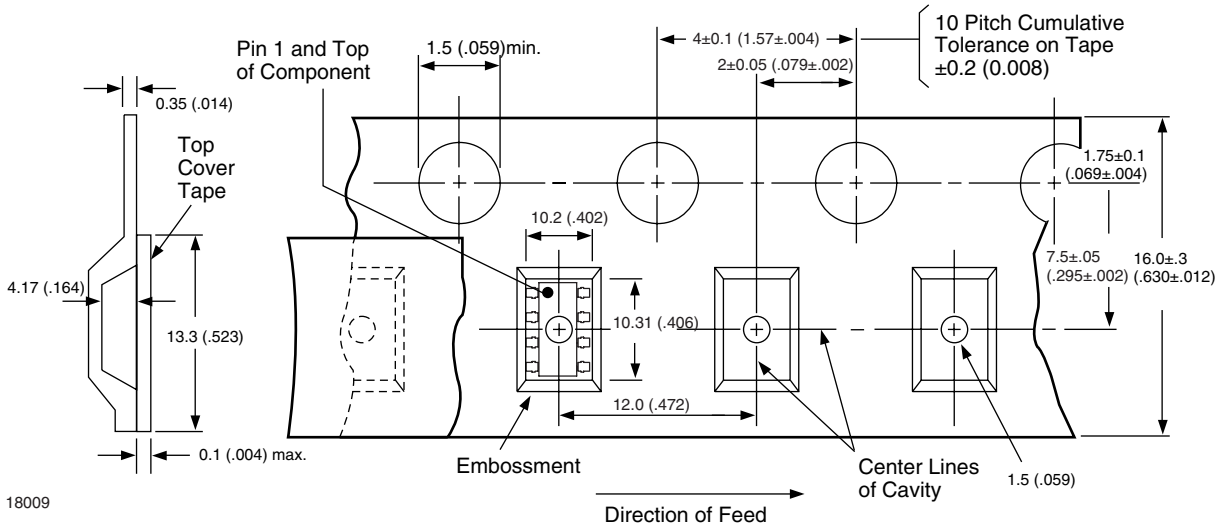
The tape is 16 mm and is wound on a 33 cm reel. There are 1000 parts per reel. Taped and reeled 8-pin optocouplers conform to EIA-481-2.



Tape and Reel Packaging for DIP-8 Optocouplers with Option 9

Selected 8-pin optocouplers with Option 9 are available in tape and reel format. To order 8-pin optocoupler with Option 9 on tape and reel, add a suffix "T" after the option, i.e., ILCT6-X009T.

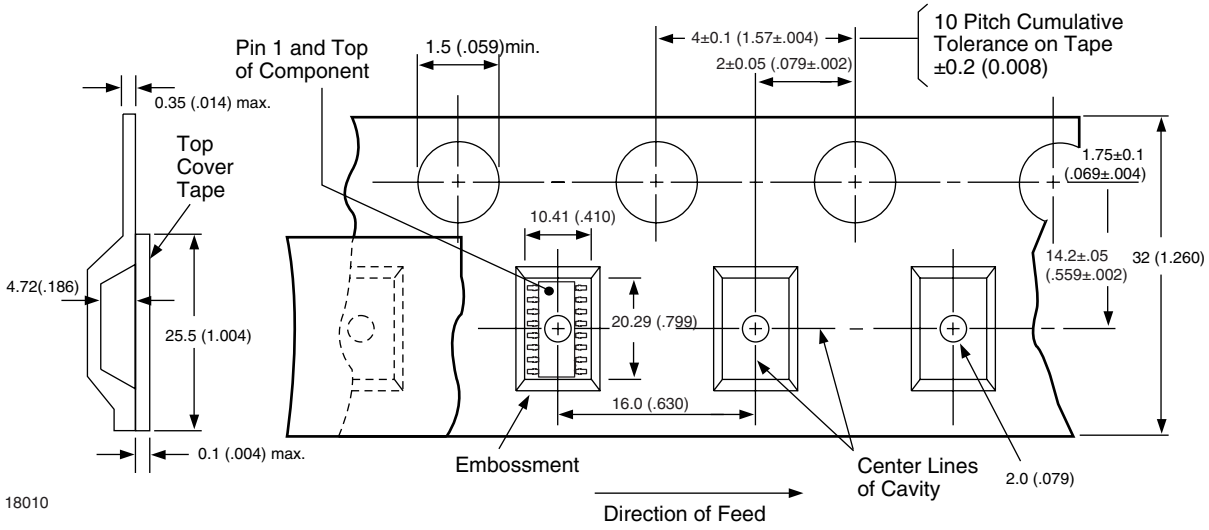
The tape is 16 mm and is wound on a 33 cm reel. There are 1000 parts per reel. Taped and reeled 8-pin optocouplers conform to EIA-481-2.



Tape and Reel Packaging for DIP-16, SMD Optocouplers with Option 7

Selected 16-pin optocouplers with Option 7 are available in tape and reel format. To order 16-pin optocoupler with Option 7 on tape and reel, add a suffix "T" after the option, i.e., ILQ-X007T.

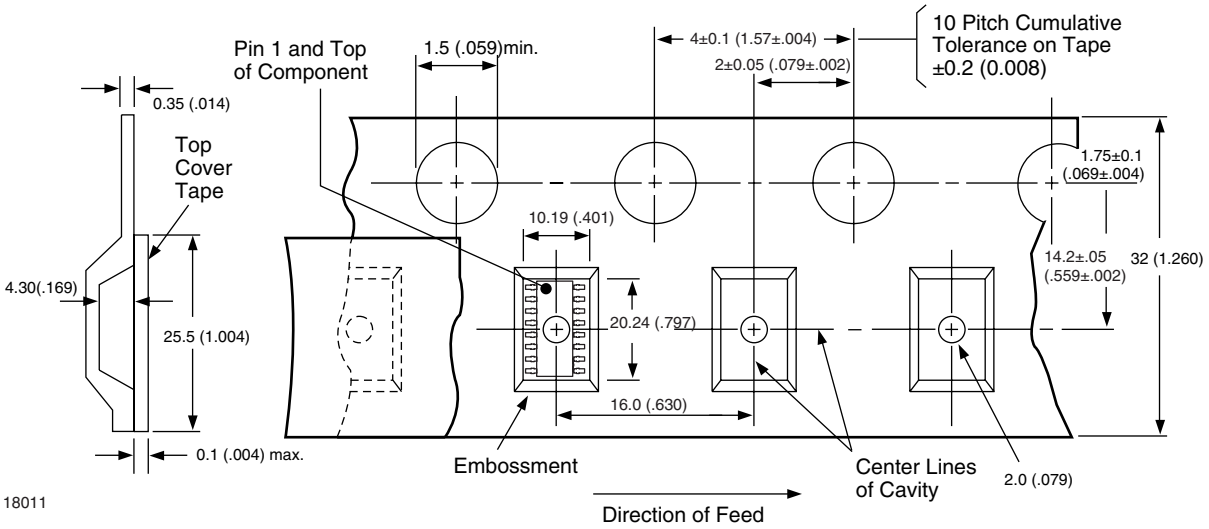
The tape is 32 mm and is wound on a 33 cm reel. There are 750 parts per reel. Taped and reeled 16-pin optocouplers conform to EIA-481.



Tape and Reel Packaging for DIP-16, SMD Optocouplers with Option 9

Selected 16-pin optocouplers with Option 9 are available in tape and reel format. To order 16-pin optocoupler with Option 9 on tape and reel, add a suffix "T" after the option, i.e., ILQ1-X009T.

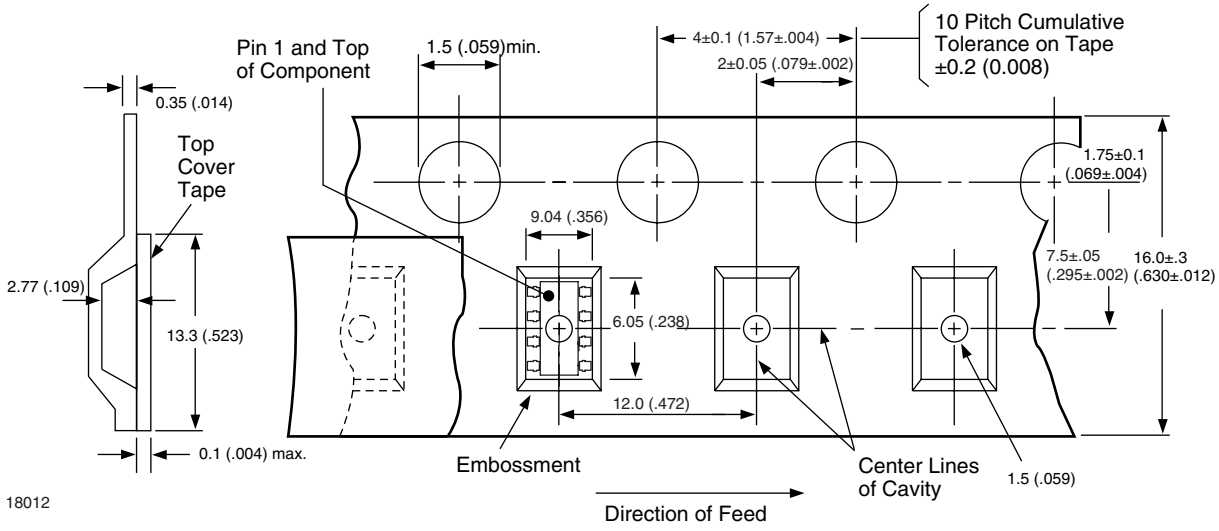
The tape is 32 mm and is wound on a 33 cm reel. There are 750 parts per reel. Taped and reeled 16-pin optocouplers conform to EIA-481.



Tape and Reel Packaging for SOP-8 Optocouplers

Selected 8-pin 2 mm optocouplers are available in tape and reel format. To order 8-pin 2 mm optocoupler on tape and reel, add a suffix "T" after the part number.

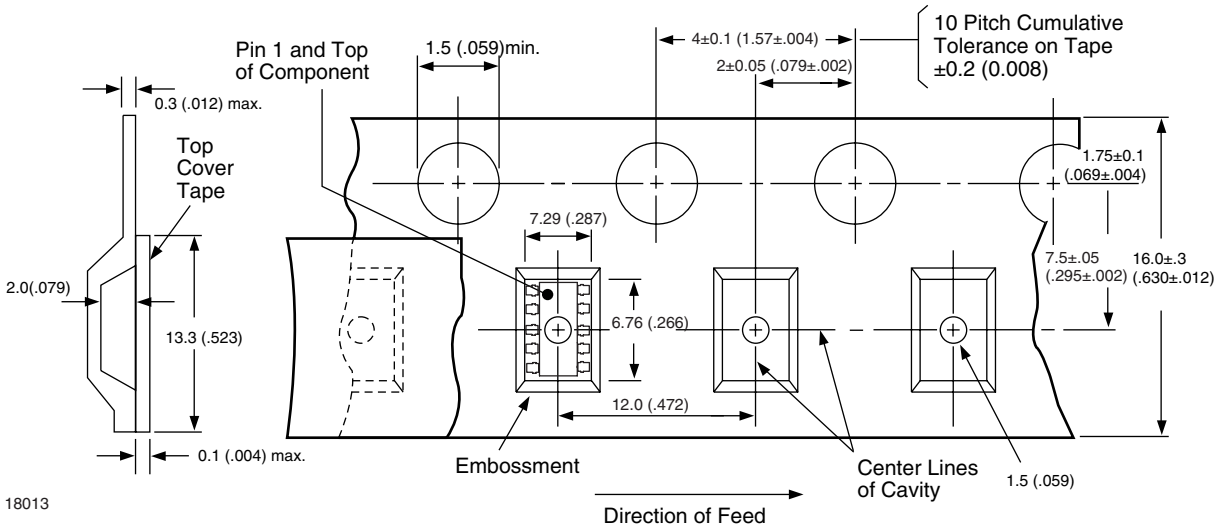
The tape is 16 mm and is wound on a 33 cm reel. There are 2000 parts per reel. Taped and reeled 8-pin 2mm optocouplers conform to EIA-481.



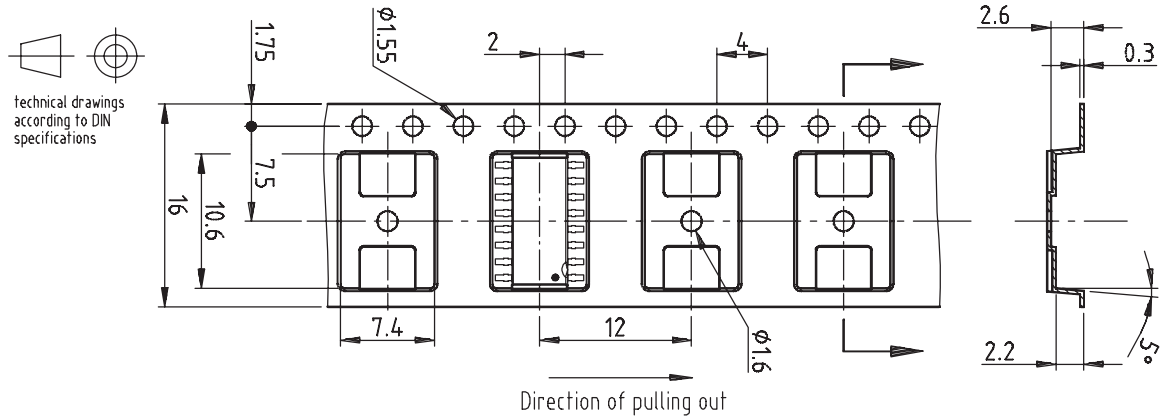
Tape and Reel Packaging for SOT223/10 Mini-couplers

Selected 10-pin mini-couplers are available in tape and reel format. To order surface mount optocoupler on tape and reel, add a suffix "T" after the part number.

The tape is 16 mm and is wound on a 33 cm reel. There are 2000 parts per reel. Taped and reeled 10-pin mini-couplers conform to EIA-481.

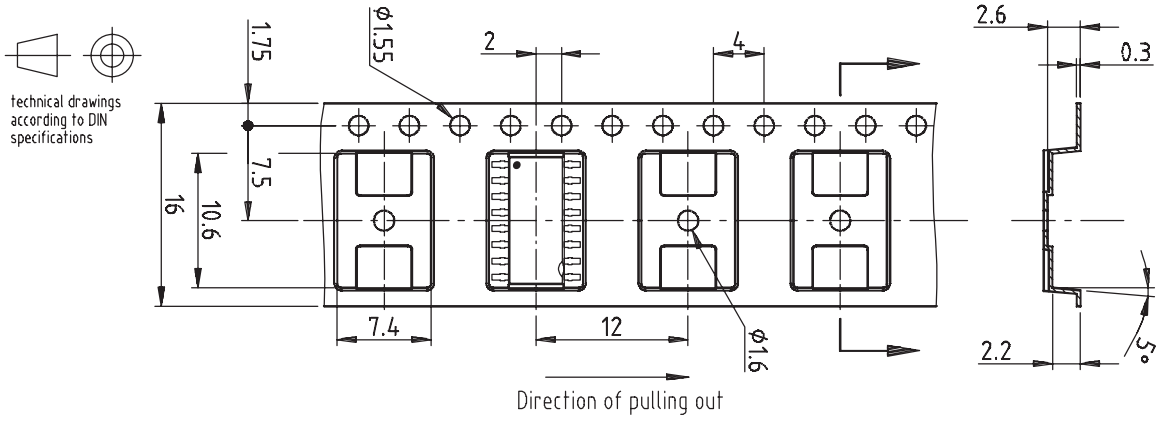


Tape and Reel Packaging for TCMT4100



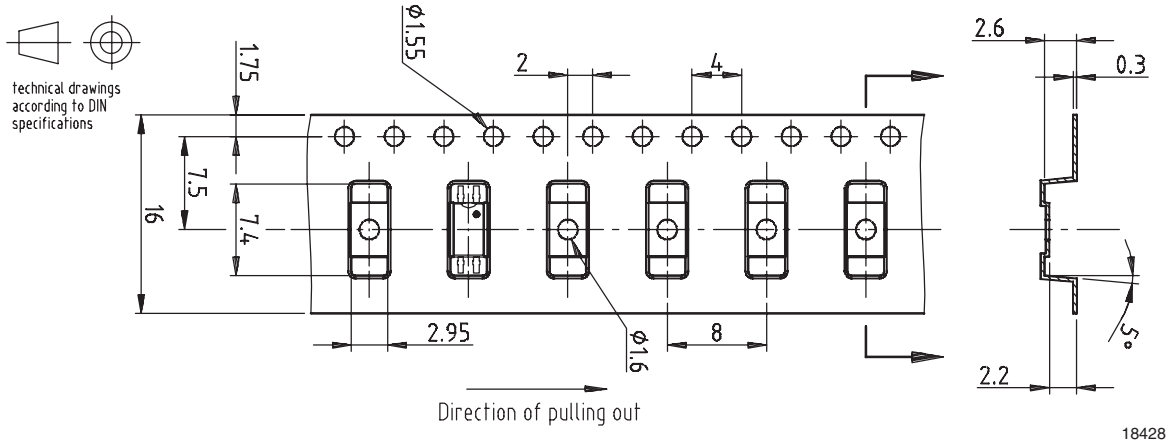
18427

Tape and Reel Packaging for TCMT4600T0

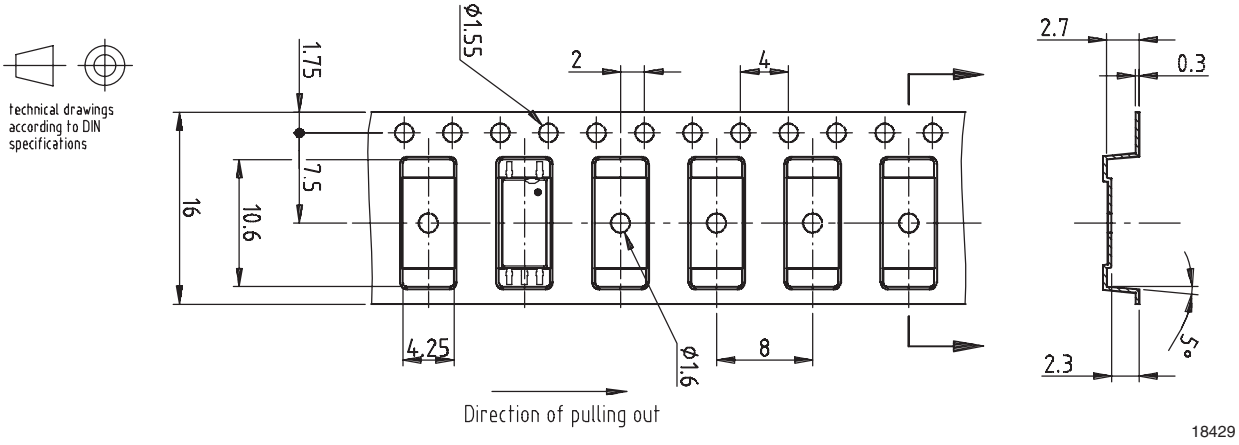


18427_1

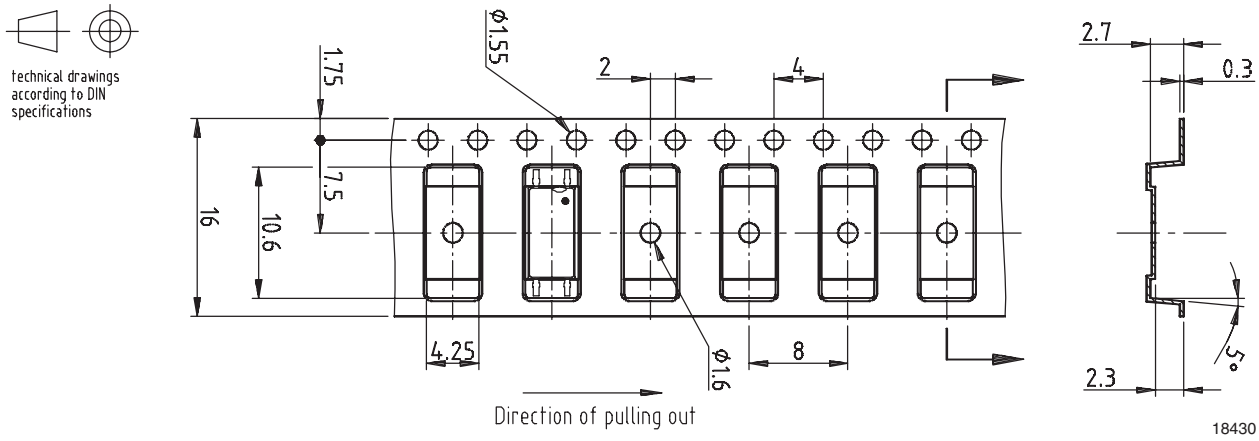
Tape and Reel Packaging for TCMT11xx Series



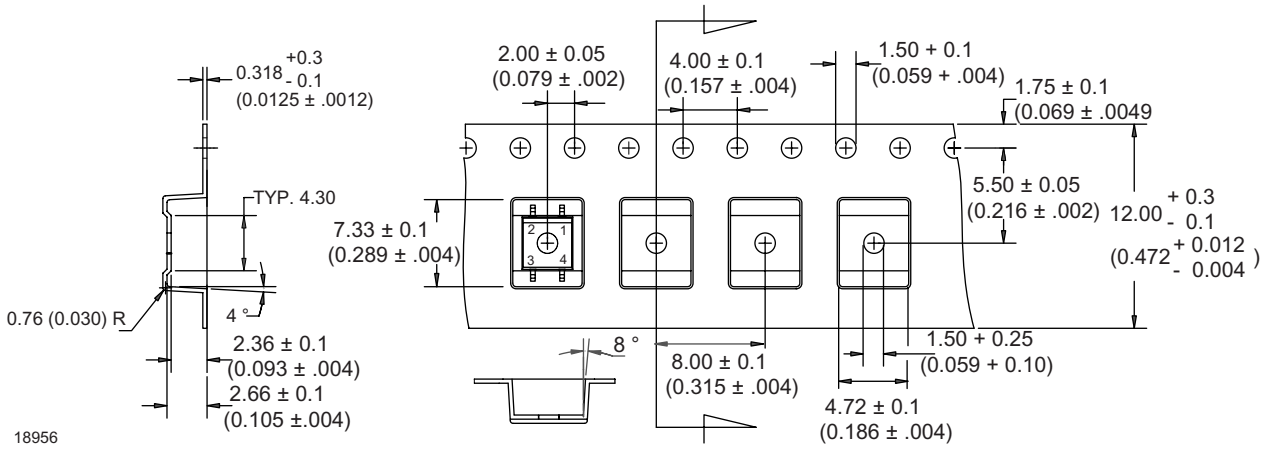
Tape and Reel Packaging for TCLT11xx Series



Tape and Reel Packaging for TCLT1600

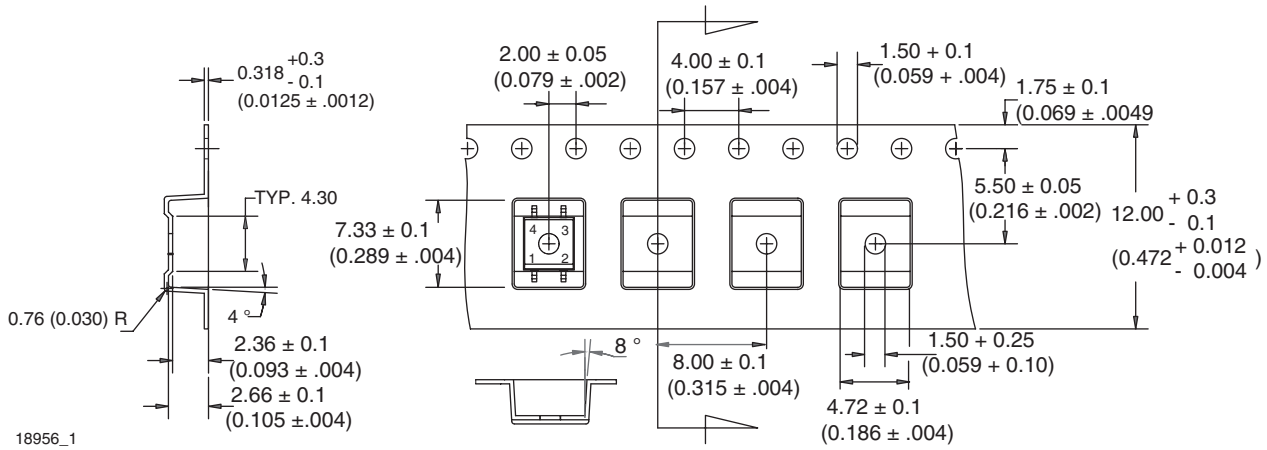


Tape and Reel Packaging 4-pin Miniflat for SFH690ABT/ AT/ BT/ CCT



Tape and Reel Packaging 4-pin Miniflat, 180° rotation

Selected 4-pin miniflats are available in tape and reel format with the part rotated by 180°. To order this version, the tape and reel suffix "T" is augmented by the numerial "3" eg. SFH690BT3. The tape is 16 mm and is wound on a 33 cm reel. There are 2000 parts per reel.



Optocoupler

Test Certificate

Electronic components

Product Services

Certificate No	7081
This is to certify that	Optocoupler types as listed in the schedule to this certificate
Submitted by	Vishay Semiconductor GmbH Theresienstraße 2 D-74072 Heilbronn Germany
	have been tested by BSI in accordance with PS082 and Test Leaflet 5 to BS EN 60065:2002 and IEC 60065:2001 Sub-clauses 13.6, 14.11 and 20.1.4 Details of the scope of the testing are given in BSI Report No 172298 and any addenda thereto.
Signed	Hoyhs
Issue date	23 April 2006
Expiry date	22 April 2008

Attention is drawn to the conditions under which this certificate is issued, namely:

1. The general conditions relating to acceptance of testing (PS082) and the specific conditions (Test Leaflet No TL5 or TL22 as stated above) apply in all respects.
2. This certificate may not be published except in full including any schedule unless permission for the publication of an approved extract has been obtained in writing from the Managing Director of BSI Product Services.
3. This certificate is valid until the expiry date shown above. It shall then be considered cancelled and withdrawn and shall not be used in any way whatsoever.
4. If BSI is satisfied that the manufacturer is marketing what is purporting to be the same model of component but which has been altered or modified or is in any material aspect different from the item tested or is satisfied in respect of evidence discovered by or submitted to it that components purported to be identical to that originally certified are no longer meeting any part of the requirements of the original examination and tests then the certificate will be immediately withdrawn and shall not be used in any way whatsoever.

UKAS TESTING 0135

Prepared by: BSI Product Services Maylands Avenue Hemel Hempstead Hertfordshire HP2 4SQ

Schedule to Test Certificate No	7081
Schedule issue date	23 April 2006
Test Certificate expiry date	22 April 2008
Schedule	Page 1 of 4

Product Services

Optocoupler types:

1. Using coupling system 'A' construction

4N25	CNY75*	K335P*	TCDT1020*	TCDT1101
4N25V	CNY75A	K335PG	TCDT1021	TCDT1102
4N25GV	CNY75B		TCDT1022	TCDT1103
4N26	CNY75C	K1150P*	TCDT1023G	TCDT1100G
4N27		K1150PG		TCDT1101G
4N28	CNY75G		TCDT1020G	TCDT1102G
4N32	CNY75GA	K206P	TCDT1021G	TCDT1103G
4N33	CNY75GB	K207P	TCDT1022G	
	CNY75GC		TCDT1023G	TCDT1110*
4N35*				TCDT1110G
4N35V	CQY80N*		TCDT1100*	
4N35GV	CQY80NG		TCDT1101A	TCDT1120*
4N36	CNY17-1		TCDT1101B	TCDT1121
4N37	CNY17-2		TCDT1101C	TCDT1122
4N38A	CNY17-3		TCDT1101G	TCDT1123
	CNY17-1G		TCDT1101GA	TCDT1124
	CNY17-2G		TCDT1101GB	TCDT1120G
	CNY17-3G		TCDT1101GC	TCDT1121G
				TCDT1122G
				TCDT1123G
				TCDT1124G

2. Using coupling system 'C' construction

K3010P	K3022P	K3020PG
K3011P	K3023P	K3021PG
K3012P	K3010PG	K3022PG
K3020P	K3011PG	K3023PG
K3021P	K3012PG	

As rated below:

1.	Insulation system:	Reinforced
2.	Mains supply voltage:	≤ 250 V r.m.s.
3.	Operating voltage:	≤ 400 V r.m.s.
4.	Peak operating voltage:	560 V peak
5.	Pollution degree:	2
6.	Flammability category:	V-0
7.	Maximum operating temperature:	100 °C

This schedule must be read in conjunction with the test certificate identified above and may not be published except in full including the certificate.

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Schedule to Test Certificate No	7081
Schedule issue date	23 April 2006
Test Certificate expiry date	22 April 2008
Schedule	Page 2 of 4

Product Services

3. Using coupling system 'U' construction

TCET1100	TCET1100G*	TCET1100W**	TCET1102GD
TCET1101	TCET1101G*	TCET1101W**	TCET1103GD
TCET1102	TCET1102G*	TCET1102W**	
TCET1103	TCET1103G*	TCET1103W**	
TCET1104	TCET1104G*	TCET1104W**	
TCET1105	TCET1105G*	TCET1105W**	
TCET1106	TCET1106G*	TCET1106W**	
TCET1107	TCET1107G*	TCET1107W**	
TCET1108	TCET1108G*	TCET1108W**	
TCET1109	TCET1109G*	TCET1109W**	

4. Darlington output

TCED1100	TCED1100G*	TCED1100W**
TCED2100	TCED2100G*	TCED2100W**
TCED4100	TCED4100G*	TCED4100W**

5. Optocouplers a.c. input type:

TCET1600	TCET1600G*	TCET1600W**
TCET2600	TCET2600G*	TCET2600W**
TCET4600	TCET4600G*	TCET4600W**

As rated below:

1.	Insulation system:	Reinforced
2.	Mains supply voltage:	≤ 250 V r.m.s.
3.	Operating voltage:	≤ 400 V r.m.s.
4.	Peak operating voltage:	560 V peak
5.	Pollution degree:	2
6.	Flammability category:	V-0
7.	Maximum operating temperature:	100 °C

This schedule must be read in conjunction with the test certificate identified above and may not be published except in full including the certificate.

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Schedule to Test Certificate No	7081
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Product Services

Using coupling system 'W' construction with a casting material innermold type Hipec Q-6633 manufactured by Dow Corning and moulding material outermold type MG17-060F manufactured by Dexter and rated at a maximum operating temperature of 100 °C.

6. Single channel; DC input; without base
Standard transistor with CTR selection

TCLT1000	TCLT1003	TCLT1006
TCLT1001	TCLT1004	TCLT1007
TCLT1002	TCLT1005	TCLT1008
		TCLT1009

7. Single channel, standard transistor with AC input

TCLT1600

8. Single channel;DC input; with base
Standard transistor with CTR selection

TCLT1100	TCLT1103	TCLT1106
TCLT1101	TCLT1104	TCLT1107
TCLT1102	TCLT1105	TCLT1108
		TCLT1109

9. Single channel; DC input; without base using Darlington transistor

TCLD1000

As rated below:

1.	Insulation system:	Reinforced
2.	Mains supply voltage:	≤ 250 V r.m.s.
3.	Operating voltage:	≤ 400 V r.m.s.
4.	Peak operating voltage:	560 V peak
5.	Pollution degree:	2
6.	Flammability category:	V-0
7.	Maximum operating temperature:	100 °C

This schedule must be read in conjunction with the test certificate identified above and may not be published except in full including the certificate.

Schedule to Test Certificate No	7081
Schedule issue date	23 April 2006
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BSI Product Services

10. Using coupling system 'U' construction and rated at a maximum operating temperature of 110 °C

TCET1110G	TCET1115G	TCET1112GD
TCET1111G	TCET1116G	TCET1113GD
TCET1112G	TCET1117G	
TCET1113G	TCET1118G	
TCET1114G	TCET1119G	

As rated below:

1.	Insulation system:	Reinforced
2.	Mains supply voltage:	≤ 250 V r.m.s.
3.	Operating voltage:	≤ 400 V r.m.s.
4.	Peak operating voltage:	560 V peak
5.	Pollution degree:	2
6.	Flammability category:	V-0
7.	Maximum operating temperature:	110 °C

This schedule must be read in conjunction with the test certificate identified above and may not be published except in full including the certificate.

Prepared by: BSI Product Services Maylands Avenue Hemel Hempstead Hertfordshire HP2 4SQ

Optocoupler

ZEICHENGENEHMIGUNG
MARKS APPROVAL

VISHAY Semiconductor GmbH
Theresienstrasse 2
74072 Heilbronn

ist berechtigt, für ihr Produkt /
is authorized to use for their product

Optokoppler
Optocoupler

die hier abgebildeten markenrechtlich geschützten Zeichen
für die ab Blatt 2 aufgeführten Typen zu benutzen /
the legally protected Marks as shown below for the types referred to on page 2 ff.

Geprüft und zertifiziert nach /
Tested and certified according to

DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01
DIN EN 60950-1 (VDE 0805 Teil 1):2003-03; EN 60950-1:2001
DIN EN 60065 (VDE 0860):2003-01; EN 60065:2002

Aktenzeichen: 422610-4880-0041 / 81492
File ref.:

VDE Prüf- und Zertifizierungsinstitut
VDE Testing and Certification Institute
Zertifizierungsstelle / *Certification*

Ausweis-Nr. 40008929 Blatt 1
Certificate No. *Page*

Weitere Bedingungen siehe Rückseite und Folgeblätter /
further conditions see overleaf and following pages

Offenbach, 2004-01-09
(letzte Änderung/updated 2006-11-06)

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VDE certificates are valid only when published on:
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http://www.vde.com/certificate

VDE VERBAND DER ELEKTROTECHNIK
ELEKTRONIK INFORMATIONSTECHNIK e.V.

VDE Prüf- und Zertifizierungsinstitut Zeichengenehmigung

Ausweis-Nr. / Certificate No. 40008929 | Blatt / page 2

Name und Sitz des Genehmigungs-Inhabers / *Name and registered seat of the Certificate holder*
VISHAY Semiconductor GmbH, Theresienstrasse 2, 74072 Heilbronn

Aktenzeichen / *File ref.*
422610-4880-0041 / 81492 / FG33 / SCT

letzte Änderung / *updated* 2006-11-06

Datum / *Date* 2004-01-09

Dieses Blatt gilt nur in Verbindung mit Blatt 1 des Zeichengenehmigungsausweises Nr. 40008929.
This supplement is only valid in conjunction with page 1 of the Certificate No. 40008929.

Optokoppler
Optocoupler

Typ(en) / *Type(s)*:

1 4 N 25
2 4 N 25 V
3 4 N 25 GV
4 4 N 26
5 4 N 27
6 4 N 28
7 4 N 32
8 4 N 32 V
9 4 N 33
10 4 N 33 V
11 4 N 35
12 4 N 35 G
13 4 N 35 GV
14 4 N 36
15 4 N 37
16 4 N 38 A
17 CNY 17-1
18 CNY 17-2
19 CNY 17-3
20 CNY 17-4
21 CNY 17 G-1
22 CNY 17 G-2
23 CNY 17 G-3
24 CNY 75
25 CNY 75 A
26 CNY 75 B
27 CNY 75 C
28 CNY 75 G
29 CNY 75 GA
30 CNY 75 GB
31 CNY 75 GC
32 CNR 20
33 CQY 80 N
34 CQY 80 NG
35 K 206 P
36 K 207 P

Fortsetzung siehe Blatt 3 /
continued on page 3

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Telefax +49 (0) 69 83 06-555

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Zeichengenehmigung

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Aktenzeichen / *File ref.*
422610-4880-0041 / 81492 / FG33 / SCT

letzte Änderung / *updated* 2006-11-06

Datum / *Date* 2004-01-09

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37 K 335 P
38 K 335 PG
39 K 1150 P
40 K 1150 PG
41 K 3010 P
42 K 3010 PG
43 K 3011 P
44 K 3011 PG
45 K 3012 P
46 K 3012 PG
47 K 3020 P
48 K 3020 PG
49 K 3021 P
50 K 3021 PG
51 K 3022 P
52 K 3022 PG
53 K 3023 P
54 K 3023 PG
55 K 3036 P
56 K 3036 PG
57 K 3053 P
58 TCDT 1100
59 TCDT 1100 G
60 TCDT 1101
61 TCDT 1101 A
62 TCDT 1101 B
63 TCDT 1101 C
64 TCDT 1101 G
65 TCDT 1101 GA
66 TCDT 1101 GB
67 TCDT 1101 GC
68 TCDT 1102
69 TCDT 1102 G
70 TCDT 1103
71 TCDT 1103 G
72 TCDT 1110
73 TCDT 1110 G
74 TCDT 1120
75 TCDT 1120 G
76 TCDT 1121
77 TCDT 1121 G

Fortsetzung siehe Blatt 4 /
continued on page 4

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Zeichengenehmigung

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Aktenzeichen / *File ref.*
422610-4880-0041 / 81492 / FG33 / SCT

letzte Änderung / *updated*
2006-11-06

Datum / *Date*
2004-01-09

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This supplement is only valid in conjunction with page 1 of the Certificate No. 40008929.

78 TCDT 1122
79 TCDT 1122 G
80 TCDT 1123
81 TCDT 1123 G
82 TCDT 1124
83 TCDT 1124 G

Fortsetzung siehe Blatt 5 /
continued on page 5

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Blatt / *page* 5

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Aktenzeichen / *File ref.*
422610-4880-0041 / 81492 / FG33 / SCT

letzte Änderung / *updated* 2006-11-06

Datum / *Date* 2004-01-09

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Gehäusematerial
Case material

Koppelmaterial
Coupling material

Fortsetzung siehe Blatt 6 /
continued on page 6

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Merianstrasse 28, D-63069 Offenbach
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VDE Prüf- und Zertifizierungsinstitut Zeichengenehmigung

Ausweis-Nr. / Certificate No. 40008929 | Blatt / page 6

Name und Sitz des Genehmigungs-Inhabers / *Name and registered seat of the Certificate holder*
VISHAY Semiconductor GmbH, Theresienstrasse 2, 74072 Heilbronn

Aktenzeichen / *File ref.*
422610-4880-0041 / 81492 / FG33 / SCT

letzte Änderung / *updated* 2006-11-06

Datum / *Date* 2004-01-09

Dieses Blatt gilt nur in Verbindung mit Blatt 1 des Zeichengenehmigungsausweises Nr. 40008929.
This supplement is only valid in conjunction with page 1 of the Certificate No. 40008929.

Rastermaß *Grid*	7,62 mm 10,16 mm
Kriechstrecke zw. Sende- + Empfangsteil *Creepage distance betw. input + output*	≥ 7,0 mm ≥ 8,0 mm
Luftstrecke zw. Sende- + Empfangsteil *Clearance distance betw. input + output*	≥ 7,0 mm ≥ 8,0 mm
Isolationsspannung (Scheitelwert) UIORM *Insulation voltage (peak voltage) UIORM*	850 V
Transiente Überspannung UTR Scheitelwert *Transient overvoltage UTR (peak voltage)*	6000 V
Kriechstromfestigkeit *Tracking resistance*	CTI 175 (Isolationsgruppe IIIa) *CTI 175 (Insulation group IIIa)*
Verschmutzungsgrad *Degree of pollution*	2
Klimaklasse *Climatic category*	50/100/21
Betriebstemperaturbereich *Operating temperature range*	-55 °C ... +100 °C
Lagertemperaturbereich *Storage temperature range*	-55 °C ... +125 °C

Fortsetzung siehe Blatt 7 /
continued on page 7

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Aktenzeichen / *File ref.*
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Datum / *Date* 2004-01-09

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This supplement is only valid in conjunction with page 1 of the Certificate No. 40008929.

Sicherheitsgrenzwerte *Safety ratings*	(unter Zugrundelegung der Derating Kurve) *(based on derating curve)*
Strom ISI *Current ISI*	Eingang: 130 mA *Input: 130 mA*
Leistung PSI *Power PSI*	Ausgang: 265 mW *Output: 265 mW*
Temperatur TSI *Temperature TSI*	150 °C
Klassifizierung *Classification*	Lötwärmebeständigkeit: Lötbadmethode 260 °C / 10s *Resistance to soldering heat:* *Solder bath method 260 °C / 10s*
Zusatznorm *Additional standard*	DIN EN 60065 (VDE 0860):1999-10 EN 60065:1998-08 Abschnitt / Clause 10.3; 13; 14.11 DIN EN 60950 (VDE 0805):1997-11 EN 60950:1992 + Änderungen/Amendments:1997 Abschnitt / Clause 2.9; 2.10; 5.2; 5.3
Äußere Kriech- und Luftstrecken *Creepage + clearance distances through air*	≥ 5 mm
Isolierung *Insulation*	Dicke durch Isolierung: ≥ 0,4 mm *Thickness through insulation: ≥ 0,4 mm*
Überspannung (Scheitelwert) *Overvoltage (peak value)*	≥ 6800 V

Fortsetzung siehe Blatt 8 /
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Zeichengenehmigung

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Aktenzeichen / *File ref.*	letzte Änderung / *updated*	Datum / *Date*
422610-4880-0041 / 81492 / FG33 / SCT	2006-11-06	2004-01-09

Dieses Blatt gilt nur in Verbindung mit Blatt 1 des Zeichengenehmigungsausweises Nr. 40008929.
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VDE Prüf- und Zertifizierungsinstitut
VDE Testing and Certification Institute
Fachgebiet FG33
Section FG33

i.V. C i.A. Schmitt

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VDE Prüf- und Zertifizierungsinstitut
Zeichengenehmigung

Ausweis-Nr. / *Certificate No.* 40008929

Beiblatt / *Supplement*

Name und Sitz des Genehmigungs-Inhabers / *Name and registered seat of the Certificate holder*
VISHAY Semiconductor GmbH, Theresienstrasse 2, 74072 Heilbronn

Aktenzeichen / *File ref.*
422610-4880-0041 / 81492 / FG33 / SCT

letzte Änderung / *updated* 2006-11-06

Datum / *Date* 2004-01-09

Dieses Beiblatt ist Bestandteil des Zeichengenehmigungsausweises Nr. 40008929.
This supplement is part of the Certificate No. 40008929.

Optokoppler
Optocoupler

Fertigungsstätte(n)
Place(s) of manufacture

Referenz/*Reference*	
30007609	Shanghai Vishay Semiconductors Opto. Co. Ltd. 501 West Jiang Chang Road Shibei - Shanghai University 200436 HIGH TECH PARK Shanghai CHINA

VDE Prüf- und Zertifizierungsinstitut
VDE Testing and Certification Institute
Fachgebiet FG33
Section FG33

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FPQU2.E76222
Optical Isolators - Component

Optical Isolators – Component

VISHAY SEMICONDUCTOR GMBH E76222
THERESIENSTRASSE 2
74072 HEILBRONN, GERMANY

Coupling system F, Part No. 6N, followed by -135, -136, -137, -138, -139.

Part Nos. CNY21, -21N, DG3831B, may or may not be followed by coupling system G. Part Nos. CNY64, -64A, -64B, may or may not be followed by coupling system H; Part Nos. CNY65 (6496479), -65A, -65B, may or may not be followed by coupling system J; Part No. CNY66, may or may not be followed by coupling system K; Part No. CNY71, may or may not be followed by coupling system B; K Series followed by -3010P, -3010PG, -3011P, -3011PG, -3012P, -3012PG, -3020P, -3020PG, -3021P, -3021PG, -3022P, -3022PG, -3023P, -3023PG, -3036P, -3036PG, may or may not be followed by coupling system C; Part No. K8013P, may or may not be followed by coupling system D; Part No. 6496479.
4N Series followed by -25, -25(G)V, -26, -27, -28, -32, -33, -35, -35(G)V, -36, -37, -38A; Part Nos. CNY75, -A, -B, -C, -GA, -GB, -GC, CQY80N, -NG, K167P, K179P, K1150P, K1150PG, TCDT110., -110.G, -111., -1020(G), -1024(G), -1101, A, -1101B, -1101C, -1101(G)A, -1101(G)B, -1101(G)C, -1120-1124(G), CNY17(G)-1, CNY17(G)-2, CNY17(G)-3, TCDT1100(G), TCDT1102(G), TCDT1103(G) may or may not be followed by coupling system A or S.
System M, Type No. TCMT10, followed by 20, 21, 22, 23, 24, 30, 31, 32, 33 or 34 and Type Nos. MOC205, 206, 207, 211, 212, 213, 215, 216, 217.
System N, Type No. TCDS1001. System O, Type Nos. K3051P, K3051PG, K3052P, K3052PG.

Double Protection, provides 5000 Vac isolation , Coupling System Type U, Part Nos. TCET1100, TCET1101, TCET1102, TCET1102(G)D, TCET1103, TCET1103(G)D, TCET1104, TCET1105, TCET1106, TCET1107, TCET1108, TCET1109, may be followed by G or W, TCET1110 TCET1111, TCET1112, TCET1113, TCET1114, TCET1115, TCET1116, TCET1117, TCET1118, TCET1119, may be followed by G or GD.

Duble protection, provides 3750 Vac isolation , Coupling System Type U Part Nos. HS817, TCET2100, TCET2101, TCET2102, TCET2103, TCET2104, TCET2105, TCET2106, TCET2107, TCET2108, TCET4100, TCET4101, TCET4102, TCET4103, TCET4104, TCET4105, TCET4106, TCET4107, TCET4108, TCET1600, TCET2600, TCET4600, TCED1100, TCED2100, TCED4100, all of which may be followed by suffix letter G or W; Part Nos. HS817GD, HS817B(G), HS817C(G).

Provides 3750 Vac isolation. System P, Types Nos. TCDF 1900 and TCDF 1910.

Double protection, provides 3750 Vac isolation, Coupling System Type U, Part Nos. TCET1100, TCET1101, TCET1102, TCET1102(G)D, TCET1103, TCET1103(G)D, TCET1104, TCET1105, TCET1106, TCET1107, TCET1108, TCET1109, HS817, TCET2100, TCET2101, TCET2102, TCET2103, TCET2104, TCET2105, TCET2106, TCET2107, TCET2108, TCET4100, TCET4101, TCET4102, TCET4103, TCET4104, TCET4105, TCET4106, TCET4107, TCET4108, TCET1600, TCET2600, TCET4600, TCED1100, TCED2100 and TCED4100, all of which may be followed by suffix letter G or W ; Part Nos. HS817GD, HS817B(G), HS817C(G).

Part Nos. CNY74-2, CNY74-2H, CNY74-4, CNY74-4H, K827P, K847P, TCDT2204, K814P, K815P, K817P, K817P1, K817P2, K817P3, K817P4, K817P5, K817P6, K817P7, K817P8, K817P9, K824P, K825P, K827PH, K844P, K845P, K847PH, MCT6, MCT6H, MCT62, MCT62H

Double protection, provides 3750 Vac isolation , Coupling system type M, Part. No. TCMT followed by 1100, 1101, 1102, 1103, 1104, 1105, 1106, 1107, 1108, 1109, 600, 4100, 4600 and Part No. TCMD, followed by 1000 and 4000; Coupling system W, Part. No. TCLT followed by 1000, 1001, 1002, 1003, 1004, 1005, 1006, 1007, 1008, 1009, 1100, 1101, 1102, 1103, 1104, 1105, 1106, 1107, 1108, 1109, 1600, TCLD1000.

Marking: Company name part or series designation, manufacturer's identification code and date code.

Optocoupler

Test Certificate
Electronic components

Product Services

Certificate No	7402
This is to certify that	Optocoupler types as listed in the schedule to this certificate
Submitted by	Vishay Semiconductor GmbH Theresienstraße 2 D-74072 Heilbronn Germany
	have been tested by BSI in accordance with PS082 and Test Leaflet 5 to BS EN 60950-1:2002 and IEC 60950-1:2001 Sub-clauses 2.9.1, 2.10.1, 2.10.7, 2.10.8, 4.7.3.4 (Clause A.2.7) and 5.2.2 Details of the scope of the testing are given in BSI Report No 172298 and any addenda thereto.
Signed	
Issue date	23 April 2006
Expiry date	22 April 2008

Attention is drawn to the conditions under which this certificate is issued, namely:

1. The general conditions relating to acceptance of testing (PS082) and the specific conditions (Test Leaflet No TL5 or TL22 as stated above) apply in all respects.
2. This certificate may not be published except in full including any schedule unless permission for the publication of an approved extract has been obtained in writing from the Managing Director of BSI Product Services.
3. This certificate is valid until the expiry date shown above. It shall then be considered cancelled and withdrawn and shall not be used in any way whatsoever.
4. If BSI is satisfied that the manufacturer is marketing what is purporting to be the same model of component but which has been altered or modified or is in any material aspect different from the item tested or is satisfied in respect of evidence discovered by or submitted to it that components purported to be identical to that originally certified are no longer meeting any part of the requirements of the original examination and tests then the certificate will be immediately withdrawn and shall not be used in any way whatsoever.

Prepared by: BSI Product Services Maylands Avenue Hemel Hempstead Hertfordshire HP2 4SQ

Schedule to Test Certificate No	7402
Schedule issue date	23 April 2006
Test Certificate expiry date	22 April 2008
Schedule	Page 1 of 4

Product Services

Optocoupler types:

1. Using coupling system 'A' construction

4N25	CNY75*	K335P*	TCDT1020*	TCDT1101
4N25V	CNY75A	K335PG	TCDT1021	TCDT1102
4N25GV	CNY75B		TCDT1022	TCDT1103
4N26	CNY75C	K1150P*	TCDT1023G	TCDT1100G
4N27		K1150PG		TCDT1101G
4N28	CNY75G		TCDT1020G	TCDT1102G
4N32	CNY75GA	K206P	TCDT1021G	TCDT1103G
4N33	CNY75GB	K207P	TCDT1022G	
	CNY75GC		TCDT1023G	TCDT1110*
4N35*				TCDT1110G
4N35V	CQY80N*		TCDT1100*	
4N35GV	CQY80NG		TCDT1101A	TCDT1120*
4N36	CNY17-1		TCDT1101B	TCDT1121
4N37	CNY17-2		TCDT1101C	TCDT1122
4N38A	CNY17-3		TCDT1101G	TCDT1123
	CNY17-1G		TCDT1101GA	TCDT1124
	CNY17-2G		TCDT1101GB	TCDT1120G
	CNY17-3G		TCDT1101GC	TCDT1121G
				TCDT1122G
				TCDT1123G
				TCDT1124G

2. Using coupling system 'C' construction

K3010P	K3022P	K3020PG
K3011P	K3023P	K3021PG
K3012P	K3010PG	K3022PG
K3020P	K3011PG	K3023PG
K3021P	K3012PG	

As rated below:

1.	Insulation system:	Reinforced
2.	Mains supply voltage:	≤ 300 V r.m.s.
3.	Working voltage:	≤ 400 V r.m.s.
4.	Peak working voltage:	None
5.	Pollution degree:	2
6.	Flammability –Sub-clause 4.7.3.4 (Clause A.2.7):	Pass
7.	Maximum operating temperature:	100 °C

This schedule must be read in conjunction with the test certificate identified above and may not be published except in full including the certificate.

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Schedule to Test Certificate No	7402
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BSI Product Services

3. Using coupling system 'U' construction

TCET1100	TCET1100G*	TCET1100W**	TCET1102GD
TCET1101	TCET1101G*	TCET1101W**	TCET1103GD
TCET1102	TCET1102G*	TCET1102W**	
TCET1103	TCET1103G*	TCET1103W**	
TCET1104	TCET1104G*	TCET1104W**	
TCET1105	TCET1105G*	TCET1105W**	
TCET1106	TCET1106G*	TCET1106W**	
TCET1107	TCET1107G*	TCET1107W**	
TCET1108	TCET1108G*	TCET1108W**	
TCET1109	TCET1109G*	TCET1109W**	

4. Darlington output

TCED1100	TCED1100G*	TCED1100W**
TCED2100	TCED2100G*	TCED2100W**
TCED4100	TCED4100G*	TCED4100W**

5. Optocouplers a.c. input type

TCET1600	TCET1600G*	TCET1600W**
TCET2600	TCET2600G*	TCET2600W**
TCET4600	TCET4600G*	TCET4600W**

As rated below:

1.	Insulation system:	Reinforced
2.	Mains supply voltage:	≤ 300 V r.m.s.
3.	Working voltage:	≤ 400 V r.m.s.
4.	Peak working voltage:	None
5.	Pollution degree:	2
6.	Flammability -Sub-clause 4.7.3.4 (Clause A.2.7):	Pass
7.	Maximum operating temperature:	100 °C

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Schedule to Test Certificate No	7402
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Product Services

Using coupling system 'W' construction with a casting material innermold type Hipec Q-6633 manufactured by Dow Corning and moulding material outermold type MG17-060F manufactured by Dexter and rated at a maximum operating temperature of 100 °C.

6. Single channel; DC input; without base
Standard transistor with CTR selection

TCLT1000	TCLT1003	TCLT1006
TCLT1001	TCLT1004	TCLT1007
TCLT1002	TCLT1005	TCLT1008
		TCLT1009

7. Single channel, standard transistor with AC input

TCLT1600

8. Single channel;DC input; with base
Standard transistor with CTR selection

TCLT1100	TCLT1103	TCLT1106
TCLT1101	TCLT1104	TCLT1107
TCLT1102	TCLT1105	TCLT1108
		TCLT1109

9. Single channel; DC input; without base using Darlington transistor

TCLD1000

As rated below:

1.	Insulation system:	Reinforced
2.	Mains supply voltage:	≤ 300 V r.m.s.
3.	Working voltage:	≤ 400 V r.m.s.
4.	Peak working voltage:	None
5.	Pollution degree:	2
6.	Flammability -Sub-clause 4.7.3.4 (Clause A.2.7):	Pass
7.	Maximum operating temperature:	100 °C

This schedule must be read in conjunction with the test certificate identified above and may not be published except in full including the certificate.

Prepared by: BSI Product Services Maylands Avenue Hemel Hempstead Hertfordshire HP2 4SQ

Schedule to Test Certificate No	7402
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BSI Product Services

10. Using coupling system 'U' construction and rated at a maximum operating temperature of 110 °C

TCET1110G	TCET1115G	TCET1112GD
TCET1111G	TCET1116G	TCET1113GD
TCET1112G	TCET1117G	
TCET1113G	TCET1118G	
TCET1114G	TCET1119G	

As rated below:

1.	Insulation system:	Reinforced
2.	Mains supply voltage:	≤ 300 V r.m.s.
3.	Working voltage:	≤ 400 V r.m.s.
4.	Peak working voltage:	None
5.	Pollution degree:	2
6.	Flammability -Sub-clause 4.7.3.4 (Clause A.2.7):	Pass
7.	Maximum operating temperature:	110 °C

This schedule must be read in conjunction with the test certificate identified above and may not be published except in full including the certificate.

Prepared by: BSI Product Services Maylands Avenue Hemel Hempstead Hertfordshire HP2 4SQ