ADAS électronique

TRACEABILITY FORM

DOCUMENT FOLLOW-UP

Title:
Titre :

ICV 150

English documentation

Edition: 1 (Document creation - *Création du document*)

Written	by	D. PIMONT	on	10/92	Visa
Revised	by	D. PIMONT	on	10/92	Visa
Approved	by	Ph. DUTIN	on	10/92	Visa

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Edition *Edition*	**Nature of the modifications (key words)** *Nature des évolutions (mots clés)*	**Written** *Rédigé*	**Revised/Approved** *Revu/Approuvé*
9	Bilingual documentation *Documentation bilingue* Rev. H	by D. PIMONT on 98/41 Visa	by Ph. DUTIN on 98/41 Visa
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11	ICV 150 board example of use suppression *Suppression de l'exemple d'utilisation de la carte ICV 150* Wiring layouts suppression *Suppression des plans de câblages* Rev. H	by D. PIMONT on 21/11 Visa	by Ph. DUTIN on 21/11 Visa
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DOCUMENT ARCHIVED
DOCUMENT ARCHIVE
No ☐ Yes ☐ on _____

Δ ed. .. [ ] = Document input/output *(Entrée/sortie modification de la documentation)*
 # ed. .. [ ] = Board new function input/output *(Entrée/sortie nouvelle fonctionnalité du produit)*

NOTES :

SUMMARY

Chapter A Presentation

The **ICV 150** is fully **VME** compatible. It is located in memory space and is fully decoded on 16 Mbytes.

The principle of the **ICV 150** is based on simplicity of use as seen from the **VME** system.

The **ICV 150** continuously scans the channels involved (from channel 0 to channel n) and refreshes a double access RAM.

The measurements are available at all times; the value read is the last refreshed value.

Each channel having been scanned since a maximum of:

(Number of channels - 1) x Acquisition time of each channel

E.g. : **number of channels : 32**

Acquisition time 25 µs i.e. 31 x 25 = 775 µs

Each channel is read at the **ICV 150** base address + (channel n° x 2)

E.g. : Channel 0 Read at Base + 000 high byte and + 001 low byte

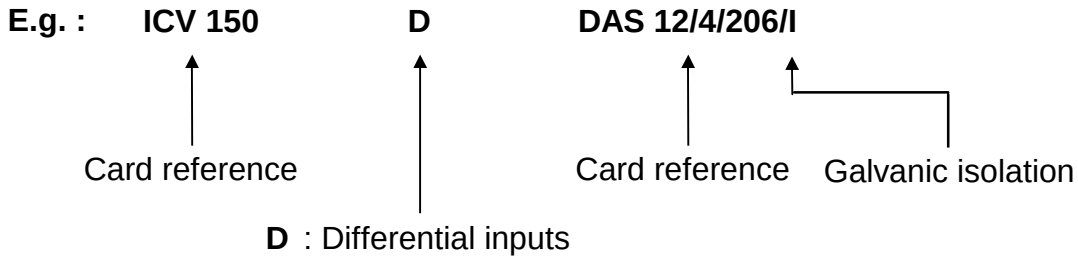
Channel 1 Read at Base + 002 high byte and + 003 low byte

#Δ ed. 12 [

The **ICV 150** exists in a wide range of different versions to meet the requirements of the application. On its own it replaces a large number of specific products.

To choose the most suitable version, it is recommended to refer to the table:

How to order?



There are 32 D inputs resident on the board.

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A.1. Wiring and interconnection

Please consult this heading on our web site or on our CD Rom.

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Chapter B Operation

B.1. Measurements

MEMORY SPACE

The **ICV 150** occupies a memory space of 4 K bytes on the **VME**.

The table below describes the board memory space seen from the **VME**.

ADDRESS	WRITE	READ
XXX FFF	Channel 255 gain code	Channel 255 gain code
XXX FFE		
XXX E07	Channel 3 gain code	Channel 3 gain code
XXX E06		
XXX E05	Channel 2 gain code	Channel 2 gain code
XXX E04		
XXX E03	Channel 1 gain code	Channel 1 gain code
XXX E02		
XXX E01	Channel 0 gain code	Channel 0 gain code
XXX E00		
XXX C00	CS/Nb of channels	
XXX 800	CS/WIT	CS/RIT
XXX 700	CS/STORE	
XXX 600	CS/ARRAY	
XXX 500	CS/EXT	
XXX 400	CS/TRIG	
XXX 300	CS/STOP	Board status
XXX 200	CS/START	
XXX 1FF		LSB channel 255
XXX 1FE	Channel 255 gain code	MSB channel 255
XXX 1FD		LSB channel 254
XXX 1FC	Channel 254 gain code	MSB channel 254
XXX 003	Channel 1 gain code	LSB channel 1
XXX 002		MSB channel 1
XXX 001	Channel 0 gain code	LSB channel 0
XXX 000		MSB channel 0

>>>Note:

All the registers are accessible **IN 16-BIT WORDS ONLY**, in both **READ** and **WRITE**.

B.2. Word read

Board equipped with a programmable gain module

Reading a gain code at the address of the channel involved.

Some modules have a smaller range than the one described below. The characteristics of the module fitted on the board therefore have to be referred to in this case.

HEXA	D3	D2	D1	D0	GAINS
0	0	0	0	0	1
1	0	0	0	1	2
2	0	0	1	0	4
3	0	0	1	1	8

MODULE	MEASUREMENT READ					
VERSION	D15	D14	D13	D12	D11	D0
16 bits	MSB					LSB
14 bits	*	*	MSB			LSB
12 bits	*	*	*	*	MSB	LSB

* : non significant (bits to be masked)

In the case of programmable gain modules, the gains are not read back when acquisition takes place.

CODE

After masquing the non significant bits, the code is in offset binary.

16 BITS

DIGITAL OUTPUT CODE				ANALOG INPUT
F	F	F	F	+ FS - 1 LSB
C	0	0	0	+ 1/2 FS
8	0	0	0	0
4	0	0	0	- 1/2 FS
0	0	0	0	- FS

14 BITS

DIGITAL OUTPUT CODE				ANALOG INPUT
3	F	F	F	+ FS - 1 LSB
3	0	0	0	+ 1/2 FS
2	0	0	0	0
1	0	0	0	- 1/2 FS
0	0	0	0	- FS

12 BITS

CODE SORTIE DIGITALE			ENTREE ANALOGIQUE
F	F	F	+ FS - 1 LSB
C	0	0	+ 1/2 FS
8	0	0	0
4	0	0	- 1/2 FS
0	0	0	- FS

B.3. Gain code programming

This phase has to be carried out with programmable gain modules.

The gain codes can be written in a non volatile RAM, which means that the board does not have to be reconfigured at each power-up.

It is automatically configured for automatic scanning (continuous refresh of the values in the double access RAM at the maximum converter rate).

The following procedures have to be carried out:

- Stop automatic scanning by a CS/STOP
- Program the gain codes required for each channel according to the amplitude of the signals:

E.g. :

CHANNEL	**ADDRESS**	**GAIN CODE**	**GAIN**
Channel 0	XXX 000	6 H	64
Channel 3	XXX 006	2 H	4

When this operation has been completed, the gain codes of each channel are recorded in the **RAM**.

They can be transferred to the **NOVRAM** by the dummy write **CS/STORE**.

The transfer takes **20 ms** : it is recommended **not to take any action** during this time.

At the next power-up, the gains stored in the **NOVRAM** are transferred to the **RAM** memory ; in this way, at each power-up, the board will be set with the gain codes you programmed.

The user can change the gain codes in the **RAM** at any time.

If desired, the original configuration can be reverted to by means of the **CS/ARRAY** function (it is this function that is automatically generated at power-up).

The **CS/START**, **CS/TRIG** and **CS/EXT** functions are disabled during the **RAM** ⇒ **NOVRAM** transfer.

They are automatically executed when the transfer is completed.

The gains in the **NOVRAM** can only be changed a maximum of 10,000 times.

The **ICV 150** with programmable gain modules is thus extremely simple to implement.

B.4. Gain code read back

The gain codes of each channel can be read back at the address XXX E00 + (channel number x 2 + 1).

E.g. :	channel 0	XXX E01	channel	0 gain code read
	channel 1	XXX E03	channel	1 gain code read
	channel 255	XXX FFF	channel 255	gain code read

The gain codes can only be read back if the board has stopped scanning.

In trigger mode at the end of scanning, the conversion value can therefore be read in words at the address:

BASE + (Channel N° x 2)

and the corresponding gain at the address:

BASE + E00 + (Channel N° x 2 + 1)

B.5. Board status bit

A board status bit is available for reading at all times at the address **XXX 300H**.

D0 = 0 if the board is stopped

D0 = 1 if the board is scanning

B.6. Choice of number of channels to be scanned

The number of channels to be scanned can be defined either via software or by straps on **ST3**.

In the channel register at **XXX C00H** bit **D8** validates either the channel register or the strap:

D8 = 0 the **ICV 150** scans the number of channels contained in the register.

D8 = 1 the **ICV 150** scans the number of channels defined by the straps on **ST3**.

In the case of a number of channels defined by straps, the modulo is 32.

In the case of the number of channels being selected via software, the board will be able to scan any channels from 1 to 128.

A write in the register XXX C00H can only be performed if the board is stopped. The write in the register XXX C00H can only be performed in 16-bit access.

B.7. Acquisition modes

AUTOMATIC ACQUISITION MODE

Programmable gain modules

At power-up or on an initialization (INIT), the board automatically loads the RAM with the gain codes from the **EEPROM** memory, then each channel is converted with the corresponding gain value.

The measurement is stored in the double access **RAM**.

The gain code does not appear in the format.

START - STOP MODE

As the board is set to automatic scanning at power-up, acquisition can be stopped by a **CS/STOP** which enables the gain settings to be changed (programmable gain modules only). The **CS/START** command switches the board back to automatic scanning.

TRIGGER MODE

This operating mode can be triggered:

- either by software CS/TRIG, in which case we have a "SOFT" TRIGGER
- or by the connector "J3" in the form of impulse on the TRIG/ pin (TTL signal min. width 50 ns active on the rising front, idle state “1” ).

PROCEDURE FOR BOTH CASES

- "SOFT" TRIGGER

After a **CS/STOP** (write at address XXX 300H) the board no longer scans the channels.

On a **CS/TRIG**, the board scans the "n" channels requested then positions an end of conversion bit Do at "0", accessible by **CS/RIT** at the low address + 800H and/or generates an interrupt to the **VME**.

This bit will be cleared when the **CS/RIT** register is read or the interrupt is acknowledged.

The channels are no longer refreshed.

The board is waiting for a new command.

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- EXTERNAL TRIGGER

Do a **CS/EXT** at XXX500H to "set" the board.

The first rising front of the external clock triggers the acquisitions (20 measurements in the diagram)

At the end of the sequence, an interrupt can be sent ITC

To stop this operating mode, do a **CS/STOP**.

<u>The diagram below illustrates operation</u>:

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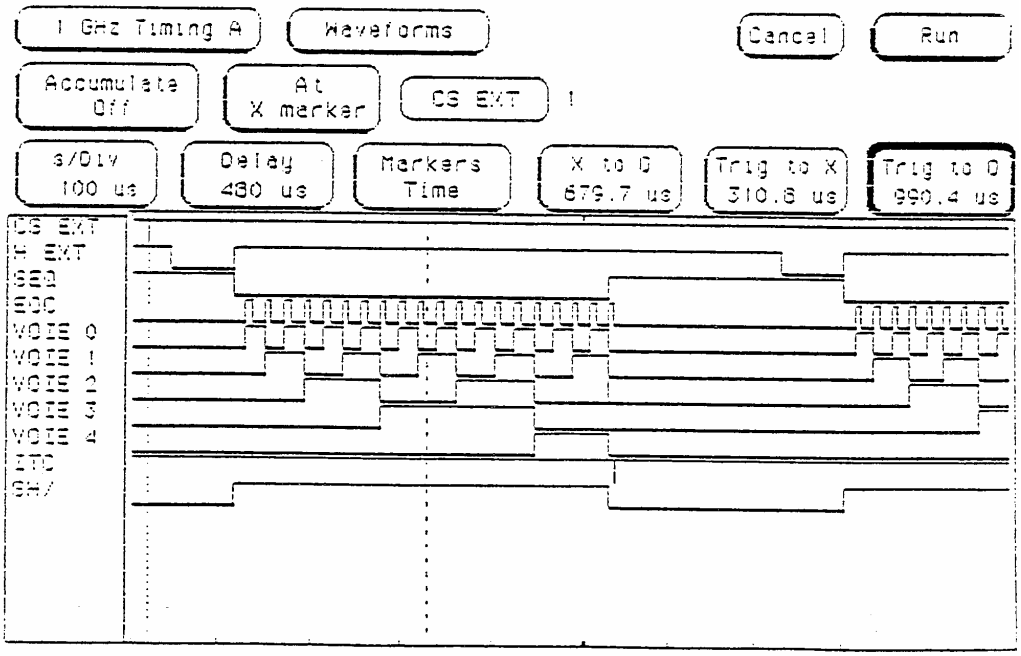
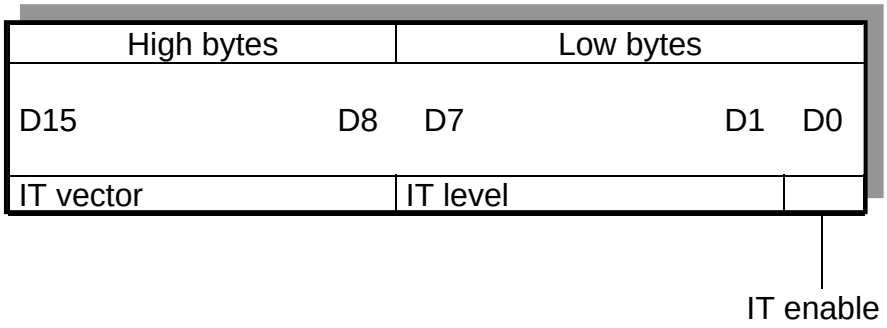


B.8. Signals and commands

CS/RAM	Channel read command.
CS/CG	Programmable gain code write command.
CS/STORE	Command to store RAM programmable gain codes in EEPROM (dummy read or write).
CS/ARRAY	Command to recall programmable gain codes from EEPROM to RAM (dummy read or write). This command is automatic at power-up or on reset.
CS/STOP	Command to stop automatic channel scanning (write in XXX 300H). Reading D0 at this address gives the board status.
	External clock invalidation
CS/START	Command to start automatic scanning with continuous refresh of the values (dummy read or write).
CS/TRIG or TRIG J3	Command to start automatic channel scanning (no refresh) generating an interrupt at the end of scanning (dummy read or on write) for the software.
CS/EXT	Command validating the external clock present on J3.
INIT/	Board initialization command by signal set to zero on J3.
CS/RIT	End of conversion bit (D0) state read. Acknowledgement is made when the register is read or by the interrupt D0 = "0" End of conversion.
CS/WIT	Write of vector, level and interrupt enable.
CS/CHANNELS	Programming of the number of channels to be scanned (write only).

VECTORIZED INTERRUPT

Write of vector, level and interrupt enable:



- The vector is written in positive logic
  E.g. : Vector = 50H
- The interrupt level is written in negative logic
  E.g. : IT4 we position Bit **D7, D6, D5 = 1**
  Bit **D4 = 0**
  Bit **D3, D2, D1 = 1**
- Interrupt enable Bit D0 = 1
- Interrupt disabled Bit D0 = 0

Overall example : 50FB H write at address CS/WIT
IT vector = 50H
IT level = IT2
IT enable

The vector, level and enable can be changed at any time.
At power-up or on initialization, the register is set to "0".

B.9. Case of galvanic isolation

The **ICV 150** can provide galvanic isolation of the analog signals with respect to the computer.

This version is greatly appreciated when the environment is disturbed.

A DC/DC converter provides the analog power supply to the isolated part.

The HP 2531 photocouplers provide isolation of the multiplexing control.

The acquisition module has his own galvanic isolation.

B.10. LEDs

Two leds, **LED S** and **LED A** indicate the state of the board.

LED S is lit when the board is scanning the channels.

LED A is lit when the **VME** is accessing the double access RAM.

Chapter C Implementation

C.1. Installation

The user will beforehand read the following document:

GENERAL INSTRUCTIONS FOR IMPLEMENTING ADAS PRODUCTS
INSTRUCTIONS GENERALES DE MISE EN OEUVRE DES PRODUITS ADAS

The frame must be turned off before plugging in the product.

C.2. Init on power-up

It is necessary to:

- Write CS/STOP on base +300H to stop the board scan
- Program on NOVRAM the requested gains codes
- Do CS/STORE to save gains codes on NOVRAM
- Program channels number or channels number mode by CS/CHANNELS strap (base +XXXC00H)
- Do a CS/START or CS/TRIG according to the requested running mode

C.3. VME interface

VME INTERFACE USED BY THE ICV 150

PIN P1	COLUMN A MNEMONIC SIGNAL	COLUMN B MNEMONIC SIGNAL	COLUMN C MNEMONIC SIGNAL
1	D00	N.U.	D08
2	D01	N.U.	D09
3	D02	N.U.	D10
4	D03	BG0IN/ *	D11
5	D04	BG0OUT/	D12
6	D05	BG1IN/ *	D13
7	D06	BG1OUT/	D14
8	D07	BG2IN/ *	D15
9	GND	BG2OUT/	GND
10	SYSCLK	BG3IN/ *	N.U.
11	GND	BG3OUT/ *	N.U.
12	DS1/	N.U.	SYSRESET/
13	DS0/	N.U.	LWORD/
14	WRITE	N.U.	AM5
15	GND	N.U.	A23
16	DTACK/	AM0	A22
17	GND	AM1	A21
18	AS/	AM2	A20
19	GND	AM3	A19
20	IACK	GND	A18
21	IACKIN/ *	N.U.	A17
22	IACKOUT/	N.U.	A16
23	AM4	GND	A15
24	A07	IRQ7/	A14
25	A06	IRQ6/	A13
26	A05	IRQ5/	A12
27	A04	IRQ4/	A11
28	A03	IRQ3/	A10
29	A02	IRQ2/	A09
30	A01	IRQ1/	A08
31	N.U.	N.U.	N.U.
32	+ 5V	+ 5V	+ 5V

N.U. : *Not Used*

***** : *Joined on the board*

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C.4. Coupler bus P2

INTERFACE WITH "COUPLEURS" BOARDS P2

The **ICV 150** can be associated with « coupler » boards to make up a data acquisition system with more than 32 D channels.

The “coupler” boards perform the functions of conditioning, multiplexing, galvanic isolation, etc.

The ICV 150 – “coupler” board connections are achieved by means of a SPECIFIC “P2” BUS.

The "P2" bus contains 5 groups of signals:

- Analog bus
- Gain code bus
- DATA bus
- Control signals
- Channel address bus

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ADAS SPECIFIC "P2" BUS

I/O BUS

PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC
A32	GND ANA.ISO		C32	GND ANA.ISO
A31	GUARD		C31	GUARD
A30	(-)	Group 0	C30	(+)
A29	(-)	Group 1	C29	(+)
A28	(-)	Group 2	C28	(+)
A27	(-)	Group 3	C27	(+)
A26	(-)	Group 4	C26	(+)
A25	(-)	Group 5	C25	(+)
A24	(-)	Group 6	C24	(+)
A23	(-)	Group 7	C23	(+)
A22	N.C.		C22	N.C.
A21	G2		C21	G3
A20	G0	GAIN CODE	C20	G1
A19	0V		C19	0V
A18	DATA E		C18	DATA F
A17	DATA C		C17	DATA D
A16	DATA A		C16	DATA B
A15	DATA 8		C15	DATA 9
A14	DATA 6	DATA BUS	C14	DATA 7
A13	DATA 4		C13	DATA 5
A12	DATA 2		C12	DATA 3
A11	DATA 0		C11	DATA 1
A10	ST (S/H ou INC)	CONTROLS	C10	EOC
A09	N.C.		C09	MACQ
A08	A7		C08	A06
A07	A5	CHANNEL	C07	A04
A06	A3	SELECT	C06	A02
A05	A1		C05	A00
A04	0V		C04	0V
A03	0V	POWER	C03	0V
A02	+ 5V		C02	+ 5V
A01	+ 5V	SUPPLY	C01	+ 5V

Row "B" is free for the 32-bit **VME** extension.

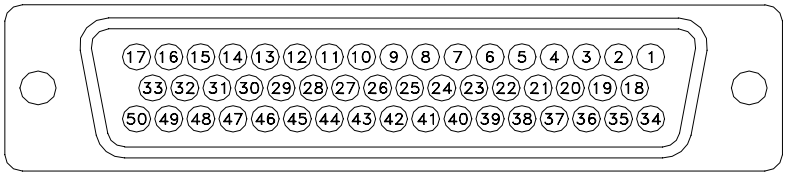
C.5. "J1" ; "J2" analog inputs

>>>Connection terminal for ICV 150 with 32 differential inputs

The inputs are made by 2 "D" type 50-point female connectors.
E.g. SUB D Male 50-point for flat cable
ODU - Ref. 620-061-035-050000
or **CONNEC -** Ref. CDS 50S

Attention : T & B et 3M not usable

J1
DD50S



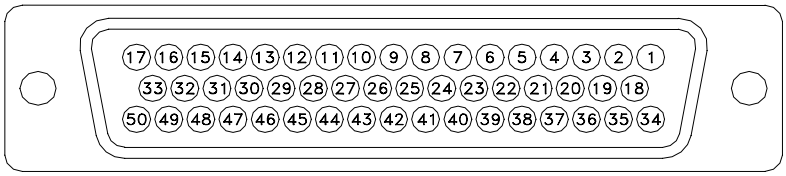
PIN	SIGNAL
1	NC
2	GND
3	GND
4	GND
5	GND
6	GND
7	GND
8	GND
9	GND
10	GND
11	GND
12	GND
13	GND
14	GND
15	GND
16	GND
17	GND

PIN	SIGNAL
18	+ V00
19	+ V01
20	+ V02
21	+ V03
22	+ V04
23	+ V05
24	+ V06
25	+ V07
26	+ V08
27	+ V09
28	+ V10
29	+ V11
30	+ V12
31	+ V13
32	+ V14
33	+ V15

PIN	SIGNAL
34	- V00
35	- V01
36	- V02
37	- V03
38	- V04
39	- V05
40	- V06
41	- V07
42	- V08
43	- V09
44	- V10
45	- V11
46	- V12
47	- V13
48	- V14
49	- V15
50	NC

J2

DD50S



PIN	SIGNAL
1	NC
2	GND
3	GND
4	GND
5	GND
6	GND
7	GND
8	GND
9	GND
10	GND
11	GND
12	GND
13	GND
14	GND
15	GND
16	GND
17	GND

PIN	SIGNAL
18	+ V16
19	+ V17
20	+ V18
21	+ V19
22	+ V20
23	+ V21
24	+ V22
25	+ V23
26	+ V24
27	+ V25
28	+ V26
29	+ V27
30	+ V28
31	+ V29
32	+ V30
33	+ V31

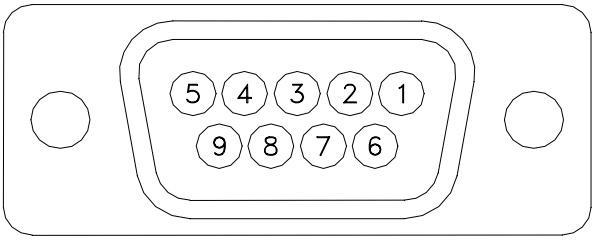
PIN	SIGNAL
34	- V16
35	- V17
36	- V18
37	- V19
38	- V20
39	- V21
40	- V22
41	- V23
42	- V24
43	- V25
44	- V26
45	- V27
46	- V28
47	- V29
48	- V30
49	- V31
50	NC

C.6. "J3" external command signals

The inputs are made via a "D" type 9-point female connector.

J3

DE9S



PIN	SIGNAL	PIN	SIGNAL
1	Earth		
		6	Earth
2	Earth		
		7	Earth
3	TRIGGER/		
		8	Earth
4	TRIGGER/		
		9	Earth
5	INIT/		

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C.7. Straps

>>>FACTORY STRAPS

ST7	Position B, D	32 differential inputs mode
ST6	Position AB	Differential mode
ST5	Position AB	Factory strap
ST4		Factory strap

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>>>CUSTOMER INDIVIDUALIZATION

ST3 Position B, D Modulo 32 channel number

ST3	H	G	F	E	D	C	B	A
Nb CHANNELS	32	64	96	128	156	192	224	256

Front panel side — Bus side

SW1 *Board low address*
SW2
SW3

SW3			
8 A23	4 A22	2 A21	1 A20
SW2			
8 A19	4 A18	2 A17	1 A16
SW1			
8 A15	4 A14	2 A13	1 A12

A strap implies a logic "1".

The **ICV 150** occupies a memory space of 4 K bytes on the **VME**.

ST1 Modified address codes

- fitted : supervisor only standard access (AM 3DH)
- not fitted: non privileged standard access (AM 39H)

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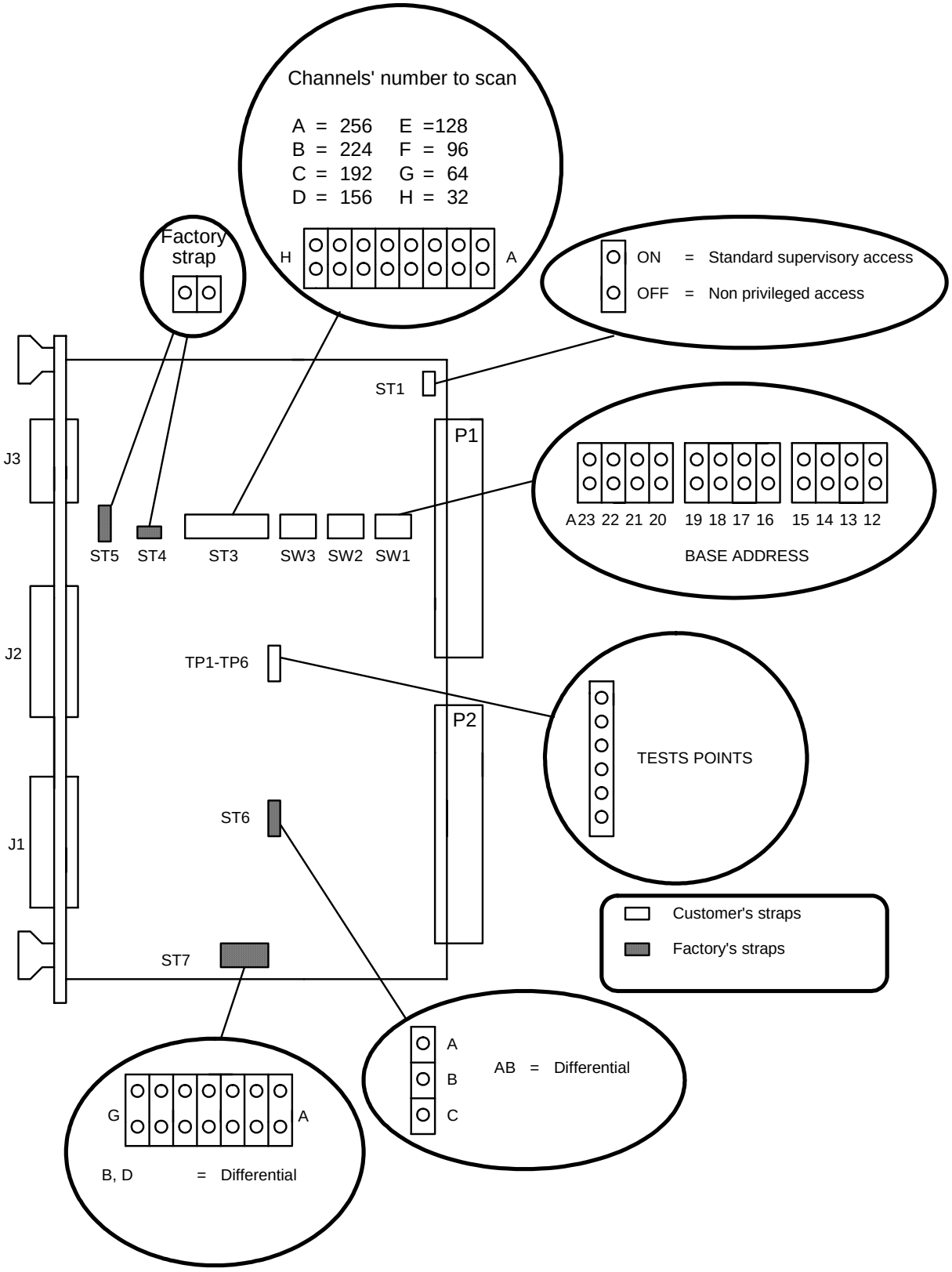

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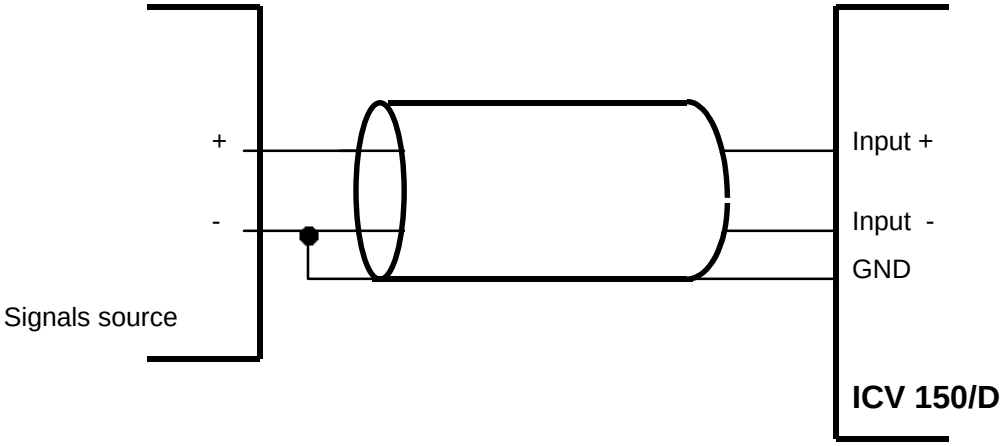
C.8. How to connect the inputs

Differential input



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>>>Notes :

- In order to avoid noise problems, it is strongly advised to short ± GND with non used inputs.

- In differential mode, there are « 3 wires » +, - and GND

  ⇒ Do not forget to wire all three.

- If single using, connect input (-) to GND

#Δ ed. 9 & 12]

Chapter D Coupler boards & terminal block

D.1. Coupler board

The **ICV 150** is able to manage 128 single or differential analog inputs.

It perform multiplexing of the first 32 D channels itself.

The extension boards described below can be coupled via a "P2" bus:

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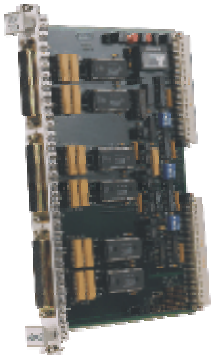


ICV 110 D

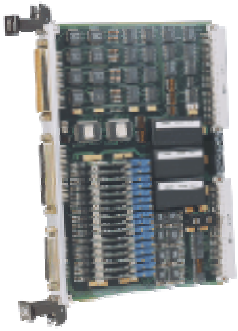
48 differential inputs, protected multiplexers.

ICV 110 DI

Galvanically isolated version of the **ICV 110 D**.

ICV 117

Coupler for **BCI** series



>>>NOTE :

When coupler boards of the **ICV 117** type are used, the channels resident on the **ICV 150** may not be used and **ICV 117** board channels may want to be placed starting from channel 0. In this case:

- remove all the straps on ST7,
- place the analog outputs on group 0 of "P2",
- address the coupler boards to decode starting from channel 0.

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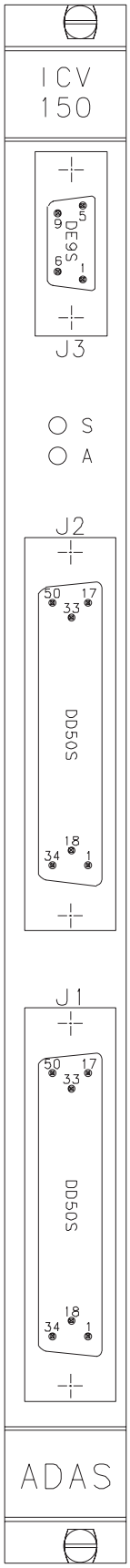
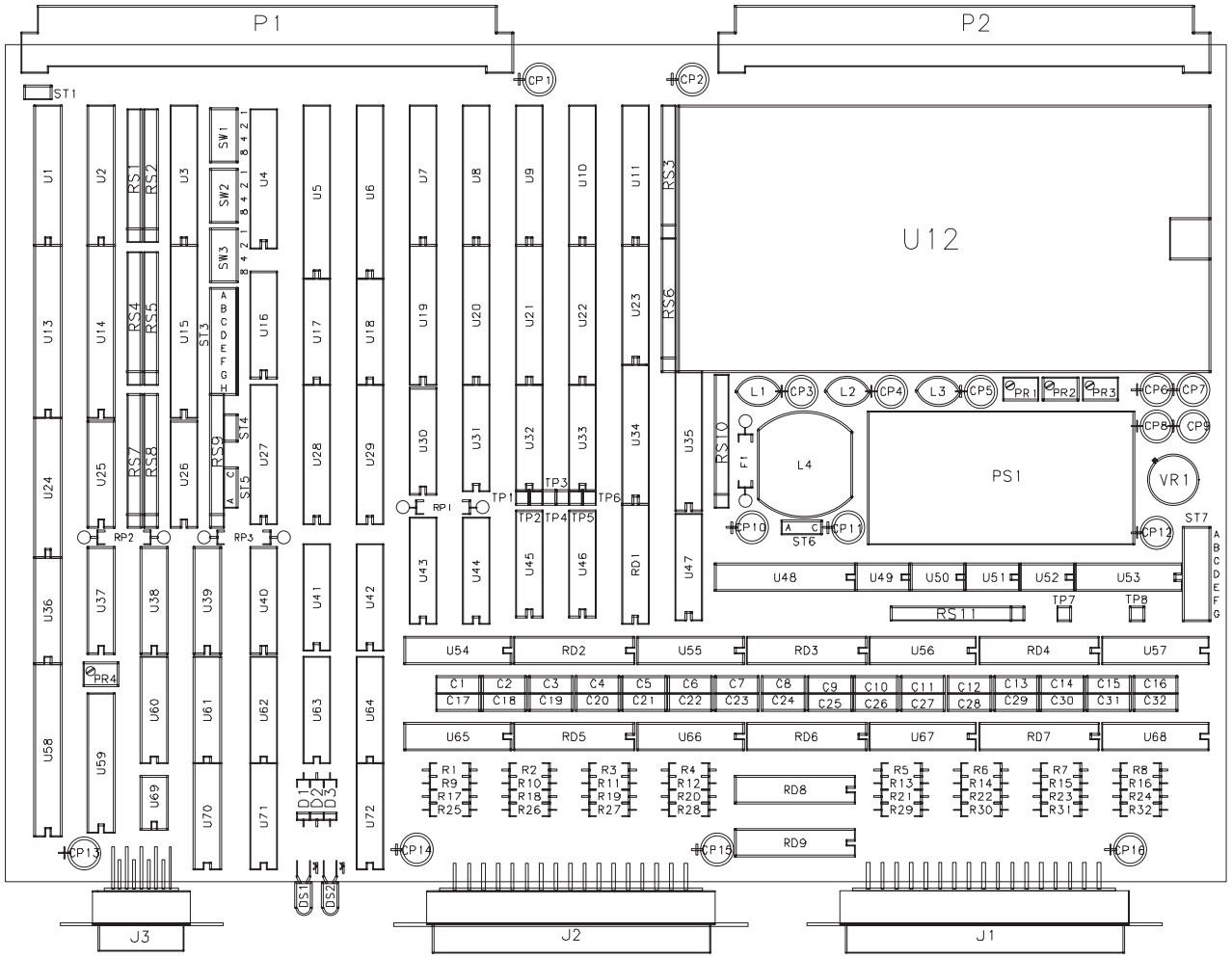
Appendix

FRONT PANEL DRAWING

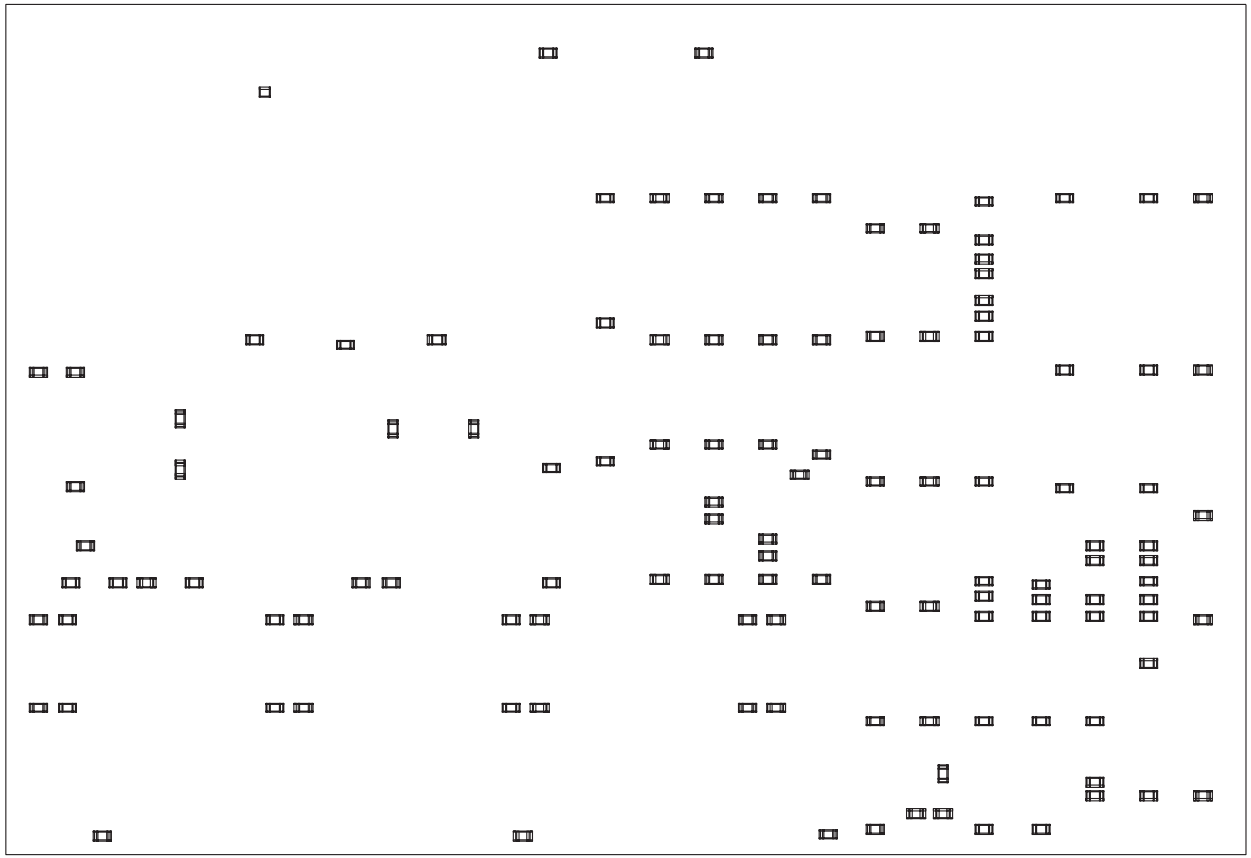
EQUIPMENT LAYOUT



MODIFICATION CONSTRUCTEUR A ORIGINAL	ECHELLE 1 1/1	MAT. : AG3 ENSEMBLE : VME	NOM	ADAS Electronique 9, rue Georges Besse 78330 FONTENAY LE FLEURY Tel : (1) 30 58 90 09
		ICV150		DATE 06/06/1995
		FAV CARTE		NUMERO



MODIFICATION CONSTRUCTEUR	ECHELLE 1	MAT. : FR04	NOM MAO	ADAS Electronique
A ORIGINAL	1/2	ENSEMBLE :		9, rue Georges Besse
		ICV150		78330 FONTENAY LE FLEURY
				Tel (1) 30 58 90 09
H REVISION		PLAN D'EQUIPEMENT		DATE : 28/07/1992
		CARTE CUIVRE NU		NUMERO :



MODIFICATION CONSTRUCTEUR A ORIGINAL H REVISION	ECHELLE 1	MAT. : FR04	NOM MAO	ADAS Electronique 9, rue Georges Besse 78330 FONTENAY LE FLEURY Tel : (1) 30 58 90 09
	2/2	ENSEMBLE :		
	ICV150			
	PLAN D'EQUIPEMENT CARTE CUIVRE NU			DATE : 28/07/1992 NUMERO :