Noise-Margin and Interface Implications of Various Emitter-Coupled-Logic Families Operating at Five Volts

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ABSTRACT

The effects of five-volt operation on the noise margin and interface compatibility of the three most common emitter-coupled logic (ECL) families is examined. A basic discussion of the fundamental differences between the ECL families is given, prefaced by a generic ECL circuit structure description. Noise margin of ECL devices is defined in terms of the input and output logic thresholds. The effects of five-volt operation on the logic thresholds is examined for each family. The noise margin implications of interfacing inhomogeneous ECL devices in five-volt systems are presented. Recommendations are given for preserving noise margin in such cases.

INTRODUCTION

Many high-speed fiber optic local area networks are being designed with transmitter and receiver modules (or transceivers) that use ECL input and output signal levels. The 259002-1 transmitter, 259003- I receiver and 502448/502543 transceivers manufactured by AMP fall` into this category. These devices are primarily used with a single five-volt power supply. This is because the majority of the logic surrounding the modules is transistor-transistor logic (TTL). Only the high-speed serial interfaces of the transmitter and receiver need be ECL. Most FDDI chip sets are designed to operate with a single five-volt supply.

The most common ECL families, 10K, 10H and 10OK, each have different (in some cases overlapping) power supply specifications. The effects of operating these families under conditions that are not optimum or fully specified for each family is the subject of this paper. Specifically, interoperation of the various ECL families with a common, positive five-volt, power supply is examined.

This paper discusses the basic circuit design common to all ECL families, illustrating how the ECL voltages are generated, and why they are referenced to V_{cc}. The basic differences between the three families are presented. These differences ultimately determine the compatibility of each family. Finally, the implications of operating the various ECL families with each other in a common five-volt system are discussed.

ECL CIRCUIT STRUCTURE

All ECL functions are based upon switching current between the collectors of NPN emitter-coupled differential amplifiers, hence the name emitter-coupled logic. ECL output voltages are generated by these circuits with reference to V_{cc}, the positive supply bus. When two ECL circuits are to share data, it is extremely important that their positive supply busses are at the same potential. A shift in V_{cc} between the two circuits produces a corresponding shift in the logic levels of the two circuits. This is why ground is specified as the positive supply bus for ECL systems, since it is typically the most stable, and the lowest impedance, supply bus in a system.

Each ECL family is based upon the basic NPN emitter-coupled limiting differential amplifier. The primary difference between the logic families, not including speed and propagation delay, is the manner in which the current and voltage references are generated to bias and regulate the operation of the basic differential amplifier (current switch).

The basic ECL gate is an OR/NOR gate as shown in Figure 1. One input of the differential amplifier is biased with a reference voltage V_{BB} which is nominally at 1/2 of the peak-to-peak logic swing. The other half of the differential amplifier consists of two or more NPN transistors connected collector-to-collector and emitter-to-emitter. The bases of these transistors are the logical OR/NOR inputs. The logic function is initiated by switching the common emitter current through the collector loads of either half of the differential amplifier. The collector voltages are buffered by emitter followers to the outside world. Since differential circuits automatically provide the complementary function, both OR and NOR outputs are available.

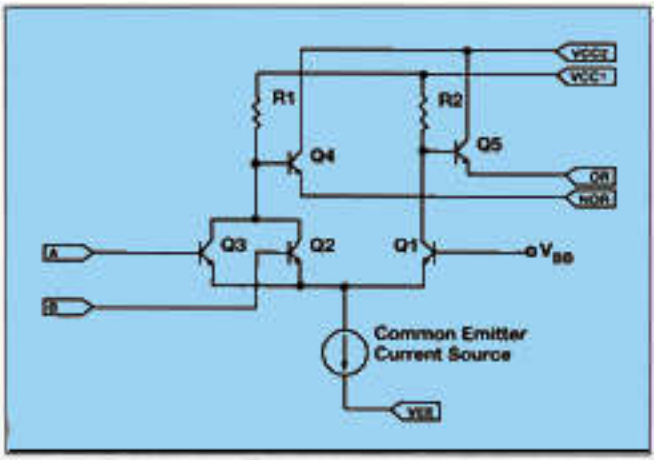

Figure 1. The basic ECL gate is an OR/NOR gate based on a differential amplifier circuit.

One notable exception to this basic circuitry is the line receiver used to sense signals over long lines. This device uses both sides of the differential amplifier as data inputs. The V_{BB} voltage is available externally if needed. This allows for the sensing of logic levels that may not be centered about V_{BB} and are attenuated by long transmission lines. This circuit will provide ECL output levels as long as the input voltage differential is greater than about 150 mV and the common-mode input voltage is within the common-mode range of about 2 volts. This ability to accept differential drive and provide ECL output levels allows the line receiver to overcome many of the problems that can arise in ECL systems because of supply bus differences. As will be presented later, these same features eliminate the problems of interfacing the different ECL families.

ECL FAMILY CHARACTERISTICS

10K ECL Family

Most 10K series ECL use a resistor as the common emitter current source. Due to this, the logic O output voltage can depend upon the input voltage level. Also, the logic O output voltage is a function of the power supply output. Some manufacturers' 10K devices use a transistor current source for the common emitter source. This stabilizes the logic O output voltage with respect to the input voltage level. V_{BB} is generated by a diode/resistor reference and is also subject to power supply variations. The logic 1 output voltage has about 1 V_{BE}'s worth of temperature drift, as it essentially is just one diode drop below V_{cc}. The logic O output voltage temperature characteristic is about 1/2 that of the logic 1. The V_{BB} temperature characteristic divides the difference between the logic 1 and the logic O to ensure equal noise margin for sensing both ECL levels. 10K ECL is designed to operate at –5.2 volts. This supply voltage was chosen as a balance between maximizing noise margin (which decreases with decreasing voltage) and minimizing power dissipation (which increases with increasing voltage).

10H ECL Family

The 10H series incorporates a Widlar bandgap reference generator which provides two improved voltage references to the basic ECL gate. The first voltage is referenced from V_{FF} and is used to bias a transistor current source serving as the common emitter current source of the differential amplifier. The second voltage is referenced to V_{cc} and provides the V_{BB} voltage. These two voltages are relatively immune to power supply changes of ±5%. This voltage regulation improves the noise margin of the 10H family by decreasing the power supply dependence of the logic O. Although the bandgap reference has the ability to provide temperature compensation as well, an additional resistor adds a V_{BE} tracking component to the reference voltages. This is done so the temperature [racking rates of the 10H family match those of the 10K family, making these two families 100% compatible. 10H ECL is specified for –5.2 volts (±5%) to maintain full compatibility with 10K and also permit operation at 5.0 volts without a loss of noise margin.

100K ECL Family

The 100K series also uses the Widlar bandgap reference as a dual-bias generator. The bias voltages are nearly fully temperature compensated, resulting in V_{BB} and logic O levels

that are very nearly independent of' power supply and temperature variations. A compensating network in the differential amplifier compensates the temperature drift of the logic 1 output level. The lOOK family is designed for very high speed operation. For the integrated devices to be operated in their maximum transition frequency (f_T) range and to keep impedances low for maximum speed, they must be operated at a relatively high current level. This increases the power dissipation of the circuit. To control overall power dissipation and die temperatures, I00K ECL is specified for use with –4.2- to –4.2-volt power supplies, instead of –5.2 volts as in the I0K and I0H families. Most l0K ECL manufacturers do not extend their specifications to operation at 5 volts

The logic levels provided by each ECL family are nominally compatible, provided that each family is operated within its own specifications. However, unless multiple power supplies are provided, the different power supply requirements of each family alone will force the operation of one or more of the different ECL families in a system to be operated at a power supply voltage that is not within its specifications. The dissimilar temperature-tracking rates of each family can provide more incompatibilities if they are not properly understood and compensated.

As mentioned earlier, most applications for the ECL transmitter, receiver and transceiver modules are in network systems which me largely TTL, and therefore are +5-volt-based systems. One obvious problem with this application is that the system is designed with the negative supply as ground, not the positive supply as specified for ECL. This places special requirements upon the system designer to regulate and control the positive supply carefully to avoid adversely affecting the ECL levels. Both 10K and 100K ECL specifications are not guaranteed by the manufacturers when operated from 5.0 volts. The implications of operating and mixing ECL families in +5. O-volt-based systems must be understood by the designer for reliable logic operation and are the focus of the next two sections.

HOMOGENEOUS OPERATION OF ECL IN FIVE-VOLT SYSTEMS

The primary concern in operating ECL circuits with power supply levels not meeting the specifications is the effect upon the noise margin, defined as:

$$\begin{aligned} V_{NMH} &= V_{OHTmin} - V_{IHTmin} && \text{for logic I,} \\ V_{NML} &= V_{ILTmiix} - V_{OLTmax} && \text{for logic O,} \end{aligned} \qquad (1)$$

where:

V_{OHTmin} = minimum HIGH level output threshold with inputs at threshold.

V_{IHTmin} = HIGH level input threshold voltage.

V_{ILTmax} = LOW level input threshold voltage.

V_{OLTmax} = maximum HIGH level output threshold with inputs at threshold.

Noise margin is defined in this way for all ECL devices (except those devices with line receiver differential type inputs). These devices compare the incoming logic voltage to an internal threshold (V_{BB}) to determine the logic state. The input thresholds defined above relate to this internal reference. Noise margin for differential inputs will be dealt with shortly. The effect of 5-volt operation on these thresholds, and therefore on the noise margin, varies by Family.

10K ECL at Five Volts

Noise margins specified for 10K ECL at 5.2 volts over temperature are

$$V_{NMH} = 125 \text{ mV and } V_{NML} = 155 \text{ mV.} \qquad (2)$$

With power supply variations, the input thresholds will track the internal logic reference (V_{BB}) and the output thresholds will track the logic output variations. Using the V_{EE} tracking rates of these parameters to calculate the thresholds at 5.0 volts, the resulting noise margins over temperature are

$$V_{NMH} = 93 \text{ mV and } V_{NML} = 129 \text{ mV.} \qquad (3)$$

Thus, 10K ECL operates at 5.0 volts with about a 25% loss in noise margin.

10H ECL at Five Volts

The noise margins specified for 10H ECL over temperature are

$$V_{NMH} = V_{NML} = 150 \text{ mV.} \qquad (4)$$

Because of the supply regulation built-in I OH ECL, the noise margin is guaranteed for power supplies of 5.2 volts (±IO%). This includes operation at 5.0 volts. As a result, 10H ECL operates at 5.0 volts with no loss in noise margin.

100K ECL at Five Volts

The noise margins for 100K ECL operating at 4.5 volts over temperature are

$$V_{NMH} = 130 \text{ mV and } V_{NML} = 135 \text{ mV.} \qquad (5)$$

Because of the built-in voltage regulation, these noise margins degrade by only about 10% when operated at 5.0 volts. The major disadvantage of 10OK ECL at 5.0 volts is excessive power dissipation: IOOK ECL functions draw more than twice the current of their I OH functional counterparts.

MIXING ECL FAMILIES AT FIVE VOLTS

With the input and output thresholds of each ECL family extrapolated to 5.0 volt operation for the previous analysis, the noise margin implications of interfacing different families can now be investigated.

Using 10K with 10H

Both 10K and 10H series ECL are designed with the same temperature-tracking rates. This means that the noise margins resulting from interfacing these two families will be relatively constant over temperature:

10K output driving a 10H logic input,

$$V_{NMH} > 150 \text{ mV and } V_{NML} > 85 \text{ mV}, \quad (6)$$

10H output driving a 10K logic input,

$$V_{NMH} > 87 \text{ mV and } V_{NML} > 180 \text{ mV}. \quad (7)$$

The noise margins resulting from the interfacing of 10K and 10H at 5.0 volts are comparable to the noise margins of 10K alone.

Using 100K with 10K/10H

This situation results in noise margins that vary greatly with temperature (as shown in Figure 2) because 100K logic levels are nearly constant over temperature while those of 10K and 10H have relatively strong temperature dependencies.

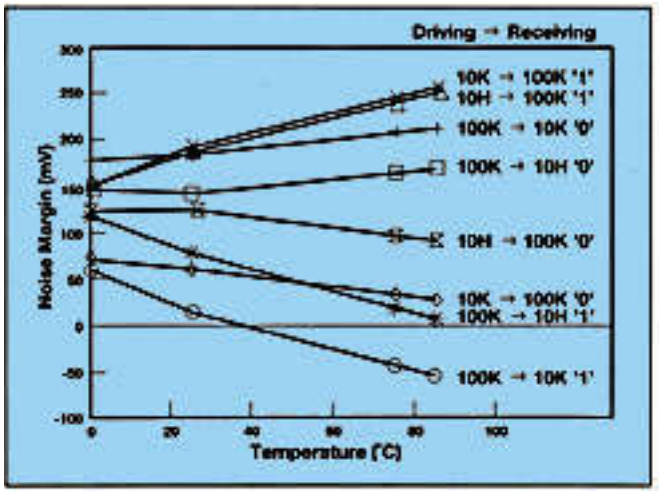

Figure 2. Mixing ECL families operating at five volts has dramatic effects on noise margins.

The worst noise-margin conditions exist when 100K and 10K are used together. The voltage regulation, and lack thereof, and the different temperature-tracking rates all work against noise margin. In the case where 10K drives 100K, V_{NML} degrades from about 70 mV at 0°C to about 30 mV at 85°C. With 100K driving 100K, V_{NMH} goes to O volts at about 40°C, representing a complete loss of noise margin.

The voltage regulation built into 10H helps to control the shifts of its input and output thresholds when the power supply is reduced to 5.0 volts. This compensation helps the 100K interface, but does not cure all of the noise-margin reductions. With I OH driving 100K, V_{NMH} equals 150 mV at low temperatures and increases to >255 mV at high temperatures, V_{NML}, equals 123 mV at low temperatures, and decreases to about 94 mV at high temperatures. Therefore, 10H driving 100K in a 5.0 volt system results in an acceptable noise margin situation. At 70°C, V_{NMI} is about 100 mV, only l% or so less than 100K-to- 100K at 5.0 volts.

When 100K drives 10H, V_{NMH} is about 120 mV at 0°C and degrades to about 10 mV at 85°C. V_{NMI} is 145 mV at 0°C and increases with temperature. The logic I noise margin for this situation would be unacceptable in most system applications.

This analysis shows that mixing of ECL families, particularly 100K with the 10K/10H families, can result in a loss of noise margin.

MAINTAINING NOISE MARGIN IN INHOMOGENEOUS INTERFACES

The previous discussion applies to single-ended logic interfaces, where the incoming logic level is compared to the internal reference of the receiving gate. All ECL devices except line receivers operate this way. The difference in the power supply voltage and temperature-tracking rates of the incoming signal and the local reference results in noise-margin variations. This section outlines guidelines to prevention. The simplest and most robust method of eliminating the noise-margin problems of interfacing different ECL families is *not to use the internal reference at the receiving end*, This is accomplished with the use of complementary signals and differential (line receiver) inputs.

Differential inputs determine the incoming logic state by sensing the difference between two complementary signals. Proper logic sensing is guaranteed provided the difference between the complementary signals is greater than 150 mV, and that the signal levels are within the 2.0 V common-mode input voltage range (V_{BB} 1.0 V). Since the complementary signals are generated by the same gate/driver, they will always track each other.

Noise margin in the differential input case can be defined as:

$$V_{NMdif} = | V_{1\sim l} - V_{1N2} | - 150\text{mV} , \quad (8)$$

where V_{1N1} and V_{1N2} are the complementary voltage levels. This relationship applies to all 10K and 10H line receivers, as well as to the differential inputs to all of ECL transmitter products manufactured by AMP.

One subtle, but important, exception to this relationship is the 100K line receiver (1001 14). The 100114, available from several manufacturers, adds an internal 75 mV offset to the differential inputs. This offset ensures a stable, guaranteed logic output when both differential inputs are at the same potential. In short, the difference between the

two inputs must be <0 mV for one state, and ≥150 mV for the other state.

The internal offset of the 100K line receiver can have a serious side effect whenever the input rise/fall times are a significant portion of the bit time. See Figure 3. Pulse-width distortion is produced by the effective shift in the switching threshold and the finite rise/fall time of the input signals.

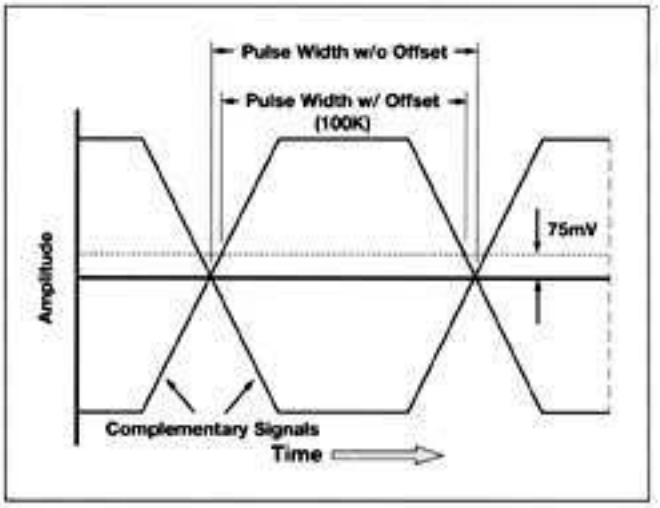

Figure 3. The differential offset in a lOOK line receiver can cause significant pulse-width distortion.

This type of distortion is commonly called duty-cycle distortion (DCD). A DCD of 200 to 300 ps, which can occur due to the offset, can cause clock recovery problems by introducing an apparent phase shift in the fundamental frequency, leading to clock jitter.

Differential drive is highly desirable when interfacing different ECL families, such as driving the inputs to AMP FDDI transmitter products, to maximize noise immunity and minimize pulse-width distortion. Complementary signals are essentially free due to the circuit design of ECL devices, most providing at least one gate with complementary outputs. In some cases, however, complementary signals may not be available to drive the differential inputs.

By connecting V_{BB} of the line receiver to one of the differntial inputs, the other input can be used as a normal gate-type logic input. The noise-margin implications outlined in the previous section apply to this case.

If the line receiver is of a different ECL family than the driving gate, the noise margins may vary considerably, as previously discussed. Improved noise margin can be obtained with the use of a reference V_{BB} from the driver's family, rather than the V_{BB} provided by the line receiver. The driver's family V_{BB} will properly track the driver's logic output voltages and will maintain adequate noise margin at the line receiver's inputs. This reference can be obtained from a line receiver of the same family as the driver, or it can be generated by an unused driver gate with simple negative feedback.

The V_{BB} generated by the AMP ECL transmitters is both power supply and temperature compensated, similar to lOOK circuits. This V_{BB} will typically vary by less than 10 mV over the entire operating temperature range of the transmitter. The compensation of this V_{BB} provides adequate noise margin in most single-ended applications with any commercial ECL family (see Figure 2). The AMP transmitter differential inputs feature the best characteristics of both worlds: low pulse-width distortion because of no built-in offset, and a temperature-compensated reference for maximum noise immunity.

The same arguments for differential drive can be applied at the receiver end. The complementary ECL outputs of the AMP ECL receiver products should be interfaced to external logic with differential inputs. This will guarantee the maximum noise immunity and lowest possible pulse-width distortion. The ECL O output level of the AMP receiver products is temperature compensated to maintain adequate noise margin with any commercial ECL family in cases where single-ended drive must be used.

CONCLUSION

The different circuit structures of the various commercial ECL devices give rise to input and output logic thresholds that can vary greatly with temperature. The use of differential inputs rather than logic inputs eliminates the noise-margin concerns of inhomogeneous ECL interfaces. Designers should be aware of the potentially dangerous input offset of true 100K ECL line receivers. Various techniques can be used for reliable single-ended interfacing of differential inputs.

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Mr. Wolke received a B.S. in electrical engineering from the New Jersey Institute of Technology in Newark. He joined Lytel in 1985 and is currently responsible for the design of custom integrated circuits, fiber-optic transmitters and receivers, and in-house test equipment and fixtures.