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TEST PROCEDURES
MANUAL
FOR
DIGITAL INPUT MODULE
VOLTAGE/RELAY CONTACTS
TYPE 322

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TABLE OF CONTENTS

	Page No.
1.0 Equipment	1
2.0 Visual Inspection	1
3.0 Opto Isolators	1
3.1 Isolation Tests	1
3.2 Voltage Type Input	1
3.2.1 Threshold	1
3.2.2 Rise, Fall, Delay	3
4.0 Contact Type Input Circuits	3
5.0 Write M1, M2 Tests	5
5.1 Overwrite Mask Registers M1, M2	5
5.2 Selective Set Commands for M1, M2	5
5.3 Selective Clear Commands for M1, M2	5
6.0 Operational Tests	5

figures

3.1 Test Fig. 322	2
4.0 Model 3222/322 Interconnect Cable	4

TABLES

5.0 Overwrite, Selective Set, M1, M2	6,7
6.0 Operational Sequence	8,9,10

Test Procedures Type 322

1.0 Equipment

1 Bi Ra Model 3222 Output Register (strapped active low out)

1 DC Source, 0 to 5V, max. ripple 50MV.

1 DC Source, 0 to 150V, ripple 0.5% max. (100 μ a limit at 150V)

1 Oscilloscope - Tektronix 465 with attached X10 probes.

1 Pulse Generator - Hewlett Packard 214A,

1 Test Box Bi Ra 6103 CAMAC Tester

1 Test Jig (Fig. 3.1)

1 Cable Bi Ra Model 3222/322 (Fig 4.0)

1 Voltmeter/Ammeter Range to read 0-5VDC, 150VDC, and 10 μ a DC. Accuracy within 1%.

2.0 Visual Inspection

Inspect the IC orientation and designations and all components and compare with 3222-CA-001 Circuit Assembly drawing. Verify no solder bridges or adjacent circuit shorts are present. Repair as required.

3.0 Opto Isolators

3.1 Isolation Tests

Connect P.C. board strap points 3 to 4 and 7 to 8 for all 16 circuits. Short each corresponding A, B input pair using Test Jig shown in Figure 3.1. Set 150V current limited source to 150VDC with series 10 μ a meter. Apply voltage from the common A, B of each channel input to all other common A, B inputs and chassis ground. Current shall not exceed 10 μ a. Turn 150V source OFF and remove source and shorts from A, B inputs. Do not remove test Jig.

3.2 Voltage Type Input

3.2.1 Threshold

On 6103 Power OFF and install unit to be tested in left N2 slot. N1/N2 switch to N2 SINGLE cycle, power ON. Verify 322 points 3,4 and 2,8 for each channel are strapped.

FIG. 3.1
TEST JIG 322

VIKING
3VH18 CON.

- +

B A
o 1 o

o 2 o

o 3 o

o 4 o

o 5 o

o 6 o

o 7 o

o 8 o

o 9 o

o 10 o

o 11 o

o 12 o

o 13 o

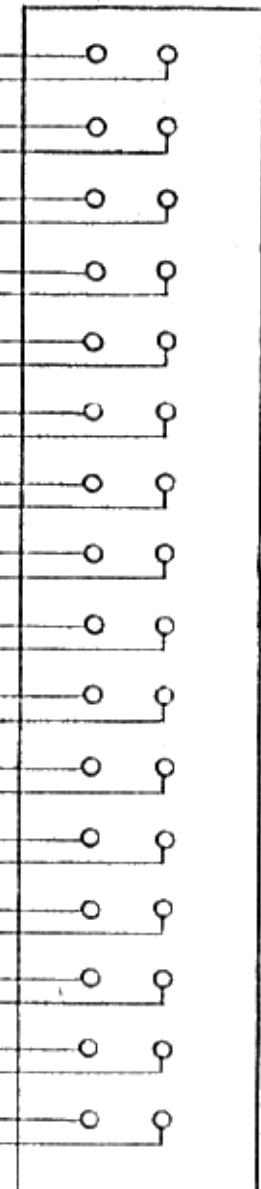
o 14 o

o 15 o

o 16 o

VECTOR
BOARD

+ -



BACK VIEW
WW PINS

NO. 30 WIRE WRAP
3 FT. CABLE

32 WW TERM

Connect variable 0 to +5VDC source from A to B begin with 1A (+), 1B (-); end with 16A, 16B. With scope monitor the corresponding MC14490 output and adjust 0 to +5VDC source from 0 toward +5V until scope trace remains solidly at TTL LOW.

With voltmeter measure the resulting DC across the A, B input. Reduce the voltage toward 0 until output is solid TTL HIGH. Voltage for TTL low shall be greater than 3.0V; for TTL HIGH voltage shall be less than 0.5V. Remove straps from 3,4 of all channels and connect corresponding 2,4 straps. Repeat DC input measurement for TTL LOW and TTL HIGH. LOW shall be less than 5.0 volts and high shall be greater than 1.5V. Remove 0 to 5VDC variable source from the circuit.

3.2.2 Rise, Fall, Delay

Verify all Opto Isolators are strapped from 2 to 4 and 7 to 8. Begin with pulse generator output +,-, to 1A(+), 1B(-) and the scope probe monitor at the respective 7,8 strap point of A25-6. Adjust pulse width and rep rate for approximately 50us and 1KHz. Measure TURN ON by time difference from the beginning 10% rise of the input pulse to the 10% fall of the output pulse. Measure FALL of the output pulse from the 10 to 90% fall. Increase the peak pulse amplitude to 30V. Measure turn off delay by measuring the time from the 10% fall of the input pulse to the 10% rise of the output. Measure the time of rise of the output pulse from the 10% to 90% rise. All measurements shall be less than 10 μ s.

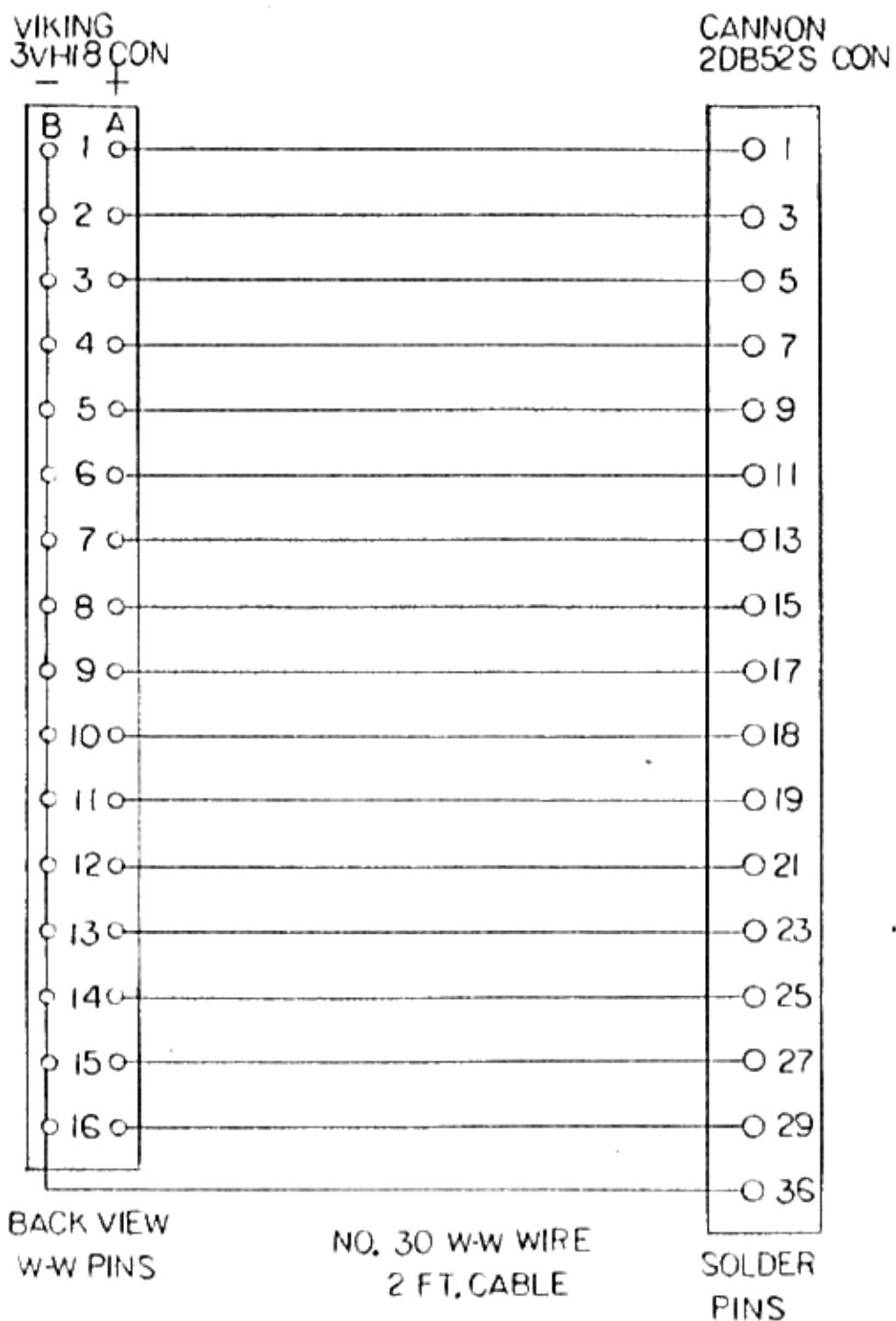
Reduce the pulse input to 0V. Remove strap 2 to 4 and connect 3 to 4. Increase pulse input to +3V peak and repeat turn-on delay and rise time measurements. Increase pulse amplitude to +5V peak and repeat turn-off delay and fall time measurement. All shall be less than 10 μ s.

Repeat above procedure for all inputs 2 through 16 to verify delay, rise, and fall is within stated limits. Remove straps from 3 to 4 and from 7 to 8 on all circuits and remove pulse generator from the unit under test.

4.0 Contact Type Input Circuits

On 6103 Power OFF and install Bi Ra 3222 Output Register in N2 slot. Connect adapter cable from 3222

FIG. 4.O
MODEL 3222/322 INTERCON
CABLE



Connector 0 to 322 Rear Auxilliary input connector. Strap respective points 1 to 8 for each of the 16 circuits. On 6103 Power ON, and set all W1-W16 WRITE switches OFF (DOWN) and all F, A switches UP (ON). RUN to OFF and issue Z+C to initialize the modules. On 6103 set N1/N2 to N2, F16 AO. First set W1 ON, all other W switches OFF and depress 6103 START. 322 LINE STATUS LAMP 1 shall light. Repeat for W2-W16 with all other W switches OFF. Depress START for each switch setting. Corresponding 322 LINE STATUS lamp shall light. All other lamps shall be Out.

5.0 Write M1, M2 Tests

5.1 Overwrite Mask Registers M1, M2

Set 6103 to N1, Single Cycle,F and A switches UP(on) and all W1-W16 switches DOWN(off). Issue Z+C and perform the overwrite command tests 1 through 10 of Table 5.0. Corresponding 6103 data read shall be the duplicate of the data written in the corresponding register. Data is listed in hexadecimal.

5.2 Selective Set Commands for M1, M2

Perform the tests 11 through 50 of Table 5.0 to selectively set the respective M1, M2 registers. Note that the F19 command does not affect M1, M2 bits which have been set.

5.3 Selective Clear Commands for M1, M2

Perform tests 51-90 of Table 5.0 to selectively clear the respective M1, M2 registers. Note that the F23 command does not affect M1, M2 bits which have been cleared.

6.0 Operational Tests

Perform the tests listed in Table 6.0 in sequence.* denotes N1 position of 6103 N1/N2 switch. Unmarked commands are the N1 position.

TABLE 5.0
OVERWRITE, SELECTIVE SET, M1, M2

-6-

TEST	INPUT	OUTPUT
1 F1 A1 2 F1 A2	CLEARED CLEARED	M1 = 0000 M2 = 0000
3 F17 A1 4 F1 A1	W = 5555 READ M1	M1 = 5555
5 F17 A2 6 F1 A2	W = 5555 READ M2	M2 = 5555
7 F17 A1 8 F1 A1	W = CCCC READ M1	M1 = CCCC
9 F17 A2 10 F1 A2	W = CCCC READ M2	M2 = CCCC
11 F17 A1 12 F1 A1	W = 0000 READ M1	M1 = 0000
13 F19 A1 14 F1 A1 15 F19 A1 16 F1 A1	W = 0001 READ M1 W = 0002 READ M1	M1 = 0001 M1 = 0003
17 : 30	Repeat 13-16 for all 16 bits	
31 F17 A2 32 F1 A2	W = 0000 READ M2	M2 = 0000
33 F19 A2 34 F1 A2 35 F19 A2 36 F1 A2	W = 0001 READ M2 W = 0002 READ M2	M2 = 0001 M2 = 0003
37 : 50	Repeat 33-36 for all 16 bits	
51 F17 A1 52 F1 A1	W = FFFF READ M1	M1 = FFFF

(TABLE 5.0 CONTINUED)

TEST	INPUT	OUTPUT
53 F23 A1 54 F1 A1 55 F23 A1 56 F1 A1	W = 0001 READ M1 W = 0002 READ M1	M1 = FFFE M1 = FFFC
56 : 70	Repeat 53-56 for all 16 bits	
71 F17 A2 72 F1 A2	W = FFFF READ M2	M2 = FFFF
73 F23 A2 74 F1 A2 75 F23 A2 76 F1 A2	W = 0001 READ M2 W = 0002 READ M2	M2 = FFFE M2 = FFFC
77 : 90	Repeat 73-76 for all 16 bits	

