MANUAL CC-91 DMA-GPIB
INTERFACE MODULE

VERSION 1.1 March 1988

Documentation history

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CC91 MODULE

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CHAPTER 1

GENERAL INFORMATION

1.1 Introduction

The CC91 module interfaces the VMEbus and the IEEE-488 standard interface bus with each other. This manual gives a full description of the hardware and software for users and system programmers. Throughout this manual, it is assumed that the reader is thoroughly familiar with the General Purpose Interface Bus (GPIB) as covered in IEEE-488 Specification, 1978 issue and 1980 supplement. It is noted here that the IEEE-488 Interface Bus is also known as HP-IB, GPIB and IEC-625 Bus. In this manual the term GPIB will be used most of the time. For specific details about the VMEbus, GPIB controller or DMA controller, the following documents may also be consulted.

- VMEbus specification manual
- IEEE Standard Digital Interface for Programmable Instrumentation (IEEE Std 488-1978, IEEE Std 488-A-1980)
- TMS9914A General Purpose Interface Bus (GPIB) controller data manual
- 68450 DMA controller data sheet

1.2 Features

The CC91 VME-GPIB interface module features the high performance 68450 DMA Controller and the TMS9914A GPIB Controller.

VME features:

- DMA Controller supports I/O to memory, memory to I/O and memory to memory transfers
- Optimal bus width utilization for mixed byte and word transfers
- Programmable Interrupt and Bus Request levels
- Programmable Interrupt vectors
- Interrupts VMEbus when GPIB requires service
- 23 bit addresses, 16 data lines and 6 AM code lines
- Highly reliable data transfer by error detect, error interrupt vector and exception features

GPIB features:

- Full Source and Acceptor handshake capability (SH1, AH1)
- All Talker and Listener functions (T5, TE5, L3, LE3)
- Full Service Request capability (SR1)
- Remote Local mode (RL1)
- Parallel Poll capability (PP1, PP2)

- Device Clear and Device Trigger capability (DC1, DT1)
- Complete Controller functions (C1, C2, C3, C4, C9)
- DMA or programmed I/O transfers

All GPIB I/O signals are available on the I/O pins of the P2 connector and optionally also on an IEEE-488 compatible 24-pole micro-ribbon connector and a 25-pole IEC-625 type connector.

1.3 General Description

The General Purpose Interface Bus (GPIB) is a carefully defined instrumentation interface which simplifies the integration of instruments, calculators, and computers into systems. The bus employs 8 data and 8 control lines and may interconnect up to 15 instruments. Data is transmitted on the 8 GPIB data lines as a series of 8-bit characters referred to as bytes. The CC91 module may perform the IEEE-488 standard functions such as Controller, Listener and Talker. The 8-bit data transfers between the GPIB bus and the VMEbus can be handled by any DTB master or by the local DMA controller. The DMA controller can also be used for memory to memory transfers on the VMEbus. The CC91 has a four-level Bus Requester and a seven-level Interrupter, which are both software programmable. The normal and error interrupt vector can also be dynamically installed.

CHAPTER 2

SPECIFICATION

2.1 VMEbus Options

Data transfer options:

- DTB MASTER A24,A16; D16,D8
- DTB SLAVE   A24,A16; D16,D8

Requester options:

- Any one of R(0) R(1) R(2) R(3) (DYN)
- RWD

Interrupter options:

- Any one of I(1) I(2) I(3) I(4) I(5) I(6) I(7) (DYN)
- Normal interrupt vector (DYN)
- Error interrupt vector (DYN)

Physical configuration options:

- NEXP

Environmental conditions:

- operating temperature 0-70 degrees C
- max operating humidity 90 %

Power supply requirements:

- 2.8 A max (2.3 A typ) at 5 VDC

2.2 GPIB Bus Options

The following options are implemented on the CC91 module.

- Supports IEEE std 488-1978
  and IEEE std 488-A-1980 supplement
- Full Controller, Talker, and Listener Function
- Both IEEE-488 and IEC-625 connector types available
- Switch selectable 5-bit device address
- Switch selectable System Control function

CHAPTER 3

INSTALLATION INSTRUCTIONS

3.1 Introduction

This chapter gives all necessary preparation and installation instructions for the CC91 VME-GPIB interface module. The module can be used in VMEbus systems and configuration options are selected by jumpers and switches. All settings are illustrated as seen from the component side with both VMEbus connectors downwards. Jumper blocks are drawn using 'o' for each pin except pin 1 which is identified as '*'. The next table shows the switch and jumper options.

OPTION	SWITCH or JUMPER BLOCK
start address	S1, S2, S3, S4
AM code	JB1, JB2
DMA clock	JB3
GPIB device address	S5
Control, Talk, Listen functions	S5
external DMA control lines	JB5, JB6, JB7

In the next sections all options are described in detail.

3.2 Address Selection

Jumper blocks JB1 and JB2 are used for the address modifier selection. JB1 when installed will make the CC91 module respond to supervisory access only. When JB1 is removed, no distinction between supervisor and non-privileged access is made.

```
                *
JB1:                        supervisory or
                o           non-privileged access


                *
JB1:            |           supervisory-only access
                o
```

JB2 is used to select standard or short address decoding.

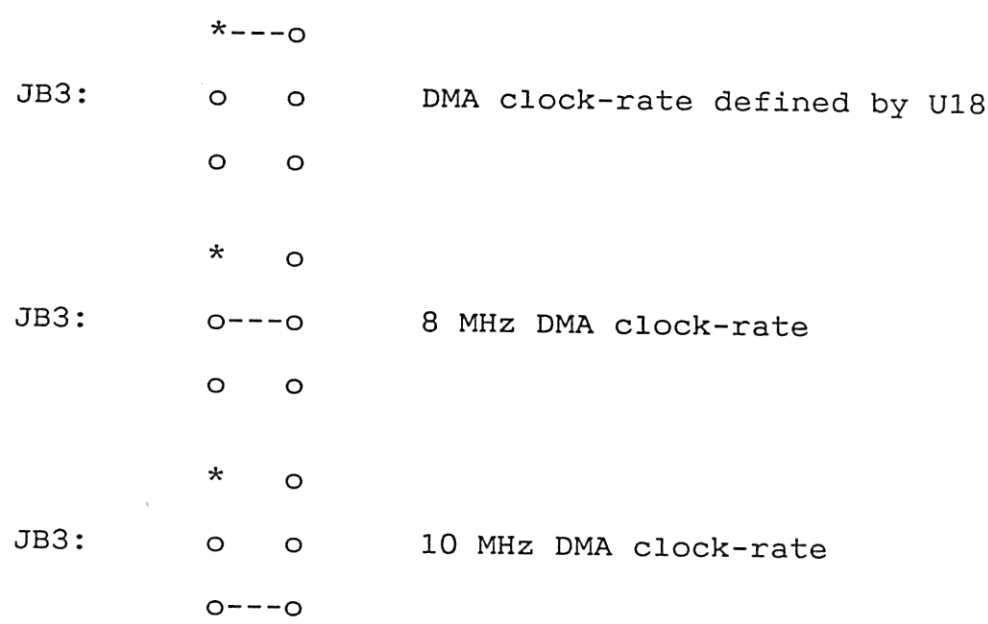
```
JB2:    *---o   o---o       standard addressing

JB2:    *   o---o   o       short addressing
```

Switches S1-S4 are hexadecimal switches used to select the base address of the module. S1 selects the most significant nibble, so the address lines A23-A20 are selected by S1, A19-A16 by S2, A15-A12 by S3, and A11-A9 are selected by S4. Note that S4 selects 3 address lines and thus has only 8 significant positions (only even numbers). Also note that S1 and S2 are not significant when JB2 is installed for short addressing.

3.3 DMA Clock Selection

Jumper JB3 is used to select the DMA clock input. When an 8 MHz DMAC is used, a derivative of the system clock can be used. When a 10 MHz DMAC is used, the local clock oscillator may be used and for other clock rates the optional oscillator U18 must be installed. Jumper JB3 must be set according to the installed DMAC type.



3.4 GPIB Device Address Selection

The 8-segment DIL switch S5, functions as the read portion of the address register of the GPIB controller. The GPIB device address is installed with switch positions 1-5 for A1-A5 respectively. Switch positions 6 and 7 are used to disable the Talker and/or Listener function respectively, and switch position 8 enables the GPIB System Control function. The switch positions and their functions are illustrated in the next table.

switch settings S5

Position	ON	OFF	Function
1	A1 = 0	A1 = 1	
2	A2 = 0	A2 = 1	
3	A3 = 0	A3 = 1	address selection
4	A4 = 0	A4 = 1	
5	A5 = 0	A5 = 1	
6	disable	enable	Talker configuration
7	disable	enable	Listener configuration
8	enable	disable	System Controller

Note that the IEEE-488 specification does not allow a device to be assigned the value 11111 for bits A1-A5. The specification also defines that only one device is allowed to drive the signal lines REN (Remote Enable) and IFC (Interface Clear). This device is called the System Controller. The CC91 module performs the System Controller function when S5-8 is switched ON.

3.5 External DMA Devices

The jumpers involved with external DMA devices are JB5, JB6 and JB7. The programmable control lines can be used for input or output. JB5 is used to select the direction of the PCL2 control line.

JB6 selects the direction of the PCL3 control line.

JB7 is used to select the direction of the DONE signal.

Jumpers JB5, JB6 and JB7 can be removed when not using the option for external DMA devices. When using this option it is necessary that there shall be no conflicts between the programmed direction and the installed jumper settings of the control lines.

3.6 GPIB Connector

Two types of interface connectors are commonly used for GPIB systems. These are the 24-pole micro-ribbon connector and the 25-pole D connector, which conform to the IEEE-488 and IEC-625 specification respectively. Both connectors can be used on the CC91 module. It is also possible to interface the GPIB through the I/O pins of the P2 connector. The assignment of the GPIB lines on the P2 connector is defined so that a flatcable can be used for a direct connection to the IEEE-488 as well as the IEC-625 type connector. All connector pin assignments are given in appendix E.

CHAPTER 4

THEORY OF OPERATION

4.1 Introduction

This chapter gives a global explanation of the functional blocks as shown in Appendix A. The schematic diagrams are given in Appendix B. The main functions of the CC91 module are performed by the 68450 DMAC and the TMS 9914A GPIB controller. These two parts are fully described in the manufacturers documentation.

4.2 DMA Controller

The 68450 DMAC has three modes of operation.
In the MPU mode, the DMAC is selected by an external bus master, through a chip select or interrupt acknowledge. The bus master is writing or reading the contents of the DMAC internal registers.
In the DMA mode, the DMAC is the current bus master and is transferring data or preparing for the data transfer.
In the IDLE mode, the DMAC is in a state other than MPU or DMA mode. A Read/Write access or transfer request will change the mode into MPU or DMA respectively.

4.2.1 MPU Mode

In MPU mode, an access is made to one of the DMAC internal registers. The registers can be accessed by byte or word. There are 64 bytes defined per channel and each channel has 17 registers. There are four channels available, so the DMAC takes 256 bytes in the memory map. The address lines A1 through A7 and the data strobes determine which register will be selected.
When an interrupt acknowledge cycle is performed the DMA controller puts the contents of the normal or error interrupt vector register of the highest channel requesting an interrupt on the data bus. The DMAC uses a multiplexed address/data bus, demultiplexing is done by U7-U10 with the control signals DDIR (Data DIRection), DBEN (Data Bus ENable) and UAS (Upper Address Strobe).

4.2.2 DMA Mode

When in DMA mode, the DMAC is the current VMEbus master and activates the OWN line, this will enable the buffers of the VMEbus interface. Transfer modes used for DMA are defined as follows.

Dual addressing with auto request:

- transfer byte or word from memory to holding register.
- transfer byte or word from holding register to memory.

Single addressing with request acknowledge handshake:

- transfer byte from GPIB PC to memory (using D0-D7).
- transfer byte from GPIB PC to memory (using D8-D15).
- transfer byte from memory to GPIB PC (using D0-D7).
- transfer byte from memory to GPIB PC (using D8-D15).

Timing and control signals are generated by U15, U16 and U29.

4.3 VMEbus Interface

The main part of the interface to the VMEbus is given in the schematic diagram (sheet 1). The address and data lines are shown with their respective buffers to the VMEbus. The control signals for these buffers are GVME to enable the data buffer on the VMEbus, FROMVME to control the data direction of the data buffers and OWNL wich is used to enable the address buffers. These control signals are generated by U29 (sheet 7). The multiplexing of the address and data lines is performed by the DMAC using the signals UAS (Upper Address Strobe), DDIR (Data DIRection) and DBEN (Data Bus ENable). The control lines on the VMEbus are buffered by U14, U26 and U27 (sheet 4). The generation of DTACK (when in MPU mode) is performed by U15 (sheet 7) and buffered by U24 and U30. A shift register U52 is used for the DTACK timing.

4.4 Address Decoding

The address decoder is given in the schematic diagram of sheet 2 and uses the address lines A9-A23 and AM code lines AM0-AM5. The LIACK signal is used to inhibit address decoding when an IACK cycle is performed. Jumper JB2 is used to enable standard or short addressing and JB1 to select supervisory only or non-privileged access. The remaining modifier codes select data I/O access.

4.5 DTB Requester

The onboard DTB requester consists of two parts, the requester logic U20 and the chaining logic U21. The bus request logic, when activated by LDBR (Local DMA Bus Request) will assert one of the BRx outputs depending on the installed request level (REQLV0, REQLV1). Now it will wait for a Bus Grant (BGT) from the chaining logic. The chaining logic checks the incoming BGxIN signals from the VMEbus and determines if the incoming signals must be chained to BGxOUT or should be used locally. Latch U19 is used to guarantee a valid BGxIN signal for the chaining logic. The level of bus request is software selectable and is discussed in chapter 5.5.

4.6 Interrupter

The Interrupter U22 (sheet 3) uses the latched VMEbus signals. This circuit asserts one of the seven VMEbus interrupt signals (IRQ1-IRQ7) when a local DMA interrupt (LIRQDMA) is received. The interrupt level is determined by IRQLV0-IRQLV2 and is software selectable (see chapter 5.4). When an interrupt has been asserted the interrupter waits for an Interrupt acknowledge cycle on the VMEbus. Then the interrupt level will be checked and when a match is found IACKSEL will be asserted, otherwise IACKOUT is asserted. The DMA controller will generate the proper interrupt vector, when necessary. When an interrupt acknowledge cycle for the DMAC is performed, the interrupter releases the VMEbus IRQ line and will only respond to another IRQDMA, after negation of LIRQDMA for at least two clock cycles (125 ns).

4.7 External DMA Devices

The 68450 is a four channel DMAC and only two channels are used by the GPIB interface. The control lines of the two unused channels are connected to the P2 connector. The direction of these signals can be selected by jumpers. The two channels may therefore be used by other devices on other modules via control lines on the P2 connector. Care should be taken here to prevent conflicts with the VMEbus specification; however, relatively simple I/O modules may take advantage of these DMA channels.

4.8 GPIB Interface

The GPIB bus is controlled by the TMS 9914A, and sheet 5 of the schematic diagrams shows the complete interface. U41 buffers the eight data lines on the GPIB bus, and U42 buffers the control lines. The data buffer (U41), when enabled, operates in the 'push/pull mode' for normal data transfer and in the 'open collector mode' during a parallel poll. All GPIB signal lines are available at the VMEbus P2 connector, and optional also on an IEEE-488 and/or IEC-625 type connector on the front panel of the CC91 module.

CHAPTER 5

PROGRAMMING CONSIDERATIONS

5.1 Introduction

This section contains all necessary information for system programmers to take full advantage of the features of the CC91 module. Additional information may be found in the respective data sheets of the GPIB controller (TMS 9914A), and the DMA controller (68450). For system programmers who want to write their own CC91 driver software, a full understanding and experience is required.

5.2 Memory Map

The memory map is given in Appendix F. The module takes $200 (=512) byte locations, starting at the installed base address. The first 256 locations are used for the DMA controller and the second block is partially used by the GPIB controller (8 bytes), the local control register (1 byte), and the end of string register (1 byte). The GPIB controller, the control register, and the EOS register are 8-bit wide and are accessed at odd memory locations. All are duplicated an arbitrary number of times in the memory map. The recommended address locations for use by system programmers are given below.

```
B_DMAC   equ  CC91_BASE+0       base address for DMAC
CNTREG   equ  CC91_BASE+$100    address of control register
EOSREG   equ  CC91_BASE+$120    address of EOS register
B_GPIB   equ  CC91_BASE+$130    base address for GPIB contr.
```

CC91_BASE depends on the address select switches S1-S4. Note that the byte-wide registers respond at odd addresses only. The registers within the DMAC and GPIB controller can be accessed by using B_DMAC and B_GPIB as the respective register base addresses and declaring each register as an offset from these addresses (see Appendices G and H)

5.3 Reset

The SYSRES* signal from the VMEbus will reset the DMAC, GPIB controller DTB Requester, the local Control Register, and the EOS Register.

When the DMAC recognizes Reset, it relinquishes the bus, clears the GCR and resets the DCR, OCR, SCR, CCR, CSR, CPR and CER of all channels. The interrupt vector registers are set to $0F (uninitialized interrupt vector number).

When reset is active, the GPIB Controller is forced into the idle state, during which it will not take part in any activity on the GPIB. The Serial and Parallel Poll registers are cleared, and the Auxiliary Command register is initiated for the software reset command.

The DTB Requester falls into the idle state after reset, which means that all output signals are negated (no bus requests active).

The local control register will be cleared after reset and all output lines will be low. This disables the interrupt request level, the bus request level will be 0 and the GPIB reset signal will NOT be asserted.

The EOS register will be cleared after reset.

5.4 Interrupts

All interrupts from the CC91 module are generated by the DMAC. These interrupts can be caused by several conditions such as channel operation complete, PCL transition or Bus error. Each channel may generate its own normal interrupt vector or error interrupt vector. An error interrupt vector is generated when a DMA transfer is terminated by a bus error response or when an address error ocurred. In the case of an error, the present values of the Memory Address, Device Address and Base Address registers, the Memory Transfer and Base Transfer counters, and Control, Status and Error registers will be available. The interrupt signal of the GPIB controller is connected to the PCL0 input of the DMAC, and the EOS comparator output is connected to the PCL1 input of the DMAC. These inputs may also cause an interrupt on the VMEbus. The interrupt signal from the DMAC is sent to the Interrupter which will assert the proper interrupt request line. The interrupt level is selected by the Control Register outputs IRQLV0, IRQLV1 and IRQLV2 (3 binary encoded level outputs).

IRQLV2	IRQLV1	IRQLV0	INTERRUPT LEVEL
0	0	0	(disabled)
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Bit 3 of the Control Register may be used to disable the DMAC IRQ line. This bit is used by the interrupt routine as follows.

-disable IRQ line (set bit 3).
-process the normal interrupt routine.
-enable IRQ line (clear bit 3).

This procedure is necessary to guarantee the proper working of the Interrupter.

5.5 Bus Request

When the DMA controller needs control of the bus it will generate a DMA Bus Request to the DTB requester. The level on which the DTB requester will generate a Bus Request on the VMEbus depends on the REQLV0, REQLV1 outputs of the control register (2 binary encoded level outputs).

REQLV1	REQLV0	BUS REQUEST LEVEL
0	0	0
0	1	1
1	0	2
1	1	3

The DMAC controls VMEbus utilization and request interval timing. The Burst Transfer Mode, Cycle Steal Mode (with or without hold), Burst time and Bandwidth Ratio are also under software control.

5.6 Control Register

The Control Register performs several functions. It is used to select the levels for the DTB Requester and the Interrupter, and to enable/disable the DMA IRQ line. It is also used to assert the reset line (LRST) of the GPIB controller. This makes it possible to give a hardware reset to the GPIB controller under software control. The following table shows the bit assignments of the Control Register.

BIT	READ	WRITE	FUNCTION
0	IRQLV0	IRQLV0	
1	IRQLV1	IRQLV1	Interrupt Request Level
2	IRQLV2	IRQLV2	
3	ENIRQ	ENIRQ	Enable DMA IRQ
4	REQLV0	REQLV0	DTB Request Level
5	REQLV1	REQLV1	
6	Spare	Spare	Not used
7	LRST	LRST	GPIB Reset

5.7 End Of String Register

The EOS register is a write only register which contains the byte that is compared with all incoming data bytes during DMA transfer operations. When a match is found the PCL1 line of the DMAC will be asserted, which may cause an interrupt.

5.8 AM Code Generation

When the DMA Controller is in the DMA mode, it will generate Function Codes on its FC0-FC2 lines. These lines are software programmable for source, destination and base address access (see chapter 5.9.1). A translation of these lines is made to generate the six Address Modifier code lines on the VMEbus. The table below shows the translation and function of the respective lines.

FC2	FC1	FC0	AM5	AM4	AM3	AM2	AM1	AM0	FUNCTION
0	0	0	1	0	1	0	0	1	short n.p. I/O
0	0	1	1	1	1	0	0	1	stand n.p. data
0	1	0	1	1	1	0	1	0	stand n.p. prog
0	1	1	1	1	1	0	1	0	stand n.p. prog
1	0	0	1	0	1	1	0	1	short priv I/O
1	0	1	1	1	1	1	0	1	stand priv data
1	1	0	1	1	1	1	1	0	stand priv prog
1	1	1	1	1	1	1	1	0	stand priv prog

5.9 Programming the CC91 Module

Programming the CC91 module can be divided into two main sections: programming the DMAC and programming the GPIB controller. It is also necessary to program the desired interrupt and bus request level as discussed in chapter 5.4 and 5.5 respectively. In chapter 5.9.1 the programming of the DMAC is discussed. Chapter 5.9.2 discusses the programming of the GPIB controller.

5.9.1 Programming The DMA Controller

The 68450 DMAC has internal control registers and performs required operation by means of control words in these registers written by the MPU. A normal programming sequence can be divided into three phases.

The Initiation phase: MPU sets up control registers, transfer address and transfer counts.

The Transfer Phase: DMAC receives requests and transfers data. The DMAC writes the transfer status into the error register and the internal status register after the completion of the transfer.

The Termination Phase: The MPU checks the post-transfer status.

The internal registers are shown in Appendix G and a short description is given below.

The Device Control Register designates an external I/O device. It will set the external request generation method, the device type, the device port size, and the PCL line operation.

The Operation Control Register designates the transfer operation. It designates the data transfer direction, the operand size, the chain operation types, and the request generation method.

The Sequence Control Register designates the increment/decrement sequence of both memory and device (source and destination) addresses.

The Channel Control Register designates the channel operation. It designates the operation start, the continuous-operation setting, HALT, abort and interrupt enable/disable.

The Channel Status Register has the channel status. It shows the channel operation completion, block transfer completion, normal termination, error status, channel active state, and PCL signal line information.

The Channel Error Register indicates what error types have occured.

The Channel Priority Register determines the priority of the channel.

The Memory Transfer Counter is a 16-bit register to hold transfer counts. The block size (transfer count) is written when one data block is transferred. When multiple blocks are transferred in Continuous Mode and Chaining Modes, the next block size is automatically loaded in the MTC after the completion of the previous block transfer.

The Base Transfer Counter is used in Continuous Mode and Array Chaining Mode. In Continuous Mode the first block size is stored in the MTC and the second block size in the BTC. The content of the BTC is copied into the MTC after the completion of the first block transfer. When more than two blocks are transferred in this mode, the BTC and the BAR (described later) are rewritten and the CNT bit in the CSR is set again during the second (or third) block transfer. In Array Chaining Mode, the BTC holds the number of blocks being transferred.

The Memory Address Register contains the memory address being output for each transfer cycle. In block transfer, the beginning address of the block is written in the MAR as an initial value. And the content of the MAR varies according to the content of the OCR and the SIZE bits in the SCR after one operand transfer. In Continuous Mode and Chain Modes, the MAR is rewritten according to the BAR or the array information in memory when a block transfer completes.

The Device Address Register is used to address an I/O device (or to address memory, in memory to memory transfer). The DAR is used only in Dual Addressing Mode, and changes its content according to the SCR and according to the SIZE bits in the OCR.

The Base Address Register is used in Continuous Mode and Chain Modes. In Continuous Mode, the start address of the second block is written in the BAR. This BAR is used in the same way as the BTC. In Chain Modes, it keeps the address where the information of the next block is contained.

The Memory Function Code, Device Function Code, and Base Function Code Registers are used together with the MAR, DAR, and BAR respectively. The MFC, DFC, and BFC are used with the same purpose as the FC outputs from the MPU. This makes it possible to transfer data between supervisor program area and user data area, for example. A translation is made to generate VMEbus AM codes from the Function Codes, which is discussed in chapter 5.8.

The Normal and Error Interrupt Vector keep the vector numbers outputted in the vector number fetch cycle (Interrupt Acknowledge Cycle). When no error has occured (the ERR bit of the CSR is not set), the DMAC outputs the NIV content. When an error has occured (ERR=1), the DMAC outputs the EIV content.

The General Control Register is common to all four channels and determines the DMAC's bus use ratio and sample interval in limited Rate Auto-Request Mode. In Maximum Rate Auto-Request Mode, the DMAC takes the bus mastership and transfers all operands until they are exhausted. In this mode, when the higher priority channels request transfer, the channel with the Maximum Rate Auto-Request stops its transfer temporarily and the higher priority channel is serviced. The Maximum Rate channel resumes its transfer after the priority channel has been serviced.

After the DMAC is properly initialized, a transfer is started by setting the STR bit in the Channel Control Register. When the DMAC completes a transfer operation, the COC (Channel Operation Complete) bit in the CSR is set. If an error occurs during the transfer, the ERR bit is also set. When the INT (Interrupt Enable) bit has been set, the DMAC will issue an interrupt request when the COC bit is set. When Interrupts are disabled the MPU should poll the COC bit. The transfer termination routine should check for errors. Error routines should be programmed case by case according to their applications. For bus error and address error, the CER (Channel Error Register) can show which address register caused the error and the address where the error occured is kept in the address register. The CER also shows which of the transfer counters between MTC and BTC caused an error.

5.9.2 Programming The GPIB Controller

The GPIB controller has a set of 8 internal 8-bit registers, which are used to read or write data, status and control information. A summary of the SCSI registers is given in Appendix H. Note that some registers are read only, and some are write only. A universal software driver outline is discussed here, and can be used as a starting point for specific GPIB applications. The CC91 may act as a Controller, Listener or Talker on the GPIB, and these functions will be discussed in the next sections. It is obvious that the CC91 module is capable of performing more than one function on the GPIB, which depends on the used software. It is also noted here that data transfers on the GPIB may be handled by the DMAC. Transfer of command bytes will normally be performed by the MPU, due to the overhead caused by initialization of the DMAC.

5.9.2.1 GPIB Controller Functions

The GPIB allows a Controller, referred to as the 'Controller in Charge', to perform the control functions on the GPIB. The GPIB allows ONE System Controller to be assigned on the bus, which may perform some additional functions. The System Controller may assert the IFC (interface clear) line, which will function as a reset on the GPIB. It may also assert the REN (remote enable) line, which makes it possible to program addressed devices with 'remote commands'.

The Controller in Charge may send commands over the GPIB. These commands are divided into two groups. The Primary command group includes the Universal, Addressed, and Address commands, while the Secondary command group includes the Secondary address, and Parallel poll enable/disable commands.

UNIVERSAL COMMANDS affect every device capable of responding on the GPIB, regardless whether they have been addressed or not.
- DCL (device clear) will return all devices capable of responding, to predetermined states.
- LLO (local lockout) is used to disable the front panel controls of responding devices.
- PPU (parallel poll unconfigure) sets all devices on the GPIB with parallel poll capability to a predefined condition.
- SPE (serial poll enable) enables serial poll mode on the bus.
- SPD (serial poll disable) disables serial poll mode on the bus.

ADDRESSED COMMANDS initiate simultaneous actions from addressed devices which are capable of responding.
- GET (group execute trigger) initiates simultaneous pre-programmed actions, by responding devices.
- GTL (go to local) returns addressed devices to local control.
- PPC (parallel poll configure) permits the DIO lines to be assigned to devices on the bus for purpose of responding to a parallel poll.
- SDC (selective device clear) returns addressed devices to

predetermined states.
- TCT (take control) is used when the active controller on the bus transfers control of the bus to another device.

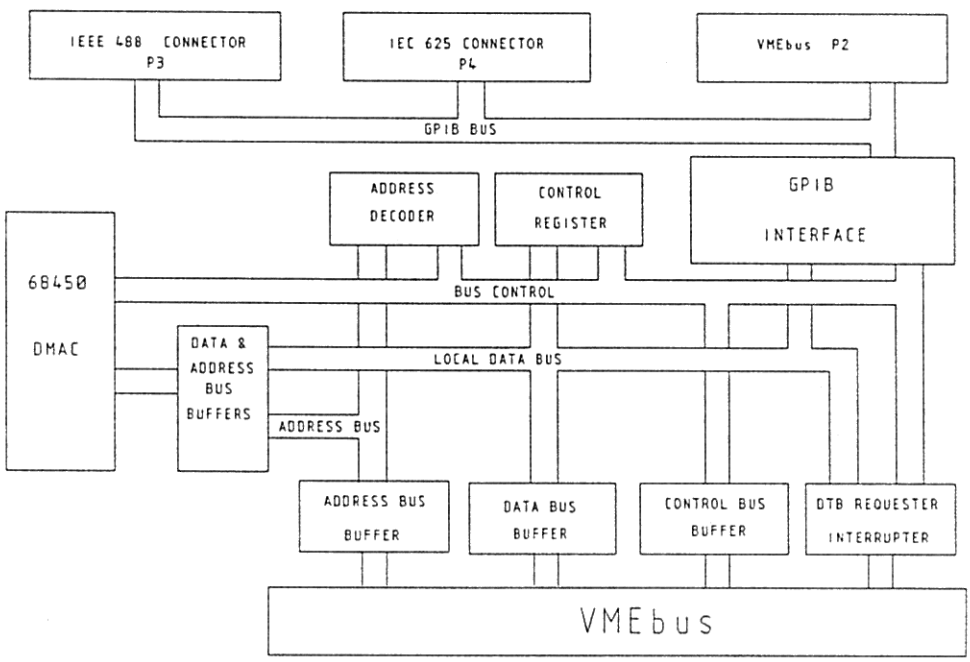
ADDRESS COMMANDS are used to address or unaddress devices on the bus.
- MLA (my listen address), enables a specific device to listen, by sending its unique listen address. Several bus devices at a time may be listeners.
- MTA (my talk address), enables a specific device to talk, by sending it unique talk address.
- UNL (unlisten) clears the bus of all listeners.
- UNT (untalk) unaddresses the current talker so that no talker remains on the bus. A talker is also unaddressed when another talk address is transmitted on the bus.

5.9.2.2 GPIB Talker / Listener Functions

For the talker and listener functions, the CC91 module can be programmed as follows. The DMAC, Interrupter and GPIB controller are setup to generate an interrupt when the device is addressed as a talker or listener. When the device is in the talker or listener addressed state (TADS or LADS), the DMAC can be initialized for the data transfer and will start when the talker or listener active state (TACS or LACS) is entered. The auxiliary command register must be set according to the desired interrupt conditions. It is also possible to program the DMAC PCL1 line to generate an interrupt when the EOS (end of string) byte is received.

APPENDIX A

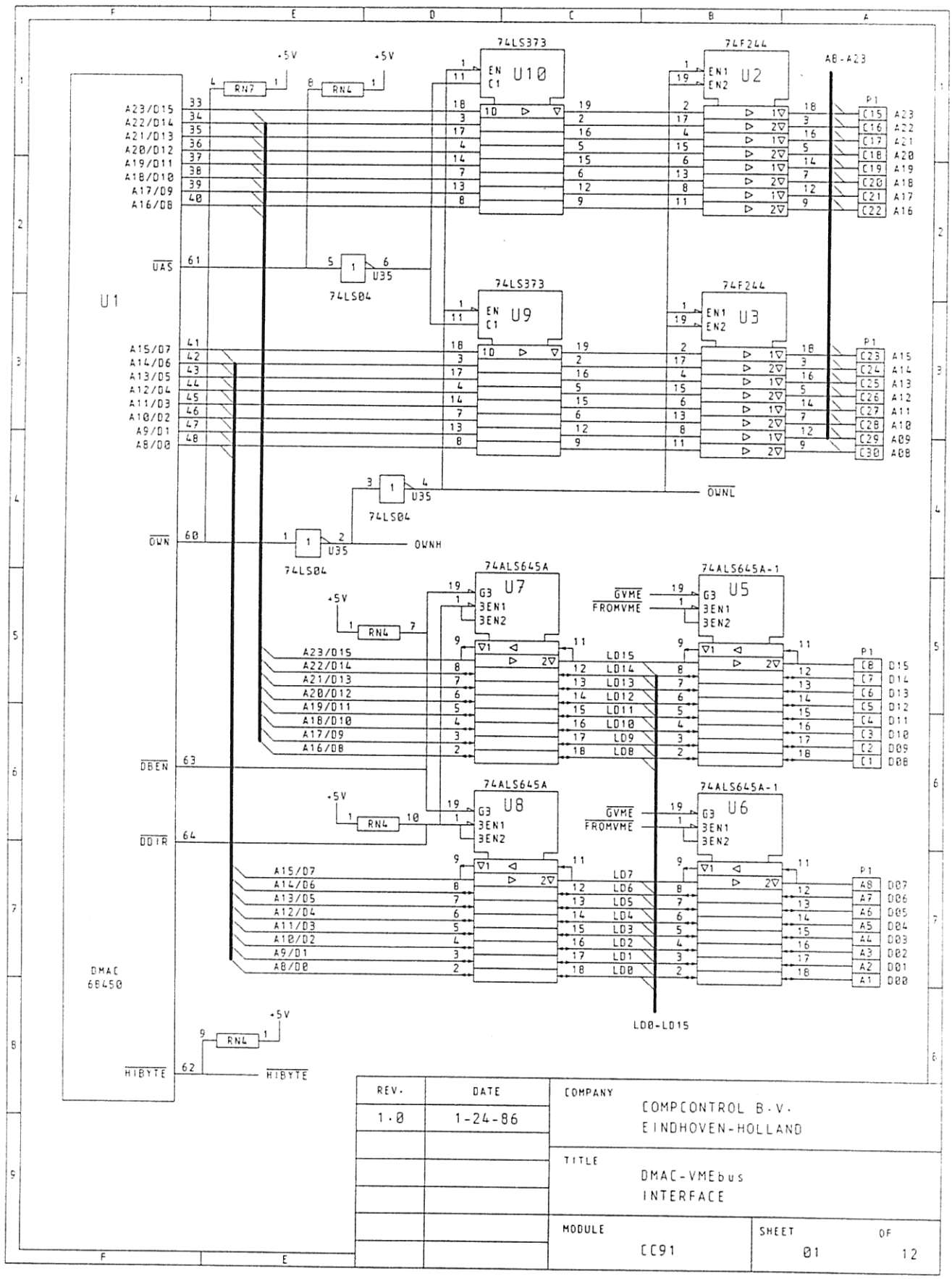
BLOCK DIAGRAM



APPENDIX B

SCHEMATIC DIAGRAMS

Sheet 1	DMAC-VMEbus interface
Sheet 2	Chip select logic
Sheet 3	Interrupter / Bus requester
Sheet 4	VMEbus interface
Sheet 5	GPIB interface
Sheet 6	DMA transfer & control logic
Sheet 7	Local data path / Control logic
Sheet 8	68450 DMAC
Sheet 9	GPIBbus connector / power supply's
Sheet 10	Decoupling
Sheet 11	VMEbus connector P1
Sheet 12	VMEbus connector P2


74LS373
U10
74F244
U2
A8-A23
74LS373
U9
74F244
U3
U1
74LS04
U35
74ALS645A
U7
74ALS645A-1
U5
74ALS645A
U8
74ALS645A-1
U6
RN4
RN7
+5V
DMAC
68450
A23/D15
A22/D14
A21/D13
A20/D12
A19/D11
A18/D10
A17/D9
A16/D8
A15/D7
A14/D6
A13/D5
A12/D4
A11/D3
A10/D2
A9/D1
A8/D0
UAS
OWN
OWNH
OWNL
DBEN
DDIR
HIBYTE
GVME
FROMVME
LD15
LD14
LD13
LD12
LD11
LD10
LD9
LD8
LD7
LD6
LD5
LD4
LD3
LD2
LD1
LD0
LD8-LD15
P1
C15 A23
C16 A22
C17 A21
C18 A20
C19 A19
C20 A18
C21 A17
C22 A16
C23 A15
C24 A14
C25 A13
C26 A12
C27 A11
C28 A10
C29 A09
C30 A08
C8 D15
C7 D14
C6 D13
C5 D12
C4 D11
C3 D10
C2 D09
C1 D08
A8 D07
A7 D06
A6 D05
A5 D04
A4 D03
A3 D02
A2 D01
A1 D00
REV. 1.0
DATE 1-24-86
COMPANY COMPCONTROL B.V. EINDHOVEN-HOLLAND
TITLE DMAC-VMEbus INTERFACE
MODULE CC91
SHEET 01 OF 12