Model 973
High-Rate Spectroiscopy Amplifier
Operating and Service Manual

Printed in U.S.A.

EG&G ORTEC Part Number 761860
Manual Revision E

3971 0896

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Standard Warranty
for
EG&G ORTEC Instruments

EG&G ORTEC warrants that the items will be delivered free from defects in material or workmanship. EG&G ORTEC makes no other warranties, express or implied, and specifically **NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.**

EG&G ORTEC's exclusive liability is limited to repairing or replacing at EG&G ORTEC's option, items found by EG&G ORTEC to be defective in workmanship or materials within **one year** from the date of delivery. EG&G ORTEC's liability on any claim of any kind, including negligence, loss, or damages arising out of, connected with, or from the performance or breach thereof, or from the manufacture, sale, delivery, resale, repair, or use of any item or services covered by this agreement or purchase order, shall in no case exceed the price allocable to the item or service furnished or any part thereof that gives rise to the claim. In the event EG&G ORTEC fails to manufacture or deliver items called for in this agreement or purchase order, EG&G ORTEC's exclusive liability and buyer's exclusive remedy shall be release of the buyer from the obligation to pay the purchase price. In no event shall EG&G ORTEC be liable for special or consequential damages.

Quality Control

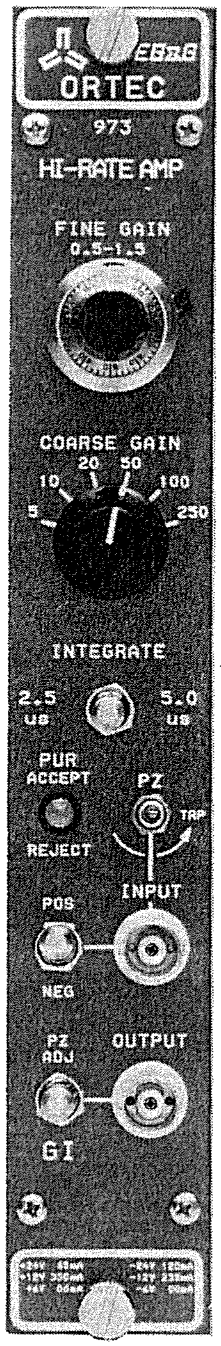
Before being approved for shipment, each EG&G ORTEC instrument must pass a stringent set of quality control tests designed to expose any flaws in materials or workmanship. Permanent records of these tests are maintained for use in warranty repair and as a source of statistical information for design improvements.

Repair Service

If it becomes necessary to return this instrument for repair, it is essential that Customer Services be contacted in advance of its return so that a Return Authorization Number can be assigned to the unit. Also, EG&G ORTEC must be informed, either in writing, by telephone [(423) 482-4411], or by facsimile transmission [(423) 483-0396], of the nature of the fault of the instrument being returned and of the model, serial, and revision ("Rev" on rear panel) numbers. Failure to do so may cause unnecessary delays in getting the unit repaired. The EG&G ORTEC standard procedure requires that instruments returned for repair pass the same quality control tests that are used for new-production instruments. Instruments that are returned should be packed so that they will withstand normal transit handling and must be shipped **PREPAID** via Air Parcel Post or United Parcel Service to the nearest EG&G ORTEC repair center. The address label and the package should include the Return Authorization Number assigned. Instruments being returned that are damaged in transit due to inadequate packing will be repaired at the sender's expense, and it will be the sender's responsibility to make claim with the shipper. Instruments not in warranty will be repaired at the standard charge unless they have been grossly misused or mishandled, in which case the user will be notified prior to the repair being done. A quotation will be sent with the notification.

Damage in Transit

Shipments should be examined immediately upon receipt for evidence of external or concealed damage. The carrier making delivery should be notified immediately of any such damage, since the carrier is normally liable for damage in shipment. Packing materials, waybills, and other such documentation should be preserved in order to establish claims. After such notification to the carrier, please notify EG&G ORTEC of the circumstances so that assistance can be provided in making damage claims and in providing replacement equipment, if necessary.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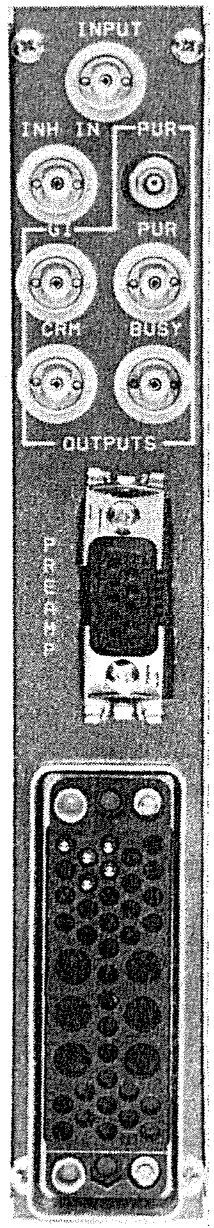
INPUT
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CRM
BUSY
OUTPUTS
PREAMP

EG&G ORTEC MODEL 973 HIGH-RATE SPECTROSCOPY AMPLIFIER

1. DESCRIPTION

The EG&G ORTEC Model 973 High-Rate Spectroscopy Amplifier provides improved energy resolution when performing gamma-ray spectroscopy with germanium detectors at high counting rates. This compact, single-width NIM module contains a "gated-integrator" amplifier, which automatically eliminates the ballistic deficit effect caused by the charge collection time variations in germanium detectors. The result is a significant improvement in the energy resolution and dead time at the short shaping time constants required for medium to high counting rates (Fig. 1.1). Compared with semi-Gaussian or triangular shaping, an improvement in amplifier throughput by a factor of approximately four can be achieved using the Model 973, without a substantial sacrifice in energy resolution (Figs. 1.2 and 1.3). The Model 973 incorporates a unique, eight-pole, active, prefilter network that offers an improved signal-to-noise ratio compared with previous gated integrator designs (Fig. 1.4). The gain of the Model 973 is continuously variable from 1.25 to 375. Its input accepts either positive or negative polarity signals from a detector preamplifier. The output provides from 0 to +10-V pulses suitable for use with single-channel or multichannel pulse height analyzers.

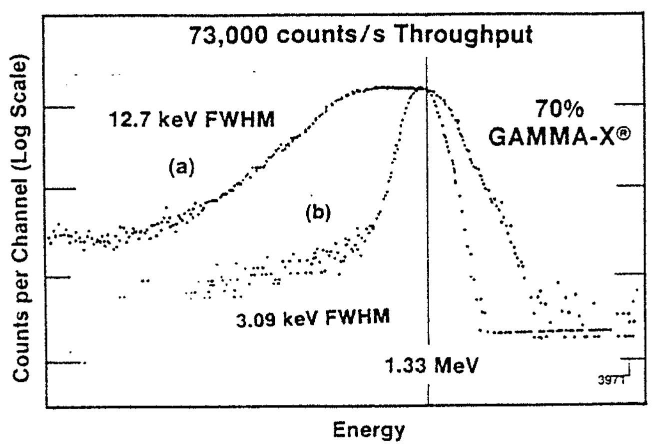

Fig. 1.1. The 1.33-MeV Gamma-Ray Peak from a ^{60}Co Source, Acquired with (a) a Model 672 Amplifier with a Triangular Pulse Shape and 0.5-μs Time Constant, and (b) the Model 973 Amplifier with a 2.5-μs Integration Time. Maximum amplifier throughput is 73,000 counts/s for both cases.

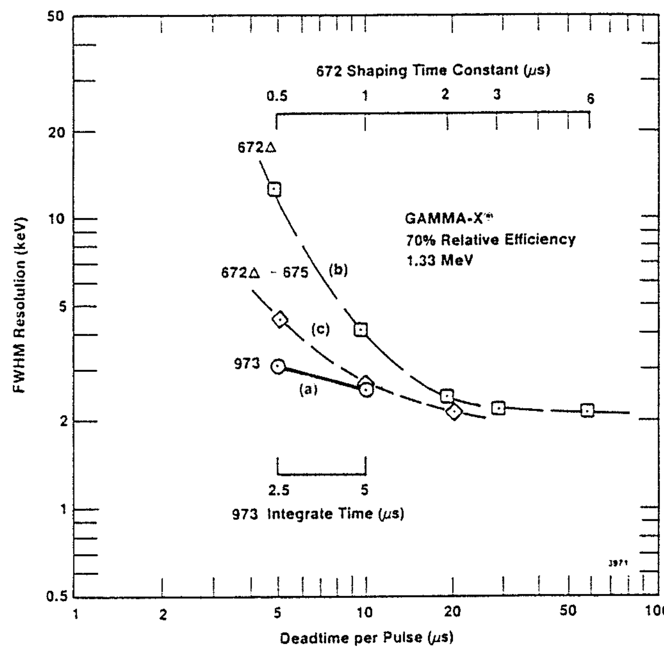

Fig. 1.2. The Energy Resolution Obtained with (a) the Model 973, (b) the Model 672 Triangular Filter Amplifier, and (c) the Model 672 Plus the 675 Ge Resolution Enhancer. The resolutions at 1.33 MeV are compared on the basis of equal amplifier dead time per pulse.

When long connecting cables are used between the detector preamplifier output and the amplifier input, noise induced in the cable by the environment can be a problem. The Model 973 provides two solutions. For low to moderate interference frequencies, the differential input mode can be used with paired cables from the preamplifier to suppress the induced noise. For medium to high frequencies, a common-mode rejection transformer built into the input reduces noise pick-up. The transformer is particularly effective in eliminating interference from the display raster generators in personal computers and display terminals. Automation of critical adjustments makes the Model 973 easy to set up with any detector, while minimizing the required operator expertise. To minimize spectrum distortion at medium and high counting rates, the prefilter output to the gated integrator incorporates a high-performance, gated baseline restorer with several levels of automation.

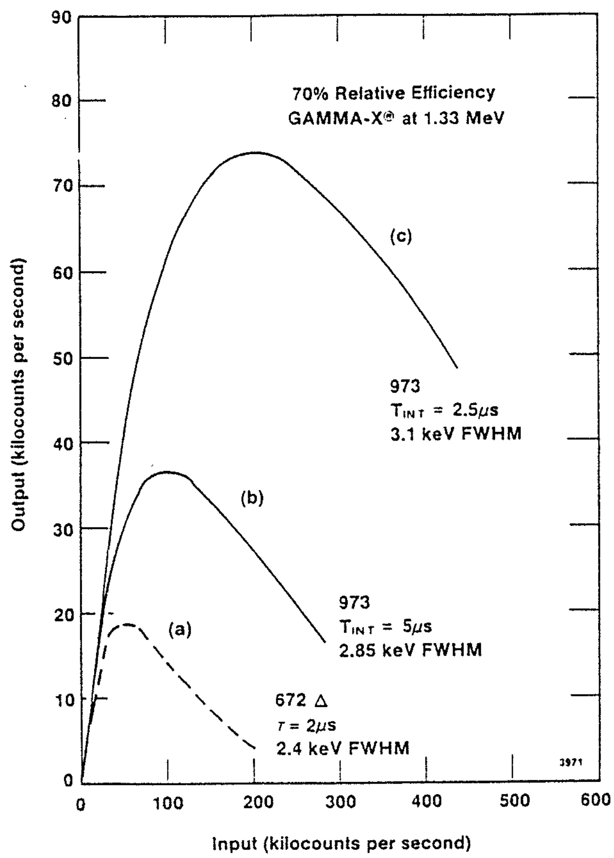

Fig. 1.3. Amplifier Output Counting Rate vs Input Rate is shown for (a) a Model 672 Amplifier with a 2-μs, Triangular Shaping Time Constant, (b) the Model 973 with a 5-μs Integration Time, and (c) the Model 973 with a 2.5-μs Integration Time.

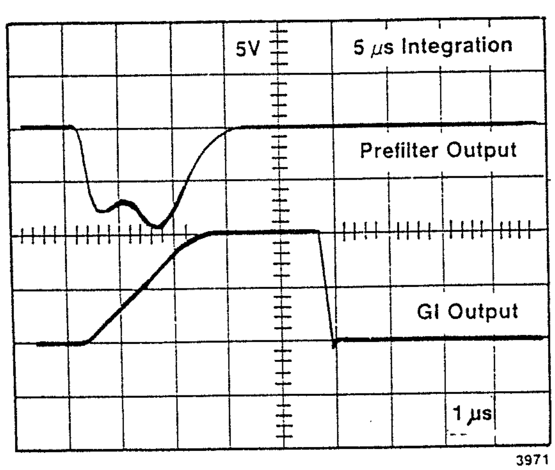

Fig. 1.4. Pulse Shapes in the Model 973 Amplifier for a 5-μs Integration Time.

Automatic positive and negative noise discriminators ensure that the baseline restorer operates only on the true baseline between pulses in spite of changes in the noise level. Both the gain and the integration time can be changed without requiring operator adjustment of the baseline restorer. In addition, the gated baseline restorer is equipped with an automatic control for the restoration rate that ensures optimum performance at both low and high counting rates.

Negative overload recovery from the reset pulses generated by transistor-reset preamplifiers is also handled automatically. A monitor circuit gates off the baseline restorer and provides a reject signal for the associated multichannel analyzer until the baseline has safely recovered from the overload. No operator adjustment of the protection time is needed with transistor-reset preamplifiers.

A high-efficiency pile-up rejector, included in the 973 High-Rate Spectroscopy Amplifier, provides an output logic pulse to the associated multichannel analyzer for suppression of the spectral distortion caused by pulses piling up on each other at high counting rates. An improved pulse pair resolving time is achieved by incorporating both pulse width and pulse separation analysis. The fast amplifier in the pile-up rejector includes a gated baseline restorer with its own automatic noise discriminator. A multi-color pile-up rejector LED on the front panel indicates the throughput efficiency of the amplifier. At low counting rates the LED flashes green. The LED turns yellow at moderate counting rates, and becomes red when pulse pile-up losses are >70%.

All toggle switches on the front panel lock to prevent accidental changes in the desired settings.

2. SPECIFICATIONS*

2.1. PERFORMANCE

GAIN RANGE Continuously adjustable from ×1.25 to ×375. Total gain is the product of the COARSE and FINE GAIN controls.

PULSE SHAPING Time-variant, trapezoidal pulse shaping, consisting of a gated integrator with an optimized, 8-pole, active prefilter. Totally eliminates resolution broadening caused by charge collection time variations in germanium detectors.

INTEGRAL NONLINEARITY <±0.05% over the output range from 0 to +10 V.

NOISE Equivalent input noise <9 μV rms, as measured at the gated integrator output with gain >100 and 5.0 μs integration.

TEMPERATURE COEFFICIENT Measured at the Gated Integrator Output, over the operating temperature range from 0 to 50°C.
Gain <±0.007%/°C.
dc Level <±7.5 μV/°C.

OVERLOAD RECOVERY Prefilter unipolar output recovers to within 2% of the maximum rated output from a ×400 overload in 2.5 non-overloaded pulse widths, using maximum gain.

SPECTRUM BROADENING† Typically, the FWHM broadens <10% when the counting rate increases from 1,000 counts/s to 300,000 counts/s (Fig. 2.1a). Measured on the 1.33-MeV gamma-ray line from a ^{60}Co radioactive source under the following conditions: 13% efficiency EG&G ORTEC GAMMA-X-PLUS detector, 8.5-V amplitude for the 1.33-MeV gamma-ray on the gated integrator output, and 2.5 μs integration time.

SPECTRUM SHIFT† Typically, the peak position shifts <0.03% when the counting rate increases from 1,000 counts/s to 300,000 counts/s (Fig 2.1b). Measured on the 1.33-MeV line under the conditions specified for SPECTRUM BROADENING.

DIFFERENTIAL INPUT Differential nonlinearity <±0.012% from -9 V to +9 V. Maximum input ±10 V (dc plus signal). Common mode rejection ratio >500.

PULSE PILE-UP REJECTOR Incorporates both pulse width and pulse separation analysis.
Threshold Automatically set just above the noise level on the fast amplifier signal. Independent of the slow amplifier BLR threshold.
Minimum Detectable Signal Limited by detector and preamplifier noise characteristics.
Pulse Pair Resolution Adjustable to match the detector charge collection time. Typically 350 ns for a 13% efficiency EG&G ORTEC GAMMA-X-PLUS detector and a 1.33-MeV gamma ray.

2.2. CONTROLS AND INDICATORS

FINE GAIN Front-panel, 10-turn precision potentiometer with locking, graduated dial provides a continuously variable, direct-reading gain factor from 0.5 to 1.5.

Specifications are subject to change without notice.

†Results may not be reproducible if measurements are made with a detector that exhibits a large number of slow-risetime signal components.

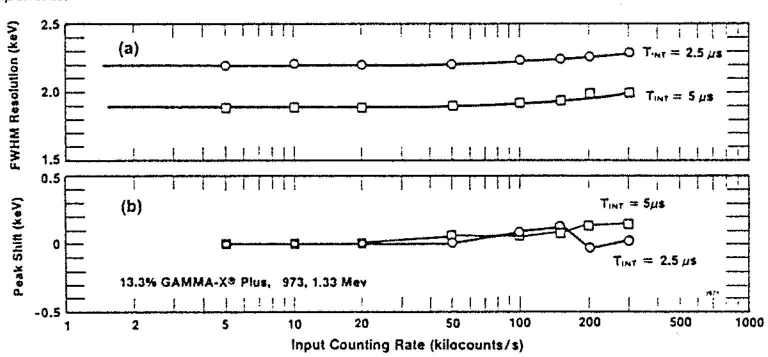

Fig. 2.1. **(a) Resolution, and (b) Peak Position Stability as a Function of Counting Rate.** See specifications for spectrum broadening and spectrum shift.

COARSE GAIN Front-panel, 6-position switch selects gain factors of 5, 10, 20, 50, 100, and 250.

×0.5/×1 Gain selection jumpers W1 and W2 on the PC-board reduce the gain of the input stage by a factor of two. Shipped in the ×1 position for normal use.

INTEGRATE Front-panel, two-position, locking, toggle switch selects either a 2.5-μs or a 5-μs integration time for the gated integrator and the matching prefilter.

PUR ACCEPT/REJECT LED Multi-color LED indicates percentage of pulses rejected because of pulse pile-up. LED appears green for 0 - 40%, yellow for 40 - 70 %, and red for >70 % rejection.

PZ Front-panel, 20-turn potentiometer permits screwdriver adjustment of the pole zero (PZ) cancellation. The adjustment covers preamplifier exponential decay time constants from 40 μs to infinity. For transistor-reset preamplifiers (TRP), set the PZ adjustment fully counterclockwise.

INPUT POS/NEG Front-panel, two-position, locking, toggle switch accommodates either positive or negative input pulse polarities.

PZ ADJ/GI Front-panel, two-position, locking, toggle switch selects either the diode-limited prefilter pulse (PZ ADJ) or the gated integrator pulse (GI) to be routed to the OUTPUT connector. In the PZ ADJ position, monitoring the diode-limited prefilter pulse on an oscilloscope aids in accurate adjustment of the PZ cancellation. The diode limiting prevents oscilloscope overload when using the most sensitive vertical input ranges. Set this switch to the GI position for normal operation.

NORM/DIFF Two-position slide switch mounted on the printed circuit board selects the normal (NORM) or differential (DIFF) input modes. In the NORM position, both front- and rear-panel INPUT connectors function as the same normal input for the preamplifier signal cable. In the DIFF mode the rear-panel INPUT connector becomes a differential ground reference input, and the front-panel INPUT remains the normal input for the preamplifier signal cable. In the DIFF mode the preamplifier signal cable is connected to the front-panel INPUT, and a cable having its center conductor connected to the preamplifier ground through an impedance matching resistor is connected to the rear-panel INPUT. The impedance-matching resistor must match the output impedance of the preamplifier.

BAL (Differential Input Gain Balance) A 12-turn potentiometer mounted on the PC board inside the module allows the gains of the normal and differential reference inputs to be matched for maximum common mode noise rejection in the DIFF mode.

PUDEL PC-board mounted, 12-turn potentiometer adjusts the pile- up delay in order to minimize the pulse-pair resolving time of the pile-up rejector to the limit set by the charge collection time of the germanium detector.

<1 Ω/93 Ω Printed circuit board jumper W7 selects the output impedance of the rear-panel GI OUTPUT to be either <1 Ω, or 93 Ω.

PUR/PUR* Printed circuit board jumper W5 selects the rear-panel PUR outputs to be active high (PUR), or active low (PUR*).

INH/INH* Printed circuit board jumper W6 selects the rear-panel INH INput to be active high (INH), or active low (INH*).

BSY/BSY* Printed circuit board jumper W3 selects the rear-panel BUSY output to be active high (BSY), or active low (BSY*).

2.3. INPUTS

INPUT (Front Panel) BNC connector accepts preamplifier signals of either polarity with rise times <600 ns, and exponential decay times of 40 μs to infinity. For the NEG INPUT switch setting, the input impedance is 465 Ω for a gain jumper setting of ×1, and 1 kΩ for a gain jumper setting of ×0.5. For the POS INPUT switch setting, the input impedance is 1460 Ω for a gain jumper setting of ×1, and 2 kΩ for a gain jumper setting of ×0.5. The input is dc-coupled and protected to ±25 V.

INPUT(Rear Panel) BNC connector. Identical to the front-panel INPUT when the NORM/DIFF slide switch is in the NORM position. When operating in the differential input mode with the slide switch set to DIFF, the rear-panel INPUT is used for the preamplifier ground reference connection. The input is dc- coupled and protected to ±25 V.

INH IN Rear-panel, BNC, inhibit input connector accepts the reset signal from a transistor-reset preamplifier. Positive NIM standard logic pulses or TTL levels can be used. The logic is selectable as active high or active low via printed circuit board jumpers. The inhibit input initiates the protection against distortions caused by preamplifier reset. This includes turning off the baseline restorers, monitoring the negative overload recovery at the prefilter output, and generating PUR (reject) and BUSY signals for the duration of the overload. The PUR and BUSY logic pulses are used to prevent analysis and correct for the reset dead time in the associated ADC or multichannel analyzer.

2.4. OUTPUTS

OUTPUT Front-panel BNC connector provides either the gated integrator output pulse or the diode-limited prefilter output pulse, depending on the PZ ADJ/GI switch position. The diode-limited prefilter output is used only during PZ adjustment (See PZ ADJ/GI switch description). For normal operation with the PZ ADJ/GI switch in the GI position, the front-panel OUTPUT delivers the positive, gated integrator output pulses. These pulses are linear over the range from 0 to +10 V. The output is dc-coupled, with an output impedance <1 Ω, a dc-offset <±2 mV, and is short-circuit protected.

GI OUTPUT Rear-panel BNC connector always provides the GI output pulses, independent of the PZ ADJ/GI switch position. Otherwise, the GI OUTPUT is identical to the front-panel OUTPUT. The output impedance of the rear-panel GI OUTPUT is selectable between 93 Ω and <1 Ω using a printed circuit board jumper.

PUR The rear-panel, Pile-Up Reject output is provided on a LEMO connector and a BNC connector, wired in parallel. Both outputs generate a +5-V, TTL-compatible, logic pulse when pulse pile-up is detected. The PUR output is also present for a transistor-reset preamplifier during reset, and reset overload recovery. The output is selectable as active high or active low by means of a printed circuit board jumper. Output impedance is 50 Ω. Used with an associated ADC or multichannel analyzer to prevent analysis of distorted pulses.

CRM The Count Rate Meter output has a rear-panel BNC connector and provides a 100-ns-wide, +5-V, TTL compatible, logic signal for every linear input pulse that exceeds the pileup inspector threshold. Output impedance is 50 Ω.

BUSY The rear-panel, BNC connector provides a +5-V, TTL compatible, logic pulse for the duration that the linear signals exceed the positive or negative baseline restorer threshold, or the pileup inspector threshold, or for the duration of the INH IN input signal. Useful for dead time corrections with an associated ADC or multichannel analyzer. The BUSY output is selectable as active high or active low via a printed circuit board jumper. Output impedance is 50 Ω.

PREAMP POWER Rear-panel, standard EG&G ORTEC power connector (Amphenol 17-10090) provides power for the associated preamplifier (±24 V, ±12 V, and ground). Mates with power cords on all standard EG&G ORTEC preamplifiers.

2.5. ELECTRICAL AND MECHANICAL

POWER REQUIRED The Model 973 derives its power from a NIM bin supplying ±24 V and ±12 V, such as the EG&G ORTEC 4001A/4002A Bin and Power Supply. The power required (excluding preamplifier) is +24 V at 65 mA, +12 V at 330 mA, −12 V at 235 mA, and −24 V at 120 mA.

WEIGHT
Net 1.5 kg (3.3 lb).
Shipping 3.1 kg (7.0 lb).

DIMENSIONS Standard single-width NIM module, 3.45 × 22.13 cm (1.35 × 8.714 in.) front panel per TID-20893 (Rev).

3. INSTALLATION

3.1. POWER CONNECTION

The Model 973 operates on power that must be provided by a NIM-standard bin and power supply such as the EG&G ORTEC 4001/4002 series. Use the convenient test points on the power supply control panel to check the dc voltage levels to ensure that they are not overloaded. The bin and power supply is designed for relay rack mounting. If the equipment is rack mounted, be sure that there is adequate ventilation to prevent any localized heating of the components that are used in the Model 973. The temperature of the equipment mounted in racks can easily exceed the maximum limit of 50° C unless precautions are taken.

3.2. PREAMPLIFIER CONNECTION

The PREAMP connector of this amplifier is directly compatible with EG&G ORTEC preamplifiers as well as with standard Aptec, Canberra, PGT, and Tennelec (serial numbers >2000) preamplifiers. Preamplifier power at +24 V, −24 V, +12 V, and −12 V is available through the PREAMP connector on the rear panel.

When a BNC cable longer than 10 ft is used to connect the preamplifier output to the amplifier input, the characteristic impedance of the cable should match the impedance of the preamplifier output. All EG&G ORTEC preamplifiers contain series terminations that are either 93 Ω or variable; coaxial cable type RG-62/U or RG-71/U is recommended.

3.3. PULSED RESET PREAMPLIFIERS AND INHIBIT IN CONNECTIONS

The Model 973 Amplifier is directly compatible with most pulsed-reset preamplifiers such as the EG&G ORTEC TRP (Transistor-Reset Preamplifier) Series. The amplifier automatically senses preamplifier resets and gates off the amplifier's baseline restorer. The amplifier will operate without using the preamplifier inhibit signal. However, connection of the preamplifier inhibit signal is recommended to avoid spurious phantom peaks in the spectrum.

PZ SETTING The Amplifier's PZ control should be set fully counterclockwise (CCW) when used with a pulsed-reset preamplifier. The front-panel control is marked with an arrow labeled TRP to indicate the direction to turn the control.

INHIBIT IN Connection of the PREAMPLIFIER INHIBIT OUT signal to the rear-panel INHIBIT IN connector will result in the system's being disabled during the reset period; this avoid spurious peaks in the spectra. Preamplifiers with an Inhibit time switch (such as EG&G ORTEC PLUS Detector with a Series 132 Preamplifier) can be set to position 1, which is the shortest preamplifier inhibit blocking time.

Operation with Energy Rates above 10^5 MeV/s If the count-rate during an experiment is expected to be above ~1×10^5 MeV/s (~1×10^5 cps of ^{60}Co), the low/high rate jumper located in the electronics compartment of the EG&G ORTEC PLUS detector should be set to "high." In addition, for maximum throughput with EG&G ORTEC PLUS detectors, the 132 Inhibit Generator box should be modified so that the inhibit pulse exists only during the actual reset time (5 μs) of the preamplifier. Details of these changes can be found in the EG&G ORTEC PLUS Detector Operating Manual.

3.4. CONNECTION OF A TEST PULSE GENERATOR

THROUGH A PREAMPLIFIER The satisfactory connection of a test pulse generator (such as the EG&G ORTEC 419 or 448 Pulse Generator or equivalent) depends primarily on two considerations; the preamplifier must be properly connected to the Model 973 as discussed in Sections 3.2 and 3.3, and the proper signal simulation must be applied to the preamplifier. To ensure proper input signal simulation, refer to the instruction manual for the particular preamplifier being used.

DIRECTLY INTO THE MODEL 973 The EG&G ORTEC test pulse generators are designed for direct connection. When any one of these units is used, it should be terminated with a 100-Ω terminator at the amplifier input or be used with at least or one of the output attenuators set at IN.

SPECIAL CONSIDERATIONS FOR POLE-ZERO CANCELLATION When a tail pulse generator is connected directly to the amplifier input, the PZ ADJ should be adjusted. See Section 4.3 for the pole-zero adjustment. If a preamplifier is used and a tail pulse generator is connected to the preamplifier test input, it is not possible to adjust the pole-zero for both the preamplifier pole and the pole from the pulse generator tail.

3.5. SHAPING CONSIDERATIONS

The INTEGRATE time switch on the front panel of the Model 973 can be set to select integration times for the gated integrator of 2.5 or 5 μs. The choice of the proper shaping time is generally a compromise between operating at a shorter time constant for accommodation of high counting rates and operating with a longer time constant for a better signal-to-noise ratio.

3.6. GI LINEAR OUTPUT CONNECTION AND TERMINATING CONSIDERATIONS

Since the Model 973 GI (Gated Integrator) output is used for spectroscopy, the Model 973 is designed with a great amount of flexibility in order for the pulse to be interfaced with a pulse-height analyzer. To minimize spectrum distortion at medium and high counting rates, the prefilter output incorporates a high-performance, gated baseline restorer with automatic setup. Automatic positive and negative noise discriminators ensure that the baseline restorer operates only on the true baseline between pulses in spite of changes in the noise level. For pulse-height analysis, the GI output must be directly connected to the input of a multichannel analyzer.

CABLE TERMINATION An unterminated output cable may cause output stage ringing and even oscillation when the cable length is >6 ft or 2 m. The relatively fast reset at the end of the integration is more likely to cause a problem than a semi-Gaussian shaped pulse.

Three general methods of termination are used. The simplest of these is shunt termination at the receiving end of the cable. A second method is series termination at the sending end. The third method is a combination of series and shunt termination, in which the cable impedance is matched both in series at the sending end and in shunt at the receiving end. The combination is most effective, but this reduces the signal amplitude at the receiving end to 50% of that available in the sending instrument.

To use shunt termination at the receiving end of the cable, connect the <1Ω front or rear (jumper W2 = 1Ω) panel output of the Model 973 through 93-Ω cable (such , at RG/62AU) to the input of the receiving instrument. Then use a BNC tee connector to attach both the interconnecting cable and a 100-Ω terminator at the input connector of the receiving instrument. If the input impedance of the receiving instrument is 1000 Ω or more, the effective instrument input impedance with the 100-Ω terminator will be of the order of 93 Ω, and this matches the cable impedance correctly.

For series termination, use the 93-Ω rear-panel output of the Model 973 for the cable connection (jumper W7 = 93 Ω). Use 93-Ω cable to interconnect with the input of the receiving instrument. The 1000 Ω (or more) normal input impedance at the input connector represents an essentially open circuit, and the series impedance in the Model 973 provides the proper termination for the cable.

For the combination of series and shunt termination, use the 93-Ω rear panel output of the Model 973 (jumper W7 = 93 Ω) and use 93-Ω cable. At the input of the receiving instrument, use a BNC "T" to attach both the signal cable and a 100-Ω resistive terminator. Note that the signal span at the receiving end of this type of circuit will always be reduced to 50% of the signal span furnished by the sending instrument.

For customer convenience, EG&G ORTEC stocks the proper terminators and BNC tees, or they can be ordered from a variety of commercial sources.

3.7. PILE-UP REJECTION USING THE PUR OUTPUT

The PUR (Pile-Up Reject) output on the rear panel is used at the gate or pile-up reject input of a multichannel analyzer to suppress pile-up in the recorded spectrum. The fast amplifier in the pile-up rejector includes a gated baseline restorer with an automatic noise discriminator to eliminate the need for any operator adjustments. When pile-up occurs, a logic true pulse is generated that lasts until the prefilter waveform returns to the baseline, normally a width of the Integrate time plus 0.5 μs. If used with a pulsed reset preamplifier, this output also includes a reject during the reset and recovery interval. If the gate input of the multichannel analyzer is used with the PUR signal, set the gate switch on the multichannel analyzer to anti-coincidence.

3.8. LIVETIME CORRECTION USING THE BUSY OUTPUT

The signal from the rear-panel Busy output connector provides a nominally +5 V logic pulse for the duration of internal Busy time. The Busy time is the logical OR of the gated integrator Busy, or the pile-up inspection time or when the external INHIBIT IN is true. For livetime correction, Busy should be connected to the Busy In connector on the MCA. The output is internally jumper selectable as active low or active high. It is shipped as active high.

3.9. INPUT COUNT-RATE USING THE CRM OUTPUT

A positive logic pulse is generated for each Model 973 input pulse that exceeds the pile-up inspector threshold level. The pulses are available through the CRM (Count Rate Meter) output on the rear panel and are intended for use with a count-rate meter or counter to monitor the true input count-rate into the amplifier.

4. OPERATION

4.1. INITIAL TESTING AND OBSERVATION OF PULSE WAVEFORMS

Refer to Section 6 for information on testing performance and observing waveforms using a pulse generator. Figure 4.1 shows some typical Prefilter and GI (Gated Integrator) output waveforms.

4.2. STANDARD SETUP PROCEDURES

a. Connect the detector, preamplifier, high voltage power supply, and amplifier into a basic system and connect the amplifier output to an oscilloscope. Connect the preamplifier power cable to the PREAMP power connector on the rear panel of the Model 973. Turn on

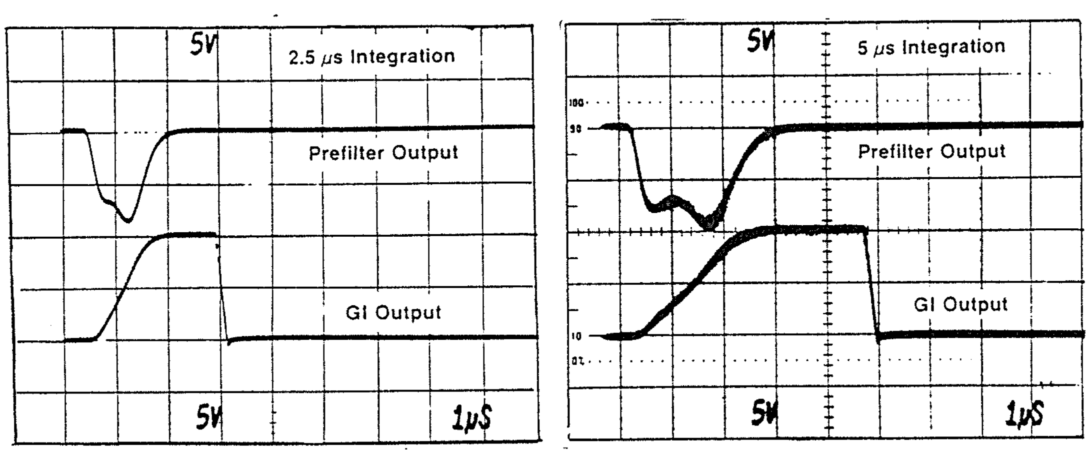

Fig. 4.1. Typical Output Waveforms.

power in the bin and power supply and allow the electronics of the system to warm up and stabilize.

A block diagram of a typical EG&G ORTEC gamma spectroscopy system is shown in Figure 4.2.

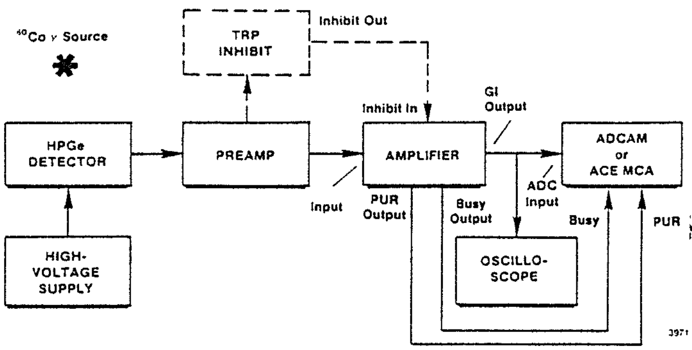

Fig. 4.2. Typical Gamma Spectroscopy System.

b. Set the Model 973 controls initially as follows:

INTEGRATE	5 μs or 2.5 μs
OUTPUT	GI
COARSE GAIN	20
FINE GAIN	1.00
POS or NEG	Match preamplifier output polarity

c. Use a ^{60}Co calibration source, located about 25 cm from the active face of the detector. The GI output pulse from the Model 973 should be about 6 V, using a detector that has a preamplifier with a conversion gain of 300 mV/MeV.

d. Readjust the Gain control so that the higher peak from the ^{60}Co source (1.33 MeV) provides an amplifier output at about 8 V.

4.3. POLE-ZERO ADJUSTMENTS FOR RESISTIVE-FEEDBACK PREAMPLIFIER

The pole-zero adjustment is extremely critical for good performance at high count-rates and for correct

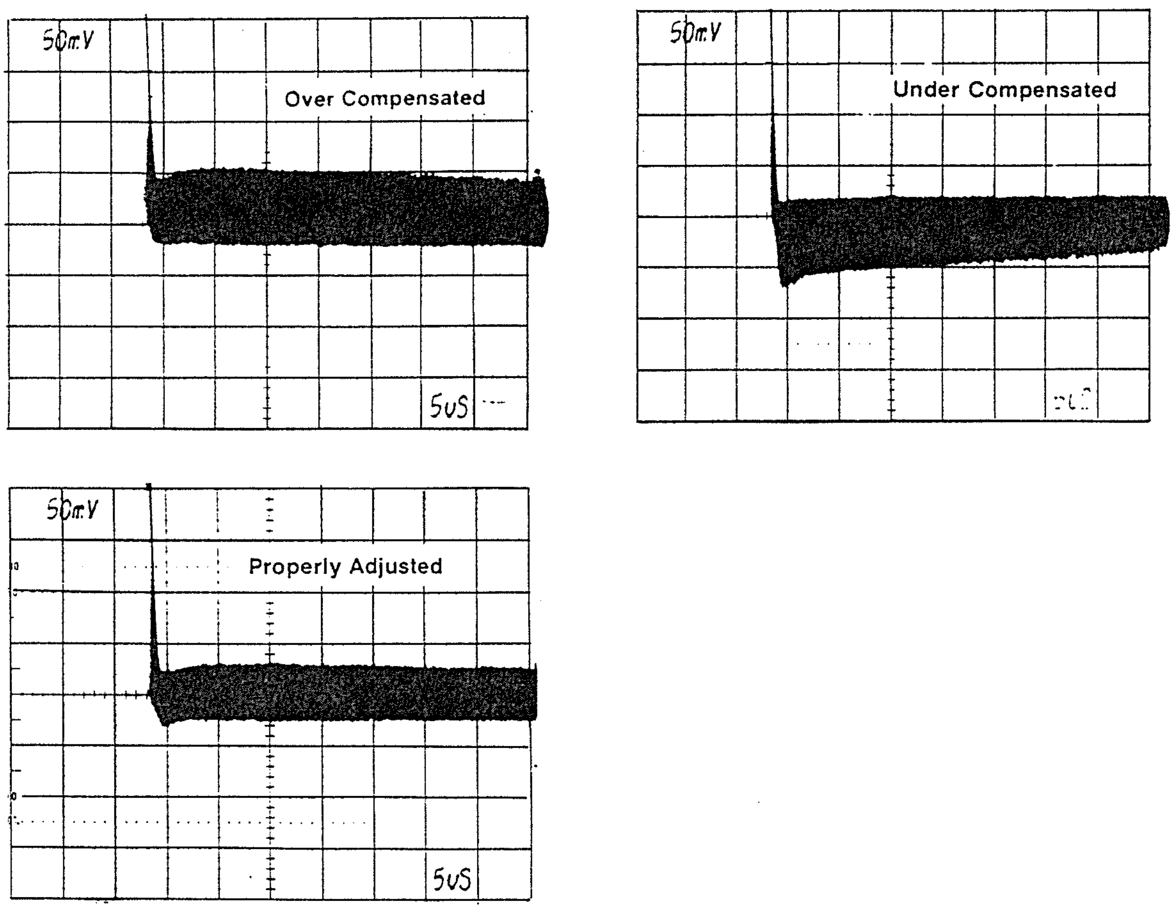

Fig. 4.3. Typical Waveforms Illustrating Pole-Zero Adjustment Effects.

operation of the BLR circuit. This adjustment should be checked carefully for the best possible results. Whenever the shaping time is changed, the pole-zero must be adjusted. When using a transistor-reset preamplifier, the PZ should be set to the full counterclockwise position.

USING AN HPGe SYSTEM AND ^{60}Co

a. Adjust the radiation source spacing from the detector to provide a count-rate between 1 and 10 kHz.

b. Set the front-panel OUTPUT switch to PZ ADJ, and observe the Output with an oscilloscope. Increase the oscilloscope input sensitivity to 20 to 100 mV per vertical division. Note that the Prefilter pulse is diode limited to approximately 0.6 V to prevent oscilloscope overload during adjustment. Adjust the PZ ADJ control so that the trailing edge of the pulses returns to the slight bias toward an undershoot often gives the best baseline without overshoot or undershoot (Fig. 4.3). A slight bias toward an undershoot often gives the best results. The PZ adjustment in a gated integrator system is far more demanding than in a standard semi-Gaussian shaping amplifier because small misadjustments may cause significant spectral distortions.

The oscilloscope used must be dc-coupled and must not contribute distortion in the observed waveforms.

USING A SQUARE WAVE THROUGH THE PREAMPLIFIER TEST INPUT

A more precise manual pole-zero adjustment of the amplifier can be obtained by using a square wave signal as the input to the preamplifier. Many oscilloscopes include a calibration output on the front panel; this is a good source of square wave signals at a frequency of

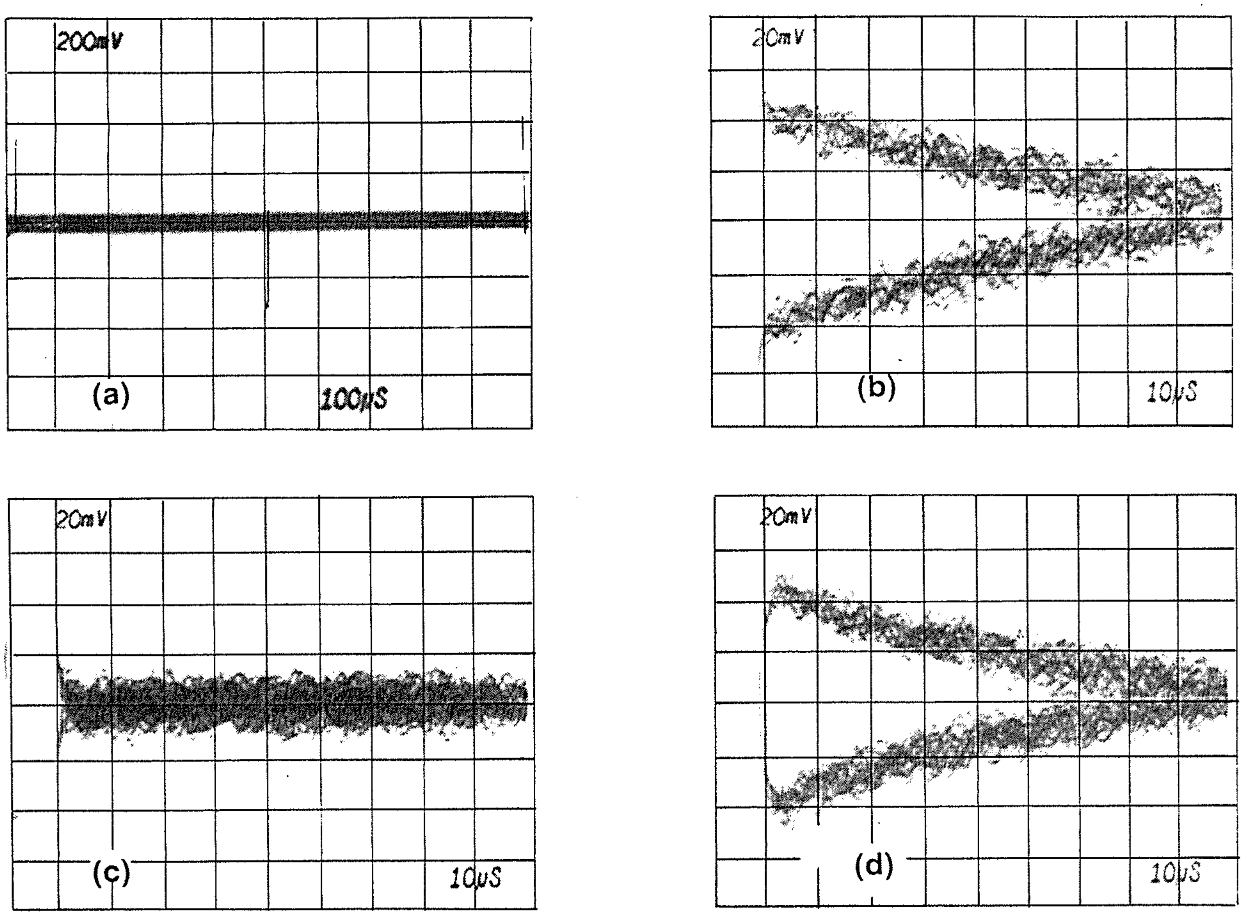

Fig. 4.4. Pole-Zero Adjustment Using a Square Wave Input to the Preamplifier: (a) PZ Properly Adjusted, Slow Trigger to Separate Pulses; (b) Overcompensated, Fast Trigger to Superimpose Pulses; (c) Properly Adjusted, Pulses Superimposed; (d) Undercompensated, Pulses Superimposed.

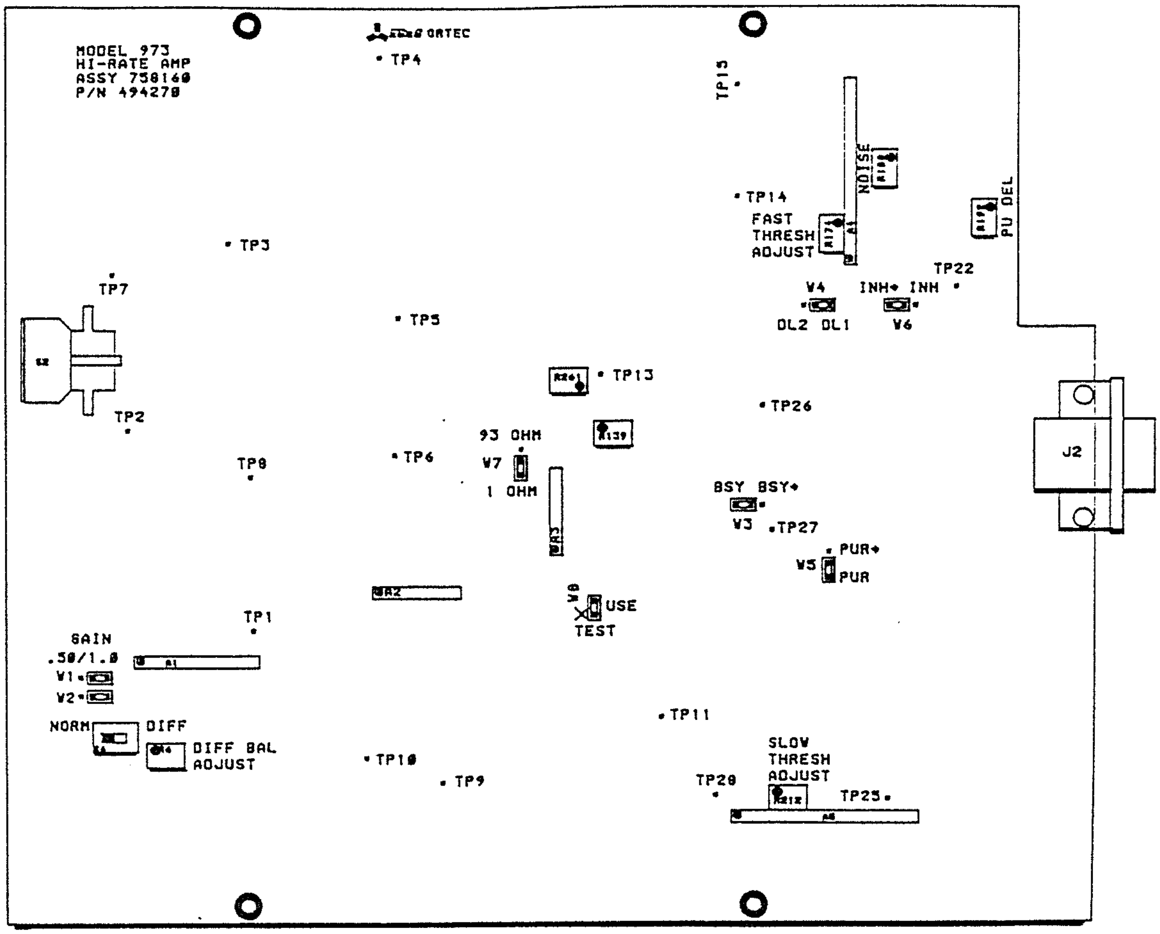

Fig. 4.5. Position of Internal Controls.

about 1 kHz. The amplifier differentiates the signal from the preamplifier so that it generates output signals of alternate polarities on the leading and trailing edges of the square wave input signal. These can be compared, as shown in Fig. 4.4, to achieve excellent pole-zero cancellation.

Use the following procedure;

a. Remove all radioactive sources from the vicinity of the detector. Set up the system as for normal operation, including detector bias.

b. Set the amplifier controls as for normal operations; this includes gain, shaping, and input polarity.

c. Connect the source of 1-kHz square waves through an attenuator to the Test input of the preamplifier. Adjust the attenuator so that the amplifier output amplitude is 8–10 volts.

d. Set the Output switch to PZ ADJ and observe the Output of the amplifier with an oscilloscope triggered from the amplifier Busy output. Adjust the PZ control for proper response according to Fig. 4.4.

Figure 4.4a shows the amplifier output as a series of alternate positive and negative shaped pulses. In b, c, and d of this figure, the oscilloscope was triggered to superimpose both positive and negative pulses simultaneously. These pictures show more detail to aid in proper adjustment.

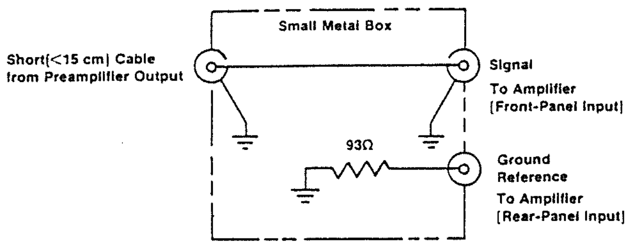

Fig. 4.6. Preamplifier Ground Reference.

4.4. BASELINE RESTORER (BLR)

The BLR rate for the baseline restorer at the output of the gated integrator Prefilter is automatically set for optimum performance throughout the usable input range for the shaping times selected. To minimize spectrum distortion at medium and high counting rates, the unipolar output incorporates a high-performance, gated, baseline restorer with several level of automation. Automatic positive and negative noise discriminators ensure that the baseline restorer operates only on the true baseline between pulses in spite of changes in the noise level. No operator adjustment of the baseline restorer is needed when changes are made in the gain, the shaping time constant, or the detector characteristics. Negative overload recovery from the reset pulses generated by transistor-reset preamplifiers is also handled automatically to eliminate the need for operator adjustments. A monitor circuit gates off the baseline restorer and provides a reject signal for a multichannel analyzer until the baseline has safely recovered from the overload.

4.5. INTERNAL CONTROLS

These controls are on the printed wiring board (PWB) and can be accessed by removing the right side cover.
DIFF GAIN BALANCE Internal PWB 20-turn screwdriver potentiometer allows maximization of noise rejection when using the differential input. See Section 4.6.

NORM/DIFF Two-position slide switch mounted to the printed circuit board selects the normal (NORM) or differential (DIFF) input modes (see Section 4.6).

×0.5/×1 Jumper plugs W1 and W2 reduce gain by a factor of 2 for very large preamplifier signals. Shipped in the ×1 position for normal use.

<1 Ω/93 Ω Jumper plug W7 provides Z_{out} less than or equal to 1 Ω or approximately 93 Ω for the rear-panel Output. Shipped in the 93 Ω position.

BUSY/BUSY* Jumper plug W3 allows the Busy output to be a positive true or negative true logic signal. Shipped in BUSY (positive true) position.

PUR/PUR* Jumper plug W5 allows the Pile-Up Reject (PUR) output to positive true or negative true logic signal. Shipped in PUR (positive true) position.

INH/INH* Jumper plug W6 allows the Inhibit In input to accept a positive true or negative true logic signal. Shipped in the INH (positive true) position.

4.6. DIFFERENTIAL INPUT MODE

When long connecting cables are used between the detector and preamplifier input, noise induced in the cable by the environment can be a problem. The differential input mode can be used with paired cables from the preamplifier to suppress the induced noise.

DIFF INPUT SIGNAL The DIFF input signal or phantom is used only in the differential input mode. The normal preamplifier output is connected to the front-panel (NORM) input, with the amplifier input polarity set to match this signal. A second output cable must be added to the preamplifier, with its center signal pin connected to the preamplifier ground with the same value as the normal preamplifier output series resistor (usually 93.1 or 51 Ω).

Many EG&G ORTEC preamplifiers have two Energy outputs, each with a 93.1-Ω series resistor. For differential operation, one output is connector to the amplifier front-panel (NORM) input. The second output is modified by connecting the preamplifier end of the series 93.1-Ω resistor to ground within the preamplifier (soldering may be necessary). This second output should be properly marked and connected to the rear-panel (DIFF) input. Both cables must be the same length and must be run next to each other.

If it is not practical to modify the preamplifier, one can create a ground reference at the preamplifier by utilizing a small shielded box fabricated as shown in Fig. 4.6. The cable from the preamplifier to the metal box should be short (<15 cm). The signal and ground reference cables going to the amplifier differential inputs should be twisted tightly together to maximize the common-mode suppression.

GAIN BALANCE The Gain Balance adjustment is used to adjust the gain balance between the positive and negative inputs and to adjust the balance between the NORM and DIFF inputs when the differential input mode is used. First set the internal NORM/DIFF slide switch to DIFF. The initial adjustment of Gain Balance is made by providing the same input to both the NORM and DIFF inputs. This can be accomplished by using a BNC "T" connector to feed the input signal on the front-panel (NORM) input to the rear-panel (DIFF) input. Set the amplifier gain to maximum. Connect an oscilloscope to the unipolar output. While observing the signal on the oscilloscope, use a small screwdriver to adjust the Gain Balance potentiometer (internal adjustment has been factory set; see Fig. 4.5) until the display on the oscilloscope shows minimum signal. Remove the BNC "T" connector when the adjustment is complete, and the positive and negative gains will be matched for use with the NORM input.

When using the DIFFerential input mode, additional adjustments of the GAIN BALANCE potentiometer must be made to achieve minimum common mode noise after the differential inputs are properly connected. To make this final adjustment, connect the differential signal cables from the preamplifier to the Model 973 and select the DIFFerential input mode. Make sure all parts of the system are connected and operating normally (Fig. 4.2). Select the PZ ADJ output on the front panel of the Model 973 and connect this output to an oscilloscope and/or a wideband rms noise meter for observation of the amplifier output noise. Remove all sources of radiation from the vicinity of the detector. Adjust the GAIN BALANCE potentiometer to minimize the amplifier output noise. If no improvement can be observed, set the potentiometer back to the position determined in the previous paragraph. After the adjustments are completed, return the output switch to the GI position.

4.7. SYSTEM THROUGHPUT

To achieve the desired results in high-rate energy spectroscopy, the experimenter must consider not only the input rate, but also the unpiled-up output rate. The unpiled-up output rate is determined by the processing time of the shaping amplifier, the pile-up inspection time, and the input rate. The unpiled-up output rate is theoretically given by[1]

$$r_o = r_i \exp(-T_d r_i) \quad , \qquad (1)$$

where r_o is the unpiled-up output count-rate, r_i is the input count-rate, and T_d is the deadtime or effective processing time of the amplifier. The value of T_d is equal to the sum of the effective amplifier pulse width T_W and the time-to-peak of the amplifier output pulse T_p. The deadtime for the Model 973 amplifier is equal to $2 \times T_{INT}$ since the pulse width and the time-to-peak are each equal to the integrate time T_{INT}. The type of deadtime in the shaping amplifier is referred to as extending deadtime because a second event arriving before the end of the initial deadtime extends the deadtime by an additional amplifier pulse width (T_{INT}) from the occurrence of the second pulse.

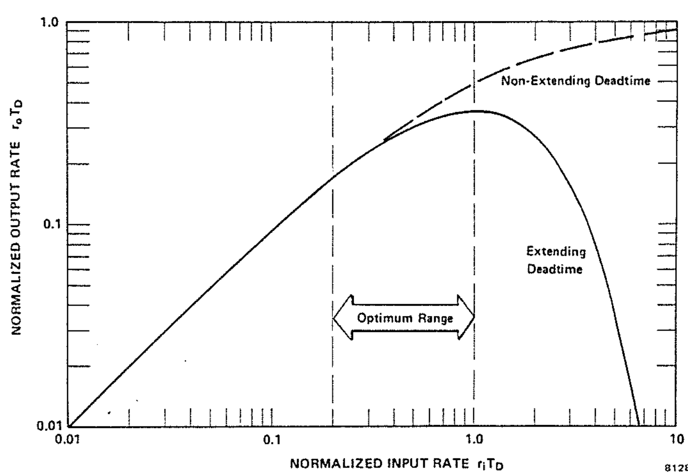

Fig. 4.7. Plot of Normalized Output Rate as a Function of Normalized Input Rate for Spectrometers with Simple Deadtime.

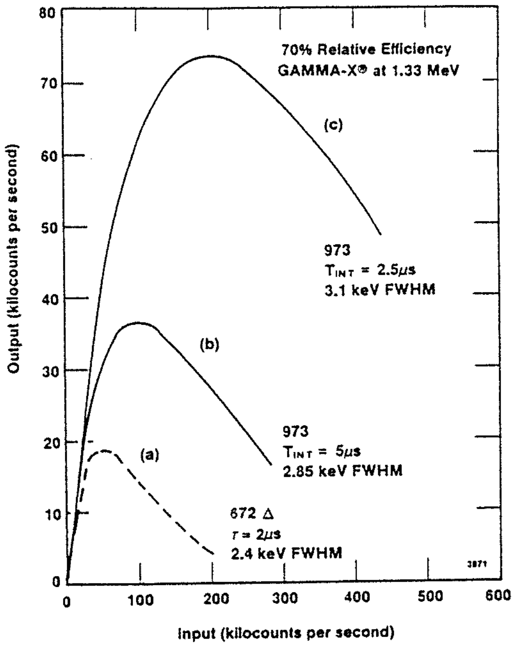

Fig. 4.8. Amplifier Output Counting Rate vs Input Rate is shown for (a) a Model 672 Amplifier with a 2-μs, Triangular Shaping Time Constant, (b) the Model 973 with a 5-μs Integration Time, and (c) the Model 973 with a 2.5-μs Integration Time.

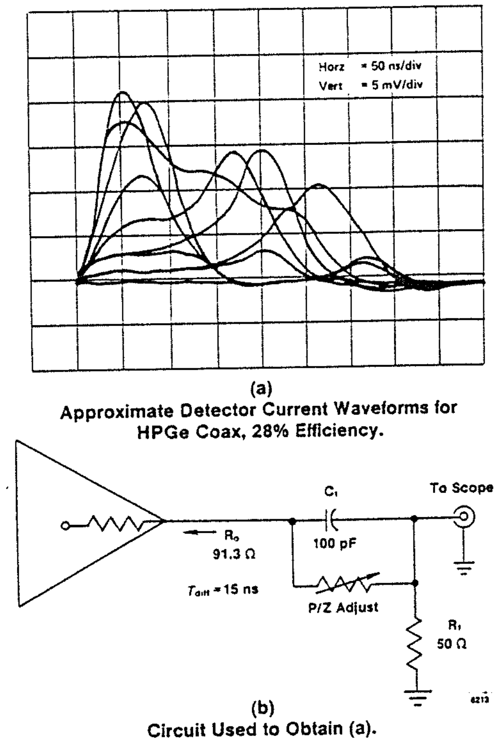

Fig. 4.9. Charge Collection Effect Waveforms. (a) Typical Current Pulse Waveforms for a 28% Efficient HPGe Detector and (b) the Simple Differentiation Circuit used to Obtain the Current Waveforms.

A normalized plot of Equation (1) is shown as the solid line in Fig. 4.7. The maximum mean output rate equals $1/T_d \exp(1)$ and occurs when the mean input rate equals $1/T_d$. At this maximum output rate, the deadtime losses are 63.2%. For input count-rates exceeding $1/T_d$, the unpiled-up output rate decreases as the input rate increases.

Spectroscopy systems also have a deadtime that is caused by the digitizing time of the Analog-to-Digital Converter (ADC). This deadtime is a non-extending deadtime because events arriving during the digitizing time are ignored. For non-extending deadtime, the output rate is given by[1]

$$r_o = \frac{r_i}{1 + r_i T_d} , \qquad (2)$$

where T_d is the digitizing time for the ADC and is designated T_M in Equation (3). This relationship is shown as the dashed line in Fig. 4.7. The maximum obtainable output count-rate is $1/T_d$ and occurs at $r_i = \infty$.

[1] R. Jenkins, R.L. Gould, and D.A. Gedcke, *Quantitative X-Ray Spectroscopy*, New York: Marcel and Dekker, Inc., 1980.

When the ADC is considered as part of the spectroscopy system, the deadtimes of the amplifier and ADC are in series. The combination of the extending deadtime of the amplifier followed by the non-extending deadtime of the ADC is given by[1]

$$r_o = \frac{r_i}{\exp[r_i(2T_{INT})] + r_i T_M} . \qquad (3)$$

Figure 4.8 shows a plot of the unpiled-up amplifier output rate as a function of input rate for two values of integrate time for the Model 973 as compared with a Model 672 triangular shaping time of 2 μs. Compared with conventional amplifiers, the Model 973 offers up to a factor of 3.8 improvement in amplifier throughput, with only a modest increase in energy resolution.

4.8. CHARGE COLLECTION OR BALLISTIC DEFICIT EFFECTS

Charge collection distances in large-volume HPGe detectors are often 3–5 cm, resulting in charge collection times exceeding 500 ns.[2,3,4] These charge collection times are due to the transit time of the holes and the electrons in germanium and are not due to defects in the detector. Figure 4.9a shows some typical current pulse waveforms from a 140-cm^3, 28% efficient HPGe detector. These current pulse waveforms were obtained using the simple differentiation circuit shown in Fig. 4.8b, which has a 15-ns time constant. The current pulses range in duration from 100 ns to greater than 350 ns. Pulses having equivalent total charge but different durations produce different output pulse heights when processed by either a triangular filter amplifier, or a semi-Gaussian filter amplifier. This results in the distortion of the spectrum in direct proportion to pulse amplitude or energy. This distortion is most pronounced at short shaping time constants.

The Model 973 eliminates the ballistic deficit effects to significantly improve the energy resolution at the short shaping time constants required for high counting rates. The spectra shown in Fig. 4.10 for the 1.33-MeV gamma-ray peak from a ^{60}Co source, acquired with (Fig. 4.10a) a Model 672 amplifier with a triangular pulse shape and 0.5-μs time constant, and (Fig.4.10b) the Model 973 amplifier with a 2.5-μs integration time. In both cases the amplifier deadtime per pulse is approximately 5 μs. The detector is a GAMMA-X® detector with a 70% relative efficiency.

Low-rate resolution data (shown in Fig. 4.11) illustrates charge collection effects as a function of deadtime per pulse. The resolution is clearly better using the Model 973 when throughput is important; i.e., when deadtime per pulse must be reduced to less than 20 μs.

4.9. PILE-UP REJECTOR (PUR) AND LIVETIME CORRECTOR

An efficient pile-up rejector is incorporated in the amplifier to suppress the spectral distortion which is caused by pulses piling up on each other at high

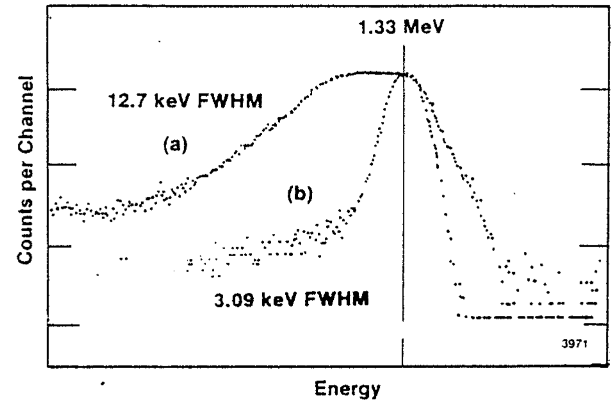

Fig. 4.10. Elimination of Charge Collection Effect: Logarithmic Display of Spectrum Taken with 70% Efficient HPGe Detector for the 1.33-MeV ^{60}Co Line. (a) A Model 672 with 0.5-μs Triangular Shaping Time Constant and (b) a Model 973 with 2.5-μs Integrate Time.

counting rates. The amount of pile-up at high counting rates depends on the deadtime per pulse (T_d), and hence the selected integration time. T_d is two times the front-panel Integrate time (T_{INT}). High count-rate for pile-up rejection occurs when the normalized count-rate $r_i \cdot T_d > 0.5$, where r_i is the amplifier input rate (see Fig. 4.7). For example, for 5-μs integration, r_i is 50 kHz; for

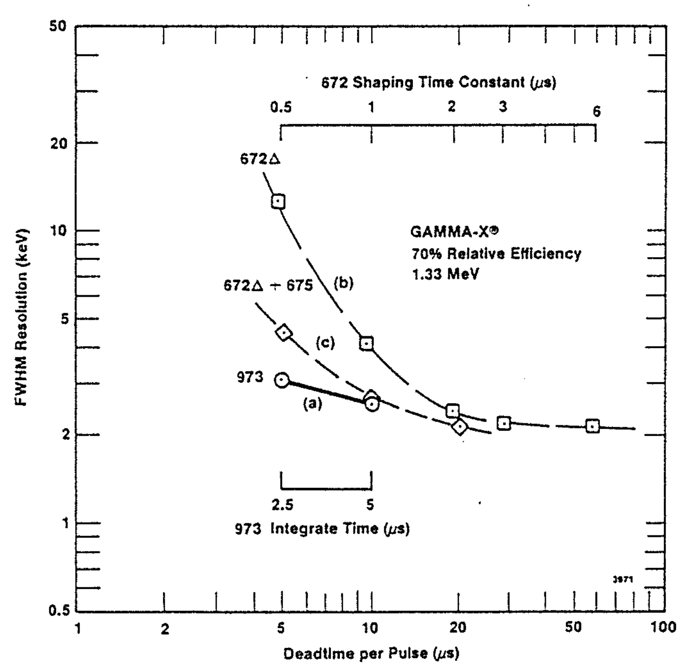

Fig. 4.11. Energy Resolution vs Deadtime per Pulse: (a) the Model 973, (b) the Model 672 Triangular Filter Amplifier, and (c) the Model 672 Plus the Model 675 Ge Resolution Enhancer.

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[2] E. Sakai, "Charge Collection in Coaxial Ge(Li) Detectors," *IEEE Trans. Nucl. Sci.*, NS-15, 310, 1968.

[3] E. Sakai, T.A. McMath, and R. G. Franks, "Further Charge Collection Studies in Coaxial Ge(Li) Detectors," *IEEE Trans. Nucl. Sci.*, NS-16, 68, 1968.

[4] T.H. Becker, E.E. Gross, and R.C. Trammell, "Characteristics of High-Rate Energy Spectroscopy Systems with Time-Invariant Filters," *IEEE Trans. Nucl. Sci.*, NS-28, 1, 1981.

2.5-μs integration, r_i is 100 kHz. Amplifier throughput forthis condition using Equation (1) in Section 4.7 is 60% of the input rate. A multi-color pile-up rejector LED is included on the front panel to indicate the throughput efficiency of the amplifier. At low counting rates (pulse pile-up losses less than 40%), the LED flashes with a green color. At moderate counting rates, the color changes to yellow. The color changes to red at high counting rates when the pulse pile-up losses are greater than 70%.

The fast amplifier in the pile-up rejector includes a gated baseline restorer with its own automatic noise discriminator to eliminate the need for any operator adjustments. This function is also protected against negative overloads from pulsed reset preamplifiers. The PUR (pile-up reject) output logic pulse can be used at the gate or reject input of a multichannel analyzer to suppress pile-up in the recorded spectrum. If the gate input is used, set the gate mode switch on the multichannel analyzer to the anti-coincidence mode.

The block diagram for a Gamma System with pile-up rejection and livetime correction is shown in Fig. 4.12.

To use the pile-up rejector, make the following connections.

a. PUT Output pulse from Model 973 to ADC PUR or ADC anticoincidence input.

b. Livetime correction signal (Busy output) to the ADC Busy In.

c. ADDITIONAL CONNECTION FOR TRP (Transistor-Reset Preamplifiers) is shown by dashed lines. Inhibit Output from TRP to the amplifier Inhibit In.

d. For optional adjustment of PUR delay, see Section 5.15.

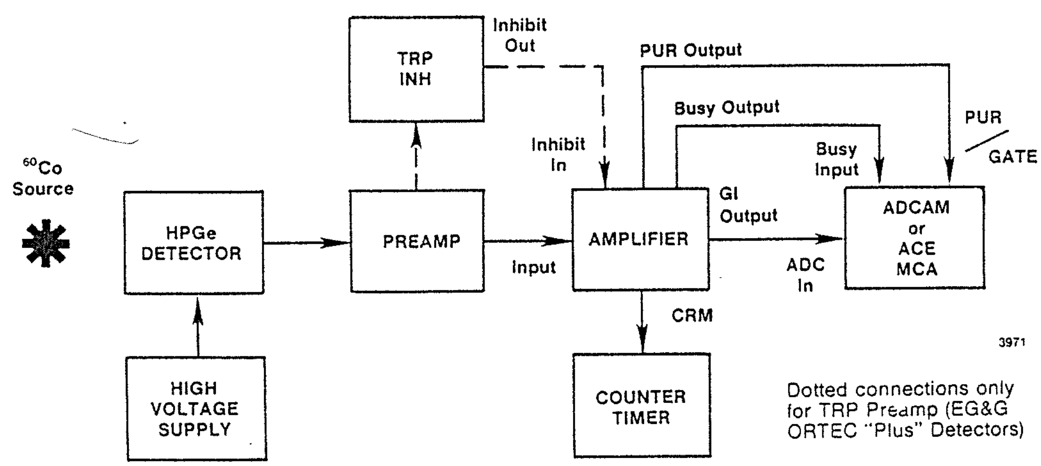


Fig. 4.12. Pile-up Rejection and Livetime Correction Block Diagram.

5. CIRCUIT DESCRIPTION

5.1. INTRODUCTION

The schematic diagrams for the Model 973 High-Rate Spectroscopy Amplifier and Pile-Up Rejector are included at the back of this manual. A block diagram of the amplifier is also located at the back of the manual.

5.2. INPUT POLARITY AND MODE SWITCH

The Input Polarity and Mode switch selects either the Normal or Differential Input mode of operation and the input polarity (positive or negative). When the amplifier is in the Differential Input mode, the DIFF REF input is used to cancel common mode pick-up introduced through the preamplifier ground. The DIFF REF input is connected to the preamplifier ground through a resistance that is equal to the output impedance (93 or 100 Ω for most ORTEC preamplifiers) of the normal preamplifier output. This provides two noise signals to the Model 973 Amplifier, which uses the Differential Input Amplifier to cancel the common mode noise.

5.3. DIFFERENTIAL INPUT AMPLIFIER STAGE

The Differential Input Amplifier provides gain and buffering of the input signal/s from the Input Polarity and Mode Switch. The analog input signal to the Differential Input Amplifier may be either a staircase of step pulses from a Pulsed-Reset Preamplifier or a series of step pulses with exponential decay from a dc (resistor/continuous) Feedback Preamplifier. When the amplifier is in the Differential Input mode, the DIFF REF input cancels common mode pickup introduced through the preamplifier ground.

The output pulse is positive with a gain of 1.8 for a PWB Gain jumper selection of ×1.0, and a gain of 0.9 for PWB Gain of 0.5. The output of this stage is provided to the Differentiator and First Coarse Gain stage and to the Pole-Zero circuit.

5.4. DIFFERENTIATOR AND FIRST COARSE GAIN STAGE

The Differentiator and Coarse Gain stage differentiates; provides a gain of 0.82, 1.64, 4.4, and 8.8; and inverts the analog signal from the Input Amplifier. The output of this stage is provided to the second Coarse Gain stage. The differentiator network contains two capacitors, C5 and C6, which are selected to set the time constant for the first real pole.

The PZ circuit connects the front panel PZ ADJ pot R5 through the selected resistors R17 and R18 to the input of the Differentiator stage. Switching is accomplished by relay RLY1. Pole-zero cancellation is used to compensate for pulse undershoot when the trailing edge of a differentiated pulse is returning to the baseline. The trailing edge of the pulse should return to the baseline as quickly as possible without undershoot. Proper adjustment prevents spectral resolution degradation and peak shift at high counting rates. Pole-zero cancellation adjustment procedures are listed in Section 4.

5.5. SECOND COARSE AND FINE GAIN STAGE

The Coarse Gain stages provide coarse gain settings from 2.5 to 250. The coarse gain of 5 results from reducing the gain of the Differential Input Amplifier as discussed in Section 5.3. The amplifier's second coarse gain is accomplished by inverting amplifier U2. The gain of this stage is switched to 1.7, 3.4, or 8.4 by means of the front panel Coarse Gain switch S2.

The output of Coarse Gain stage U2 is sent to the Integrator stages, the Fast Amplifier, and the Gain DC stabilizer.

5.6. GAIN DC STABILIZER

The Gain DC Stabilizer circuitry is used to maintain the dc level at the output of Coarse Gain stage U2 near zero volts over the range of gains and temperatures. The

Gain DC Stabilizer circuitry monitors the output of Coarse Gain U2, integrates the error voltage, and produces an offset current through R19 to the Differentiator stage to slowly restore the output to zero volts. The time constant is long enough to be neglected in the overall transfer function of the amplifier.

5.7. INTEGRATOR STAGES

Three Sallen-Key type Integrator stages (F1, F2, and F3) provide three complex pole pairs to the pulse shaping prior to being sent to the Prefilter amplifier. Two pairs of resistors are available in each network for selection of the desired shaping time constant. The output pulses from the third Integrator stage are nearly Gaussian.

5.8. PREFILTER AMPLIFIER STAGE

The Prefilter stage provides the final amplification, shaping, and baseline restoration for the PZ ADJ output and Gated Integrator input. The gain provided is negative 2.9, and the second real pole is implemented with a time constant of 1/3 the Input Differentiator. The Prefilter 'Camel' shaping sums fractions of the amplified differentiated signal (Fo) and the first Integrator output (F1) with the third Integrator output (F3) through inverting amplifier U9/A2.

5.9. DELAY AMPLIFIER STAGE

The output of the Prefilter is also provided to the Gated Integrator stage through a 200-ns delay line and inverting amplifier.

5.10. GATED BASELINE RESTORER

The Gated Baseline Restorer (BLR) circuit centers the Prefilter output noise band around ground between pulses. The BLR circuit consists of the "gain of 7" amplifier (U10), gated transconductance amplifier (U8), and capacitor (C53). The capacitor (C53), averages the noise and dc-level at the Prefilter output at a rate set by the automatic BLR Rate circuit. The charge on the capacitor is used to control the offset to the positive input of the Prefilter output stage. The transconductance amplifier is gated off when a signal is present to prevent the baseline from shifting as the count-rate varies.
The restoration rate is set by controlling the current through the transconductance amplifier. The current and thus the BLR Rate is very low when the rate (duty cycle) is low, so that PZ observation is not disturbed. The restoration rate is automatically increased as the count-rate increases, taking into account the shaping time, as the dead time increases.

5.11. SLOW DISCRIMINATORS

The Slow Discriminators monitor the Unipolar Output signal to determine when selected thresholds are reached. The Slow Discriminator circuitry contains: an Automatic Noise Level Sensor (A5), a Slow Positive Discriminator (U31A), and a Slow Negative Discriminator (U31B). The Automatic Noise Level Sensor sets the threshold level for the Positive Discriminator just above noise. The threshold for the Negative Discriminator is three times the noise level set for the Positive Discriminator. Only pulses that exceed the Automatic Noise Level Sensor threshold will produce outputs from the Slow Discriminators. The outputs from the discriminators are used to gate off the Gated Baseline Restorer when a pulse is detected.

5.12. FAST DIFFERENTIATOR AND AMPLIFIER

The Fast Differentiator and Amplifier process the output of Coarse Gain B to provide a dc-restored, pole-zeroed, 90-ns differentiated signal to the Fast Discriminator. A gated transconductance amplifier (U20) accomplishes the Fast Gated BLR function.

5.13. FAST DISCRIMINATOR

The Fast Discriminator monitors the output of the Fast Amplifier to determine when the Fast Amp signal threshold is reached. The Fast Discriminator circuitry contains a Fast Auto Noise Sensor to set the threshold of the Fast Discriminator just above the noise in the Fast Channel. An output from the Fast Discriminator (FD) is sent to the CRM generator and its leading edge starts the gate period for the gated integrator and initiates BUSY.

5.14. CRM GENERATOR

The CRM generator is initiated by the fast discriminator (FD). Figure 5.1. shows the timing relationship between FD and NOISE and PUDEL pulses. In a germanium detector system, FD will have a family of pulse widths determined by the charge collection times of particular events in the germanium detector. Two circuits generate the NOISE and PUDEL pulses shown in Fig. 5.1. The NOISE circuit reduces sensitivity to noise when it triggers the fast discriminator. The NOISE circuit output is generated only if the width of FD is >100 ns.

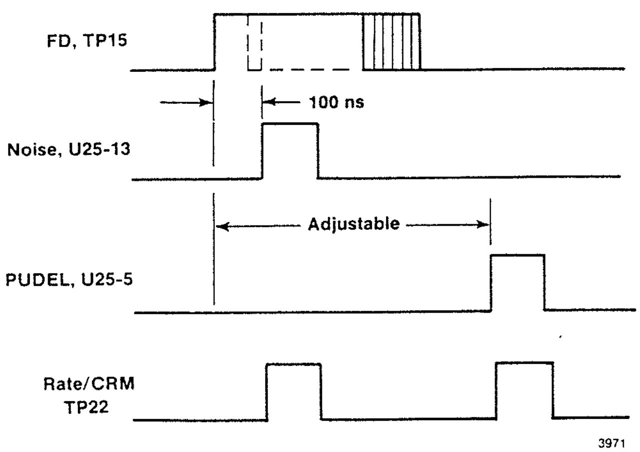


Fig. 5.1. Generation of CRM from Fast Discriminator.

The pile-up delay, PUDEL, circuit only gives an output if the FD lasts longer than the PUDEL delay setting which is factory set to 1 μs. Pulse pile-up is indicated if FD lasts longer than the delay setting. A more accurate representation of the input rate is then obtained by the logical "OR" of NOISE and PUDEL. The combined signal is RATE, which is output to the rear panel as CRM.

5.15. OPTIONAL ADJUSTMENT OF PUR DELAY

The optimum delay time for PUDEL is a function of the detector charge collection characteristics. Good pile-up rejection is obtained with the factory setting of the delay, but improved performance can be obtained by performing the optional delay optimization procedure.

Initial system setup of amplifier polarity, gain, and pole-zero should be done before adjusting the pile-up delay, PUDEL. Place a source near the detector to give an average count rate of about 5K counts per second. Channel 1 of a two channel oscilloscope should be connected to FD (test point 15) and should be selected as the positive trigger channel. Connect channel 2 to RATE/CRM (test point 22); the display should resemble Fig. 5.2a (delay too long).

Shorten the PUDEL delay time by turning potentiometer R192 counterclockwise until the leading edge of PUDEL (second pulse) falls within the charge collection family of FD as shown in Fig. 5.2b (delay too short). PUDEL should now fire regularly and is a bright trace.

Now turn R192 clockwise until PUDEL becomes faint again and falls just beyond the charge collection times of FD as illustrated in Fig. 5.2c (delay properly adjusted). If PUDEL is adjusted for too short a delay, one will notice rejection of an excessive number of valid pulse at low and moderate count-rates. Readjustment of PUDEL may be necessary.

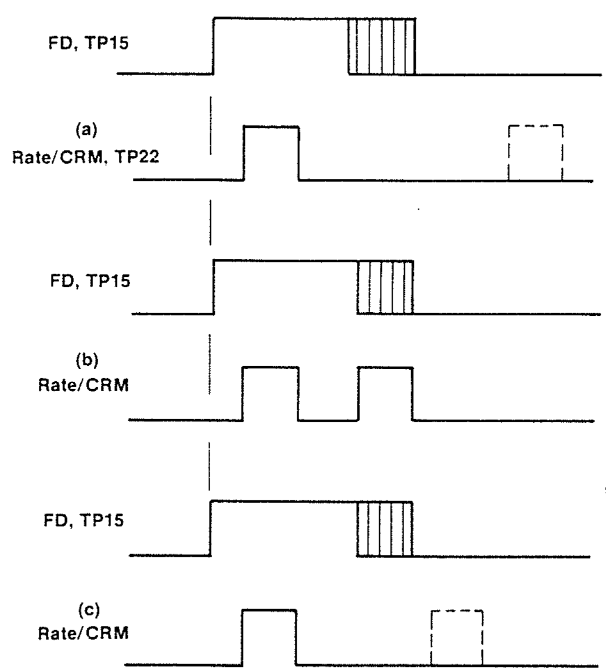


Fig. 5.2. PUDEL Delay Time Optimization. (a) Delay too long, (b) Delay too short, and (c) Delay properly adjusted.

5.16. PILE-UP INSPECTOR

The Pile-up Inspector circuit provides a PUR signal to prevent processing and analyzing of distorted pulses caused by pulse pile-up. Pulse pile-up is caused by two or more closely spaced (overlapping) pulses that sum together to produce a higher amplitude (distorted) pulse. The Pile-up Inspector monitors the output of the Fast Discriminator. Each time the Fast Amplifier pulse exceeds the noise threshold set by the Auto Noise Level Sensor output, the Fast Discriminator produces a logic pulse. The first pulse detected by the Pile-up Inspector sets an inspect interval; if a second pulse occurs within the inspect interval, the inspect interval is retriggered, and a PUR is generated.

Figure 5.3 illustrates the relative timing of the signals in the Model 973. The solid-line waveforms show a normal response to a single linear input signal from the preamplifier without any pulse pile-up condition. The broken-line waveforms show the modifications that occur when there is a pile-up condition.

The PUR signal is sent to the PUR (Pile-Up Rejector) input of the MCA such as an ORTEC ADCAM® with 8K ADC. The 8K ADC uses the PUR signal to inhibit analog-to-digital conversion of the distorted pulse and to turn off the livetime clock. If the PUR occurs before peak detect occurs in the ADC, both the original pulse and pulse causing the pile-up are rejected. If the PUR occurs after peak detect, the first pulse amplitude was not distorted and only the second pulse is rejected. Not all pile-up pulses are rejected. Some of the pile-ups that occur within the duration of the Fast Amplifier pulse cannot be resolved and will be processed even though they are distorted pulses. Each time an inspect interval is generated, a Busy signal is generated that can be connected to the ADC Busy In connector to generate a livetime correction signal for the ADC.

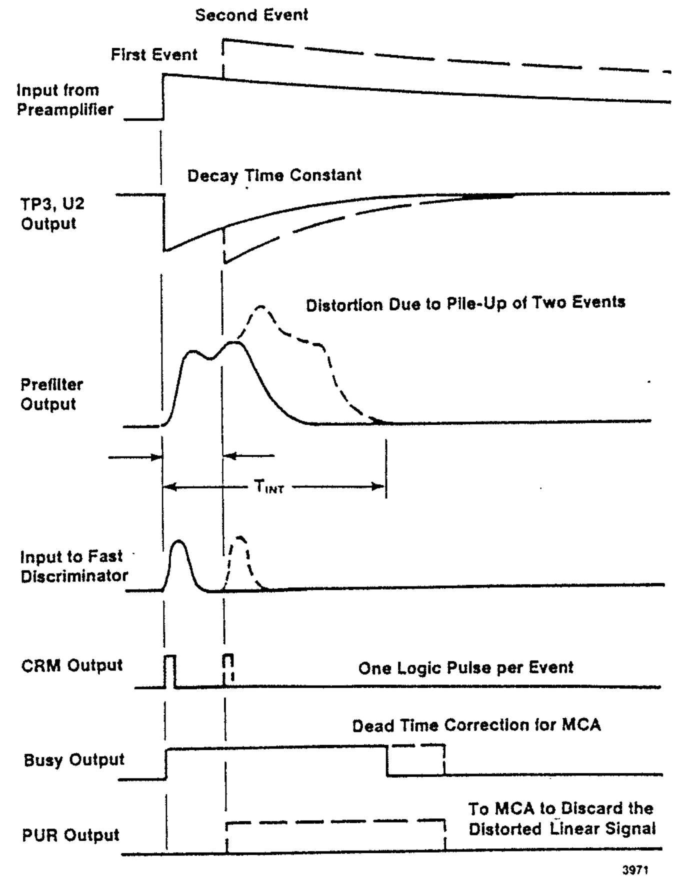


Fig. 5.3. Pile-up Inspector Timing Relationships in the Amplifier.

5.17. GATED INTEGRATOR OUTPUT AMPLIFIER

The Prefilter signal through the Delay Amplifier provides a negative input signal for the Gated Integrator. The amount of current fed to the integrator is selected by switch S3 and relay RLY6B. The selected resistor is chosen to provide 10-V signal from the integrator for a 10-V Prefilter signal at the selected time constant. The DMOS FETs U9A and U9B are the switches for the Gated Integrator. Since U9B is normally off, no current is fed into the integrator. The FET U9A is normally on resetting the integrator capacitor C84 (and hence the output of the feedback integrator amplifier U16/A3) to zero.

The gate signal for the FETs is initiated by the inverted fast discriminator signal FD. This sets the integrate flip-flop U21A, if the amplifier is not busy. The end of the integrate pulse INT is determined by one-shots U22A, U22B, and U23A for the selected integration time. The INT gate is the input for complementary drive amplifiers U13 and U14, which are used to switch FETs U9A and U9B, respectively. Variable resistor R261 is used to minimize the gating pedestal. The integrate time is logically OR-ed into the amplifier BUSY output signal.

6. MAINTENANCE

6.1. TEST EQUIPMENT REQUIRED

The following test equipment should be utilized to adequately test the specifications of the Model 973 High-Rate Amplifier.

1. EG&G ORTEC 419 Precision Pulse Generator or 448 Research Pulser.

2. Tektronix 465, 475, or 485 Series Oscilloscope, or equivalent with bandwidth greater than 100 MHz.

3. Hewlett-Packard 3400A RMS Voltmeter or equivalent.

6.2. PULSER TEST (See IEEE Standard 301-1976)

Coarse Gain	250
Fine Gain	1.5
Input Polarity	Positive
Integrate Time	5 μs

a. Connect a positive pulse generator output to the Model 973 input and adjust the pulse generator to obtain +10 V at the Model 973 GI output. Switch output to PZ ADJ and adjust the PZ control for best return to baseline. Switch back to GI and adjust pulse generator amplitude if needed. This should require an input pulse of 26 mV, using a 100-Ω terminator at the input.

b. Change the input polarity switch to NEG and then back to POS while monitoring the PZ ADJ output for a polarity inversion. The positive output should clamp at 0.6–0.8 V and the negative should clamp at –0.4 V.

c. Decrease the Coarse Gain switch stepwise from 250 to 5 and ensure that the output amplitude changes by the appropriate amount for each step. Return the Coarse Gain switch to 250.

d. Decrease the Fine Gain control from 1.5 to 0.5 and check to see that the GI amplitude decreases by a factor of 3. Return the Fine gain control to maximum at 1.5.

e. With the Integrate Time switch set for 5 μs, measure the width of the GI output pulse at the 0.2 V amplitude level; the width should be about 5 μs.

f. Change the Integrate Time switch to 2.5 μs; the width should be near 2.5 μs. Return the switch to 5 μs.

LINEARITY The integral nonlinearity of the Model 973 can be measured by the technique shown in Fig. 6.1. In effect, the negative pulse generator output is subtracted from the positive amplifier output to cause a null point that can be measured with excellent sensitivity. The pulse generator output must be varied between 0 and 10 V, which usually requires an external control source for the pulse generator (EG&G ORTEC Model 419). The amplifier gain and pulse generator attenuator must be adjusted to measure 0 V at the null point when the pulse generator output is 10 V. The variation in the null point as the pulse generator is reduced gradually from 10 V to 0 V as a measure of the nonlinearity. Since the subtraction network also acts as a voltage divider, this variation must be less than (10 V full scale) × (±0.05% maximum nonlinearity) × (1/2 for divider network) = ±2.5 mV for the maximum null-point variation.

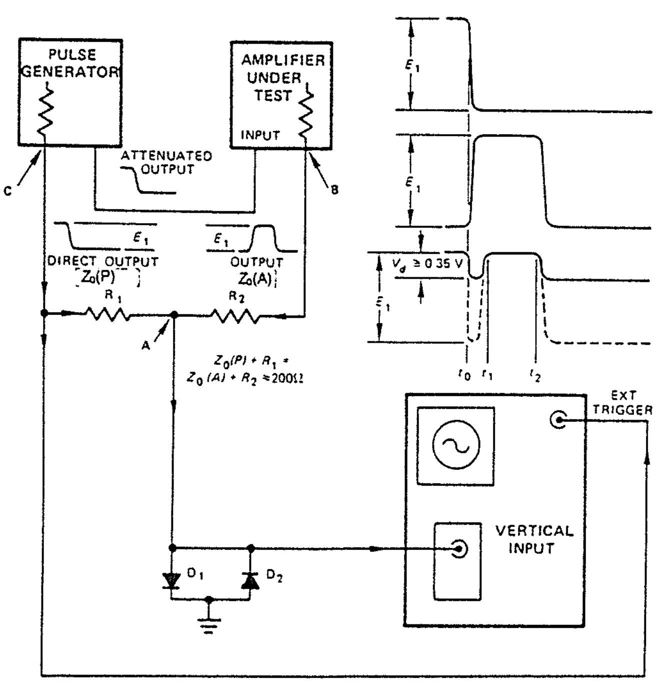


Fig. 6.1. Circuit Used to Measure Nonlinearity.

OUTPUT LOADING Use the test setup of Fig. 6.1. Adjust the amplifier output to 10 V and observe the null point when the front-panel output is terminated in 100 Ω. The change should be <5 mV.

NOISE Measure the noise at the amplifier PZ ADJ output with maximum amplifier gain and 5-μs Integrate time. Using a true rms voltmeter, the noise should be less than 9 μV × 375 (gain), or 3.37 mV. Do not terminate output with 100 Ω.

For an average responding voltmeter, the noise reading would have to be multiplied by 1.13 to calculate the rms noise.

6.3. SUGGESTIONS FOR TROUBLESHOOTING

In situations where the Model 973 is suspected of a malfunction, it is essential to verify such malfunction in terms of simple pulse generator impulses at the input. The Model 973 must be disconnected from its position in any system and routine diagnostic analysis performed with a test pulse generator and an oscilloscope. It is imperative that testing not be performed with a source and detector until the amplifier performs satisfactorily with the test pulse generator.

The testing instructions in Section 6.2 and the circuit descriptions in Section 5 provide assistance in locating the region of trouble and repairing the malfunction. The two side plates can be completely removed from the module to enable oscilloscope and voltmeter observations.

6.4. FACTORY REPAIR

This instrument can be returned to the EG&G ORTEC factory for service and repair at a nominal cost. Our standard procedure for repair ensures the same quality control and checkout that are used for a new instrument. Always call Customer Services at EG&G ORTEC, (615) 482-4411, before sending in an instrument for repair to obtain shipping instructions and so that the required Return Authorization Number can be assigned to the unit. This number should be marked on the address label and on the package to ensure prompt attention when the unit reaches the factory.

6.5. TABULATED TEST POINT VOLTAGES

The voltages given in Table 6.1 are intended to indicate typical dc levels that can be measured on the PWB. In some cases the circuit will perform satisfactorily even though, due to component tolerances, there may be some voltage measurements that differ slightly from the listed values. Therefore, the tabulated values should not be interpreted as absolute voltages, but are intended to serve as an aid in troubleshooting.

Table 6.1. Typical dc Voltages.

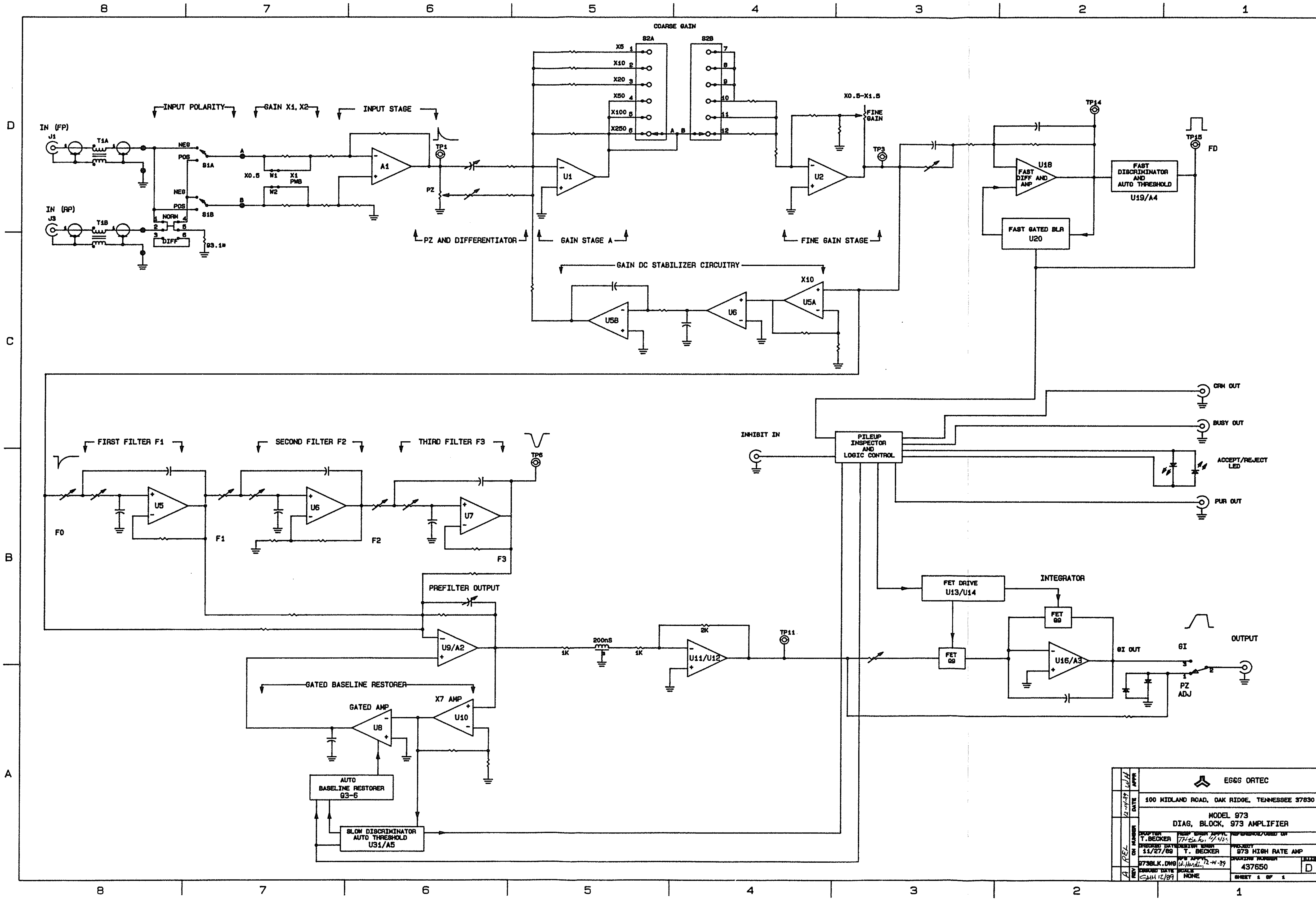
Location	Voltages*
TP1	±25 mV
TP2	±25 mV
TP3	±25 mV
TP4	±30 mV
TP5	±40 mV
TP6	±60 mV
TP7	±40 mV
TP8	±50 mV
TP9	−12.5 V
TP10	−11.4 V
TP11	± 2 mV
TP13	+ 5 V
TP15	0 to +0.4 V
TP25	+0.05 to +0.3 V
TP26	−0.4 V
TP28	HC Logic 1
PZ ADJ OUT	± 2 mV
GI OUT	± 2 mV

* All voltages measured with no input signal, with the input terminated in 100 Ω, and with all controls set fully clockwise at maximum.

BIN/MODULE CONNECTOR PIN ASSIGNMENTS FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES PER TID-20893 (Rev) (adopted by DOE)

Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	−3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	−24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Spare
*10	+6 volts	32	Spare
*11	−6 volts	*33	117 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Spare	35	Reset (Scaler)
14	Spare	36	Gate
15	Reserved	37	Reset (Auxiliary)
*16	+12 volts	38	Coaxial
*17	−12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	117 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

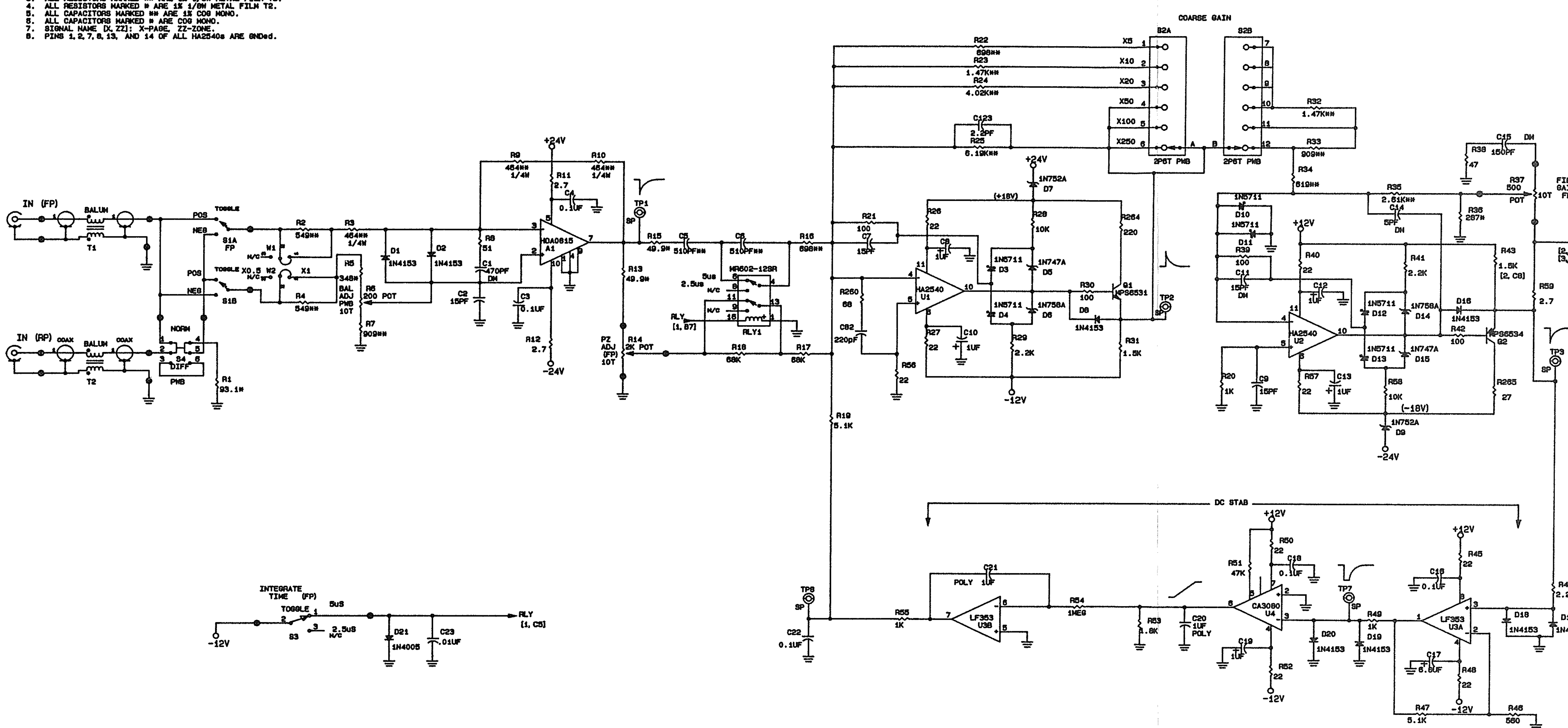
Pins marked (*) are installed and wired in EG&G ORTEC's 4001A and 4001C Modular System Bins.



COARSE GAIN
S2A
S2B
X5
X10
X20
X50
X100
X250
INPUT POLARITY
GAIN X1, X2
INPUT STAGE
IN (FP)
J1
T1A
IN (RP)
J3
T1B
NEG
POS
S1A
S1B
NORM
DIFF
X0.5
W1
X1
PMB
W2
A1
TP1
PZ
U1
U2
X0.5-X1.5
FINE GAIN
TP3
TP14
TP15
FD
U18
FAST DIFF AND AMP
FAST DISCRIMINATOR AND AUTO THRESHOLD
U19/A4
FAST GATED BLR
U20
PZ AND DIFFERENTIATOR
GAIN STAGE A
FINE GAIN STAGE
GAIN DC STABILIZER CIRCUITRY
X10
U5A
U6
U5B
CRM OUT
BUSY OUT
INHIBIT IN
PILEUP INSPECTOR AND LOGIC CONTROL
ACCEPT/REJECT LED
PUR OUT
FIRST FILTER F1
SECOND FILTER F2
THIRD FILTER F3
TP6
U5
U6
U7
F0
F1
F2
F3
PREFILTER OUTPUT
U9/A2
1K
200nS
1K
2K
U11/U12
TP11
FET DRIVE
U13/U14
INTEGRATOR
FET Q9
FET Q9
U16/A3
GI OUT
GI
OUTPUT
PZ ADJ
GATED BASELINE RESTORER
GATED AMP
X7 AMP
U8
U10
AUTO BASELINE RESTORER
Q3-6
SLOW DISCRIMINATOR AUTO THRESHOLD
U31/A5
EG&G ORTEC
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
MODEL 973
DIAG, BLOCK, 973 AMPLIFIER
T.BECKER
11/27/89
T. BECKER
973 HIGH RATE AMP
973BLK.DWG
437650
NONE
D
SHEET 1 OF 1
REL

NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS.
2. ALL RESISTORS ARE 5% 1/8 WATT CARBON FILM.
3. ALL RESISTORS MARKED ## ARE 1% 1/8W METAL FILM T9.
4. ALL RESISTORS MARKED # ARE 1% 1/8W METAL FILM T2.
5. ALL CAPACITORS MARKED ## ARE 1% COG MONO.
6. ALL CAPACITORS MARKED # ARE COG MONO.
7. SIGNAL NAME [X, ZZ]: X-PAGE, ZZ-ZONE.
8. PINS 1, 2, 7, 8, 13, AND 14 OF ALL HA2540s ARE GNDed.



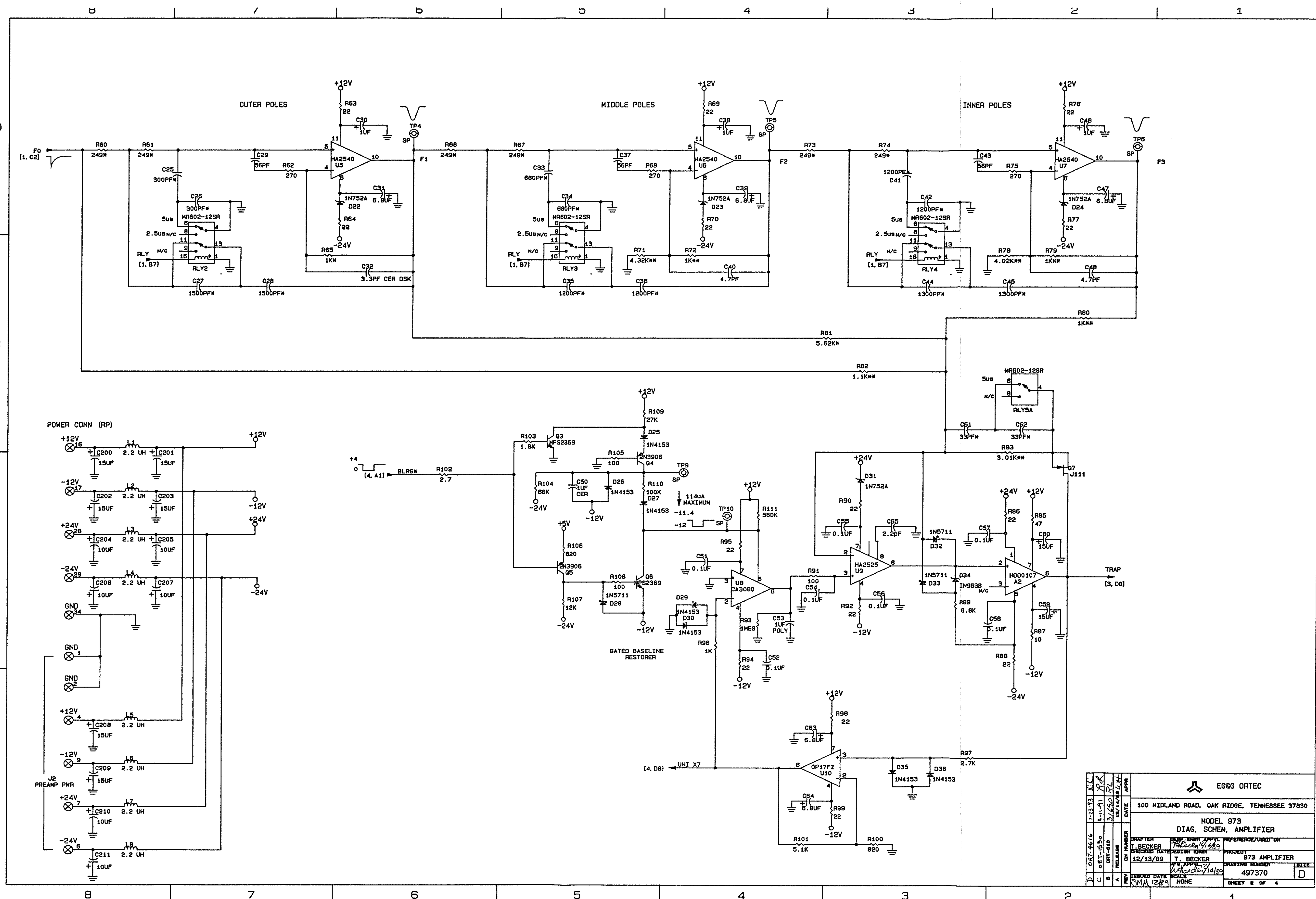
EG&G ORTEC

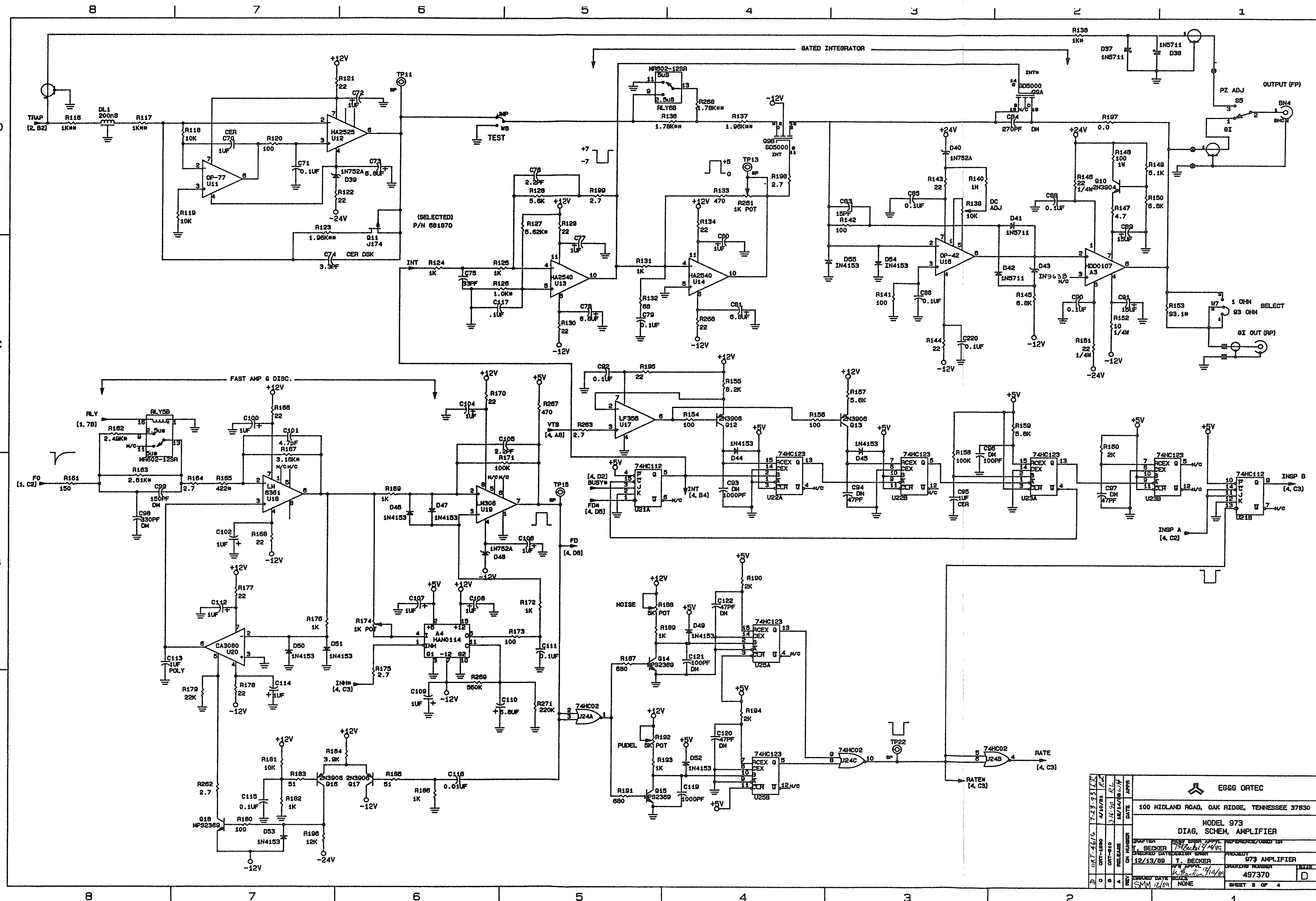
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

MODEL 973
DIAG, SCHEM, AMPLIFIER

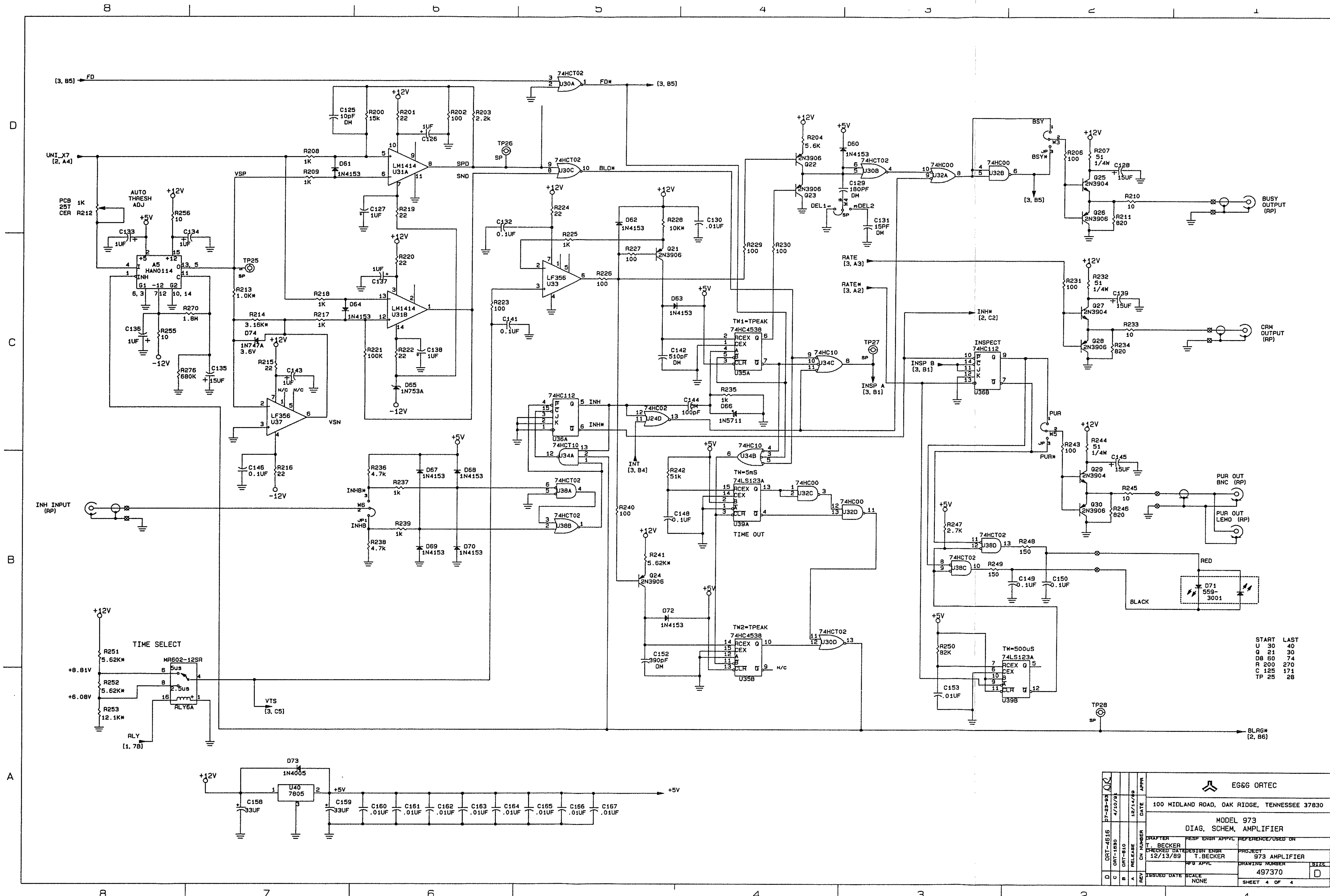
REV	ECN NUMBER	DATE	APPR
D	ORT-4616	7-23-93	KK
C	ORT-1530	4/10/91	RL
B	ORT-810	3-16-90	RL
A	RELEASED	12-14-89	GH

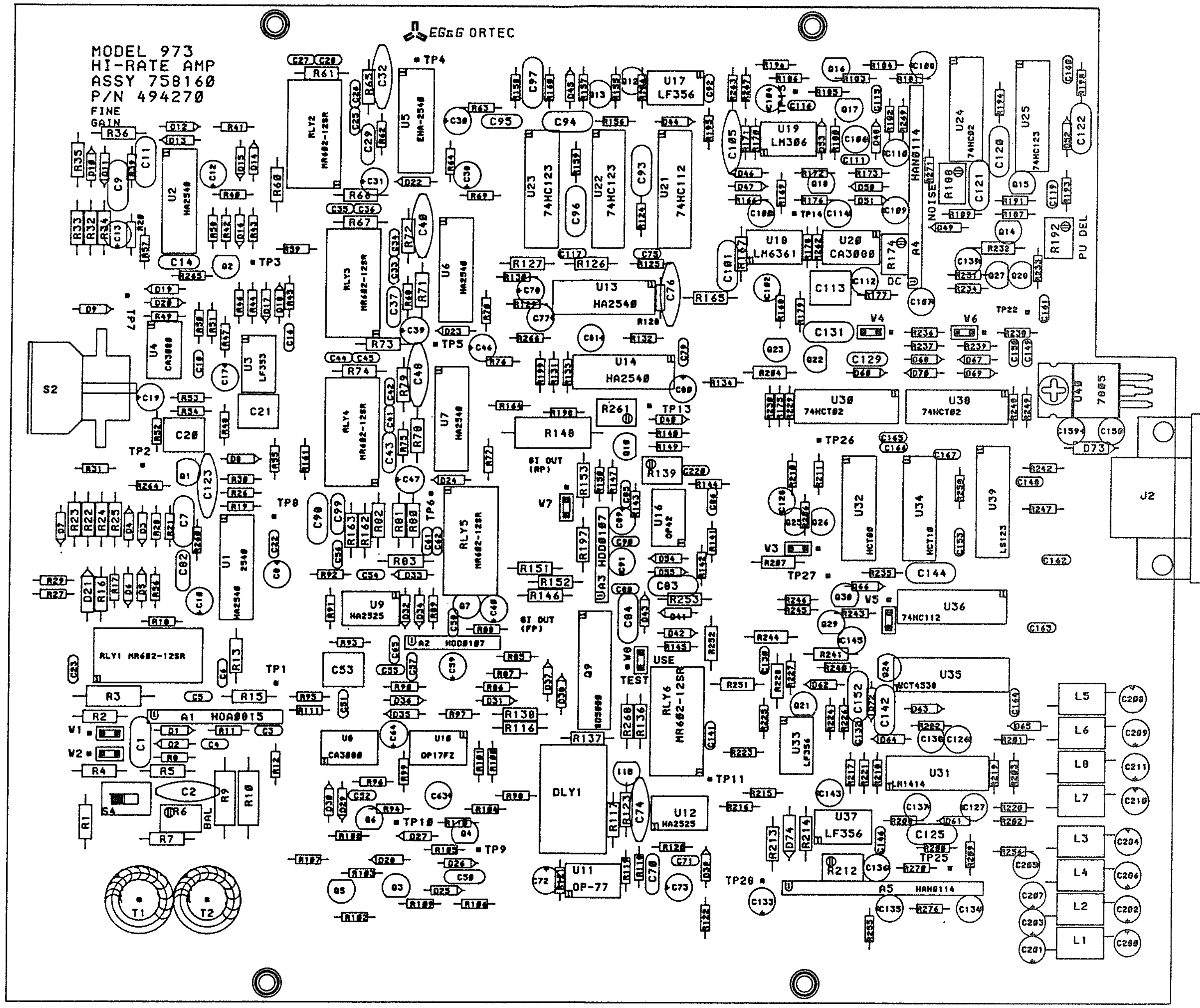
DRAFTER: T. BECKER
CHECKED DATE: 10/17/89
DESIGN ENGR: T. BECKER
ISSUED DATE: SMM 12/89
SCALE: NONE
PROJECT: 973 AMPLIFIER
DRAWING NUMBER: 497370
SIZE: D
SHEET 1 OF 4


OUTER POLES
MIDDLE POLES
INNER POLES
HA2540 U5
HA2540 U6
HA2540 U7
MR602-12SR
RLY2
RLY3
RLY4
RLY5A
5us
2.5us
RLY [1, B7]
F0 [1, C2]
F1
F2
F3
TP4
TP5
TP6
TP9
TP10
R81 5.62K**
R82 1.1K**
R83 3.01K**
R80 1K**
POWER CONN (RP)
J2 PREAMP PWR
GND
BLRG*
[4, A1]
GATED BASELINE RESTORER
114uA MAXIMUM
CA3080 U8
HA2525 U9
HOD0107 A2
OP17FZ U10
J111 Q7
TRAP [3, D8]
UNI X7
[4, D8]
EG&G ORTEC
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
MODEL 973
DIAG. SCHEM. AMPLIFIER
DRAFTER T.BECKER
CHECKED DATE 12/13/89
DESIGN ENGR T. BECKER
PROJECT 973 AMPLIFIER
DRAWING NUMBER 497370
SIZE D
SCALE NONE
SHEET 2 OF 4



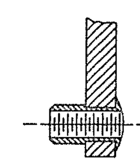
GATED INTEGRATOR
FAST AMP & DISC.
TRAP [2, B2]
TEST
(SELECTED) P/N 681670
INT
PZ ADJ
OUTPUT (FP)
DC ADJ
1 OHM
93 OHM
SELECT
SI OUT (RP)
RLY [1, 7B]
F0 [1, C2]
VTS [4, A8]
BUSY* [4, D2]
FD* [4, D8]
INT [4, B4]
FD [4, D8]
INH* [4, C3]
INSP B [4, C3]
INSP A [4, C2]
NOISE
PUDEL
RATE [4, C3]
RATE* [4, C3]
EG&G ORTEC
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
MODEL 973
DIAG, SCHEM, AMPLIFIER
DRAFTER T. BECKER
CHECKED DATE 12/13/89
DESIGN ENGR T. BECKER
PROJECT 973 AMPLIFIER
DRAWING NUMBER 497370
SIZE D
SCALE NONE
SHEET 3 OF 4


EG&G ORTEC
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
MODEL 973
DIAG. SCHEM. AMPLIFIER
DRAFTER T. BECKER
CHECKED DATE 12/13/89
DESIGN ENGR T. BECKER
PROJECT 973 AMPLIFIER
DRAWING NUMBER 497370
SIZE D
SCALE NONE
SHEET 4 OF 4
START LAST
U 30 40
Q 21 30
D8 60 74
R 200 270
C 125 171
TP 25 28
TIME SELECT
AUTO THRESH ADJ
INH INPUT (RP)
BUSY OUTPUT (RP)
CRM OUTPUT (RP)
PUR OUT BNC (RP)
PUR OUT LEMO (RP)
TIME OUT
RED
BLACK
BLRG* (2, B6)
UNI_X7 (2, A4)
VTS (3, C5)
RLY (1, 7B)



NOTES UNLESS OTHERWISE SPECIFIED:

1. ASSEMBLE COMPONENTS IN ACCORDANCE WITH ORTEC WORKMANSHIP STANDARD SECTION 4, PC ASSEMBLY.
2. SOLDER PER ORTEC WORKMANSHIP STANDARD SECTION 5.



SECTION A-A

QTY REQD	FIND NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REMARKS
-001			PARTS LIST	

REV	ECN NUMBER	DATE	APPR
C	ORT-1530	4-11-91	[illegible]
B	ORT-610	3-16-90	RL
A	RELEASE	12-14-89	WH

REVISIONS

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES
DO NOT SCALE THIS DRAWING
TOLERANCES ARE

FRACTIONS	DECIMALS	ANGLES	FINISH
± 1/64	.X ± .09 .XX ± .01 .XXX ± .005	± 0°30'	√

MATERIAL

FINISH

APPLIED PRACTICES

EG&G ORTEC
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

MODEL 973
PWB ASSY, AMPLIFIER

DRAFTER: CS	DATE: 12-89	ENG APPROVAL: T.W. Becker	DATE: 12/14/89
CHECKED	DATE	DESIGN ENGR: T. BECKER	
		MFG APPROVAL: W. Hardin	DATE: 12-14-89
DWG ISSUE: EMM	DATE: 12/89	SCALE	

REFERENCE/USED ON

PROJECT

DRAWING NO 758160

SHEET OF