ENERPRO
5780 Thornwood Drive
Goleta, California 93117

Report No. R153
December 2, 1994

OPERATING MANUAL FOR A 12-SCR GENERAL PURPOSE GATE FIRING BOARD, PART NO. FCOG1200 REV. C

INTRODUCTION

This manual is intended to familiarize the user with the salient features and specifications of the firing board. A simple checkout procedure is included together with typical firing circuit signal waveforms.

PRODUCT DESCRIPTION

APPLICATION

The general purpose firing board responds to a voltage or milliamp current signal to produce a delayed hard firing "picket fence" gate pulses for firing parallel or series connected 12-pulse converters or ac controllers. The twelve gate pulses are precisely spaced at 30° as required to eliminate the 5th and 7th harmonic of the mains current.

Advantages of twelve pulse rectification:

When used as a converter, the FCOG1200 automatically adapts to the sequence of the ac mains voltage (whether a-b-c or a-c-b) and to the 30° phase shift (whether +30° or -30°) between the two groups of three phase voltages applied to the converter input.

Twelve pulse rectification provides the benefits of reduced harmonic current into the input transformer and reduced ripple current in the dc output (ripple frequency is doubled to 720Hz and ripple driving voltage is halved). The result is improved power quality of the ac mains current and reduced size of the dc filter choke.

LSI LOGIC DEVICE

All of the firing circuit logic is contained in two custom CMOS LSI gate array's (labeled U3 and U4). Additional detail on the firing circuit theory may be found in the theory section (pages 4-6).[1]

BOARD MOUNTED CONNECTORS

The firing board is completely connectorized to simplify maintenance and trouble shooting.

[1] Also see: Bourbeau, F. J., "Phase Control Thyristor Firing Circuit: Theory and Applications", Power Quality '89, Long Beach, California.

Gate/Cathode Connectors

The SCR gate/cathode interface is provided by 8-position Mate-N-Lok™ vertical headers, J1 through J4, and mating plugs, P1 through P4. The jacks are keyed to prevent incorrect installation of the mating plugs. Plug's P1 and P3 accesses the gates and cathodes of the six SCRs having load connected cathodes when the SCRs are arranged in the in-line ac controller or bridge converter configurations. Similarly, plug's P2 and P4 accesses the gates and cathodes of the six SCRs having line connected cathodes.

Control Signal Connector

The firing board is connected to the gate delay command and inhibit controls through a 12-position Mate-N-Lok™ connector designated as J6. This connector also accesses the 24Vac board power, the 30Vdc rectifier, the regulated +12Vdc and the regulated +5Vdc output's. The 24Vac and 30Vdc connections permit the board to be powered from an external source. With 24VA 24Vac applied, approximately 10 watts of dc power is available from J6 to power lamps or a control relay.

Test Signal Input Connector

A 8-position cable header, J7, is used to inject low level 6-phase test reference signals from a firing board test fixture into the delay generator circuit. This allows the board checkout to proceed without connection to high voltage power. This connection also allows for connection to circuit common and an unregulated 15Vdc supply.

Frequency Selection Connector

A 3-position header, J5, is used in conjunction with RN4[2] to select between 50Hz and 60Hz operation. In 60Hz operation RN4 is 120kΩ and R36 is connected in parallel with R35. In 50Hz operation RN4 is 150kΩ and J5 removes R36 from the circuit in order to maintain TP2 at 5.0Vdc.

PHASE-LOSS INHIBIT

A phase loss circuit operates to instantly inhibit SCR gating if the mains phase balance is abnormal or, in the extreme case, if one phase voltage is missing. Gating is enabled when the proper phase balance is restored: gating initiates at the maximum delay angle, and ramps down to the commanded angle at a rate determined by the Soft-Start RC time constant.
The phase-loss inhibit circuit is also activated when six phase power is initially applied to the SCRs. Gating is inhibited until the power supply voltage has stabilized. Gating then commences at the delay angle limit and ramps down to the commanded angle at a rate determined by the Soft-Start RC time constant.

[2] RN4 may be placed in a socket for ease of installation.

BOARD MOUNTED POWER SUPPLY

The power supply on the FCOG1200 board operates from an external 24Vac, 24VA, single phase power source. The power supply produces unregulated 30Vdc, and regulated 12Vdc and 5Vdc.

GATE DELAY COMMAND

The gate delay command signal, SIG HI, may be a 0.9Vdc to 5.9Vdc voltage signal or a current signal with an upper limit of 50mA. The input resistance presented to the delay command signal is determined by resistor R40, connected in shunt with the control signal input. The value of R40 is selected at 10 kΩ when the control signal is a voltage source. As an option, a zero to 5.0Vdc input signal may be used by changing R25 to 150kΩ.

When the gate delay command is a current signal, R40 is selected to give a 5.0Vdc level at the maximum delay command signal current.

GATE INHIBITS

SCR gating is inhibited by making either or both of the inhibit signal points, designated as I1 and I2 and appearing at pins 4 and 12 of J6, a logic zero.

In the case of the instantaneous inhibit, I1, resistor R41 on the firing board is provided to pull the I1 signal point low if the connection between I1 and +12Vdc is opened. This ensures that SCR gating is inhibited if plug P6 is inadvertently disconnected. In applications where the instantaneous gate inhibit function is not utilized, a jumper wire is installed between pins 4 and 6 of P6 to hold I1 at +12Vdc when P6 is installed in J6.

The inhibit signal I2 is connected to +12Vdc through pull-up resistor R42 on the firing board. When I2 is grounded, the gate delay angle is ramped to the maximum delay angle before gating is inhibited. This is termed the "Soft-Stop" shutdown mode. Removing the ground on I2 causes gating to be enabled with the delay angle set to the maximum limit. The delay angle then ramps down to the commanded angle. This is termed the "Soft-Start" turn-on mode. The Soft-Stop and Soft-Start periods are determined by timing resistors R39 and R22, and capacitor C4.[3]

As an option the I2 signal may be tied to common through R41. In this case R42 would be omitted and the I2 signal would be toggled as for I1.

[3] See specification table for formulas.

THEORY OF OPERATION

PHASE REFERENCES

The phase references for the phase locked loop (PLL) delay angle generator are derived from the two sets of 30° phase shifted three phase ac supply voltages that power the two SCR circuits. These voltages are sensed at the gate trigger transformers[4] on the firing board. The supply voltages are processed by resistive attenuators, low pass filters, phasor addition circuitry, and differential comparators.

The time constant of the low pass filter is selected to give a lagging phase shift of q = 60° at the 60 Hz operating frequency. A phasor addition technique adds a 60° phase lead, giving an adjusted reference delay phase shift at 60 Hz of 60° - 60° = 0°.

The six attenuated and filtered reference signals are applied to six voltage comparators. These comparators are contained on LSI device U5. Additional circuitry is contained in U5 to modify the comparator input signals to give correct reference phasing when the sequence of the ac power is reversed.

SIX PHASE; PHASE LOCKED LOOP (PLL)

Three of the reference comparator outputs, designated as A_X, B_X, and C_X in Figure 1, are applied to three EX-OR phase detectors in LSI device U3. The other three reference comparator outputs, designated as A_Y, B_Y, and C_Y, are applied to the three EX-OR phase detectors in LSI device U4. The other six inputs to the phase detectors are produced by ring counters in LSI devices U3 and U4, as described below.

The outputs of the six phase detectors in U3 and U4 are summed with six 100kΩ resistors and applied to the inverting input of the summing amplifier. The output of the summing amplifier sets the frequency of the voltage controlled oscillator (VCO). This clock signal is designated as CK1 in Figure 1. The clock frequency is 384 (6 x 64) times the mains frequency when the PLL is in lock. A ÷64 binary counter (BC) operates on CK1 to produce a second clock signal CK2 which is six times the mains frequency. A ÷6 ring counter (RC1) outputs the three delayed phase references for the EX-OR phase detector in U3.

An Inverter in LSI U4 produces the inverted clock signal NOT(CK2). This clock toggles a second ring counter RC2 to produce the three delayed reference outputs A_{dy}, B_{dy}, and C_{dy}. Because of the clock signal inversion, these references are shifted in phase by 30° from the corresponding delayed reference signals A_{dx}, B_{dx}, and C_{dx} in LSI device U3.

The mains voltage references, Ax through Cy, are input into EX-NOR gates to produce the phase detector outputs, Dax through Dcy.

---

[4] The value of this internal resistor (R) can be determined by the pulse module part number: All pulse modules used are EP1024-x, where x = 0 (R = OMIT), x = 1 (R = 2.0MΩ, used at E≥ 240Vac), x = 2 (R = 511kΩ, used at 120Vac ≤ E ≤ 240Vac), and x = 3 (R = 200kΩ, used at E ≤ 120Vac) .

The six phase detector outputs and the buffered delay command input must sum to a constant value if the VCO frequency is to remain a fixed multiple of the mains frequency. Therefore, an increase in the buffered delay command input must be accompanied by a corresponding decrease in the average value of the summed phase detector outputs. Thus the dc level change is produced by a proportional change in the delay angle between the mains frequency and the delayed reference. A proportional relationship is enforced between the mains voltage phase reference and the delayed phase references.

STEADY-STATE TRANSFER FUNCTION

The 0.9Vdc/5.9Vdc gate delay command signal is amplified by a factor of -100/47.5 = 2.11 in the buffer amplifier and applied through a pair of 8.87kΩ resistors to the inverting input of the summing amplifier. The output voltage of the summing amplifier is at a constant average level (in the range of 4.5Vdc to 5.5Vdc) when the PLL is in lock. This enforces the requirement that a change in the output of the buffer amplifier be matched by a proportional and opposite change in the average voltage at the outputs of the six EX-OR phase detectors. The factor of proportionality is the ratio of the control signal input resistance (= 2 x 8.87kΩ = 17.74kΩ) to the effective value of the resistance's that sum the phase detector outputs (= 100kΩ/6 = 16.67kΩ). Since a 180° change in the phase angle between the mains voltage phase references A_X through C_Y and the delayed phase references A_{dX} through C_{Yd} corresponds to a 12Vdc change in each EX-OR output, a change in the delay angle command, ΔSIG HI, results in a gate delay angle change of Δα, of

$$\Delta\alpha/\Delta\text{SIG HI} = (100/47.5) \times (16.7/17.74) \times (180/12) = 29.67\ °/V$$

FIRING BOARD FREQUENCY RESPONSE

Figure 2 shows the simplified block diagram of the PLL gate delay determinator.

$$\frac{\alpha}{\text{SIG HI}} = \frac{a(jwT + 1)}{(j\omega/bc + 1)(j\omega T/2 + 1)}$$

where T is the lead-lag time constant, a is scale factor relating gate delay angle to delay command voltage, c is the summing amplifier gain, and d is the VCO integration constant. Choosing T = 1/bc for pole-zero cancellation results in a simple lag transfer of

$$\frac{\alpha}{\text{SIG HI}} = \frac{a}{j\omega/2bc + 1}$$

For b = 1.5V/V and c = 300/sec.

$$\frac{\alpha}{\text{SIG HI}} = \frac{29.67}{j\omega/939 + 1} \left(\frac{\text{deg}}{\text{Volt}}\right)$$

This transfer function has 45° phase shift and -3db attenuation at w = 939

rad/sec (150Hz).

GATE COMMAND DECODING

The delayed reference signals A_{dx}, B_{dx}, C_{dx} and A_{dy}, B_{dy}, C_{dy} are applied to decoding circuits in LSI devices U3 and U4 to produce the required 12 gate pulse signals. These signals are precisely spaced by 30° and shifted in phase from the line-to-line voltage zero crossings by phase angle a. The gate pulse profile is a "picket fence" of 128 pulses having a 50% duty cycle and a pulse width of 26 ms[5] . This profile is produced by decoding circuitry which ANDs the 23,040 Hz clock CK1 with the 60Hz outputs of the ring counters in U3 and U4. Since the gate pulse carrier is phase-locked to the mains frequency, the first pulse in the gate pulse train always has a full 26 µs pulse width.

GATE PULSE AMPLIFIER

Circuitry shown in drawing E640 consisting of transistor arrays U10 and U11, resistors R1 through R8, capacitors C11 through C16, and gate pulse isolation modules PM1 through PM12 amplify and shape the thyristor gate current pulses. Each pulse module consists of a 2:1 ratio pulse transformer tested for 3500 Vrms isolation, two secondary diodes, noise suppression resistors across the primary and across the gate drive output, and a fuse in series with the output.

ELECTRICAL SPECIFICATIONS

The electrical specifications of the General Purpose Firing Board are summarized in the table below. Part numbers refer to drawing E640, Rev. C.

Characteristic	Performance Requirement.	Supporting. Information
1. Line voltage reference sensing	Resistive attenuators and 60° phase shift single pole filters.	Reference signals automatically interchanged for negative phase sequence.
2. PLL reference signal. phasing w.r.t. mains line-to-neutral voltage: a. ref. signals in phase with mains voltage. b. ref. signals lagging mains voltage by 30°.	Application: a. AC controllers with high power factor loads. b. Converters of AC controllers with low power factor loads.	
3. SCR gate waveform. a. Mode 1 b. Mode 2	Pulse Profile: 120° burst of 128 pulses(23,040 Hz carrier) two 30° bursts of 32 pulses(23,040 Hz carrier)	

[5] An optional pulse pattern is available consisting of: two 32 pulse, 6.5 ms wide, 6.5 ms spaced gate pulse trains.

4. Input control signal.	0.9Vdc to 5.9Vdc control signal. Load resistance is 8.33 KΩ.	Option 1: 0.0 Vdc to 5.0Vdc control signal. Option 2: a Shunt resistance (R41) across signal input can be selected for milliamp control signal.
5. Control signal isolation from ground.	653 KΩ	Produced by the six 2.00 MΩ mains voltage sense resistors, internal to PM4-6 and PM9-12.
6. Gate delay steady-state transfer function.	Increase in command voltage produces a proportional decrease in gate delay angle, α.	α_{max} and α_{min} change equally with change in R_{bias}(R32). (α_{max}-α_{min}) changes with R_{span}(R31).
7. Gate delay dynamic transfer function bandwidth.	Attenuation = -3dB at 119Hz. Phase shift = -45° @ 68Hz.	Frequency response can be modified by changing summing amplifier parameters.
8. Gate delay angle balance.	Gate pulses for same polarity SCRs are displaced by 120° ± 1.0°. Gate pulses for opposite polarity SCRs are displaced by 180° ± 1.0°.	Assumes balanced line-to-line mains voltage. Balance determined by reference comparator offset and attenuator/filter component tolerances.
9. Effect of frequency.	Da/Df = 1.5°/Hz. For 50 Hz operation, compensate by removing R36 and changing RN4 to 150KΩ.	Due to Type I PLL and 60° phase shift low pass reference filters. Optional MFCVIA-1 J6 plug in board available to make insensitive to frequency.
10. Effect of phase rotation.	none	SCR gating sequence matches mains voltage sequence.
11. Effect of mains voltage distortion.	1) unaffected by false reference voltage zero crossing. 2) 60° filter attenuates 5th harmonic by 12.8dB relative to fundamental.	1) No PLL response to short-time false reference logic states. 2) Reference filter attenuates 5th, 7th, 11th, etc. harmonics from 6-pulse SCR switching.
12. Lock acquisition time.	Approximately 29ms.	Gating is inhibited for 20ms or longer at power-on. Inhibit period depends on Soft-Start time constant.
13. Soft-Start	Gating commences at α_{max} and exponentially decays to the commanded delay when <I2> is ungrounded (J6-12).	Soft-Start time constant is set by C4 and R22. T = (1.5k + R22)(C4)(0.579) T = mSec, R = kΩ, C = µF R22 ≥ 20.0kΩ
14. Soft-Stop	Gate-delay angle ramps to α_{max} before being inhibited when <I2> is grounded.	Soft-Stop time constant is set by C4 and R39. T = R39(C4)(1.84) T = mSec, R = kΩ, C = µF R39 ≥ 1.0kΩ
15. Phase loss inhibit.	Loss of a mains voltage or severe phase unbalance causes gate inhibit.	Gating resumes with $\alpha = \alpha_{max}$. a ramps to commanded delay angle as determined by Soft-Start time constant
16. Power-on inhibit.	Phase loss inhibit circuit is activated at power-on.	Same delay angle response as with phase loss inhibit.
17. Instantaneous inhibit.	Opening the connection of <I1>(P6-4) to +12V instantly inhibits SCR gating. Closing the connection of <I1> to +12V instantly enables SCR gating.	Gating is inhibited if P6 is removed.
18. SCR gate current individual pulse width.	T_{on} and T_{off} vary from 15µs to 28µs.	Gate current ON and OFF times vary with gate delay angle because of 360Hz FM in the VCO output.

19. Peak gate drive open circuit voltage	14V	With a 30Vdc supply voltage
20. Peak gate drive short circuit current.	1.8A	Measured with a 30Vdc supply voltage and a 1.0Ω load resistor
21. Gate drive current risetime(short circuit)	.5A in .5µs	Measured with a 30Vdc supply voltage and a 1.0Ω load resistor

INSTALLATION AND CHECKOUT

The following procedure should be followed to ensure proper operation prior to the application of mains power to the SCR unit.

1. **Ensure that the power is off!** Wire plug's P2 and P4, with mains voltage connected to sockets 2, 5, and 8. Insert plug's P2 and P4 into header's J2 and J4.

2. Connect the appropriate power to J6; J6-1 and J6-2 for 24Vac or J6-3 and J6-8 for +30Vdc.

3. Install plug P6 with the 0.9/5.9Vdc delay command signal, signal common, and inhibit contact closure leads wired to the plug.

4. Energize the board power to J6, this will energize the FCOG1200 board.

5. Verify the presence of regulated +12Vdc ± 5% at J6-6 and regulated +5Vdc ± 5% at J6-7.

6. Energize the mains voltage, this will remove the phase loss condition from the FCOG1200.

7. Verify that the DC level of the VCO control voltage at TP2 is approximately 5.0Vdc.

8. Determine the PLL gate delay angle from the pulse width of the A-phase detector output at TP7 and TP12: Calibrate the oscilloscope timebase at 20°/div. Read the gate delay angle directly from the TP7 and TP12 pulse off time.

9. Vary the delay command voltage from 0.9Vdc to 5.9Vdc. Observe that the gate delay angle at TP7 and TP12 has the desired minimum and maximum values.

10. To increase the minimum and maximum gate delay angles by an equal amount, increase the value of the delay bias resistor, R32. To increase the difference between the maximum and minimum delay angles, reduce the value of the delay span resistor, R31.

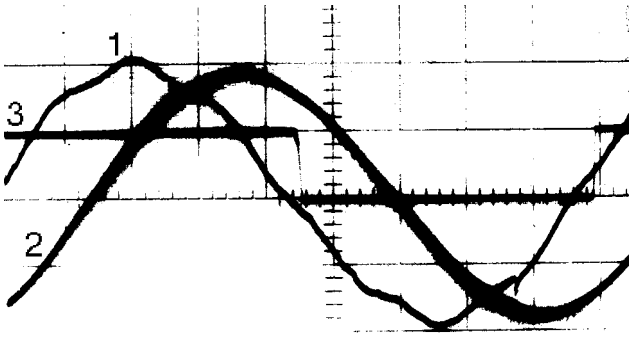
Firing Board Waveforms

The following waveforms were obtained with the firing board connected to 240 Vac 60 Hz balanced 6-phase power via sockets 2, 5, and 8 of plug's P2 and P4. All logic signals are shown with a scale factor of 10 V/div. The time (X) axis scale factor is 40°/div unless otherwise noted. Component designations U5 etc. refer to drawing number E640A, Rev. A. Component pins are designated U5-11, etc.

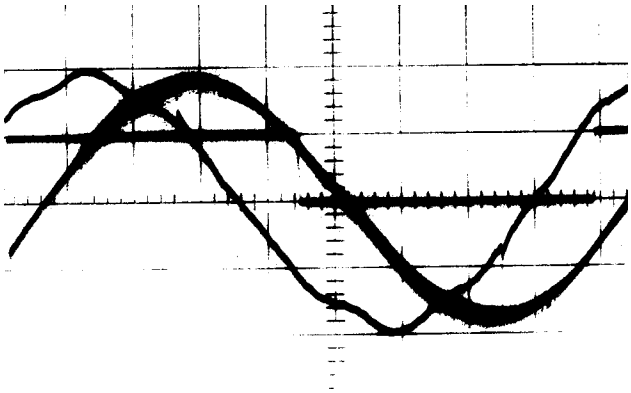
A. Mains Voltage Signals, A phase.

Trace: 1. line to neutral mains voltage, 150 V/div
2. attenuated and filtered mains voltage at RN4-11, .2 V/div
3. reference comparator output at TP10, U5-11

a. 0° references



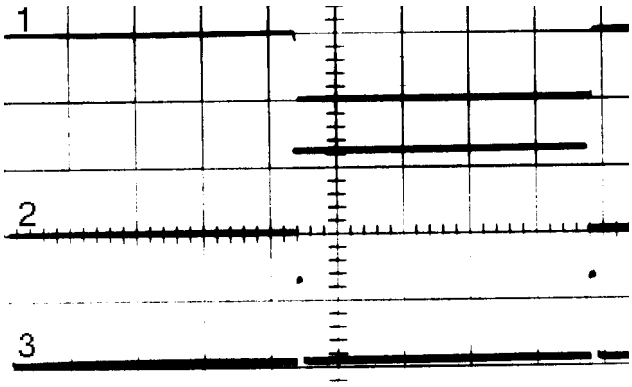
b. -30° references



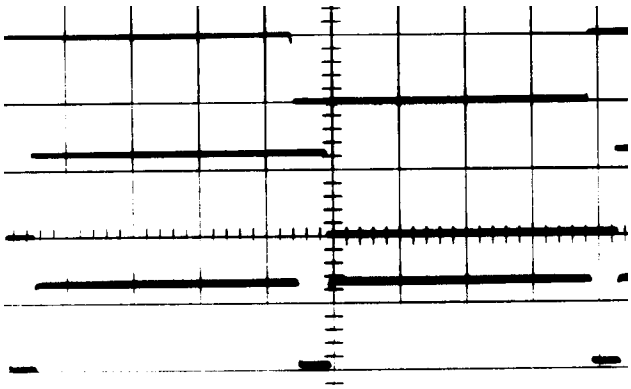
B. Phase Detector Signals, A phase.

Trace: 1. A-phase reference at TP10 (U5-11).
2. Delayed ring counter output at TP11 (U4-22)
3. Phase detector output at TP12 (U4-15).

a. a = 175°



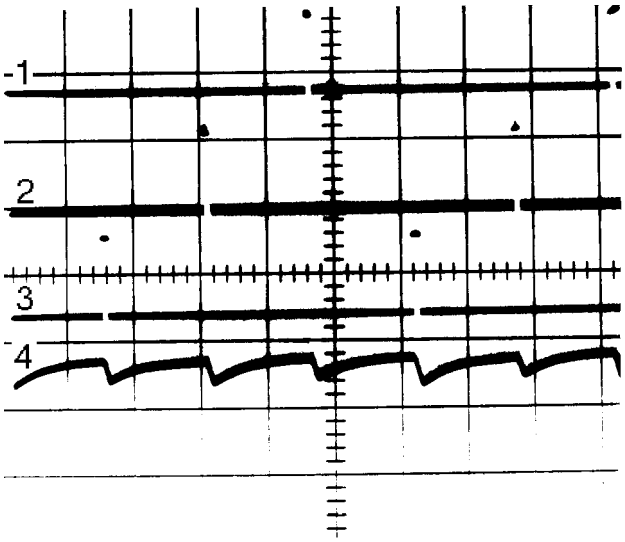
b. a = 18°



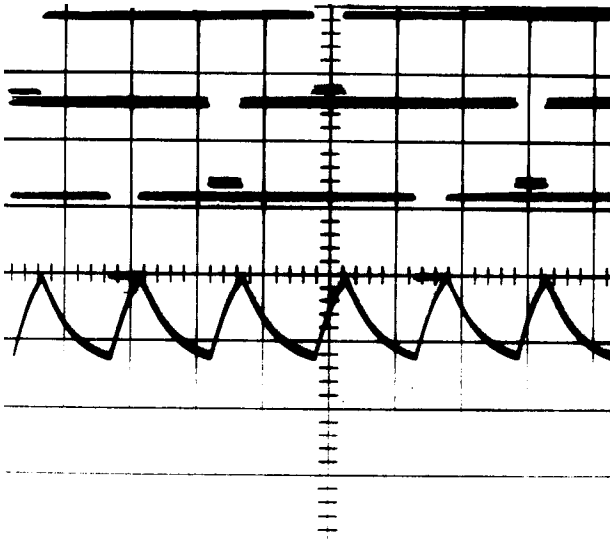
C. PLL Summing Amplifier Signals

Trace: 1. A phase detector output at U4-15 (TP12)
2. B phase detector output at U4-14
3. C phase detector output at U4-13
4. summing amplifier output at U8-1 (TP2), 2 V/div.

a. a = 175°



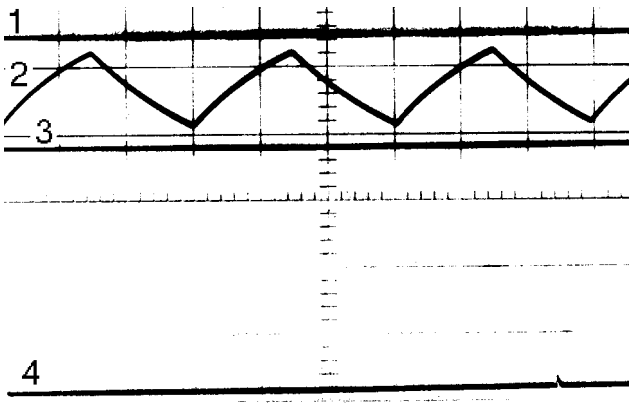
b. a = 18°



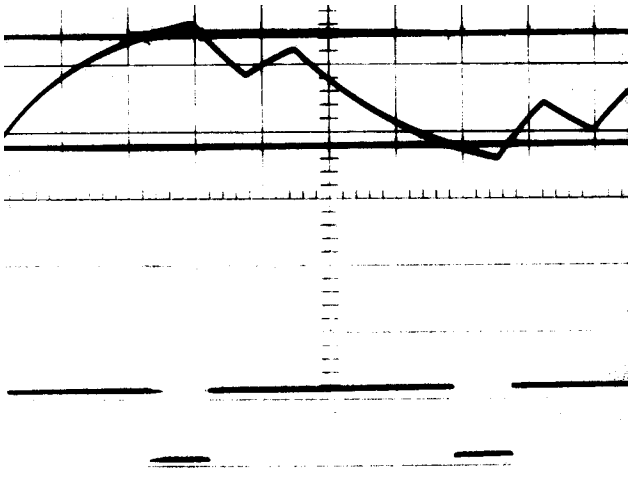
D. Phase Loss Comparator Signals

Trace: 1. upper threshold voltage at U6-9
2. summed and filtered A-B-C reference signal at U6-8 (TP16)
3. lower threshold at U6-10
4. comparator output at U6-1 ($\overline{PL}$ logic signal)

a. normal operation

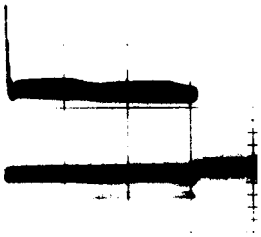


b. one mains phase missing

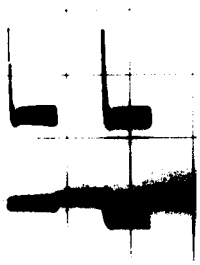


E. Pulse Transformer Output into 1.0 Ω load (.5 A/div)

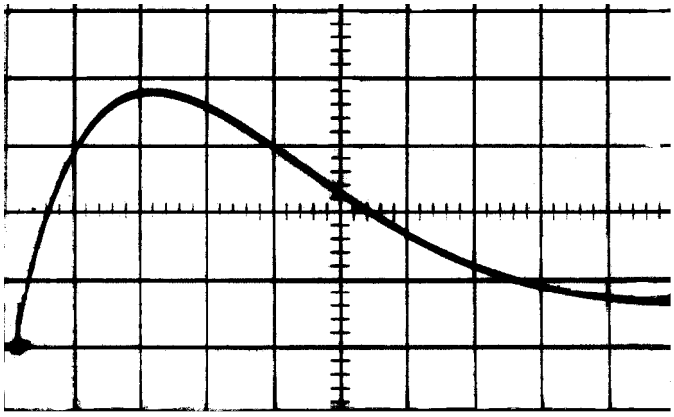
1. 120° burst of 23kHz



2. two 30° bursts



4. initial pulse detail (.5 A/div, 2 µs/div)



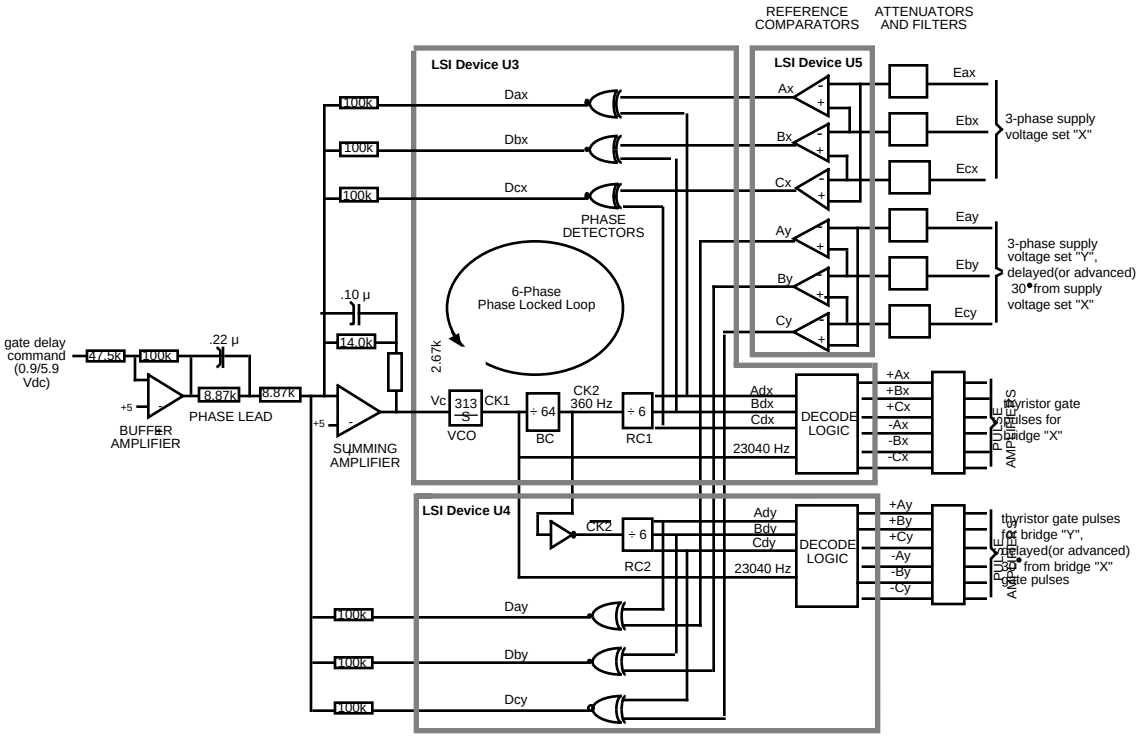
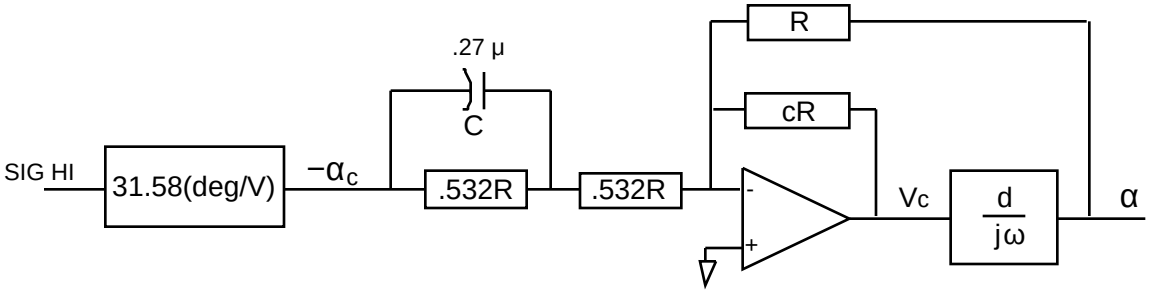


Figure 1 -- 12-Pulse Gate Delay Generator Equivalent Circuit



$$\frac{\alpha}{\text{SIG HI}} = \frac{a(jwT + 1)}{(j\omega/bc + 1)(j\omega T/2 + 1)}$$

where T = .532RC

for T = 1/bc

$$\frac{\alpha}{\text{SIG HI}} = \frac{a}{j\omega/2bc + 1}$$

for a = 29.67 deg/V, b = 1.5 V/V,
c = 300/sec, R = 16.67kΩ, C = .27 µF

$$\frac{\alpha}{\text{SIG HI}} = \frac{29.67}{j\omega/939 + 1} \left(\frac{\text{deg}}{\text{Volt}}\right)$$

Figure 2 -- 6-Phase PLL Equivalent Circuit and Transfer Function