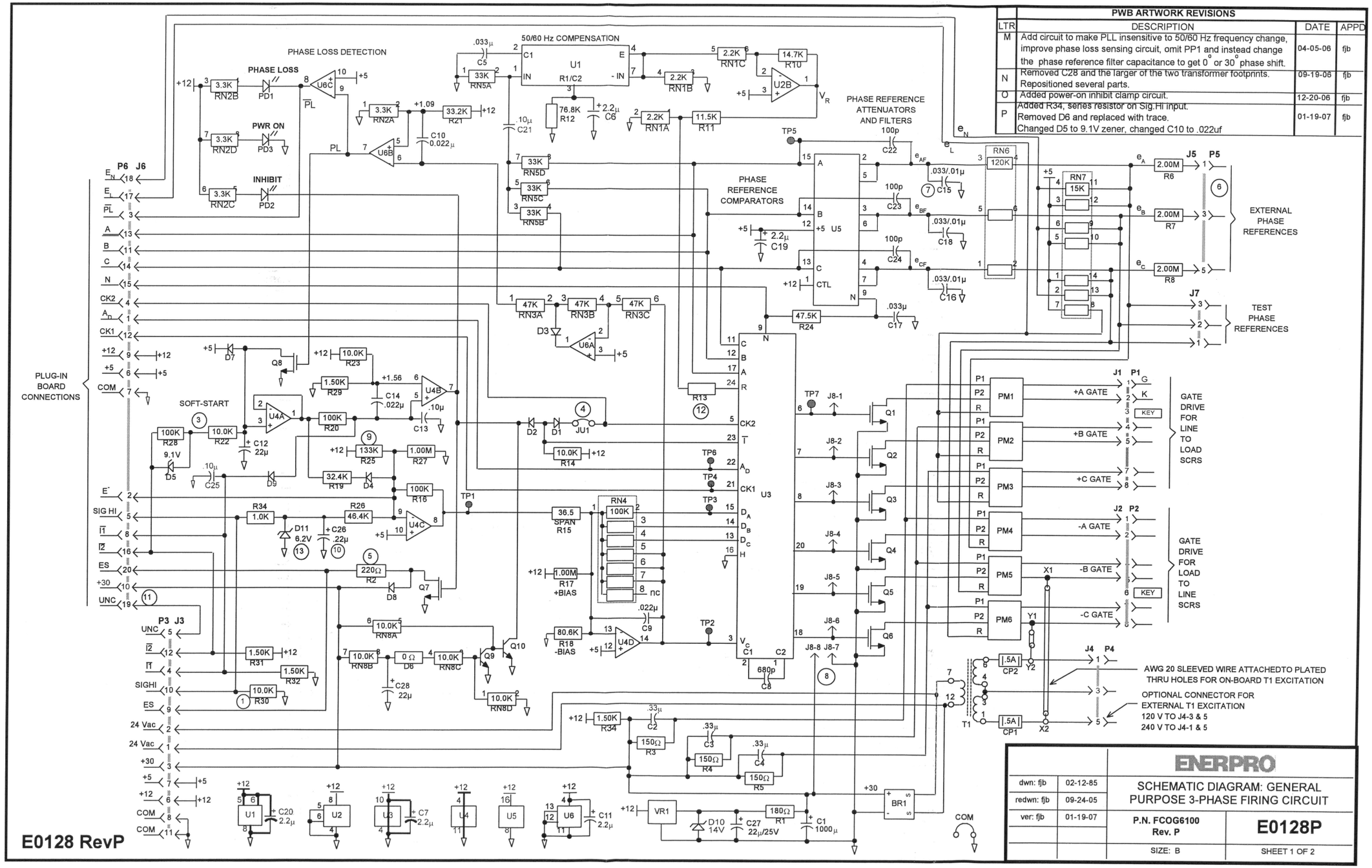

PWB ARTWORK REVISIONS

LTR	DESCRIPTION	DATE	APPD
M	Add circuit to make PLL insensitive to 50/60 Hz frequency change, improve phase loss sensing circuit, omit PP1 and instead change the phase reference filter capacitance to get 0° or 30° phase shift.	04-05-06	fjb
N	Removed C28 and the larger of the two transformer footprints. Repositioned several parts.	09-19-06	fjb
O	Added power-on inhibit clamp circuit.	12-20-06	fjb
P	Added R34, series resistor on Sig.Hi input. Removed D6 and replaced with trace. Changed D5 to 9.1V zener, changed C10 to .022uf	01-19-07	fjb

ENERPRO

dwn: fjb	02-12-85	SCHEMATIC DIAGRAM: GENERAL PURPOSE 3-PHASE FIRING CIRCUIT
redwn: fjb	09-24-05	
ver: fjb	01-19-07	P.N. FCOG6100 Rev. P — E0128P
		SIZE: B — SHEET 1 OF 2

PART	PART NUMBER	STOCK NUMBER
U1	MM2907N-8	I12907N-8
U2	MC34072BC	I134072P
U3	EP1014	I11014S
U4	MC34074BC	I134074P
U5	EP1016	I11016S
U6	MC34074BC	I134074P
VR1	LM78L12CZL	T2VL78L12
Q1-Q7	IRF110	T2IRFD110
Q8	BS170	T2NBS170
Q9-10	2N2222	T2N2222A
D1-D4	1N914B	D1N914B
D5	1N5239 9.1 V	D1N5239
D6	JF25S0R	R1F0000
D7	1N914B	D1N914B
D8	1N4004	D1N4004
D9	1N914B	D1N914B
D10	1N 5351B 14 V	D1N5351B
D11	1N 5341B 6.2 V	D1N5341B
PD1-PD2	550-2404	DIL5502404R
PD3	550-2204	DIL5502204G
BR1	W02G	D1BRW02G
RN1	6R-2-222	R1S06I222
RN2	8R-2-332	R1S08I332
RN3	6R-2-473	R1S06I473
RN4	4308R-1-1-104	R1S08NI104
RN5	8R-2-333	R1S08I333
RN6	6R-2-124	R1S06I124
RN7	4114RLF1-153	R1D14I153
RN8	8R-2-103	R1S08I103
R1	CW2C 180Ω	R1W03W180
R2	CW2C 220Ω	R1W03W220
R3-R5	CW2C 150Ω	R1W03W150
R6-R8	RN65 2.00M	RN65D2004F
R10-R34	RN60 (see table)	

RN60 RESISTORS (K Ω)

R10	14.7	R22	10.0
R11	11.5	R23	10.0
R12	76.8	R24	47.5
R13 12	select	R25 9	130
R14	10.0	R26 9	46.4
R15	36.5	R27 9	1000
R16	100	R28	100
R17	1000	R29	1.50
R18	80.6	R30	10.0
R19	32.4	R31	1.50
R20	100	R32	1.50
R21	32.3	R33	1.50
		R34	1.00

PART	PART NUMBER	STOCK NUMBER
C1	ECEA1HV102S	C1EL063102
C2	MKS4 .33u	C1FL06334
C3	MKS4 .33u	C1FL06334
C4	MKS4 .33u	C1FL06334
C5	MKS4 .033u +/-1% absolute	C1FL063333
C6	ECS-F1CE16225	C1TN016225
C7	ECS-F1CE16225	C1TN016225
C8	FKS 680p +/-1%	C1FL160681
C9	MKS4 .022u	C1FL063223
C10	MKS3 .022u	C1FL100223
C11	ECS-F1CE16225	C1TN016225
C12	ECS-F1CE16226	C1TN016226
C13	MKS02.10u	C1FL063104
C14	MKS4 .10u	C1FL100104
C15-C17	MKS4 .033u +/-1% or MKS4 .01u +/-1% 7	C1FL06333 C1FL06310
C18	MKS .033 5%	C1FL06333
C19	ECS-F1CE16225	C1TN016225
C20	ECS-F1CE16225	C1TN016225
C21	MKS3 .10u	C1FL100104
C22	FKS3 100p	C1FL160101
C23	FKS3 100p	C1FL160101
C24	FKS3 100p	C1FL160101
C25	MKSO2 .10u	C1FL063104
C26 10	ECS-F1CE16224	C1TN025224
C27	ECS-F1CE25226	C1TN025226
C28	ECS-F1CE35226	C1TN035226
PM1-PM6	EP1024	TIPW1024
CP1-CP2	PC1-2	F1PCB2
J1-J2/P1-P2	640584-2/ 640582-1	
J3/P3	340433-1/1-480708-0	
J4/P4	1-350945/ 350809-1	
J5/P5	640900/350809-1	
J6/P6	103311-5/499568-4	
J7/P7	640454-3/640440-3	
T1	EP1032B	TIPW1032B
COM RING		W1JCOMM

NOTES

NO.	DESCRIPTION
1	For current signal input, select R30 to give SIG HI = +5.0 V with maximum signal current.
2	Select R15 for desired PLL delay angle span, where $\alpha_{SPAN} = \alpha_{MAX} - \alpha_{MIN}$ Select R17 and R18 for desired PLL delay angle bias, where $\alpha_{BIAS} = 90 - (\alpha_{MAX} + \alpha_{MIN})/2$.
3	Select R28 for desired soft-start time. Select R22 for desired soft-stop time.
4	For 120 deg. burst gating, remove JU1; otherwise gating is 2-30 deg. burst mode.
5	Select R2 resistance to provide desired status relay or lamp voltage.
6	For off-board phase references, install J5 and R6-R8 in place of T1.
7	For converter gating with 30 deg. phase shifted references, install .033 μF for C15-C17. For controller gating with 0 deg. phase shifted references, install .01 μF for C15-C17.
8	For gating paralleled SCRs, connect FCOAUX60 auxiliary firing board via cable to J8
9	Refer to buffer amplifier resistance table for SIG HI range other than 0 to 5 V.
10	Select C26 capacitance in conjunction wih SIG HI source resistance to reduce the firing circuit bandwidth.
11	Jumper J6-9 to J6-19 to connect +12 to J3-5.
12	Select R13 resistance to make Vc = 5.00 +/-.05 V at TP2 with F = 60 Hz.

BUFFER AMPLIFIER RESISTANCE TABLE

SIG HI Range	Resistances in KΩ					
	R16	R19	R25	R26	R27	R30
0 / 5 V (default)	100	32.4	130	47.5	1000	10.0
.85 / 5.85 V	100	32.4	196	47.5	1000	10.0
0 / 10 V	100	32.4	1000	90.9	374	10.0
0 / 2 V	274	32.4	78.7	47.5	1000	10.0
4 / 20 mA	100	32.4	130	47.5	1000	.249

CHANGE	REASON FOR CHANGE
Date: 10-6-05 PCB Rev.: L by: fjb	
1. Replace the EP1011B LSI device with the EP1014.	The 40-pin EP1011 package will not be available in the future.
2. Replace U7 (LM 224N) quad op amp and U8 (MC14053) with the EP1016 LSI device.	Eliminates one IC
3. Replace the EP1019 pulse module with E1024 which contains internal phase reference attenuator resistors.	Eliminates exposed mains voltage conductors.
4. Remove U9 (MC14077BCP) and other components associated with reverse polarity gating.	The EP1014 does not provide reverse polarity gating.
5. Replace the power transformer with the UL/CSA regonized SPW2104.	Customers require UL/CSA recognised components.
6. Change gate drive transistors and the ES status relay from ULN2004 to six IRFD110 MOSFETS.	Allows increased gate current and eliminates CW2C resistor.
7. Omit R3 (10 ohm) and change R4-R6 from 200 ohm to 150 ohm.	Increase gate current.
8. Change zener pre-regulator from 18 V to 15 V.	Allows use of TO92 12 V regulator
9. Change 12 V regulator from TO5 to TO92 package.	Reduces board space and parts cost.
10. Replace DN1 with individual diodes.	Eases conductor routing.
11. Add hysteresis capacitors to the phase reference comparators.	Increase comparator noise immunity.
12. Take the phase loss window comparator input from the VCO command voltage instead of from the sum of the phase reference signals.	Ensures that gating is not enabled until the PLL has achieved lock.
Date: 10-21-05 PCB Rev.: M by: fjb	
1. Change the phase loss detector from a window comparator to an absolute value circuit followed by a simple comparator.	Quad op amp Plus MOSFET replaces dual comparator and diode. One op amp is now available for the automatic 50/60 Hz circuit.
2. To make the PLL delay angle independent of 50/60 Hz frequency change: use a LM2907 F/V converter followed by an inverting amplifier to produce a voltage to bias the PLL VCO timing resistance with a voltage decreasing with frequency.	A change in frequency from 60 Hz to 50 Hz now gives a -5 ^{o} change in the PLL delay angle. This compensates for the +7 ^{o} delay angle change in the phase reference filters.
3. Replace 6-pin RN4 SIP and R32 with an 8-pin non-isolated SIP.	Less board space required.
4. Move T1 right, move J1 and J2 toward board sides, remove center holes in top and bottom board edges.	Provide space for components, Enerpro logo, S.N. and P.N.
Date: 03-22-06 PCB Rev.: M by: fjb	
1. Correct error in phase reference circuit.	1. Enable operation with in-phase references.
2. Add 6.2 V zener D11 to limit SIG HI.	2. Ensure proper phase loss sensor operation.
3. Change soft-start diode D5 from 11 V zener to 1N915 diode.	3. Zener does not significantly decrease soft-start delay time.
4. Move C1 away from board edge, move R1 to board edge, increase trace width to VR1 and D10.	4. Reduce C1, R1 and D10 temperatures.
5. Delete PP1, use .01 uF or .033 uF reference filter capacitors to get 0 ^{o} or 30 ^{o} phase references.	5. Improve phase reference delay accuracy and reduce parts count.
Date: 04-01-06 PCB Rev.: M by: fjb	
1. Add C28 NOT(01) filter cappacitor.	1. Improve inhibit signal noise immunity.
2. Move VR1, R1, C1 and Q1 following 3-31-06 design review.	2. Reduce VR1 and R1 temperatures, protect C1 from handling damage, increase board edge margin.
3. Add 6.2 V zener D11 from SIG HI to COM.	3. Assure reliable phase loss circuit operation when SIG HI is out of active range.
Date: 05-09-06 PCB Rev.: M by: fjb	
1. Change R26 from 47.5K to 46.4K.	1. Provide rail-to-rail buffer amp output.
2. Add values to Buffer Amp Resistance Value Table for 0 V to 2 V SIG HI range.	2. For current regulation with the CR400 board.
3. Change Q1-Q7 part number from IRFD9110 to IRF9110	3. IRF9110 is N-channel MOSFET.
Date: 06-02-06 PCB Rev.: M by: fjb (drs)	
1. Rewire RN7	1. Phase reference correction.
Date: 09-19-06 PCB Rev.: N by: drs	
Removed C28 and the larger of the two transformer footprints. Repositioned several parts.	1. Provide more space for components.
Date: 12-19-06 PCB Rev.: 0 by: drs	
1. Add power-on inhibit clamp circuit of RN8, Q9, Q10, C28 and D8. 2. Move C13 from U4-6 to U4-5.	1. Prevent false gate enable when control power is applied. 2. Increase power-on inhibit comparator noise immunity.
Date: 01-05-07 PCB Rev.: P by: fjb	
1. Replace D6 with 0 ohm RN60 resistor. 2. Replace D5 with a 9.1 V zener. 3. Change C10 from .10 u to .022 u. 4. Added R34 on Sig. Hi input	1. Prevent gate inhibit at reduced board supply voltage. 2. Reduce soft-start enable delay time to Rev. K enable delay time. 3. Ensure phase loss inhibit when SCR circuit is disconnected from 3-phase supply. 4. Limit current through D11 and allow lowpass filter with C26

dwn: fjb	02-12-85	SCHEMATIC DIAGRAM: GENERAL PURPOSE 3-PHASE FIRING CIRCUIT
redwn: fjb	09-24-05	
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		SIZE: B — SHEET 2 OF 2