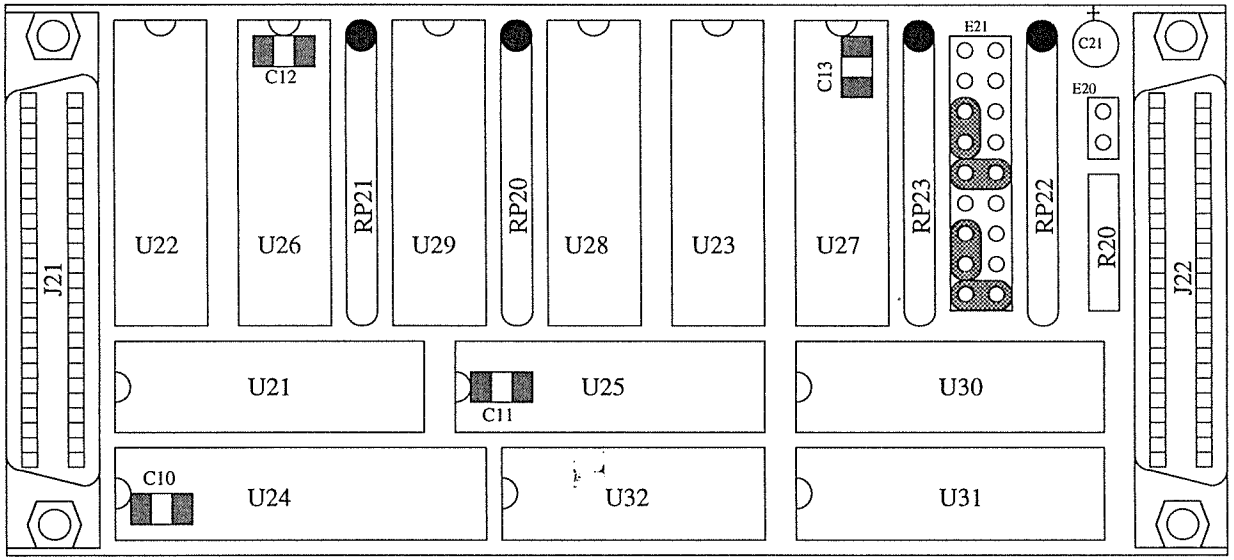
Hall A

GREENSPRING COMPUTERS, INC.
ASSEMBLY NAME: IP-DIGITAL
REVISION LEVEL: B 9013
REVISION DATE: 23-Mar-94
ELEC ASSY#: 4001410062
COMPL ASSY#: 6001410062
SHIP ASSY#: 9001410062

Part Number	DESCRIPTION	PER	LOCATION
1002014020	SKT, SIP, MS, LP, 20 pin	8	U24-U27,U31,U32,RP20-RP22
1003023106	CAP, TANT, 10µF, 16V, .1 SP	1	C21
1003133104	CHIP CAP,CER,.1µF,50V,CASE 1206	4	C10-C13
1004000101	RES, 100 Ω, 1/4W, 5%	1	R20
1004212103	RES NET, 10 PIN, 9 RES, 10K Ω	4	RP20-RP23
1006013048	HEADER, LP, STR, 1 X 48	1	E20,E21
1006973279	CONN, HD, PLUG, 50 PIN	2	J21, J22
1007030641	IC, 74ALS641-1, TI ONLY	3	U25,U26,U27
1007030990	IC, 74ALS990, TI ONLY	3	U21,U22,U23
1007070245	IC, 74HCT245, TI ONLY	3	U28, U29,U30
1007400192	PROM, 32 X 8, P40001B	1	U32
1007622210	CMOS PAL, 22V10A, G40500A	1	U24
1007721681	GAL, 16V8-25, 1/4 POWER, G40501C	1	U31
1009000002	SHUNT, LOW PROFILE	8	E21, (3 ENG KIT)
3001410062	PCB, IP-DIGITAL24 B	1	
3007010006	LABEL, IP-DIGITAL	1	SOLDER SIDE

REVISIONS

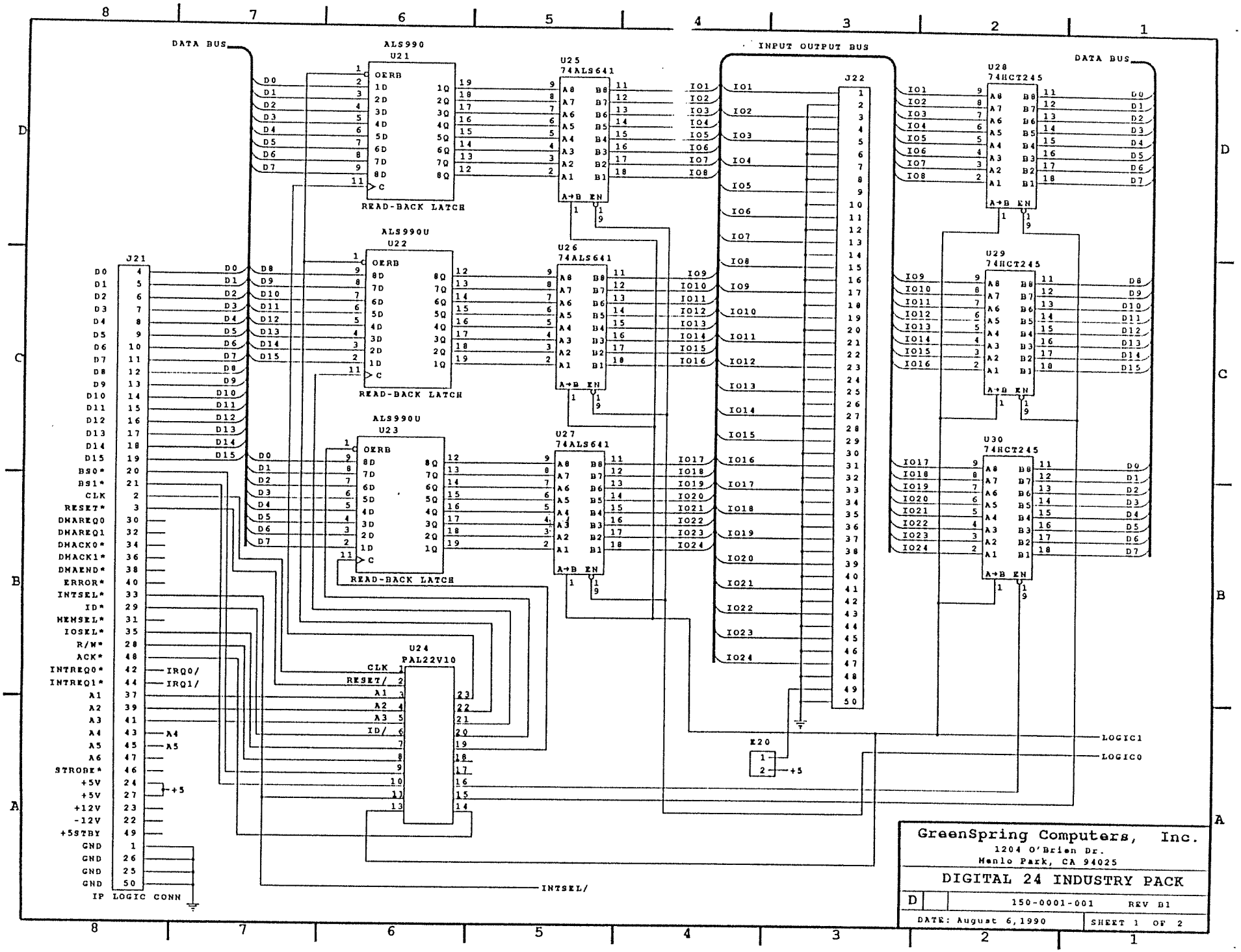
ECO #	DESCRIPTION	DATE
	RELEASE TO PRODUCTION	May 15, 1989
9013	REMOVE INTERUPT JUMPER	2/22/90



ASSEMBLY NOTES:

1: MAXIMUM HEIGHT OF TANT CAPS IS .30"
2: COMPONENT LEAD LENGTH ON SOLDER SIDE IS NOT TO EXCEED .040"
3: ASSEMBLE PER QUALITY STANDARDS IPC CLASS II
4: EXPOSED COPPER ON SOLDER SIDE IS NOT ACCEPTABLE
5: WARP / TWIST NOT TO EXCEED .010"
6: CONNECTORS J21 AND J22 MUST BE FLUSH WITH BOARD
7: ALL LOCATIONS ARE FILLED
8: NO COMPONENTS MAY PROTRUDE FROM BOARD EDGE

GREENSPRING COMPUTERS, INC.		
	ASSEMBLY: 4001410062	DRAWN BY
		FRED TREVOR
IP-DIGITAL ELECTRONIC ASSEMBLY		
REV B	Dec 1, 1990	SHEET 1 OF 1

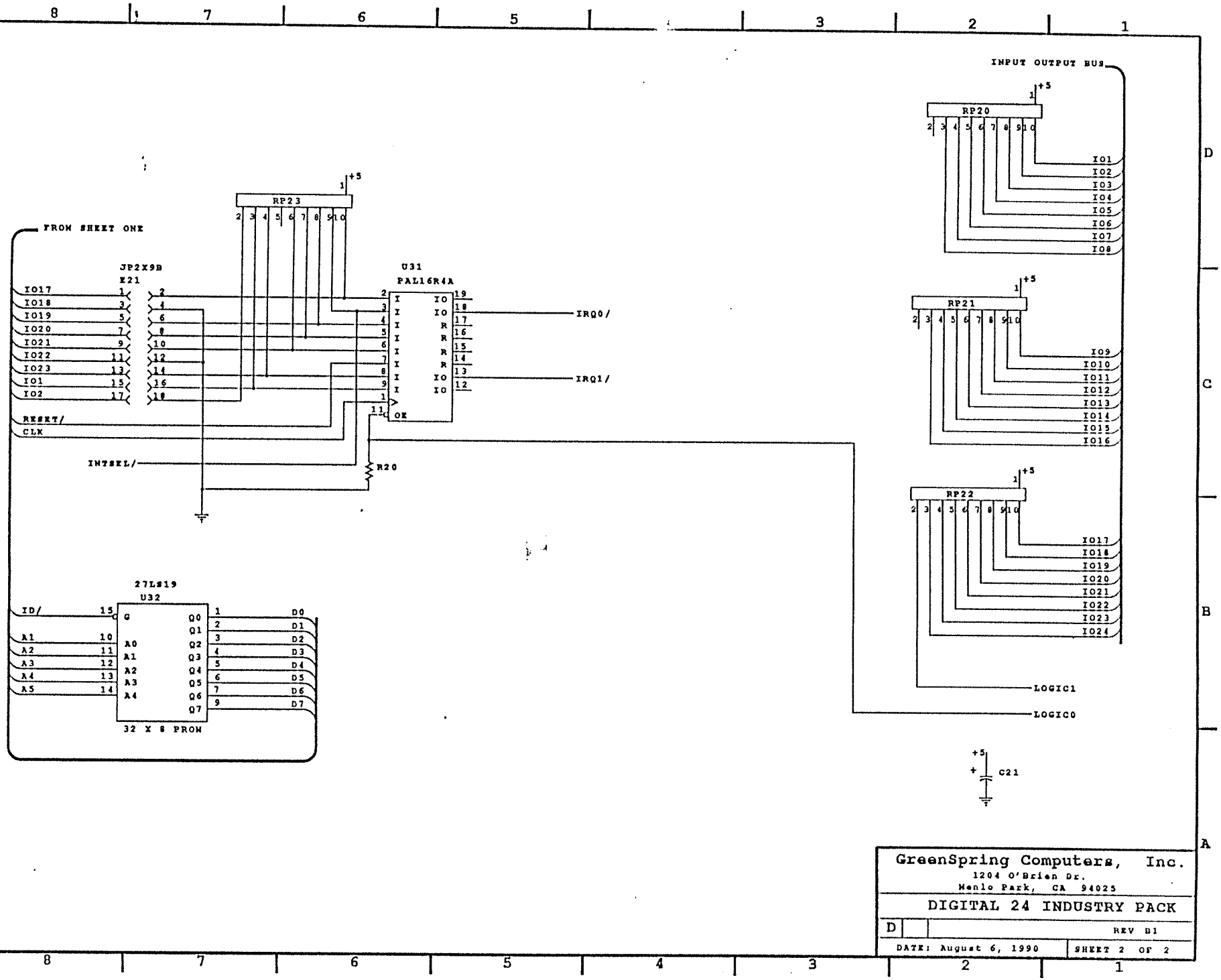


GreenSpring Computers, Inc.
1204 O'Brien Dr.
Menlo Park, CA 94025

DIGITAL 24 INDUSTRY PACK

D | 150-0001-001 REV B1

DATE: August 6, 1990 | SHEET 1 OF 2



GreenSpring Computers, Inc.
1204 O'Brien Dr.
Menlo Park, CA 94025

DIGITAL 24 INDUSTRY PACK

D | REV B1

DATE: August 6, 1990 | SHEET 2 OF 2

```
Name            N40500A;
Partno          0204-0500A;
Revision        A3;
Date            1 dec 88;
Designer        Kim Rubin;
Company         GreenSpring Computers, Inc.;
Assembly        IPdigit;
Location        U24;
Device          P22V10;         /* CMOS only */
Format          j;

/* Copyright 1989 GreenSpring Computers */

/*************************************************************************/
/*                              TTL                                      */
/*                                                                       */
/*      This PAL is the primary control for the TTL Industry Pack.       */
/*                                                                       */
/*                                                                       */
/*      Allowable Devices: CMOS 22V10 only.                              */
/*                                                                       */
/*************************************************************************/

/**  Inputs  **/

Pin     1       =       CLK;            /* 8 Mhz from IP Logic Interface    */
Pin     2       =       !RESET;         /* From Logic Interface             */
Pin     3       =       A1;             /* From Logic Interface             */
Pin     4       =       A2;             /* From Logic Interface             */
Pin     5       =       A3;             /* From Logic Interface             */
Pin     6       =       !ID;            /* From Logic Interface             */
Pin     7       =       !IOSEL;         /* From Logic Interface             */
Pin     8       =       !WR;            /* From Logic Interface             */
Pin     9       =       !BS0;           /* From Logic Interface             */
Pin     10      =       !BS1;           /* From Logic Interface             */
Pin     11      =       !INTSEL;        /* From Logic Interface             */


/**  Outputs  **/

Pin     23      =       LDLOW;          /* Load Byte D7..D0                 */
Pin     22      =       !RBDATA;        /* Readback Data (hi and lo)        */
Pin     21      =       LDHIGH;         /* Load Byte D15..D8                */
Pin     20      =       !OEINT;         /* Output Enable Int Vect           */
Pin     19      =       LDINT;          /* Load Interrupt Vector            */
Pin     18      =       !cycle;         /* Used internally                  */
Pin     16      =       !RDEXT;         /* Enable transceiver D23..D16      */
Pin     15      =       !RDDATA;        /* Enable transceiver D15..D0       */
Pin     14      =       !ACK;           /* To Logic Interface               */

/**  Declarations and intermediate equations  **/

lowdat  =       !A3 & !A2 & !A1;        /* read/write data 15..0            */
highdat =       !A3 & !A2 &  A1;        /* read/write data 23..16           */
dirlow  =       !A3 &  A2 & !A1;        /* direct read data 15..0           */
dirhigh =       !A3 &  A2 &  A1;        /* direct read data 23..16          */
MEMSEL  =       IOSEL;                  /* for future expansion             */


/*************************************************************************/
/*                      ADDRESS MAP                                      */
/*                                                                       */
/*              Word 00         Data write and readback 15..0            */
/*              Byte 03         Data write and readback 23..16 (int vect)*/
/*              Word 04         Direct read of 15..0                     */
/*              Byte 07         Direct read of 23..16                    */
/*                                                                       */
```

```
/*      Writing a bit value of 1 generates a pull-up high.                  */
/*      Writing a bit value of 1 enables input for that bit.                */
/*      Writing a bit value of 0 generates an active sink (low) output.     */
/*      Readback reads writen values, not actual data on I/O pins.          */
/*      Readback is useful for software read-modify-write cycles.           */
/*      Use Direct read for reading actual data on I/O pins.                */
/*      Bits 23..16 used for the interrupt vector, if interrupts used.      */
/*                                                                          */
/**************************************************************************/


/**  Logic equations  **/

LDLOW.d         =       lowdat & BS0 & WR & IOSEL & !cycle
                #       lowdat & BS0 & WR & MEMSEL & !cycle
                #       RESET & !LDLOW;

RBDATA.d        =       lowdat & !WR & IOSEL
                #       lowdat & !WR & MEMSEL
                #       RBDATA & !ACK;

LDHIGH.d        =       lowdat & BS1 & WR & IOSEL & !cycle
                #       lowdat & BS1 & WR & MEMSEL & !cycle
                #       RESET & !LDHIGH;

OEINT.d         =       highdat & !WR & IOSEL
                #       highdat & !WR & MEMSEL
                #       INTSEL & !WR
                #       OEINT & !ACK;

LDINT.d         =       highdat & BS0 & WR & IOSEL & !cycle
                #       highdat & BS0 & WR & MEMSEL & !cycle
                #       RESET & !LDINT;

cycle.d         =       (IOSEL # MEMSEL) & !ACK & WR
                #       (IOSEL # MEMSEL # ID # INTSEL) & !WR
                #       cycle & IOSEL & !RESET
                #       cycle & MEMSEL & !RESET
                #       cycle & ID & !RESET
                #       cycle & INTSEL & !RESET;

RDEXT.d         =       dirhigh & !WR & IOSEL
                #       dirhigh & !WR & MEMSEL
                #       RDEXT & !ACK;

RDDATA.d        =       dirlow & !WR & IOSEL
                #       dirlow & !WR & MEMSEL
                #       RDDATA & !ACK;

ACK.d           =       IOSEL
                #       MEMSEL
                #       ID
                #       INTSEL;


/**  Fixup equations  **/

LDLOW.AR        =       'b'0;
LDLOW.SP        =       'b'0;
RBDATA.AR       =       'b'0;
RBDATA.SP       =       'b'0;
LDHIGH.AR       =       'b'0;
LDHIGH.SP       =       'b'0;
OEINT.AR        =       'b'0;
OEINT.SP        =       'b'0;
LDINT.AR        =       'b'0;
```

```
LDINT.SP        =       'b'0;
RDEXT.AR        =       'b'0;
RDEXT.SP        =       'b'0;
RDDATA.AR       =       'b'0;
RDDATA.SP       =       'b'0;
ACK.AR          =       'b'0;
ACK.SP          =       'b'0;
cycle.AR        =       'b'0;
cycle.SP        =       'b'0;
```

```
Name            G40501C;
Partno          G40501C;
Revision        C;
Date            22 February 1990;
Designer        Kim Rubin;
Company         GreenSpring Computers, Inc.;
Assembly        IP-DIGITAL 24;
Location        U31;
Device          g16v8;
Format          j;
```

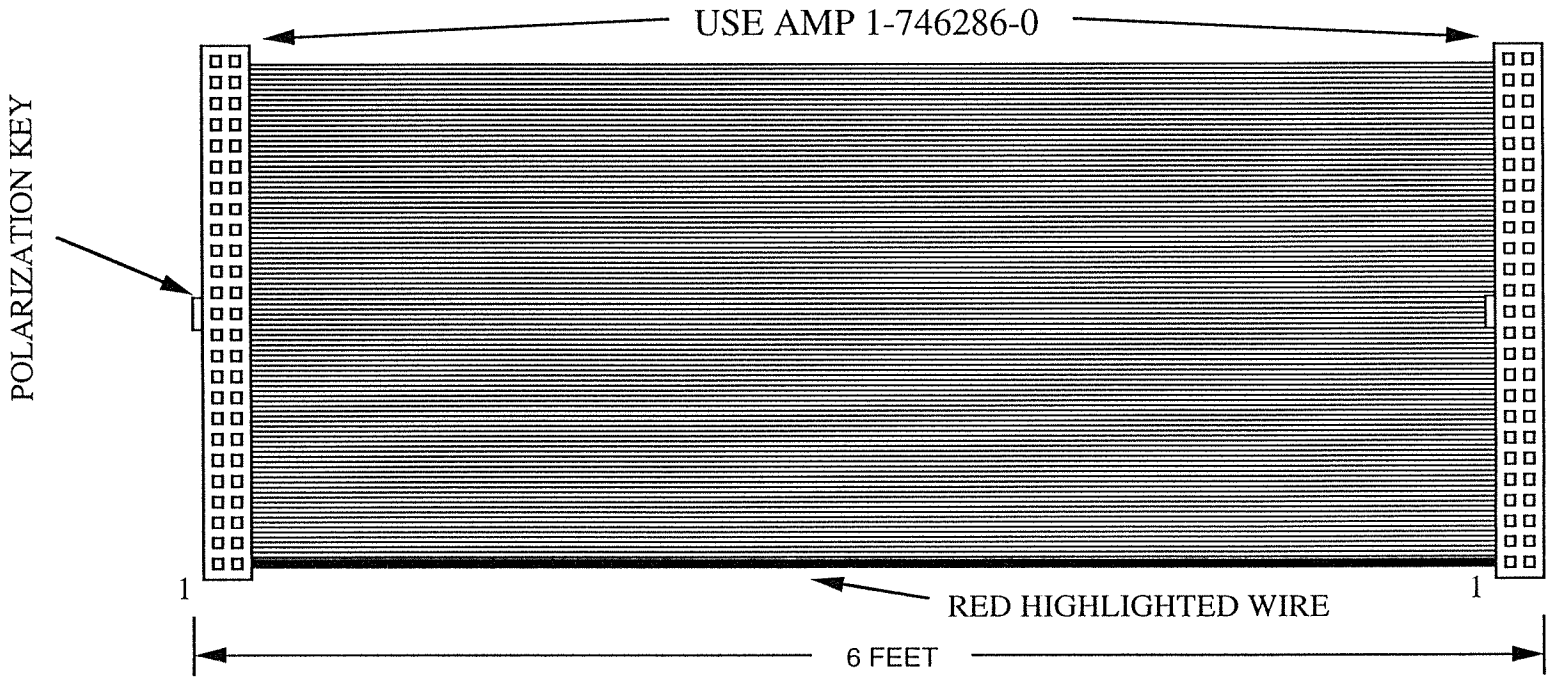


```
/*************************************************************************/
/*                                                                       */
/*      This PAL is the Interrupt Control for the IP-Digital 24          */
/*      Industry Pack.                                                   */
/*                                                                       */
/*      Allowable Devices: GAL 16V8 or similar                           */
/*                                                                       */
/*      Rev C   2/22/90 XKR     Fixed REQ0                               */
/*      GAL     2/22/90 XKR     Switched to GAL                          */
/*************************************************************************/

/*************************************************************************/
/*                                                                       */
/*      int disable     IRQ0    A       low = enable    I/O 17 default  */
/*      rising edge     IRQ0    C                       GND default     */
/*      falling edge    IRQ0    D                       open default    */
/*      int disable     IRQ1    E       low = enable    I/O 21 default  */
/*      rising edge     IRQ1    G                       GND default     */
/*      falling edge    IRQ1    H                       open default    */
/*                                                                       */
/*      Pullup resistors on all lines mean open is logic high.           */
/*************************************************************************/

/**  Inputs  **/

Pin     1       =       CLK;            /* 8 Mhz from IP Logic Interface    */
Pin     2       =       A;              /* E21 pin 2                        */
Pin     3       =       !INTSEL;        /* From Logic Interface             */
Pin     4       =       C;              /* E21 pin 6                        */
Pin     5       =       D;              /* E21 pin 8                        */
Pin     6       =       E;              /* E21 pin 10                       */
Pin     7       =       !RESET;         /* From Logic Interface             */
Pin     8       =       G;              /* E21 pin 14                       */
Pin     9       =       H;              /* E21 pin 16                       */
Pin     11      =       !OE;            /* Logic Low                        */


/**  Outputs  **/

Pin     18      =       !IRQ0;          /* To Logic Interface               */
Pin     17      =       !DSYNC;         /* Synchronize D input              */
Pin     16      =       !HSYNC;         /* Synchronize H input              */
Pin     15      =       !REQ0;          /* Int Req 0 latch                  */
Pin     14      =       !REQ1;          /* Int Req 1 latch                  */
Pin     13      =       !IRQ1;          /* To Logic Interface               */

/**  Declarations and intermediate equations  **/

/**  Logic equations  **/

/*  Below are two switch debounce equations:
    Commented out.
IRQ0            =       !RESET & !INTSEL & !(!IRQ0 # !A)
/               #       !RESET &  C
```

```
                #       !RESET & !D ;

IRQ1            =       !RESET & !INTSEL & !(!IRQ1 # !E)
                #       !RESET &  G
                #       !RESET & !H ;
*/

/*      D is the falling edge asynchronous INT0 external
input.  C is the rising edge asysnchronous INT0 external
input.
*/
DSYNC.D         =       C
                #       !D ;

/*      H is the falling edge asynchronous INT1 external
input.  G is the rising edge asynchronous INT1 external
input.
*/
HSYNC.D         =       G
                #       !H ;

/*      First term is the latch: once set REQ0 stays set
until the IACK cycle. Second term detects D falling edge.
Third term detects C rising edge.  RESET clears pending.
*/
REQ0.D          =       !RESET & !INTSEL & REQ0
                #       !RESET & !D & !DSYNC
                #       !RESET &  C & !DSYNC;

/*      First term is the latch: once set REQ1 stays set
until the IACK cycle.  Second term detects H falling edge.
Third term detects G rising edge.  RESET clears pending.
*/
REQ1.D          =       !RESET & !INTSEL & REQ1
                #       !RESET & !H & !HSYNC
                #       !RESET &  G & !HSYNC;

/*      A is the active low interrupt enable for IRQ0.
*/
IRQ0            =       REQ0 & !A ;

/*      E is the active low interrupt enable for IRQ1.
*/
IRQ1            =       REQ1 & !E ;
```

REVISIONS

ECO #	DESCRIPTION	DATE
	RELEASE TO PRODUCTION	February 6, 1990



Kit includes:

1: 6' Data cable (3005051650)
2: Terminal Block (3009001050)
3: Technical documentation

GREENSPRING COMPUTERS, INC.		
ENGINEERING KIT		DRAWN BY FRED TREVOR
IP-DIGITAL24		
REV **A**	February 6, 1990	SHEET 1 of 1