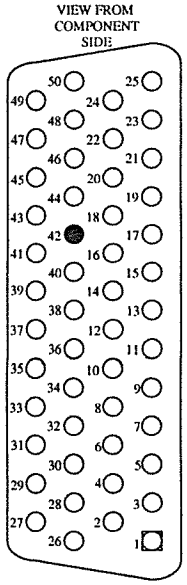
Hall A

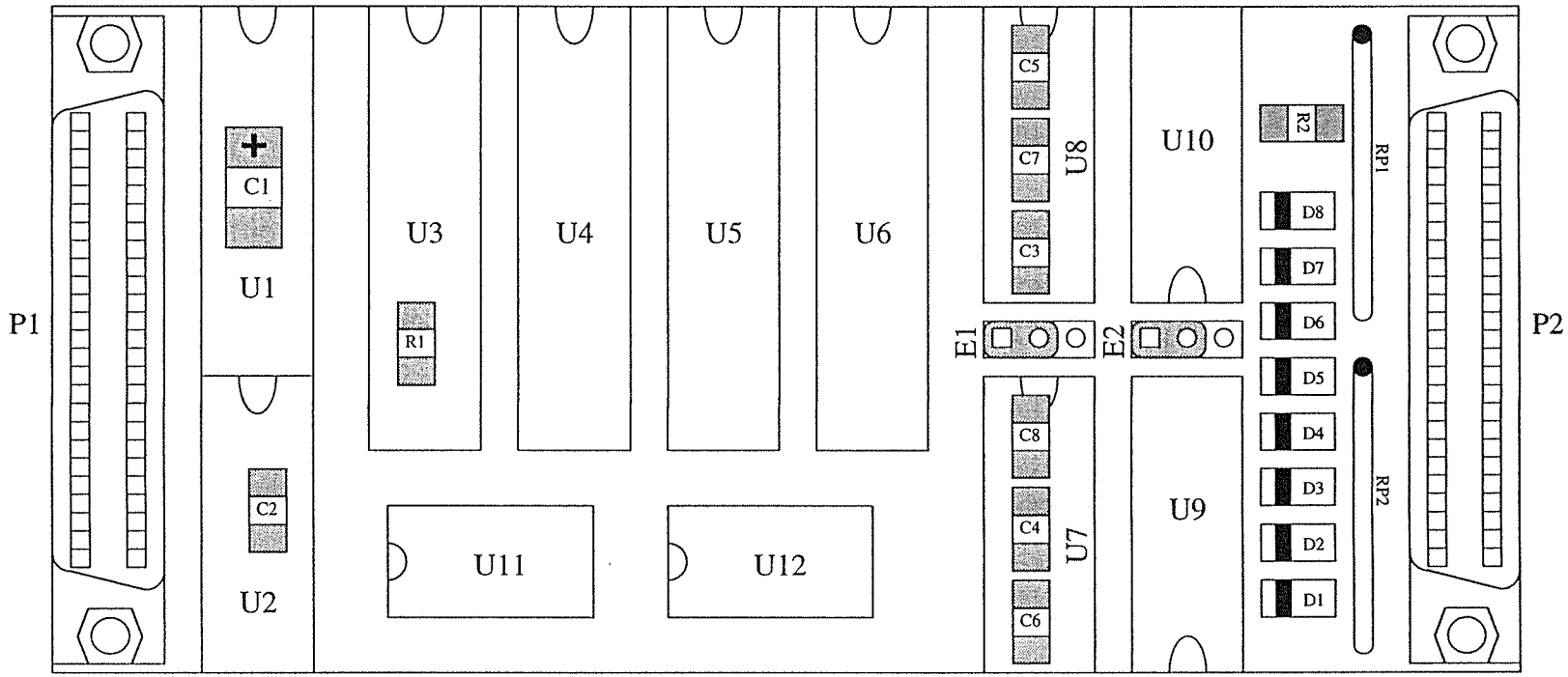
GreenSpring Computers, Inc
ASSEMBLY NAME: IP-Opto Interrupter
REVISION LEVEL: A 93066
REVISION DATE: 13-Oct-93
ELEC ASSY#: 4001410441
COMPL ASSY#: 6001410441
SHIP ASSY#: 9001410441

PART NUMBER	DESCRIPTION	PER	LOCATION
1002014008	SKT, SIP, MSLP, 8 PIN	8	U2,U7,U8, RP1, RP2
1002014010	SKT, SIP, MSLP, 10 PIN	2	U1
1002014012	SKT, SIP, MSLP, 12 PIN	8	U3-U6
1003127226	CHIP CAP,TANT,22µF,6.3V,CASE SIZE C	1	C1
1003133033	CHIP CAP, CER, 3.3pF, SIZE 1206	2	C3,C4
1003133102	CHIP CAP,CER,1000pF,SIZE 1206	2	C5,C6
1003133103	CHIP CAP,CER,.01µF,SIZE 1206	2	C7,C8
1003133104	CHIP CAP,CER,.1µF,SIZE 1206 CHIP	1	C2
1004100101	RES, 100 Ω, 1206 CHIP, 5%	2	R1,R2
1004221152	RES NET, 8 PIN, 4 RES, 1.5KΩ	2	RP1,RP2
1005164148	DIODE, 1N4148, LL-34	8	D1-D8
1006013003	HEADER, LP, 1 X 3	2	E1, E2
1006973279	CONN, HD, PLUG, 50 PIN	2	P1,P2
1007170374	SOIC, 74HCT374	2	U11,U12
1007214490	IC, MC14490P	2	U7,U8
1007245720	IC, ILQ2	2	U9,U10
1009000002	SHUNT, LOW PROFILE	2	E1
3001410441	PCB, IP-OPTO INTERUPTER A	1	
5003428011	PRG PROM, P42801	1	U2
5003428021	PRG PROM, P42802	4	U3-U6
5005428011	PRG GAL, G42801	1	U1
	label, sticky back ...	1	
OPTIONAL RES NETS			
1004221751	RES NET, 8 PIN, 4 RES, 750 Ω (-LOGIC)	2	RP1,RP2
1004221472	RES NET, 8 PIN, 4 RES, 4.7K Ω (-12V)	2	RP1,RP2
1004221752	RES NET, 8 PIN, 4 RES, 7.5K Ω (-24V)	2	RP1,RP2
1004221101	RES NET, 8 PIN, 4 RES, 100 Ω (RS422)	2	RP1,RP2

REVISIONS

ECO #	DESCRIPTION	DATE
9016	RELEASE TO PRODUCTION	27 Mar 90
9059	PAL Restriction	15 Nov 90
	Correct U11 & U12 Polarity	19 Feb 1991
93066	Add -422 Option	13 Oct 1993

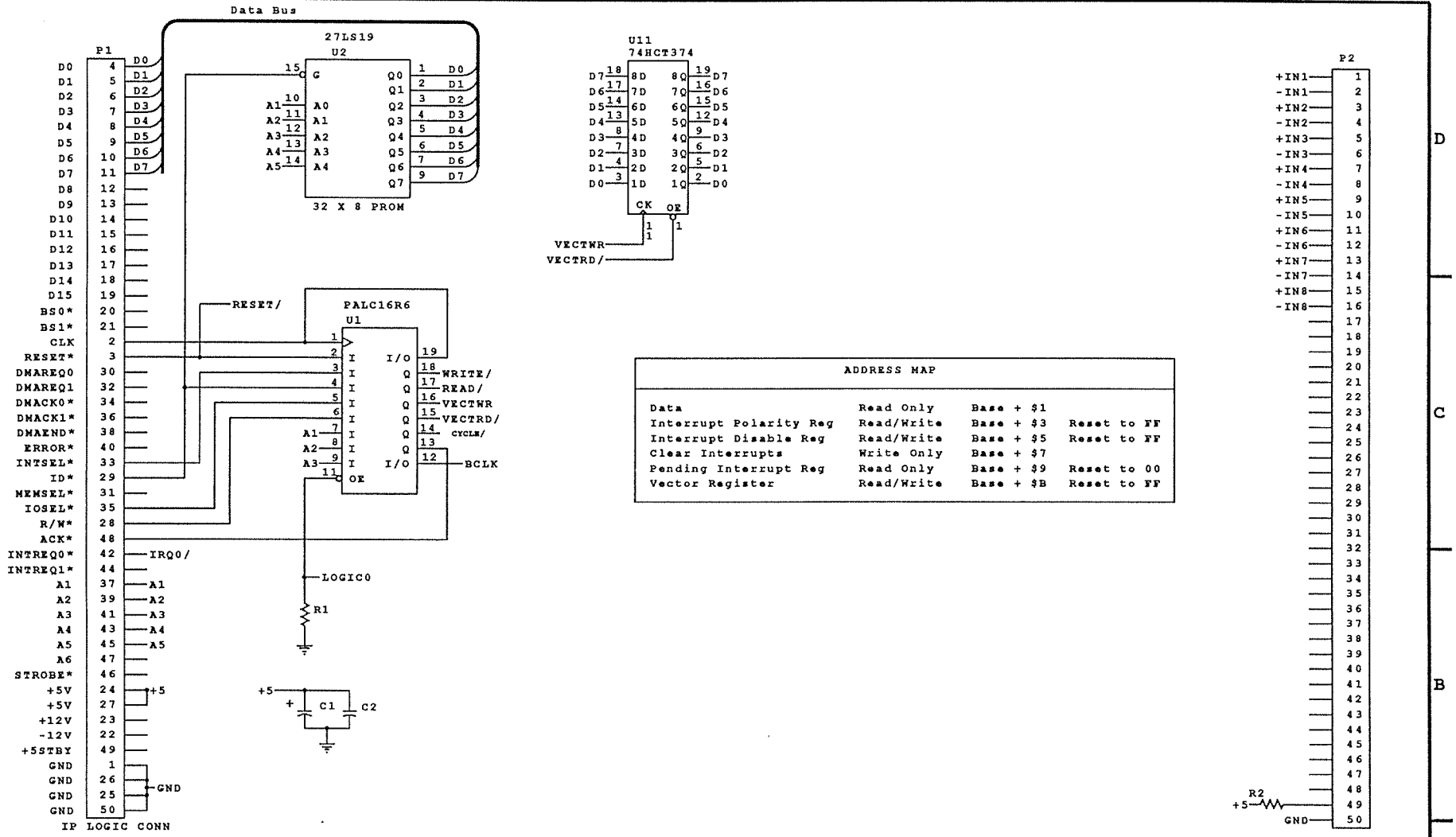




ASSEMBLY NOTES:

1: COMPONENT LEAD LENGTH ON SOLDER SIDE IS TO BE SANDED FLUSH
2: ASSEMBLE PER QUALITY STANDARDS IPC CLASS II
3: EXPOSED COPPER ON SOLDER SIDE IS NOT ACCEPTABLE
4: WARP / TWIST NOT TO EXCEED .010"
5: ALL COMPONENTS MUST BE FLUSH WITH BOARD
6: ALL LOCATIONS ARE FILLED
7: NO COMPONENTS MAY PROTRUDE FROM BOARD EDGE
8: ADD WIRE COMPONENT SIDE P1.42 TO U3.10

GREENSPRING COMPUTERS, INC.		
	ASSEMBLY: 4001410441	DRAWN BY Fred Trevor
IP-Opto Interrupter Electronic Assembly		
REV A	13 Oct 1993	SHEET 1 of 1



ADDRESS MAP			
Data	Read Only	Base + $1	
Interrupt Polarity Reg	Read/Write	Base + $3	Reset to FF
Interrupt Disable Reg	Read/Write	Base + $5	Reset to FF
Clear Interrupts	Write Only	Base + $7	
Pending Interrupt Reg	Read Only	Base + $9	Reset to 00
Vector Register	Read/Write	Base + $B	Reset to FF

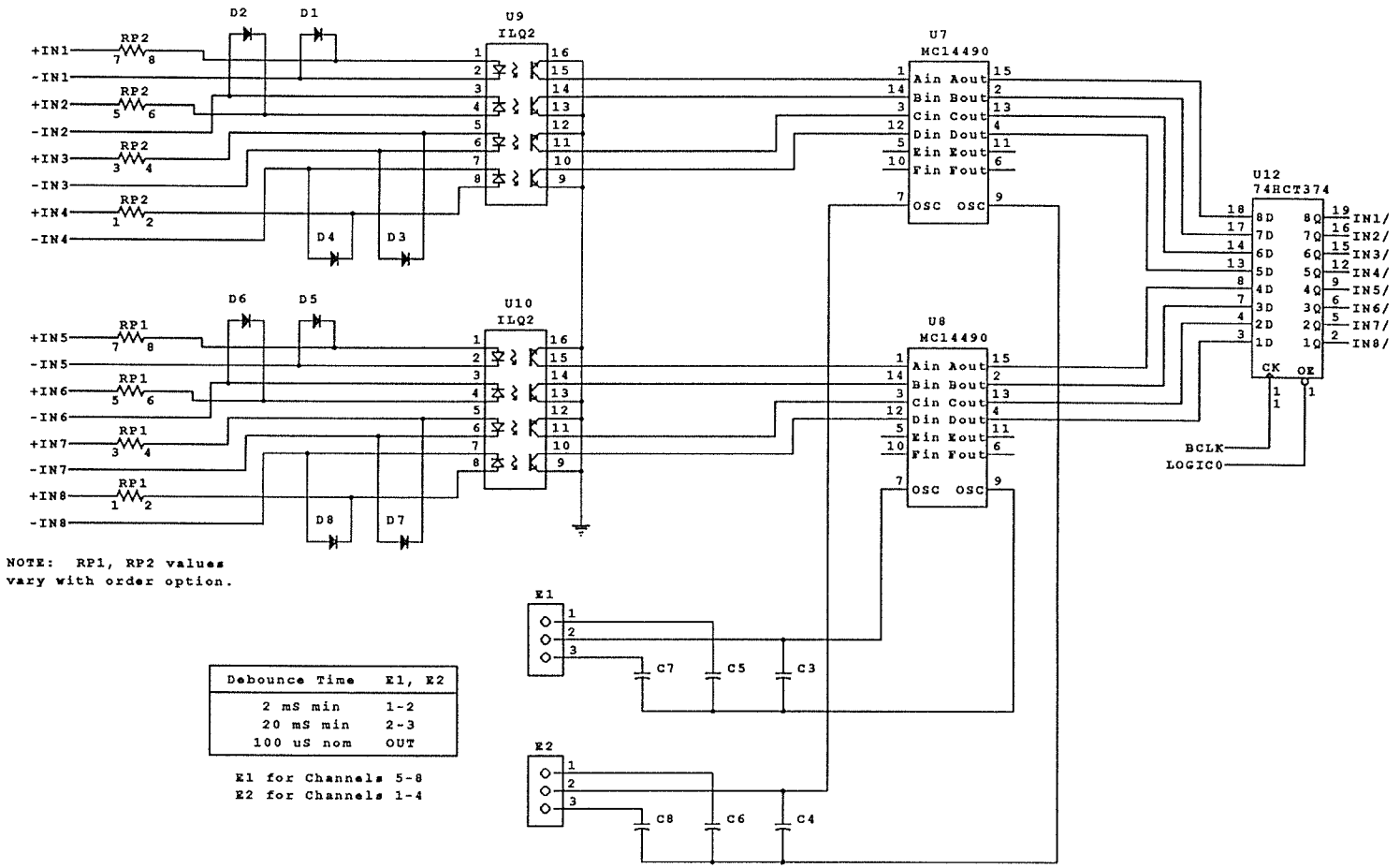
ECO 9016

GREENSPRING COMPUTERS INC
1204 O'BRIEN DR
MENLO PARK, CA

IP-Opto Interrupter

D | REV A

DATE: February 27,1990 | SHEET 1 OF 3



NOTE: RP1, RP2 values vary with order option.

Debounce Time	E1, E2
2 mS min	1-2
20 mS min	2-3
100 uS nom	OUT

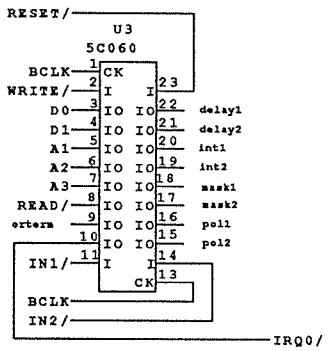
E1 for Channels 5-8
E2 for Channels 1-4

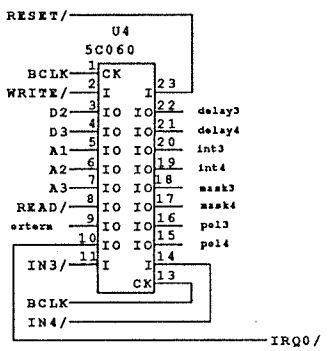
GREENSPRING COMPUTERS INC
1204 O'BRIEN DR
MENLO PARK, CA

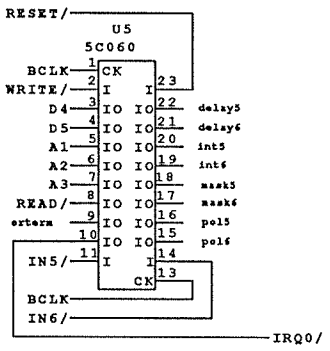
IP-Opto Interrupter

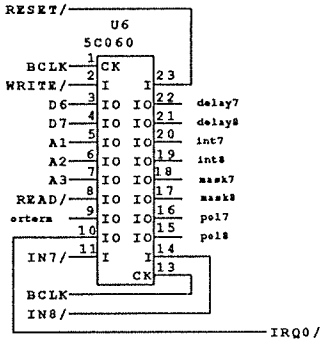
D REV A

DATE: February 27, 1990 SHEET 2 OF 3









GREENSPRING COMPUTERS INC	
1204 O'BRIEN DR MENLO PARK, CA	
IP-Opto Interrupter	
D	REV A
DATE: February 27,1990	SHEET 3 OF 3

```
Name        G42801B ;
Partno      G42801B ;
Revision    B;
Date        14 May 1990;
Designer    Kim Rubin;
Company     GreenSpring Computers, Inc;
Assembly    IP-Opto Interrupter;
Location    U1;
Device      g16v8;
Format      j;

/*  COPYRIGHT 1990, GREENSPING COMPUTERS, INC.  */

/*************************************************************************/
/*                                                                       */
/*      Allowable Devices: GAL 16V8Q25 or similar.                       */
/*                                                                       */
/*      Rev A   26 Feb 90                                                */
/*      Rev B   14 May 90       Fixed vector and read on at same time.   */
/*************************************************************************/

/**  Inputs  **/

Pin     1       =       CLK;            /* 8 MHz from IP Logic Interface     */
Pin     2       =       !RESET;         /* Data Line I/O from Logic Interf.  */
Pin     3       =       !INTSEL;        /* Interrupt Select from Logic.      */
Pin     4       =       !ID;            /* ID Select from Logic Interface    */
Pin     5       =       !IOSEL;         /* Data Line I/O from Logic Interf.  */
Pin     6       =       !WR;            /* Write Strobe from control PAL     */
Pin     7       =       A1;             /* Address Line from Logic Interf.   */
Pin     8       =       A2;             /* Address Line from Logic Interf.   */
Pin     9       =       A3;             /* Address Line from Logic Interf.   */
Pin     11      =       !OE;            /* Registered Outputs enabled        */
Pin     19      =       CLKin;          /* 8MHz clock, same as pin 1         */


/**  Outputs  **/

Pin     18      =       !WRITE;         /* Write Strobe to other logic       */
Pin     17      =       !READ;          /* Read (OE) Strobe to other logic   */
Pin     16      =       !VECTWR;        /* Interrupt Vector write            */
Pin     15      =       !VECTRD;        /* Interrupt Vector read             */
Pin     14      =       !cycle;         /* Records cycle in progress         */
Pin     13      =       !ACK;           /* To Logic Interface                */
Pin     12      =       CLKout;         /* Buffered 8 MHz.                   */



/**  Declarations and intermediate equations  **/

Data            =       !A1 & !A2 & !A3;
PolReg          =        A1 & !A2 & !A3;
MaskReg         =       !A1 &  A2 & !A3;
ClearReg        =        A1 &  A2 & !A3;
IntReg          =       !A1 & !A2 &  A3;
VectReg         =        A1 & !A2 &  A3;
ClearAll        =        A1 &  A2 &  A3;

/*************************************************************************/
/*                      ADDRESS MAP                                      */
/*                                                                       */
/*  Data                        Read    base + $1                        */
/*  Interrupt Polarity Register R/W     base + $3                        */
/*  Interrupt Disable Register  R/W     base + $5                        */
/*  Clear Interrupts            Write   base + $7                        */
/*  Pending Interrupts Register Read    base + $9                        */
```

```
/*  Vector Register            R/W     base + $B                          */
/*                                                                        */
/*  See listing for N42802 for more info on register usage.               */
/*                                                                        */
/*  Rev A       2/27/90 XKR Release, ClearAll location not supported.     */
/*                                                                        */
/************************************************************************/


/**  Logic equations  **/

/*  CLKout is the opposite polarity of CLKin to give the
    interrupt logic PLDs their necessary setup time.
*/
CLKout          =       !CLKin;

/*  cycle implements one wait state.
*/
cycle.d         =       IOSEL & PolReg
                P       IOSEL & MaskReg
                P       IOSEL & IntReg & !WR
                P       IOSEL & Data & !WR
                P       IOSEL & ClearReg & WR
                P       IOSEL & VectReg
                P       cycle & IOSEL & !RESET;

/*  No wait states on ID.
    One wait state for register access.
*
 ..d            =       ID
                P       INTSEL
                P       cycle & !ACK
                P       ACK & IOSEL & !RESET;

/*  The WRITE strobe goes to the four bit-slice interrupt control
    EPLDs.  It is one clock wide.
*/
WRITE.d         =       IOSEL & PolReg & WR & !cycle
                P       IOSEL & MaskReg & WR & !cycle
                P       IOSEL & ClearReg & WR & !cycle;

/*  READ is also a control line to the bit-slice EPLDs.
    On always except for vector read.
    It stays on to implment hold states.
*/
READ.d          =       IOSEL & !WR & !VectReg
                P       READ & !ACK & !RESET;

/*  VECTWR latches the vector into the discreet vector register
    on its trailing edge.  It is one clock wide.
*/
VECTWR.d        =       IOSEL & VectReg & WR & !ACK
                P       RESET;

/*  VECTRD reads the vector back.  This is used mostly
    for interrupt cycles, but the register can be read
    in the IO space, too.
*/
VECTRD.d        =       IOSEL & VectReg & !WR & !RESET
                P       INTSEL & !WR & !RESET;
```

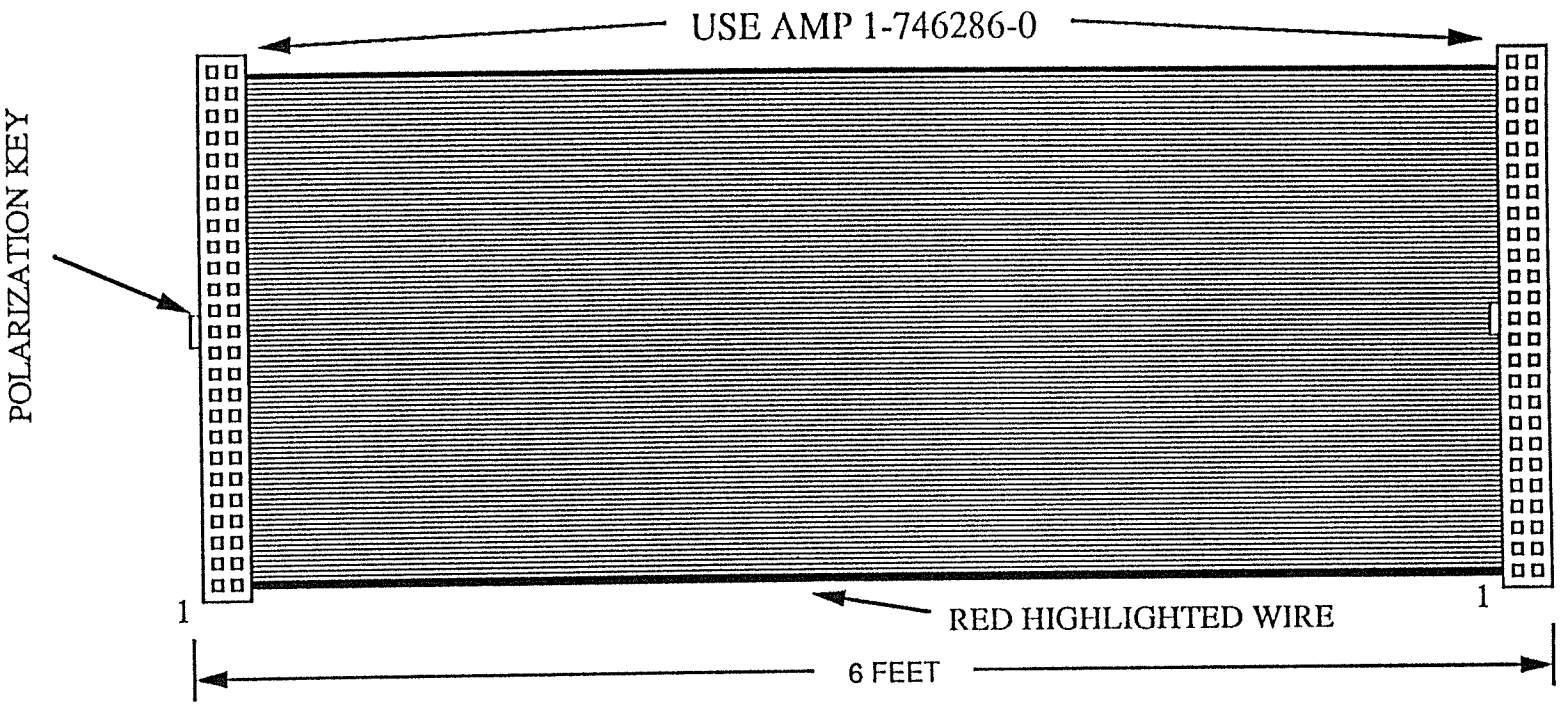
```
Name        N42802B ;
Partno      N42802B ;
Revision    B;
Date        27 Feb 90;
Designer    Kim Rubin;
Company     GREENSPRING COMPUTERS, INC.;
Assembly    IP OPTO INPUT;
Location    U3;
Device      EP600;
Format      j;

/*  COPYRIGHT 1990, GREENSPING COMPUTERS, INC.  */

/*****************************************************************************/
/*                                                                           */
/*      Allowable Devices: EPLD Altera EP610 only.                           */
/*                                                                           */
/*****************************************************************************/

/**  Inputs  **/

Pin     1       =       CLK1;           /* 8 MHz inverted from Logic Inter.  */
Pin     2       =       !WRITE;         /* Write Strobe from control PAL     */
Pin     3       =       D0;             /* Data Line I/O from Logic Interf.  */
Pin     4       =       D1;             /* Data Line I/O from Logic Interf.  */
Pin     5       =       A1;             /* Address Line from Logic Interf.   */
Pin     6       =       A2;             /* Address Line from Logic Interf.   */
Pin     7       =       A3;             /* Address Line from Logic Interf.   */
Pin     8       =       !READ;          /* Read Stobe from control PAL       */
Pin     11      =       !IN0;           /* Input from Opto, Debounce, Sync.  */
Pin     14      =       !IN1;           /* Input from Opto, Debounce, Sync.  */
Pin     23      =       !RESET;         /* From Logic Interface              */
Pin     13      =       CLK2;           /* same as pin 1                     */


/**  Outputs  **/

Pin     22      =       DELAY0;         /* IN0 delayed                       */
Pin     21      =       DELAY1;         /* IN1 delayed                       */
Pin     20      =       INT0;           /* Interrupt Request Latch           */
Pin     19      =       INT1;           /* Interrupt Request Latch           */
Pin     18      =       MASK0;          /* Mask Register                     */
Pin     17      =       MASK1;          /* Mask Register                     */
Pin     16      =       POL0;           /* Polarity Register                 */
Pin     15      =       POL1;           /* Polarity Register                 */
Pin     10      =       !IRQ;           /* Interrupt Request out             */
Pin     9       =       orterm;         /* used internally                   */

/**  Declarations and intermediate equations  **/

Data            =       !A1 & !A2 & !A3;
PolReg          =        A1 & !A2 & !A3;
MaskReg         =       !A1 &  A2 & !A3;
ClearReg        =        A1 &  A2 & !A3;
IntReg          =       !A1 & !A2 &  A3;
ClearAll        =        A1 &  A2 &  A3;

/*****************************************************************************/
/*                      ADDRESS MAP                                          */
/*                                                                           */
/*  Data                        Read    base + $1                            */
/*  Interrupt Polarity Register R/W     base + $3                            */
/*  Interrupt Disable Register  R/W     base + $5                            */
/*  Clear Interrupts            Write   base + $7                            */
/*  Pending Interrupt Register  Read    base + $9                            */
/*  Vector Register             R/W     base + $B                            */
```

```
/*                                                                          */
/*                      NOTES                                               */
/*  Data polarity at IN pin is reversed because input current causes a      */
/*  logic low.  When reading the data register a 1 indicates input current. */
/*  A 1 in the Polarity register means respond to rising edges.             */
/*  A 1 in the Int. Disable Register means do not interrupt on that bit.    */
/*  The Int. Disable Register is cleared to FF.                             */
/*  Writing a 1 to any bit in the Clear Interrupts Reg clears that bit      */
/*  in the Pending Int. Reg.                                                */
/*  A bit is set in the Pending Interrupt Reg even if the interrupt is      */
/*  masked off.                                                             */
/*                                                                          */
/*  Rev A       2/27/90 XKR Turbo bit must be set for parts to work.        */
/*  Rev B       2/27/90 XKR Turbo bit off for EP610 parts.                  */
/*                                                                          */
/**************************************************************************/

FUSE (6480,0);  /* Turbo Bit OFF */
FUSE (6481,0);  /* Turbo Bit OFF */


/** Logic equations **/

/* Inputs are synchronized.  The two DELAY latches are used to
   deatect leading and trailing edges.
*/
DELAY0.d        =       IN0;

DELAY1.d        =       IN1;

/* The first line detects leading edges, the second trailing edges,
   the third and fourth detect virtual edges if the polarity register
   is changed.  The fifth line latches until cleared.  The .ar term
   performs normal reset on either clear interrupt write or clear all.
*/
INT0.d          =        POL0 & !DELAY0 &  IN0 & !INT0
                P       !POL0 &  DELAY0 & !IN0 & !INT0
                P       PolReg & WRITE &  D0 &  DELAY0 & !POL0 & !INT0
                P       PolReg & WRITE & !D0 & !DELAY0 &  POL0 & !INT0
                P       !RESET & INT0;

INT0.ar         =       A1 & A2 & WRITE & D0;

INT1.d          =        POL1 & !DELAY1 &  IN1 & !INT1
                P       !POL1 &  DELAY1 & !IN1 & !INT1
                P       PolReg & WRITE &  D1 &  DELAY1 & !POL1 & !INT1
                P       PolReg & WRITE & !D1 & !DELAY1 &  POL1 & !INT1
                P       !RESET & INT1;

INT1.ar         =       A1 & A2 & WRITE & D1;

/*  The mask and polarity registers are set to FF on RESET.
*/
MASK0.d         =       MaskReg & WRITE & D0
                P       !(MaskReg & WRITE) & MASK0
                P       ClearAll & WRITE
                P       RESET;

MASK1.d         =       MaskReg & WRITE & D1
                P       !(MaskReg & WRITE) & MASK1
                P       ClearAll & WRITE
                P       RESET;

POL0.d          =       PolReg & WRITE & D0
                P       !(PolReg & WRITE) & POL0
                P       ClearAll & WRITE
```

```
                P       RESET;

POL1.d          =       PolReg & WRITE & D1
                P       !(PolReg & WRITE) & POL1
                P       ClearAll & WRITE
                P       RESET;

/* D0 is a data line out.  The equations below act as a simple mux
   to read one of three internal registers, or the data input.
*/
D0              =       Data & IN0
                P       PolReg & POL0
                P       MaskReg & MASK0
                P       IntReg & INT0;

D1              =       Data & IN1
                P       PolReg & POL1
                P       MaskReg & MASK1
                P       IntReg & INT1;

D0.oe           =       READ;

D1.oe           =       READ;

/*  orterm is needed because we cannot
    use OR gates in .oe equations.  A 0 in the mask reg. enables.
*/
orterm          =       INT0 & !MASK0
                P       INT1 & !MASK1;

/* IRQ is "open collector".
*/
IRQ             =       'b'1;

IRQ.oe          =       orterm;


/**  Fixup equations  **/

DELAY0.ar       =       'b'0;
DELAY1.ar       =       'b'0;
MASK0.ar        =       'b'0;
MASK1.ar        =       'b'0;
POL0.ar         =       'b'0;
POL1.ar         =       'b'0;
```

REVISIONS

ECO #	DESCRIPTION	DATE
	RELEASE TO PRODUCTION	April 24, 1990



Hall A

Kit includes:

1: 6' Data cable (3005051650)
2: Terminal Block (3009001050)
3: Data sheet reprint ILQ2
4: Data sheet reprint MC14490
5: Technical documentation

GREENSPRING COMPUTERS, INC.		
ENGINEERING KIT		DRAWN BY Fred Trevor
IP-OPTO INTERRUPTER		
REV A	April 24, 1990	SHEET 1 of 1